Application Note AN-90
TinySwitch-III Family

Design Guide

Introduction

The TinySwitch™-III family of ICs are a highly integrated monolithic off-line switcher IC designed for power supplies with scalable outputs up to 28.5 W for universal input voltage range (85 VAC – 265 VAC) and 36.5 W for high-line input (230 VAC). Example applications include PC standby and auxiliary supplies, DVD and other low power set-top decoders, chargers/adapters and bias supplies for appliances and industrial power sub-system including metering and controls. Innovative features such as on-time extension, latching output overvoltage shutdown, selectable current limit, thermal shutdown and line undervoltage greatly simplifies the design, reducing engineering design time and system cost while providing complete system level of protection.

The ICs combine a high-voltage (700 V) power MOSFET switch with an ON/OFF controller in one device. The simple ON/OFF control doesn't need a compensation loop and provides constant efficiency down to very light load conditions. Internal start-up current is drawn from the DRAIN pin, eliminating the need for external start-up components. Additional features such as selectable current limit for design flexibility, jittered switching frequency for low EMI, and line undervoltage lockout to prevent the output glitches during power up and down. Safety and reliability features include auto-restart to limit device and overall circuit dissipation during overload, output short-circuit and open-loop conditions, latching output overvoltage shutdown to protect the load, and hysteretic over-temperature protection to disable the supply during a thermal fault. On-time extension improves power delivery at low-line as well as the hold-up time.

EcoSmart™ technology enables designs to easily attain <150 mW no-load consumption without bias winding or <30 mW with the bias winding, both measured at 265 VAC input voltage. Together with the flat efficiency characteristics vs. load, this makes meeting energy efficiency standards straightforward, including programs from Energy Star and California Energy Commission.

The design of flyback power supplies involves a highly iterative process with several variables that have to be considered and adjusted to optimize the design. The design methodology described in this document consists of four parts, a quick start guideline which utilize the Power Integrations design software, a simplified step-by-step design procedure, application example and an in-depth information section. The quick start, in which the engineer may opt to rapidly design the transformer and select the components. The step-by-step design procedure is a design method at which at the implementation level, guides the engineer from a set of given system requirements all the way to the completion of the desired flyback power supply using TinySwitch-III devices. This also includes look up tables and a simple spreadsheet program that is also from the PI Expert™ software. In addition, part of this section discuss design recommendation, guidelines and considerations, such as component selection, PCB layout design and etc. A brief description of the device features and functionality was also specified. The application example, describes an actual reference design using a TinySwitch-III device indicating the operation, its performance data and waveforms. The in-depth information section, makes available the key background information for the design method, such as equations, design guidelines and best practices. Cross references are provided among the three which allow the reader to switch among conceptual, implementation and optimization levels at any given stage for an in-depth understanding and further optimization.

Features	TinySwitch-II	TinySwitch-III	TinySwitch-4
BV_{DSS}, Breakdown Voltage	650 V	700 V	725 V
Line Undervoltage Protection	N/A	Yes	Yes
Line Compensated OCP	N/A	N/A	Yes
I_{LUV}, EN/UV Pin Line Undervoltage Threshold	N/A	25 µA ± 10%	25 µA ± 5%
$V_{BP/M(RESET)}$, BP/M Pin Power-Up Reset Threshold Voltage	2.6 V Typical	2.6 V Typical	3.0 V Typical
Surface Mount	Yes	Yes	Yes
Packages	DIP-8C SO-8C	DIP-8C SMD-8C	SO-8 DIP-8C/SMD-8C eSOP-12

Table 1. Features Comparison of TinySwitch Family of Devices.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a flyback power supply designed using TinySwitch-III. Because of the high level integration of TinySwitch-III, flyback power supply design is greatly simplified and fewer design change are left to be addressed externally, resulting in one common circuit configuration for all applications. For example, different output power levels may require values for some circuit components, but the circuit configuration stays unchanged. Application specific issues outside this basic configuration such as constant current, constant power outputs are beyond the scope of this document.

In addition to this application note, the reader may also find the TinySwitch-III Design Examples (DER) as an example of a working power supply. The Reference Design Kit of TinySwitch-4, its design process and recommendations are also applicable to TinySwitch-III family of devices and vice versa, provided that the engineers are well aware and should take note the differences between the two families such as the maximum drain voltage rating, features and device tolerances. Further details on downloading PI Expert, obtaining of DER, RDK and updates to this documents can be found at www.power.com.
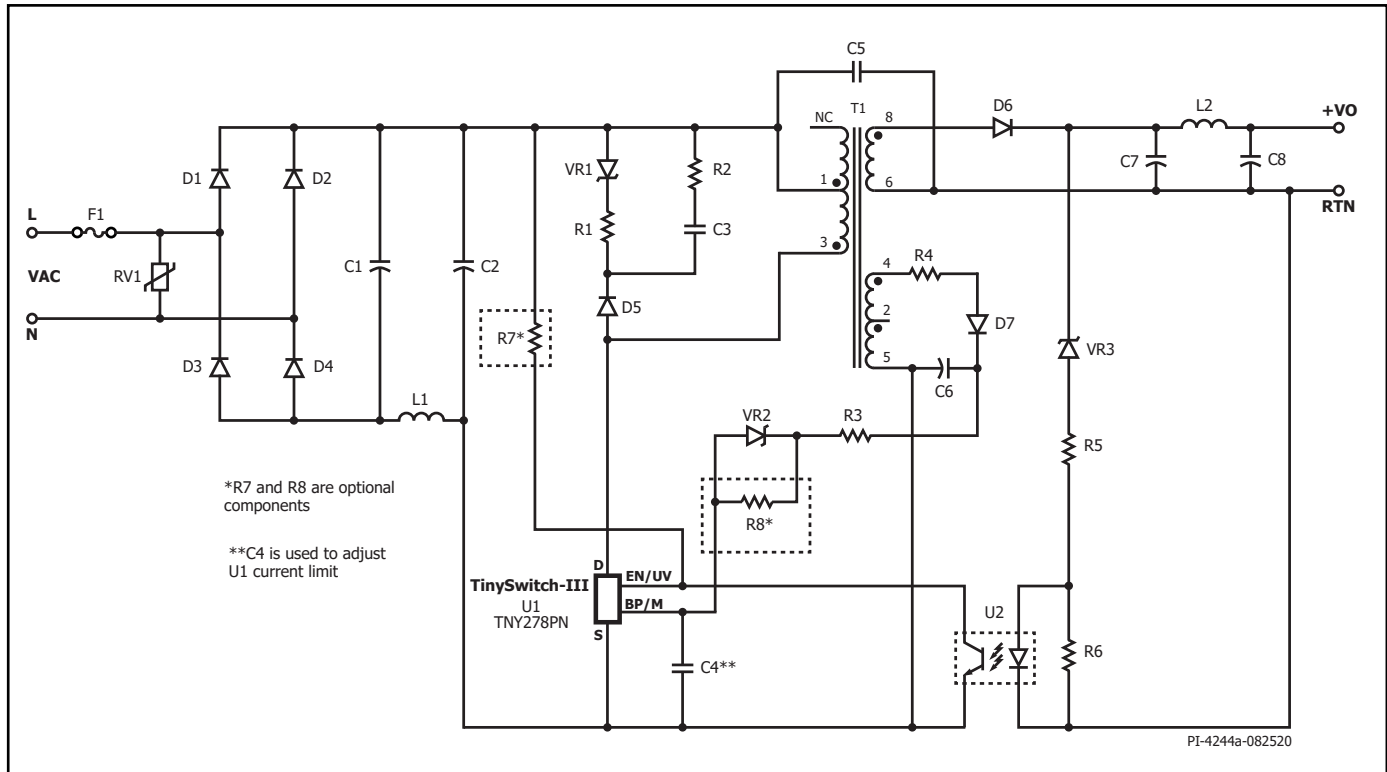

Figure 1. Typical Flyback Power Supply Schematic using TinySwitch-III with Line Undervoltage Lockout and the PI Proprietary Output Overvoltage Detection.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply or charger using TinySwitch-III family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To help simplify the task, this application note refers directly to the PIXls designer spreadsheet that is part of the PI Expert design software suite available online (https://piexpertonline.power.com/site/login).

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach described later, and can use the following information to quickly design the transformer and select the components for a first prototype. For this approach, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet line numbers are provided in square brackets [line reference].

- Enter AC input voltage range VACMIN [B3], VACMAX [B4] and minimum line frequency fL [B5]
- Enter nominal output voltage VO [B6]
- Enter continuous output current IO [B7]
- Enter estimated efficiency, η [B9]
  - 0.8 for universal input voltage (85-265 VAC) or single 100/115 VAC (85 – 132 VAC) and 0.85 for a single 230 VAC (185 – 265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype board at peak load and VAC$_{MIN}$.
- Enter loss allocation factor Z [B10]
  - 0.5 for typical application. Adjust the number accordingly after the first prototype-board evaluation.
- Enter Bridge Rectifier Conduction Time estimate tC [B11]
  - The conduction time, tC is usually set at 3 ms and can be verified by direct measurement.
- Enter input capacitance CIN [B12]
  - 2-3 μF/W for universal (85 – 265 VAC) or single (100/115 VAC) line input.
  - 1 μF for single 230 VAC (185-265 VAC) line input. If this cell is left blank, then the capacitance value for a VMIN of 70 VDC (universal input) or 150 VDC (single 230 VAC) is calculated. Often this will lead to an optimal input filter capacitance value.
- Select TinySwitch-III IC from the drop-down list or enter directly [B15]
  - Select the device from Table 1 according to output power, input voltage and application.
- Select configuration for current limit mode [B17]
  - Three current limit configurations are available, REDUCED, STANDARD or INCREASED.
- Enter the desired reflected output voltage, VOR [B23]
  - A good starting value for VOR is to set it within the range of 90 V – 110 V.
- Enter the TinySwitch-III IC on-state Drain to Source Voltage, VDS [B24]
  - The default value given is 10 V. If no available value given in MOSFET data sheet, typical setting of VDS during on-state is 10 V.
- Enter the Output Winding Diode Forward Voltage Drop, VD [B25]
  - VD is typically set at 0.7 V.
- Enter the desired Bias Winding Voltage, VB [B30]
  - Typically, the default value given in the spreadsheet is 22 V as this gives the optimized performance on OVP setting.
- Enter Bias Winding Diode Forward Voltage Drop, VDB [B31]
  - Typically set at 0.7 V.
- Enter the desired Over Voltage Protection Zener Diode Voltage, VZOV [B33]
  - Typically set 6 V above the bias winding voltage.
- Enter the desired DC under-voltage threshold target, above which the power supply will start, V_UV_TARGET [B36]
  - The V_UV_ACTUAL [B37] indicated the actual DC start-up voltage based on the standard value of RUV_ACTUAL [B39]. V_UV_TARGET can be verified by direct measurement and can be adjusted based on the design requirements.
- Enter the closest standard value resistor RUV_ACTUAL to RUV_IDEAL [B39]
- Enter core type (if desired), Core Type [B42] from drop-down menu.
  - Suggested core size will be selected automatically if none is entered [B42]
  - AE [B45], LE [B46], AL [B47], BW [B48] are automatically reflected based on the selected core type.
  - For custom core, enter the core parameters from [B45] to [B48]

- Enter the desired Safety Margin Width, M [B49]
  - The default margin in the spreadsheet is 0 mm, assuming that a triple insulated wire will be used for secondary windings.
  - If triple insulated wire is not used at the secondary winding, the value that should be entered for safety margin M is 3.1 mm, half of the required safety margin of 6.2 mm. This is the typical margin for universal input (85 – 265 VAC).
- Enter number of primary layers (if desired), L [B50]
  - The default number of primary layers reflected in the spreadsheet is 3.
- Enter secondary number of turns, NS [B51]
  - If the grey override cell is left blank, the spreadsheet will automatically calculate the secondary number of turns.
- Enter the Minimum DC Input Voltage, VMIN [B54]
  - If the requirement of the power supply main input is from a DC Source, enter the minimum DC input voltage requirements.
  - If the grey override cell is left blank, the reflected value is automatically calculated by the spreadsheet based on the minimum AC input voltage requirement, output power, efficiency and bridge rectifier conduction time.
- Enter the Maximum DC Input Voltage, VMAX [B55]
  - If the requirement of the power supply main input is from a DC Source, enter the maximum DC input voltage require-ments.
  - If the grey override cell is left blank, the reflected value is automatically calculated by the spreadsheet based on the maximum AC input voltage requirement.
- Enter Primary Inductance Tolerance, LP_TOLERANCE [B66]
  - The default value given is 10%. If no available data from the supplier, typical setting is 10% to ensure manufacturability of the transformer.
- Enter the Maximum Primary Wire Diameter including insulation, OD [B74]
  - The value recommended is based on the given/calculated primary current. If desired to alter the value other parameters and ensure that no warnings are generated.

For multiple outputs design enter the following requirements under Transformer Secondary Design Parameters (Multiple Outputs):

1st Output
(If unused, the defaults are from the single output design)
- Enter the Main Output Voltage, VO1 [B95]
- Enter the Main Output DC Current, IO1 [B96]
- Enter the output diode voltage drop, VD1 [B98]

2nd Output
(If unused, leaved the section blank)
- Enter the 2nd Output Voltage, VO2 [B110]
- Enter the 2nd Output DC Current, IO2 [B111]
- Enter the output diode voltage drop for the 2nd output, VD2 [B113]

3rd Output
(If unused, leaved the section blank)
- Enter the 3rd Output Voltage, VO3 [B125]
- Enter the 3rd Output DC Current, IO3 [B126]
- Enter the output diode voltage drop for the 3rd output, VD3 [B128]

Negative Output
- If Negative Output exists enter the Output Number, Negative Output [B141]
Example: If VO2 is negative output, enter or choose 2 from the drop down selection.

If any warnings are generated, make changes to the design by following instructions in spreadsheet column D.
- Build transformer as suggested in "Transformer Construction" tab
- Select key components
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency, VMIN). Note that the initial efficiency estimate is very conservative.

Output Power Table

Products[3]	230 VAC ± 15%		85-265 VAC	
	Adapter[1]	Peak or Open Frame[2]	Adapter[1]	Peak or Open Frame[2]
TNY274P/G	6 W	11 W	5 W	8.5 W
TNY275P/G	8.5 W	15 W	6 W	11.5 W
TNY276P/G	10 W	19 W	7 W	15 W
TNY277P/G	13 W	23.5 W	8 W	18 W
TNY278P/G	16 W	28 W	10 W	21.5 W
TNY279P/G	18 W	32 W	12 W	25 W
TNY280P/G	20 W	36.5 W	14 W	28.5 W

Table 2.   TinySwitch-III Output Power Table.
Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 ºC ambient. Use of an external heat sink will increase power capability.
2. Minimum peak power capability in any design or minimum continuous power in an open frame design (see Key Applications Considerations).
3. Packages: P: DIP-8C, D: SO-8C, K: eSOP-12B.

Step-by-Step Design Procedure

This design procedure uses the PI Expert design software (available from Power Integrations), which automatically performs the key calculations required for the TinySwitch flyback power supply design. PI Expert allows designers to avoid the typical highly iterative design process. Look-up tables and empirical design guidelines are provided in this procedure where appropriate to facilitate the design task.

Iterate the design to eliminate warnings. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Once all warnings have been cleared, the output transformer design parameters can be used to create a prototype transformer.

Step 1 – Application Variables

Enter: VACMIN, VACMAX, fL, VO, IO, η, Z, and CIN
Minimum and Maximum Input Voltage, VACMIN [B3], VACMAX [B4]
Determine the input voltage range from Table 2 for a particular regional requirement. Enter the required VACMIN and VACMAX directly (see Figure 2 for reference).

Line Frequency, LINEFREQ (Hz) [B5]
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst-case or based on the product specification reduce these numbers by 6% (47 Hz or 56 Hz). Table 2 provides the line frequency reference for a given line input voltage and particular regional requirements.

Nominal Output Voltage, VO (V) [B6]
Enter the nominal output voltage of the main output current. Generally, the main output is the output from which the feedback is derived. And for multiple outputs, the output with the highest output power is commonly the main output.

Power Supply Output Current, IO (I) [B7]
Enter the maximum continuous output current of the power supply.

Continuous Output Power, Power (W) [B8]
This is automatically calculated value based on the Output Voltage and maximum continuous Output Current.

Power Supply Efficiency, η [B9]
Enter the estimated efficiency of the complete power supply measured from the input and output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 0.8 or 80%, typical for design where the majority of the output power is drawn from an output voltage of 12 V or greater and no current sensing is present on the secondary. Once a prototype has been constructed then the measured efficiency should be entered and further transformer iteration(s) can be performed if required.

Power Supply Allocation Factor, Z [B10]
This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc) are not processed by the power stage (transferred through the transformer) and therefore, although they reduced efficiency the transformer design is not affected.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

For the designs that do not have a peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement enter 0.65. The higher number indicates larger secondary side losses.

Bridge Rectifier Conduction Time, tC (ms) [B11]
Enter a bridge diode conduction time of 3.00 ms if there is no better data available.

Total Input Capacitance, CIN (μF) [B12]
Enter total input capacitance using Table 3 for guidance.

The capacitance is used to determine the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, VMIN > 70 VDC.

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For example, from Figure 2 the output power PO is calculated as 15 W. Using Table 3 with reference to Universal Input Voltage, the recommended Total Input Capacitance Value is 2 to 3 μF/W; therefore, the total input capacitance value should be in the range of 30 μF to 45 μF. Choose a capacitor value from this range that would provide a VMIN of greater than 70 VDC. Factor to consider in selecting the input capacitor are, capacitance value single or in parallel combination must be standard and it should provide a VMIN that could result in an optimized design of the transformer. Enter the value selected in CIN [B12] cell. As shown in Figure 2, the designer selects and enter 44 μF capacitor in [B12] cell. This gives a VMIN [B54] of 92.9 VDC which is automatically calculated by the spreadsheet. See Figure 3 for VMIN [B54] and VMAX [B55] values.

In-depth information provides the equation for calculating the minimum DC input voltage given the minimum AC input and the assumed bridge diode conduction time (tC).

For designs that have a DC rather than an AC input, the value of the minimum and maximum DC input voltages, VMIN and VMAX, may be entered into the grey override cells on the design spreadsheet as shown on Figure 3.

		INPUT	INFO	OUTPUT	UNIT	
1	ACDC_TinySwitch-III_032514; Rev.1.27; Copyright Power Integrations 2014					ACDC_TinySwitch-III_032514_Rev1-27.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
2	▼ENTER APPLICATION VARIABLES					Customer
3	VACMIN	85			Volts	Minimum AC Input Voltage
4	VACMAX	265			Volts	Maximum AC Input Voltage
5	fL	50			Hertz	AC Mains Frequency
6	VO	12.00			Volts	Output Voltage (at continuous power)
7	IO	1.25			Amps	Power Supply Output Current (corresponding to peak power)
8	Power			15	Watts	Continuous Output Power
9	n	0.82				Efficiency Estimate at output terminals. Under 0.7 if no better data available
10	Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
11	tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
12	CIN	44.00		44.00	uFarads	Input Capacitance

Figure 2.   Application Variables for TinySwitch-III Design Spreadsheet with Gray Override Cells.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	122	50 / 60
United States, Canada	120	90	132	60
Europe, Asia, Africa	115, 120, 127	90	155	50 / 60
Australia, Americas and rest of the world	220, 230 240	185 185	265 265	50 / 60 50

Table 3.   Standard Worldwide Input Line Voltage Ranges and Line Frequencies.

AC Input Voltage (VAC)	Total Input Capacitance per Watt Output Power (μF/W)	VMIN (V)
100 / 115	2 ~ 3	≥80
Universal	2 ~ 3	≥80
230	1	≥240

Table 4.   Recommended Total Input Capacitance for Different Input Voltage Ranges.

53	▼DC INPUT VOLTAGE PARAMETERS				
54	VMIN		92.90	Volts	Minimum DC Input Voltage
55	VMAX		374.77	Volts	Maximum DC Input Voltage

Figure 3.   DC Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.

Step 2 – Enter TinySwitch-III Variables: TinySwitch-III Device, Current Limit, VOR, VDS, VD

Figure 4 shows the variables for TinySwitch-III device.

Select the Correct TinySwitch-III Device [B15]
The default option is automatically selected based on input voltage range and maximum output power. Ensure that no 'Warning' is indicated and 'Info' shall be carefully review in the columns [D] and [F] before proceedings with the other design parameters. If Warning is displayed in the spreadsheet, choose a larger device to remove the warning.

For manual selection of device size, refer to the TinySwitch-III power table and select a device based on the peak output power design. Then compare the continuous power to adapter column numbers in the power table, (if the power supply is fully enclosed type, or compare to the open-frame column (if the power supply is an open-frame design). If the continuous power exceeds the value given in the power table (Table 1), then the next larger device should be selected. Similarly, if the continuous power is closed to the maximum adapter power given in the power table, it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

14	▼ENTER TinySwitch-III VARIABLES					
15	**TinySwitch-III**	TNY278P		TNY278P		User defined TinySwitch-III
16	Chosen Device		TNY278P			
17	Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
18	ILIMITMIN			0.512	Amps	Minimum Current Limit
19	ILIMITTYP			0.550	Amps	Typical Current Limit
20	ILIMITMAX			0.588	Amps	Maximum Current Limit
21	fSmin			124000	Hertz	Minimum Device Switching Frequency
22	I^2fmin			35.937	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
23	VOR	108.00		108.00	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
24	VDS			10.00	Volts	TinySwitch-III on-state Drain to Source Voltage
25	VD	0.55		0.55	Volts	Output Winding Diode Forward Voltage Drop
26	KP			0.64		Ripple to Peak Current Ratio (KP < 6)
27	KP_TRANSIENT			0.36		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25

Figure 4.   TinySwitch-III Variables Section of Design Spreadsheet.

Select the Current Limit Configuration [B17]
The value of the BYPASS/MULTI-FUNCTION pin capacitor determines the device current limit setting. TinySwitch-III allows the internal current limit to be selected between three levels, Standard Current Limit or I_{LIMIT}, Reduced Current Limit or $I_{LIMIT-1}$, Increased Current Limit or $I_{LIMIT+1}$. The choice can be selected in the spreadsheet by entering RED, STD or INC in cell [B17].

Selecting the correct current limit level depends on the thermal environment, the amount of board area or use of an external heat sink, and the average output power.

Selecting RED gives the lowest current limit and results in lowest device dissipation. This minimizes heat sinking needed even in high ambient conditions. An example where RED would be selected is in a sealed adapter with minimal heat sinking.

Selecting INC gives the highest current limit and therefore maximum power from a given device. This is ideal for open frame designs, adapters where an external heat sink is attached to the Source pins of the device.

Selecting STD is optimum for most applications, balancing heat dissipation and system efficiency.

Figure 5 shows the minimum practical power at three selectable current limits; $I_{LIMIT-1}$, I_{LIMIT} and $I_{LIMIT+1}$ corresponds for RED, STD and INC respectively. This serves as a guideline in choosing the TinySwitch-III device in reference with the power capability and input voltage.

In the given spreadsheet design, Figure 4 shows the selected device is TNY278P with standard [STD] current limit. The Current Limit tolerance of the selected device are reflected on [B18] as the

ILIMMIN or the minimum current limit, [B19] as the ILIMTYP or typical current limit and [B20] as the ILIMMAX or maximum current limit. This current limit tolerance of the selected device is important factor in determining the key parameters such as the minimum inductance, primary number of turns and maximum flux density.

Peak Output Power Table

Products	230 VAC ± 15%			85 −265 VAC		
	$I_{LIMIT-1}$	I_{LIMIT}	$I_{LIMIT+1}$	$I_{LIMIT-1}$	I_{LIMIT}	$I_{LIMIT+1}$
TNY274P	9.1 W	10.9 W	9.1 W	7.1 W	8.5 W	7.1 W
TNY275P	10.8 W	12 W	15.1 W	8.4 W	9.3 W	11.8 W
TNY276P	11.8 W	15.3 W	19.4 W	9.2 W	11.9 W	15.1 W
TNY277P	15.1 W	19.6 W	23.7 W	11.8 W	15.3 W	18.5 W
TNY278P	19.4 W	24 W	28 W	15.1 W	18.6 W	21.8 W
TNY279P	23.7 W	28.4 W	32.2 W	18.5 W	22 W	25.2 W
TNY280P	28 W	32.7 W	36.6 W	21.8 W	25.4 W	28.5 W

Figure 5.   Minimum Practical Power at Three Selectable Current Limit levels.

Minimum Switching Frequency, fS_{MIN} (Hz) [B21]
This parameter is the data sheet minimum switching frequency which is equivalent to 124 kHz.

Minimum Device Power Coefficient, I^2f_{MIN} (A²kHz) [B22]
This value is the minimum data sheet I^2f parameter for the selected device and current limit mode. The calculation for primary inductance is based on this value.

Reflected Output Voltage, VOR (V) [B23]

This parameter is the secondary winding voltage during the diode conduction time reflected back to the primary through the turns ratio of the transformer. The default value is 120 V and VOR can be adjusted to achieve a design that does not violate design rules, acceptable recommended maximum value is less than 135 V. Adjust VOR as necessary to ensure that no warnings in the spreadsheet are triggered. For design optimization purposes, the following factors should be considered.

- Higher VOR reduces the voltage stress on the output diodes, which in some cases may allow a lower voltage rating for higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary-side which may increase secondary-side copper wire size and diode losses thereby reduces efficiency.
- Another important consideration in selecting the desired VOR is the maximum drain voltage de-rating. In the design, the typical drain voltage de-rating is set less than 90% of BV_{DSS}. Table 4 below shows a recommended VOR versus output power at an estimated efficiency of >80%. Optimization can be done after building the first prototype and evaluation.

Output Power	Input Voltage (VAC)	Recommended VOR Starting Point Value	Recommended VOR Range
POUT < 20 W	85 − 265	100 V	90 V − 120 V
20 W < POUT < 28 W	85 − 265	110 V	100 V − 120 V
POUT ≥ 30 W	230 VAC	120 V	110 V − 130 V

Table 5.   VOR Recommendation vs. Output Power.

On-State Drain to Source Voltage, VDS (V) [B24]

This is the assumed Drain to Source voltage drop when MOSFET is on. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, VD (V) [B25]

Enter the average forward voltage drop of the main output diode. Use 0.5 V for a Schottky diode or 0.7 V for PN diode, if no better data is available. By default, a value of 0.7 V is assumed.

Ripple to Peak Current Ratio, KP (STEADYSTATE) [B26] and KP_TRANSIENT [B27]

KP is a measure of how continuous or discontinuous the mode of operation is. These parameters are automatically calculated in the spreadsheet.
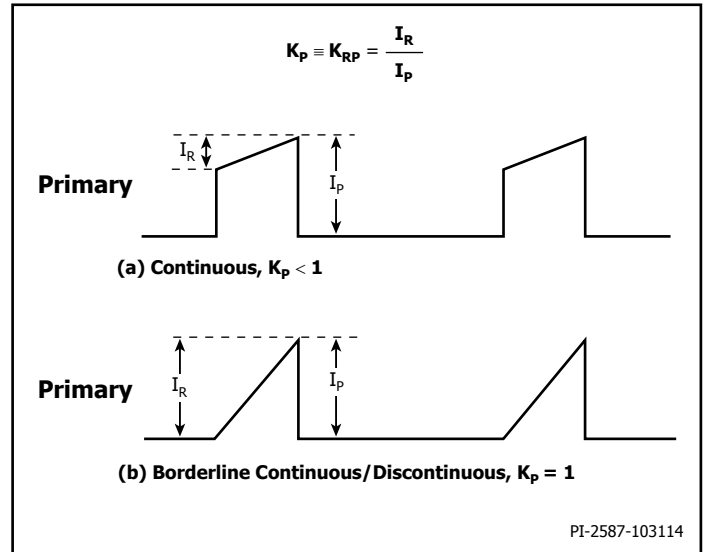

Figure 6.   Continuous Mode Current Waveform, K_p < 1.

K_p < 1 indicating continuous conduction mode or CCM operation. K_p is the ratio of ripple to peak primary current (Figure 6).

K_p > 1 indicating discontinuous mode or DCM operation (Figure 7).

K_p is the ratio of primary MOSFET off-time to the secondary diode conduction time.

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

$$K_P \equiv K_{DP} = \frac{(1 - D) \times T}{t}$$
$$= \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

The value of K_p should be in the range of 0.25 < K_p < 6, and guidance is given in the comments cell if the value is outside this range.

KP (STEADYSTATE) is the calculated K_p value under the condition where several switching cycles have occurred consecutively.

KP (TRANSIENT) is the calculated minimum KP value that occurs after a switching cycle has been skipped. As the drain current starts from zero, ramping to current limit, the on-time for this cycle is much longer than during steady-state. This reduces the off-time, lowering the time for the magnetizing inductance to reset and causing the next cycle to start with a much higher initial current, lower ripple current and lower value of KP. It should be above a value of 0.25 to prevent the large initial current pedestal from falsely triggering the current limit at the end of the leading edge blanking time and limiting power delivery.
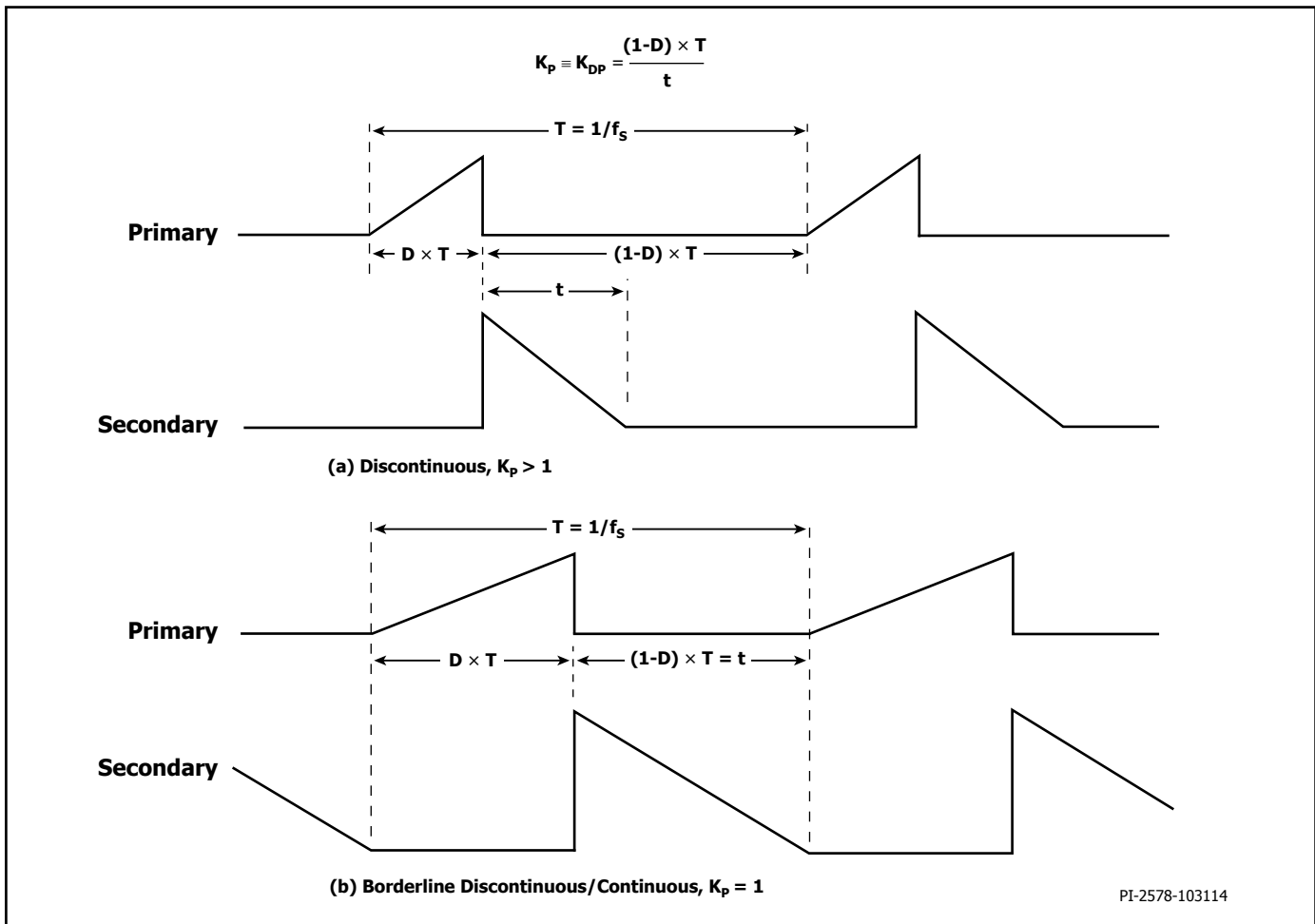
$$K_P \equiv K_{DP} = \frac{(1-D) \times T}{t}$$

T = 1/f$_S$

Primary

D × T   **(1-D) × T**

t

Secondary

(a) Discontinuous, K$_P$ > 1

T = 1/f$_S$

Primary

D × T   **(1-D) × T = t**

Secondary

(b) Borderline Discontinuous/Continuous, K$_P$ = 1

PI-2578-103114

Figure 7.   Discontinuous Mode Current Waveform, KP > 1.

Step 3 – Choose Bias Winding Voltage, VB (V) [B30]

By the default, if the grey override cell is left empty, a value of 22 V is assumed. The user can override this value as needed; a value in the range 15 V – 30 V is recommended. The value must ensure an adequate headroom for supplying the current into the BYPASS/ MULTI-FUNCTIONAL pin and to limit no-load input power due to bias winding power consumption. The number of bias winding turns, NB, is used for transformer construction, and an ultra-fast diode (such as BAV19WS, BAV20WS and UF4003 diodes are ideal) with a voltage rating above PIVB value should be selected.

The **VZOV value** is an estimate for the Zener diode voltage rating used for output overvoltage protection. When the Zener diode conducts and exceeds the shutdown threshold current (I_{SD}) of 6.5 mA into the BYPASS/MULTI-FUNCTIONAL pin, the latching shutdown feature of TinySwitch-III is triggered, and the power supply latches off. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or the OVP Zener (VR2) as shown in Figure 1. The resistor (R3) in series with the OVP Zener also limits the maximum current into the BYPASS/MULTI-FUNCTIONAL pin.

NB or the bias winding [B32] is calculated based on the desired secondary number of turns NS and the bias winding voltage VB.

The Zener diode voltage (VZOV) [B33] to be selected is approximately 6 V above the bias winding voltage VB. This value gives good OVP performance taking into account the variations in leakage inductance.

Figure 8 shows the bias winding variables from the spreadsheet.

Step 4 – Enter Under Voltage Lock Out (UVLO) Variables, V_UV_TARGET (V) [B36]

The line undervoltage lockout feature of TinySwitch-III defines the startup voltage of the supply. This prevents the power supply output from glitching when the input voltage is below the normal operating range. Connecting a resistor from an input capacitor to the EN/UV pin enables this feature. V_UV_TARGET is automatically calculated by the spreadsheet, but the designer may enter the desired DC voltage across the input capacitor at which the power supply should operate. The spreadsheet calculates both the ideal resistor value (RUV_IDEAL, [B38]), the closest preferred value (RUV_ACTUAL, [B39]) and its actual undervoltage (UV_ACTUAL, [B37]) setting. The resistor voltage rating (or sum of ratings if two or three resistors are used) should exceed VMAX. Figure 9 shows the undervoltage variables section from the spreadsheet.

The undervoltage threshold also resets the output overvoltage latching shutdown. After AC removal, once the voltage of the DC bus falls below the undervoltage threshold, the OV latch is reset.

Step 5 – Transformer Core/Construction Variables

Core Type [B42]

By default, if the core type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous (average) output power specified. Different core types and sizes from the drop-down list are available to choose from if a user-preferred core is not available, the grey override cells **(AE, LE, AL, BW)** can be used to enter the core and bobbin parameter directly by user. This is useful if a core is selected that is not on the list, or the specific core or bobbin information differs from that recalled by the spreadsheet. Refer to Figure 10 for transformer core

and construction variables from the spreadsheet. And Table 5 are the recommended and typically used core type with different output power levels at 132 kHz switching frequency of operation of the power supply

Where,

AE, Core Effective Cross Sectional Area (cm^2)
LE, Core Effective Path Length (cm)
AL, Ungapped Core Effective Inductance (nH/T^2)
BW, Bobbin Physical Winding Width (mm)

29	▼ENTER BIAS WINDING VARIABLES					
30	VB	11.00		11.00	Volts	Bias Winding Voltage
31	VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
32	NB			5.26		Bias Winding Number of Turns
33	VZOV			17.00	Volts	Over Voltage Protection zener diode voltage.

Figure 8. Bias Winding Variables of Design Spreadsheet.

35	▼UVLO VARIABLES					
36	V_UV_TARGET			102.19	Volts	Target DC under-voltage threshold, above which the power supply with start
37	V_UV_ACTUAL			99.70	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
38	RUV_IDEAL			4.00	Mohms	Calculated value for UV Lockout resistor
39	RUV_ACTUAL			3.90	Mohms	Closest standard value of resistor to RUV_IDEAL

Figure 9. Transformer Core and Construction Variables Section of Design Spreadsheet

41	▼ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
42	Core Type	EE25		EE25		Enter Transformer Core
43	Core		EE25		P/N:	PC40EE25-Z
44	Bobbin			EE25_BOBBIN	P/N:	EE25_BOBBIN
45	AE			0.40	cm^2	Core Effective Cross Sectional Area
46	LE			7.34	cm	Core Effective Path Length
47	AL			1420.00	nH/T^2	Ungapped Core Effective Inductance
48	BW			10.20	mm	Bobbin Physical Winding Width
49	M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
50	L	2.00		2.00		Number of Primary Layers
51	NS			6		Number of Secondary Turns

Figure 10. Transformer Core and Construction Variables Section of Design Spreadsheet

Output Power at 132 kHz	Core Table	
	Triple Insulated Wire	**Margin Wound**
0 – 10 W	EF12.6 EE13 EF16 EE16	EI22 EE19 EI22/19/6 EEL16
10 – 20 W	EE19 EI22 EI22/19/6 EF20	EF20 EI25 EEL19
20 – 30 W		EI28
30 – 50 W	EF25	EEL22

Table 6. Commonly Available Cores and Power Levels at Which Cores can be used for Typical Designs.

Safety Margin, M (mm) [B49]

For designs that require isolation but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically, many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin datasheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required. As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire.

Primary Layers, L [B50]

By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of $1 < L < 3$, and in general it should be the lowest number that meets the primary current density limit (CMA) of 200 Cmils/Amp. Values above 3 layers are possible, but the increase leakage inductance and physical fit of the windings should be considered. Due to the high switching frequency of TinySwitch-III designs, it is important to minimize transformer leakage inductance. A split primary construction may be helpful for designs where primary clamp dissipation is unacceptably high. Here half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich management.

The value of KP should be in the range of $0.25 < KP < 6$, and guidance is given in the comments cell if the value is outside this range.

Secondary Turns, NS [B51]

By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density BM is kept below the recommended maximum of 3000 Gauss (300mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of BM limits).

If the engineer desired to iterate the secondary number of turns, a good assumption is by using 1 turn/volt for 100/115 VAC and 0.6 turn/volt for 230 VAC or universal inputs.

Step 6 – Iterate Transformer Design and Generate Initial Design

Iterate the design making sure that no 'Warnings' are displayed and 'Info' shall be review by the engineer (both are indicated in column D and F). Any parameters outside the recommended range of values can be corrected by following the guidance in the right-hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or sent to a vendor for samples. Figure 13 is the section from the spreadsheet for transformer primary design parameters..

DC Input Voltage Parameters, [B54] – [B55]

See Figure 3 for reference.

Minimum DC Input Voltage, VMIN [B54]

VMIN is the minimum DC input voltage and it is dependent on the AC input voltage, bridge rectifier, output power, efficiency and energy storage capacitor. This is automatically calculated value on the spreadsheet based on the entered minimum AC input voltage. If the power supply requirements input voltage is DC, the designer may enter the required minimum DC input voltage.

Maximum DC Input Voltage, VMAX [B55]

VMAX is the maximum DC input voltage and it is simply the peak value of the highest AC input voltage VACMAX. This is automatically calculated value on the spreadsheet based on the entered maximum AC input voltage. If the power supply requirements input voltage is DC, the designer may enter the required maximum DC input voltage.

Current Waveform Shape Parameters, [B58] – [B62]

These are key parameters of the primary block of the flyback power supply that are automatically calculated by the spreadsheet. Figure 12 displays the section in the spreadsheet for current waveform shape parameters.

Maximum Duty Ratio, DMAX [B58]

Calculated at full load and at minimum input voltage. DMAX is a factor in calculating the required minimum primary inductance and dependent on the reflected voltage and calculated or entered minimum DC input voltage.

Average Primary Current, IAVG [B59]

Calculated based on the ripple factor KP, the maximum duty ratio DMAX and ILIMIT of the TinySwitch-III device given in the datacsheet.

Minimum Peak Primary Current, IP [B60]

Automatically calculated parameters and used for the calculation of the required minimum inductance.

Primary Ripple Current, IR [B61]

Identify the current wave shape slope based on the calculated ripple factor and the given peak primary current.

Primary RMS Current, IRMS [B62]

For sizing of primary winding wire gauge and power loss calculation.

Key Transformer Electrical Parameters [B65] – [B79]

Figure 14 shows the section in the spreadsheet for transformer primary design parameters. All are automatically calculated by the spreadsheet except for primary inductance tolerance (LP_TOLERANCE [B66]). A default value of 10% is specified on LP_TOLERANCE, but the user can alter the value if desired or if there's available data from the transformer supplier. And for maximum primary wire diameter (OD, [B74]), this can be change in the grey override cell if specific information is known.

Primary Inductance, LP (µH) [B65]

This is the target nominal primary inductance of the transformer and it is automatically calculated by the spreadsheet. This is with a 10% margin given in the primary inductance tolerance to meet the required minimum primary inductance value.

Primary Inductance Tolerance, LP_TOLERANCE (%) [B66]

This is the assumed primary inductance tolerance. A value of 10% is used by default; however, if specific information is known from the transformer vendor, then this may be entered in the grey override cell. This is also a factor in the calculated value of primary inductance.

Number of Primary Turns, NP [B67]

The total number of primary turns is automatically calculated parameter. The number of primary turns is calculated such that the maximum operating flux density BM is kept below the recommended maximum of 3000 Gauss. For low leakage inductance applications, a split primary construction may be used.

Gapped core effective inductance, ALG (nH/t²) [B68]
Used by the transformer vendor to specify the core gap.

Maximum Operating Flux Density, BM (Gauss) [B69]
The maximum operating flux density is a calculated parameter. A maximum value of 3000 Gauss during normal operation is recommended to limit the maximum flux density under start-up and output short-circuit. Under these conditions the output voltage is low, and little reset of the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device, together with the built-in protection features of TinySwitch-III, provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

The cycle skipping mode of operation used in TinySwitch-III can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitors having a different dielectric, for example a polyester film type.

Maximum Primary Wire Diameter, OD (mm) [B74]
By default, if the override cell is empty, double insulated wire is assumed, and the standard wire diameter is chosen. The grey override cells can be used to enter the wire diameter directly by the user if the wire used is different from the standard double coated/heavy nyleze types.

The other transformer electrical parameters that are automatically calculated by the spreadsheet includes:

AC Flux Density for Core Loss Curves, BAC [B70]
The calculated value is use in estimating the power loss of the core.

Relative Permeability of Ungapped Core, ur [B71]
The relative permeability is a constant parameter.

Gap Length, LG [B72]
The recommended gap length must be greater than 0.1 mm for manufacturability.

Effective Bobbin Width, BWE [B73]
The effective bobbin width is a given parameter from the selected core bobbin.

Estimated Total Insulation Thickness, INS [B75]
Used in the selection of the wire gauge.

Bare Conductor Diameter, DIA [B76]
Used to identify the primary wire gauge the could handle the primary current.

Primary Wire Gauge, AWG [B77]
This is rounded to the next smaller standard AWG value.

Bare Conductor Effective Area in Circular Mils, CM [B78]
To identify the current capacity for the primary windings.

Primary Winding Current Capacity, CMA [B79]
The recommended primary winding current capacity must be, 200 < CMA < 500.

To aid the designer in optimizing the transformer design, Figure 11 shows the relationship between the parameters that are indicated when they are varied.

		B_M	L_G	CMA
L	↑	-	-	↑
N_S	↑	↓	↑	↓
Core Size	↑	↓	↑	↑

Figure 11.   Transformer Parameters Relationship.

Where:
↑, indicates the value Increases.
↓, indicates the value Decreases.
-, indicates No Change.

Key Transformer Secondary Design Parameters That Are Automatically Calculated: [B83] − [B87]
Figure 14 is the section from the spreadsheet that display the transformer secondary design parameters.

Peak Secondary Current, ISP [B87]
Used to determine the secondary RMS current and ESR requirement for the output capacitor.

Secondary RMS Current, ISRMS [B84]
The calculated value is use for the selection wire size for the secondary winding which is also calculated in the spreadsheet and for the selection of output capacitor ripple current rating.

Output Capacitor RMS Ripple Current, IRIPPLE [B85]
Used in the selection of output capacitor.

Secondary Bare Conductor Minimum Circular Mils, CMS [B86]
To identify the wire current capacity for the secondary windings.

Secondary Wire Gauge, AWGS [B87]
This parameter is rounded up to the next larger standard AWG value. A larger wire diameter is necessary to maintain transformer temperature within acceptable limits during continuous short-circuit conditions.

Voltage Stress Parameters [B90] − [B91]
Figure 15 shows the voltage stress parameters on primary MOSFET and secondary output diode, which are both automatically calculated.

Maximum Drain Voltage Estimate, VDRAIN [B90]
The reflected maximum drain voltage or VDRAIN in the spreadsheet will provide the proper selection of the MOSFET. For derating purposes, the calculated value should be at least 80% to 90% of the maximum Drain voltage of TinySwitch-III which is 700 V.

Output Rectifier Maximum Peak Inverse Voltage, PIVS [B91]
The PIV of the secondary rectifier reflected in the spreadsheet will provide the proper selection of the output diode. For derating purposes, the calculated value should be at least 80% to 90% of the selected diode maximum reverse voltage.

57	▼CURRENT WAVEFORM SHAPE PARAMETERS				
58	DMAX		0.59		Duty Ratio at full load, minimum primary inductance and minimum input voltage
59	IAVG		0.22	Amps	Average Primary Current
60	IP		0.51	Amps	Minimum Peak Primary Current
61	IR		0.36	Amps	Primary Ripple Current
62	IRMS		0.31	Amps	Primary RMS Current

Figure 12.   Current Waveform Shape Parameters.

64	▼TRANSFORMER PRIMARY DESIGN PARAMETERS				
65	LP		1132	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 1018 uH
66	LP_TOLERANCE		10	%	Primary inductance tolerance
67	NP		57		Primary Winding Number of Turns
68	ALG		344	nH/T^2	Gapped Core Effective Inductance
69	BM		2871	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
70	BAC		1004	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
71	ur		2053		Relative Permeability of Ungapped Core
72	LG		0.11	mm	Gap Length (Lg > 0.1 mm)
73	BWE		20.4	mm	Effective Bobbin Width
74	OD		0.36	mm	Maximum Primary Wire Diameter including insulation
75	INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
76	DIA		0.30	mm	Bare conductor diameter
77	AWG		29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
78	CM		128	Cmils	Bare conductor effective area in circular mils
79	CMA		416	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

Figure 13.   Transformer Primary Design Parameters Section of Design Spreadsheet.

81	▼TRANSFORMER SECONDARY DESIGN PARAMETERS				
82	**Lumped parameters**				
83	ISP		4.90	Amps	Peak Secondary Current
84	ISRMS		2.45	Amps	Secondary RMS Current
85	IRIPPLE		2.10	Amps	Output Capacitor RMS Ripple Current
86	CMS		489	Cmils	Secondary Bare Conductor minimum circular mils
87	AWGS		23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)

Figure 14.   Transformer Secondary Design Parameters Section of Design Spreadsheet.

Step 7 – Multiple Output Parameters [B94 – B141]

This section allows the user to design up to three secondary outputs (excluding bias supply) and chose a suitable secondary rectifier diode. The spreadsheet will provide a warning should the total power of the multiple outputs exceed the power described in the POUT cell.

For single output design, cells VO1, IO1 and PO1 will be the main output parameters entered in Step 1. Figure 16 displays the multiple output parameters in the spreadsheet. Figure 17 is for the design with negative output.

The spreadsheet also automatically calculates the critical electrical parameters for each secondary output:

Number of Turns for Output, NS
- Calculated turns for each output. The NS1 is for the main output which is equivalent to the calculated or desired secondary number turns reflected on cell [B51].

RMS Current of the Secondary Output, ISRMS (A)
- Used to size the secondary winding wire and determine the ripple current at the output capacitor.

Current Ripple on the Secondary, IRIPPLE (A)
- Used to size the output filter capacitor.

Secondary Rectifier Maximum Peak Inverse Voltage, PIVS (V)
- Used to size the output diode rectifier for voltage rating selection.

Additional information for the magnetic wire are also given:

Secondary Winding Conductor Bare Diameter CMS (Cmils)

Secondary Wire Gauge AWGS (AWG)

Minimum Secondary Bare Conductor Diameter DIAS (mm)

Maximum Secondary Outside Diameter for Triple Insulated Wire ODS (mm)

98	▼VOLTAGE STRESS PARAMETERS				
99	VDRAIN		596	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
100	PIVS		62	Volts	Output Rectifier Maximum Peak Inverse Voltage
101					
102					

Figure 15. Voltage Stress Parameters Drain of the Primary MOSFET and Secondary Output Diode.

93	▼ TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
94	**1st output**				
95	VO1		12.00	Volts	Main Output Voltage (if unused, defaults to single output design)
96	IO1		1.25	Amps	Output DC Current
97	PO1		15.00	Watts	Output Power
98	VD1		0.55	Volts	Output Diode Forward Voltage Drop
99	NS1		7.00		Output Winding Number of Turns
100	ISRMS1		2.349	Amps	Output Winding RMS Current
101	IRIPPLE1		1.99	Amps	Output Capacitor RMS Ripple Current
102	PIVS1		56	Volts	Output Rectifier Maximum Peak Inverse Voltage
103	Recommended Diodes		SB380		Recommended Diodes for this output
104	CMS1		470	Cmils	Output Winding Bare Conductor minimum circular mils
105	AWGS1		23	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
106	DIAS1		0.58	mm	Minimum Bare Conductor Diameter
107	ODS1		1.17	mm	Maximum Outside Diameter for Triple Insulated Wire
108					
109	▼ **2nd output**				
110	VO2			Volts	Output Voltage
111	IO2			Amps	Output DC Current
112	PO2		0.00	Watts	Output Power
113	VD2		0.70	Volts	Output Diode Forward Voltage Drop
114	NS2		0.39		Output Winding Number of Turns
115	ISRMS2		0.000	Amps	Output Winding RMS Current
116	IRIPPLE2		0.00	Amps	Output Capacitor RMS Ripple Current
117	PIVS2		2	Volts	Output Rectifier Maximum Peak Inverse Voltage
118	Recommended Diode				Recommended Diodes for this output
119	CMS2		0	Cmils	Output Winding Bare Conductor minimum circular mils
120	AWGS2		N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
121	DIAS2		N/A	mm	Minimum Bare Conductor Diameter
122	ODS2		N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
123					
124	▼ **3rd output**				
125	VO3			Volts	Output Voltage
126	IO3			Amps	Output DC Current
127	PO3		0.00	Watts	Output Power
128	VD3		0.70	Volts	Output Diode Forward Voltage Drop
129	NS3		0.39		Output Winding Number of Turns
130	ISRMS3		0.000	Amps	Output Winding RMS Current
131	IRIPPLE3		0.00	Amps	Output Capacitor RMS Ripple Current
132	PIVS3		2	Volts	Output Rectifier Maximum Peak Inverse Voltage
133	Recommended Diode				Recommended Diodes for this output
134	CMS3		0	Cmils	Output Winding Bare Conductor minimum circular mils
135	AWGS3		N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
136	DIAS3		N/A	mm	Minimum Bare Conductor Diameter
137	ODS3		N/A	mm	Maximum Outside Diameter for Triple Insulated Wire

Figure 16. Transformer Secondary Design Parameters for Multiple Outputs Section of Design Spreadsheet.

139	Total power			15	Watts	Total Output Power
140						
141	Negative Output	N/A	⌄	N/A		If negative output exists enter Output number; eg: If VO2 is negative outpu

Figure 17. Negative Output Section of Design Spreadsheet.

Step 8 – Selection of TinySwitch-III External Components

BYPASS/MULTI-FUNCTION Pin Capacitor

The capacitor connected to the BYPASS/MULTI-FUNCTION pin is used for both local supply decoupling and selection of one of three current limit levels.

A value of 0.1 μF selects Standard current limit or I_{LIMIT}, 1 μF selects Reduced current limit or $I_{LIMIT}-1$ and 10 μF selects Increased limit or $I_{LIMIT+1}$.

For flexibility in device selection, the current limit values overlaps between adjacent family members. For TNY275-TNY280, a 1 μF BP/M pin capacitor will select a lower current limit equal to the standard current limit of the next smaller device and a 10 μF BP/M pin capacitor will select a higher current limit equal to the standard current limit of the next larger device. This makes switching from one family member to another as simple as changing the value of BP/M pin capacitor. The TNY274 MOSFET does not have the capability for increase current limit so this feature is not available in this device.

Selectable MOSFET current limit provides design flexibility. Figure 18 shows the current limit values overlaps between adjacent device.

Operating in $I_{LIMIT+1}$, increases the output power capability without requiring a larger but, depending on the continuous or average power, may require an external heat sink attached to the source pins of the device.

Operating in $I_{LIMIT-1}$, decreases output power from a given device but reduces dissipation and therefore increases efficiency
.

Device	Current Limit (mA)		
	BP/M CAP 1 μF $I_{LIMIT(RED)}$	BP/M CAP 0.1 μF I_{LIMIT}	BP/M CAP 10 μF $I_{LIMIT(INC)}$
TNY274*	210	250	210
TNY275	250	275	350
TNY276	275	350	450
TNY277	350	450	550
TNY278	450	550	650
TNY279	550	650	750
TNY280	650	750	850

Figure 18. Adjacent Devices Current Limit Values Overlaps.

- *250 mA is the maximum current limit of the TNY274. All BP/M capacitor values ≥ 1 μF select $I_{LIMITred}$.
- TNY275 to TNY280, $I_{LIMITred}$ equals the standard I_{LIMIT} of the next smaller device.
- $I_{LIMITinc}$ equals the standard I_{LIMIT} of the next larger device.

- Optimum device and current limit by simply changing the value of the BP/M capacitor.
- $I_{LIMITinc}$ = highest power solution.
- $I_{LIMITred}$ = highest efficiency.
- Enables same supply to be used in applications with different ambient temperatures.

If a 0.1 μF bypass capacitor has been selected it should be a high frequency ceramic type (e.g. with X7R dielectric). It must be placed directly between BYPASS/MULTI-FUNCTION and SOURCE pins to filter external noise entering the BYPASS pin.

If a 1 μF or 10 μF bypass capacitor was selected, it is recommended that a 0.1 μF capacitor is placed directly across BYPASS/MULTI-FUNCTION and SOURCE pins for high frequency decoupling.

To ensure correct current limit, it is recommended that nominal 0.1 μF / 1 μF / 10 μF capacitors are used. In addition, the BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum acceptable capacitor tolerance values are set by IC characterization (Table 6). All though electrolytic capacitors can be used; surface mount multi-layer ceramic capacitors are often preferred for use with double sided boards as they enable the capacitor to be placed close to the IC. A surface mount multi-layer ceramic X7R capacitor rated at least 10 V / 0805 size is recommended. Figure 19 (TDK MLCC DC Bias Characteristic) shows the graph for capacitance variation versus the applied voltage. This is simulated with a nominal capacitor value of 4.7 μF both on X7R and X5R types, different sizes and voltage rating.

Nominal PRIMARY BYPASS Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
0.1 μF	-60%	+100%
1 μF	-50%	+100%
10 μF	-50%	NA

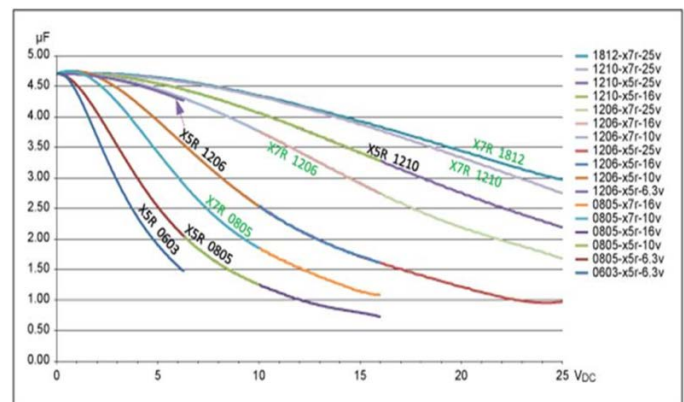Table 7. BP/M Pin Capacitor Tolerance Value.

Figure 19. Example of MLCC DC characteristic using 4.7 μF (X7R and X5R Type) Capacitance Variation vs. Applied Voltage

Selection of Undervoltage Components

Line undervoltage prevents the supply from starting until the input voltage is above a defined level. During power-up or when the switching of the power MOSFET is disabled in auto-restart, the current into the ENABLE/UNDERVOLTAGE pin must exceed 25 μA to initiate switching. As a resistor from the DC rail to the ENABLE/UNDER-VOLTAGE pin is used to sense the input voltage, the supply voltage that causes the current into the EN/UV to exceed 25 μA defines the undervoltage threshold. During power-up while the line undervoltage still exist the voltage at the ENABLE/UNDERVOLTAGE pin is being hold at 4.9 V. When the line undervoltage no longer exists the BYPASS or ENABLE/UNDERVOLTAGE pin voltage will rise from 4.9 V to 5.85 V. Figure 20 illustrates the start-up sequence with the resistor/s across positive input rail (typically connected at the input capacitor) and ENABLE/UNDERVOLTAGE pin of the TinySwitch device.

The line undervoltage circuit also detects when there is no external resistor connected to the ENABLE/UNDERVOLTAGE pin (less than ~ 2 μA into the pin). In this case the line undervoltage function is disabled.

As a guide, the following equations can be used to calculate the undervoltage sense resistor and the equivalent AC input undervoltage.

$$R_{UV} = \frac{V_{UV} - V_{EN}}{I_{EN}}$$

Where, V_{EN} and I_{EN} is from TinySwitch-III data sheet.
$V_{EN} = 2.2\ V_{TYP}$ and $I_{EN} = 25\ \mu A$.
V_{UV}, is the equivalent DC input undervoltage.

For example: At universal input, V_{UV} is typically set at 100 V. Therefore, using the R_{UV} equation, it is equivalent to 3.9 MΩ. Similarly for high-line input of 230 VAC, V_{UV} is set at 200 V. Therefore, R_{UV} is equivalent to 8.2 MΩ.

The Line Undervoltage (VLUV) or the equivalent AC input undervoltage threshold is calculated below:

$$V_{LUV} = \frac{V_{UV}}{\sqrt{2}}$$
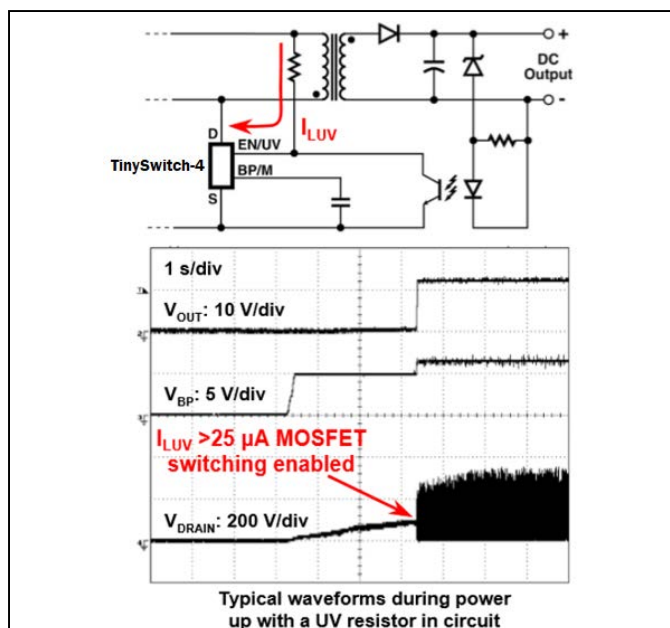
Figure 20. EN/UV Schematic and Start-Up Waveforms with a UV Resistor.

The sense resistor should be rated above 400 V, generally requiring either a single 0.5 W or two 0.25 W or three 0.125 W (0805 resistor) devices connected in series.

Selection of Primary Clamp Components

Describe in this section are three commonly used primary clamp configurations; RCD, Zener Clamp and Zener Bleed (RCD with Zener) Configurations. Each clamp is discussed in details with design guidelines and best practices to aid the engineers to properly select the correct clamp configuration and its components for their design. Figures 21 shows the comparison of the circuit and power dissipation of the Zener diode for Zener Clamp and RCDZ configuration. And Figure 22 shows primary clamp circuits arrangement of RCD and RCDZ. Table 9 states the relative benefits of each clamp circuits

Key Design Points Primary Clamp Circuit Optimization

- Minimize leakage inductance, completely fill each winding layer of the transformer. Following the assumption of leakage inductance or L_{LK} to be less than 3% of the primary inductance (L_P) is a good starting point for the calculation of primary clamp parameters, but the best practice is to measure the leakage inductance of the actual transformer sample.
- Optimize the value of snubber resistors in the RCD clamp to further reduce power losses meeting the following conditions: 1. The EMI performance is not compromised, and 2. Enough drain voltage margin for the internal MOSFET (BV_{DSS}), typically set in the range of 80% to 90% of BV_{DSS} under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit). If sufficient margin is needed for efficiency and no-load input power, other primary clamp configurations such as Zener Clamp or Zener Bleed (RCD+Z) configurations are options.
- Minimize clamp losses by optimizing the reflected voltage (VOR) value.
- Minimizing interwinding capacitance by following proper layout and transformer construction such as maintaining a tightly coupled loop between the primary snubber and windings and putting layers of tape between each primary winding.

RCD Clamp Configurations

RCD is for applications where lowest cost and EMI are most important. This is the most commonly used clamp in low power supply application. Figure 22 shows the circuit using RCD clamp.

In RCD Clamp circuit of Figure 22, the clamp diode, D_{CLAMP} must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of ≤ to 2 μs. The use of standard recovery glass passivated diodes allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the MOSFET inside TinySwitch-III turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{CLAMP}. Resistor R_{DAMP}, which is in the series path, offers damping preventing excessive ringing due to resonance between the leakage reactance and the clamp capacitor C_{CLAMP}. Damping the ringing reduces the EMI, and R_{DAMP} typical value is in the range of 22 Ω to 100 Ω. Resistor R_{CLAMP} bleeds-off energy stored inside the capacitor C_{CLAMP}. Power supplies using different TinySwitch-III devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor C_{CLAMP}, and resistors R_{CLAMP} and R_{DAMP} must therefore be optimized for each design. As a general rule it is advisable to minimize the value of capacitor C_{CLAMP} and maximize the value of resistors R_{CLAMP} and R_{DAMP}, while still meeting BV_{DSS} limit at highest input voltage and full load. The value of R_{DAMP} should be high enough to damp the ringing in the required time, but must not be so large as to cause the drain voltage to exceed 80% to 90% of BV_{DSS} (depends on the derating requirements). Note that The BV_{DSS} of TinySwitch-III devices is at 700 V.

A ceramic capacitor that uses a dielectric such as Z5U when used in clamp circuit for C_{CLAMP} may generate audible noise, so a polyester film type or a ceramic capacitor with X7R as a dielectric, 1 kV rating, 1206 size are commonly used.

Recommended for clamp diode D_{CLAMP} is a 1N4007G, a glass passivated version of standard 1N4007 diode. This diode has a reverse recovery time of 2 μs. If unavailable, a fast diode such as FR107G or FR106G may be used instead.

As a guide the following equations can be used to calculate R2CD component values:

$$R_{SN} = \left[\frac{V_C^2}{\frac{1}{2} L_{IK} \times I_{PK}^2 \times \frac{V_C \times F_s}{V_C - V_{OR}}} \right]$$

$$C_S = \frac{V_C}{RSN1 \times F_s \times dV_{CSN}}$$

$$R_S = \left(\frac{L_{IK}}{C_{SN}} \right)^{\frac{1}{2}}$$

Where:
V_C or VC_{CLAMP}, is the voltage across the clamp circuit
I_{PK}, is the peak switching current
F_s, is the switching frequency
L_{LK}, is the leakage inductance which is measured from the actual transformer sample.
V_{OR}, is the reflected output voltage
dV_{CSN}, is the maximum ripple voltage across the clamp capacitor which is typically 10% of the clamp voltage.
For example:
V_C = 150 V, F_S = 124 kHz, I_{PK} = 0.6 A, V_{OR} = 95 V, L_{LK} = 5 μH and d_{VSN} = 15 V

The following values are the results by applying the equations above:
R_{CLAMP} = 86.02 kΩ, C_{CLAMP} = 1.09 nF, R_{DAMP} = 67.7 Ω

Estimate Power Dissipation on R_{CLAMP}:

$$PR_{CLAMP} = \frac{V^2 C_{CLAMP}}{R_{CLAMP}}$$

Measure the voltage across C_{CLAMP} at full load and low-line using DMM.

Zener Clamp Configurations
RCD clamp is the simplest way to snub the primary drain MOSFET voltage. However, with an RCD clamp, the light load losses suffer from continuous power dissipation and gives higher input power at no-load. For applications where lower no-load consumption and higher light load efficiency are most important, the recommended primary clamp to be used is Zener Clamp configuration (Figure 21). This configuration is much more effective in clamping the leakage energy during start-up transients. The nominal value of Zener clamp voltage V_{CLO} needs to be 50% greater than the reflected voltage so that the Zener clamps only the leakage energy and does not impede the switch-over of current from primary to the secondary. Experimental measurements show that this voltage margin is needed for the secondary current to be quickly established through the leakage inductance. Lower clamp voltage should not be used because part of the stored energy in the core would be delivered to the Zener which increases its dissipation. The clamp voltage V_{CLM} at high current and high temperature can be much higher. Experimental data shows that the V_{CLM} can be as high as 40% above V_{CLO}.

V_{CLM} = 1.4 x V_{CLO}

In addition, with the blocking diode in series with the Zener, a voltage spike of 20 V is added due to the forward recovery of the diode. The resistor in series RS serves as to dampen the ringing. Even though the average power dissipation in the clamp is low, the pulse power dissipation in the Zener is high. The high stress and power requires the use of a transient voltage suppressor (TVS) part from the P6KE series, which should be appropriately selected with sufficient derating.

Table 7 provides recommended Zener or TVS diode and the blocking diode used in Zener Clamp configuration at different input voltage.

Input Voltage (VAC)	Zener Voltage, VCLO (V)	TVS	Diode
100 / 115	90	P6KE91	FR107, 1N4937, UF4005
85 – 265	200	P6KE200	FR107, 1N4937, UF4005
230	200	P6KE200	FR107, 1N4937, UF4005

Table 8.   TVS and Diode Recommendation for Zener Clamp.

RCDZ Clamp (Zener Bleed) Configuration
The goal of the primary clamp design is to reduce the drain node ringing as well as limiting the peak drain voltage and minimizing the dissipation for high efficiency and low no-load input power. In order to meet these goals, an RCDZ Clamp or Zener Bleed (Figure 21) configuration is an option. This is an RCD clamp where the resistor is replaced by the series combination of a resistor R_{CLAMP} and low power Zener (VR_{CLAMP}). The addition of the Zener prevents the clamp capacitor (C_{CLAMP}) from being discharged below the Zener voltage rating at light or no-load that would normally occur with a standard RCD clamp. This improves light load efficiency and reduces no-load input power. The instantaneous current through VR_{CLAMP} is limited by R_{CLAMP} allowing a standard low-cost, low power Zener as opposed to a TVS type.

The value of VR_{CLAMP} is typically set at 0% – 20% above the value of the reflected voltage. Table 8 listed some of the recommended Zener diode components.
The value of C_{CLAMP} is typically 1 nF for converters under 10 W and 10 nF for designs above 10 W.

The value of R_{CLAMP} was selected to discharge C_{CLAMP} to the value of VR_{CLAMP}. R_{CLAMP} is typically 2 kΩ to 20 kΩ, adjusted such that the voltage on C_{CLAMP} is approximately V_{OR} × 1.5. The voltage rating of D_{CLAMP} should be the next standard value above V_{OR} + 10 V. In designs with higher transformer leakage inductance the value of R_{CLAMP} may need to be increased to keep the dissipation of VR_{CLAMP} acceptable.

To prevent high frequency ringing D_{CLAMP} was selected as a standard recovery diode versus a fast or ultrafast type. Standard diode with part number 1N4007G from Vishay is recommended. If not available 1N4937, RS1J, FR106G and FR107G are also an option.
R_{DAMP} acts to dampen the ringing at the drain voltage, the value being chosen to dampen the ringing to an acceptable level while keeping the peak drain voltage below the BV_{DSS} of the internal MOSFET. Recommended range is 47 Ω to 330 Ω with a typical value of 100 Ω. Table 8 listed some recommended Zener diode for R2CDZ Clamp configuration.

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Zener Part Number	Voltage Rating
1N5270B − 1N5275B	91 V − 140 V
BZG03C91 − BZG03C150	91 V − 150 V

Table 9.   Recommended Zener Diode for R2CDZ Clamp Configuration.

Primary Clamp Configurations Comparison

The RCD clamp aside from the simplicity, it provides the lowest cost with the best performance in attenuating the EMI noise as opposed to the other two clamp configurations. However, the circuit simplicity has its drawbacks, it can lead to a significant increase in no-load input power (see comparison in Figure 23), it has the lowest light load efficiency and poor light and no-load regulation if preload is not present. The RCD clamp may also cause of oscillation at light load if the components within the snubber are not properly selected.

The Zener Bleed is actually a configuration that combines the RCD clamp and the Zener diode, wherein the R_{CLAMP} is in series with the Zener while the capacitor C_{CLAMP} is in parallel with that series combination. While in Zener Clamp, the resistor in series with the Zener and the parallel capacitor is not present. Both clamp circuits

are shown on Figure 21. Therefore, in Zener clamp configuration, the Zener dissipates all the power and is subjected to peak currents close to the primary current. Even though the average power dissipation in clamp is low, the pulse power dissipation is high. This high stress and power requires the use of a transient voltage suppressor (TVS) part from the P6KE series, which should be appropriately selected with sufficient derating. Unlike the Zener (TVS) clamp, the Zener Bleed circuit has a soft-knee which results in a non-linear increase in the load across the clamp capacitor. This reduces the peak current and lowers the pulse power dissipation in the Zener, thereby ensuring low Zener stress. Typically, in the Zener Bleed configuration, the peak current is limited by the series resistor to tens of mA. The much lower stress on the Zener allows the use of low-cost 1 W components as opposed to TVS types and removes reliability concerns due to operating the Zener close to its maximum rating.

As shown on Figure 21, the power dissipation in the Zener used in the Zener Bleed circuit, is considerably lower than the peak power dissipated in a Zener (TVS) clamp type circuit.

RCDZ (Zener)	Zener Clamp

PI-5108b-050420

PI-5107b-050420

RCDZ Clamp (300 VDC Input, 2.5 A Load).
Upper: I_{ZENER}, 1 mA / div, 2 μs / div. (Waveforms measured voltage across 3 kΩ resistor)
Middle: V_{ZENER}, 100 V / div, 2 μs / div
Lower: Power Dissipation of Zener, 0.17 W / div.
Zener: Peak Power Dissipation = 0.36 W.
Zener: Mean Power Dissipation (approximately) = 165 mW.

Zener Clamp (300 VDC Input, 2.5 A Load).
Upper: I_{TVS}, 500 mA / div, 2 μs / div.
Middle: V_{TVS}, 100V / div, 2 μs / div.
Lower: Power Dissipation of TVS, 100 W / div.
TVS: Peak Power Dissipation = 97 W.
TVS: Mean Power Dissipation (approximately) = 843 mW.

Figure 21.   Comparison Between Zener Bleed (RCDZ) and Zener Clamp.

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With an RCD clamp and operation at light load or no-load, the voltage of C_{CLAMP} discharges below the value of V_{OR}. When the next flyback cycle occurs, the primary clamp circuit now appears as a load, the voltage of C_{CLAMP} must exceed the value of V_{OR} before the output diode and bias diode will conduct. This loading effect causes the output voltage sampled via the bias winding to appeared low and therefore the control loop responds and the output voltage rises above the correct value. This error might cause burst of pulses as the bias on C_{CLAMP} changes erratically depending on operating frequency.

At higher load the RCD clamp allows the leakage spike amplitude to become significantly higher causing more ringing on the primary and feedback winding which may cause oscillation due to the variation in the sampled voltage. As opposed to the RCD clamp, the Zener Bleed circuit ensures that there is virtually no-load across the clamp capacitor once it is discharged to a level below the rated Zener voltage. This non-linearity provides excellent regulation from a PSR converter since it allows the bias winding and primary winding voltages to track the secondary output voltage even at light-load.

Shown in Figure 23 the comparison of the input power consumption using RCD and Zener Bleed primary clamp. A significant decrease of input power when a Zener Bleed (RCDZ) is implemented as primary clamp circuit.

As can be seen in the output voltage regulation from Figure 24, the RCD snubber also causes the output to rise outside of regulation limits at light load for the same preload condition. Solving this requires a heavier preload resistor which further increases no-load input power.

Finally, the RCDZ clamp shown on Figure 22 can be optimized to minimize ringing on the feedback winding flyback pulse. The damping resistor R_{DAMP} value has a strong effect on the amount of ringing that develops on the feedback winding as can be seen in the two cases below. Notice at the MOSFET turn-off edge how strongly the feedback winding waveform follows the primary winding qualitatively

RCD	RCDZ (Zener Bleed)

PI-5107a-050420   PI-5108a-050420
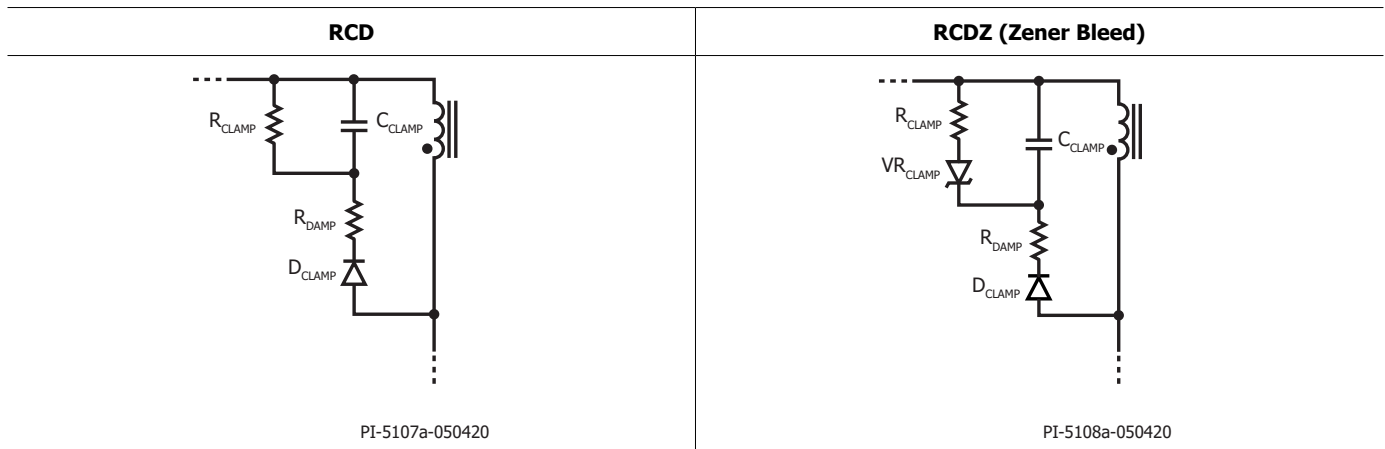
Figure 22. Primary Clamp Arrangement: RCD and RCDZ (Zener Bleed)
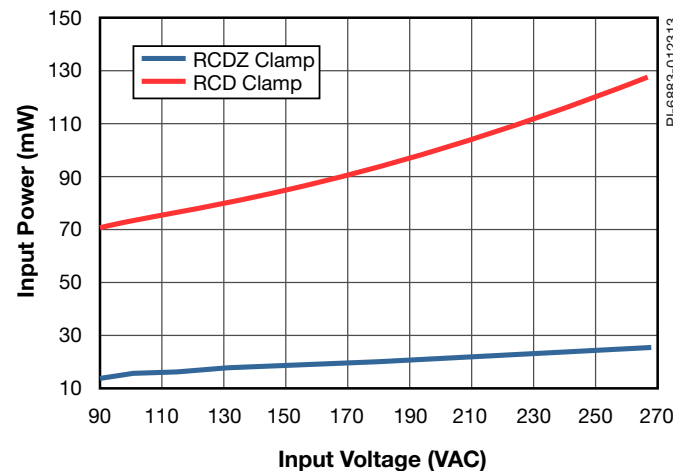
Figure 23. Comparison of Input Power for 30 W Adapter Using RCD and RCDZ.
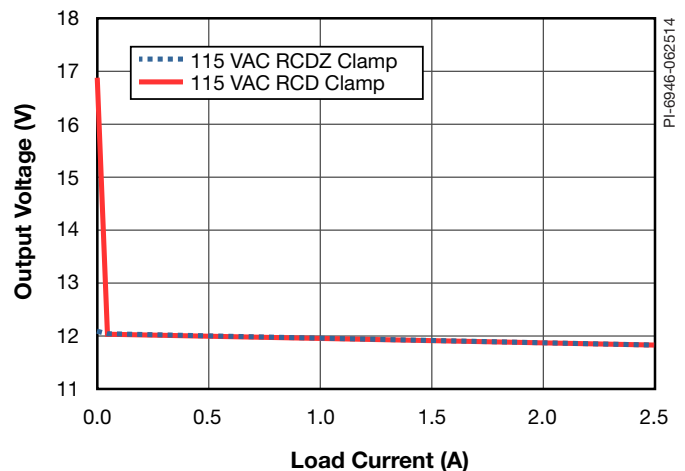
Figure 24. Comparison of Regulation for 30 W Adapter Using RCD and RCDZ Clamp.

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Primary Clamp Circuit

Benefits	R2CD	Zener	R2CDZ
Component Cost	Low	Medium	High
No-load Input Power	High	Low	Medium
Light-load Efficiency	Low	High	Medium
EMI Response	High	Low	Medium

Table 10.   Comparison Benefits of Primary Clamp Circuits.

External Bias Supply Components

TinySwitch-III has an internal (5.85 V) regulator that charges the bypass capacitor connected to the BYPASS/MULTI-FUNCTION pin to 5.85 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS/MULTI-FUNCTION pin is the internal supply voltage node. When the MOSFET is on, the device operates from the energy stored in the bypass capacitor. Figure 25 and 26 illustrates the charging of the BYPASS/MULTI-FUNCTION pin capacitor and starts of switching the MOSFET. Extremely low power consumption of the internal circuitry allows TinySwitch-III to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a shunt regulator clamping the BYPASS/ MULTI-FUNCTION pin at 6.4 V when current is provided to the BYPASS/MULTI-FUNCTION pin through an external resistor (R_{BIAS}, see Figure 28). This facilitates powering of TinySwitch-III externally through a bias winding to decrease the no-load consumption to well below 50 mW.
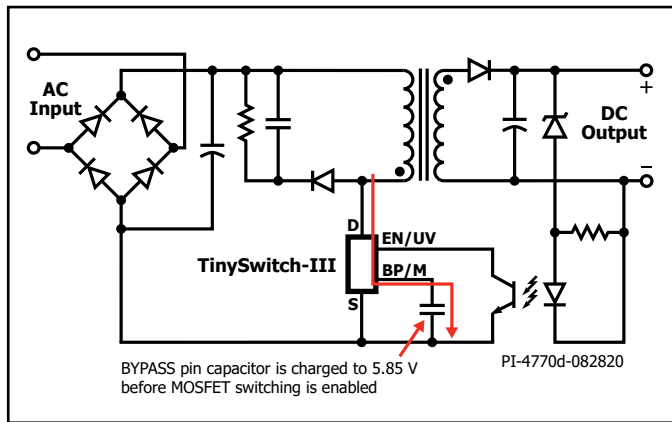
Figure 25.   Charging the BYPASS/MULTI-FUNCTION Pin Capacitor.
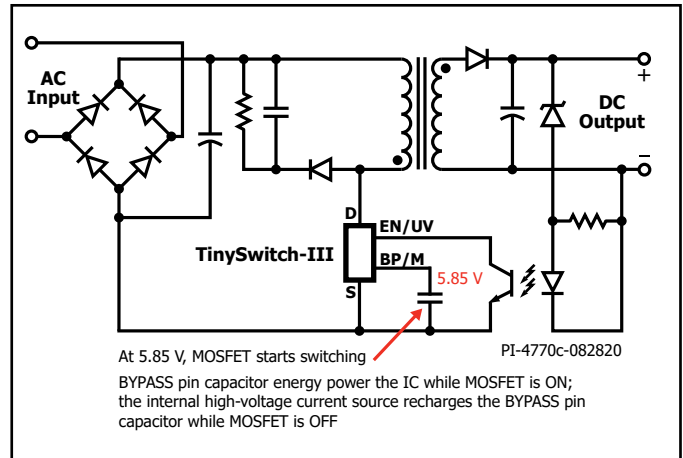
Figure 26. Illustrating the Start of MOSFET Switching.

Figure 27 illustrates the TinySwitch-III start-up waveforms with the BYPASS pin voltage enabled as it reaches 5.85 V before TinySwitch switching cycles.
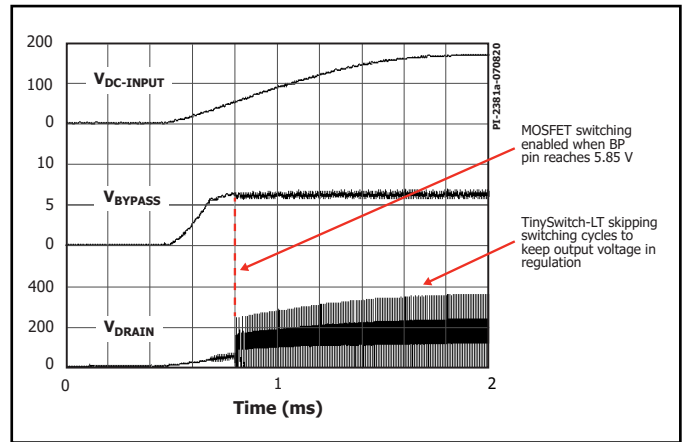
Figure 27.   TinySwitch-III Start-Up Waveforms.

IC Bias Current

During normal operation, TinySwitch-III must have an external supply current equal to $I_{S2\_MAX} + |I_{DIS\_MAX}|$. In Figure 28, resistor R_{BIAS} provides this current from the bias voltage across C_{BIAS}. As switching frequency can be low during light or no-load conditions, to prevent excessive voltage droop an electrolytic capacitor with a value $\geq 1\ \mu F$ (depends on the bias voltage) and rated above the maximum bias voltage is implemented.

$$I_{BIAS} = \frac{V_{BIAS} - V_{BP/M}}{R_{BIAS}}, I_{BIAS} > I_{S2\_MAX} + |I_{DIS\_MAX}|$$

Where,

I_{BIAS}, is the external supply current of the IC during normal operation.
V_{BIAS}, is the external supply voltage of the IC, that is generated by the bias winding.
$V_{BP/M}$, is the BP/M pin voltage from the data sheet.
I_{S2_MAX}, is the maximum Drain supply current of the IC from the data sheet (I_{S2}).
I_{DIS_MAX}, is the maximum upper turn-off threshold current of EN/UV pin from the data sheet (I_{DIS}).

The value of bias resistor R_{BIAS} in the schematic of Figure 28 together with the bias voltage must be optimized to meet the no-load consumption requirements as well as the TinySwitch IC supply current.

No-Load Consumption

For lower no-load input power consumption, the bias winding may also be used to supply the TinySwitch-III device. From Figure 28, Resistor R_{BIAS} feeds current into the BYPASS/MULTI-FUNCTIONAL (BP/M) pin, inhibiting the internal high-voltage current source that normally maintains the BYPASS/MULTI-FUNCTIONAL pin capacitor voltage (C_{BP}) during the internal MOSFET off-time. This reduces the no-load input power consumption below 50 mW especially at high-line input, where it is highest. To achieve such low input power, there are key factors to be optimized, the external bias supply voltage, choice of bias filter capacitor and bias resistor value. Select the value of the bias resistor to provide the data sheet Drain supply current (I_{S2}). In practice, due to the reduction of the bias voltage at light load, start with a value equal to 40% greater than the data sheet maximum current, and then increase the value of the resistor to give the lowest no-load consumption.

Optimization of bias output voltage is also key to keep the no-load input power across the line input especially at high-line. As a rule-of-thumb, the minimum bias voltage at no-load condition should be 7 V, this still gives enough headroom to supply current to the BYPASS pin of the IC.

Depending on the bias winding voltage, it is recommended that a $1\ \mu F$ to $10\ \mu F$ capacitance is used for the bias winding output filter capacitor (C_{BIAS}) to prevent excessive droop during light or no-load conditions. A low ESR electrolytic capacitor is recommended as it reduced no-load input power and rated above maximum bias voltage. Ultrafast diodes are recommended for the bias winding rectifier to likewise reduce no-load power consumption.
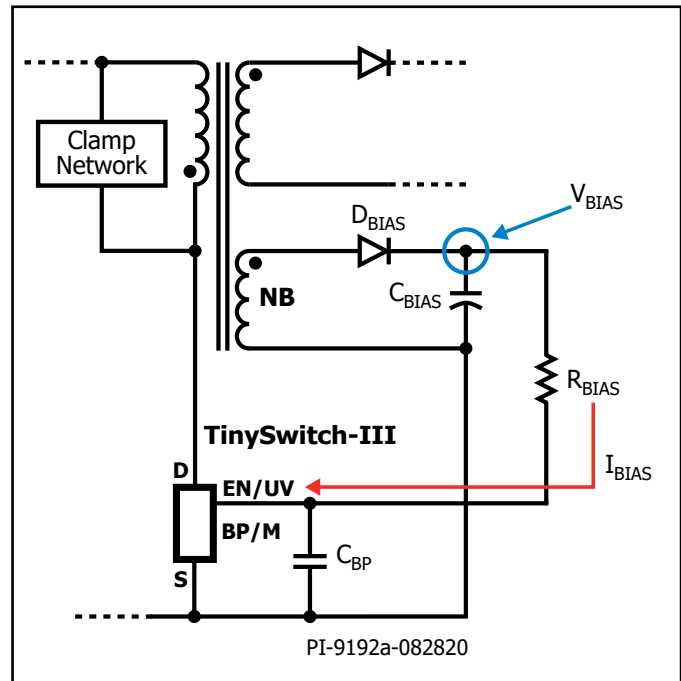
Figure 28. TinySwitch-III with the Bias Winding.

Output Overvoltage Shutdown

The latching shutdown feature can be used to protect the load from a catastrophic open loop fault, such as failure of the optocoupler.

The design implements the PI's proprietary primary overvoltage sensing via the bias winding voltage during MOSFET off-time. To trigger the latching shutdown feature of TinySwitch-III, a current (I_{SD}) >6.5 mA must flow into the BYPASS/MULTI-FUNCTIONAL pin. This can be achieved by sensing the bias winding voltage. In Figure 29, the bias voltage across C6 is typically 22 V. During an open-loop condition, the bias voltage will rise in proportion to the output voltage. Once this rises above the sum of the maximum BYPASS/MULTI-FUNCTIONAL pin voltage (6.15 V_{BP_MAX}) and the breakdown voltage of the Zener diode, VR2 (for example a 28 V Zener), then current will flow into the BYPASS/MULTI-FUNCTIONAL pin. When this exceeds I_{SD} then the part will latch off. To reset the latch, either the ENABLE/UNDERVOLTAGE pin current must fall below the UV threshold current (25 μA), or the BYPASS/MULTI-FUNCTIONAL pin voltage falls below 4.9 V. Typically, this would occur after the AC input is removed, and the input bulk capacitor discharges. In designs where a faster reset is required, then a separate AC sense circuit can be used to feed the ENABLE/UNDERVOLTAGE pin. Shown on Figure 29 is the schematic with OVP implementation.

Selecting the Zener diode (VR2) voltage to be approximately 6 V above the bias winding voltage gives good OVP performance for most designs, but can be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or OVP Zener as shown by R3 in Figure 29.
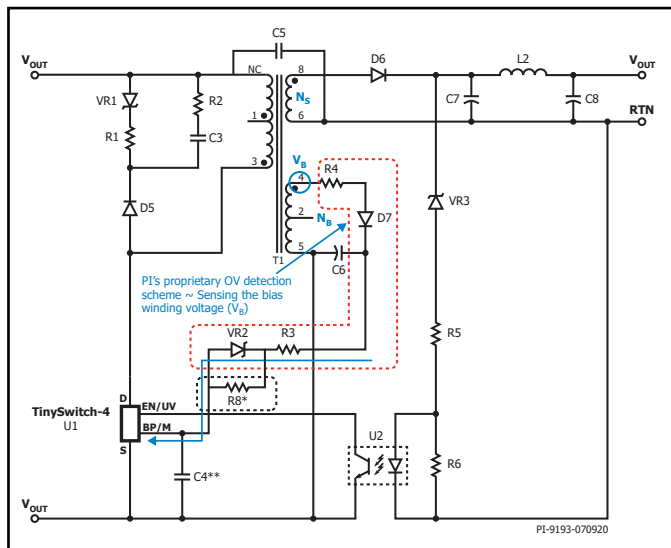
Figure 29.   External Schematic Showing Implementation of OV Shutdown and External Bias Circuit

Primary Sense OVP Guidelines:

- $V_B \approx V_{OUT} \times N_B/N_S$; High bias voltage improves accuracy by reducing the effect of the leakage inductance. Works well within bias voltage range of 12 V to 22 V. N_B is the number of turns of bias winding and N_S is the number of turns of secondary winding.
- Zener Voltage (VR2), $VR_{OVP} > V_B + V_{BP\_MAX}$
  Where $V_{BP\_MAX} = 6.15$ V (from the data sheet).
- R4 filters the leakage spike and R3, adjust the trip point. Recommended value is from 10 Ω to 47 Ω.
- Verify that OVP does not falsely trigger: Test at low-line at maximum load where leakage energy is highest. Perform start-up at highest line, no-load, where output overshoot is at maximum.

Step 11 – Select Output Rectifier Diode

For each output, use the values of peak inverse voltage (PIVS) and output current (IO) provided in the design spreadsheet to select the output diode's voltage rating (VR). Table 10 shows some commonly available types.

VR ≥ 1.25 × PIVS: where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

ID ≥ 2 × IO: where ID is the diode rated DC current, and IO is the average output current. Depending on the temperature rise and the duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heat sinking necessary. Table 10 provides recommended part numbers for output rectifiers.

Part Number	IF$_{AVE}$ (A)	VR (V)	Type
SB120 − SB160	1	20 − 60	Schottky
SB120 − SB1100	1	20 − 100	Schottky
1N5820 − 1N5822	3	20 − 40	Schottky
SB320 − SB360	3	20 − 60	Schottky
STPS3150	3	150	Schottky
SB540 − SB560	5	40 − 60	Schottky
VS-6TQ035 − 6TQ045	6	35 − 45	Schottky
MBR745 − MBR760	7.5	45 − 60	Schottky
VS-90SQ30 − 90SQ45	9	30 − 45	Schottky
MBR1035 − MBR10200	10	50 - 200	Schottky
UF4001 − UF4003	1	100 − 300	Ultrafast
ES2A − ES2D	2	50 − 200	Ultrafast
UF5401 − UF5403	3	100 − 300	Ultrafast
BYV28-50 − BYV28-100	3.5	50 − 200	Ultrafast
VS-MURB820PbF	8	200	Ultrafast
LQAQOT300	10	300	Ultrafast

Table 11.   Recommended Diodes Suitable for Output Rectifier.

Step 12 – Select Output Capacitor

A low ESR electrolytic capacitors is one of the key parameters in smoothing the output ripple voltage. Other parameters to be considered for their selection are the RMS ripple current rating, DC working voltage and ESR. The actual capacitance value is of secondary importance.

Considerations for Selection of Output Capacitor:

- Capacitor ripple current is specified @ 105 ºC, 100 kHz must be equal or larger than IRIPPLE, where IRIPPLE [B85] is from Step 6.
- Use low ESR, electrolytic capacitor. Output switching ripple voltage is ISP × ESR, where ISP [B83] is from Step 6. Table 11 listed some low ESR electrolytic capacitors with 35 V voltage rating.
- Use parallel capacitors to increase ripple current capacity for high current outputs.

Output Voltage / Current	Output Capacitor
5 V to 24 V, 1 A	330 μF, 35 V, low ESR, electrolytic United Chemi-Con (UCC): EKZ350ELL331MJ16S Nichicon: UHD1V331MPD1TD Panasonic: EEU-FM1V331
5 V to 24 V, 2 A	1000 μF, 35 V, low ESR, electrolytic United Chemi-Con: EKZH350ETE102MK20S Nichicon: UHW1V102MHD

Table 12.   Output Capacitor Sample Selection for given Output Voltage and Current

Ripple Current Rating

The spreadsheet calculates the output capacitor ripple current at the peak load condition. Therefore, the actual rating of the capacitor will depend on the peak-to-average power ratio of the design. For conservative design select the output capacitor(s) such that the ripple rating is greater than the calculated value, I_{RIPPLE} from the spreadsheet, calculated at the peak load condition. However, in designs with high peak-to-continuous (average) power, the capacitor rating can be reduced based on the measured capacitor temperature rise under worst-case load and ambient temperature. If a suitable individual capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should be considered to ensure that the capacitor is not oversized.

Actual ripple current of the output capacitor can be calculated as follows:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

Where I_{SRMS} is the secondary winding RMS current which is also automatically calculated in the spreadsheet and I_O is the DC output current.

ESR Specification

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

$$ESR = \frac{V_{RIPPLE}}{I_{SP}}$$

Where V_{RIPPLE} is the maximum allowed output ripple and I_{SP} is peak secondary current.

Voltage Rating

Select a voltage rating such that $V_{RATED} \geq 1.25 \times VO$. A margin of 25% is recommended for reliability purposes.

Output Capacitance

Effective series resistance (ESR) causes internal heating of the capacitor and basically determines the switching frequency voltage ripple, which is superimposed on top of DC output value. This is true as long as the capacitance contribution to the ripple is negligible, that is if:

$$C_{OUT} >> \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times f_{SW}}$$

For ease of selection and assumption, sample selection of output capacitors actual part numbers are given on Table 11 as starting point. These capacitors are rated for 35 V and designer will simply adjust the rated voltage for the power supply required output voltage and select from manufacturers data sheets.

Step 13 – Add Output LC Post Filter

Adding parallel output capacitors is the simplest solution to achieve the required ESR in order to reduce the output ripple voltage, but this is sometimes costlier and requires short traces on the layout to make it effective. An alternative solution is to add a LC post filter, instead using additional low ESR capacitors, a small current rated inductor and a general purpose electrolytic capacitor can be used.

As shown on Table 13, a post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple.

Inductor L_{PF} should be in the range of 2.2 μH – 4.7 μH with a current rating above the peak output current. Use ferrite bead for low output power or output current ≤ 1 A and standard off-the-shelf choke for higher current output. Increase choke current rating or wire size if necessary to avoid significant DC voltage drop.

Capacitor C_{PF} typical value is in the range of 100 μF to 330 μF with a voltage rating ≥ $1.25 \times V_{OUT}$.
Example: United Chemi-Con with part number ELXZ160ELL101MFB5D for the required 12 V output.

If a post filter is used, then the optocoupler should be connected before the post filter inductor as shown in Figure 1 and Tables 13 and 14 schematics, but the feedback sense resistors should be connected after the post filter inductor, shown on Table 14 schematic, for good regulation.

Step 14 – Select Feedback Circuit Components

Zener Feedback

Table 13 shows a typical implementation of Zener feedback. The series drops across D_{FB}, VR_{FB}, R_{FB1} and the forward drop of the LED U_{FB2} determine the output voltage. Diode D_{FB} is optional depending on the availability of a suitable Zener voltage. Resistor R_{BIAS} provides a 0.5 mA bias current so that VR_{FB} is operated close to its knee voltage. Resistor R_{FB1} adjust the output voltage and limits the feedback current during output load transient. Both of these can be 0.125 W or 0.25 W, 5% types. Selecting a Zener with a low test current (5 mA) is recommended to minimize the current needed to bias the feedback network, reducing no-load input power consumption. Table 13 shows values using a Zener feedback circuit. Sample component for Zener diode is BZX79 series. For example, the output voltage is regulated at 12 V, the recommended component is BZX79-B11 from Vishay. Equation below will estimate the Zener voltage rating needed for the desired output voltage.

$$VR_{FB} = V_{OUT} - (VU_{FB2} + VR_{FB1})$$

Where,
VR_{FB}, is the Zener diode voltage rating.
V_{OUT}, is the output voltage regulation.
VU_{FB2}, is the forward drop of the optocoupler LED.
VR_{FB1}, is the voltage across the series resistor.

Reference IC (TL431) Feedback

For improved accuracy, Table 14 shows a typical implementation using a reference IC. Reference U_{FB2} or TL431 IC is used to set the output voltage programmed via the resistor divider R_{S1} and R_{S2}. Resistor R_{BIAS} provides the minimum operating current which is approximately equal to 1 mA for U_{FB2} while R_{FB1} sets the DC gain and limits the feedback current during output load transient. Capacitor C_{FB2} rolls off the high frequency gain of U_{FB2} so that it does not respond to the cycle-by-cycle output ripple current voltage. AC feedback is provided directly through the optocoupler. TL431 provides output accuracy of ± 2%. Table 14 shows the typical component values using reference IC for feedback circuit.

Optocoupler with CTR of 80% – 200% is recommended. Table 12 shows actual part number selections for optocoupler.

Optocoupler Part No.	Manufacturer	CTR%
PS2501-1-H-A	CEL	80 – 160
PS2501-1-H-A	Renesas	80 – 160
TPC817A C9G	Taiwan Semiconductor	80 – 160
LTV186A	Liteon	80 – 160
LTV817A	Liteon	80 – 160
K1010A	Cosmo	80 – 160
PC817X1	SHARP	80 – 160

Table 13.   Optocoupler Recommended Part Number.

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Output Voltage (V)	Zener Value, V_{RFB} (V)	Feedback Bias Resistor, R_{BIAS} (kΩ)	Opto Series Resistor, R_{FB1} (Ω)	Series Diode DFB Required?
5	4.3			No
8	7.5			
12	11	1	220	
18	16			Yes
24	22			
30	28			
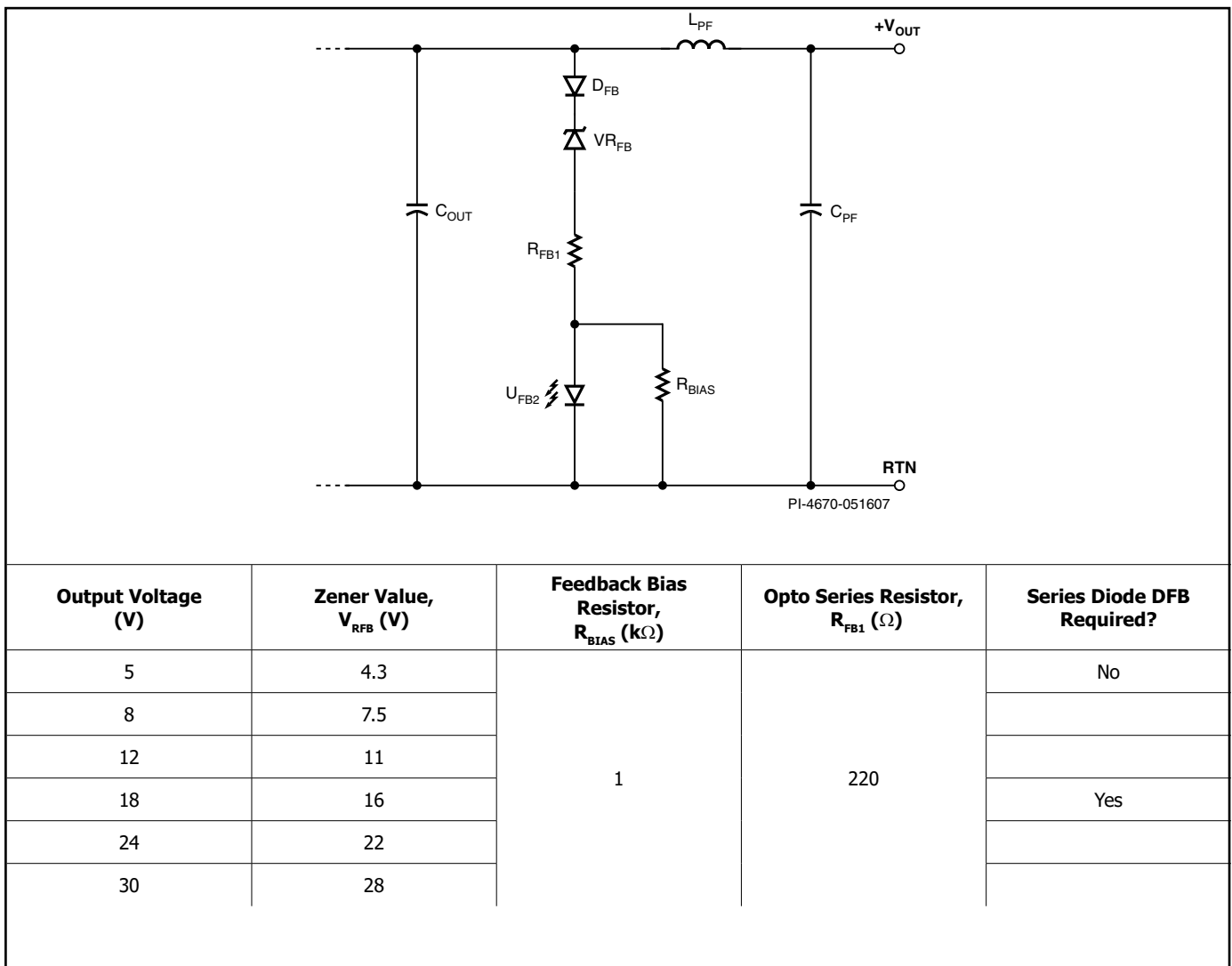
Table 14.   Typical Component Values for Zener Feedback Circuit.

PI-4671-051607

Table 15.   Typical Component Using a Reference IC for Feedback Circuit.
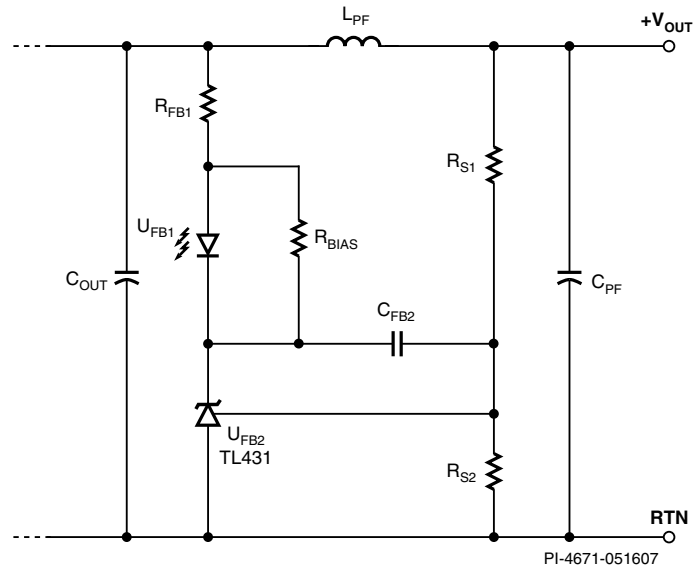
Output Voltage (V)	Feedback Bias Resistor, R_{BIAS} (kΩ)	Opto Series Resistor, R_{FB1} (Ω)	Feedback Capacitor C_{FB2} (nF)	Series Resistor 1, RS1 1% (kΩ)	Sense Resistor 2, RS2 1% (kΩ)
5		27		10	
8		91		22.1	
12	1	160	100	38.3	10
18		430		86.6	
24		470		102	
30		510		110	

TinySwitch-III Key Functional Descriptions and Operations

The TinySwitch-III IC combines a high-voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM or Pulse Width Modulator controllers, the device uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit for sensing and logic, current limit state machine, 5.85 V regulator, BYPASS/MULTI-FUNCTIONAL pin, overvoltage circuit and current limit selection circuitry, over-temperature protection, leading edge blanking and a 700 V power MOSFET. TinySwitch-III IC also incorporates additional circuitry for line undervoltage sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. As most of the key functionalities are already covered by previous sections; this part will focus and gives a brief descriptions of other key functionalities such as enable input, on/off control, current limit state machine, auto-restart, adaptive on-time extension and over temperature protection.

Oscillator

The oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator, first is the maximum duty cycle, DCMAX and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates switching frequency jitter function. The frequency jitter has a modulation of ±4 kHz of the switching frequency at a 1 kHz rate. This reduces EMI emission and reduces the size, cost and number of EMI filter components. Figure 30 illustrates the switching frequency jitter function.
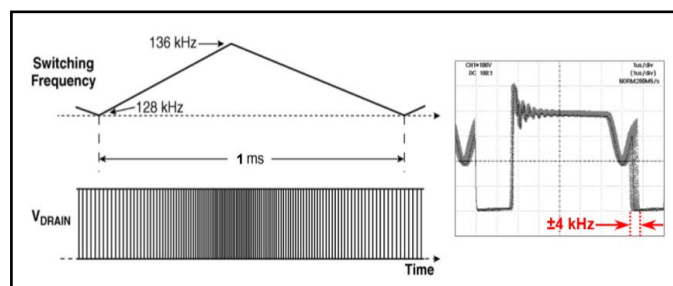
Figure 30. Switching Frequency Jitter Function.

Enable Input

During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than a threshold current is drawn from this pin. Switching resumes when the current being pulled from this pin drops to less than a threshold current. To evenly spread switching cycles, preventing group pulsing, the EN pin threshold current is modulated between 75 μA and 115 μA.

5.85 V Regulator and 6.4 V Shunt Voltage Clamp

The internal 5.85 V regulator charges the bypass capacitor by drawing a current from the DRAIN pin when the MOSFET is off. When the MOSFET is on, the stored energy in the bypass capacitor will continue to charge the device.

In addition, there is a 6.4 V shunt regulator clamping the BYPASS/MULTI-FUNCTION pin at 6.4 V when current is provided to the BYPASS/MULTI-FUNCTION pin through an external resistor. This facilitates powering of TinySwitch-III IC externally through a bias winding to decrease the no-load consumption to well below 50 mW.

BYPASS/MULTI-FUNCTION Pin

The BYPASS/MULTI-FUNCTION pin undervoltage circuitry disables the power MOSFET when the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady-state operation. Once the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady-state operation, it must rise back to 5.85 V to enable (turn-on) the power MOSFET.

ON/OFF Operation with Current Limit State Machine

The internal clock of the TinySwitch-III IC runs all the time. At the beginning of each cycle, it samples the ENABLE/UNDERVOLTAGE pin to decide whether or not to implement a switching cycle and based on the sequence of samples over multiple cycles, it determines the appropriate current limit (Figure 31 illustrate the ON/OFF control operation). At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.
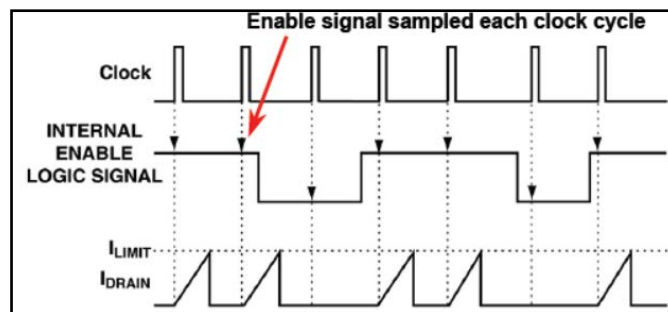
Figure 31. ON/OFF Control Operation.

MOSFET current ramps to a fixed limit every enabled switching cycle. The switching cycles are disabled to maintain the regulation. The effective switching frequency is proportional to the load. This makes the efficiency virtually constant over entire load range, even in standby mode. And the multi-level MOSFET current limit practically eliminates audible noise. The response time of the ON/OFF control scheme is very fast, that it provides tight regulation and excellent transient response, without the needs of loop compensation. Figure 32, 33 and 34, illustrate the Current Limit State Machine Operation for light, mid and full load respectively.

ON/OFF control allows output voltage regulation using a Zener diode as a reference and not required to implement circuitry for frequency compensation.
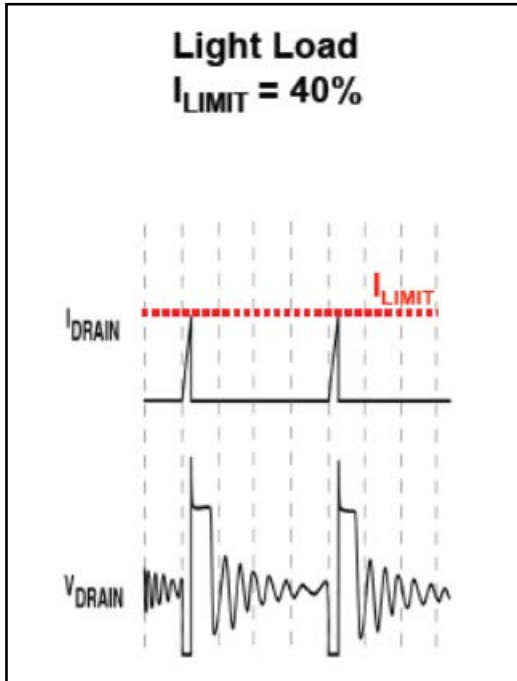

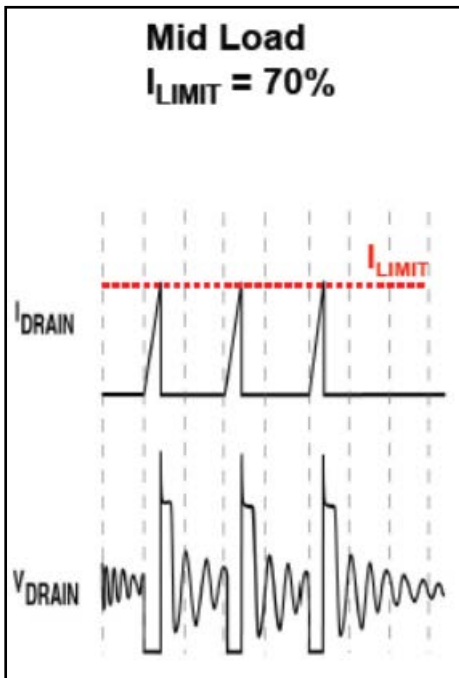Figure 32. Current Limit State Machine at Light Load.

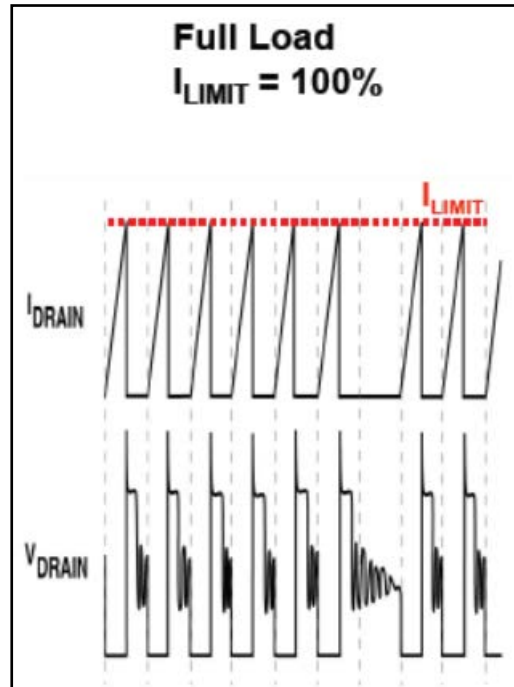Figure 33. Current Limit State Machine at Mid Load.

Figure 34. Current Limit State Machine at Full Load.

Auto-Restart

In the event of a fault condition such as output overload, output short-circuit, or an open-loop condition, TinySwitch-III enters into auto-restart operation. An internal clocked by the oscillator is reset every time the ENABLE/UNDERVOLTAGE pin is pulled low. If the ENABLE/UNDERVOLTAGE pin is not pulled low for 64 ms, the power MOSFET switching is normally disabled for 2.5 seconds (except in the case of line undervoltage condition, in which case it is disabled until the condition is removed). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

Auto-restart limits average output power to < 3% of maximum power during fault condition. This lowers the dissipation in primary clamp, MOSFET, transformer and output diode. It also reduces the size and cost of the output clamp Zener diode if one is used for output overvoltage protection. Figure 35 illustrates the auto-restart sequence and Figure 36 shows the typical auto-restart waveforms.
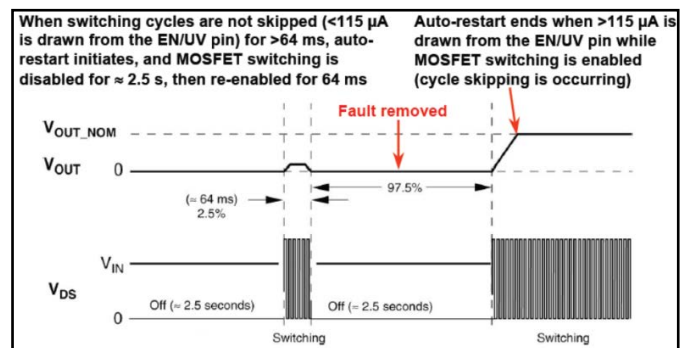
Figure 35. Auto-Restart Waveforms.
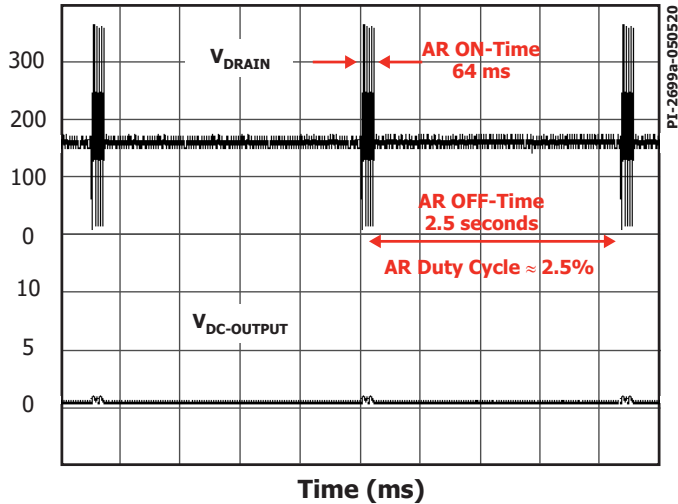
Figure 36. Typical waveform During Auto-Restart.

Adaptive On-Time Extension

The On-time extension feature of TinySwitch-III maximizes the power delivered to the load when the DC input (bulk capacitor) voltage is low. This feature reduces the minimum input voltage required to maintain regulation, extending hold-up time and minimizing the size of bulk capacitor required. The on-time extension is disabled during the start-up of the power supply, until the power supply output reaches regulation and the ENABLE/UNDERVOLTAGE pin has been pulled low. Figure 37 shows the hold-up time difference between with and without the on-time extension.
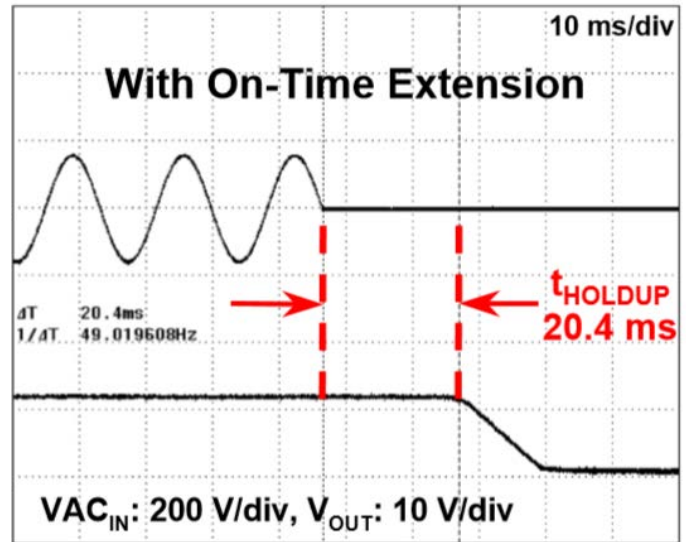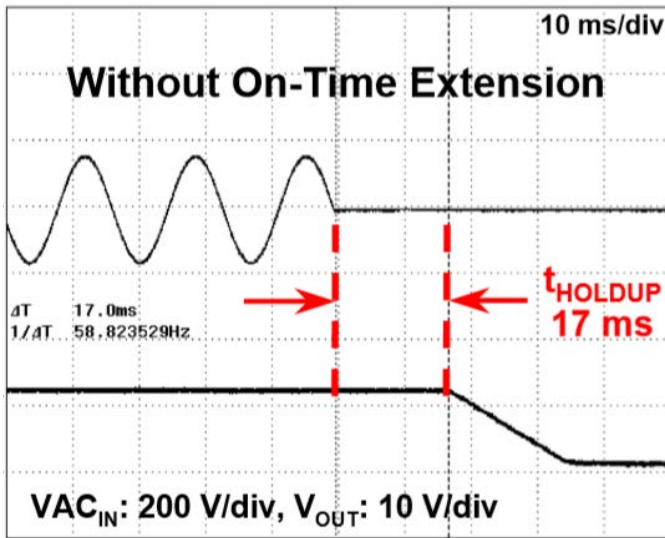
Figure 37. Comparison Between Without and With On-Time Extension.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition. The wide hysteresis keeps the average PCB temperature below 100 °C. This will allow the use of low-cost PCB material and protects the IC, transformer and PCB from temperature rise. Figure 38 illustrate the temperature level for thermal shutdown and its hysteresis.
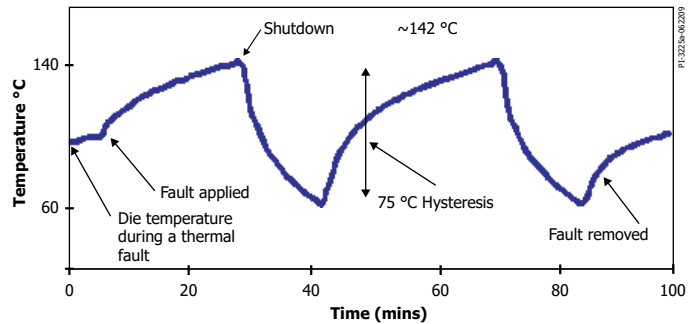
Figure 38. TinySwitch-III Integrated Thermal Shutdown Function.

Key Application Design Considerations

TinySwitch-III Design Considerations

Output Power Table

The data sheet output power table (Table 2) represents the minimum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency of 75%.
3. Minimum data sheet value of I^2f.
4. Transformer primary inductance tolerance of ±10%.
5. Reflected output voltage (VOR) of 135 V.
6. Voltage only output of 12 V with a fast PN rectifier diode.
7. Continuous conduction mode operation with transient KP* value of 0.25.
8. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
9. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink is used to keep the SOURCE pin temperature at or below 110 °C.
10. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*Below a value of 1, KP is the ratio of ripple to peak primary current. To prevent reduced power capability due to premature termination of switching cycles a transient KP limit of ≥ 0.25 is recommended. This prevents the initial current limit (I_{INIT}) from being exceeded at MOSFET turn-on.

For reference, Table 15 provides the minimum practical power delivered from each family member at the three selectable current limit values. This assumes open frame operation (not thermally limited) and otherwise the same conditions as listed above. These numbers are useful to identify the correct current limit to select for a given device and output power requirement.

Peak Output Power Table

Product	20 VAC ±15%			85-265 VAC		
	$I_{LIMIT-1}$	I_{LIMIT}	$I_{LIMIT+1}$	$I_{LIMIT-1}$	I_{LIMIT}	$I_{LIMIT+1}$
TNY274P	9.1 W	10.9 W	9.1 W	7.1 W	8.5 W	7.1 W
TNY275P	10.8 W	12 W	15.1 W	8.4 W	9.3 W	11.8 W
TNY276P	11.8 W	15.3 W	19.4 W	9.2 W	11.9 W	15.1 W
TNY277P	15.1 W	19.6 W	23.7 W	11.8 W	15.3 W	18.5 W
TNY278P	19.4 W	24 W	28 W	15.1 W	18.6 W	21.8 W
TNY279P	23.7 W	28.4 W	32.2 W	18.5 W	22 W	25.2 W
TNY280P	28 W	32.7 W	36.6 W	21.8 W	25.4 W	28.5 W

Table 16.   Minimum Practical Power at Three Selectable Current Limit Levels.

Typical Flyback Power Supply Schematic
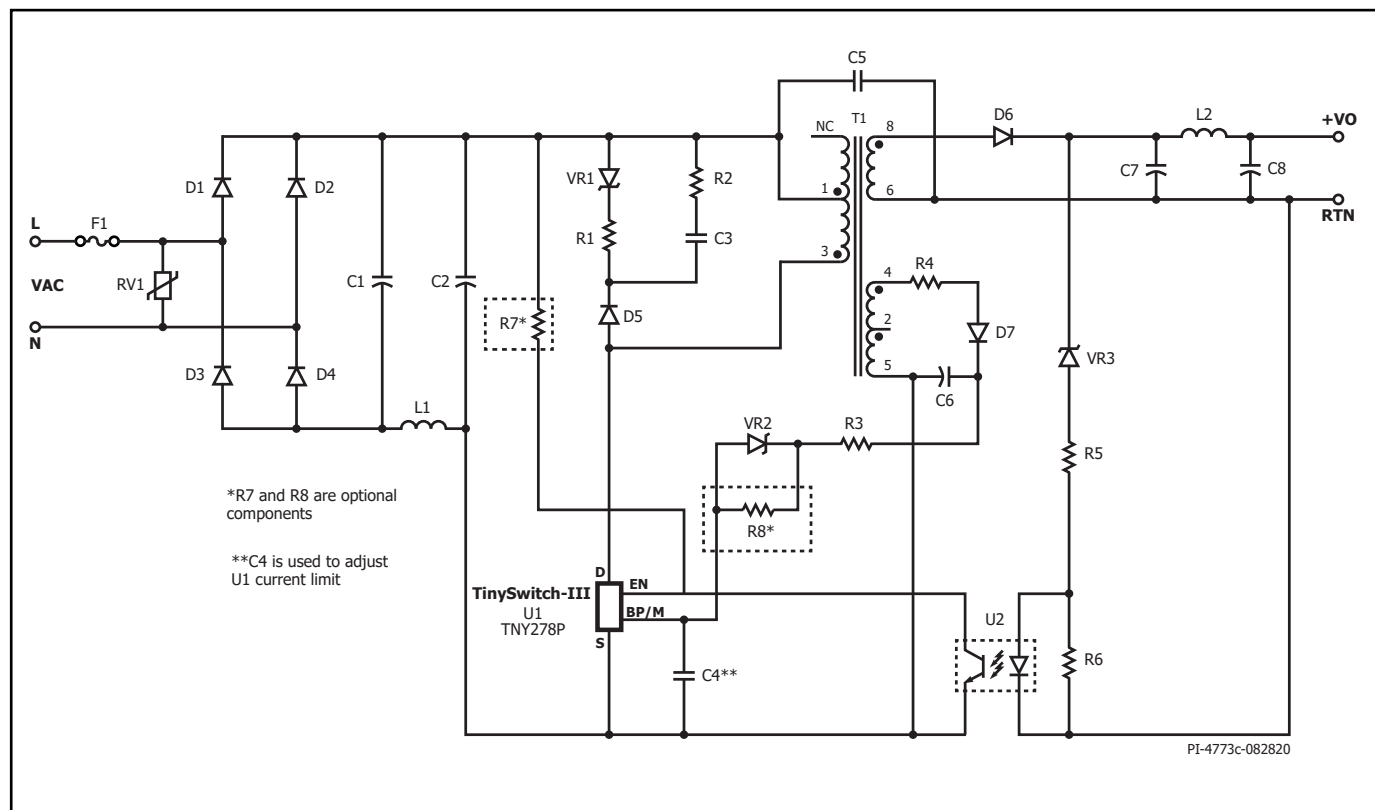
Figure 39.   Typical Schematic TinySwitch-III Flyback Power Supply.

Overvoltage Protection

The output overvoltage protection provided by TinySwitch-III IC uses an internal latch that is triggered by a threshold current typically at 6.5 mA into the BYPASS/MULTI-FUNCTION pin. In addition to an internal filter, the BYPASS/MULTI-FUNCTION pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS/MULTI-FUNCTION pins of the device.

For best performance of the OVP function, it is recommended that a relatively high bias winding voltage is used, in the range of 15 V – 30 V (typically set at 22 V). This minimizes the error voltage on the bias winding due to leakage inductance and also ensures adequate voltage during no-load operation from which to supply the BYPASS/MULTI-FUNCTION pin for reduced no-load consumption.

To achieve a good OVP performance, select a Zener diode voltage that is approximately 6 V above the bias winding voltage. For example, for a 22 V bias voltage, select a 28 V Zener voltage rating. This will be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by placing a low value resistor in series with the bias winding diode and/or to the

OVP Zener as shown by R3 and R4 in Figure 38. Typical value is 10 Ω to 47 Ω. The resistor/s in series also limits the current that will flow on BYPASS/MULTI-FUNCTION pin.

Recommendation to Reduce No-Load Consumption

The TinySwitch-III IC will start in self-powered mode, drawing energy from the BYPASS/MULTI-FUNCTION pin capacitor that is charged from an internal current source. With the addition of a bias winding, it can reduce the no-load consumption from 150 mw down to < 50 mW by supplying the TinySwitch-III IC from the lower bias voltage and inhibiting the internal high-voltage current source. Resistor R3, R4 and R8 shown in Figure 39 should be adjusted to achieve the lowest no-load input power.

Other areas that may help reduce no-load consumption further are:

1.   Low value of primary clamp capacitor, C3.
2.   Schottky or ultrafast diode for bias supply rectifier, D7.
3.   Low ESR capacitor for bias supply filter capacitor, C6.
4.   Implementing RCD–Zener primary clamp configuration.
5.   Tape between primary winding layers and multi-layer tapes between primary and secondary windings to reduce interwinding capacitance.
6.   Optimized primary clamp.

Figure 40 shows the no-load input power without the bias winding and Figure 41, the no-load input power with bias winding supplementation. The data shows the input power at no-load is reduced from 130 mW to less than 45 mW with the supplementation of bias winding into the design. The data is from EP-91 12W Flyback Power Supply.
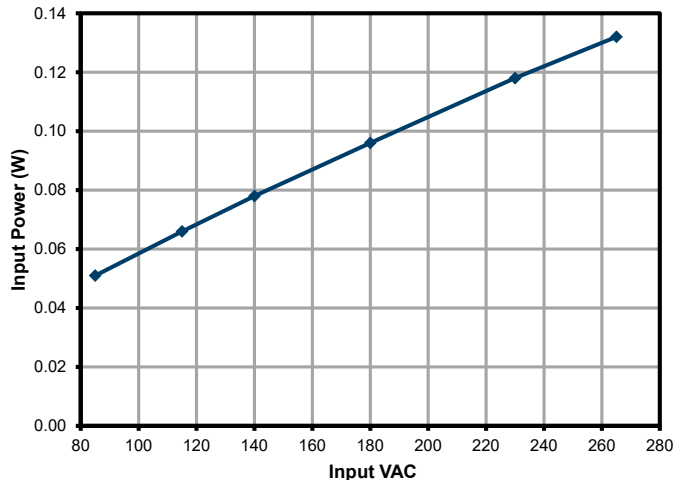

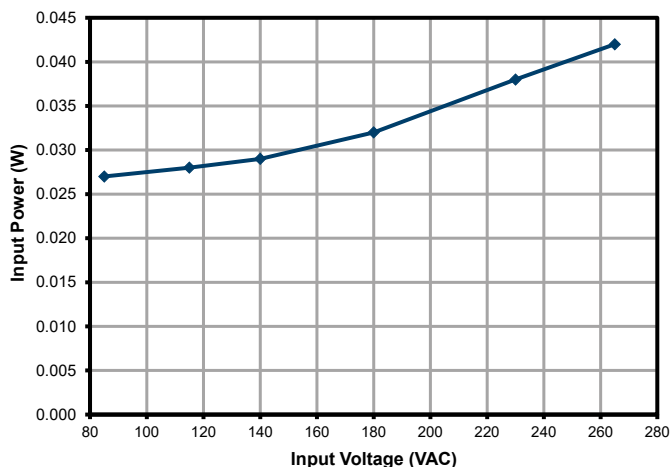Figure 40. No-Load Input Power vs. Input Line Voltage, without Bias Winding.

Figure 41. No-Load Input Power vs. Input Line Voltage, with Bias Winding.

Recommendation for Reducing EMI
1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize conducted and radiated EMI. Care should be taken to achieve a compact loop area. See Figures 42, 43 and 44 for reference.
2. A small resistor (2 – 47 Ω) in series with the bias winding helps reduce radiated EMI.
3. In addition to the simple input π filter (C1, L1 and C2) for differential mode EMI, use of shielding techniques in the transformer to sufficiently attenuate common-mode noise.
4. Primary snubber R2 and C3 are added to act as damping network to reduce high frequency transformer ringing.
5. Adjusting the secondary rectifier RC snubber component values can help reduce high frequency conducted and radiated EMI.
6. A diode with slow t_{RR} (i.e. 500 ns < t_{RR} < 2 μs) as the bias rectifier (D5) is generally good for reducing higher frequency conducted and radiated EMI.

These recommendations combine with the frequency jitter feature of TinySwitch gives excellent conducted and radiated EMI performance.

Recommendation for Increased ESD Immunity
1. Use a spark gap connected between secondary output terminals and one of the AC input. The Reference Design RDR-839 utilizing TNY288P (TinySwitch-4 device) is also applicable for TinySwitch-III. Place the spark gap between RTN and Neutral terminal. A 5.5 mm gap is often sufficient to meet creepage and clearance requirements of applicable safety standards.
2. Use a Y capacitor connected from either positive or negative output terminals to the input bulk capacitor's positive terminal. In the design example EP-91 (Schematic, Figure 45) and DER-228 (Figure 50), the traces routing of Y capacitor C5 is connected across the high-voltage primary positive rail and the other end directly to RTN output terminal. Place the Bypass capacitor CBP as close as possible and directly across BYPASS/MULTI-FUNCTION and SOURCE pins.
   It is not recommended to route the trace of Y capacitor under the transformer especially if the transformer is horizontally oriented to avoid noise to couple magnetically to the trace.
3. Place the bypass capacitor CBP as close as possible and directly across BYPASS/MULTI-FUNCTION and SOURCE pins.
4. Separate the ground trace of optocoupler U2 from the ground trace of bias capacitor C6. The two ground will be star–connected at the bulk capacitor C2 ground plane. This minimizes coupling of ESD. See Figure 44 for layout and component placement reference and Figure 42 and 43 for schematic reference (primary- and secondary-side).

Audible Noise
The skip cycle mode of operation applied in TinySwitch-III IC can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 Gauss or 300 mT. Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increase losses that result. Other simple techniques such as adding glue to the transformer core gaps also helps in limiting the audible noise. Higher flux densities are possible; however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, a capacitor having a different dielectric or construction such as a film type capacitor may help to eliminate the audible noise generated by the ceramic capacitor.

Another audible noise generator is the use of EEL types of core. They are long cores which increases the audible noise due to tuning fork effect. If EEL type of core is the only option in the design, lowering the flux density may help to reduce the audible noise.

TinySwitch-III Layout Considerations

Layout
See Figures 42, 43 and 44 for a recommended circuit board layout for TinySwitch-III.

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor (CBP)
The BYPASS/MULTI-FUNCTIONAL pin capacitor must be located directly adjacent to the BYPASS/MULTI-FUNCTIONAL and SOURCE pins.

If a 0.1 μF bypass capacitor has been selected it should be a high frequency ceramic type (e.g. with X7R dielectric). It must be placed directly between the ENABLE and SOURCE pins to filter external noise entering the BYPASS pin. If a 1 μF or 10 μF bypass capacitor was selected, then an additional 0.1 μF capacitor should be added across BYPASS and SOURCE pins to provide noise filtering (see Figure 42).

ENABLE/UNDERVOLTAGE
Keep traces connected to the ENABLE/UNDERVOLTAGE pin short and, as far as is practical, away from all other traces and nodes above source potential including, but not limited to, the bypass, drain and bias supply diode anode nodes.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and TinySwitch-III should be kept as small as possible. Illustrated in Loop 1 of Figure 41.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener (~ 200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and TinySwitch-III IC. Illustrated in Loop 2 of Figure 41.

Thermal Considerations
The SOURCE pins are internally connected to the IC lead frame and provide the main path to remove heat from the device. Therefore, all the SOURCE pins should be connected to a copper area underneath the TinySwitch-III IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area should be maximized for good heat sinking. Similarly, for axial output diodes, maximize the PCB area connected to the cathode. The grounding and copper plating at the Source pins are shown on Figure 44.

Sufficient copper area should be provided on the board to keep the temperature safely below absolute maximum limits. It is recommended that the copper area to which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 90 ºC when operating under maximum power, lowest rated AC input voltage and at the nominal ambient temperature.

Y Capacitor
The placement of the Y capacitor should be directly from the primary input filter capacitor positive terminal to the common / return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the TinySwitch-III device. It is not recommended to route the trace of Y capacitor under the transformer especially if the transformer is horizontally oriented to avoid noise to couple magnetically to the trace.

Note – if an input η (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Optocoupler
Place the optocoupler physically close to the TinySwitch-III IC minimizing the primary-side trace lengths. Keep the high current, high-voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

Output Diode
For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor, should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

ESD Immunity
The spark gap is best placed between output return and/or positive terminals and one of the AC inputs. A 6.4 mm is more than sufficient to meet the creepage and clearance. See AN-82 TinySwitch-4 Design Guide for the layout implementation of spark gap.

PC Board Leakage Currents
TinySwitch-III IC is designed to optimize energy efficiency across the power range and particularly in standby/no-load conditions. Current consumption has therefore been minimized to achieve this performance. The ENABLE/UNDERVOLTAGE pin undervoltage feature for example has a low threshold (~1 μA) to detect whether an undervoltage resistor is present.

Parasitic leakage currents into the ENABLE/UNDERVOLTAGE pin are normally well below this 1 μA threshold when PC board assembly is in a well-controlled production facility. However, high humidity conditions together with board and/or package contamination, either from no-clean flux or other contaminants, can reduce the surface resistivity enough to allow parasitic currents >1 μA to flow into the ENABLE/UNDERVOLTAGE pin. These currents can flow from higher voltage exposed solder pads close to the ENABLE/UNDERVOLTAGE pin such as the BYPASS/MULTI-FUNCTIONAL pin solder pad preventing the design from starting up. Designs that make use of the undervoltage lockout feature by connecting a resistor from the high-voltage rail to the ENABLE/UNDERVOLTAGE pin are not affected.

If the contamination levels in the PC board assembly facility are unknown, the application is open frame or operates in a high pollution degree environment and the design does not make use of the undervoltage lockout feature, then an optional 390 kW resistor should be added from ENABLE/UNDERVOLTAGE pin to SOURCE pin to ensure that the parasitic leakage current into the ENABLE/UNDERVOLTAGE pin is well below 1 μA. Note that typical values for surface insulation resistance (SIR) where no-clean flux has been applied according to the suppliers' guidelines are >>10 MW and do not cause this issue.
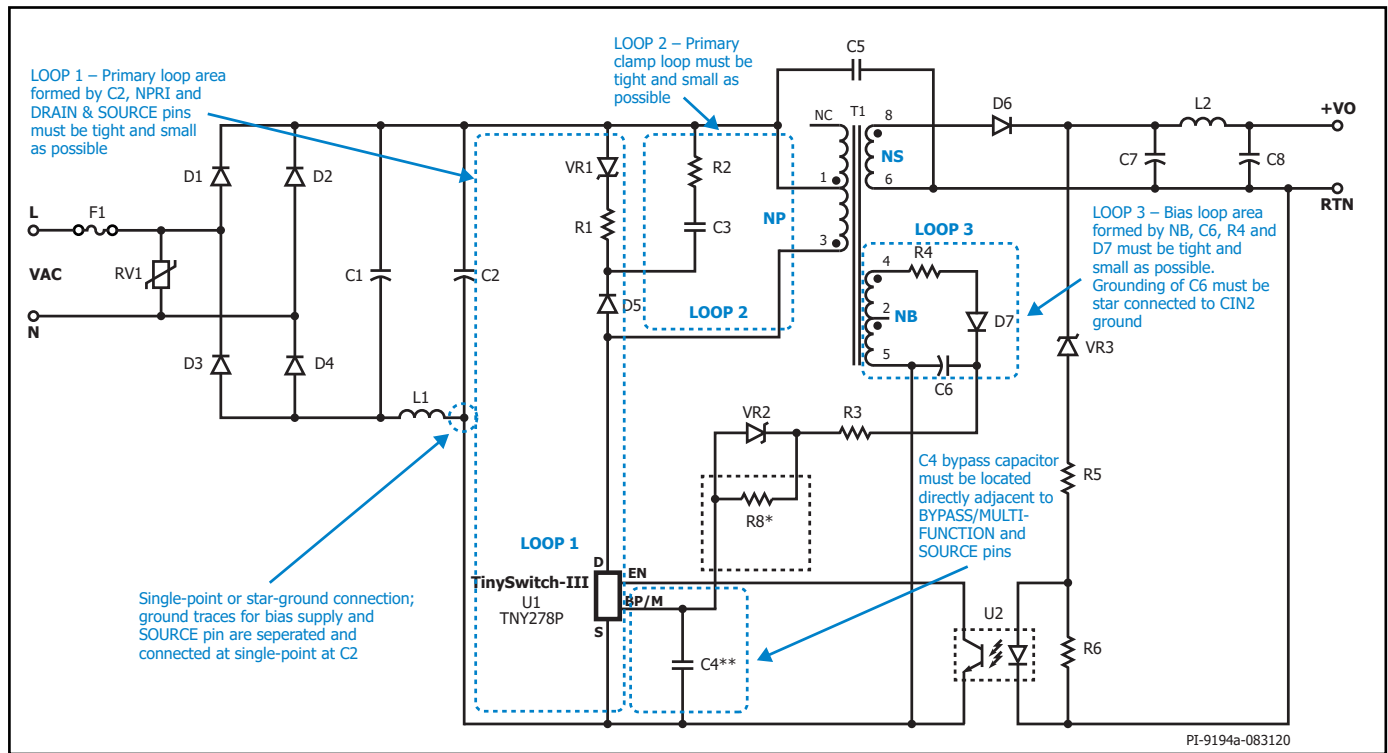
Layout Considerations

Primary

LOOP 1 – Primary loop area formed by C2, NPRI and DRAIN & SOURCE pins must be tight and small as possible

LOOP 2 – Primary clamp loop must be tight and small as possible

LOOP 3 – Bias loop area formed by NB, C6, R4 and D7 must be tight and small as possible. Grounding of C6 must be star connected to CIN2 ground

C4 bypass capacitor must be located directly adjacent to BYPASS/MULTI-FUNCTION and SOURCE pins

Single-point or star-ground connection; ground traces for bias supply and SOURCE pin are seperated and connected at single-point at C2

PI-9194a-083120

Figure 42.   Primary-Side Typical Schematic of TinySwitch-III Showing Critical Loops Area, Critical Component Traces and Single-Point or Star Grounding.

Secondary
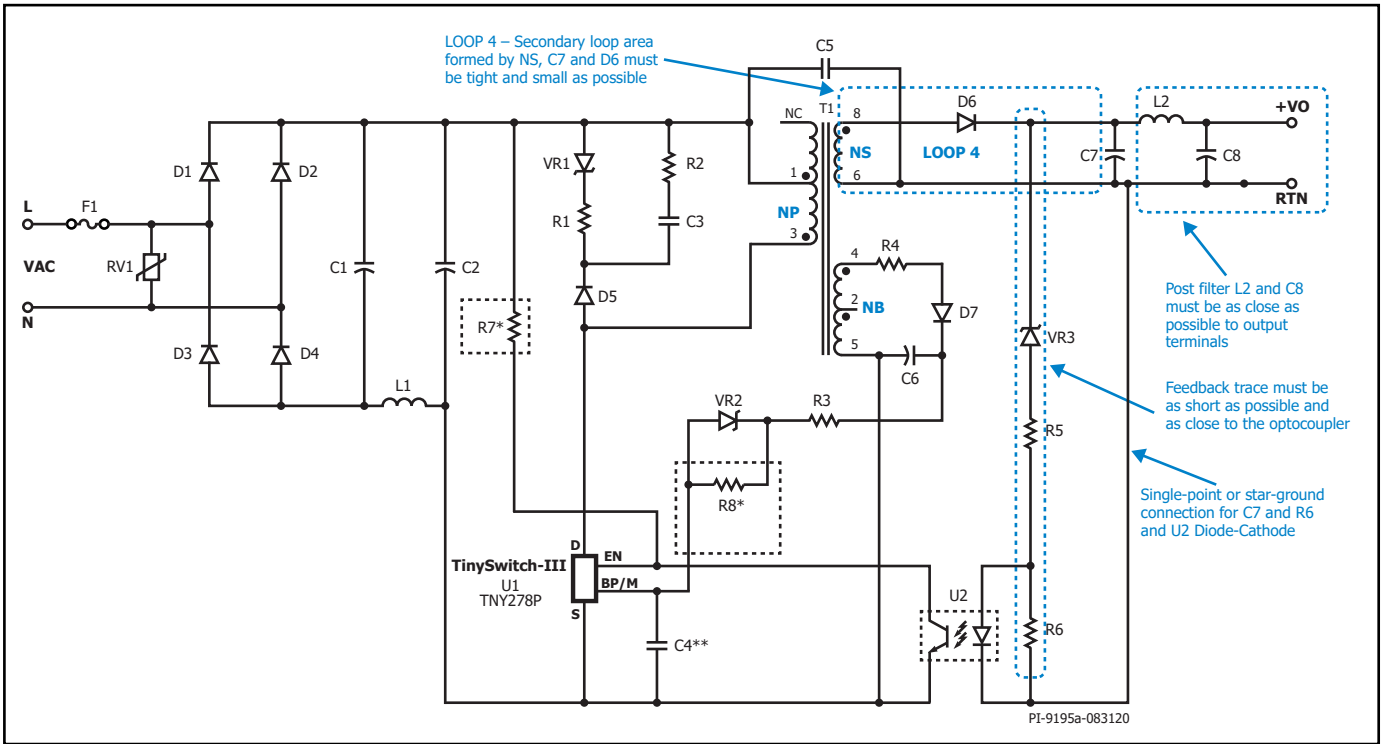
Figure 43. Schematic using TinySwitch-III Device Showing Critical Loops Area, Critical Component Traces and Single-Point or Star Grounding at the Secondary-Side.

Layout Example
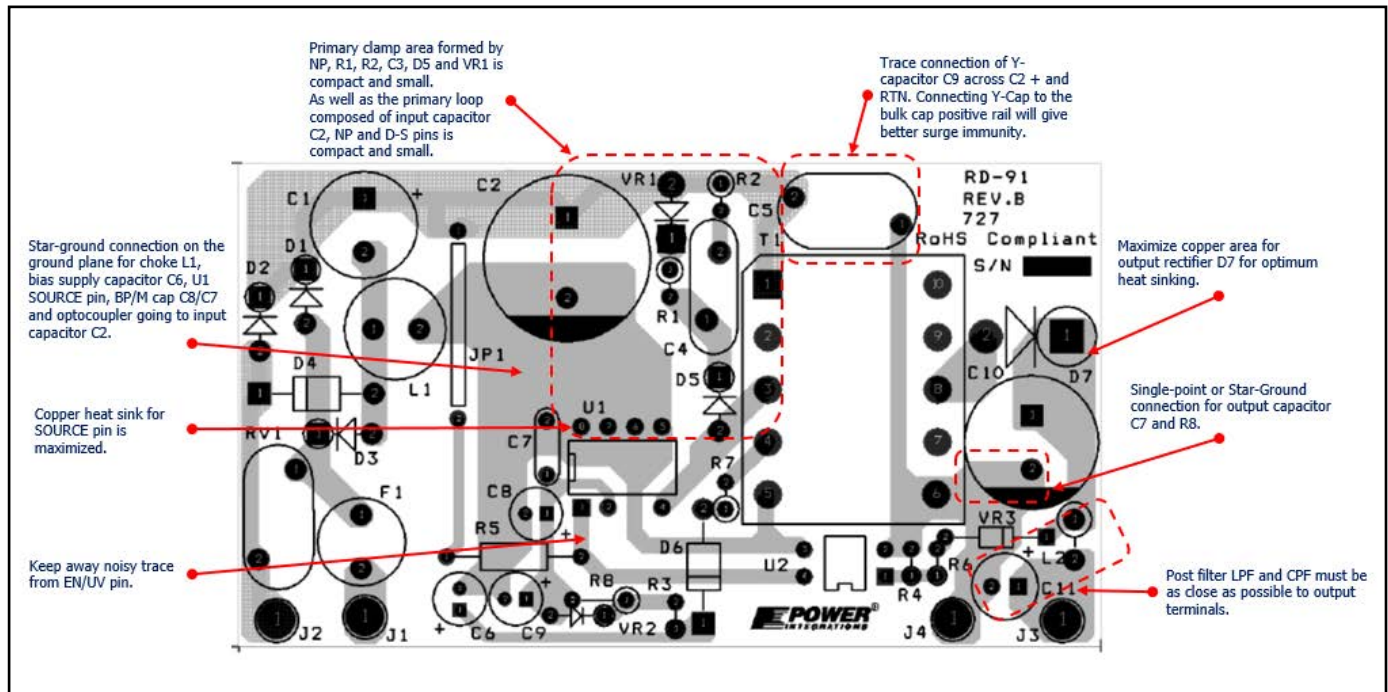
Figure 44. TinySwitch-III Layout Guidelines.

Quick Design Checklists

As with any power supply design, all TinySwitch-III IC designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} does not exceed 650 V at highest input voltage and peak (overload) output power. The 50 V margin to the 700 V B_{VDSS} specification gives margin for design variation.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation

and excessive leading edge current spikes at start-up. Repeat under steady-state conditions and verify that the leading edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.

3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for TinySwitch-III, transformer, output diode, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of TinySwitch-III IC as specified in the data sheet. Under low-line, maximum power, a maximum TinySwitch-III SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Application Example
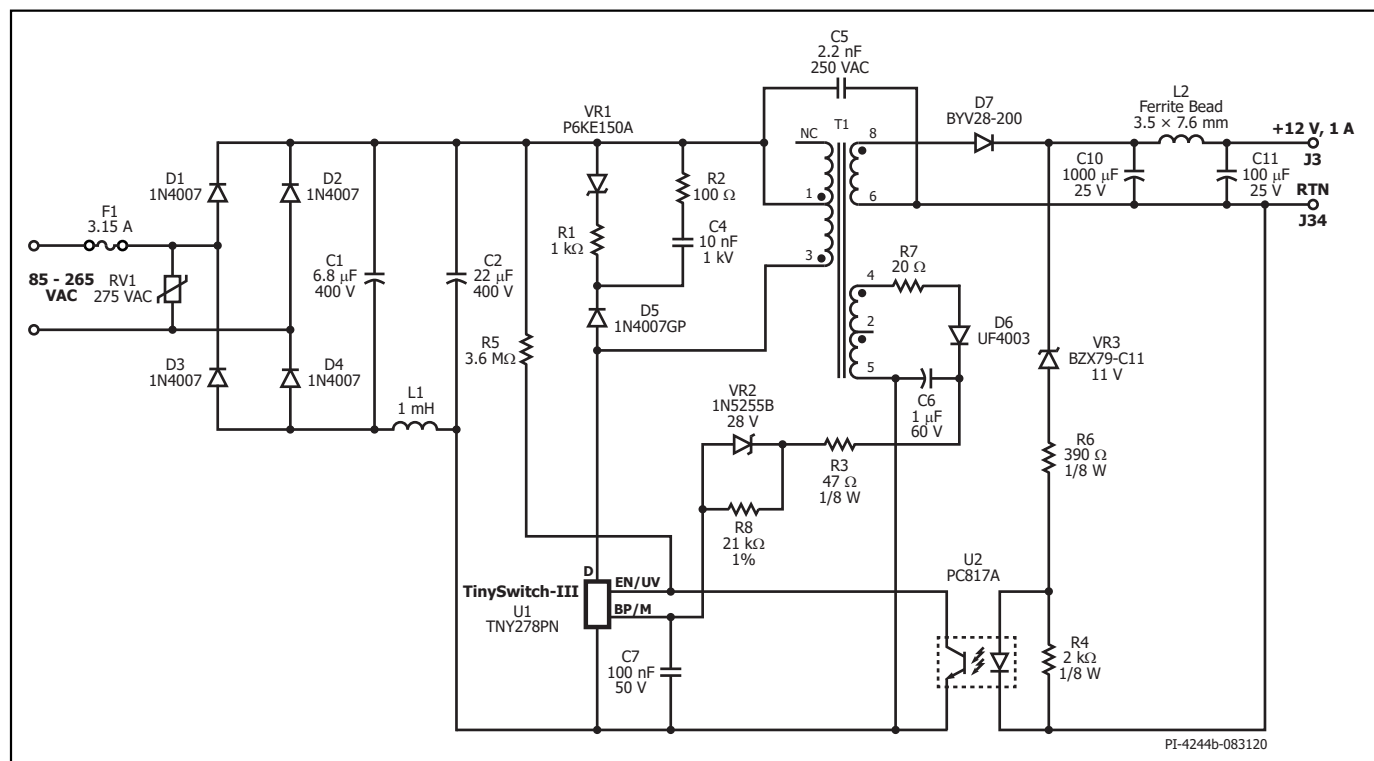
Figure 45. Schematic of EP-91 12 W, 12 V / 1 A Power Supply using TinySwitch-III TNY278P.

12 W Universal Input Flyback Power Supply Using TNY278P

The circuit shown in Figure 45 is a low-cost, high efficiency, flyback power supply designed for 12 V, 1 A output from universal input (85 VAC to 265 VAC) using TNY278P.

The power supply features undervoltage lockout, primary sensed output overvoltage latching shutdown protection, high efficiency (>80%), and low no-load consumption. Output regulation is accomplished using a simple Zener reference and optocoupler feedback.

AC power is rectified and filtered by diodes D1-D4, C1, L1 and C2 to create the high-voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within TNY278P (U1). Inductor L1 together with C1 and C2 formed an input π filter that attenuates differential mode noise conducted EMI. Y capacitor C5 is used connected across the positive trace of bulk capacitor C2 and directly to the RTN terminal to minimize common mode noise. When the MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consist of D5, C4 and R2. Resistors R1 and Zener diode VR1 provides hard clamping of the drain voltage, only conducting during output overload. Resistor R2 allows the use of a slow recovery (with a recovery time of ≤ 2 μs.), low-cost glass passivated rectifier diode by limiting the reverse current through D5. The selection of slow diode also improves efficiency and conducted EMI. Shielding techniques in the transformer is utilized to reduce common mode EMI displacement currents. The techniques implemented in this design combined with the frequency jitter of TNY278P gives an excellent conducted and radiated EMI performance.

The power secondary winding is rectified and filtered by D7, C10, L2 and C11 to generate the 12 V output voltage. The output voltage is determined by the Zener diode VR3, voltage drop across the opto-coupler U2 and resistor R6. When the output voltage exceeds the sum of the Zener, R6 and optocoupler LED forward drop, current will flow in the optocoupler (U2) LED. This will cause the transistor of the optocoupler to sink current. When this current exceeds the ENABLE/UNDERVOLTAGE pin threshold current (>115 μA), the next switching cycle is inhibited. When the output falls below the feedback threshold, a conduction cycle is allowed to occur and by adjusting the number of enabled cycles, output regulation is maintained. As the load reduces, the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements. The value of R4 was calculated to bias VR3 to about 0.5 mA when it goes into reverse avalanche conduction. Resistor R6 limits the maximum current during load transients. The Zener diode VR3 can be replaced by a TL431 reference circuit for improved accuracy.

To decrease the no-load consumption, the design implements the used of bias winding to generate the bias voltage and feeds current into the BYPASS/MULTI-FUNCTIONAL pin via resistor R3 and R8, inhibiting the internal high-voltage current source that normally maintains the BYPASS/MULTI-FUNCTIONAL pin capacitor voltage (C7) during the internal MOSFET off-time. R7, D6 and C6 rectified and filtered the bias winding voltage. Bypass capacitor C7 with a value of 0.1 μF determines the current limit which is set at standard limit.

For output overvoltage shutdown, the design implements the PI's proprietary primary overvoltage sensing via the bias winding voltage during MOSFET off-time. This circuit configuration eliminates the use of an additional optocoupler. When the power MOSFET is off, the reflected bias winding is proportional to the output voltage by a factor determined by the bias and output turns ratio. When this voltage exceeds the sum of Zener diode VR2 breakdown voltage and the BYPASS (BP/M) pin voltage of U1 (28 V + 5.85 V_{TYP_BP}), an overvoltage occurs and current begins to flow into the BYPASS pin. If this current exceeds 6.5 mA, an internal latching shutdown circuit in U1 is activated. Reset is accomplished by removing input power and allowing the BYPASS pin voltage to drop below 2 V. Resistors R3 and R7 provides additional filtering of the bias voltage, with R3 also limiting the maximum current into the BYPASS pin during overvoltage condition.

The line undervoltage (UV) lockout detection is accomplished by sensing the input rectified DC voltage. This feature is enable by connecting resistor/s (R5 on Figure 43) from the input capacitors to the EN/UV pin of U1. This feature defines the input start-up voltage of the power supply. If the resistors are implemented, power MOSFET at start-up is disabled until the current that feeds into the ENABLE/UNDERVOLTAGE pin exceeds 25 μA.

This prevents the power supply output from glitching when the input voltage is below the normal operating range. The undervoltage threshold also resets the output overvoltage latching shutdown. After AC removal, once the voltage of the DC bus falls below the undervoltage threshold, the OV latch reset. For example, the engineering design EPR-91, the resistor R5 value is 3.6 MΩ. This will exceed the threshold of 25 μA on ENABLE/UNDERVOLTAGE pin at approximately 92 VDC across the input capacitor C2 or equivalent to 65 VAC at the mains input. The resistor voltage should not exceed VMAX. In other designs, the resistor R5 is a series combination of two to three ladder resistors to comprise the total resistance value of the target undervoltage limit and also not to exceed the voltage rating of the resistor.

The transformer T1, implements the shielding techniques to reduce common mode noise. Engineering design reference EP-91 further elaborate the transformer design construction

No-Load Consumption

Utilizing a bias winding, the no-load input power is reduced to 42 mW compared with self-bias which has 150 mW input power at no-load. It also allows the implementation of primary OVP shutdown circuit sensing the bias voltage during overvoltage or open-loop condition. Figure 46 shows the input power at no-load condition and different input voltage for EP-91.
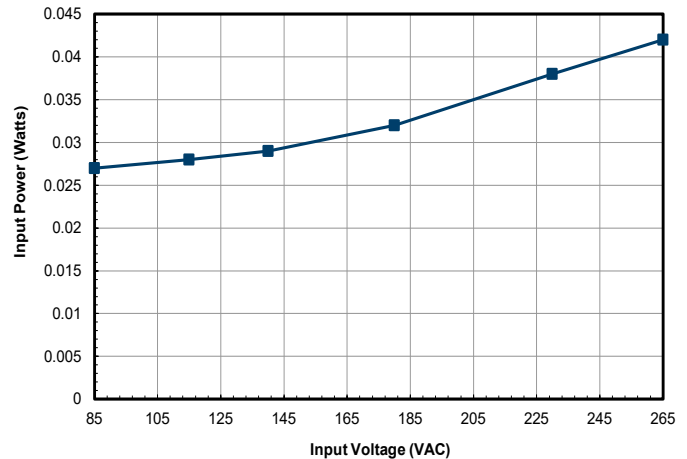

Figure 46. EP-91 12 W No-Load Input Power with Bias Winding.

Standby Power Availability

The ON/OFF control keeps the efficiency high even at standby and sleep mode. Figure 47 shows the power availability during standby mode.
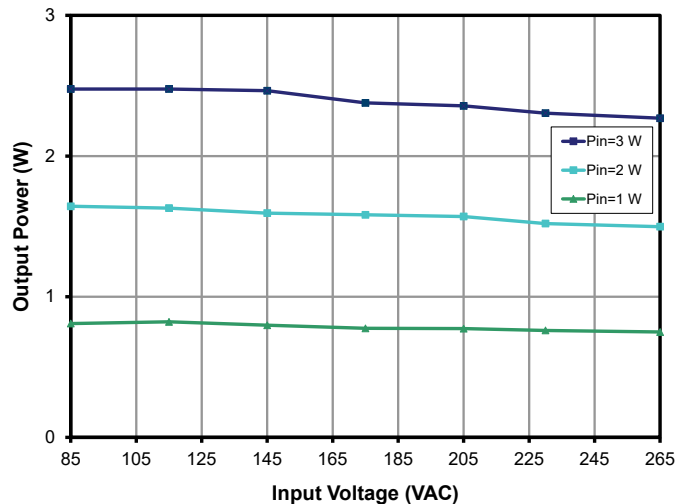

Figure 47. EP-91 Input Power at Standby Mode and Different Input Voltage.

Overvoltage Shutdown Waveforms
Figure 48 and 49 shows the overvoltage response of the EP-91 at
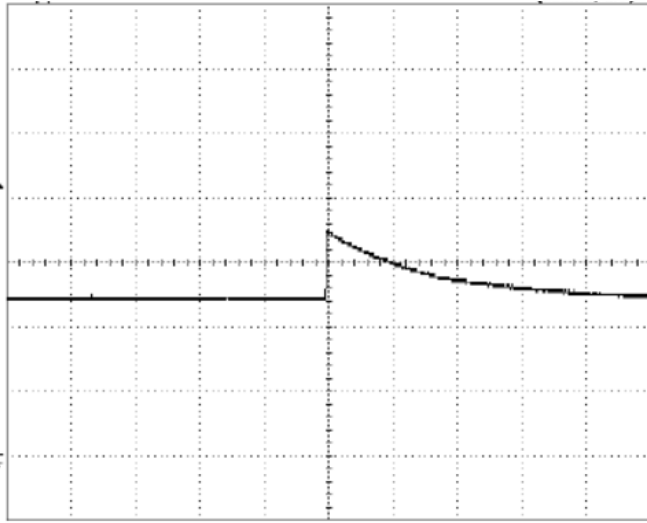no-load and full load conditions both at 265 VAC input.

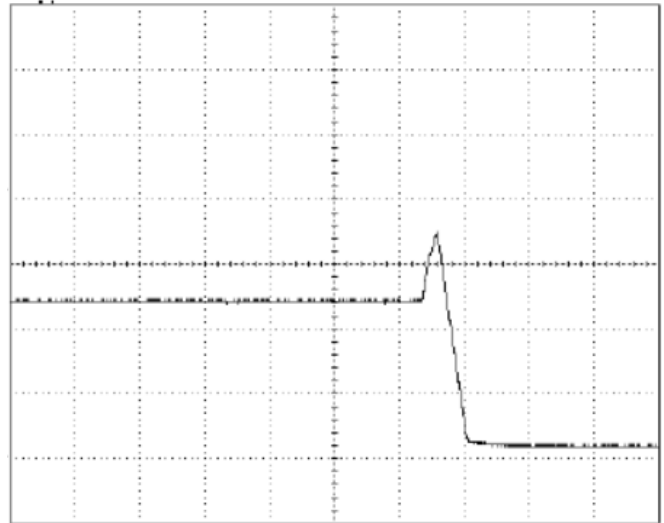Figure 48. EP-91 Overvoltage Shutdown Response at No-Load.

Figure 49. EP-91 Overvoltage Shutdown Response at Full Load.
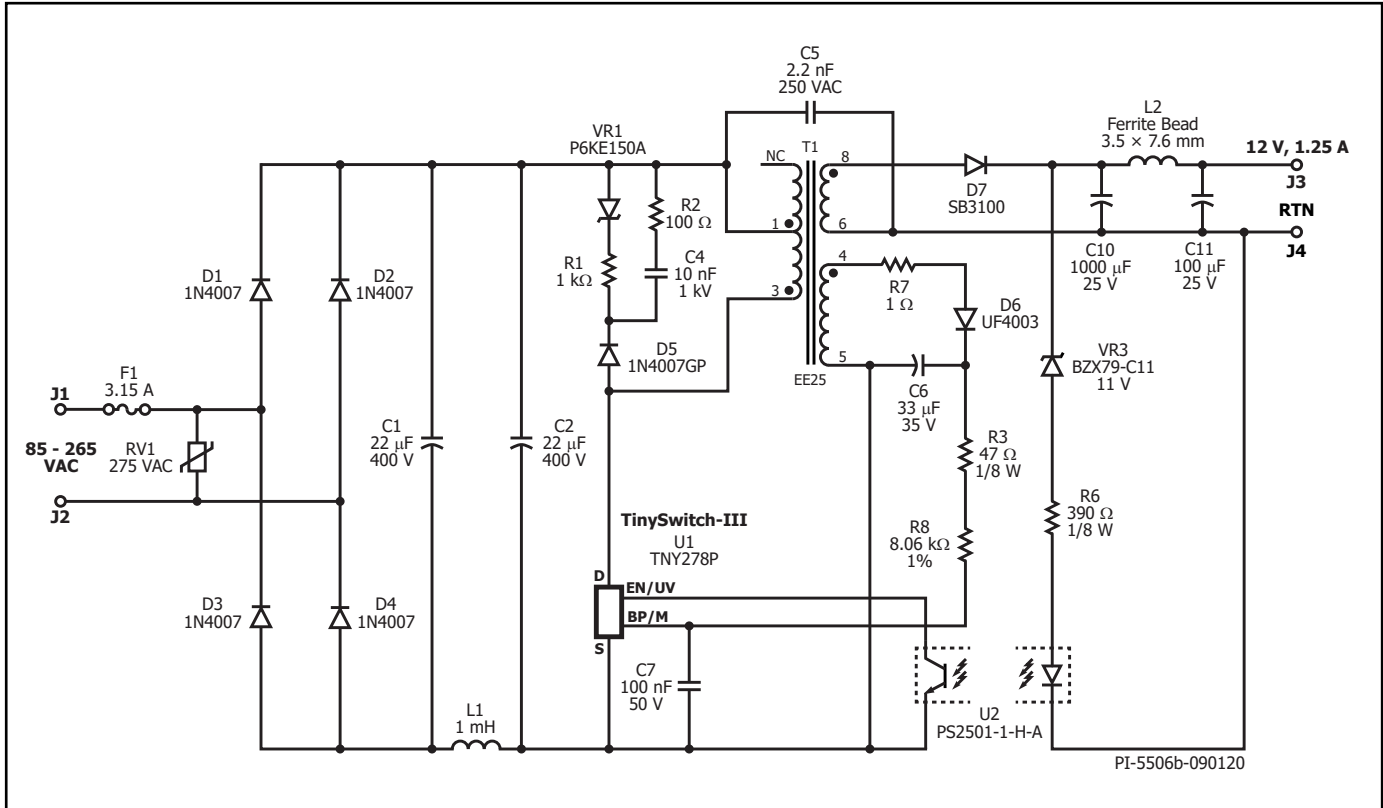
Application Example 2

Figure 50. Schematic of DER-228 15 W, 12 V / 1.25 A Flyback Power Supply using TinySwitch-III TNY278P.

15 W Universal Input Flyback Power Supply Using TNY278P

The circuit shown in Figure 50 is a low-cost, high efficiency, flyback power supply designed for 12 V, 1.25 A output from universal input (85 VAC to 265 VAC) using TNY278P.

The power supply features undervoltage lockout, high efficiency (>80%), and low no-load consumption (<30 mW). Output regulation is accomplished using a simple Zener reference and optocoupler feedback.

DER-228 Performance Data
This section will show some test results of DER-228 that highlights the performance using TinySwitch-III TNY278P IC.

Efficiency
The ON/OFF control scheme employed by TinySwitch-III yields flat efficiency response across the 25% to 100% load range required for compliance with Energy Star and EuP energy efficiency standards for external power supplies (EPS). Even at 10% of the power supply's full rated output power, the efficiency remains above 75%, providing excellent standby performance. Figure 51 shows the active mode efficiency and Table 16 the average efficiency which exhibits a very good margin in reference with the efficiency compliance standard.

Active Mode Efficiency
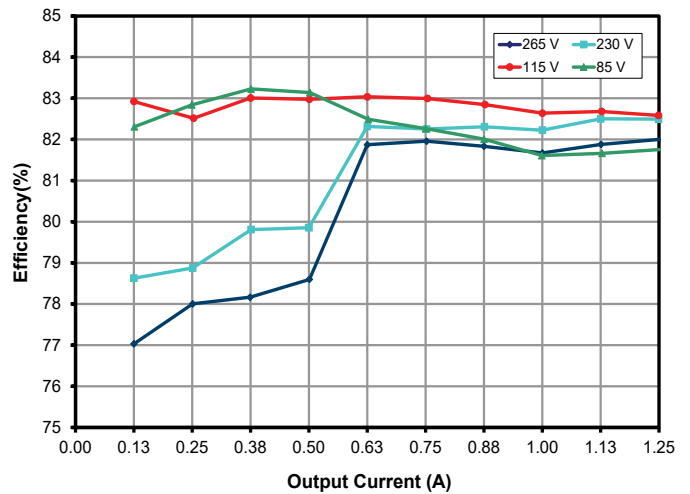
Figure 51. Efficiency vs. Output Current.

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	82.4	79.2
50	82.7	81.8
75	82.6	82.0
100	82.5	82.4
Average	82.5	81.4

Table 17.   Average Efficiency.

No-Load Input Power
The design optimization yields <20 mW of input power at no-load and input voltage of 265 VAC. Figure 52, shows the no-load input power performance of the design.
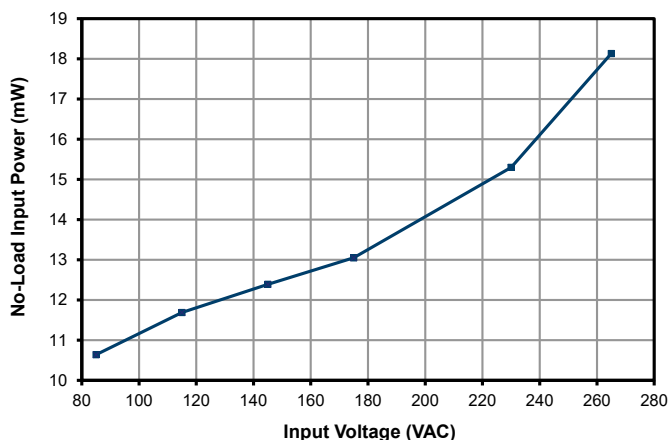

Figure 52. No-Load Input Power at Different Input Voltage.

Output Voltage Response
The design is also subjected with several test conditions such different line and load settings, load transient response, start-up and output ripple and noise. Performance data demonstrated a remarkable output voltage regulation and response, indicating a very good stability feedback loop of the design.

Output Voltage Line and Load Regulation
Figure 53 shows the output voltage regulation at different load and line conditions. The data validated a stable output voltage.
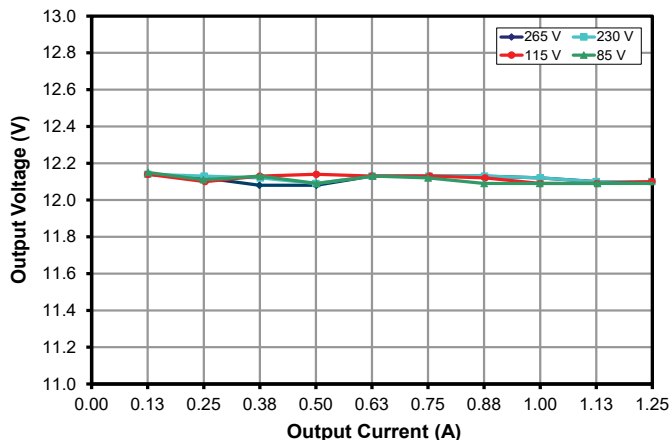
Figure 53. Load and Line Regulation.

Load Transient Response
The measured maximum and minimum change of the output voltage during load transient is 50 mV (Figure 54 and 55). The data validated the claim of ON-OFF control scheme having a fast response.
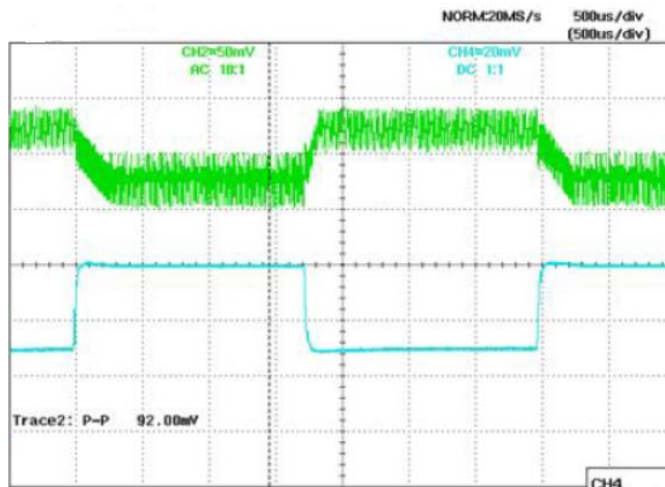
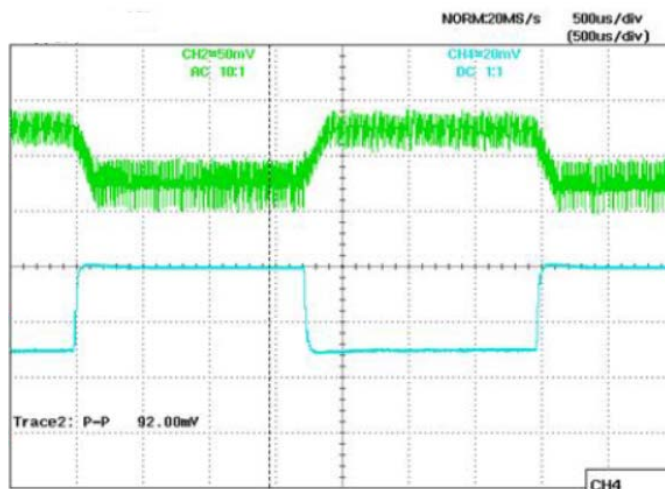Figure 54. 50% - 100% Load Transient at 115 VAC.

Figure 55. 50% - 100% Load Transient at 230 VAC.

Output Voltage Start-Up Response
Start-up in full resistive load and no-load yield a monotonic rise time of the output voltage (Figure 56 and 57).

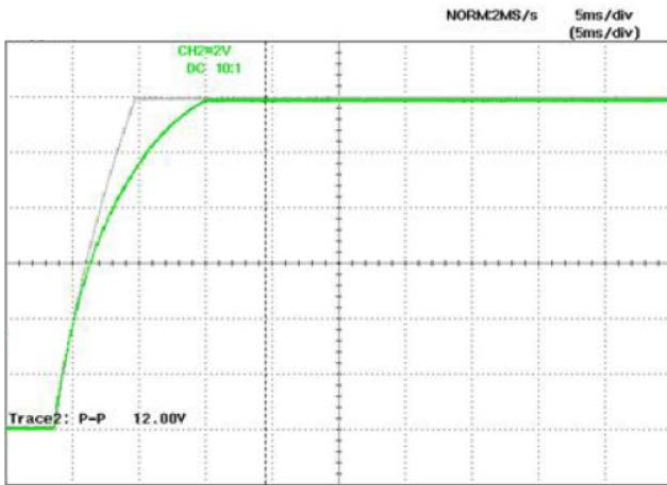Black Trace – Start-up at No-load
Green Trace – Start-up at Full Load

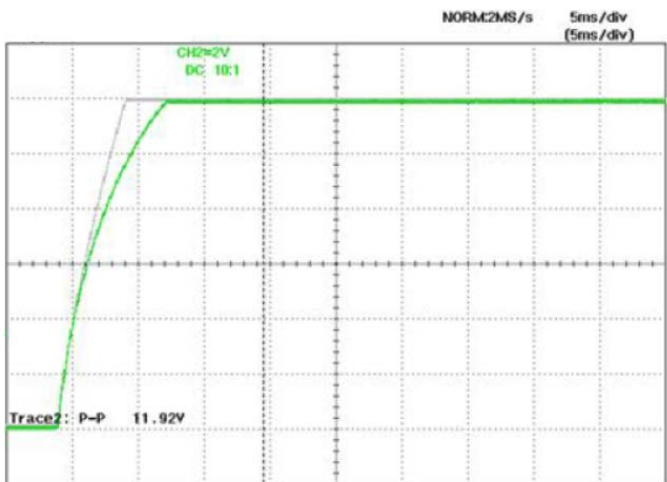Figure 56.   50% - Start-Up Profile at 115 VAC.

Figure 57.   50% - Start-Up Profile at 230 VAC.

Output Ripple and Noise
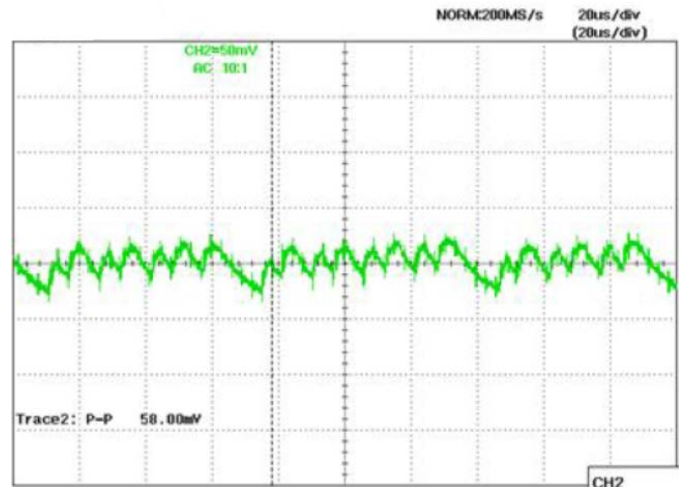The maximum output ripple measurement is 58 mV at worst-case condition as illustrated on Figure 58 and 59.

Figure 58.   Output Ripple at Full Load and 85 VAC Input.
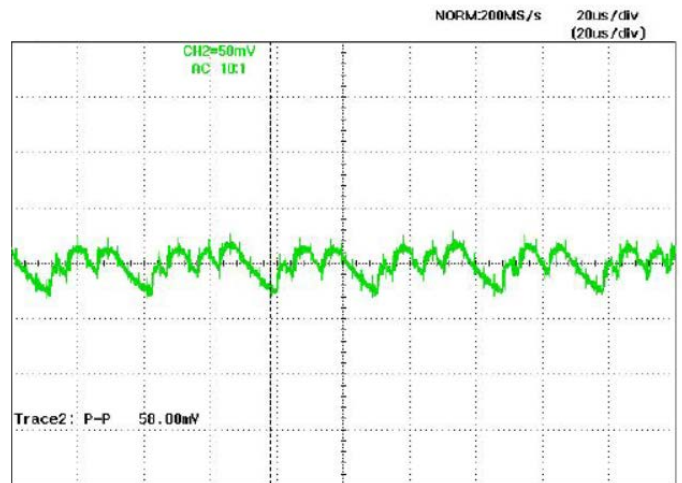
Figure 59.   Output Ripple at Full Load and 230 VAC Input.

Switching Waveforms

The data shows that the drain voltage are well within the maximum drain voltage of the internal MOSFET of the IC. It also demonstrates the current limit state machine having different current limit at high-line and low-line.
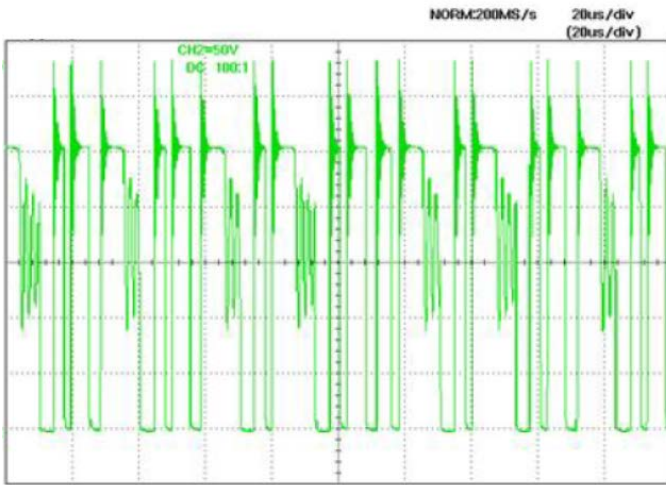

Figure 60. Drain Voltage and Current of the Primary MOSFET at 115 VAC.
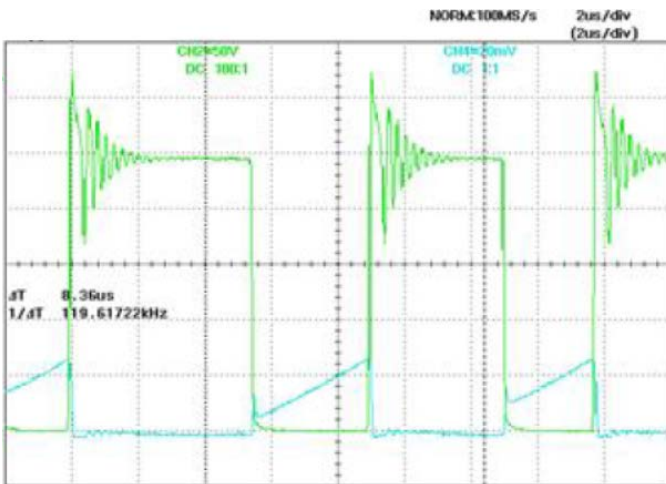

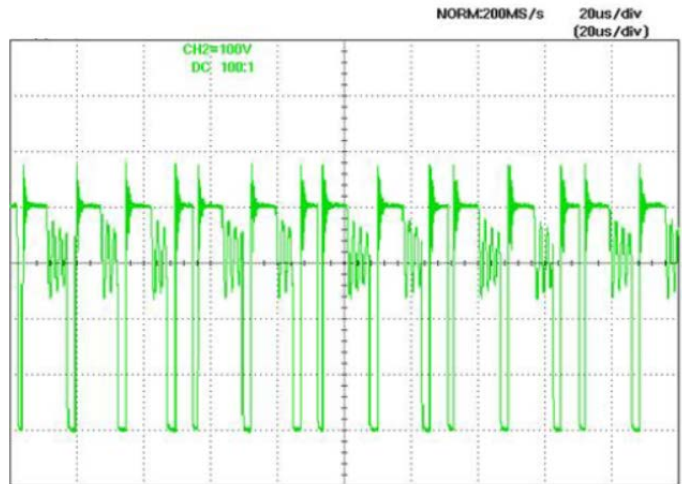Figure 61. Drain Voltage Switching Cycles of the Primary MOSFET at 115 VAC.

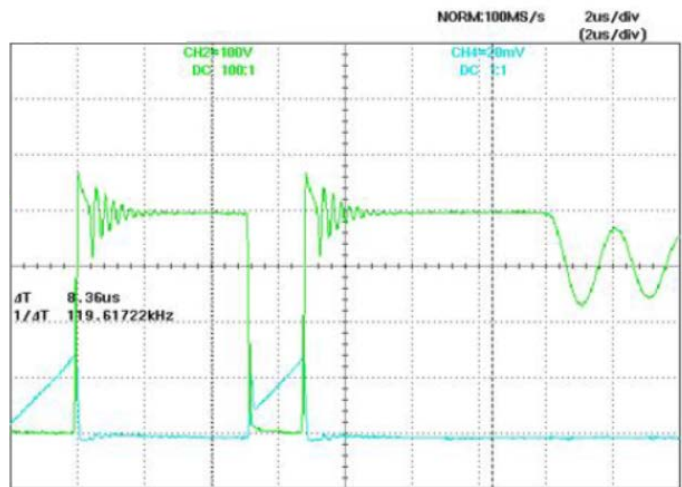Figure 62. Drain Voltage and Current of the Primary MOSFET at 230 VAC.

Figure 63. Drain Voltage Switching Cycles of the Primary MOSFET at 230 VAC.

Conducted EMI Response

Figures 64 and 65 shows the conducted EMI both at 115 VAC and 230 VAC at 100% load, exhibiting a very good performance with higher margin greater than 6 dB both average and quasi-peak.
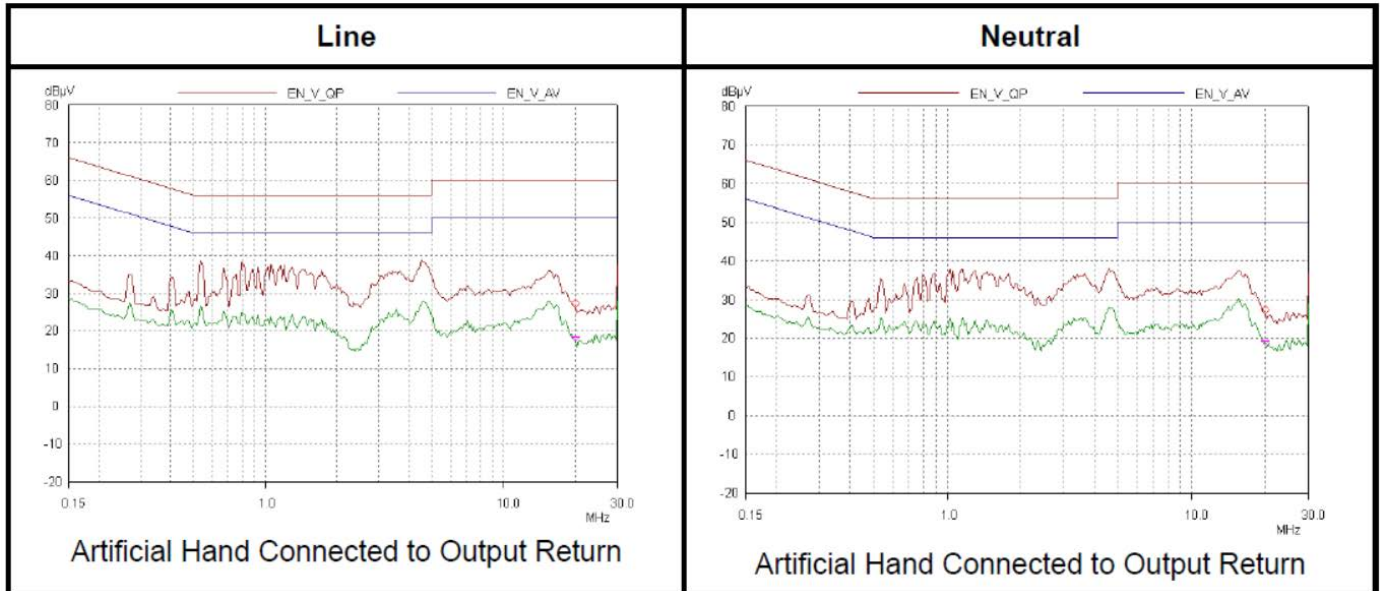

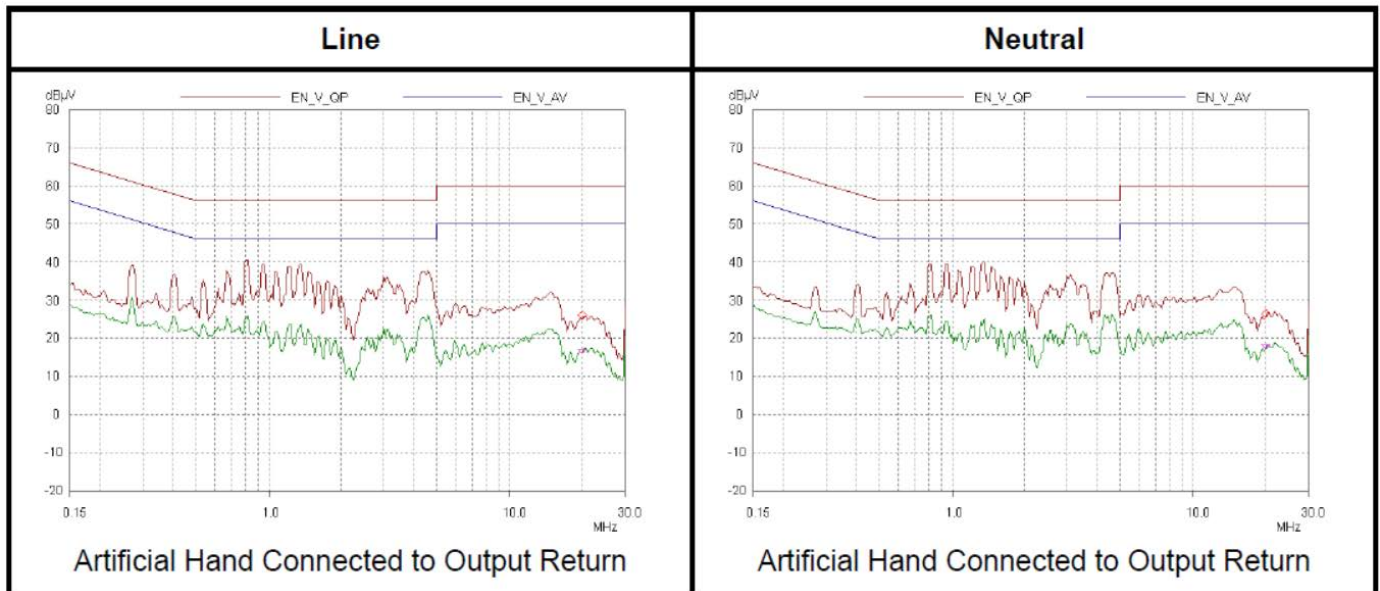Figure 64. Conducted EMI at Full Load and 115 VAC.

Figure 65. Conducted EMI at Full Load and 230 VAC.

In-depth Information

The In-depth Information section is divided into two parts. The first part discusses the Continuous Mode or CCM operation of flyback power supply, and the second part is for Discontinuous Mode or DCM operation. The other steps and design equations in the first part are also applicable for DCM and it will be noted to reference those steps for designing power supply in DCM operation.

I.   Continuous Conduction Mode

Step 1 – Determine System Requirements: VACMIN, VACMAX, fL, VO, PO, η

Determine input voltage using Table 2 as guidelines for the standard worldwide Input Voltage and Line Frequency. For quick design reference, engineers can also use Table 17.

Input (VAC)	V_{ACMIN} (VAC)	V_{ACMAX} (VAC)
100/115	85	132
230	195	265
Universal	85	265

Table 18.   Input Voltage Range.

Efficiency η is the ratio of output power to input power. Since efficiency can vary significantly with output voltage due to secondary diode loss, it is best to use a number that is representative of similar power supplies. Switching power supply efficiencies typically range from 75% for supplies delivering most of their power at low voltage outputs (5 V or 3.3 V) to 85% for those supplying most of their power through higher voltage outputs (12 V and above). If this data is not available, 80% is a reasonable choice.

Step 2 – Decide on Feedback/Sense Circuit

Two types of feedback/sense circuits are presented in this documents. Optocoupler with a Zener diode sense circuit similar to the design implemented on Figure 1 and application example is suitable for medium power levels (up to 30 W) and is reasonably accurate, particularly at output voltages higher than 5 V. The optocoupler feedback using an accurate reference/comparator IC such as the TL431 provides a higher accuracy and regulation at a slightly added cost and is applicable to all power and output voltage ranges.

Tables 13 and 14 give the typical component values for each approach.

Step 3 – Determine the Input Capacitor CIN and Minimum DC Input Voltage V_MIN

When the full-wave rectified AC line is filtered with an input capacitance CIN (C1 + C2 in Figure 1). The resulting high-voltage DC bus has a ripple voltage as shown in Figure 66. The minimum DC voltage VMIN occurring at the lowest line voltage VACMIN is an important parameter for the design of the power supply. A rule of thumb on choosing the CIN value is to use 2 to 3 μF/watt of output power for 100/115 VAC or universal input, and 1 μF/Watt of output power for 230 VAC. The total CIN value obtained by using this rule represents a nearly optimum design in terms of system cost in most applications.

The accurate calculation of V_{MIN} for a given C_{IN} (or vice versa) is a very complicated task which involves the solving of an equation with no closed form solution. The equation shown below represents a good first order approximation which is accurate enough for most situations.

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}^2) - \frac{2 \times P_O \times \left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN}}}$$

The bridge rectifier conduction time t_c is typically at 3 msec, and can be verified by direct measurement. The ON-time extension feature of TinySwitch-III IC minimizes the value of C_{IN}. It maximizes energy delivery and holdup time during power-down and brownout.
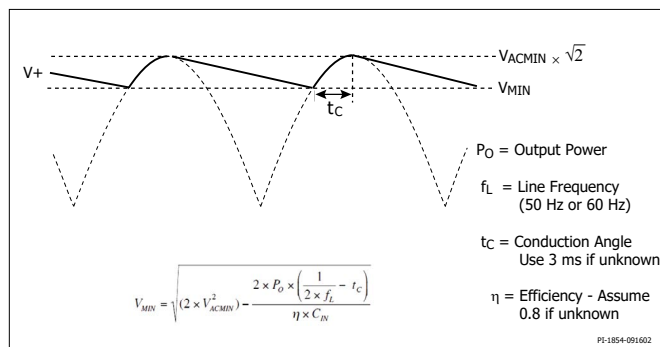

Figure 66. Input Voltage Waveform.

Step 3 – Select Output Diode and Estimate Associated Efficiency Loss

The output diode can be selected based on expected power supply efficiency and cost.
- Use a Schottky diode for highest efficiency requirements especially for low output voltages such 3.3 V and 5 V.
- Output voltages higher than 5 V can use an Ultrafast diode.
- If efficiency is not a concern or cost is paramount, use a Fast PN-diode.
- The Schottky and Ultrafast may be used with continuous mode of operation. And Fast PN-diode should only be used for discontinuous mode of operation.
- Choose output diode type.
- Output diode efficiency loss is the power supply efficiency reduction cause by the diode. Table 18 shows the estimated efficiency loss percentage with different types of output rectifier diode.
- The final diode current rating is to be determined after accommo-dating the continuous short-circuit current I_{OS}.
- Table 10 shows some commonly used diodes. V_R is the reverse voltage rating and I_O is the diode DC current rating.

Diode Type	V_D (V)	Efficiency Loss
Schottky	0.5	$(0.5/V_O)$ x 100%
Ultrafast	1.0	$(1.0/V_O)$ x 100%
Fast	1.0	$(1.0/V_O)$ x 100%

Table 19.   Diode Forward Voltage and Efficiency Loss.

Step 4 – Determine Output Diode Peak Inverse Voltage (PIV). Calculate Reflected Output Voltage V_{OR} Based on V_{MAX}, V_O, V_D and PIV

When the power MOSFET integrated to the TinySwitch-III IC is off and the secondary is conducting, the voltage on the secondary is reflected to the primary side of the transformer by the turns ratio. This reflected voltage VOR adds to the input DC voltage at the TinySwitch-III drain node. Worst-case voltage at the drain occurs at high line when the DC input voltage is at its maximum value. The maximum DC input voltage can be calculated as:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX}$$

Look up output diode rectifier reverse voltage VR from the diode data sheet.

Calculate maximum peak inverse voltage PIV. The usual maximum recommended PIV is 80% of the reverse voltage rating VR.

PIV = 0.8 x VR

Calculate the reflected output voltage VOR:

$$V_{OR} = \frac{V_{MAX} \times (V_O + V_D)}{PIV - V_O}$$

- V_{OR} must be less than 135 V.
- A good starting value for < 20 W output power is to set V_{OR} equals to 100 V.
- Higher than 20 W, set V_{OR} between 100 V – 110 V.

Step 5 – Choose TinySwitch-III Based on Input Voltage Range and Output Power

Select appropriate TinySwitch according to Table 19 for TinySwitch-III for family of devices.

Output Power Table

Products[3]	230 VAC ± 15 %		85 – 265 VAC	
	Adapter[1]	Peak or Open Frame[2]	Adapter[1]	Peak or Open Frame[2]
TNY274P/G	6 W	11 W	5 W	8.5 W
TNY275P/G	8.5 W	15 W	6 W	11.5 W
TNY276P/G	10 W	19 W	7 W	15 W
TNY277P/G	13 W	23.5 W	8 W	18 W
TNY278P/G	16 W	28 W	10 W	21.5 W
TNY279P/G	18 W	32 W	12 W	25 W
TNY280P/G	20 W	36.5 W	14 W	28.5 W

Table 20. TinySwitch-III Family of Devices.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 ºC ambient. Use of an external heat sink will increase power capability;
2. Minimum peak power capability in any design or minimum continuous power in an open frame design (see Key Application Considerations from the data sheet);
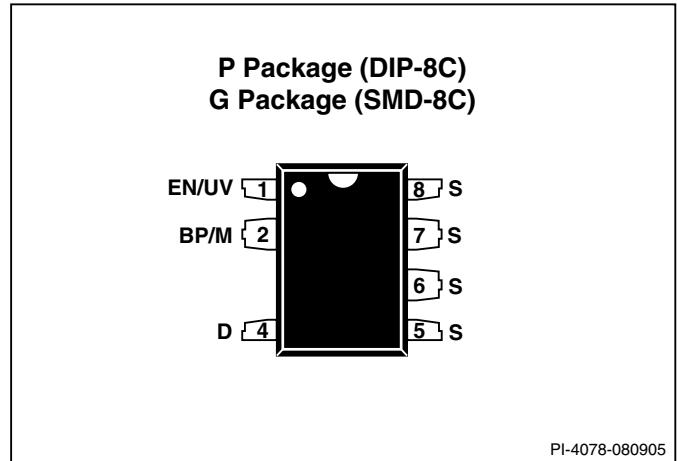3. Packages: P: DIP-8C: SMD-8C (Figure 50). See Part Ordering Information.

Figure 67. TinySwitch-III IC Package.

Step 6 – Determine Maximum Duty Cycle D_{MAX} at Low-Line Using V_{OR} and V_{MIN}

For Continuous Mode Operation:

$$D_{MAX} = \frac{V_{OR}}{V_{OR} + (V_{MIN} - V_{DS})}$$

V_{DS} is the average Drain to Source voltage during TinySwitch-III ON-time. Set V_{DS} to approximately 10 V which results in a slight increase in D_{MAX}.

Higher V_{MIN} directly increases the output power capability of a given TinySwitch, while lower V_{MAX} allows larger V_{OR} and consequently larger D_{MAX} which also increases the output power of a given TinySwitch.

Step 7 – Calculate K_{RP} From V_{MIN}, P_O, η, I_P and D_{MAX}

KRP is the ratio between the primary ripple current IR and primary peak current I_P. And I_P is 90% of minimum I_{LIMIT}.

$$I_P = \frac{I_{AVG}}{\left(1 - \dfrac{K_{RP}}{2}\right) \times D_{MAX}}$$

The average DC current I_{AVG} at low line is simply the input power divided by V_{MIN}, where the input power is equal to the output power divided by the efficiency.

$$I_{AVG} = \frac{P_{OUT}}{\eta V_{MIN}}$$

By combining the above equations for I_P and I_{AVE}, K_{RP} can be expressed as:

$$K_{RP} = \frac{2 \times (I_P \times D_{MAX} \times \eta \times V_{MIN} - P_O)}{I_P \times D_{MAX} \times \eta \times V_{MIN}}$$

Primary ripple current can be easily derived as,

$$I_R = I_P \times K_{RP}$$

When the MOSFET switch turns on before the secondary current has reduced to zero, the power supply is operating CCM. Figure 68a and 68b depicts the primary drain and secondary diode current waveform shapes both continuous and discontinuous mode respectively.
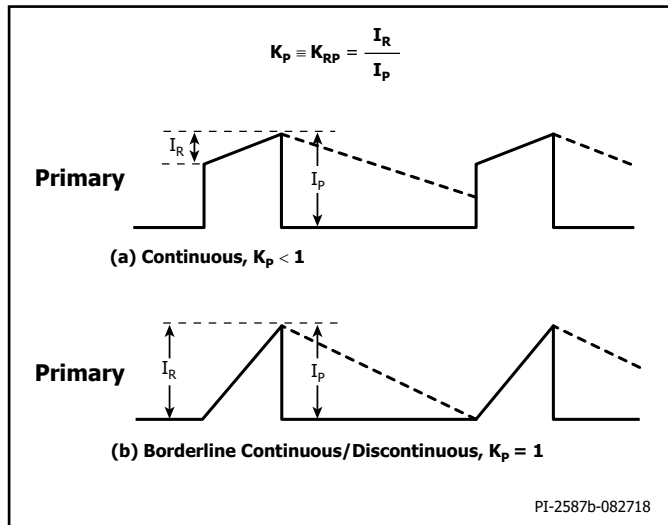

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

Primary

(a) Continuous, $K_P < 1$

Primary

(b) Borderline Continuous/Discontinuous, $K_P = 1$

PI-2587b-082718

Figure 68. Primary Drain Current and Secondary Diode Current Waveforms.

Step 8 – Check K_{RP} Against 0.6

If $K_{RP} > 0.6$, go to Step 9.
If $K_{RP} < 0.6$, set $K_{RP} = 0.6$, then follow the process below.
- Recalculate D_{MAX} using Step 7 equation.
- Recalculate V_{OR} using Step 6 equation.
- If $V_{OR} < 135$ V, go to Step 9.
- If $V_{OR} > 135$ V, go back to Step 5 and select higher current TinySwitch.

Step 9 – Calculate Primary Inductance, L_P

Continuous Mode:

$$L_P = \frac{10^6 \times P_O}{K_{RP} \times \left(1 - \frac{K_{RP}}{2}\right) \times \frac{1}{0.9} \times I_P^2 \times f_S} \times \frac{Z \times (1-\eta) + \eta}{\eta}$$

The η is the efficiency and Z is the loss factor. If $Z = 1$, all losses are on the secondary-side. If $Z = 0$, all losses are on the primary-side. Z is simply the ratio of secondary loss to total loss. If no better reference information is available, Z should be set to 0.5.

- I_P is the minimum I_{LIMIT} from TinySwitch data sheet as previously defined in Step 7.
- f_S is the minimum switching frequency from TinySwitch data sheet.
- Not the cancellation effect between the over-temperature variations of I_P and fs resulting in the additional 1/0.9 term.
- Z is the loss allocation factor.

Primary Inductance (LP) Tolerance
For transformer design manufacturability, the design engineer needs to provide the desired tolerance of the primary inductance. If no reference for the tolerance, good design approach and typically used tolerance is ± 10% of the calculated primary inductance (LP).

In order to ensure the minimum primary inductance requirement, the +10% should be added on the total required primary inductance.

Step 10 – Transformer Design

- Calculate turns ratio N_P/N_S:

$$\frac{N_P}{N_S} = \frac{V_{OR}}{V_O + V_D}$$

- Select core and bobbin. For a typical design, Table 5 gives recommendation for commonly available cores and power levels. This is however a conservative guideline; design iteration is recommended in order to have an optimized solution to meet the design specifications.

AN-18 Appendix A also provides a table of recommended core types for various power ranges. For single output designs, a triple insulated secondary simplifies transformer construction and allows the use of the smallest size core and bobbin for a given output power. Margin winding, which is suitable for both single and multiple output secondaries, will require wider bobbins and therefore, longer/taller cores. If there is no specific form factor requirement, it is best to start with the smallest EE type core for the power level. EE cores are usually the least expensive type. The two-digit number following the core type indicates the core size in mm. For 100 kHz operation, the selection of core material is not very critical. TDK PC40 material is a good first choice. Other ferrite materials with similar characteristics are available from many manufacturers such as Philips 3C85 and its equivalent will also work at 100 kHz, and could be used if there is a cost advantage.

Once a core has been selected from the catalog, a suitable bobbin can be easily identified.

Manufacturer specified core parameters A_E, L_E, A_L and bobbin parameter BW are usually found in the same catalog.

- Calculate primary and secondary number of turns for peak flux density (B_P) not to exceed 3000 Gauss. Limit B_P to 2500 Gauss for low audio noise designs. Use the lowest practical value of B_P for the greatest reduction in audio noise. See AN-24 for additional information regarding audio noise suppression technique.
- There are different means to determine number of turns for each winding. One is to calculate first the primary number of turns (N_P) by choosing maximum flux density B_P to be less than 3000 Gauss. Knowing L_P and I'_P from previous steps we can calculate N_P as:

$$N_P = 100 \times I'_P \times \frac{L_P}{B_P \times A_E}$$

Where I'_P equals to maximum I_{LIMIT}.

Another way is to select the secondary number of turns, N_S which the spreadsheet applied. A good starting point is to pick the number for the secondary turns. Using 1 turn/volt for 100/115 VAC and 0.6 turn/volt for 230 VAC or universal inputs is a good assumption. As an example, for a 115 VAC and an output V_O of 12 V plus the rectifier forward drop V_D of 0.7, a 13 turn secondary would be used as the initial value. The primary number of turns N_P is related to the secondary number of turns N_S by the ratio between V_{OR} and $V_O + V_D$.

- Calculate secondary number of turns, N_P:

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

- Similarly, the number of bias windings N_B can be derived from.

$$N_B = N_S \times \frac{V_B + V_{DB}}{V_O + V_D}$$

V_B is the bias voltage, and V_{DB} is the bias rectifier forward voltage drop.

- Then after determining the primary number of turns N_P, another critical parameter that must be checked is the maximum flux density in the core (B_M).

$$B_M = \frac{100 \times I_P \times L_P}{N_P \times A_E}$$

Where, A_e is the effective cross sectional area of the core. The primary inductance L_P, calculated from Step 9. And I_P or the primary current which is already given.

If B_M is greater than 3000 Gauss, either the core cross sectional area (core size) or N_P must be increase to bring it within the 2000 to 3000 Gauss range. On the other hand, if B_M is less than 2000 Gauss, a smaller core or fewer turns on the primary can be used.

- Calculate gap length L_g. Gap length should be larger than 0.1 mm to ensure manufacturability.

$$L_g = 40 \times \pi \times A_e \times \left(\frac{N_P^2}{1000 \times L_P} - \frac{1}{A_L} \right)$$

The core cross sectional A_e and ungapped effective inductance A_L can be found from the data sheets of the core. L_g is usually incorporated as an air gap ground into the center leg of the core and needs to be at least 51 μm or 2 mils for manufacturability. If L_g is less than 51 μm, once again the core size or N_P must be increase.

One other parameter always required by transformer manufacturer is the gapped core effective inductance A_{LG}, which can be determined only after N_P is fixed:

$$A_{LG} = 1000 \times \frac{L_P}{N_P^2}$$

Step 11 – Calculate Primary RMS Current I_{RMS}, Secondary Peak Current I_P, RMS Current I_{SRMS} and Output Ripple Current I_{RIPPLE}

Continuous Mode:

- Calculate primary RMS current I_{RMS}:

$$I_{RMS} = I_P \times \sqrt{D_{MAX} \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1 \right)}$$

- Calculate secondary peak current I_{SP} and can be derived from the primary peak current I_P and the turns ratio between primary and secondary N_P/N_S.

$$I_{SP} = I_P \times \frac{N_P}{N_S}$$

- Calculate secondary RMS current I_{SRMS}. The K_{RP} of the secondary is always identical to that of the primary, since it is only a reflected version of the primary current with the duty cycle (1-D). Therefore, the secondary RMS current I_{SRMS} can be expressed in a manner similar to the primary RMS current, only with D_{MAX} replaced by $(1 - DM_{AX)}$.

$$I_{SRMS} = I_{SP} \times \sqrt{(1 - D_{MAX}) \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1 \right)}$$

I_{RIPPLE} is the RMS ripple current of the output capacitor and it is calculated as:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

I_O is the power supply output current which can be calculated as:

$$I_O = \frac{P_O}{V_O}$$

Step 12 – Determine Wire Gauge Both on Primary and Secondary

From the core and bobbin size, it is possible to determine the outside diameter of the primary wire OD in mm that is required to accommodate the primary turns on one or two full layers allowing for margins as appropriate.

$$OD = \frac{BW_E}{N_P}$$

BW_E is the effective bobbin width, which takes into account physical bobbin width BW, margins M (all in mm), and the number of winding layers L:

$$BW_E = L \times [BW - (2 \times M)]$$

The closest standard magnet wire gauge that is less than or equal to this diameter can be selected. Determine the bare conductor diameter DIA of this wire gauge using information from a wire table. The next step is to find out if this conductor size is sufficient for the maximum I_{RMS}. The current capacity for magnet wire is specified of "Circular mile per Amp" or CMA, which is the inverse of current density:

$$CMA = \frac{1.27 \times DIA^2 \times \frac{\pi}{4}}{I_{RMS}} \times \left(\frac{1000}{25.4} \right)^2$$

If the CMA is less than 200, a larger gauge wire is needed to handle the current. This could be accommodated by adding a second layer if there is only one existing layer and/or by using a larger core/bobbin and/or smaller N_P. On the other hand, a CMA greater than 500 would indicate that a smaller core/bobbin and/or larger N_P could be used.

Note that in the AN-17 spreadsheet, DIA is actually derived from OD using an empirical equation. A practical wire size, AWG, is determined according to DIA (see AN-18 Appendix A, Table 2 for wire size information). CMA is then calculated from AWG.

With the secondary RMS current I_{SRMS} available, the minimum secondary wire diameter DIA_S (in mm), can be calculated as follows:

$$DIA_s = \sqrt{\frac{4 \times CMA \times I_{SRMS}}{1.27 \times \pi} \times \frac{25.4}{1000}}$$

If the required secondary wire diameter turns out to be larger than that of the AWG #26 wire size which corresponds to twice the skin depth at 100 kHz, a parallel configuration of windings using a gauge equal to or smaller than #26 AWG should be used to provide the same effective cross sectional area. The parallel windings must have identical number of turns equal to N_S. For example, if the equation above indicates a #23 AWG wire, a winding consisting of NS turns of two parallel strands of #26 AWG will be a good choice.

Note that if triple insulated wire is to be used for secondary, the insulated wire diameter is actually larger than DIA_S by twice the thickness of the insulator. Therefore, the maximum outside diameter OD_S (in mm) must be calculated:

$$OD_S = \frac{BW - (2 \times M)}{N_S}$$

A triple insulated wire should be specified with a conductor diameter equal to or greater than DIA_S and insulated outside diameter equal to or less than OD_S.

As can be seen from steps 10 to 12, the transformer design is a highly iterative process in itself. When N_P is changed, N_S and N_B will change according to ratios already established. Similarly, any change in core size requires a recalculation of CMA, B_M and L_g to make sure that they are within the specified limits. Table 20 shows the relation and effect upon varying the number of layers (L), secondary number of turns (N_S) and Core/Bobbin.

		Maximum Flux Density (B_M)	Gap Length (L_g)	Current Capacity (CMA)
Number of Layers (L)	↑	–	–	↑
Secondary Number of turns (NS)	↑	↓	↑	↓
Core	↑	↓	↑	↑

Table 21.   Iteration Relation of L, N_S and Core.

Step 13 – Determine Output Short-Circuit Current I_{os}

• Calculate maximum output short-circuit current I_{OS} from I'_P and N_P/N_S, where I'_P is the maximum I_{LIMIT} from TinySwitch data sheet and N_P/N_S is the turns ratio from Step 10.

$$I_{OS} = I'_P \times \frac{N_P}{N_S} \times k$$

Where k is the peak RMS current conversion factor.

• The value of k is determined based on empirical measurements: k = 0.9 for Schottky diode and k = 0.8 for PN junction diode.
• Check I_{OS} against diode current rating I_D. If necessary, choose higher current diode.

Step 14 – Select Output Capacitor

ESR is the most important parameter for output filter capacitor selection. Capacitor ESR directly determines the output ripple voltage of the power supply and the ripple current rating of the capacitor. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

$$ESR = \frac{V_{RIPPLE}}{I_{SP}}$$

Ripple current is typically specified at 105 ºC ambient which is much higher than the ambient temperature required in most applications. Therefore, it is possible to operate the capacitor at higher ripple currents determined by a multiplier factor from the capacitor data sheet.

Actual ripple current of the capacitor can be calculated as follows:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

Where I_{SRMS} is the secondary winding RMS current and I_O is the DC output current.

• Choose output capacitor with RMS current rating equal to or larger than output ripple current.
• Use low ESR electrolytic capacitor rated for switching power supply use.
• Example are KZH series from UCC, UHD or UHW series from Nichicon, and EEU series from Panasonic.

For actual output capacitance value is of secondary importance. As long as the capacitance contribution is negligible to the ripple. And this will hold as true by following the selected actual capacitance value as reflected by the equation below for C_{OUT}:

$$C_{OUT} >> \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times f_{SW}}$$

Where,
C_{OUT} is the actual capacitance value.
I_{OUT} is the DC output current.
D_{MAX} is the maximum duty cycle.
V_{RIPPLE} is the required ripple voltage of the output.
f_{SW} is the switching frequency of operation of the power supply.

Step 15 – Select Output Post Filter

If the measured switching ripple voltage at the output capacitor is higher than the required specification, an LC post filter consisting of a 2.2 to 4.7 µH inductor or ferrite bead (only for output current <1 A) with a low ESR electrolytic capacitor is recommended. This will provide a lower cost solution compared to increasing the capacitance value and/or lowering the ESR of the main output filter capacitor.

Step 16 – Select Bias Rectifier

Bias rectifier selection is similar to output rectifier selection with the exception that since the bias winding carries very little current (typically less than 10 mA). The considerations for current capacity and very fast recovery no longer apply.

The peak inverse voltage across the bias rectifier diode is given by:

$$PIV_B = V_B + \left(V_{MAX} \times \frac{N_B}{N_P} \right)$$

Step 17 – Select Bridge Rectifier Based on Input Voltage V_{ACMAX} and Input RMS Current I_{ACRMS}

Maximum operating current for the input bridge rectifier occurs at low-line:

$$I_{ACRMS} = \frac{P_O}{\eta \times V_{ACMIN} \times PF}$$

PF is the power factor of the power supply. Typically, for a power supply with a capacitor input filter, PF is between 0.5 and 0.7. Use 0.5 if there is no better reference data available.

Select the bridge rectifier such that:

- $I_D > 2 \times I_{ACRMS}$, where I_D is the rated RMS current of the bridge rectifier.
- $V_R > 1.25 \times 1.414 \times V_{ACMAX}$; where V_R is the rated reverse voltage of the rectifier diode.

Step 18 – Design Complete for Continuous Current Mode (CCM) Operation of Flyback Power Supply

II.   Discontinuous Mode Operation

This section is mainly focus on the steps procedure with design equations for the design implementing discontinuous mode operation.

Step 1 – Follow the Step 1 to 5 Procedures From Part I of In-depth Information

Step 2 – Determine Primary Peak Current I_P. Calculate Maximum Duty Cycle D_{MAX} for Discontinuous Mode of Operation Based on V_{MIN}, P_O and I_P

- Primary peak current is 90% of minimum I_{LIMIT} from the data sheet of the selected TinySwitch. $I_P = 0.9$ x I_{LIMIT} minimum.
- Calculate maximum duty cycle D_{MAX} for discontinuous mode of operation as:

$$D_{MAX} = \frac{2 \times P_O}{\eta \times V_{MIN} \times I_P}$$

Step 3 – Calculate K_{DP} from V_{MIN}, V_{OR} and D_{MAX}

In Discontinuous Current Mode or DCM operation, the secondary current is zero when the MOSFET turns on. Figure 69 illustrate the primary drain and secondary rectifier currents in DCM operation.
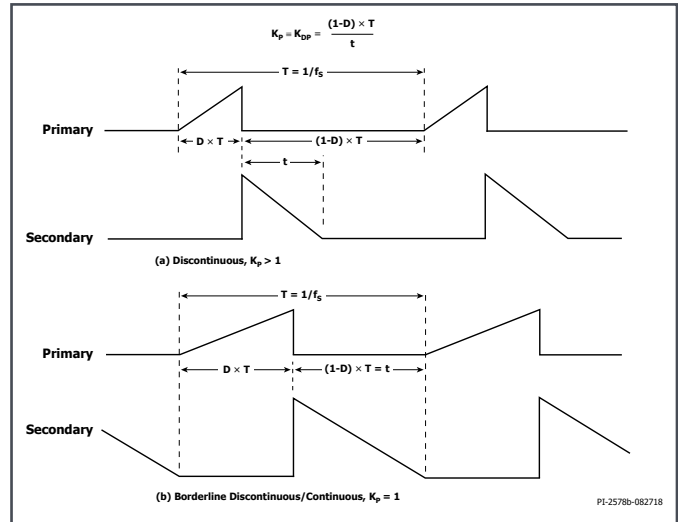

Figure 69.   Primary Drain and Secondary Rectifier Current in DCM Operation.

- K_{DP} is the ratio between the off-time of the switch and the reset time of the core:

$$K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{V_{MIN} \times D_{MAX}}$$

Step 4 – Check KDP to Ensure Discontinuous Mode of Operation

With discontinuous mode of operation, generally, the output filter is smaller, output rectifier is inexpensive using a PN junction diode, EMI and noise are lower.

Fully discontinuous mode of operation (discontinuous under all conditions) may be necessary in some applications to meet specific requirements such in very low output ripple voltage. Use of RC snubber, and/or PN junction diode as output rectifier also demand full discontinuous mode of operation. This can be accomplished by raising V_{OR} higher if necessary. To keep the worst-case drain voltage below recommended level of 725 V for TinySwitch-III device, V_{OR} should be kept below 135 V.

Mostly discontinuous mode of operation ($K_{DP} > 1$) refers to a design in discontinuous mode under most situations, but do have the possibility of operating in continuous mode occasionally.

Continuous mode operation ($K_{DP} < 1$) provides higher output power. In this mode a Schottky output diode should be used to prevent longer diode reverse recovery time that could exceed leading edge blanking period (t_{LEB}).

Step 5 – Check for Fully Discontinuous Operation

$K_{DP} > (1 - D_{MAX}) / (0.67 - D_{MAX})$: Fully discontinuous.

0.67 is the reciprocal of the percentage of duty cycle relaxation caused by various parameters such as the tolerance in TinySwitch current limit and frequency.

Recalculate VOR as:

$$V_{OR} = \frac{K_{DP} \times V_{MIN} \times D_{MAX}}{1 - D_{MAX}}$$

- If V_{OR} < 135 V, go to Step 6.
- If V_{OR} > 135 V, go back to first section of the In-depth Information Step 5 and select higher current TinySwitch.

Step 6 – Calculate Primary Inductance LP for Discontinuous Mode

$$L_P = \frac{10^6 \times P_O}{K_{RP} \times \left(1 - \frac{K_{RP}}{2}\right) \times \frac{1}{0.9} \times I_P^2 \times f_S} \times \frac{Z \times (1 - \eta) + \eta}{\eta}$$

Where:
I_P is the minimum I_{LIMIT} from TinySwitch data sheet.
f_s is minimum switching frequency from TinySwitch data sheet. Please note the cancellation effect between the over temperature variations of I_P and f_S resulting in the additional 1/0.9 term.
Z is loss allocation factor. If Z = 0, all losses are on the primary-side. If Z = 1, all losses are on the secondary-side. If no reference, Z = 0.5 is a reasonable staring point.

Step 7 – Transformer Design

Transformer design steps done on continuous mode operation is also applicable for DCM. For Step 7, transformer design for discontinuous mode operation, Step 10 of Part I design equations and procedures will be applied.

Step 8 – Calculate Primary RMS Current I_{RMS} and Secondary RMS Current I_{SRMS}

Discontinuous Mode:

- Calculate primary RMS current I_{RMS}

$$I_{RMS} = \sqrt{D_{MAX} \times \frac{I'^2_P}{3}}$$

Where I'_P equals to maximum I_{LIMIT}.

- Calculate secondary RMS current I_{SRMS}.

$$I_{SRMS} = I_{SP} \times \sqrt{\frac{1 - D_{MAX}}{3 \times K_{DP}}}$$

Where $I_{SP} = I'_P \times [N_P/N_S]$ and $I'_P = I_{LIMITMAX}$.

- Choose wire gauge for primary and secondary windings based on I_{RMS} and I_{SRMS}.
- In some designs, a lower gauge (larger diameter) wire may be necessary to maintain transformer temperature within acceptable limits during continuous short-circuit conditions.
- Do not use wire thinner than 36 AWG to prevent excessive winding capacitance and to improve manufacturability.

Step 9 – Determine Wire Gauge Both on Primary and Secondary

Wire gauge calculation both on primary and secondary steps in Part I is also applicable for discontinuous mode. For Step 9 of discontinuous mode, design equations and procedures on Step 12 of Part I will be applied.

Step 10 – Determine Output Short-Circuit Current I_{OS} and Selection of Output Capacitor (C_{OUT}), Output Post Filter, Bias Rectifier and Bridge Rectifier

The calculation and selection of other design parameters such as output short-circuit (I_{OS}), output capacitor (C_{OUT}), output post filter, bias rectifier and bridge rectifier had the same calculations as in Part I. For Step 10 of discontinuous mode operation, the Steps 13 to 17 of Part I design equations and procedures will be applied.

Step 11 – Design Complete for Discontinuous Current Mode (DCM) Operation of Flyback Power Supply

Revision	Notes	Date
A	Initial release.	09/20

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