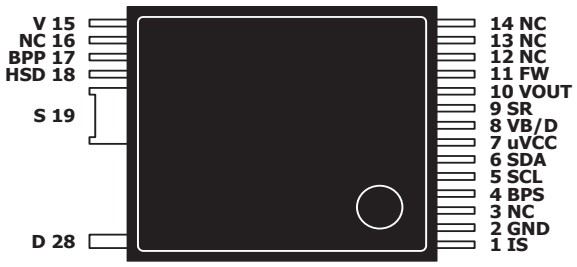
Application Note AN-134
Failure Mode and Effect Analysis
InnoSwitch5-Pro

Failure Mode Analysis Summary

Device Level Failure Mode Analysis

Tables 1 and 2 show the device level failure mode analysis including the system effects of an open-circuit for each pin and as well as adjacent pin-to-pin shorts. In each case a safe failure is expected.



Fault Type: Pin Open	Observed Behavior	
	Fault applied Before Power-up	**Fault applied After Power-up**
IS	Power supply may continuously AR with 1.6s off time. With the IS pin disconnected, all features related to current sensing such as CC, CDC, CVO, ISSC, CCSC, and VBUSSC fault may get activated based on the floating pin voltage.	Power supply may continuously AR with 1.6s off time. With the IS pin disconnected, all features related to current sensing such as CC, CDC, CVO, ISSC, CCSC, and VBUSSC fault respond accordingly based on the floating pin voltage.
GND	Output capacitor will regulate at 5.7 V and SR gate drive will not be generated.	Output capacitor voltage rises 0.7 V above voltage setpoint. Risk of cross conduction – a TVS in the primary clamp circuit helps protect the primary switch from damage.
NC3	Power supply will start-up normally.	Power supply will operate normally.
BPS	Flyback VOUT will increase beyond 5 V during start-up. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.	Power supply will AR with 1.6s off time, then at recovery, Flyback VOUT will increase beyond 5 V. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed OVP circuit is not present.
SCL	I2C communication is not possible.	Power supply will operate normally, but further I2C communication is not possible. If Watchdog is enabled, InnoSwitch secondary registers will reset, and AR will trigger for output voltages higher than 9.6 V.
SDA	I2C communication is not possible.	Power supply will operate normally, but further I2C communication is not possible. If Watchdog is enabled, InnoSwitch secondary registers will reset, and AR will trigger for output voltages higher than 9.6 V.
uVCC	I2C interface will be non-functional.	I2C interface will stop working. Power supply may enter auto-restart.

Table 1. Failure Mode Analysis for Pin Open Fault.

Fault Type: Pin Open	Observed Behavior	
	Fault applied Before Power-up	**Fault applied After Power-up**
VB/D	Flyback VOUT will regulate at 5 V and bus switch will remain open.	The bus switch may either 1) completely turn off, or 2) remain partially on. If the bus switch remains partially on, a voltage lower than Flyback VOUT will be present on VBUS_OUT. Risk of damage to the bus switch when sufficient load current is drawn due to excessive power dissipation in the bus switch (VDS*IDS).
SR	Power supply will continuously AR with 1.6s off time.	If the SR pin opens while the gate voltage is high, the SR FET will remain ON which will pose a risk of cross conduction. Output voltage will collapse, and the power supply will enter auto-restart. If the SR pin opens while the gate voltage is low, power supply will continue operation with the secondary current flowing through SR FET body diode. Higher SR FET voltage stress may occur and may result in higher SR FET temperature. A TVS in the primary clamp circuit helps protect the primary switch from damage of cross conduction occurs.
VOUT	Flyback VOUT will increase beyond 5 V during start-up. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.	Flyback VOUT will increase beyond regulation when the fault is applied. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.
FWD	Flyback VOUT will increase beyond 5 V during start-up. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.	Power supply will AR with 1.6s off-time, and then at recovery, Flyback VOUT will increase beyond 5 V. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.
NC12	Power supply will start-up normally.	Power supply will operate normally.
NC13	Power supply will start-up normally.	Power supply will operate normally.
NC14	Power supply will start-up normally.	Power supply will operate normally.
V	Primary power switch will not switch due to Line UV condition.	Primary power switch will stop switching due to Line UV condition.
NC16	Power supply will start-up normally.	Power supply will operate normally.
BPP	Primary power switch will not switch. Continuous operation of the high-voltage internal regulator into the floating BPP will increase the power supply input power consumption.	Primary power switch will stop switching. Continuous operation of the high-voltage internal regulator into the floating BPP will increase the power supply input power consumption.
HSD	Power supply will start-up normally.	Power supply will operate normally.

Table 1 (cont). Failure Mode Analysis for Pin Open Fault.

Fault Type: Pin Open	Observed Behavior	
	Fault applied Before Power-up	**Fault applied After Power-up**
S	Primary power switch attempts to switch, but no current will flow in the flyback transformer. Voltage across the BPP capacitor exceeds 5.3 V. Power supply output will remain 0 V.	No energy will be transferred from flyback primary to secondary. Power supply output will collapse to 0 V and the succeeding behavior is same as fault applied before start-up.
D	Primary power switch will not switch.	Primary power switch will stop switching.

Table 1 (cont). Failure Mode Analysis for Pin Open Fault.

Fault Type: Pin-to-Pin Short	Observed Behavior	
	Fault applied Before Power-up	**Fault applied After Power-up**
IS & GND	No output current sensing. All features related to current sensing such as CC, CDC, CVO, ISSC, CCSC, and VBUSSC fault will respond accordingly with IS pin at 0 V, regardless of actual load current.	No output current sensing. All features related to current sensing such as CC, CDC, CVO, ISSC, CCSC, and VBUSSC fault will respond accordingly with IS pin at 0 V, regardless of actual load current.
GND & NC3	Power supply will start-up normally.	Power supply will operate normally.
NC3 & BPS	Power supply will start-up normally.	Power supply will operate normally.
BPS & SCL	A small overshoot in Flyback VOUT may occur due to slower charging of BPS capacitor during start-up. I2C communication is not possible.	Normal operation will continue, but further I2C communication is not possible. SCL will be pulled up to BPS voltage. If Watchdog is enabled, InnoSwitch secondary registers will reset, and AR will trigger for output voltages higher than 9.6 V.
SCL & SDA	I2C communication is not possible.	Normal operation will continue, but further I2C communication is not possible. If Watchdog is enabled, InnoSwitch secondary registers will reset, and AR will trigger for output voltages higher than 9.6 V.
SDA & uVCC	I2C communication is not possible.	Normal operation will continue, but further I2C communication is not possible. If Watchdog is enabled, InnoSwitch secondary registers will reset, and AR will trigger for output voltages higher than 9.6 V.
uVCC & VB/D	A low voltage may appear at VBUS_OUT, indicating the bus switch is partially on even when VBEN is still disabled. If load current exceeds VBUSSC fault threshold before VBEN = Enable command is sent, then AR will trigger.	Depending on the initial output voltage, uVCC may go above the absolute maximum rating due to the path formed by the bus switch gate-source diode and resistor into VBD. If uVCC rises above BPS, AR may happen due to reset of secondary registers. Otherwise, a low voltage may appear at VBUS_OUT, indicating the bus switch is only partially on. Risk of damage to the bus switch when sufficient load current is drawn due to excessive power dissipation in the bus switch (VDS*IDS).
VB/D & SR	SR signal is attempting to drive the bus switch partially on and off, which may create small pulses on VBUS_OUT even when VBEN is still disabled.	VBD will be pulled low to SR pin voltage level. Bus switch will be only partially on when fault is created during high VOUT operation. Risk of damage to the bus switch when sufficient load current is drawn due to excessive power dissipation in the bus switch (VDS*IDS).

Table 2. Failure Mode Analysis for Adjacent Pin-to-Pin Short Fault.

Fault Type: Pin-to-Pin Short	Observed Behavior	
	Fault applied Before Power-up	Fault applied After Power-up
SR & VOUT	Power supply will continuously AR (1.6s off time). During each recovery attempt, the Flyback VOUT only reaches a low voltage (about 2.0 to 2.5 V) before AR triggers.	Risk of cross conduction – a TVS in the primary clamp circuit helps protect the primary switch from damage. Power supply may enter AR with 2s off time. Risk of damage to the InnoSwitch Secondary controller and SR FET due to high voltage imposed on SR pin and SRFET gate-source. Failure of BPS can lead to failure of uVCC and potentially leading to failure of microcontroller, if connected to uVCC.
VOUT & FWD	Flyback VOUT will increase beyond 5 V during start-up. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.	Power supply will AR with 1.6s off-time, and then at recovery, Flyback VOUT will increase beyond 5 V. Latch-off will trigger due to activation of primary sensed OVP circuit. Part damage may occur if primary-sensed output OVP circuit is not present.
FWD & NC12	Power supply will start-up normally.	Power supply will operate normally.
NC12 & NC13	Power supply will start-up normally.	Power supply will operate normally.
NC13 & NC14	Power supply will start-up normally.	Power supply will operate normally.
V & NC16	Power supply will start-up normally.	Power supply will operate normally.
NC16 & BPP	Power supply will start-up normally.	Power supply will operate normally.
BPP & HSD	Primary power switch will not switch.	Primary power switch will stop switching.
HSD & S	Power supply will start-up normally.	Power supply will operate normally.
S & D	Fuse at AC input will open.	Fuse at AC input will open.

Table 2 (cont). Failure Mode Analysis for Adjacent Pin-to-Pin Short Fault.

Revision	Notes	Date
A	Initial Release.	11/25
B	HSD & S pin short description update	04/26

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