Application Note AN-130
TOPSwitchGaN Family

Design Guide

Introduction

The TOPSwitchGaN™ family of ICs are highly integrated off-line switcher devices for power supplies in the range of 10 W to 300 W output. When operating with PCB cooling, devices within the TOPSwitchGaN family can deliver 300 W for universal input voltage range (85 VAC - 265 VAC), 400 W for high-line input (230 VAC), and up to 440 W when operating from a Power Factor Correction (PFC) input delivering 400 VDC. Applications include appliances, smart grid, and industrial power supplies and for power tools.

TOPSwitchGaN devices combine a high-voltage PowiGaN™ switch with a controller that provides a variable frequency, variable peak-current control scheme which ensures very high conversion efficiency across the load range. TOPSwitchGaN based designs can seamlessly transition between DCM and CCM operating modes. Jitter is added to the switching frequency to reduce EMI. Start-up current is drawn internally from the DRAIN pin, eliminating the need for external start-up components. An integrated soft-start minimizes component stress when power is applied. Input protection includes line undervoltage (UV) detection which prevents output glitches during power up plus line overvoltage (OV) shutdown which increases protection from line surge and mis-wire. In addition, the auto-restart limits output power to < 3% during overload and output short-circuit events. Over-temperature protection interrupts switching during thermal overload. The high thermal shutdown threshold is ideal for applications where the ambient temperature is high, while the large hysteresis protects the PCB and surrounding components from the effects of excessive average temperatures during fault conditions.

The TOPSwitchGaN family is ideal for applications requiring high average power efficiency. Power Integrations' EcoSmart™ technology used in TOPSwitchGaN family ensures that efficiency remains high across line and load. This makes the family ideal for applications that must meet energy efficiency standards such as the United States Department of Energy DoE 6, California Energy Commission (CEC) requirements and the European Code of Conduct.

The design of flyback power supplies is a highly iterative process with multiple variables that must be reviewed and adjusted to optimize the design. The design methodology described in this document utilizes the Power Integrations design software (PI Expert™) and allows the designer to follow either a quick-design (for power supply experts) or step-by-step approach. The quick-design approach employs a quick-start guide which a simplified design procedure that describes key application design considerations and recommendations and provides a quick design checklist and application examples. This approach allows an experienced engineer to rapidly design the power train and select a transformer. The step-by-step design procedure guides the engineer through each design step, starting with the inputting of system requirements through to the completion of the power supply using the most appropriate TOPSwitchGaN device. The process employs lookup tables to aid selection and utilizes the powerful PIXIs design tool that is part of the PI Expert software suite.

A section in the Application Note on Design Considerations and Recommendations provides engineers with ideas and guidance for design optimization. The quick design checklist provides a list of recommend tests to perform before proceeding to full circuit evaluation. Finally, the Application Note section on Application Examples describes actual reference designs using a TOPSwitchGaN device analyzing operation and sharing performance data.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a flyback power supply designed using TOPSwitchGaN IC. The high-level of integration results in and fewer design choices being required for external components. This greatly simplifies the design process and leads to a common circuit configuration for all applications with changes only required in the power-train components between designs. Different output voltage and power levels may require different values for some circuit components, but the general circuit remains similar. Features such as line overvoltage and undervoltage protection and output overvoltage protection are implemented using passive components.

Quick Start

Engineers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach and can use the following information to quickly design the transformer and select components for a first prototype.
For this approach, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet line numbers are provided in square brackets [line reference]

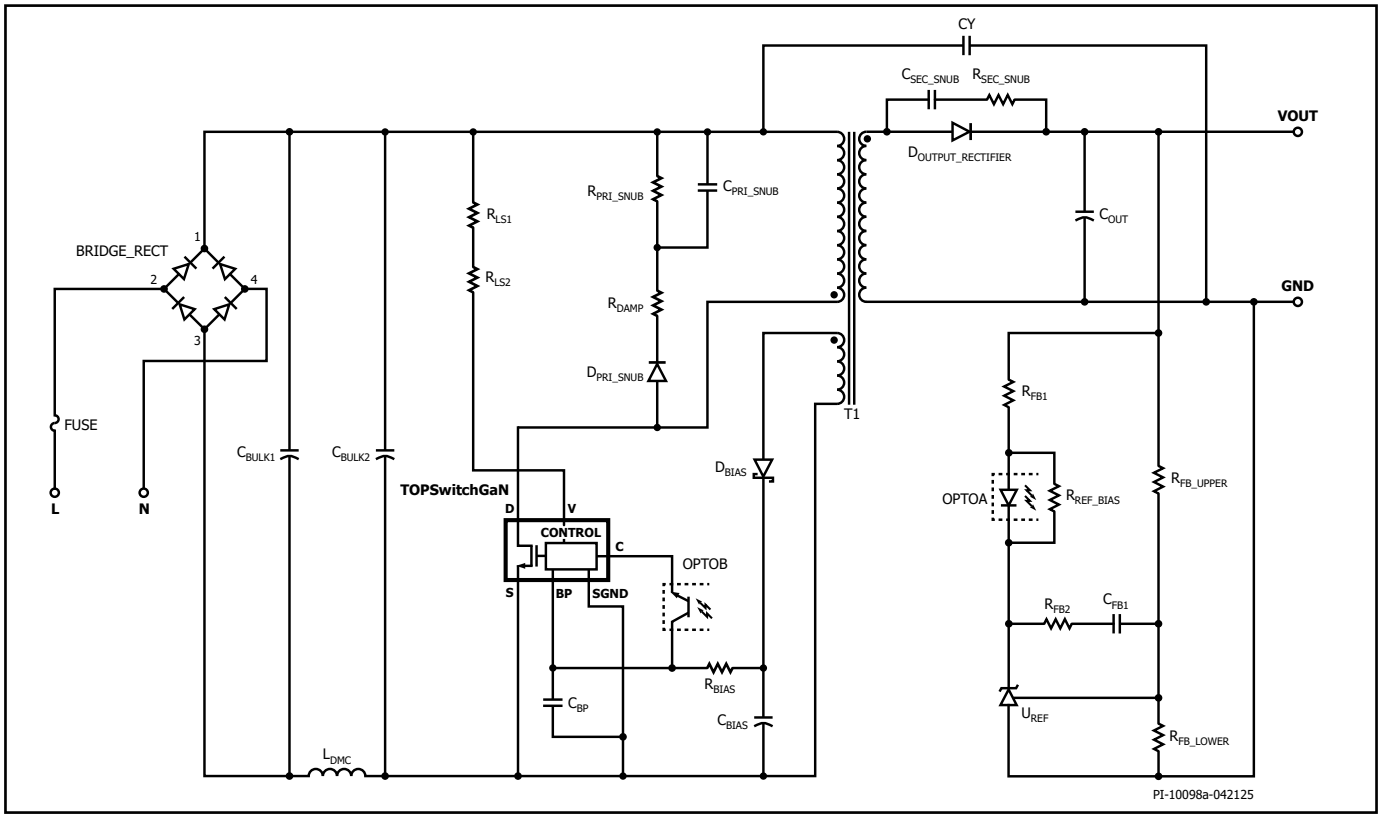


Figure 1. Typical Power Supply Schematic using a TOPSwitchGaN device with Line Undervoltage Lockout and Line Overvoltage Shutdown.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply or charger using the TOPSwitchGaN family of devices. It provides guidance which enables an engineer to quickly select key components and complete a suitable transformer design. To help simplify the task, this application note refers directly to the PIXls design spreadsheet that is part of the PI Expert design software suite available online as a free download from https://piexpertonline.power.com/site/login. The basic configuration used in a TOPSwitchGaN IC-based flyback power supply is shown in Figure 1, which also serves as the reference circuit for component identification that is used in descriptions throughout this application note.

In addition to this application note, there are the TOPSwitchGaN Design Examples Reports (DERs), Reference Design Kits (RDKs) which provide design examples of fully functional power supplies. A DER provides a detailed report covering design, construction, and performance. The RDK contains a similar report (described as the Reference Design Report - RDR) plus a fully tested power supply board. Details on how to download PI Expert, RDRs or DERs, and how to order an RDK along with the latest versions of all TOPSwitchGaN family documentation can be found at www.power.com.

- Enter INPUT_TYPE [B3]. Select if input is AC or DC
- Enter AC/DC input voltage range and line frequency, VIN_MIN [B4],
- VIN_MAX [B5], LINEFREQ [B7]
- Enter input capacitance, CAP_INPUT [B8]
  - 2-3 µF / W for universal (85-265 VAC) or single (100/115 VAC) line. Higher input capacitance is recommended for higher efficiency provided that increased cost and capacitor dimensions are acceptable. A more aggressive value of 2 µF / W can be used for designs that do not need to meet a hold-up-time requirement.
  - Use 1 µF/W for 230 VAC (185-265 VAC) line.
  - If this cell is blank, the input capacitance will be 2 times the output power for low-line and universal input and 1 times the output power for high-line input in microfarads.

- Enter nominal output voltage, VOUT [B9]
- Enter continuous output current, IOUT [B10]
- Enter efficiency estimate, EFFICIENCY [B12]
  - 0.87 for universal input voltage (85-265 VAC) or low-line input 100/115 VAC (85-132 VAC) and 0.89 for a high-line input 400 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype-board at maximum load and VIN_MIN.
- Select the TOPSwitchGaN device from the drop-down list or enter directly [B21]
  - Select the device from Table 1 according to output power and input voltage.
- Enter desired maximum switching frequency (30 kHz to 130 kHz) at full load, FSWITCHING_MAX [B35]
- Enter core type (if desired), from drop down menu CORE [B64]
  - Suggested core size will be selected automatically if none is entered [B64]
  - For custom core, enter CORE CODE [B65], and core parameters from [B67] to [B73]
- Enter secondary number of turns [B88]

If any warnings are generated, make changes to the design by following instructions in spreadsheet column D.

- Build transformer as suggested in "Transformer Construction" tab
- Select other components.
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were initially used (e.g. efficiency, V_{MIN}). Note that the efficiency estimate provided by the tool for the first prototype is very conservative.

Output Power Table[1]

Product[3]	PCB Copper Area[1]		
	400 VDC	230 VAC ±15%	85-265 VAC
	Peak or Open Frame[2,3]	**Peak or Open Frame[2,3]**	**Peak or Open Frame[2,3]**
TOP7074K	90 W	85 W	70 W
TOP7075K	105 W	95 W	85 W
TOP7078K	180 W	170 W	135 W
Product[3]	**Metal Heat Sink[1]**		
	400 VDC	230 VAC ±15%	85-265 VAC
	Peak or Open Frame[2,3]	**Peak or Open Frame[2,3]**	**Peak or Open Frame[2,3]**
TOP7074E	200 W	185 W	130 W
TOP7075E	240 W	210 W	165 W
TOP7078E	440 W	400 W	300 W

Table 1. Output Power Tables of TOPSwitchGaN device

Notes:

1. The Table 1 represents maximum practical continuous output power based on the following assumptions:
   a. 12 V output.
   b. Schottky or high-efficiency output diode.
   c. 130 V reflected voltage (VOR) and 85% efficiency.
   d. A 100 VDC minimum DC bus voltage for 85-265 VAC and 300 VDC bus voltage for 230 VAC.
   e. Sufficient heat-sinking to keep device temperature ≤110 °C.
   f. Power levels shown for the V package device assume 19.4 cm^2 of 610 g/m^2 copper heat sink area.
   g. Maximum continuous power for an open frame design operating in a +50 °C ambient.
2. Minimum peak power capability.
3. Packages: E: eSIP-7C, K: eSOP-12B.

Step-by-Step Design Procedure

This design procedure uses the PI Expert design software (available as a free download from Power Integrations), which automatically performs the key calculations required for designing a flyback power supply using TOPSwitchGaN ICs. PI Expert allows designers to avoid the typical highly iterative power supply design process. Look-up tables and empirical design guidelines are provided where appropriate to simplify the design task.

Adjust the design to eliminate warnings. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right-hand column of the spreadsheet. Once all warnings have been cleared, the output transformer design parameters and manufacturing information provided by PI Expert can be used to create a prototype transformer.

Step 1 – Application Variables

Enter: INPUT_TYPE, VIN_MIN, VIN_MAX, LINEFREQ, CAP_INPUT, VOUT, IOUT, EFFICIENCY, FACTOR_Z, and ENCLOSURE

INPUT TYPE
Select AC for application using AC input voltage and DC for application with PFC input.

Minimum and Maximum Input Voltage, V_{MIN}, V_{MAX} (VAC or VDC)
Determine the input voltage range from Table 3 for a particular regional requirement.

Line Frequency, LINEFREQ (Hz)
60 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate design margin. For absolute worst-case operating conditions or to match a power supply specification reduce these numbers by 6% (47 Hz or 56 Hz).

Total Input Capacitance, C_{AP_INPUT} (µF)
Enter total input capacitance using Table 2 for guidance. The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage.

Nominal AC Input Voltage (VAC)	Total Input Capacitance per Watt Output Power (µF/W)
100 / 115	>2
Universal	>2
230	>1

Table 2. Suggested Total Input Capacitance for Different Input Voltage Ranges.

2	APPLICATION VARIABLES	INPUT	INFO	OUTPUT	UNITS	Design Title
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	85		85	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			85-265 VAC		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	450.0		450.0	µF	Input capacitor
9	VOUT	42.00		42.00	V	Output voltage at the board
10	IOUT	4.000		4.000	A	Output current
11	POUT		Info	168.00	W	The specified output power exceeds the device power capability: Verify thermal performance if no other warnings
12	EFFICIENCY	0.89		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.60		Z-factor estimate

Figure 2. Application Variable Section of TOPSwitchGaN Design Spreadsheet. Note the Gray Override Cells which Allow the User to Specify Values.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	132	50 / 60
United States, Canada	120	90	132	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	90	265	50
Indonesia, Thailand, Vietnam	220	185	265	50
	115, 120, 127	90	155	50 / 60
UK and rest of Europe, Asia, Africa, Americas and rest of the world	220, 230 240	185 185	265 265	50 / 60 50

Table 3. Guide to Typical line Voltage Conditions Encountered in Different Geographic Regions.

Nominal Output Voltage, V_{OUT} (V)

Enter the nominal Output voltage of the main output at full load. Usually for a multi output power supply, the main output is the output from which feedback is derived.

Power Supply Output Current, I_{OUT} (A)
This is the maximum continuous load current of the power supply. If the power supply has multiple outputs, enter the output current which allows the product of VOUT and IOUT will match the intended total output power.

Output Power, P_{OUT} (W)
This is a calculated value and will be automatically adjusted.

Power Supply Efficiency, (η)
Enter the estimated efficiency of the complete power supply measured between the input and output terminals under peak load conditions and worst-case line (lowest input voltage). Use a value of 0.86 if no other data is available. Once a prototype has been constructed the measured efficiency should be entered, and further transformer iteration(s) can be performed if necessary.

Power Supply Loss Allocation Factor, FACTOR_ Z
This factor describes the apportioning of losses between the primary and the secondary sides of the power supply. Z factor is used together with the efficiency to determine the actual power that must be delivered by the power stage. This is required because losses in the input stage (EMI filter, rectification etc.) are not processed by the power stage (transferred through the transformer) and so although they reduce efficiency the transformer design is not affected.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

For designs that do not have a peak power requirement, a Z value of 0.5 is recommended. For designs with a peak power requirement enter 0.65. The higher number indicates the increased secondary-side losses typically seen with peak-power designs.

Step 2 – Primary Controller Selection

Enter: Device Current Limit mode, ILIMIT and Generic Device Code, DEVICE_GENERIC

18	PRIMARY CONTROLLER SELECTION	INPUT	INFO	OUTPUT	UNITS	Design Title
19	PACKAGE_DEVICE	eSIP		eSIP		Device Package
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	TOP7075		TOP7075		Generic device code
22	DEVICE_CODE			TOP7074E		Actual device code
23	POUT_MAX		Warning	165	W	Power output desired is more than the power capability of the device. Please select a different device or reduce power output desired.
24	RDSON_100DEG			0.49	Ω	Primary switch on-time drain resistance at 100 ºC
25	ILIMIT_MIN			4.185	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			4.500	A	Typical current limit of the primary switch
27	ILIMIT_MAX			4.815	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			800	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.94	V	Primary switch on-time drain voltage
30	VDRAIN_OFF_PRSW			633.7	V	Peak drain voltage on the primary switch during turn-off. A 130 V leakage spike voltage is assumed

Figure 3. Primary Controller Selection in the TOPSwitchGaN Family Design Spreadsheet.

Generic Device Code, DEVICE_SERIES
The default option is automatically selected based on input type, input voltage range, and maximum output power.

For manual selection of device size, refer to the TOPSwitchGaN family power table from Table 1 and select a device based on the input type and output power. If the continuous power exceeds the value given in the power table (Table 1), then the next larger device should be selected. If the continuous power is close to the maximum power given in the power table, it may be necessary to switch to a larger device based on the actual measured thermal performance of the prototype.

On-Time Drain Voltage, VDRAIN_ON_PRSW (V)
This parameter is calculated based on RDSON_100DEG and primary RMS current.

Drain Peak Voltage, $V_{DRAIN\_OFF\_PRSW}$ (V)
This parameter is the assumed drain-to-source voltage seen by the device during off-time. A warning will be shown if this parameter exceeds 650 V. The calculation assumes a 130 V leakage spike.

$$V_{DRAIN} < (VIN\_MAX \times 1.414) + VOR + V_{(LK\text{-}PRI)}$$

$V_{(LK\text{-}PRI)}$ is the voltage induced by the leakage inductance of the transformer when TOPSwitchGaN IC turns-off.

Other data sheet electrical parameters are displayed **POUT_MAX, RDSON_100DEG, VDRAIN_BREAKDOWN.**

Step 3 – Worst-Case Electrical Parameters

Enter: FSWITCHING_MAX, VOR and LPRIMARY_TOL, or VMIN

34	WORST CASE ELECTRICAL PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
35	FSWITCHING_MAX	126000		126000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage.
36	VOR	130.0		130.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			94.62	V	Valley of the minimum input AC voltage at full load
38	KP		Info	0.44		Design is too continuous and may result in leading edge SOA triggering: increase the VOR
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.581		Primary switch duty cycle
41	TIME_ON			12.50	µs	Primary switch on-time
42	TIME_ON_AT_FSWITCHING_MAX			4.61		Primary switch on-time at FSWITCHING_MAX
43	TIME_OFF			3.32	µs	Primary switch off-time at 85 VAC, 168 W, and 126000 Hz.
44	LPRIMARY_MIN			226.4	µH	Minimum primary inductance
45	LPRIMARY_TYP			238.3	µH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			250.2	µH	Maximum primary inductance
48						
49	PRIMARY CURRENT					
50	IPEAK_PRIMARY			4.734	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			2.385	A	Primary switch current pedestal
52	IAVG_PRIMARY			1.926	A	Primary switch average current
53	IRIPPLE_PRIMARY			2.838	A	Primary switch ripple current
54	IRMS_PRIMARY			2.603	A	Primary switch RMS current
55						
56	SECONDARY CURRENT					
57	IPEAK_SECONDARY			14.793	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			7.452	A	Secondary winding current pedestal
59	IRMS_SECONDARY			6.905	A	Secondary winding RMS current

Figure 4. Worst-Case Electrical Parameters Section of TOPSwitchGaN Design Spreadsheet with Gray Override Cells.

Switching Frequency, FSWITCHING_MAX (Hz)
This parameter is the switching frequency at full load and minimum input voltage. The maximum switching frequency for TOPSwitchGaN devices is 150 kHz. In normal operation, the switching frequency at full load is below the maximum switching frequency described in the data sheet.

The programmable switching frequency range is 60 kHz to 142 kHz. Pushing frequency higher to reduce transformer size is possible but the designer will need to consider the primary inductance, peak current, and parts tolerances to ensure that the design can deliver the required energy at the minimum input voltage. We recommend a maximum operating frequency of 130 kHz to ensure adequate margin for part tolerances and effective jitter function.

Reflected Output Voltage, VOR (V)
This parameter is the secondary winding voltage during the diode conduction-time reflected back to the primary through the turns ratio of the transformer. The default value is 115 V. VOR can be adjusted if necessary to meet design rules.

For design optimization purposes, the following factors should be considered,

- Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery.
- Higher VOR reduces the voltage stress on the output diode(s), which in some cases may allow a lower voltage rated device to be used, typically increasing efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary-side which may increase secondary-side copper, and diode losses thereby reducing efficiency.

It should be noted that there are exceptions to this guidance especially for very high output currents where the VOR should be reduced to obtain highest efficiency. Higher output voltages (above 15 V) should employ a higher VOR to maintain an acceptable peak inverse voltage (PIV) across the output diode.

Optimal selection of VOR depends on the specific application and is based on a compromise between the factors mentioned above.

Minimum Rectified Input Voltage, VMIN
Valley of the rectified minimum AC input voltage at full power is calculated based on input capacitance **(CAP_INPUT)**.

Mode of Operation, KP
KP is a measure of how discontinuous or continuous the mode of switching is. KP > 1 is described as discontinuous operation (DCM), while KP < 1 denotes continuous operation (CCM).

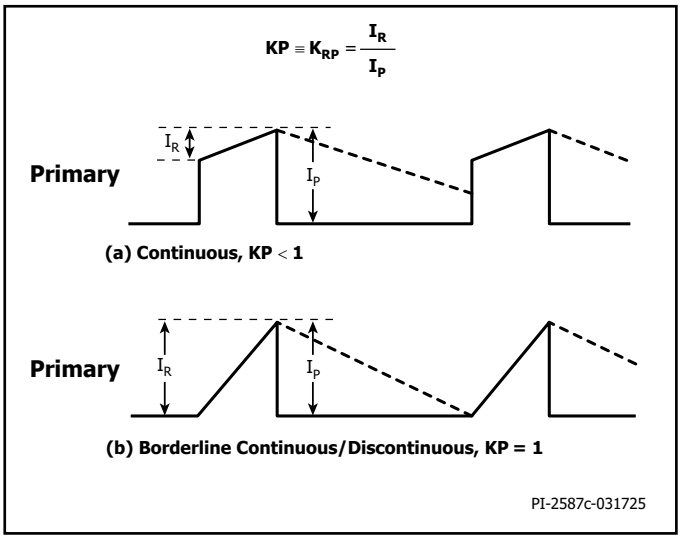


Figure 5. Continuous Mode Current Waveform, KP ≤ 1.

Ripple to Peak Current Ratio, KP
KP is the ratio of ripple current to peak primary current (Figure 5).

$$KP = K_{RP} = I_R / I_P$$

KP value > 1. In this case, KP is the ratio of primary switch off-time to secondary diode conduction time.

$$KP = K_{DP} = \frac{(1 - D) \times T}{t}$$

$$= \frac{VOR \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

The value of KP should be greater than 0.4. Guidance is given in the comments cell if the value of KP drops below 0.4.

Experience has shown that a KP value between 0.8 and 1.0 will result best efficiency by ensuring DCM or critical mode operation (CRM).

The spreadsheet will calculate the values of peak primary current, primary RMS current, primary ripple current, primary average current, and maximum duty cycle for the design based on the parameters chosen.

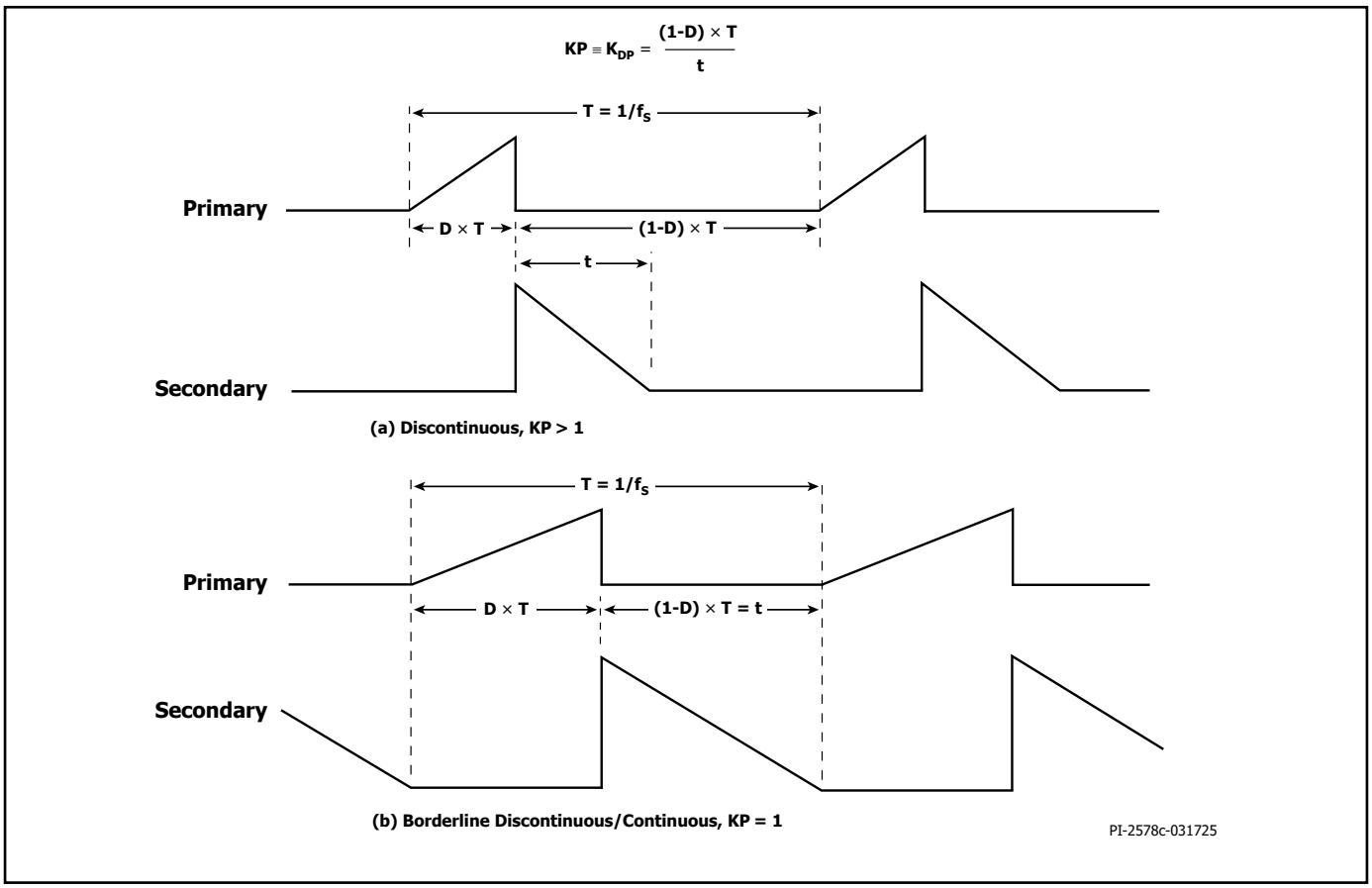


Figure 6. Discontinuous Mode Current Waveform, KP ≥ 1.

Typical Primary Inductance, LPRIMARY_TYP (µH)
This is the typical transformer primary inductance target value.

Primary Inductance Tolerance, LPRIMARY_TOL (%)
This parameter is the assumed primary inductance tolerance. A value of 5% is used by default, however if specific information is provided by the transformer vendor, then this value may be entered in the grey override cell. LPRIMARY_MIN and LPRIMARY_MAX will be calculated based on LPRIMARY_TOL.

Minimum Primary Inductance, LPRIMARY_MIN (µH)
Minimum possible primary inductance. LPRIMARY_MIN is calculated based on LPRIMARY_TOL.

Maximum Primary Inductance, LPRIMARY_MAX (µH)
Maximum possible primary inductance. LPRIMARY_MAX is calculated based on LPRIMARY_TOL.

PRIMARY CURRENT
IPEAK_PRIMARY – Peak primary current
IPEDESTAL_PRIMARY – Primary PowiGaN switch current pedestal in CCM mode
IAVG_PRIMARY – Primary PowiGaN switch average current
IRIPPLE_PRIMARY – Primary PowiGaN switch ripple current
IRMS_PRIMARY – Primary PowiGaN switch RMS current

SECONDARY CURRENT
IPEAK_SECONDARY – Peak secondary current IPEDESTAL_
SECONDARY – Secondary winding current pedestal IRMS_
SECONDARY – Secondary winding RMS current

Step 4 – Transformer Construction Parameters

Enter: CORE, AE, LE, AL, VE, BOBBIN, AW, BW, MARGIN
Choose core and bobbin based on maximum output power.

63	TRANSFORMER CONTRUCTION PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
64	CORE SELECTION					
65	CORE	PQ32		PQ32		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
66	CORE CODE			PQ32/30-3C95		Core code
67	AE			167.00	mm^2	Core cross sectional area
68	LE			74.70	mm	Core magnetic path length
69	AL			6200	nH/turns^2	Ungapped core effective inductance
70	VE			12500.0	mm^3	Core volume
71	BOBBIN			CPV-PQ32/30-1S-12P-Z		Bobbin
72	AW			98.18	mm^2	Window area of the bobbin
73	BW			18.70	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75						
76	PRIMARY WINDING					
77	NPRIMARY			25		Primary turns
78	BPEAK			2978	Gauss	Peak flux density
79	BMAX			2813	Gauss	Maximum flux density
80	BAC			826	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			381	nH/turns^2	Typical gapped core effective inductance
82	LG			0.519	mm	Core gap length
83						
84	PRIMARY BIAS WINDING					
85	NBIAS_PRIMARY			3	turns	Primary bias winding number of turns
86						
87	SECONDARY WINDING					
88	NSECONDARY	8		8	turns	Secondary winding number of turns
89						
90	SECONDARY BIAS WINDING					
91	NBIAS_SECONDARY			3	turns	Secondary bias winding number of turns

Figure 7. Transformer Core and Construction Variables Section of the TOPSwitchGaN family PIXLs Spreadsheet.

Core Type, CORE
The user must select the core to use. Different core types and sizes from the drop-down list are available to choose from. If a user-preferred core is not available, the grey override cells (AE, LE, AL, VE, AW, Bobbin & BW) can be used to enter the core and bobbin parameters directly from the manufacturer's data sheet.

Output Power at 75 kHz Universal Inputs	Core and Bobbin Table								
	Core						Bobbin		
	Core	Code	AE (mm^2)	LE (mm)	AL (nH/T^2)	VE (mm^3)	Code	AW (mm^2)	BW (mm)
0 W – 10 W	EE10	PC47EE10-Z	12.1	26.1	850	300	B-EE10-H	12.21	6.60
0 W – 10 W	EE13	PC47EE13-Z	17.1	30.2	1130	517	B-EE13-H	18.43	7.60
0 W – 10 W	EE16	PC47EE16-Z	19.2	35.0	1140	795	B-EE16-H	14.76	8.50
0 W – 10 W	EE19	PC47EE19-Z	23.0	39.4	1250	954	B-EE19-H	29.04	8.80
10 W – 20 W	EE22	PC47EE22-Z	41.0	39.4	1610	1620	B-EE22-H	19.44	8.45
10 W – 20 W	EE25	PC47EE25-Z	41.0	47.0	2140	1962	B-EE25-H	62.40	11.60
20 W – 50 W	EE30	PC47EI30-Z	111.0	58.0	4690	6290	B-EE30-H		13.20
0 W – 10 W	RM5	PC95RM05Z	24.8	23.2	2000	574	B-RM05-V		4.90
10 W – 20 W	RM6	PC95RM06Z	37.0	29.2	2150	1090	B-RM06-V		6.20
20 W – 30 W	RM8	PC95RM08Z	64.0	38.0	5290	2430	B-RM08-V	30.00	8.80
30 W – 50 W	RM10	PC95RM10Z	96.6	44.6	4050	4310	B-RM10-V		10.00
45 W – 65 W	EQ25	EQ25-3C96	100	41.4	4400	4145	EQ25-15.5A-4P-TH-J-12	34.83	8.1
50 W – 70 W	PQ26/20	PC95PQ26/20Z-12	119	46.3	7470	5490	BPQ26/20-1112CPFR	30.7	9.2
70 W – 100 W	EER35	PC47EER35-Z	107	90.8	2770	9720	EER35 - 1 (P8-S8)	154.4	26.4
70 W – 100 W	EI35	PC47EI35-Z	101	67.1	3800	6780	EE35 - 1 (P6-S6)	88.7	15.7
70 W – 100 W	PQ26/25	PQ26/25-3C95	120	54.3	6010	6530	PQ26/25 - 2 (P6-S6)	47.5	13.55
100 W – 150 W	ATQ27	ATQ27/18.4	129	51	6200	6579	ATQ27/18.4 - 1 (P2-S2)	56.16	10.4
100 W – 150 W	RM12/I	RM12/I-3C95	146	56.6	6790	8340	RM12/I - 1 (P6-S6)	75	14.3
100 W – 150 W	PQ32/20	PC32/20-3C95	169	55.9	7560	9440	PQ 32/20 (P6-S6)	47.3	9.1
> 150 W	PQ3535	PQ35/35-3C95	190	86.1	6600	16300	PQ35V(P6+S6)	164.64	20.8
> 150 W	PQ4040	PQ40/40-3C95	201	102	6100	20500	PQ4040-1(P6+S6)	233.68	25.4
> 150 W	E42	E42/15-3C95	178	97	6950	22700	E42/21/20-3(P6-S6)	177.48	26.1
> 150 W	E55	E55/28/21-3C95	353	124	8625	44000	E55/28/21-1(P7-S7)	286.27	33

Table 4. Commonly Available Cores and Power Levels at Which These Cores Can be used for Typical Designs.

Safety Margin, MARGIN (mm)
For designs that require safety isolation between primary and secondary, but that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical; however if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin is only present on one side of the bobbin. For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet required safety creepage distances. Typically several bobbins exist for each core size and each will offer different mechanical spacing. Refer to the bobbin data sheet and applicable standards to determine what specific margin is required.

Margin reduces the available area for the windings so marginated construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero margin approach using triple insulated wire.

Primary Turns, NPRIMARY
This is the number of turns for the main winding of the transformer calculated based on VOR and Secondary Turns.

Peak Flux Density, BPEAK (Gauss)
A maximum value of 3800 gauss is recommended to limit the peak flux density at maximum current limit and 150 kHz operation. Under an output-short condition, the output voltage is low and little reset of the transformer occurs during the PowiGaN switch off-time. This allows the transformer flux density to "staircase" beyond the normal operating level. A value of 3800 gauss at the maximum current limit of the selected device together with the built in protection features of TOPSwitchGaN devices provides sufficient margin to prevent core saturation under output short-circuit conditions.

Maximum Flux Density, BMAX (Gauss)
Light load operation can generate audible noise from the transformer, especially if a long core is used. To limit audible noise, the transformer should be designed such that the maximum core flux density is below 3000 gauss (300 mT). Following this limit for flux density and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of audible noise performance should be made using production transformer samples before approving the design.

AC Flux Density, BAC (Gauss)
The BAC value is used to calculate core loss.

Gapped Core Effective Inductance, ALG: (nH/N^2)
Used to determine the CORE GAP [LG].

Primary Bias Winding Turns, NBIAS_PRIMARY
Calculated integer number determined from the desired secondary number of turns NSECONDARY and the primary bias winding voltage VBIAS_PRIMARY.

Secondary Winding Turns, NSECONDARY
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the peak operating flux density BPEAK is kept below of 3800 gauss (380 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired.

Secondary Bias Winding Turns, NBIAS_PRIMARY
Calculated integer number based on the desired secondary number of turns NSECONDARY and the secondary bias winding voltage VBIAS_SECONDARY.

Step 5 – Primary Components Selection

Enter: BROWN-IN VOLTAGE, VBIAS, VF_BIAS

Required Line Undervoltage Brown-in, BROWN-IN REQUIRED
This is the input AC/DC voltage at which the power supply will turn on (once the brown-in threshold (I_{UV+}) is exceeded). The typical value is 20% below minimum AC input voltage (VIN_MIN). The brown-in voltage can be changed to a specific voltage [C97].

Line Undervoltage / Overvoltage Sense Resistor, RLS
The spreadsheet will calculate the resistance value based on the brown-in voltage. Shown as R_{LS1} + R_{LS2} on Figure 1, they are typically connected at the bulk capacitor. Typical total value for R_{LS1} and R_{LS2} is 4.02 MΩ. Resulting to a total resistance (RLS) of 8.04 MΩ RLS is approximately equal to [($V_{BROWN-IN}$ × 1.414) – 2.5] / I_{UV+} for AC input and [$V_{BROWN-IN}$ – 2.5] / I_{UV+} for DC input.

BROWN-IN ACTUAL
Calculated brown-in input AC or DC input voltage based on the calculated RLS resistance and I_{UV+}.

BROWN-OUT ACTUAL
Calculated brown-out input AC or DC input voltage based on the calculated RLS resistance and I_{UV-}.

Line Overvoltage, OVERVOLTAGE_LINE
This is the input AC or DC input voltage at which the power supply will immediately stop switching once the overvoltage threshold current (I_{OV+}) is exceeded. Switching will be when switching the line overvoltage recovery threshold (I_{OV-}) is reached. Line OV voltage is approximately equal to:

[(I_{OV+} × RLS) + 2.5] / 1.414 for AC Input

[(I_{OV+} × RLS) + 2.5] for DC Input

Primary Bias Voltage, VBIAS_PRIMARY
This is the bias voltage when the main output is at full load. A default value of 12 V is assumed. The voltage may be set to different values (for example for applications when the bias winding output is also used as a non-isolated primary-side auxiliary output). Higher voltages typically increase no-load input power. Values below 10 V are not recommended since at light load there may be insufficient voltage to supply current to the BYPASS pin which will increase no-load input power.

Bias Diode Forward Drop, VF_BIAS_PRIMARY
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the bias winding (D_{BIAS}).

Reverse Voltage Primary Bias, VREVERSE_BIASDIODE_PRIMARY
Calculated reverse voltage across the primary bias diode. Parasitic voltage ring is not included.

Bias Supply Capacitor, CBIAS_PRIMARY
A 22 µF, 25 V low ESR electrolytic capacitor is recommended for the bias winding rectification filter capacitor, C_{BIAS}. This will also improve no-load and standby input power.

BP Pin Capacitor, CBP
Although, electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they can be placed very close to the IC. A ceramic capacitor X7R (or better), rated to 10 V, and 0805 size or larger is recommended.

95	PRIMARY COMPONENT SELECTION	INPUT	INFO	OUTPUT	UNITS	Design Title
96	LINE UNDERVOLTAGE					
97	BROWN-IN REQURED			66.30	V	Required AC RMS/DC line voltage brown-in threshold
98	RLS			6.80	MΩ	Connect two 3.4 MΩ resistors to the V pin for the required UV/OV threshold
99	BROWN-IN ACTUAL			55 - 67.7	V	Actual AC RMS/DC brown-in range
100	BROWN-OUT ACTUAL			46.9 - 58.5	V	Actual AC RMS/DC brown-out range
101						
102	LINE OVERVOLTAGE					
103	OVERVOLTAGE_LINE		Info	256.4 - 287.7	V	The line over-voltage threshold is lower than the maximum input AC RMS/DC voltage

Figure 8. Primary Components Section of TOPSwitchGaN PIXls Spreadsheet.

Step 6 – Bias Components

	BIAS COMPONENTS	INPUT	INFO	OUTPUT	UNITS	Design Title
104						
105	PRIMARY BIAS DIODE					
106	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
107	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE_ PRIMARY			60.55		Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
110	CBP			0.47	µF	BP pin capacitor
115	VREF_REG			1.25	V	Reference voltage of the feedback
116	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
117	RFB_LOWER			3.09	kΩ	Lower feedback resistor
118						
119	SECONDARY BIAS DIODE					
120	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
121	VBIAS_SECONDARY	12.0		12.0	V	Rectified secondary bias voltage
122	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
123	VREVERSE_BIASDIODE_ SECONDARY			56.80	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
124	CBIAS_SECONDARY			10	µF	Bias winding rectification capacitor

Figure 9. Secondary Component Section of TOPSwitchGaN family PIXLs Spreadsheet.

Enter: VREF_REG and RFB_UPPER

Feedback Reference Voltage, VREF_REG
This is the reference voltage for the feedback circuit. VREF_REG is used to calculate the upper and lower feedback resistor values.

Upper Feedback Resistor, RFB_UPPER
The RFB_UPPER resistor is calculated based on VOUT and feedback reference voltage (VREF_REG). The value will change if a specified value is used for the RFB_LOWER resistor.

Lower Feedback Resistor, RFB_LOWER
The RFB_LOWER resistor value is a user-defined parameter. A default value of 10 kΩ will be used if no specific value is provided.

Enable Secondary Bias, USE_SECONDARY_BIAS
Secondary bias supply is needed when the output voltage is too high to bias the secondary feedback circuit directly. If a secondary bias supply is required, select "Yes" from the drop-down list. Default setting in this field is "No".

Secondary Bias Voltage, VBIAS_SECONDARY
This is the secondary bias voltage when the main output is at full load. A default value of 5 V is assumed. The voltage may be set to a different value.

Secondary Bias Diode Forward Drop, VF_BIAS_SECONDARY
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the secondary bias winding.

Reverse Voltage Secondary Bias, VREVERSE_BIASDIODE_ SECONDARY
Calculated reverse voltage across the secondary bias diode. Parasitic voltage ring is not considered.

Secondary Bias Supply Capacitor, CBIAS_SECONDARY
A 47 µF low ESR electrolytic capacitor is recommended for the bias winding rectification filter capacitor, CBIAS_SECONDARY.

127	MULTIPLE OUTPUT PARAMETERS	INPUT	INFO	OUTPUT	UNITS	Design Title
128	OUTPUT 1					
129	VOUT1			42.00	V	Output 1 voltage
130	IOUT1			4.00	A	Output 1 current
131	POUT1			168.00	W	Output 1 power
132	VD1			0.70	V	Forward voltage drop of diode for output 1
133	NS1			8.00	turns	Number of turns for output 1
134	ISPEAK1			14.79	A	Instantaneous peak value of the secondary current for output 1
135	ISRMS1			6.905	A	Root-mean-squared value of the secondary current for output 1
136	ISRIPPLE1			5.628	A	Current ripple on the secondary waveform for output 1
137	PIV1_CALCULATED			193.41	V	Computed peak inverse voltage stress on the diode for output 1
138	OUTPUT_RECTIFIER1	AUTO		BYV32-200		Recommended diode for output 1.
139	PIV1_RATING			200.00	V	Peak inverse voltage rating on the diode for output 1
140	TRR1			25.00	ns	Reverse recovery time of the diode for output 1
141	IFM1			18.00	A	Maximum forward continuous current of the diode for output 1
142	PLOSS_DIODE1			8.18	W	Maximum diode power loss for output 1

Figure 10. Secondary Components Section of TOPSwitchGaN Spreadsheet.

Step 7 – Multiple_Output Parameters

This section allows the user to design up to three secondary outputs (excluding bias supply) and choose suitable secondary rectifier diode. The spreadsheet will provide a warning should the total power of the multiple outputs exceed the power described in the **POUT** cell.

For single output design, cells **VOUT1**, **IOUT1** and **POUT1** will be the main output parameters entered in section 1.

Each output provides a selection of typical diode types for the secondary rectifier in drop-down menu. Based on the secondary rectifier diode chosen, diode forward voltage drop **VD1 (V)**, rated diode reverse voltage **PIV1_RATING (V)**, diode reverse recovery time **TRR1 (ns)**, and diode maximum forward continuous current **IFM1 (A)** will be displayed in the spreadsheet.

The spreadsheet also calculates the critical electrical parameters for each secondary output:

Number of Turns for Output1, NS1
Calculated turns for each output.

Instantaneous Secondary Peak Current, IPEAK1 (A)
Used to select the secondary rectifier diode.

RMS Current of the Secondary Output, ISRM1 (A)
Used to set the diameter of the secondary winding wire.

Current Ripple on Secondary, IRIPPLE1 (A)
Used to select the output filter capacitor.

Calculated Diode Reverse Voltage , PIV1 (V)
Calculated diode reverse voltage stress for selection of the secondary rectifier diode.

Calculated Secondary Rectifier Diode Power Loss, PLOSS_DIODE1 (W)
Calculated secondary rectifier diode power loss for device selection and temperature management.

144	OUTPUT 2	INPUT	INFO	OUTPUT	UNITS	Design Title
145	VOUT2			0.00	V	Output 2 voltage
146	IOUT2			0.000	A	Output 2 current
147	POUT2			0.00	W	Output 2 power
148	VD2			N/A	V	Forward voltage drop of diode for output 2
149	NS2			N/A	turns	Number of turns for output 2
150	ISPEAK2			N/A	A	Instantaneous peak value of the secondary current for output 1
151	ISRMS2			N/A	A	Root mean squared value of the secondary current for output 2
152	ISRIPPLE2			N/A	A	Current ripple on the secondary waveform for output 2
153	PIV2			N/A	V	Computed peak inverse voltage stress on the diode for output 2
154	OUTPUT_RECTIFIER2	AUTO		N/A		Recommended diode for output 2.
155	PIV2_RATING			N/A	V	Peak inverse voltage rating on the diode for output 2
156	TRR2			N/A	ns	Reverse recovery time of the diode for output 2
157	IFM2			N/A	A	Maximum forward continuous current of the diode for output 2
158	PLOSS_DIODE2			N/A	W	Maximum diode power loss for output 2
159						
160	OUTPUT 3					
161	VOUT3			0.00	V	Output 3 voltage
162	IOUT3			0.000	A	Output 3 current
163	POUT3			0.00	W	Output 3 power
164	VD3			N/A	V	Forward voltage drop of diode for output 3
165	NS3			N/A	turns	Number of turns for output 3
166	ISPEAK3			N/A	A	Instantaneous peak value of the secondary current for output 1
167	ISRMS3			N/A	A	Root mean squared value of the secondary current for output 3
168	ISRIPPLE3			N/A	A	Current ripple on the secondary waveform for output 3
169	PIV3			N/A	V	Computed peak inverse voltage stress on the diode for output 3
170	OUTPUT_RECTIFIER3	AUTO		N/A		Recommended diode for output 3.
171	PIV3_RATING			N/A	V	Peak inverse voltage rating on the diode for output 3
172	TRR3			N/A	ns	Reverse recovery time of the diode for output 3
173	IFM3			N/A	A	Maximum forward continuous current of the diode for output 3
174	PLOSS_DIODE3			N/A	W	Maximum diode power loss for output 2
175						
176	PO_TOTAL			168.00	W	Total power of all outputs
177	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Figure 11. Multiple Output Parameters Section of TOPSwitchGaN PIXIs Spreadsheet. (continued)

Step 8 – Critical External Component Selection

The schematic in Figure 12 shows the key external components required for a practical single output TOPSwitchGaN IC based design. Component selection criteria are as follows:

Bypass Pin Capacitor (C_{BP})
Although electrolytic capacitors can be used, surface mount multi-layer ceramic capacitors are often preferred for double-sided boards as they can be placed close to the IC. A surface mount multi-layer ceramic X7R capacitor rated for 10 V or greater with 0805 size or bigger package is recommended.

In addition, the BP capacitor tolerance should be equal or better than indicated below taking into account the ambient temperature range of the target application. The minimum and maximum acceptable capacitor tolerance values are set by IC characterization.

Line Sense Resistors (R_{LS1} and R_{LS2})
Line sensing helps to ensure that the IC will operate within the designed input voltage range, protecting the power supply from line undervoltage and line overvoltage conditions.

The TOPSwitchGaN IC will start to switch when the V pin senses a current greater than the V Pin Brown-In Threshold (I_{UV+}). The TOPSwitchGaN IC will be disabled when the V pin senses a current lower than the V Pin Brown-Out Threshold (I_{UV-}). Increasing the input voltage, TOPSwitchGaN IC will stop switching when the V pin senses a current higher than the V Pin Line Overvoltage Threshold (I_{OV+}). The TOPSwitchGaN IC will resume operation once the V pin senses a current lower than the V Pin Line Overvoltage Recovery Threshold (I_{OV-}).

General Formula:

$$I_{UV+} = (V_{IN} - V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$$
$$I_{UV-} = (V_{IN} - V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$$
$$I_{OV+} = (V_{IN} - V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$$
$$I_{OV-} = (V_{IN} - V_{PIN\_Voltage}) / (R_{LS1} + R_{LS2})$$

Where:

I_{UV+}: V Pin Brown-In Threshold
I_{UV-}: V Pin Brown-Out Threshold
I_{OV+}: V Pin Line Overvoltage Threshold
I_{OV-}: V Pin Line Overvoltage Recovery Threshold
$V_{PIN\_Voltage}$: V pin voltage = 2.5 V
$R_{LS1} + R_{LS2}$: Line sense resistors
V_{IN}: For DC input, V_{IN} = VDC_INPUT
For AC input, V_{IN} = VAC x 1.414

Connecting the V pin to SOURCE disables the line sensing function. It is not recommended to allow the V pin to float.

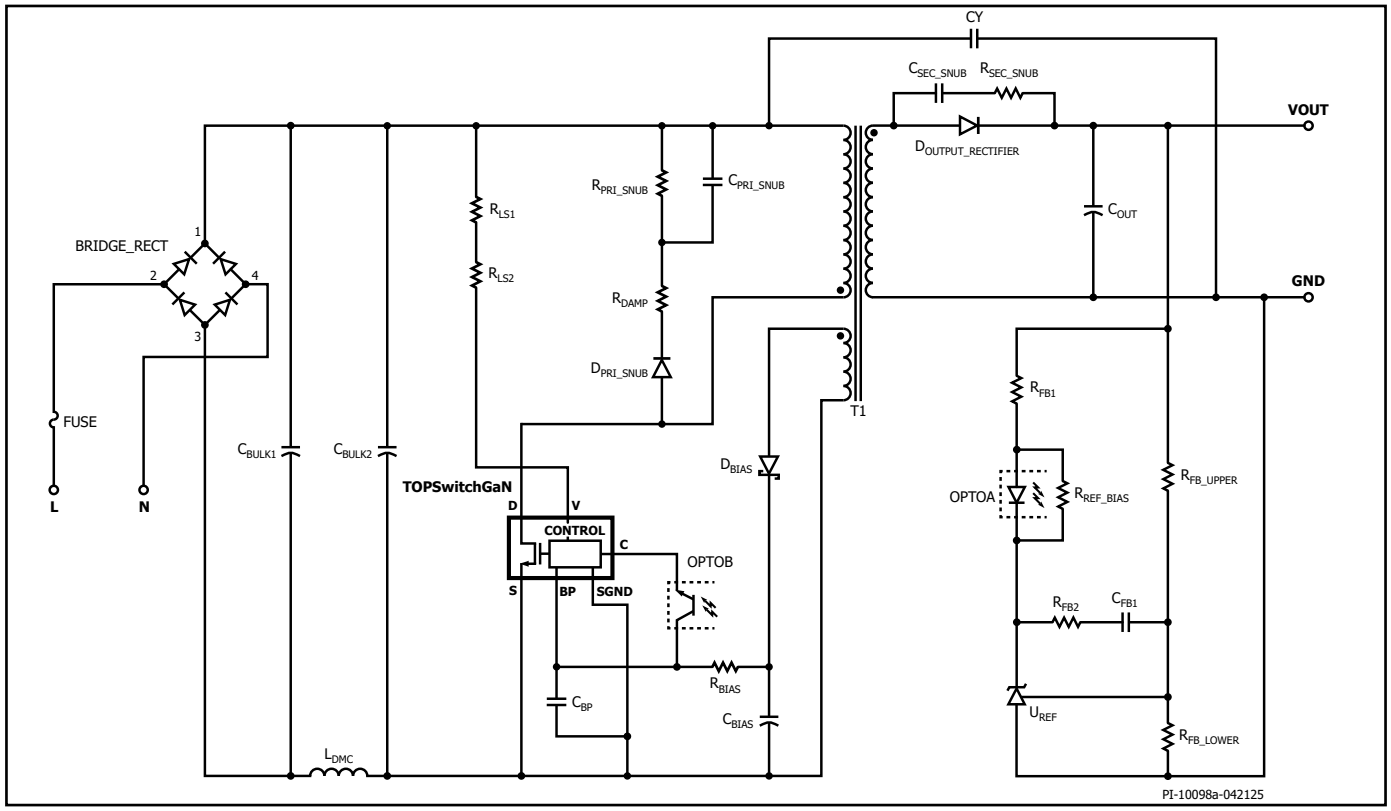


Figure 12. Typical TOPSwitchGaN Flyback Power Supply.

Primary Clamp Network Across Primary Winding

(D_{PRI_SNUB}, R_{DAMP}, R_{PRI_SNUB}, C_{PRI_SNUB})

An R2CD clamp is the most commonly used clamp in low power flyback power supplies. For higher power designs, a Zener clamp or the R2CD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 650 V (depending on derating requirements) under worst-case conditions (maximum input voltage, maximum overload power or output short- circuit). In Figure 12, the clamp diode, D_{PRI_SNUB} must be a standard recovery glass-passivated type, or a fast recovery diode with a reverse recovery time of less than 500 ns. The use of a standard recovery] glass passivated diode allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the power switch inside the TOPSwitchGaN IC turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{PRI_SNUB}. Resistor R_{DAMP}, which is in the series path, offers damping to prevent excessive ringing due to resonance between the leakage inductance and the output capacitance - C_{OSS} of the GaN switch. Resistor R_{PRI_SNUB} bleeds-off energy stored in capacitor C_{PRI_SNUB}. Different TOPSwitchGaN ICs will each have their own primary current and leakage inductance characteristics and therefore different leakage energy. Capacitor C_{PRI_SNUB} and resistor R_{PRI_SNUB} and R_{DAMP} should be optimized for each design. As general rule it is advisable to minimize the value of capacitor C_{PRI_SNUB} and maximize the value for R_{PRI_SNUB} and R_{DAMP}, while still meeting the 650 V BVDSS limit under worst case conditions. The value of R_{DAMP} should be large enough to reduce ringing in the required time but not so large as to cause the drain voltage to exceed 650 V BV_{DSS}.

A polyester film type or ceramic capacitor with an X7R dielectric, 1 kV rating and 1206 size are recommended for the primary clamp. A ceramic capacitor that uses a dielectric such as Z5U if used in the clamp circuit for C_{PRI_SNUB} may generate audible noise so should not be used.

Key Design Points Primary Clamp Circuit Optimization

- Assuming that Leakage inductance (L_{LK}) is less than 3% of primary inductance (L_p) is a good starting point for the calculation of primary clamp parameters. The Recommended next step is to measure the actual value of leakage inductance in a prototype transformer and modify the clamp and or magnetics design if necessary.
- Resistor R_{DAMP} must be large enough to prevent excessive ringing caused by the leakage inductance and the GaN switch output capacitance (C_{OSS}).
- Reduce the value of the snubber resistor R_{DAMP} to reduce power loss while monitoring the following:
  1. EMI performance
  2. Voltage across the primary switch
- Minimize leakage inductance by completely filling each winding layer.
- Further reduce clamp losses by optimizing the reflected voltage (VOR).
- Minimizing inter-winding capacitance - add layers of tape between each primary winding if appropriate.
- Optimizing layout and transformer construction to ensure a tightly coupled loop between the primary snubber and the primary winding.

Common Primary Clamp Configurations

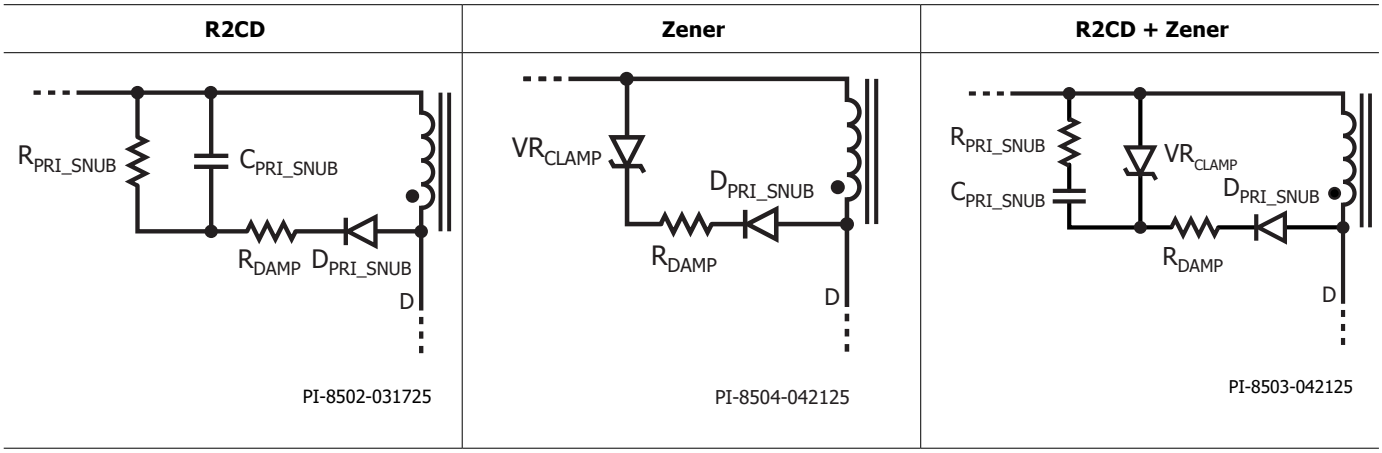


Figure 13. Recommended Primary Clamp Configurations.

Primary Clamp Circuit

Benefits	R2CD	Zener	R2CD + Zener
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 5. Respective Benefits of Different Primary Clamp Circuits.

External Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BIAS})

The BYPASS pin has an internal regulator that charges the BYPASS pin capacitor to V_{BP} by drawing current from the DRAIN pin whenever the primary switch is off. The BYPASS pin is the internal supply voltage interface node. When the primary switch is on, the device operates from the energy stored in the BYPASS pin capacitor. In addition, a shunt regulator clamps the BYPASS pin voltage to VSHUNT when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the TOPSwitchGaN IC to be powered externally through a bias winding, decreasing the no-load consumption.

12 V is the recommended bias voltage at full load. Higher voltage will increase no-load input power. Ultrafast or Schottky diodes are recommended for the bias winding rectifier to reduce no-load power consumption and increase standby input power efficiency.

A 22 µF, > 25 V low ESR (Equivalent Series Resistance) electrolytic aluminum capacitor is recommended for the bias supply filter, C_{BIAS}. Low capacitance and a low ESR (electrolytic capacitor) will help to improve the no-load input power and standby efficiency. The use of ceramic surface mount capacitors is not recommended as they can cause audible noise due to a piezoelectric effect in their mechanical structure.

To have the minimum no-load input power and high full load power efficiency, Resistor R_{BIAS} should be selected such that the current through this resistor is higher than the BYPASS pin current.

The BYPASS pin supply current at normal operating frequency can be calculated as shown below:

$$I_{SSW} = \frac{F_{SW}}{150\,kHz} \times (I_{S2} - I_{S1}) + I_{S1}$$

Where,

I_{SSW}: BYPASS pin supply current at operating switching frequency
F_{SW}: Operating switching frequency (kHz)
I_{S1}: BYPASS pin supply current at no switching (refer to data sheet)
I_{S2}: BYPASS pin supply current at 132 kHz (refer to data sheet)

The BP voltage is internally clamped to 5.3 V when bias current is higher than BYPASS pin supply current. If BP voltage is ~ 5.0 V, then this indicates that the current through R_{BIAS} is less than the BYPASS pin supply current and charge is being drawn from the DRAIN pin to keep the BYPASS pin above 5.0 V. This should be avoided, except during start-up.

To determine maximum value of R_{BIAS}:

$$R_{BIAS} = [V_{BIAS(Full\text{-}LOAD)} - V_{BP}]/I_{SSW}$$

$$V_{BP} = 5.3\ V$$

Secondary Rectifier Diode ($D_{OUTPUT\_RECTIFIER}$)

For each output, use the values of peak inverse voltage (PIV) and output current (IOUT) provided in the design spreadsheet to select the output diode's reverse voltage rating (VR).

$V_R \geq 1.25 \times$ PIV: where PIV is taken from the Multiple Output Parameters section of the spreadsheet.

$I_D \geq 2 \times$ IOUT: where I_D is the diode rated DC current, and IOUT is the average output current. Depending on the temperature rise and the duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heat sinking necessary.

To reduce the peak inverse voltage of secondary rectifier diode, it is necessary to select C_{SEC_SNUB} to be three times of parasitic capacitance and R_{SEC_SNUB} to make it approximately equal to the characteristic impedance of the oscillation due to the parasitic capacitance and inductance of the secondary rectifier circuit.

$$C_{SEC\_SNUB} = 3 \times c_0, \qquad R_{SEC\_SNUB} = \sqrt{\frac{L}{c_0}}$$

Where,

c_0: the parasitic capacitance
L: is the parasitic inductance of the secondary rectifier

The parasitic capacitance and inductance can be calculated from the frequency shift ratio (m) introduced by adding an arbitrary small capacitor in parallel with the secondary rectifier diode:

$$c_0 = \frac{c_1}{m^2 - 1}, \qquad L = \frac{(m^2 - 1)}{(2\pi f_0)^2 \times c_1}, \qquad m = \frac{f_0}{f_1}$$

Where,

c_1: an arbitrary external capacitor in parallel with a rectifier
m: the frequency shift ratio due to an external capacitor c_1
f_0: the natural circuit oscillation frequency without c_1
f_1: the shifted circuit oscillation frequency with c_1

Output Filter Capacitance (C_{OUT})

A low ESR electrolytic capacitor is one of the key components in reducing the output ripple voltage. Other parameters to be considered are their RMS ripple current rating, DC working voltage and ESR. The actual capacitance value is of secondary importance.

Considerations for selection of output capacitor:

1. Capacitor ripple rating (specified at 105 ºC, 100 kHz) must be larger than the expected ripple current (ISRIPPLE).
2. Use low ESR electrolytic capacitor. Output switching ripple voltage is ISPEAK x ESR.
3. Use parallel capacitors to increase ripple current capacity for high current outputs.

Output Capacitor Ripple Current Rating:

The spreadsheet calculates the output capacitor ripple current at the peak load condition. Therefore, the actual rating of the capacitor will depend on the peak-to-average power ratio of the design. For a conservative design select the output capacitor(s) such that the ripple rating is greater than the calculated value, ISRIPPLE from the spreadsheet, calculated at the peak load condition. In designs with high peak-to-continuous (average) power, the capacitor rating can be reduced based on the measured capacitor temperature rise under worst-case load and ambient temperature. If a suitable individual capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should be considered to ensure that the capacitor is not oversized.

Output Capacitor ESR:

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

$$ESR = \frac{V_{RIPPLE}}{ISPEAK}$$

Where V_{RIPPLE} is the maximum allowed output ripple and ISPEAK is the peak secondary current from spreadsheet Multiple Output Parameters section.

Output Capacitor Voltage Rating:
Select a voltage rating such that $V_{RATED} \geq 1.25 \times VOUT$. A margin of 25% is recommended for reliability purposes.

Output Post Filter Components (L_{PF} and C_{PF}):
If necessary, a post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 µH- 3.3 µH with a current rating above the peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥ 1.25 × VOUT. If a post filter is used, then the output voltage sense resistor and optocoupler should be connected before the post filter inductor. Figure 14 shows the connection of post filter components L_{PF} and C_{PF}.

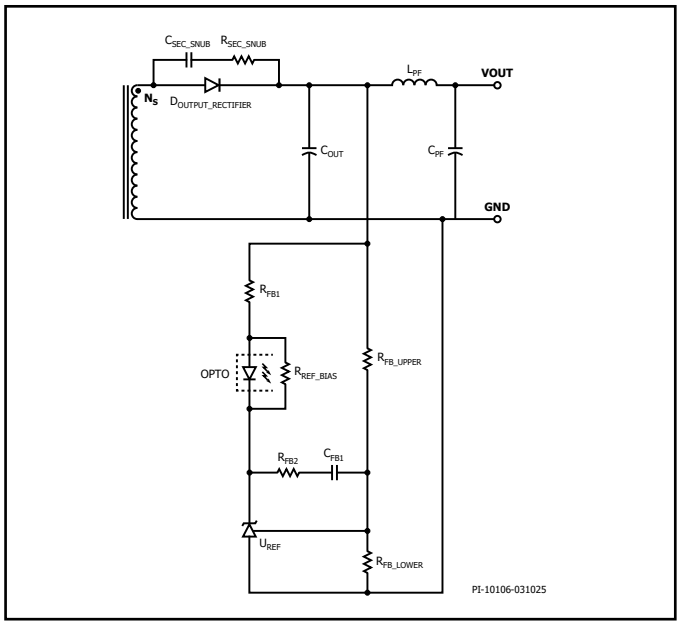


Figure 14. Secondary Output with Post Filter Components (L_{PF} and C_{PF}).

FEEDBACK Pin Divider Network (R_{FB_UPPER}, R_{FB_LOWER})
A suitable resistive voltage divider should be connected from the output of the power supply to the feedback circuit. The voltage across R_{FB_LOWER} will be made equal to the reference voltage of the feedback circuit.

Feedback Circuit
The reference IC (U_{REF}) - typically a TL431 is used to set the output voltage programmed via the resistor divider R_{FB_UPPER} and R_{FB_LOWER}. Resistor R_{REF_BIAS} provides the minimum cathode current for regulation of the TL431 (U_{REF}). Each reference IC type will have a different minimum cathode current for regulation, so it is recommended that the designer confirm minimum current requirements from the appropriate manufacturers data sheet. No-Load consumption will be reduced and light load efficiency will improve if an IC with low minimum cathode current is used. R_{FB1} sets the DC gain and limits the feedback current during output load transients. R_{FB2} and C_{FB1} adjust the role-off of the high frequency gain of U_{REF} so that it ignores output ripple. AC feedback is provided directly through the optocoupler. Use of an optocoupler with high CTR is recommended for reduced no-load input and better standby efficiency.

Key Applications Design Considerations

Output Power Table

The output power table in the data sheet (Table 1) represents the maximum practical continuous output power that can be obtained under the following conditions:

1. Minimum DC input voltage is 90 V or higher for 85 VAC input, and 220 V or higher for 230 VAC input.
2. Efficiency assumptions depend on input voltage range. Universal input voltage or low-line input assumes efficiency >87% increasing to >89% for a high-line input. The assumed efficiency is based on the lowest voltage of the input range.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain KP > 0.4 at a minimum input voltage to provide the maximum power. At high-line nominal, it recommended to design KP between 1 and 1.1 to increase efficiency.
5. Low forward voltage drop (V_F) Schottky O/P diode
6. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep SOURCE pin temperature at or below 110 °C at the required highest ambient temperature.
7. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
8. It is unique feature of TOPSwitchGaN IC that a designer can set the full-load switching frequency, between 25 kHz to 142 kHz depending on the transformer design. One of the ways to effectively lower device temperature is to design the transformer to operate at a low switching frequency, with a good starting point being 66 kHz. If smaller size transformer is needed, the operating switching frequency can be increased up to 130 kHz.

Primary-Side Overvoltage Protection
Primary-side output overvoltage protection provided by TOPSwitchGaN IC uses an auto-restart method that is triggered by a threshold current of I_{SD} flowing into the BYPASS pin. For the bypass capacitor to be effective as a high frequency filter, it should be located as close as possible to the SOURCE and BYPASS pins of the device.

Primary sensed output OVP can be realized by connecting a series combination of a Zener diode (V_{ZOVP}), a resistor (R_{OVP}), and a blocking diode (D_{OVP}) from the rectified and filtered bias winding output to the BYPASS pin (as shown if Figure 1616). The configuration will provide stable OVP level, with respect to output load. The OVP circuit will be activated based on the bias winding plateau level. The bias winding voltage spike cannot trigger the OVP circuit due to its short duration. Since there is little to no variation of the bias winding voltage plateau, the OVP trip voltage is constant across load.

The blocking diode (D_{OVP}) prevents any reverse current charging the bias capacitor during start-up. A small signal standard recovery diode is recommended for this role. The value of the series resistor (R_{OVP}) is set such that a current higher than I_{SD} will flow into the BYPASS pin during an output overvoltage event. Finally, the Zener diode will be selected based on the required output over voltage level, turns ratio of the secondary and bias winding, BP voltage, D_{OVP} voltage drop and voltage across R_{OVP} resistor.

Improve Noise immunity for high level ESD and Common mode surge (level 4 and higher) tests

It is recommended to add LC Pi filter at BP pin as shown in the Figure 15 to improve noise immunity for high level Electrostatic Discharge (ESD) and common mode ring wave tests.

The recommended impedance value for SMD ferrite bead is between 40 Ω to 50 Ω @ 100 MHz with a tolerance of ± 25% and a DC Resistance of < 1 Ω.

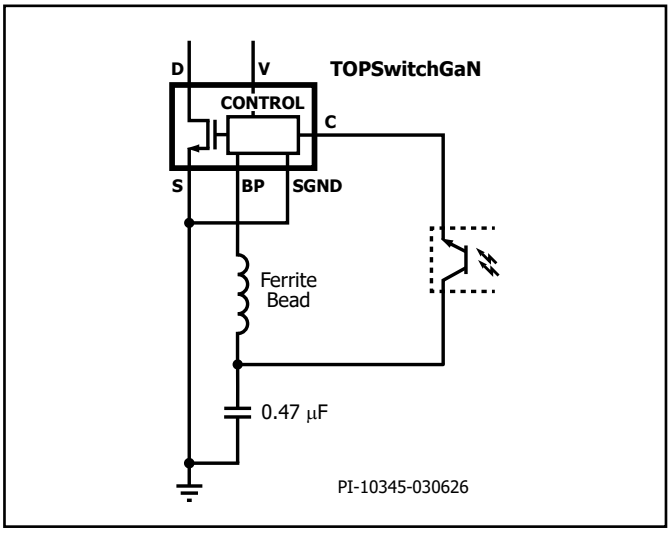


Figure 15. BP LC filter and optocoupler connection.

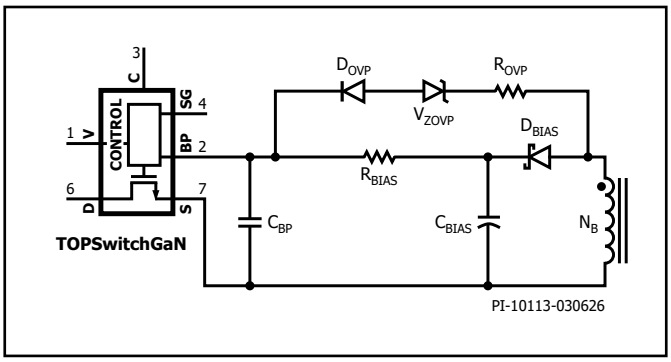


Figure 16. Primary-Side Secondary OVP Which Directs Current into the BP pin via Zener V_{ZOVP}.

Considerations for Selection of Output Capacitor:

Where:

$V_{BIAS\_WINDING\ OVP}$: Bias winding voltage when output reaches OVP level
V_{OUT_OVP} : Output voltage OVP level
$V_{F\_SEC\_DIODE}$: Output secondary rectifier V_F
N_{BIAS} : Bias winding turns
$N_{SECONDARY}$: Secondary winding turns
R_{OVP} : OVP resistor resistance
I_{SD} : BYPASS pin fault shutdown threshold current (please refer to the TOPSwitchGaN datasheet)
V_{Z_OVP} : OVP Zener diode voltage rating
V_{BP} : BYPASS pin voltage
V_{F_OVP} : V_F OVP circuit blocking diode

First, calculate the $V_{BIAS\_WINDING\ OVP}$ and select the appropriate Zener diode. The voltage drop of the Zener diode should be less than the $V_{BIAS\_WINDING\ OVP}$. Finally, calculate the value of resistor R_{OVP} .

$$V_{BIAS\_WINDING\_OVP} = (V_{out\_OVP} + V_{F\_SEC\ DIODE}) \times \frac{N_{BIAS}}{N_{SECONDARY}}$$ **No-load**

$$R_{OVP}I_{SD} + V_{Z\_OVP} = V_{BIAS\_WINDING\_OVP} - V_{BP} - V_{F\_DOVP}$$

Consumption.
The TOPSwitchGaN IC will start in a self-powered mode, drawing energy from the BYPASS pin capacitor that is charged from the internal current source in the TOPSwitchGaN IC (connected to the drain tab). A bias winding is required to provide supply current to the BYPASS pin once the TOPSwitchGaN IC has started switching. A bias winding supply to the BYPASS pin ensures low no-load power consumption. Resistor R_{BIAS} should be adjusted to achieve the lowest no-load input power.

The current limit for the TOPSwitch primary switch is set by the BP capacitor (C_{BP}) discharge time – measured at startup. The value of R_{BIAS} must be sufficient to prevent C_{BIAS} from significantly altering the discharge time of C_{BP} during this phase of operation. A blocking diode can also be added in series with the R_{BIAS} resistor to reduce power consumption at no-load.

Other areas that may help reduce no-load consumption:

1. Lower capacitance of primary clamp capacitor, C_{PRI_SNUB}.
2. Use a Schottky or ultrafast diode for the bias supply rectifier, D_{BIAS}.
3. Use a low ESR capacitor for bias supply filter capacitor, C_{BIAS}.
4. Use a low value RC snubber capacitor, C_{SEC_SNUB}, for the secondary rectifier.
5. Add tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter-winding capacitance.

Recommendation for EMI Reduction

1. Ensure appropriate component placement and minimize loop areas for the primary and secondary power circuits to reduce radiated and conducted EMI Aim for a compact loop area.
2. Adding a small capacitor in parallel with the clamp diode on the primary side can help reduce radiated EMI.
3. A resistor in series with bias winding can help reduce radiated EMI.
4. Common mode chokes (CMC) are typically required at the power supply input to attenuate common node noise. Alternatively, shield windings on the transformer can achieve similar performance. Shield windings can also be used with common mode filter inductors at the input to improve conducted and radiated EMI margines.
5. Adjusting RC snubber component values for the secondary rectifier diode can help reduce high frequency radiated and conducted EMI.
6. Use a pi-filter comprising differential inductors and capacitors in the input rectifier circuit to reduce low frequency differential EMI.
7. Connecting a 1 μF ceramic capacitor at the power supply output helps reduce radiated EMI.

Quick Design Checklist

As with any power supply, the operation of all TOPSwitchGaN part based designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

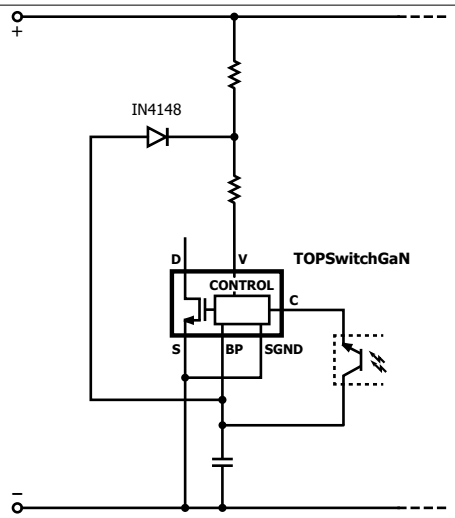
Maximum Drain Voltage
Verify that V_{DS} of TOPSwitchGaN IC does not exceed 650 V maximum continuous and 800 V for non-repetitive pulse and V_{DS} of secondary rectifier diode does not exceed 90% of the breakdown voltage at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current
At maximum ambient temperature, maximum input voltage and peak output (overload) power, review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary PowiGaN switch should be below the specified absolute maximum rating.

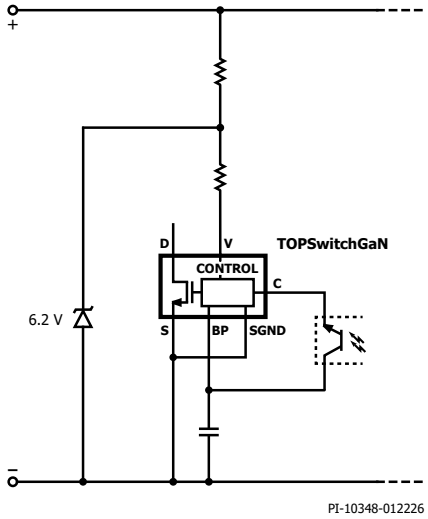
Thermal Check
At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for the TOPSwitchGaN IC, transformer bridge rectifier, secondary rectifier diode, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation.

Simple Circuit Ideas

Line OV Only
Diode biased from BPP and provides constant current into the VOLTAGE pin via R2 above I_{UV} threshold, thus disabling UV function of the IC.



Line UV Only
Zener clamps the voltage on R1-R2 node and provides constant voltage above I_{UV} thresholds, thus disabling OV function of the IC.



Wide Range Line UV/OV (for High Input Voltage Application)
Additional current supply flowing towards V-pin via BPP will increase the UV/OV ratio because current flowing through V-pin will be the summation of current from V pin resistors and current through R3 resistor.

Voltage stress in V-pin will be low during switch off time due to current flow R3.

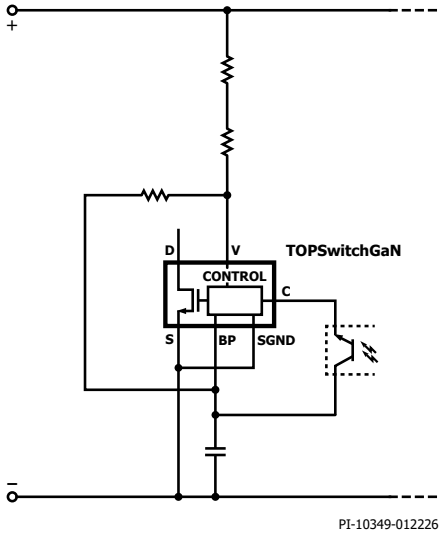
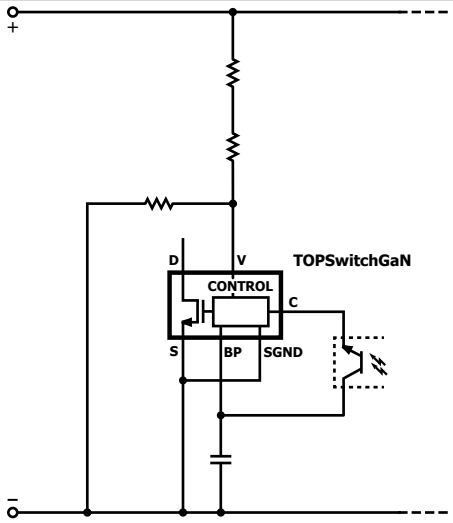


Figure 17. Circuit Ideas to Enhance Design.

Narrow Range
Reducing the current flowing towards V-pin will lower the UV/OV ratio.



Enable/Disable Circuit
Use two switches, Q1 (PNP) and Q2 (NPN), to control the current flowing into V pin to Enable/Disable circuit with logic level signal.

Logic High – Disable: V pin current = $(V_{BPP} / (R1//R2)) > I_{OV+}$
Logic Low – Enable: V pin current = $I_{UV+} < (V_{BPP} / R1) < I_{OV+}$

Note: TOPSwitchGaN device needs to be turned on first before receiving Logic High signal due to Innoswitch's own start-up sequence.

	Enable/ Disable Signal	Q3	Q2	TOPSwitch
Start-up Condition	Logic Low grounded or OPEN)	OFF	OFF	Switching
Disable TOPSwitch	Logic High	ON	ON	Not switching
Enable TOPSwitch	Logic Low (grounded or OPEN)	OFF	OFF	Switching

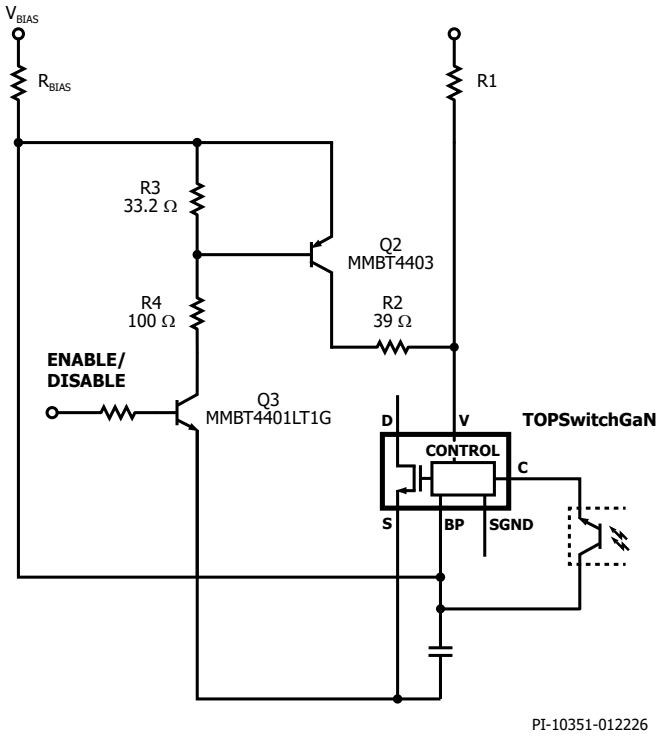


Figure 18 (cont.). Circuit Ideas to Enhance Design.

Recommendations for Circuit Board Layout

For this section refer to Figure 18 to Figure 21.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. C_{BIAS} ground should have a dedicated trace that is star-connected to the input filter capacitor ground pin.

Bypass Capacitors
The BYPASS pin decoupling capacitor (C_{BP}) must be located directly adjacent to the BYPASS and SOURCE pins. Ensure that the connections are routed via short traces.

Critical Loop Area
Circuits with high dv/dt or di/dt should be kept as small as possible. Minimize the area of the primary loop that connects the input filter capacitor, transformer primary, and IC. Similarly, reduce the area of the loop connecting the secondary winding, output rectifier diode, and output filter capacitor. (Figure 18 and Figure 19 loops 1 to 4)

To minimize crosstalk between circuits ensure that no loop area is placed inside another loop.

Drain Node
The drain switching node is the dominant noise generator. As such, the components connected to the drain node should be placed close to the IC and away from sensitive primary control circuits. The clamp circuit components should be located away from the BYPASS pin. Trace width and length in this circuit should be minimized.

Power Trace Routing
Current will flow through the path of least resistance. Even if the trace is connected to the capacitors, there is a possibility that the current will not flow to the capacitors which will make the capacitors ineffective. For best filtering and noise immunity, it is recommended that power signal traces to pass through the capacitors.

Primary Clamp Circuit
A clamp is used to limit the peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD or RCDZ clamp across the primary winding. To reduce EMI, minimize the loop area between the clamp components, the transformer, and the IC.

Y Capacitor
The Y capacitor should be placed directly from the positive terminal of the primary input filter capacitor to the output positive or return terminal of the transformer secondary. This placement will route high-magnitude common mode surge currents away from the IC. If an input pi EMI filter (C_{BULK1}, L_{DMC}, C_{BULK2}) is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

ESD Immunity
Sufficient clearance should be maintained between the primary-side and secondary-side circuits to ensure compliance with ESD and hi-pot isolation requirements. A spark gap should be placed between the output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration, a 6.4 mm spark gap (5.5 mm maybe acceptable, depending on customer requirements) is sufficient to meet the creepage and clearance requirements of most safety standards applicable to a universal input power supply. For effective ESD immunity, the spark gap spacing should provide the shortest distance between the primary and secondary sections.

Secondary Rectifier Diode
For optimal performance, the loop area connecting the secondary winding, secondary rectifier diode, and output filter capacitor should be minimized. When using SM diodes, ensure sufficient copper area at the terminals of the secondary rectifier diode for heat dissipation. A heatsink will be required for a non-SM secondary diode.

Thermal Protection
The SOURCE pin is internally connected to the IC lead frame and serves as the main path for heat removal in K packages. The SOURCE pin should be connected to a copper area underneath the IC, functioning as both a single-point ground and a heat sink. Since this area is connected to the quiet source node, it can be maximized for effective heat dissipation without causing EMI issues. K packages feature an exposed pad on the bottom of the IC, which should be soldered to the SOURCE connected copper heatsink to further reduce IC temperature.

For E packages, the exposed Source pad on the back of the IC is necessary to ensure that the IC operates safely below the absolute maximum junction temperature limit when connected to an appropriate heatsink.

Sufficient copper area or a heatsink should be provided to maintain the IC temperature below absolute maximum limits. It is recommended that the cooling method be sufficient to keep the IC temperature below 110 °C when operating the power supply at full rated load, the lowest rated input supply voltage, and maximum ambient temperature.

TOPSwitchGaN device is typically the only component that will have over-temperature protection. Designing cooling such that other components in the circuit will have lower temperatures than the TOPSwitchGaN IC will ensure that it protects the whole circuit from thermal damage in the event that excess ambient temperatures are encountered. This will ensure that the TOPSwitchGaN part will protect the other devices when ambient temperature increases.

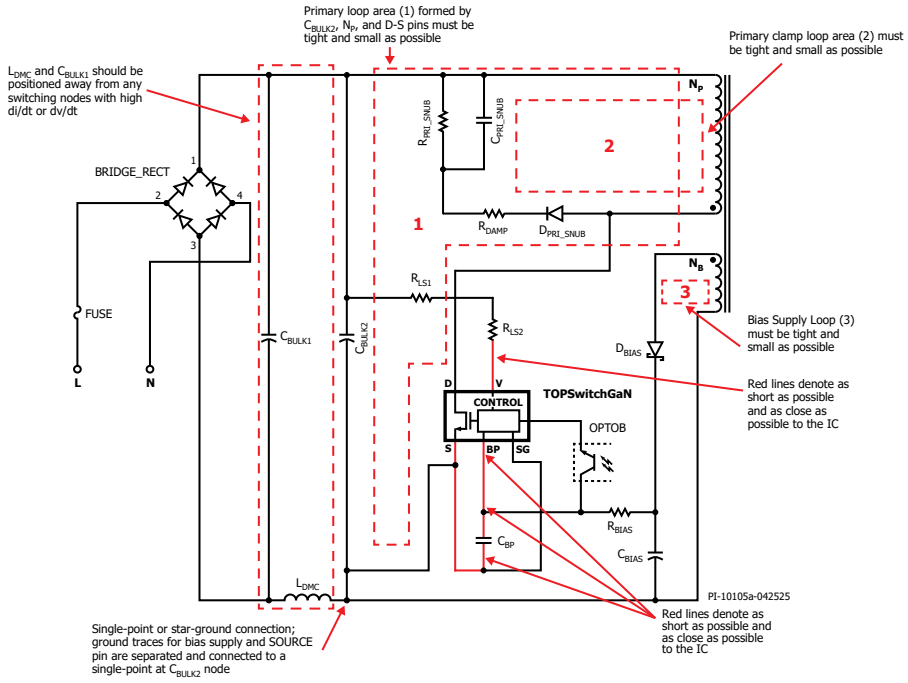


Figure 18. Typical Schematic of TOPSwitchGaN Primary-Side Showing Critical Loops Areas, Critical Component Traces, and Single-Point or Star Grounding.

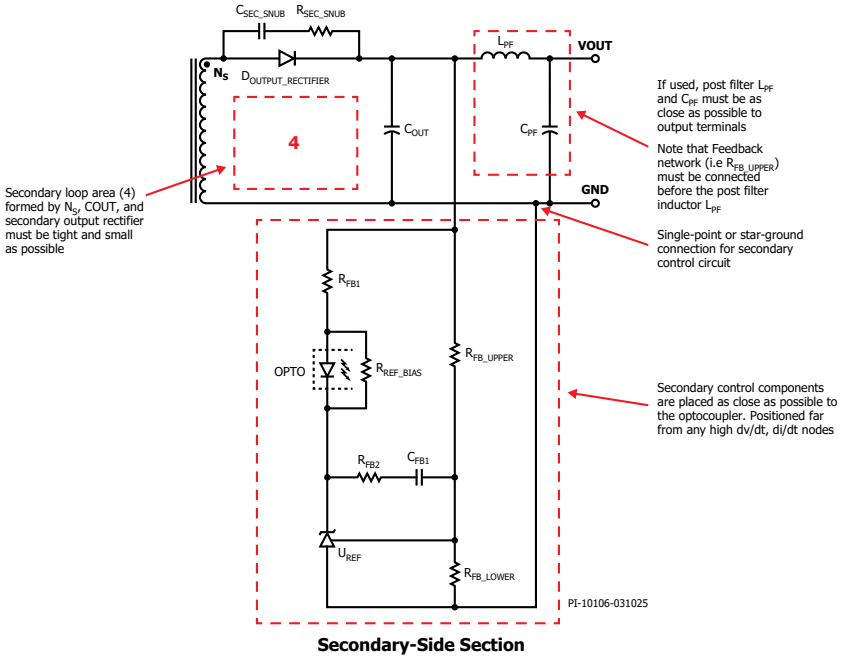


Figure 19. Typical Schematic of TOPSwitchGaN Secondary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding. Optional LC Post Filter Included.

Layout Example for TOPSwitchGaN E-package

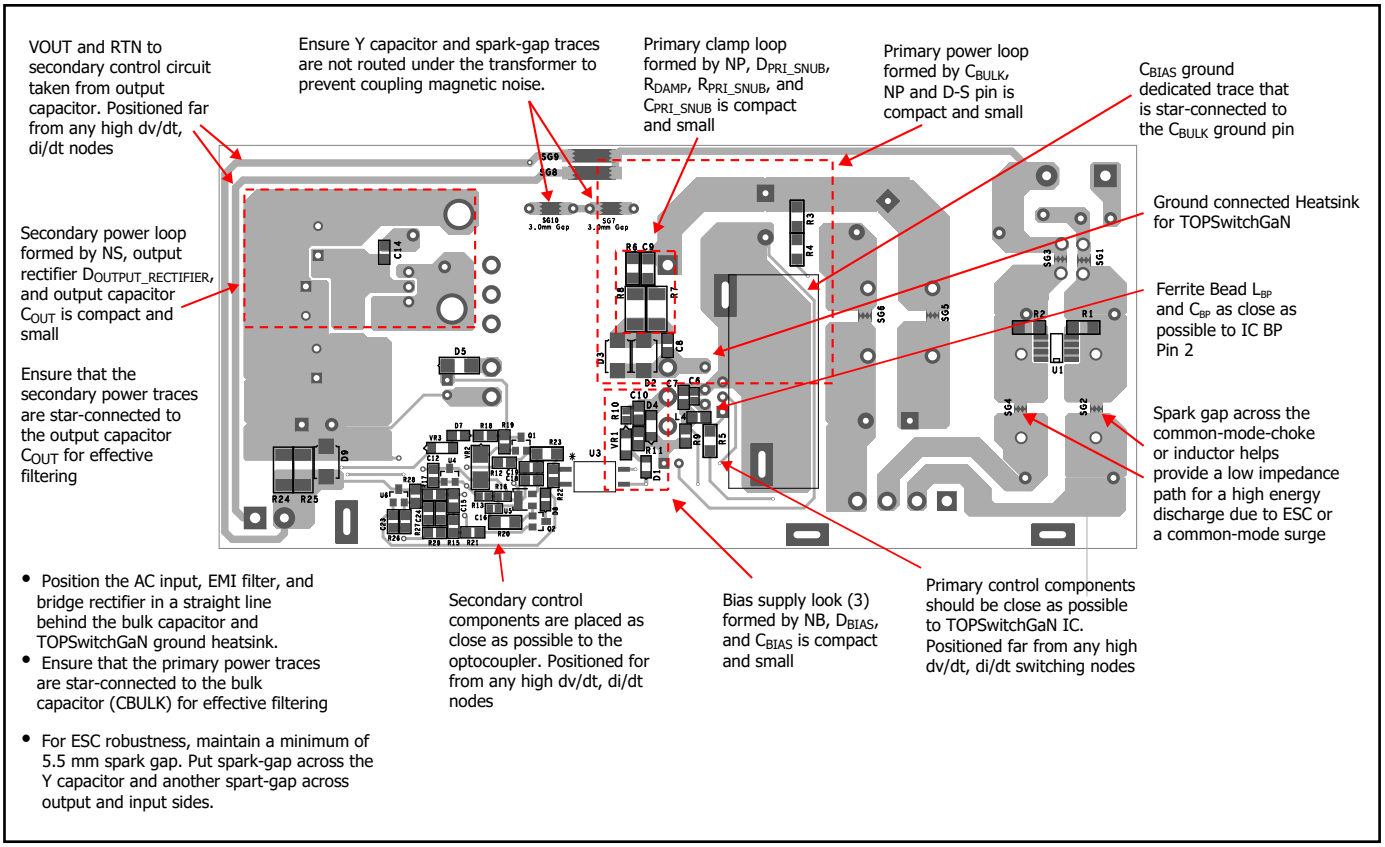


Figure 20. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TOPSwitchGaN E-package and K-package.

Layout Example for TOPSwitchGaN K-package

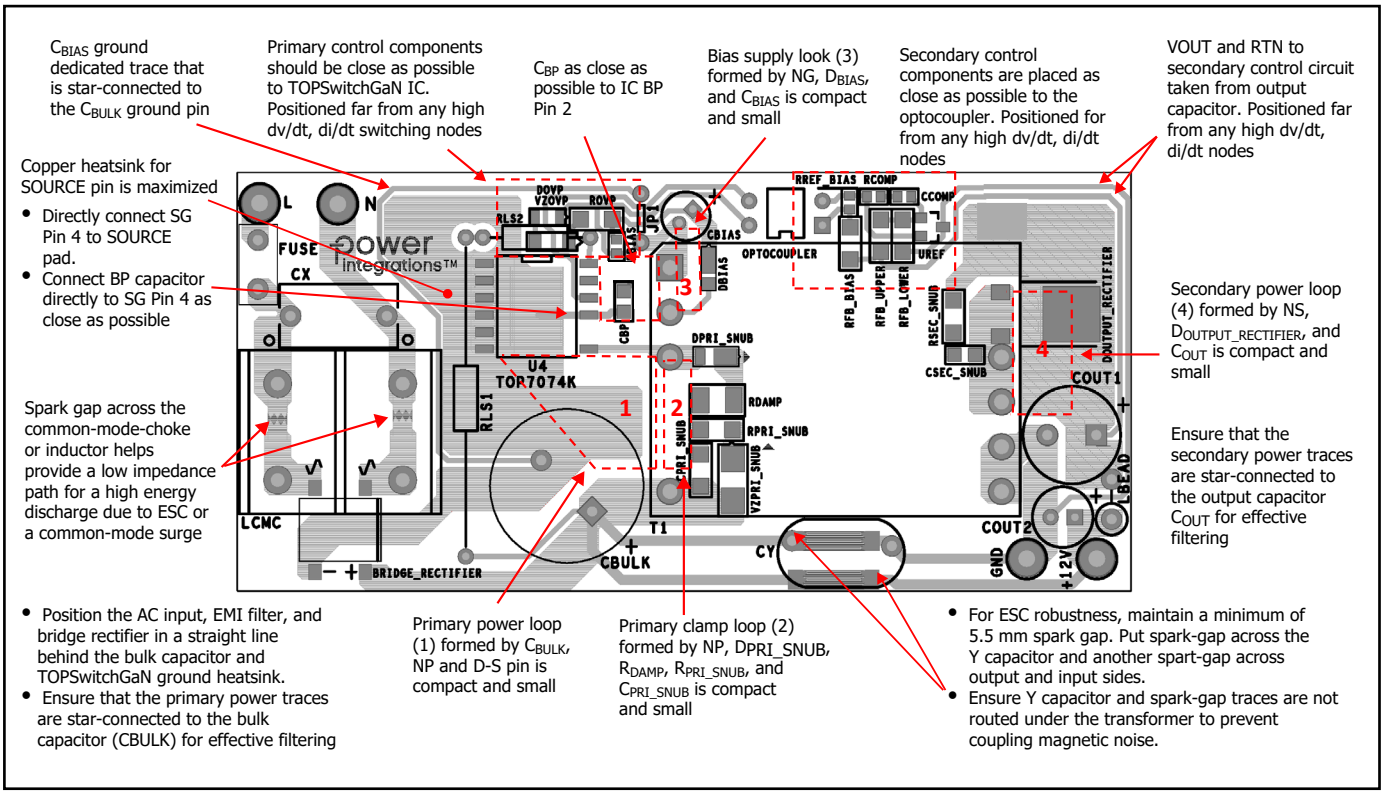


Figure 21. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TOPSwitchGaN E-package and K-package.

Special notes:

- All loops are separated; no loop is inside a loop. This will avoid ground impedance noise coupling.
- Keep trace surface area and length of high dv/dt nodes such as Drain, as small and short as possible to minimize RFI generation.
- No (quiet) signal trace such as Y capacitor and feedback return should be routed near to or across noisy nodes (high dv/dt or high di/dt) such as Drain, underneath transformer belly, switching-side of any winding or output rectifier diode. This avoids capacitive or magnetic noise coupling.
- No signal trace should share a path with traces having an AC switching current such as output capacitors. Connection must be star-connected to the capacitor pad in order to avoid ground impedance coupled noise.

Quick Design Checklist

As with any power supply, the operation of all TOPSwitchGaN part based designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage

Verify that V_{DS} of the TOPSwitchGaN IC and reverse voltage of the secondary rectifier diode do not exceed 90% of their respective breakdown voltages at the highest input voltage and peak (overload) output power in normal operation or during start-up.

Maximum Drain Current

At maximum ambient temperature, maximum input voltage and peak output (overload) power, review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB\ (MIN)}$. Under all conditions, the maximum drain current for the primary GaN should be below the specified absolute maximum rating.

Thermal Check

At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature limits for the TOPSwitchGaN IC, transformer, bridge rectifier, secondary rectifier diode, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation. At low-line, maximum power, a maximum a TOPSwitchGaN IC temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

Design Support

Up-to-date information on design support can be found at the Power Integrations website: www.power.com

Application Examples

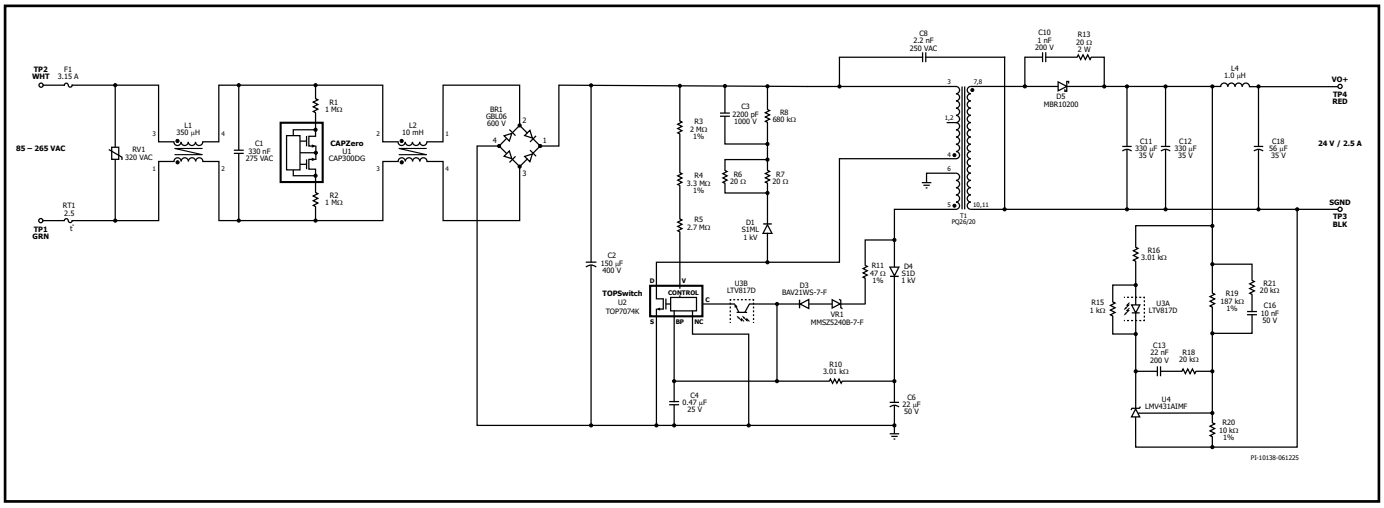


Figure 22. Schematic of DER-1079 50 W, 24 V Power Supply using TOP7074K.

A High-Efficiency, 50 W Output Power Supply (TOPSwitchGaN device)

The circuit shown in Figure 22 is a 50 W output high-efficiency flyback power supply designed for 24 V, 2.5 A output from universal input using the TOP7074K.

The supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage auto-restart protection, output short-circuit protection, high full load efficiency (>90%), high average efficiency (>90%) and low no-load input power consumption (<80 mW at 230 VAC). Output regulation is accomplished using an optocoupler and a shunt regulator (LMV431) .

Fuse F1 isolates the circuit and provides protection from component failure. Common mode choke L1 and L2 with X capacitor C1 attenuate EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C2. Capacitor C8 is used to mitigate common mode EMI. Additionally, TOPSwitchGaN IC frequency jitter improves EMI performance.

The bleed resistors, R1 and R2 together with a CAPZero™ IC are used to discharge the stored energy in the input X capacitor C1 to meet safety discharge requirements.

Line undervoltage and overvoltage is determined by the current supplied to the V pin by resistors R3, R4 and R5.

The input capacitor C2 is sufficient to maintain full output power delivery at 85 VAC input. The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated PowiGaN switch in U2. A RCD clamp formed by D1, R6, R7, R8, and C3 limits the peak drain voltage, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value.

As the TOPSwitchGaN devices are completely self-powered, there is no mandatory requirement for an auxiliary or bias winding on the transformer. However, by adding a bias winding, TOPSwitchGaN IC power consumption will be significantly reduced. Resistor R10 feeds current into the BP pin, inhibiting the internal high-voltage current source that would otherwise maintain the BP pin capacitor (C4) voltage during the internal GaN switch off-time. This reduces no-load consumption <80 mW at 230 VAC.

Output overvoltage protection (resistor R11, Zener VR1, and blocking diode D3) of the load against open loop faults is achieved using the bias circuit. When an overvoltage condition occurs, the bias voltage exceeds the sum of Zener VR1, D3, R11 and the BP pin voltage, current begins to flow into the BP pin. When this current exceeds I_{SD}, TOPSwitchGaN IC will stop switching. Auto-restart will occur and continue until the output returns to regulation.

Schottky diode D5 rectifies the 24 V output from the transformer (T1). Resistor R13 and capacitor C10 snub the voltage spike caused by the commutation of D5. The output voltage is filtered by C11, C12, L4, and C18. Low ESR capacitors C11 and C12 minimize output voltage ripple, while the post filter, L3 and C14, further attenuates noise and ripple.

The output voltage is sensed via resistor divider R19 and R20. Output voltage is adjusted to achieve a voltage of 1.24 V on the LMV431 REF pin. As the cathode voltage changes, the current through the optocoupler LED and transistor within U2 changes. R16, R18, R21, C13 and C16 maintain stable operation while resistor R15 ensures minimum bias to U4.

Output regulation is achieved by modulation of off-time (switching frequency) and primary ILIM which are adjusted according to the input from U4 as output load changes. At high load, low switch off-time ensures high switching frequency while higher ILIM increases the amount of energy transferred per cycle. As load is reduced, off time increases reducing switching frequency and ILIM - allowing shorter on time and less energy transfer per switch cycle.

Application Examples

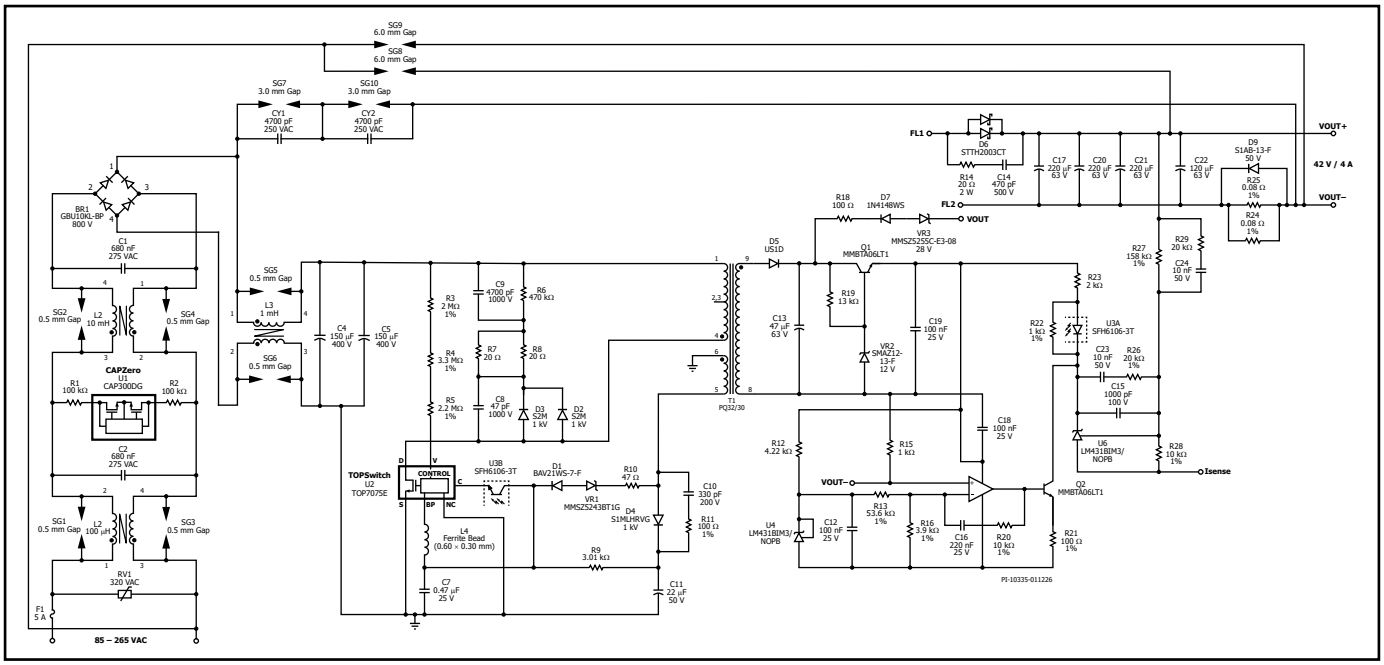


Figure 23. Schematic of DER-1081 168 W, 42 V Power Supply using TOP7075E.

High-Efficiency, 168 W Output Power Supply (TOPSwitchGaN device, E-package)

The circuit shown in Figure 23 is a 168 W output high-efficiency flyback power supply designed for 42 V, 4.0 A output from universal input using the TOP7075E.

The supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage auto-restart protection, output short-circuit protection, high full load efficiency (>90%), high average efficiency (>90%) and low no-load input power consumption (<80 mW at 230 VAC). Output regulation is accomplished using an optocoupler and a shunt regulator (LMV431) .

Fuse F1 isolates the circuit and provides protection from component failure. Common mode choke L1 and L2 with X capacitor C1 and C2 attenuate EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C3, C4, and C5. Capacitor CY1 and CY2 are used to mitigate common mode EMI. Additionally, TOPSwitchGaN IC frequency jitter improves EMI performance.

The bleed resistors, R1 and R2 together with a CAPZero IC U1 are used to discharge the stored energy in the input X capacitor C1 and C2 to meet safety discharge requirements.

Line undervoltage and overvoltage is determined by the current supplied to the V pin by resistors R3, R4 and R5.

The input capacitors C3, C4, and C5 are sufficient to maintain full output power delivery at 85 VAC input. The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated PowiGaN switch in U2. A RCD clamp formed by D2, D3, R6, R7, R8, C8, and C9 limits the peak drain voltage, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value.

As the TOPSwitchGaN devices are completely self-powered, there is no mandatory requirement for an auxiliary or bias winding on the transformer. However, by adding a bias winding, TOPSwitchGaN IC power consumption will be significantly reduced. Resistor R9 feeds current into the BP pin, inhibiting the internal high-voltage current source that would otherwise maintain the BP pin capacitor (C7) voltage during the internal PowiGaN switch off-time. An optional ferrite bead (L7) was used to increase noise immunity.

Output overvoltage protection (resistor R10, Zener VR1, and blocking diode D1) of the load against open loop faults is achieved using the bias circuit. When an overvoltage condition occurs, the bias voltage exceeds the sum of Zener VR1, D1, R10 and the BP pin voltage, current begins to flow into the BP pin. When this current exceeds I_{SD}, TOPSwitchGaN IC will stop switching. Auto-restart will occur and continue until the output returns to regulation.

Schottky diode D6 rectifies the 42 V output from the transformer (T1). Resistor R14 and capacitor C14 snub the voltage spike caused by the commutation of D5. The output voltage is filtered by C17, C20, C21, and C22. Low ESR capacitors C17, C20, C21 and C22 minimize output voltage ripple.

The output voltage is sensed via resistor divider R27 and R28. Output voltage is adjusted to achieve a voltage of 2.5 V on the LM431 REF pin. As the cathode voltage changes, the current through the optocoupler LED and transistor within U2 changes. R23, R26, R29, C24 and C23 maintain stable operation while resistor R22 ensures minimum bias to U6.

Output regulation is achieved by modulation of off-time (switching frequency) and primary ILIM which are adjusted according to the input from U6 as output load changes. At high load, low switch off-time ensures high switching frequency while higher ILIM increases the amount of energy transferred per cycle. As load is reduced, off time increases reducing switching frequency and ILIM - allowing shorter on time and less energy transfer per switch cycle.

Revision	Notes	Date
A	Initial release.	03/26
B	Change "The resistance of ferrite bead is between 40 ohms to 80 ohms" to "The recommended impedance value for SMD ferrite bead is between 40 Ω to 50 Ω @ 100 MHz with a tolerance of ± 25% and a DC Resistance of < 1 Ω."	04/26

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

https://www.power.com/company/sales/sales-offices