Application Note AN-120
HiperLCS-2 Family

Design Guide

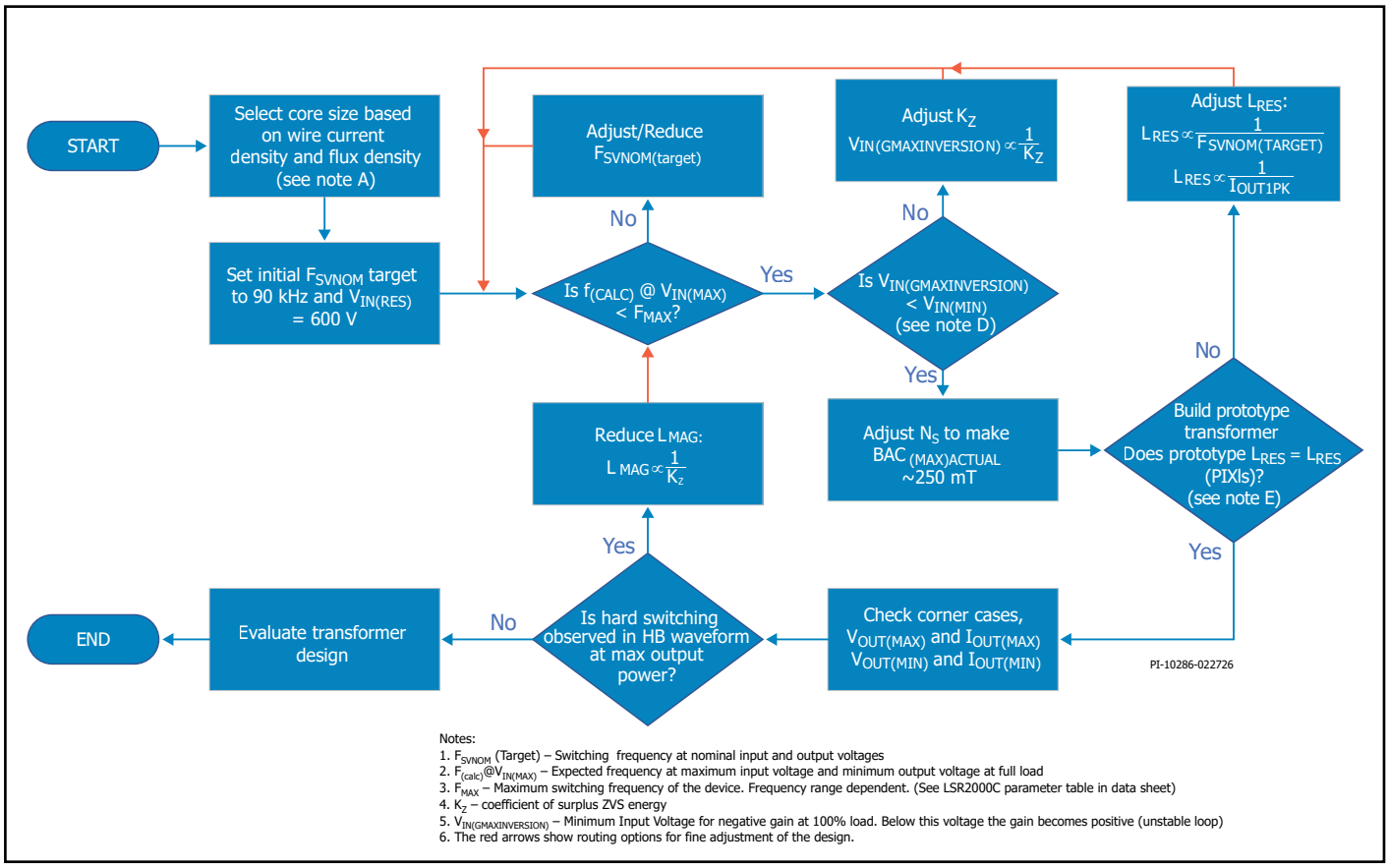
Introduction

This document serves as a practical guide for designers who may have limited experience with LLC resonant converters and/or the HiperLCS™-2 chipset. Given the complexities associated with designing resonant converters, this guide focuses on providing step-by-step design instructions, key considerations, and best practices. The goal is to help users develop efficient and reliable designs that work the first time, minimizing trial and error and reducing development time.

Determine, Input and Output Requirements

For this design example, we will create an LLC power supply for a battery charger with the specifications described below. The circuit will be fed from a boost-PFC front end. Figure 1 shows a flowchart that will guide the use of PI Expert™, the free online tool from Power Integrations.

Nominal Input Voltage: 400 VDC
Input Voltage Range: 350 V to 450 VDC
Output Power: 720 W
Output Voltage Range: 26 VDC to 60 VDC
Variable CC: Yes
Output Load: 4 A to 12 A



Notes:
1. F_{SVNOM} (Target) – Switching frequency at nominal input and output voltages
2. $F_{(calc)}@V_{IN(MAX)}$ – Expected frequency at maximum input voltage and minimum output voltage at full load
3. F_{MAX} – Maximum switching frequency of the device. Frequency range dependent. (See LSR2000C parameter table in data sheet)
4. K_Z – coefficient of surplus ZVS energy
5. $V_{IN(GMAXINVERSION)}$ – Minimum Input Voltage for negative gain at 100% load. Below this voltage the gain becomes positive (unstable loop)
6. The red arrows show routing options for fine adjustment of the design.

Figure 1. Flow Chart for Implementing a CV/CC Design with the HiperLCS-2 Chipset.

HiperLCS-2 Design Notes

Note A. Selecting Core Size and Wire Gauge
Generally, it is advisable to use cores with long center legs such as ETD, EFD, PQ, and EEL. This will provide room for separating primary and secondary windings in order to generate suitable leakage inductance to set Fs.

Commonly used core geometries for different power levels.

100 W: EFD30
200 W: ETD34, POT3319, PQ3230
400 W: ETD39, PQ3230, POT4020
720 W: PQ3535
1.4 kW: ETD49, PQ40 or PQ50

Best transformer efficiency is a balance between core and copper losses. For best efficiency, select number of turns such that flux density is approximately 250 mT.

Choose wire gauge and number of strands such that current density is in the range of 6-8 A / mm^2.

If resultant wire volume is too big for the winding space, move to a larger core size.

Use served Litz wire for primary and unserved Litz wire for secondary.

Current density and flux density will determine whether the correct core size has been selected for the design.

Use the equation below to calculate K_{CORE} factor. The calculated value will typically be in the range of 0.8 to 1. The practical limits for core factor are 0.5 to 1.5. The designer should proceed with caution when design choices result in values that exceed these limits.

$$K_{CORE} = \frac{P_{OUT}}{A_E A_W B_W}$$

Where,

K_{CORE} : Arbitrary number used to estimate power handling capability of a certain core geometry
P_{OUT} : Output power (mW)
A_E : Core cross section area in mm^2
A_W : Core winding window area in mm^2
B_W : Bobbin winding width in mm

Guidelines

K_{CORE} ~ 0.8 to 1: Chosen core approaches nominal size

K_{CORE} <0.5: Core may be too big for the power level, consider choosing smaller core if other parameters permit

K_{CORE} > 1.5: Core may be too small for the power level, check if temperature is acceptable

AWG# 40-44 is recommended for high frequency designs (180 to 240 kHz)

AWG# 38-40 is recommended for low frequency designs (90 to 120 kHz)

In choosing Litz wire, consider bundle-level skin effects, where the high frequency current will only flow through the strands of the outer layer. The equations below determines the practical limit on the number of strands for a given design.

$$\eta_{1MAX} = 4\frac{\alpha^2}{d_S^2}$$

$$\alpha = \sqrt{\frac{\rho}{\pi f \mu_0}}$$

Where,

η_{1MAX} : Maximum number of strands to be twisted in a bundle
d_S : Diameter of an individual strand
f : Switching frequency
ρ : Resistivity of conductor (1.72×10^{-8} Ω-m for copper at 60 ºC)
μ_0 : Permeability of free space (4×10^{-7} π H/m)

Example: In a design where the switching frequency is 250 kHz and AWG#42 wire strands (diameter of a single strand is .064 mm) is initially selected, the equation gives η_{1MAX} = 34 strands. This means that 750 strands of AWG#42, would be grouped into 5 sub-bundles of wire with 30 strands each, which would themselves be combined into 5 bundles to implement a design which avoids significant skin-effect.

Note B. Additional General Notes
The LSR2000C-H005 IC is a frequency range 3 device and is the recommended device for CV/CC applications because its wide frequency range will accommodate the wide output voltage variation expected with CC operation. Frequency range 3 is optimized for wide range LLC operation from 60 kHz to 366 kHz.

Select CC operation in PIXIs, $F_{SVNOM(TARGET)}$ and provide the minimum output voltage. Check that $F_{(CALC@VINMAX)}$ is less than F_{MAX} which is 366 kHz.

Use 120% of the maximum specified continuous output current as the peak current value to ensure suitable margin.

Note C. PFC Input for Variable CC and Variable CV Designs
Choose resonant voltage to be ~1.5x the nominal input voltage to the LLC. This is recommended for typical charger applications where $V_{OUT(MAX)}$ is approximately twice $V_{OUT(MIN)}$. This value places the resonance midway between $V_{OUT(MAX)}$ and $V_{OUT(MIN)}$.

The minimum bulk voltage will be highly dependent on the bulk capacitance. The valley of the minimum input voltage across the bulk capacitor during full power, should be higher than the gain inversion voltage.

Frequency range 3 is strongly recommended for this application since both output voltage and output current are variable. The LSR2000C-H005 IC has a reduced burst threshold to prevent this mode of operation at very low output voltage and current. This will allow the design to meet ripple current requirements.

Choose $F_{SVNOM(Target)}$ such that $F_{(CALC@VINMAX)}$ is approximately 250 kHz to provide margin when operating at the lowest CC and CV setting. Switching frequency can go beyond 250 kHz providing that it remains below F_{MAX} of 366 kHz. It is advisable to confirm operation for corner case conditions ($V_{OUT(MAX)}$ and $I_{OUT(MAX)}$ and $V_{OUT(MIN)}$ and $I_{OUT(MIN)}$).

Suggested L_m/L_r ratio for this application is 1.8 to 2.5.

Note D. Setting Value of K_z
K_z is an arbitrary coefficient describing ZVS energy. Increased K_z means more magnetizing energy (i.e. lower magnetizing inductance)

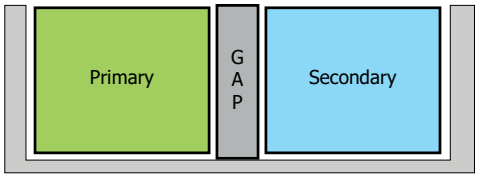
For constant voltage designs the default value of K_z is 2. For CVCC designs, K_z should be close to 1.

Lower K_z may result in hard-switching at high frequencies – usually during $V_{OUT(MIN)}$ and $I_{OUT(MIN)}$, or at no-load, resulting in lower efficiency in these conditions. In contrast at higher output voltages and load currents, frequency is much lower and results in more magnetizing energy for ZVS, resulting in higher efficiency. It is also important to verify that the primary switches are operating in ZVS during full load conditions.

E. Constructing the Transformer

With an integrated LLC transformer design, several design iterations may be required in order for L_{RES} to approach the value described in PIXls. This may require a change in the construction of the transformer.

Check if transformer construction or chamber can be adjusted to modify L_{RES}.



Gap can be achieved through use of a sectional bobbin or with margin tape

Figure 2. Simplified Integrated LLC Transformer Build Diagram.

L_{RES} ∝ gap: Modify the gap if desired change in L_{RES} is less than 10 µH. Increasing the gap between primary and secondary windings increases L_{RES} but reduces the winding window. This may force a move to smaller wires in order to fit the required number of turns into the available space. If a reduction of L_{RES} is needed, it is also possible to eliminate the gap between primary and secondary windings (apart from the thickness of the insulation tape) in single chamber designs. This maximizes window usage efficiency. The example shown in Figure 3 is the cross section of a transformer that does not have any gap aside from the thickness of 3 layers of tape used to isolate the primary and secondary windings from each other.

L_{RES} ∝ N_{PRI}^2: Modify the number of turns if a change of more than 10 µH is required.

The leakage inductance is directly proportional to the square of the number of primary turns. Changing the number of turns will therefore have a significant effect on leakage inductance. Increasing number of turns will necessitate wire size reduction and increase copper loss. Changing the number of turns will also change flux density.

With copper-loss, current density and flux density considered, if the achieved value of L_{RES} is still not equal to that described in PIXls, then modify PIXls to move the calculated value close to the measured L_{RES} value.

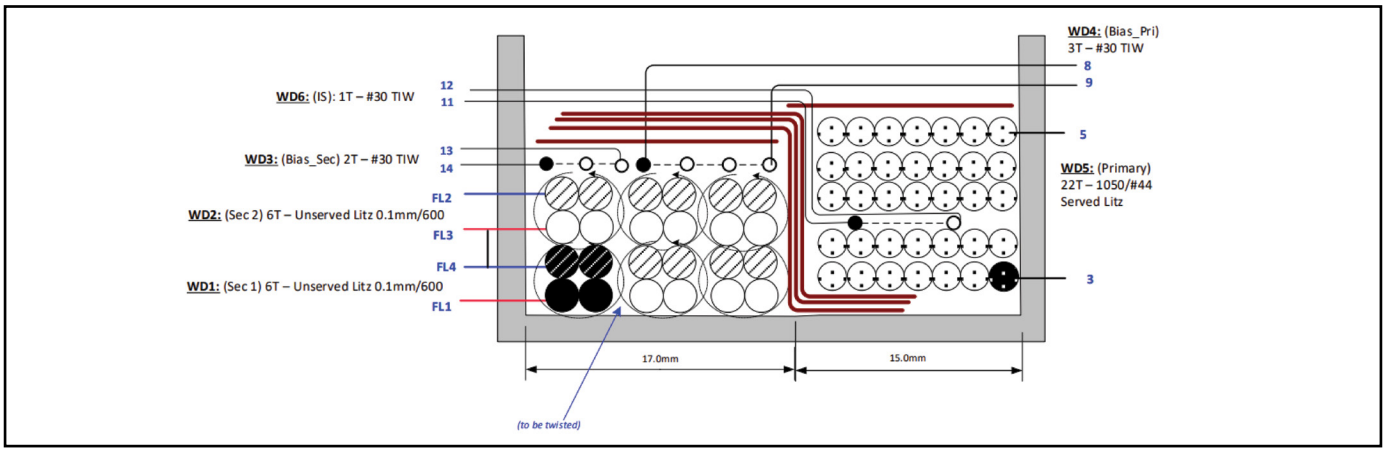


Figure 3. Integrated LLC Transformer Build Diagram.

Hard Switching

Hard switching refers to the event where one of the half-bridge FETs turns on when the voltage is not zero. It can be seen on the half bridge voltage waveform as a change in slew-rate once the half bridge current crosses zero.

This occurs when the tank circuit does not provide sufficient magnetizing current to discharge the C_{OSS} of the switching transistor to 0 V before it turns on.

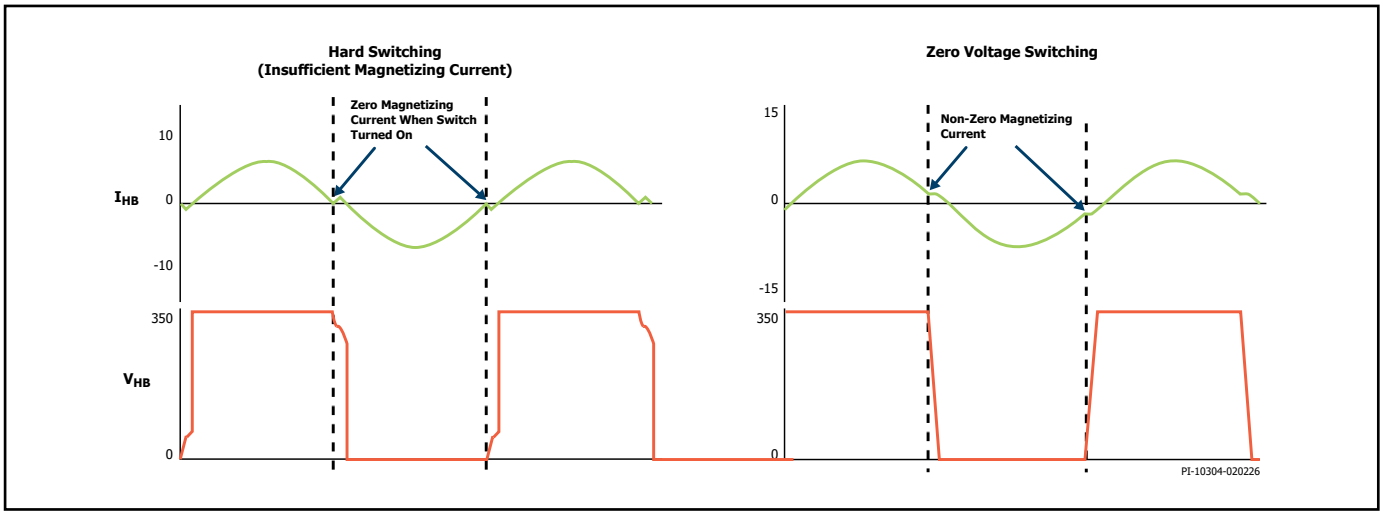
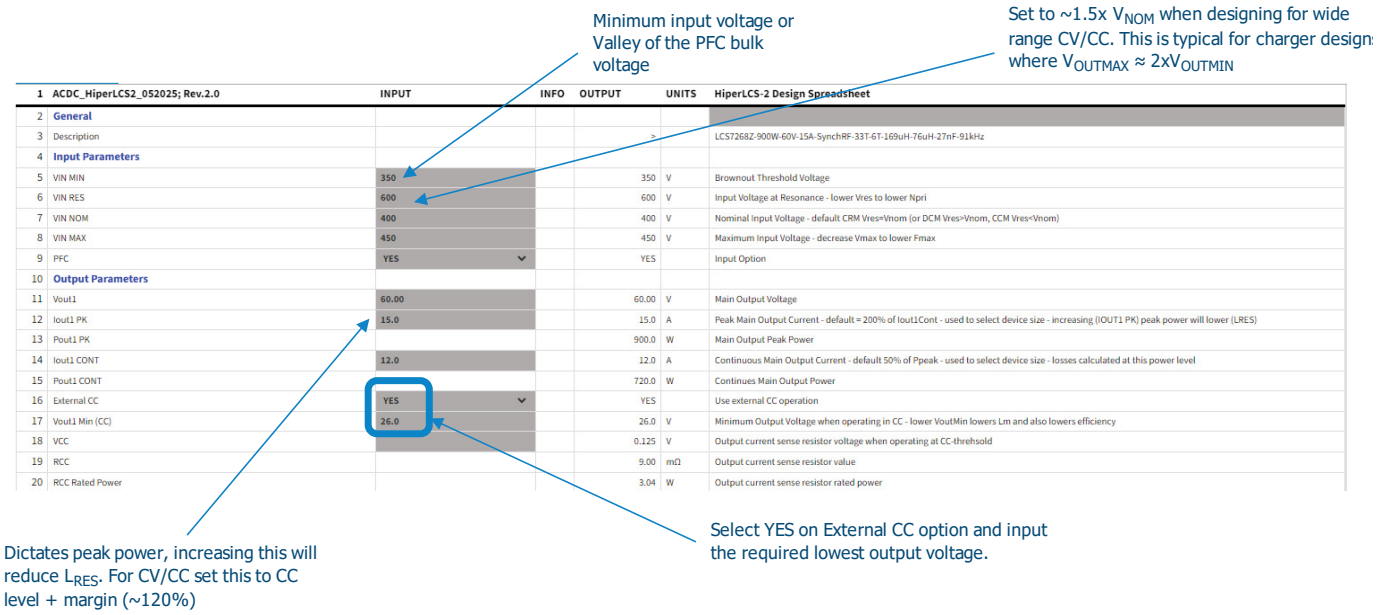


Figure 4. Hard-Switching (left) vs. ZVS (right).

Guide in Using PIXls

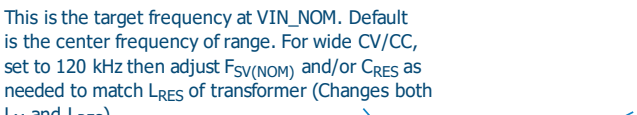
Input and Output Parameters



	1 ACDC_HiperLCS2_052025; Rev.2.0	INPUT	INFO	OUTPUT	UNITS	HiperLCS-2 Design Spreadsheet
2	General					
3	Description			>		LCS7268Z-900W-60V-15A-SynchRF-33T-6T-169uH-76uH-27nF-91kHz
4	Input Parameters					
5	VIN MIN	350		350	V	Brownout Threshold Voltage
6	VIN RES	600		600	V	Input Voltage at Resonance - lower Vres to lower Npri
7	VIN NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	VIN MAX	450		450	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	YES		YES		Input Option
10	Output Parameters					
11	Vout1	60.00		60.00	V	Main Output Voltage
12	Iout1 PK	15.0		15.0	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - increasing (IOUT1 PK) peak power will lower (LRES)
13	Pout1 PK			900.0	W	Main Output Peak Power
14	Iout1 CONT	12.0		12.0	A	Continuous Main Output Current - default 50% of Ppeak - used to select device size - losses calculated at this power level
15	Pout1 CONT			720.0	W	Continues Main Output Power
16	External CC	YES		YES		Use external CC operation
17	Vout1 Min (CC)	26.0		26.0	V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC			0.125	V	Output current sense resistor voltage when operating at CC-threhsold
19	RCC			9.00	mΩ	Output current sense resistor value
20	RCC Rated Power			3.04	W	Output current sense resistor rated power

Figure 5. PIXls Screenshot: Input and Output Parameters.

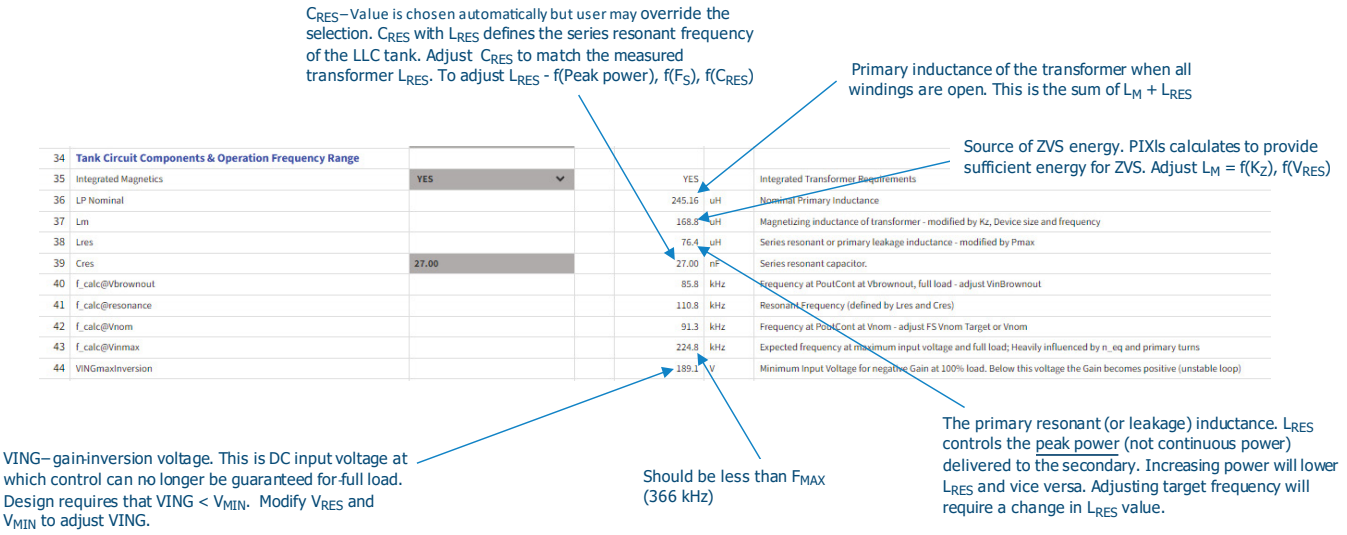
Selecting the Frequency Range



21	Estimated Parameters, Design Choices and Selections					
22	FS Range	3		3		Frequency Range
23	FS Vnom (Target)	111.0		111.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1			5.0	mΩ	Sync. Rectifier ON Resitance
26	VF_SR1				V	Output Diode Average Voltage Drop
27	Design Results					
28	DESIGN RESULT			Design Passed		Current Design Status
29	Device Variables					
30	DEVNAME	LCS7268Z		LCS7268Z		PI Device Name
31	QOSS			302	nC	Equivalent Combined Half-bridge charge (Qoss) at 480V
32	RDSON			0.260	Ω	RDSON of selected device
33	Fault Responce	NON_LATCHING		NON_LATCHING		..

Figure 6. PIXls Screenshot: Frequency Range Selection.

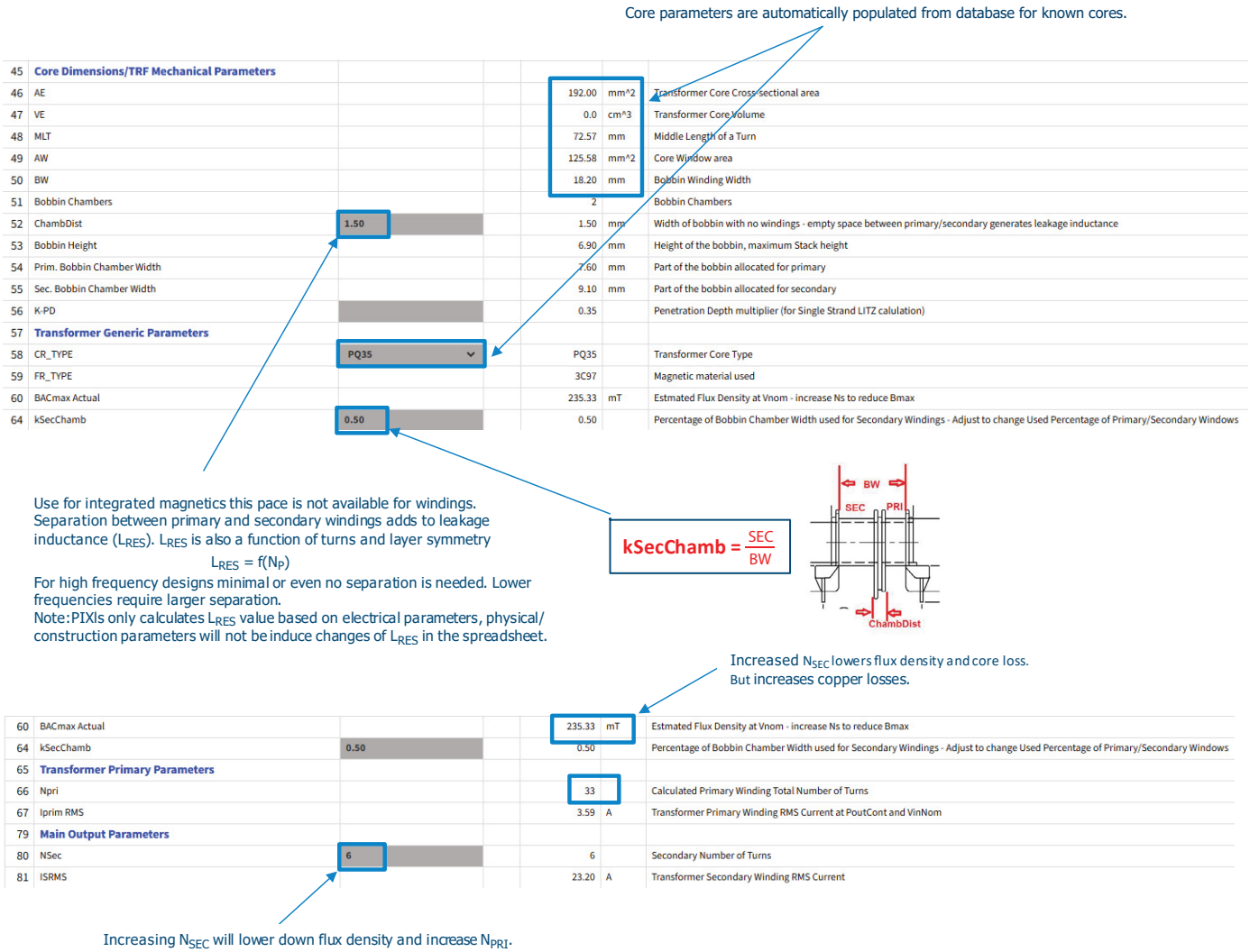
Tank Parameters



34	**Tank Circuit Components & Operation Frequency Range**				
35	Integrated Magnetics	YES	YES		Integrated Transformer Requirements
36	LP Nominal		245.16	uH	Nominal Primary Inductance
37	Lm		168.8	uH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
38	Lres		76.4	uH	Series resonant or primary leakage inductance - modified by Pmax
39	Cres	27.00	27.00	nF	Series resonant capacitor.
40	f_calc@Vbrownout		85.8	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
41	f_calc@resonance		110.8	kHz	Resonant Frequency (defined by Lres and Cres)
42	f_calc@Vnom		91.3	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom
43	f_calc@Vinmax		224.8	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
44	VINGmaxInversion		189.1	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain becomes positive (unstable loop)

Figure 7. PIXIs Screenshot: LLC Tank Parameters.

Transformer Design



45	**Core Dimensions/TRF Mechanical Parameters**				
46	AE		192.00	mm^2	Transformer Core Cross-sectional area
47	VE		0.0	cm^3	Transformer Core Volume
48	MLT		72.57	mm	Middle Length of a Turn
49	AW		125.58	mm^2	Core Window area
50	BW		18.20	mm	Bobbin Winding Width
51	Bobbin Chambers		2		Bobbin Chambers
52	ChambDist	1.50	1.50	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
53	Bobbin Height		6.90	mm	Height of the bobbin, maximum Stack height
54	Prim. Bobbin Chamber Width		7.60	mm	Part of the bobbin allocated for primary
55	Sec. Bobbin Chamber Width		9.10	mm	Part of the bobbin allocated for secondary
56	K-PD		0.35		Penetration Depth multiplier (for Single Strand LITZ calulation)
57	**Transformer Generic Parameters**				
58	CR_TYPE	PQ35	PQ35		Transformer Core Type
59	FR_TYPE		3C97		Magnetic material used
60	BACmax Actual		235.33	mT	Estmated Flux Density at Vnom - increase Ns to reduce Bmax
64	kSecChamb	0.50	0.50		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows

60	BACmax Actual		235.33	mT	Estmated Flux Density at Vnom - increase Ns to reduce Bmax
64	kSecChamb	0.50	0.50		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
65	**Transformer Primary Parameters**				
66	Npri		33		Calculated Primary Winding Total Number of Turns
67	Iprim RMS		3.59	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
79	**Main Output Parameters**				
80	NSec	6	6		Secondary Number of Turns
81	ISRMS		23.20	A	Transformer Secondary Winding RMS Current

Figure 8. PIXIs Screenshot: Transformer Design.

Magnetics Designer

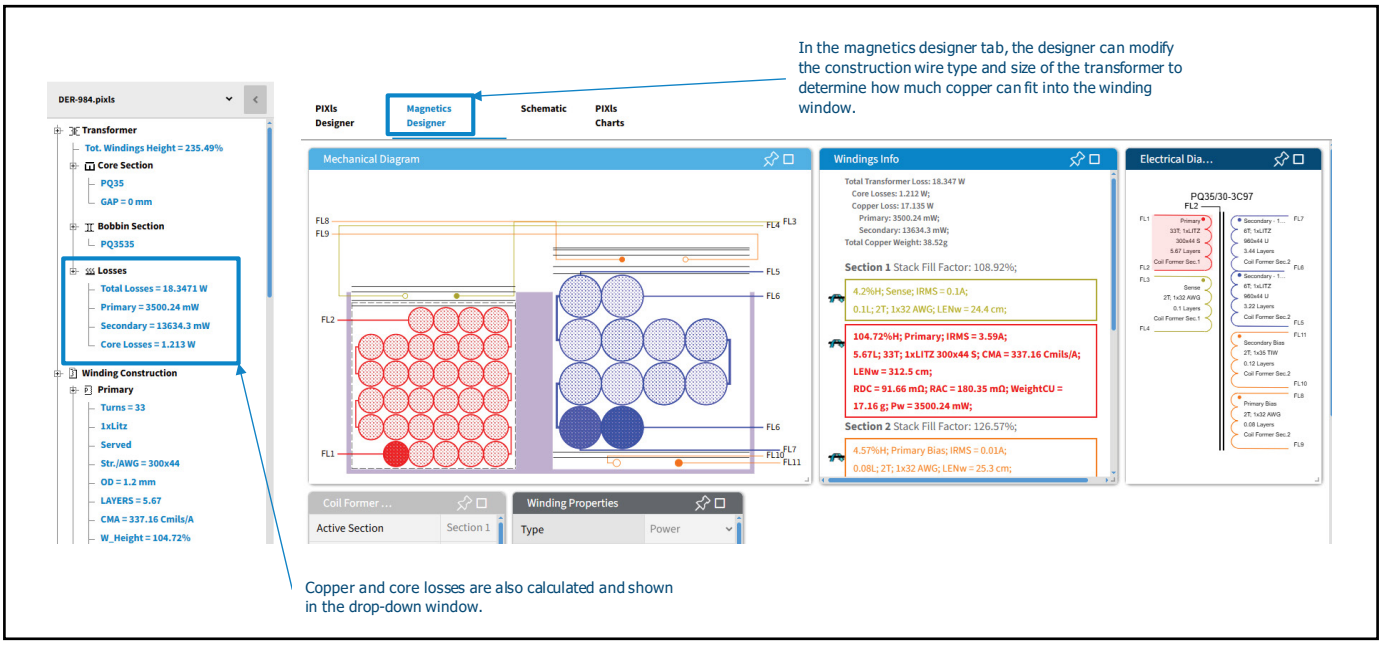


Figure 9. PIXls Screenshot: Magnetics Designer.

Implementation of Variable CV

This section showcases two approaches for dynamically adjusting output voltage - using either variable resistors or an MCU based approach.

Variable CV using Variable Resistor

R60, R64 and R62 form a resistance ladder that senses the output voltage, and applies it the no-inverting input of an amplifier. Gain is set by R57 and R66. The output of the amplifier stage is applied to the FB pin of the HiperLCS2-HB IC. R65 limits the current into the FB pin. Biasing is adjusted such that as R64 is varied, the output voltage of the charger will change to keep the FB pin voltage at 3.75 VDC.

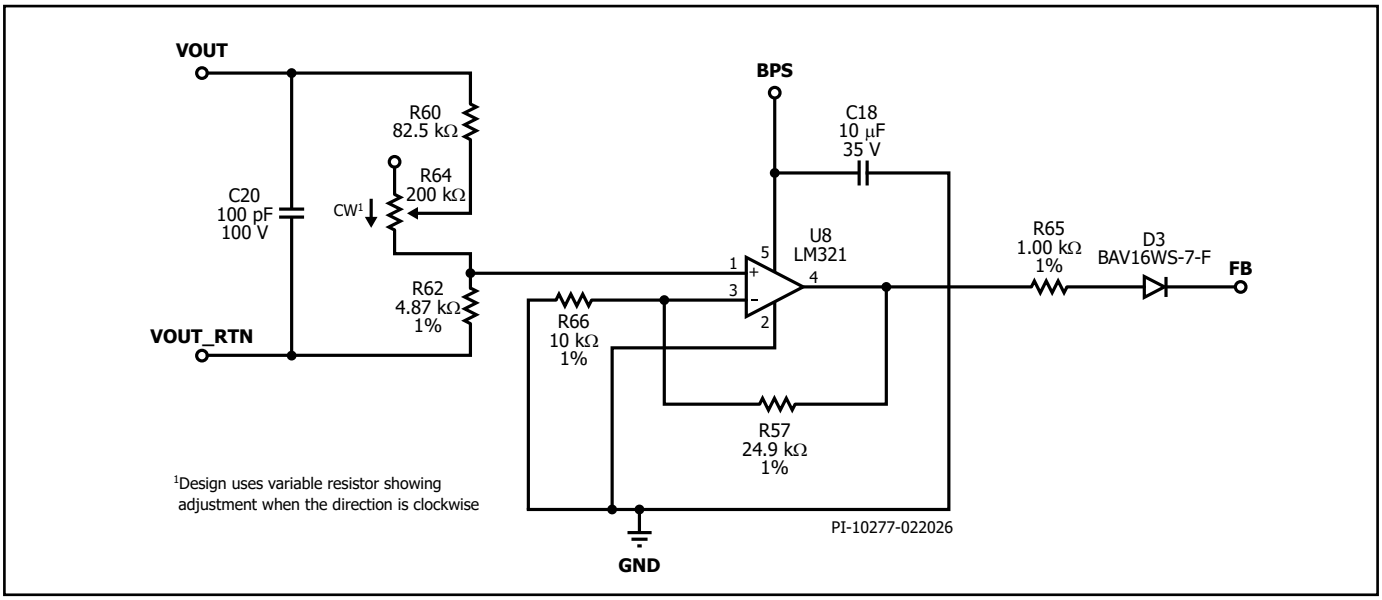


Figure 10. External Variable CV Control Circuit using Variable Resistors.

Variable CV Using MCU/CAN

In EV charging applications typically an output relay is positioned between the charger and the load. In order to minimize inrush current, the controller instructs the charger to set its output voltage close to that of the battery string before the load is connected. The output voltage of the power supply is measured via the potential divider formed by R80 and R81, and is applied the ADC of the MCU. The MCU will then produce a PWM signal "MCU_VPWM" that will be filtered by a 2 stage RC filter (R45-C55 and R87-C60) which converts the PWM signal into a DC voltage. This method of creating a reference voltage is popular as it avoids the need for an expensive DAC. Fast dynamic response of the reference signal is not required in charger applications since there are no CV or CC changes. The filtered PWM signal is then applied to the amplifier with gain set by R70 and R69. The output of the amplifier directly biases the FB pin of the HiperLCS2-SR IC. This approach allows the MCU to directly control the output voltage.

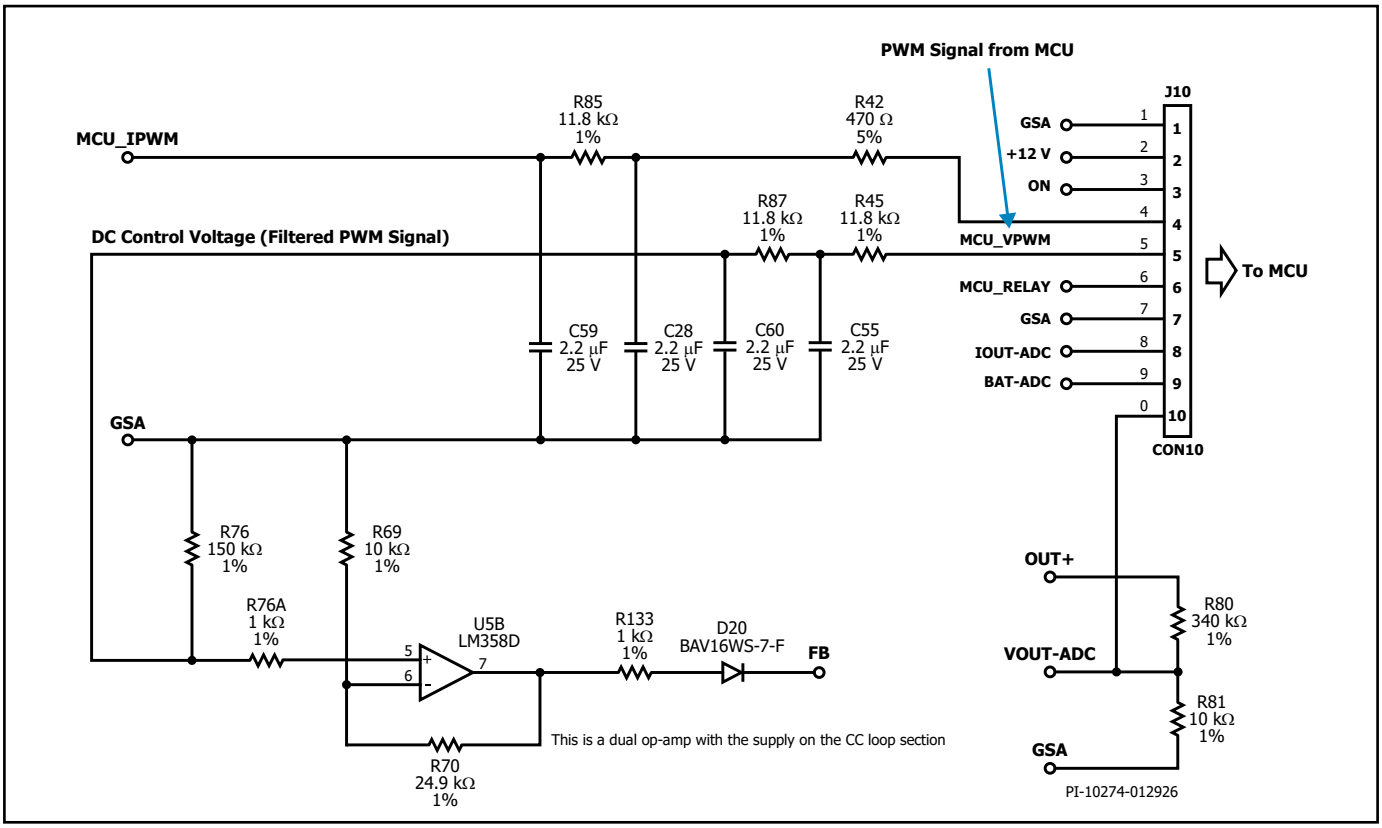


Figure 11. External Variable CV Control Circuit using PWM from MCU.

Implementation of Variable CC

Designers may opt to change charging current based on battery type and charge state. This can be implemented as either a continuous range or via discrete steps. Similar to variable CV, there are two approaches to showcase variable CC operation-on-board variable resistors or via an MCU.

Adjust CC using Variable Resistors

In Figure 12 the voltage developed across the current sense resistors is amplified by U7 before being fed into a non-inverting error amplifier U5A. A reference voltage for the error amplifier is obtained from U4, a 2.5 V reference. To adjust CC, R64 and R152 for a voltage divider which is applied to the error amplifier. R151 and C39 provide a zero that provides phase boost to increase phase margin. R147 and C114 provide low pass filtering at the output of the error amplifier. The output of the amplifier U5A will provide an error signal to the FB pin. In response to this bias signal, the controller in the LSR2000C IC will adjust the output current of the LLC to regulate the FB voltage to 3.75 V.

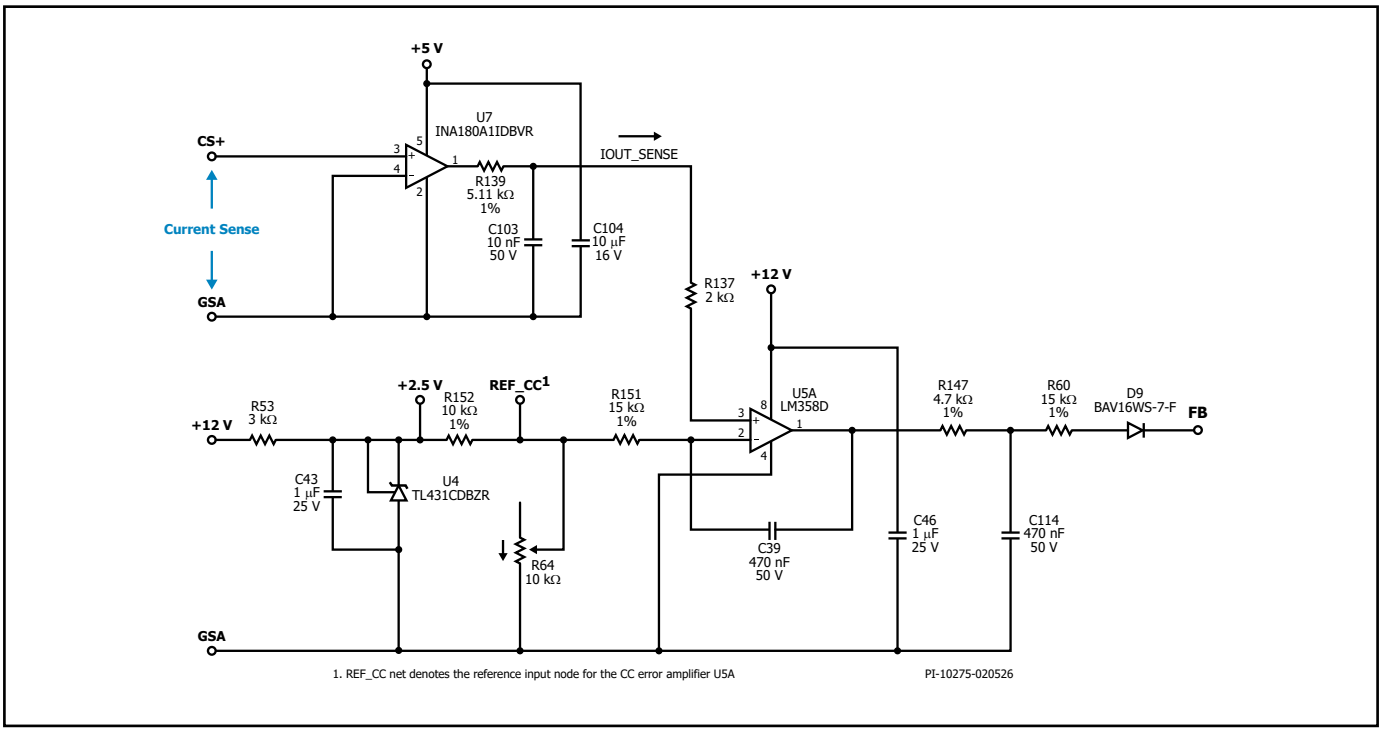


Figure 12. External Variable CC Control Circuit using Variable Resistors.

Variable CC Using MCU/CAN

Figure 13 shows a circuit for providing dynamic adjustment of output current via an MCU. The output of the current sense amplifier is fed into both the error amplifier and to the ADC of the MCU. The MCU determines the output current via the output of the current sense amplifier and generates a corresponding PWM signal depending on the state of charge of the battery. The PWM signal passes through a 2-stage low pass RC filter formed by R42, C28, R85 and C59 which converts the PWM to a DC signal.

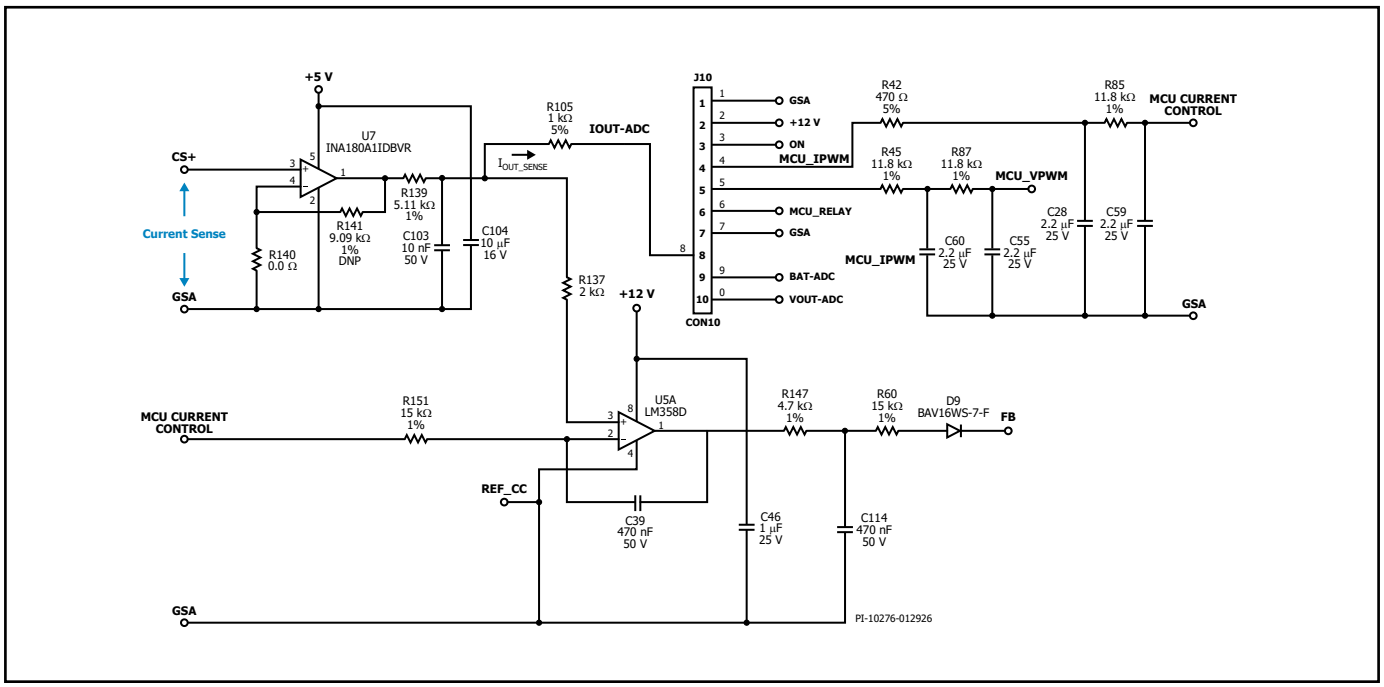


Figure 13. Variable CC Control Circuit using PWM from MCU.

Loop Stability

In order to correctly assign poles and zeros to achieve stable operation it is necessary to derive the transfer function for the power supply and external CV and CC bias circuits if present. This is shown below.

Deriving Plant Transfer Function

The energy delivered per switching cycle can be described by the net charge on the resonant capacitor plus the charge on the C_{OSS} of the 2 MOSFETs of the half-bridge as they are charged and discharged between V_{IN} and 0 V.

Net Charge delivered per cycle:

$$Q_{NET} = C_R \Delta V_{CR} + 2C_J V_{IN} \quad (1)$$

Where,

$\Delta V_{CR} = V_{CR(tHoff)} - V_{CR(tLoff)}$

C_R = Resonant Capacitance

C_J = Junction capacitance of each MOSFET

V_{IN} = Input Voltage

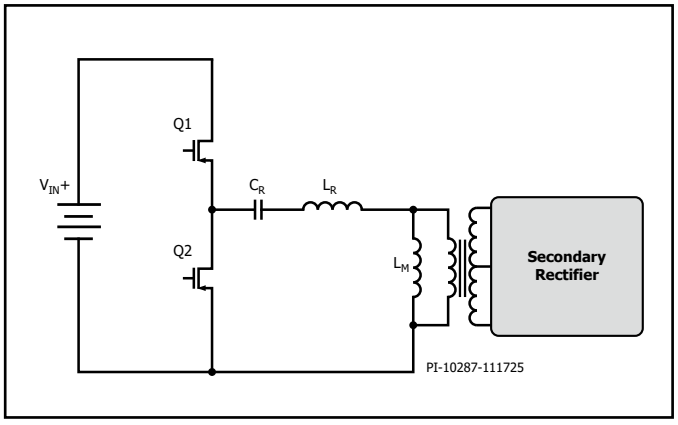


Figure 14. Simplified LLC Circuit.

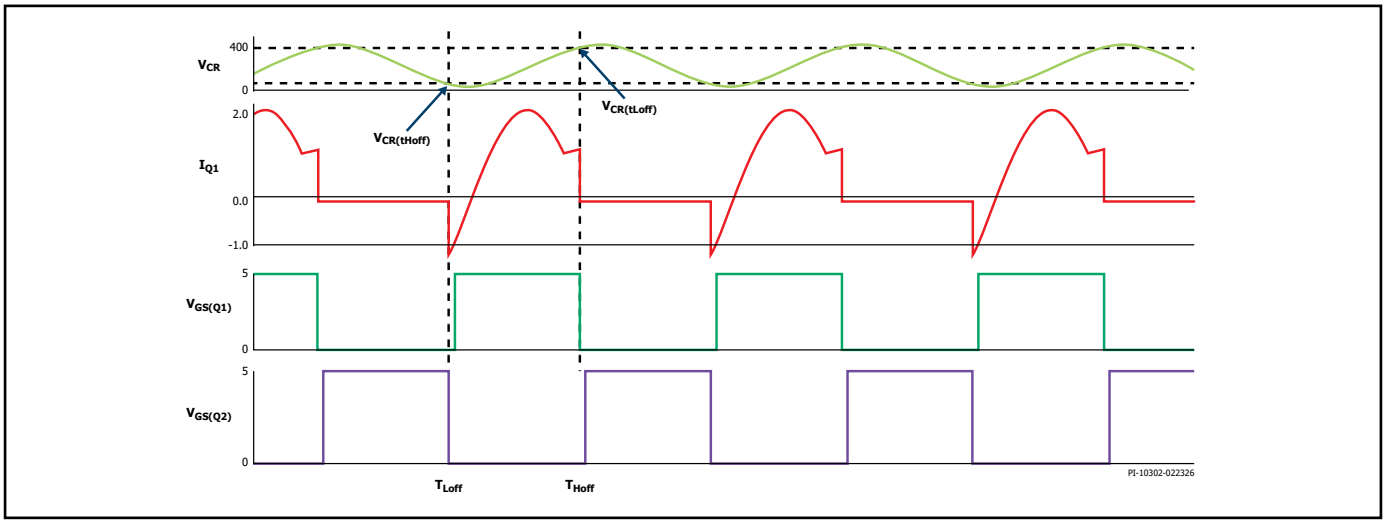


Figure 15. LLC Primary-Side Voltage and Current Waveforms.

From equation 1 we can derive the input power per switching cycle.

$$P_{IN} = V_{IN} f_{SW} C_R \Delta V_{CR} + 2C_J V_{IN}^2 \qquad (2)$$

Since C_R blocks the DC content of the half bridge switching wave, its voltage is symmetrical to one half of the input voltage. Therefore we can say in equation 3 that:

$$V_{CR(tHoff)} + V_{CR(tLoff)} = V_{IN} \qquad (3)$$

$$V_{CR(tLoff)} = V_{IN} - V_{CR(tHoff)}$$

$$\Delta V_{CR} = V_{CR(tHoff)} - (V_{IN} - V_{CR(tHoff)}) \qquad (4)$$

$$\Delta V_{CR} = 2V_{CR(tHoff)} - V_{IN}$$

Since the HiperLCS-2 IC senses the voltage signal from $V_{LR} + V_{LM}$ rather than V_{CR}, we need to derive the relationship between V_{CR} with the combination of V_{LR} and V_{LM}.

In an LLC half bridge resonant converter, at the instant the low side switch is off:

At t = t_{Loff}

$V_{LR} + V_{LM} = V_{IN} - V_{CR(tLoff)}$

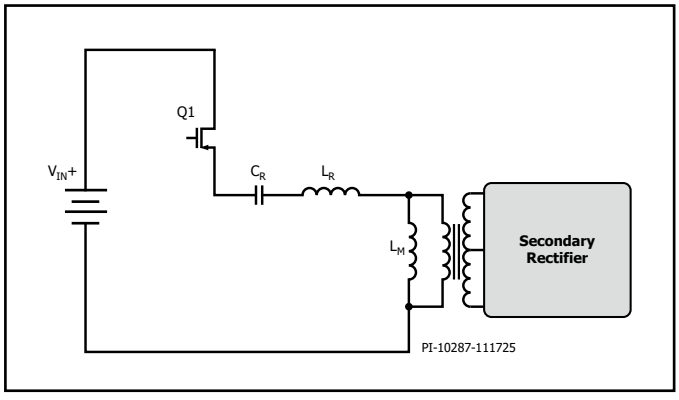


Figure 16. LLC with High-Side FET (Q1) On and Low-Side FET (Q2) Off.

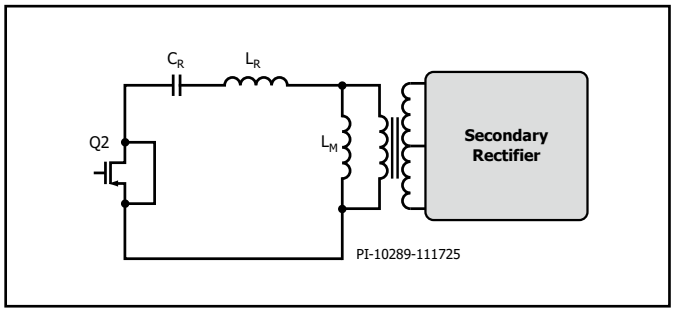


Figure 17. LLC with High-Side FET (Q1) off and Low-Side FET (Q2) on.

At t = t_{Hoff}

$V_{LR} + V_{LM} = -V_{CR(tHoff)}$

$V_{LR} + V_{LM}$ are sensed through an auxiliary winding that is tightly coupled to the primary side winding. This will then be fed to the IS pin of the HiperLCS2-SR IC where it will create an internal sense voltage V_{LL}.

$$V_{LL} = \frac{N_{ISP}(V_{LR} + V_{LM})}{R_{IS}} Z_{IS} + V_{OFFSET} \qquad (5)$$

Where,

$N_{ISP} = N_{IS}/N_P$: is the turns ratio of IS winding to primary winding

R_{IS}: is the IS pin sense resistor

Z_{IS}: Impedance presented by the IS pin (72 kΩ)

Substituting $V_{LR} + V_{LM} = -V_{CR(tHoff)}$

At $t = t_{Hoff}$

$$V_{LL} = \frac{N_{ISP}(-V_{CR(tHoff)})}{R_{IS}} Z_{IS} + V_{OFFSET}$$

$$V_{LL} - V_{OFFSET} = \frac{N_{ISP}(-V_{CR(tHoff)})}{R_{IS}} Z_{IS}$$

$$V_{CR(tHoff)} = \frac{R_{IS}}{N_{ISP} Z_{IS}} (V_{OFFSET} - V_{LL})$$

$$V_{CR(tHoff)} = G_{IS} V_{thH} \quad (6)$$

Where,

$G_{IS} = R_{IS}/(N_{ISP}Z_{IS})$: Sense gain of IS pin signal

$V_{thH} = V_{OFFSET} – V_{LL}$: IS signal high-side off threshold

V_{OFFSET}: Internal comparator offset voltage

Substituting equation 6 into equation 4

$$\Delta V_{CR} = 2G_{IS} V_{thH} – V_{IN}$$

Substituting $\Delta V_{CR} = 2G_{IS} V_{thH} – V_{IN}$ into P_{IN}

$$P_{IN} = V_{IN} f_{SW} C_R (2G_{IS} V_{thH} - V_{IN}) + 2C_J V_{IN}^2$$

The equation is linearized around the operating point by keeping the term proportional to a small change in V_{thH}.

The derivative of P_{IN} with respect to V_{thH} is:

$$\frac{dP_{IN}}{dV_{thH}} = V_{IN} f_{SW} C_R 2G_{IS}$$

Therefore, the small-signal variation in input power is:

$$P_{IN}(s) = V_{IN} f_{SW} C_R 2G_{IS} V_{thH}(s)$$

Calculating P_{OUT} in terms of V_{OUT} and output impedance:

$$P_{OUT} = \frac{V_O^2}{Z_L}$$

The derivative of P_{OUT} with respect to V_O is

$$\frac{dP_{OUT}}{dV_O} = \frac{2V_O}{Z_L}$$

Therefore, the small-signal variation in output power is:

$$P_{OUT}(s) = \frac{2V_O}{Z_L} V_O(s)$$

Assuming that power supply losses are negligible

$$P_{IN}(s) = P_{OUT}(s)$$

$$V_{IN} f_{SW} C_R 2G_{IS} V_{thH}(s) = \frac{2V_O}{Z_L} V_O(s)$$

$$\frac{V_O(s)}{V_{thH}(s)} = \frac{V_{IN} f_{SW} C_R 2G_{IS} Z_L}{2V_O}$$

$$\frac{V_O(s)}{V_{thH}(s)} = \frac{V_{IN} f_{SW} C_R G_{IS} Z_L}{V_O}$$

Where Z_L is the output impedance which is the combination of output capacitance and load.

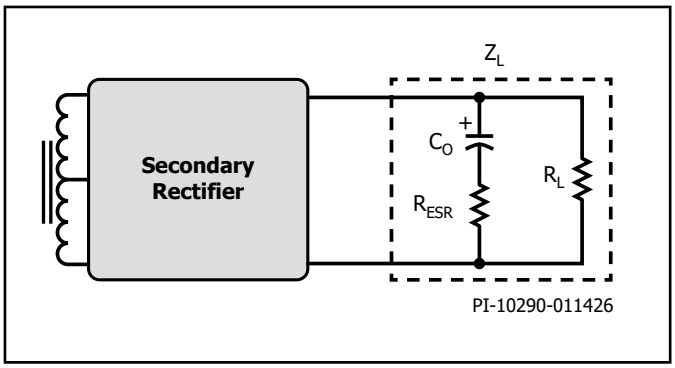


Figure 18. Circuit Diagram of Effective Output Impedance.

$$Z_L = \frac{R_L(1 + sR_{ESR}C_O)}{1 + sC_O(R_L + R_{ESR})}$$

Substituting Z_L into the equation gives us the

$$\frac{V_O(s)}{V_{thH}(s)} = \frac{V_{IN} f_{SW} C_R G_{IS} R_L (1 + sR_{ESR} C_O)}{V_O (1 + s(R_L + R_{ESR}) C_O)} = G(s) \quad (7)$$

Equation 7 shows that the plant has a single pole and a single zero. The locations of the pole and zero can be calculated below:

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (8)$$

$$f_P = \frac{1}{2\pi \times (R_L + R_{ESR}) \times C_O} \approx \frac{1}{2\pi \times R_L \times C_O} \quad (9)$$

we can disregard R_{ESR} because it is << R_L

Plotting the derived equations using C_O = 780 µF, R_{ESR} = 19 mΩ and R_L = 5 Ω, the corresponding ploe and zero locations can be determined. From equations (8) and (9), we can get f_Z = 10.7 kHz f_P = 40.8 Hz.

Figure 19 shows the locations of the pole and zero for the plant.

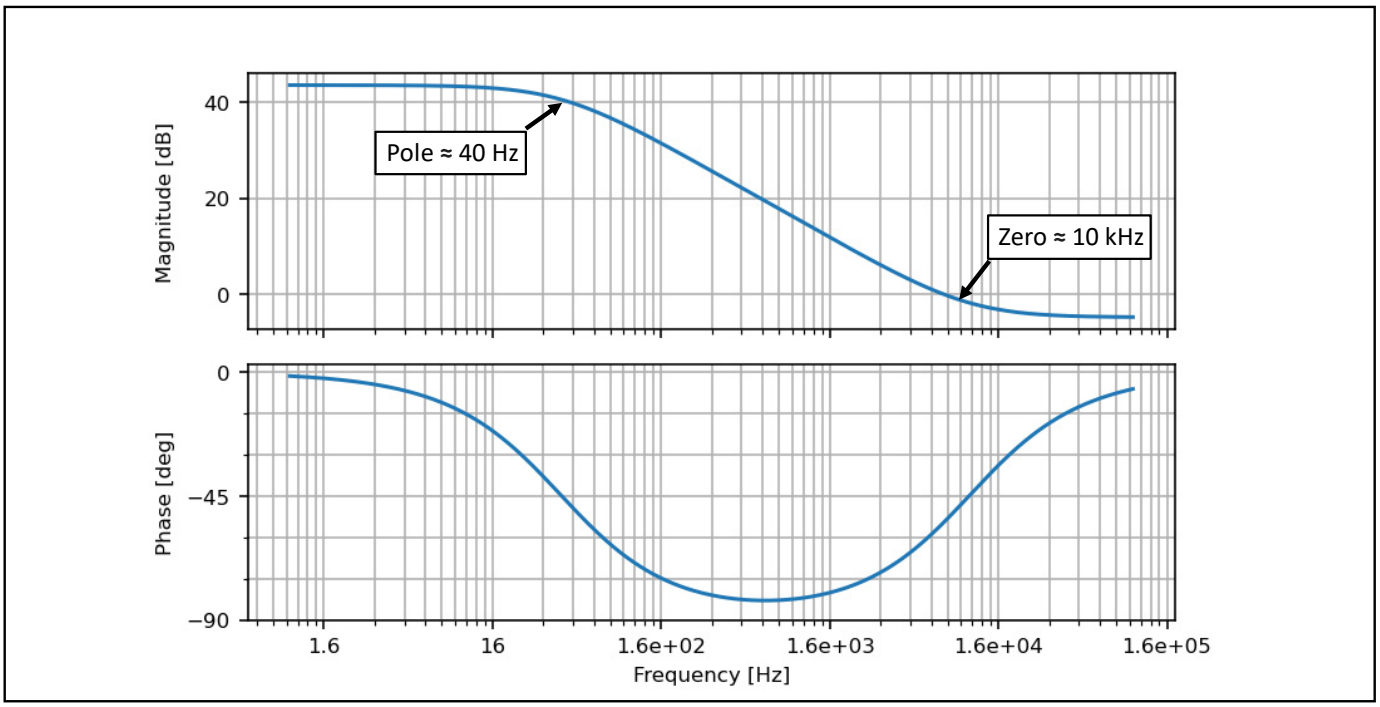


Figure 19. Plant Pole Zero Map.

Main CV Loop Compensation Transfer Function

The HiperLCS-2 CV loop uses an Operational Transconductance Amplifier (OTA) as the error amplifier with Type II compensation. Figure 20 shows a simplified representation of the FB network. Note that the type II compensator in the OTA also introduces a pole at the origin.

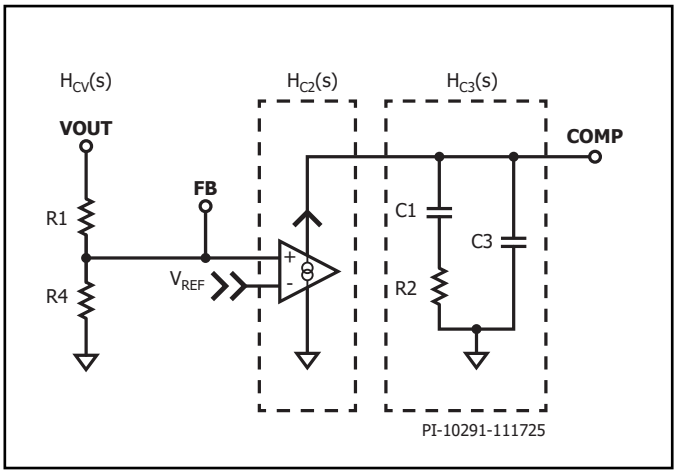


Figure 20. Circuit Diagram of the Voltage Feedback Loop.

The transfer function can be written as:

$$H_{CV}(s) = \frac{R_4}{R_1 + R_4}$$

$$H_{C2}(s) = gm$$

$$H_{C3}(s) = \frac{1 + sR_2C_1}{s(C_3 + C_1) + R_2C_3C_1s^2}$$

$$H_C(s) = H_{C2}(s) \times H_{C3}(s)$$

$$H_C(s) = gm\frac{1 + sR_2C_1}{s(C_3 + C_1) + R_2C_3C_1s^2} \quad (10)$$

Note: $H_{CV}(s)$ is not yet included. This will be accounted for in the CC loop derivation section.

The transfer function $H_{C3}(s)$ can be used to calculate for the locations of the pole and zero.

$$f_Z = \frac{1}{2\pi \times R_2 \times C_1}$$

$$f_P = \frac{C_1 + C_3}{2\pi \times R_2 \times C_1 \times C_3}$$

CV-Only Loop

Combining all equations to get the overall transfer function for CV mode. $L_{CV}(s)$ can be written as.

$$L_{CV}(s) = G(s) \times H_{CV}(s) \times H_C(s)$$

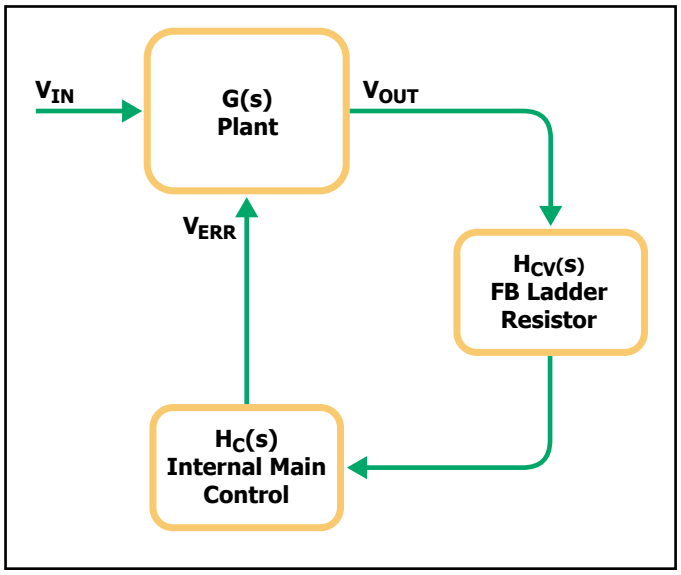


Figure 21. CV Closed-Loop Diagram.

Generally, it is desirable to put the crossover frequency between the plant's pole and zero locations. For CV-mode-only designs, the crossover frequency is typically set at 5 kHz. In a design that also offers CC operation, the bandwidth of the CC loop and the crossover frequency will be lower. In CC mode this loop will dominate.

Following an approach similar to the K-factor method where the poles and zeros are replaced by a factor K will show the maximum phase boost at the crossover frequency. Larger value of K results in more phase boost, but generally the poles and zeros from the compensation circuits must be close to the plant pole and zero. A typical starting value for K is 5.

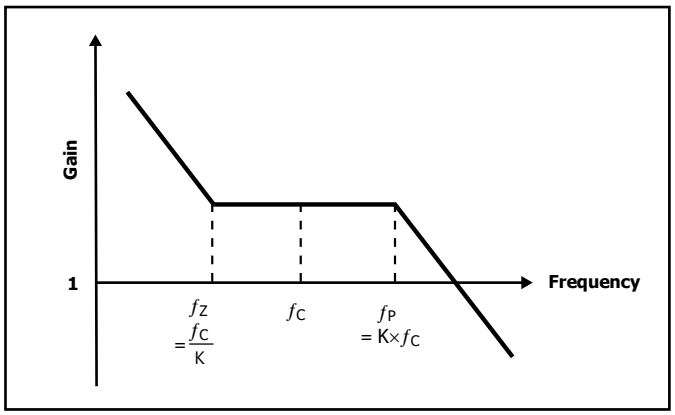


Figure 22. Placement of Pole and Zero with Respect to Crossover Frequency.

For this example set 2.5 kHz as the target crossover frequency. Using a factor of 5 to calculate f_Z and f_P will give:

$$f_Z = \frac{f_C}{K} = \frac{2.5\,kHz}{5} = 500\,Hz$$

$$f_P = K \times f_C = 5 \times 2.5\,kHz = 12.5\,kHz$$

The equation for the poles and zeros of the compensator was derived in equation (10). Substituting the calculated frequencies into this equation, corresponding RC values can be determined.

Calculating capacitor value for the Zero:

$$f_Z = \frac{1}{2\pi \times R_2 \times C_1}$$

Using 75 kΩ for R2:

$$C_1 = \frac{1}{2\pi \times 75\,k\Omega \times 500\,Hz} = 4.2\,nF \rightarrow 4.7\,nF$$

Calculating capacitor value for the Pole:

$$f_P = \frac{C_1 + C_3}{2\pi \times R_2 \times C_1 \times C_3}$$

Using 75 kΩ for R2 and 4.7 nF for C1:

$$C_3 = \frac{4.7\,nF}{(12.5\,kHz \times 2\pi \times 75\,k\Omega \times 4.7\,nF) - 1} = 176\,pF \rightarrow 150\,pF$$

These values can be added to the CV (only) equation to confirm that gain and phase margins are acceptable.

$$L_{CV}(s) = G(s) \times H_{CV}(s) \times H_C(s)$$

It can be seen in Figure 23 that the result is close to the target crossover frequency and provides very good phase margin.

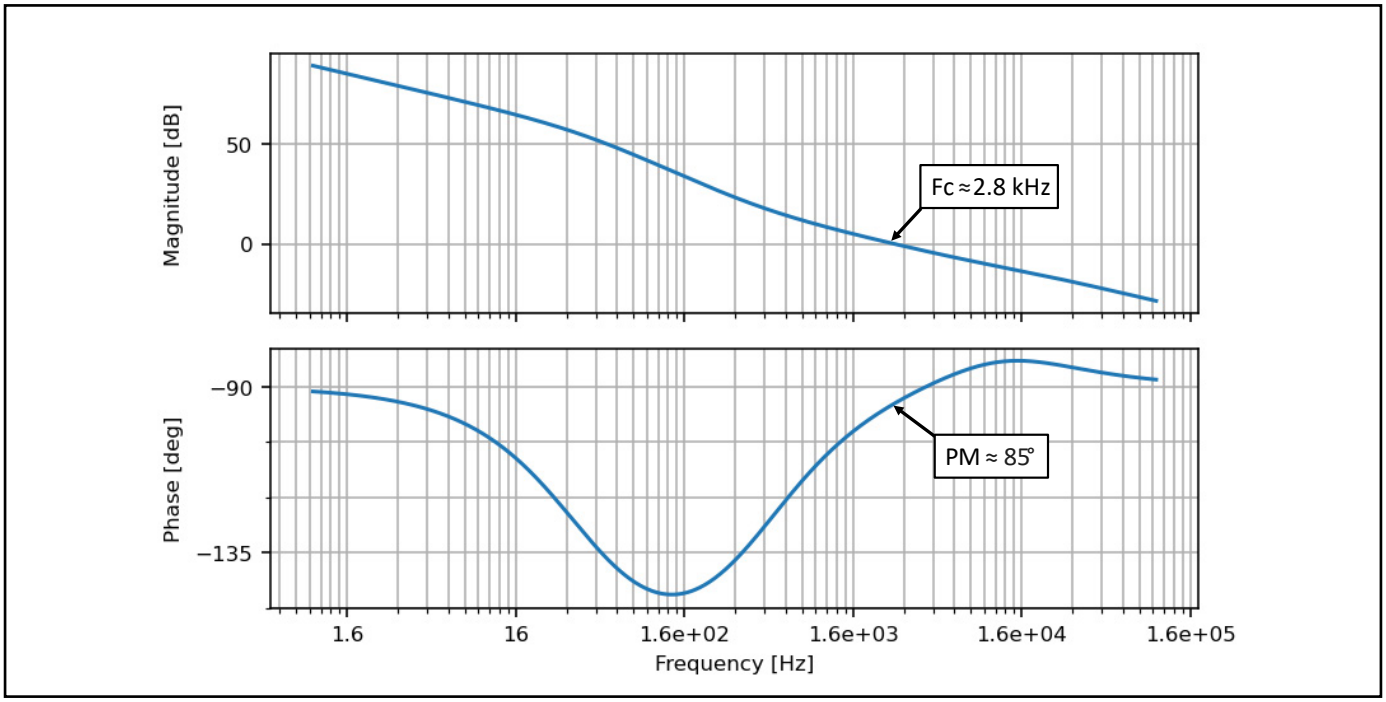


Figure 23. Closed Loop Bode Plot of CV Loop.

External Current Loop Compensation Transfer Function

As described previously the charger designs using the HiperLCS2-SR chipset employ an external circuit to implement CC operation.

The error amplifiers are used to regulate output current by regulating the FB pin of the LSR2000C IC. Figure 24 shows the simplified diagram of the external current loop and the derivation of its transfer function follows.

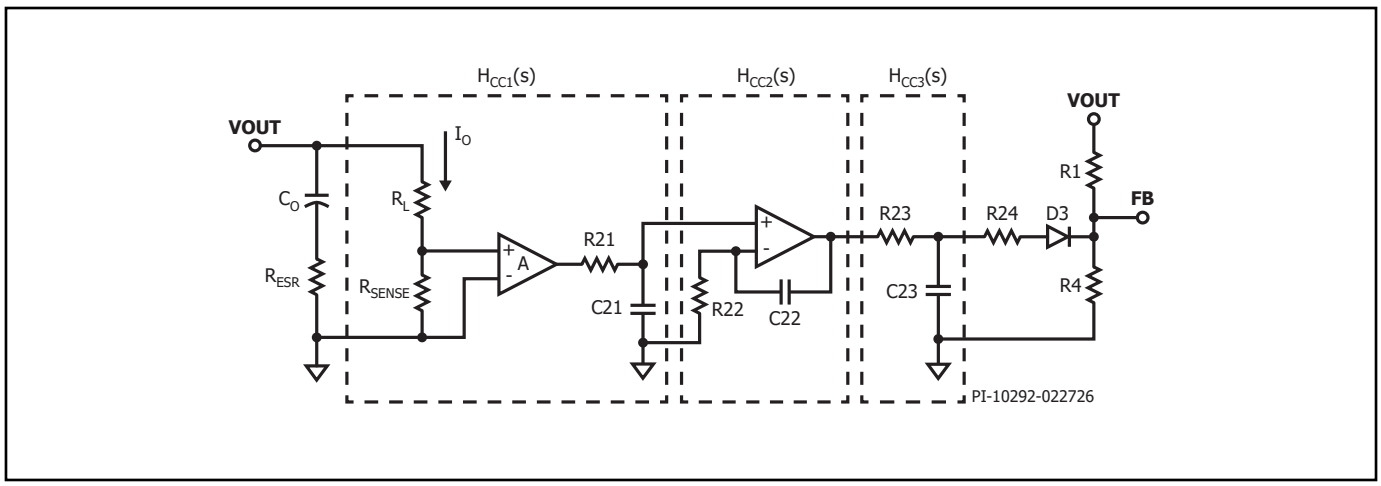


Figure 24. External CC Control Loop.

$H_{CC1}(s)$ is the transfer function of the current sense amplifier and RC filter. In Figure 24, R21 and C21 provide a noise filter for the amplified signal derived from the sense resistor.

$$H_{CC1}(s) = \frac{A \times R_S}{1 + sC_{21}R_{21}}$$

A is amplifier gain. R_S is the sense resistance (R_{SENSE}).

$H_{CC2}(s)$ is the transfer function for the error amplifier. R22 and C22 form a zero that provides phase boost. The non-inverting error-amplifier also introduces a pole at the origin.

$$H_{CC2}(s) = 1 + \frac{1}{sC_{22}R_{22}}$$

$H_{CC3}(s)$ is the transfer function for the RC filter. The OTA has a very fast response which necessitates to provision of the RC filter to prevent noise and transients from effecting the CC output. The RC filter has minimal effect on the overall loop response.

$$H_{CC3}(s) = \frac{1}{1 + sC_{23}R_{23}}$$

Writing the transfer function for the whole CC loop:

$$H_{CC}(s) = H_{CC1}(s) \times H_{CC2}(s) \times H_{CC3}(s)$$

$$H_{CC}(s) = \frac{A \times R_S\left(1 + \frac{1}{sC_{22}R_{22}}\right)}{(1 + sC_{21}R_{21})(1 + sC_{23}R_{23})} \quad (11)$$

The output signal of the CC control loop I_O, which gives:

$$I_O \times H_{CC}(s) = \frac{V_O}{R_L} \times H_{CC}(s)$$

Assuming the diode is ideal and applying nodal analysis, we can re-arrange the circuit shown in Figure 25.

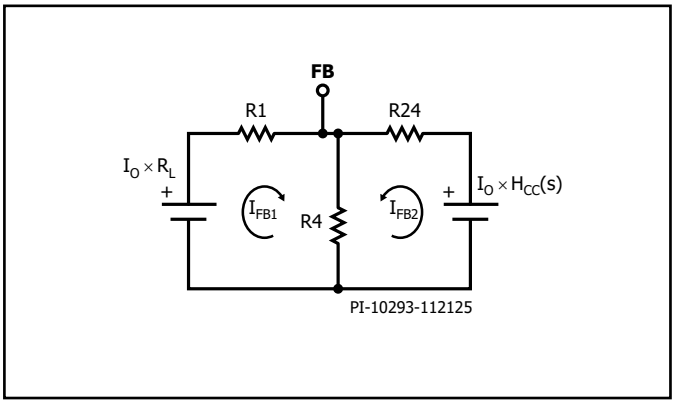


Figure 25. Nodal Analysis of FB Pin with CV and CC Loop.

$$\frac{V_O - V_{FB}}{R_1} + \frac{H_{CC}(s)I_O - V_{FB}}{R_{24}} = \frac{V_{FB}}{R_4}$$

$$R_{24}(V_O - V_{FB}) + R_1(H_{CC}(s)I_O - V_{FB}) = \frac{R_1 R_{24}}{R_4}V_{FB}$$

$$R_{24}V_O + \frac{R_1 H_{CC}(s)}{R_L}V_O = \frac{R_1 R_{24}}{R_4}V_{FB} + (R_1 + R_{24})V_{FB}$$

$$\left(R_{24} + \frac{R_1 H_{CC}(s)}{R_L}\right)V_O = \frac{R_1 R_{24} + R_1 R_4 + R_4 R_{24}}{R_4}V_{FB}$$

$$V_{FB} = \frac{R_L R_{24} R_4 + R_1 R_4 H_{CC}(s)}{R_L(R_1 R_{24} + R_1 R_4 + R_4 R_{24})}V_O$$

$$\frac{V_{FB}}{V_O} = \frac{R_L R_{24} R_4 + R_1 R_4 H_{CC}(s)}{R_L(R_1 R_{24} + R_1 R_4 + R_4 R_{24})} = H_{CVCC}(s) \quad (12)$$

Where,

$$V_O = I_O(R_L + R_S)$$

$$R_L >> R_S$$

$$V_O = I_O R_L$$

In CV mode, there will not be any feedback from the CC error-amplifier.

$$V_{FB} = \frac{R_4}{R_1 + R_4}V_O$$

$$V_{FB} = H_{CV}(s)V_O$$

Where,

$$H_{CV}(s) = \frac{R_4}{R_1 + R_4}$$

Combining Derived Equations

Combining equations provides an overall transfer function including CC mode $L_{CC}(s)$.

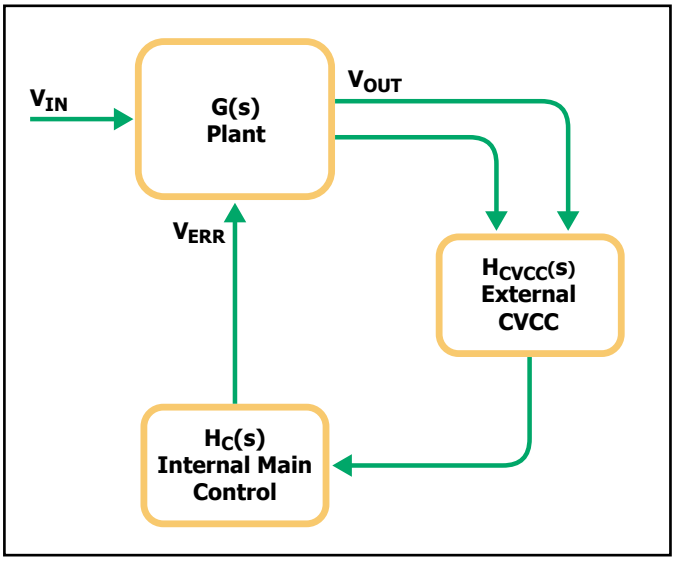


Figure 26. CV + CC Closed-Loop.

$$L_{CC}(s) = G(s) \times H_{CVCC}(s) \times H_C(s) \quad (13)$$

Tuning the External CC Loop

Introducing an external error amplifier for the CC loop, configured as non-inverting integrator, adds a pole at the origin. This combined with the CV loop origin-pole and the plant pole from the output capacitance and load impedance, creates a significant phase roll-off. To maintain stability, the zero of the CC loop error-amplifier should be placed near the plant pole to offset this effect.

The pole and zero from the CC loop can be calculated as,

$$H_{CC2}(s) = 1 + \frac{1}{sC_{22}R_{22}}$$

$$H_{CC2}(s) = \frac{1 + sC_{22}R_{22}}{sC_{22}R_{22}}$$

Plant pole is located at,

$$f_P = \frac{1}{2\pi \times R_L \times C_O}$$

CC loop zero is located at,

$$f_Z = \frac{1}{2\pi \times R_{22} \times C_{22}}$$

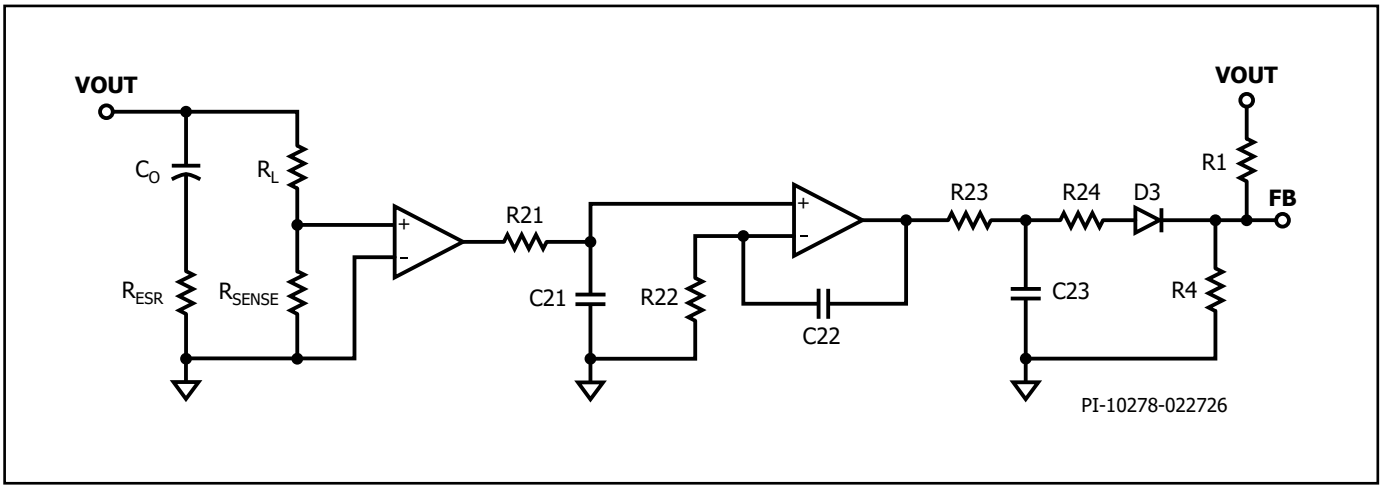


Figure 27. Circuit Diagram of External CC Control Loop .

Measuring Loop Response with a Frequency Analyzer

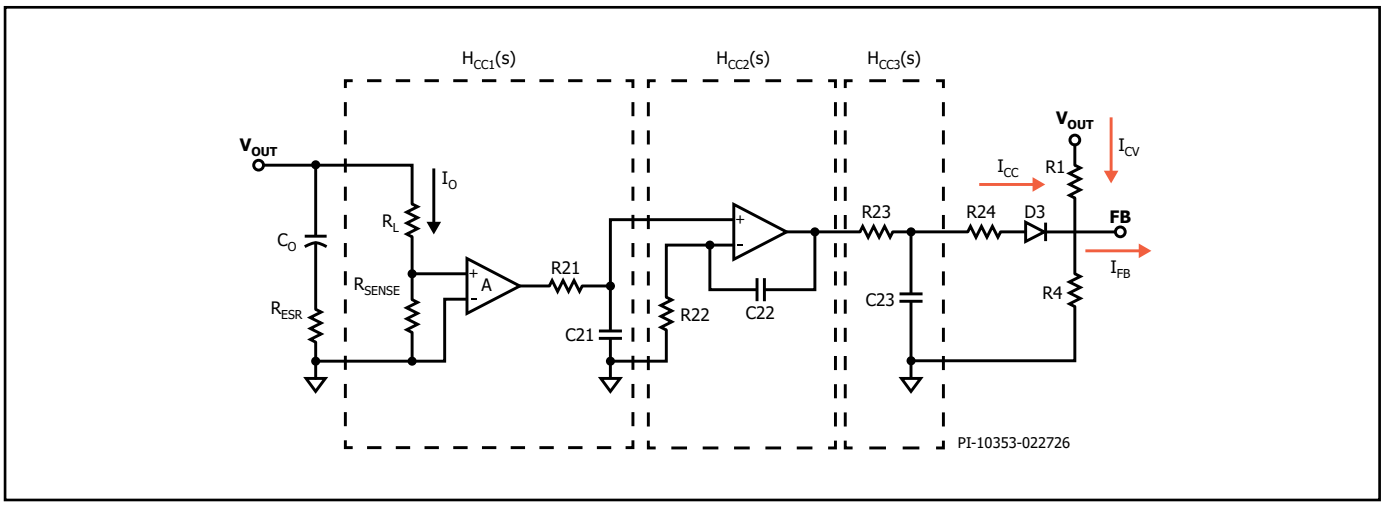


Figure 28. Effect of Voltage Feedback Resistors in the CC Loop.

When measuring the bode plot of the CC loop, the signal is taken from the I_{CC} path. However, as shown in Figure 28, during CC mode the CC loop controls regulation. There is still a fixed current introduced by V_{OUT} (I_{CV}). This current acts as a fixed gain in the transfer function and must also be considered. To include this in the loop measurement, the circuit shown in Figure 29 is used which will account the currents going into the FB pin from both I_{CC} and I_{CV}.

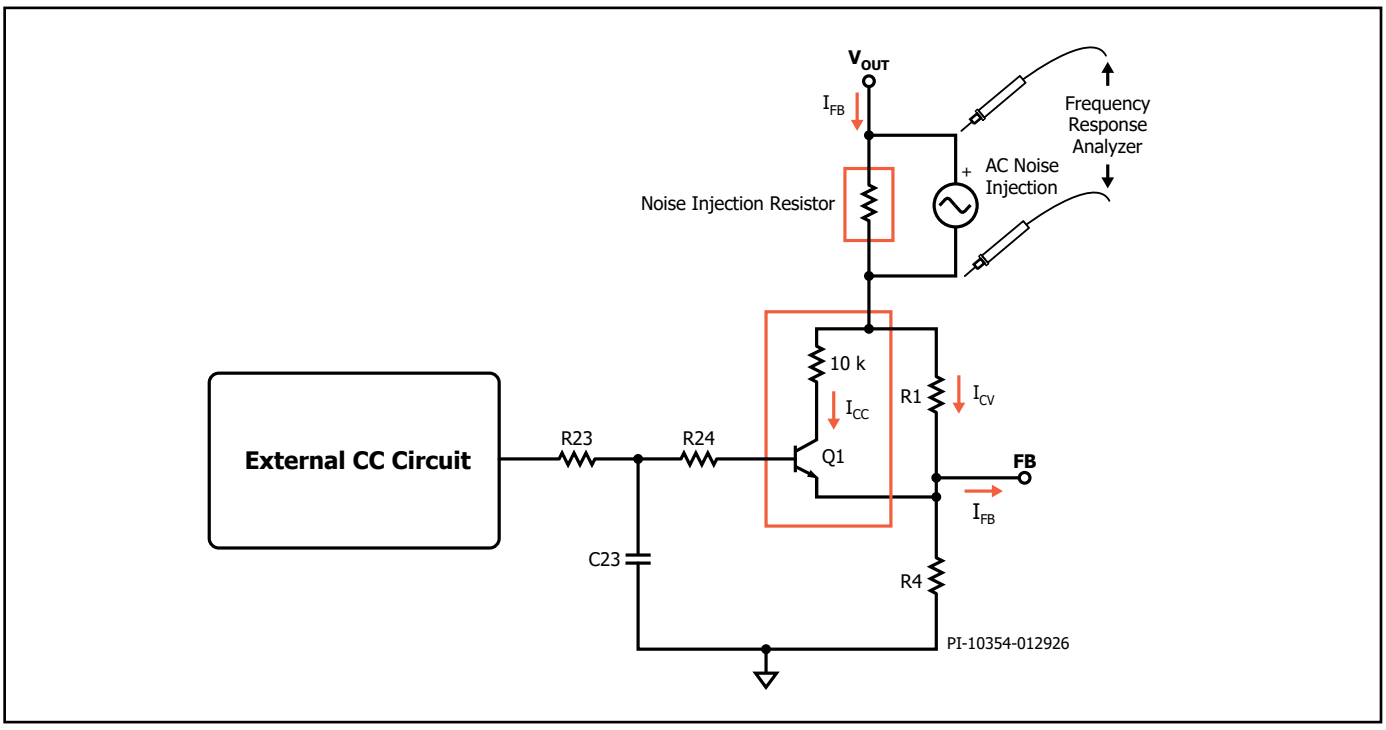


Figure 29. CC Loop Bode Plot Set-Up.

Instead of the external CC circuit directly sourcing current into the FB pin, it is now biasing the base of Q1 which modulates the current (I_{CC}) going into the FB pin. This allows gain and phase response of the I_{FB} path which includes both currents for I_{CC} and I_{CV} to be measured. This will allow measurement of the bode plots for both CC and CV modes with the same set-up.

In the design example, the plant pole is at ~40 Hz. Using R22 = 15 kΩ and C22 = 470 nF, the zero is positioned just before the plant pole, preventing rapid phase roll-off and ensuring adequate phase margin.

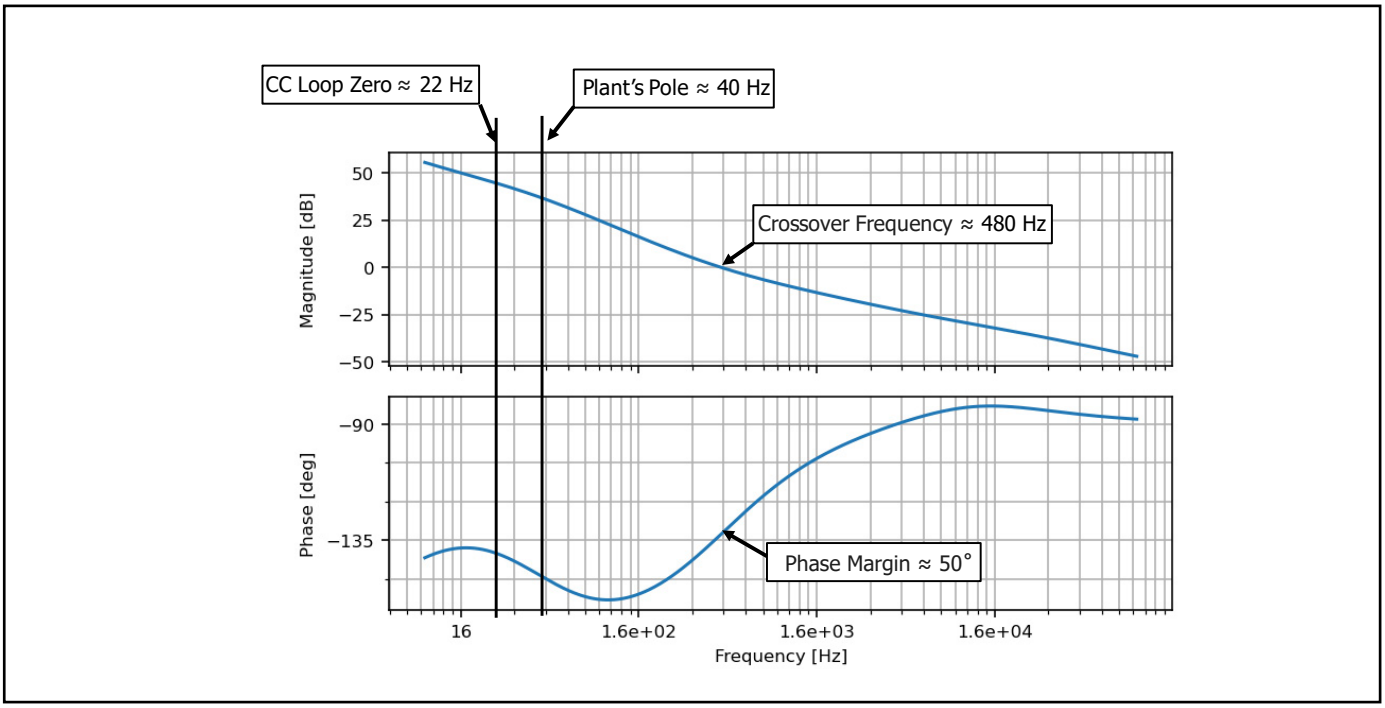


Figure 30. Closed-Loop Bode Plot of CC Control in Correctly Compensated Design.

Conversely, reducing the capacitor C22 to a very small value, (4.7 nF), shifts the zero far beyond the multiple poles. This causes the phase to diminish before the crossover frequency, resulting in a loss of phase margin as shown in Figure 31.

A 470 nF capacitor and a 15 kΩ resistor combination is a good compromise. As a general rule, position the zero for the CC loop close to the plant's pole location.

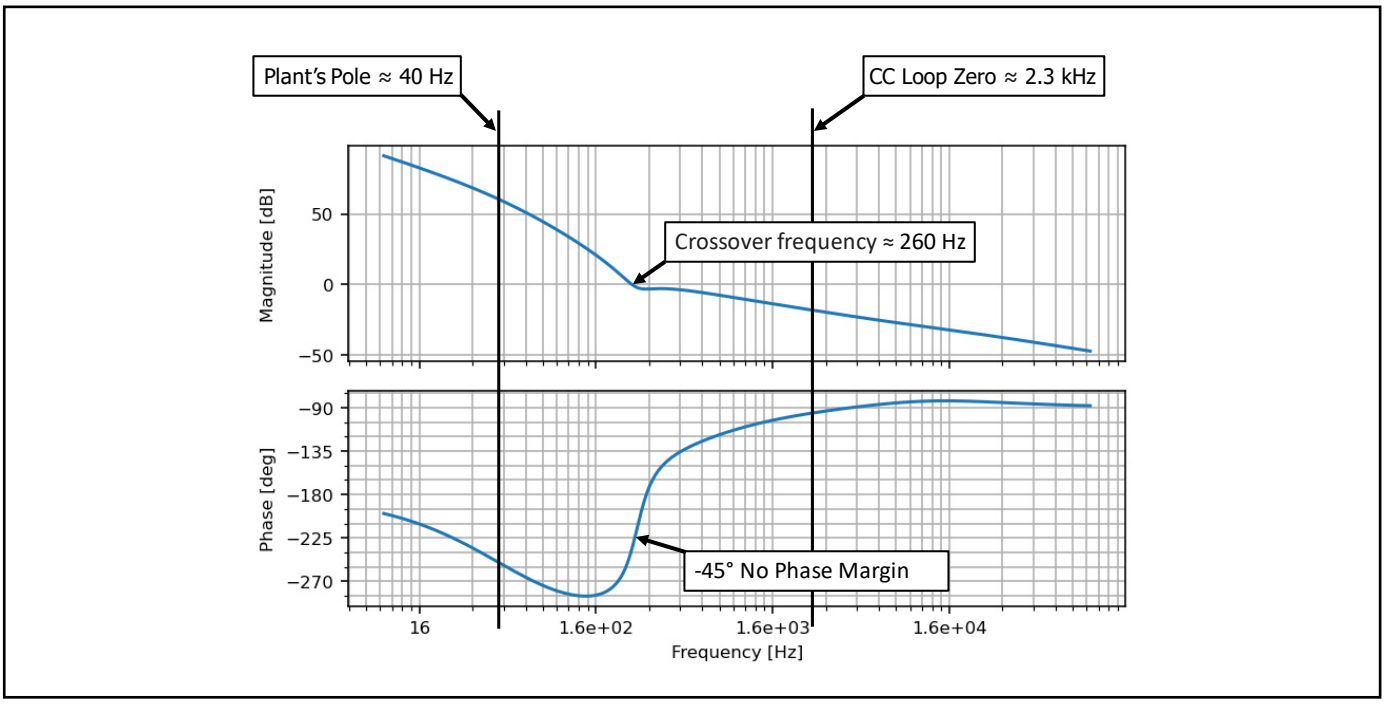


Figure 31. Closed-Loop CC Bode Plot of Control with poor Placement of Loop Zero.

To check the accuracy of the derivation, gain and phase plots from bench measurements were compared to the derived transfer functions. Figure 32 shows similar results with respect to the measured crossover frequency and phase margin. However, in the high frequency region, the actual measurement showed no roll-off as predicted in the simulation. This was because the derivation assumed 100% conversion efficiency and ignored energy storage in the resonant components. The assumption is valid because the effect only becomes apparent close to the switching frequency - beyond the useful range of the model.

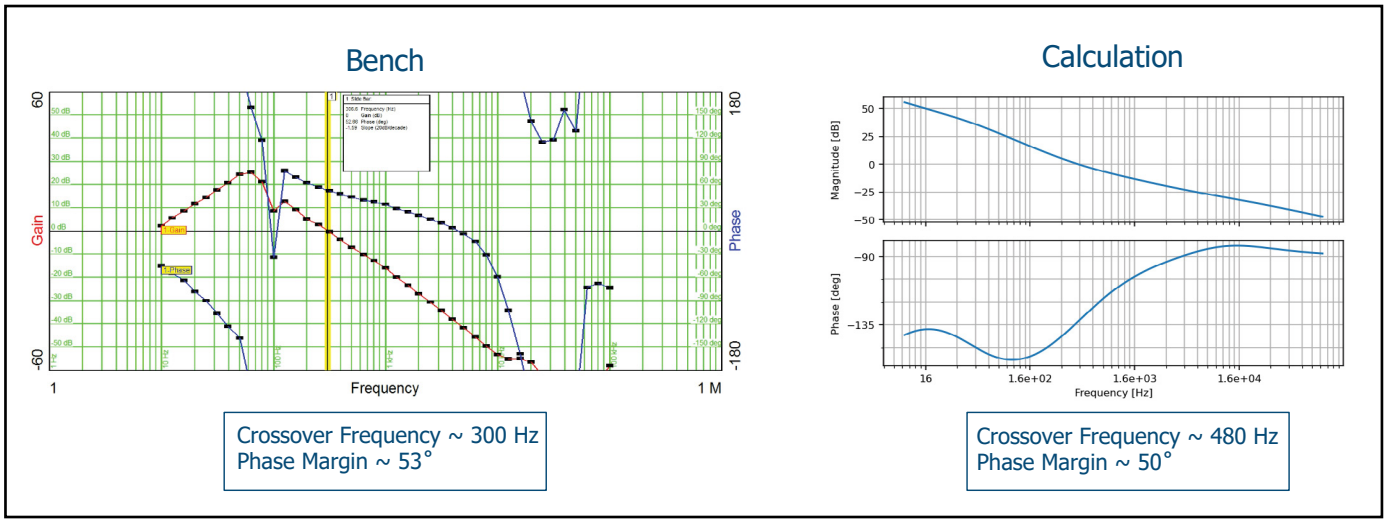


Figure 32. Bench and Calculation Bode Plot Correlation.

CC Loop Large Signal Filter

In order to regulate output current, the current from the CC loop must go into the FB pin. The FB pin drives a transconductance amplifier which regulates the output voltage and provides very fast dynamic response. This fast response can make the circuit susceptible to noise. This is not an issue with CV mode, because ripple or noise seen at the FB pin will still give <1% output ripple voltage which is adequate for power supply applications. However for battery chargers, <1% output voltage ripple can cause >10% current ripple because of the low impedance characteristics of the load.

A low pass filter (R23 and C23) after the CC error-amplifier helps reduce ripple. This filter asserts a strong effect on large signals. The RC value has minimal effect on AC small signal analysis and associated gain-phase plots.

For the example circuit, 4.7 kΩ and 470 nF were chosen which gave the smallest current ripple across various loads (E-load, capacitor bank and battery) seen in the actual bench measurements. These values have been proven to work across several designs.

Note: For charger designs that are housed in metal enclosures, ensure that both primary and secondary side Y capacitors have a solid connection to earth/enclosure via the PCB and mounting screws to prevent circulating noise that can increase output current ripple.

Figure 34 shows bench measurement of CC loop response with and without the RC filter.

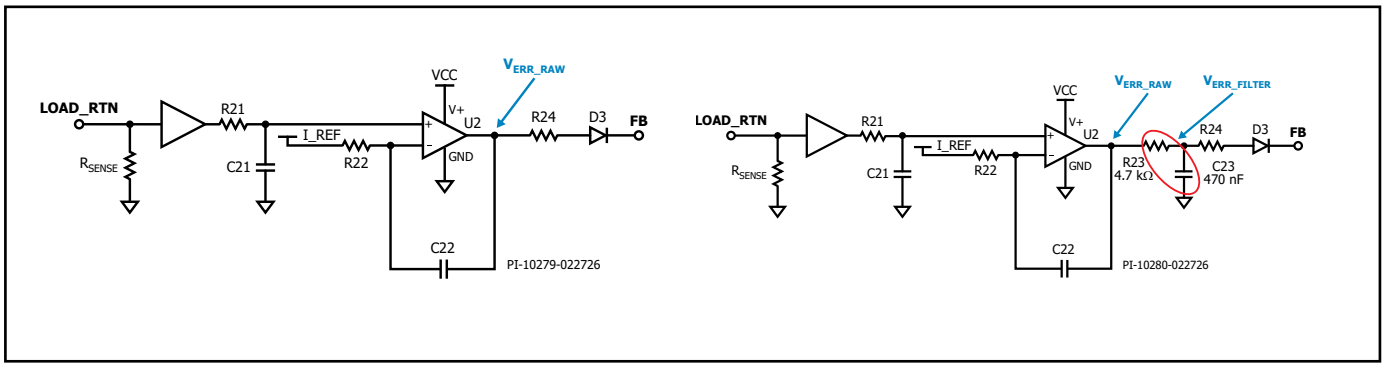
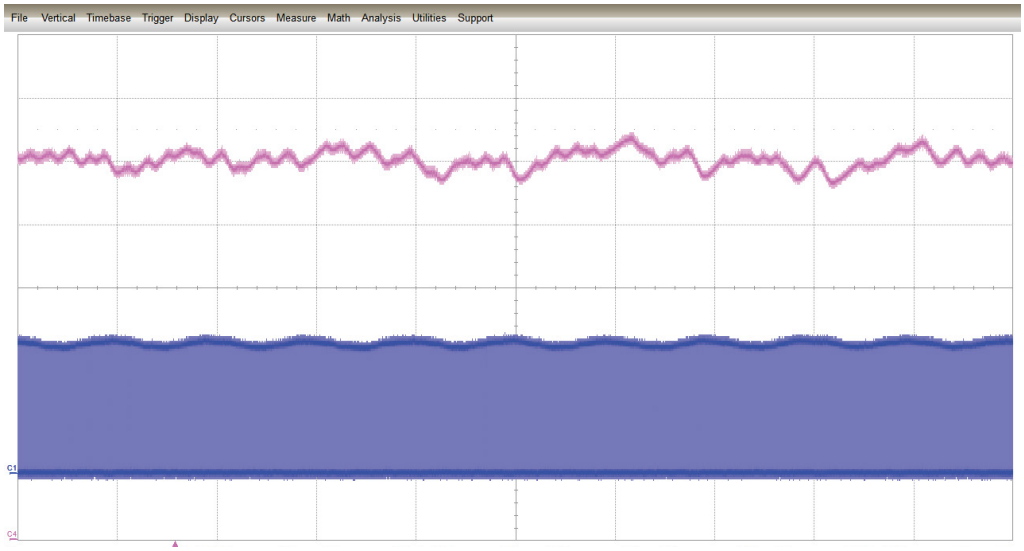


Figure 33. Simplified Schematic without RC Filter (left), and with RC Filter (right).

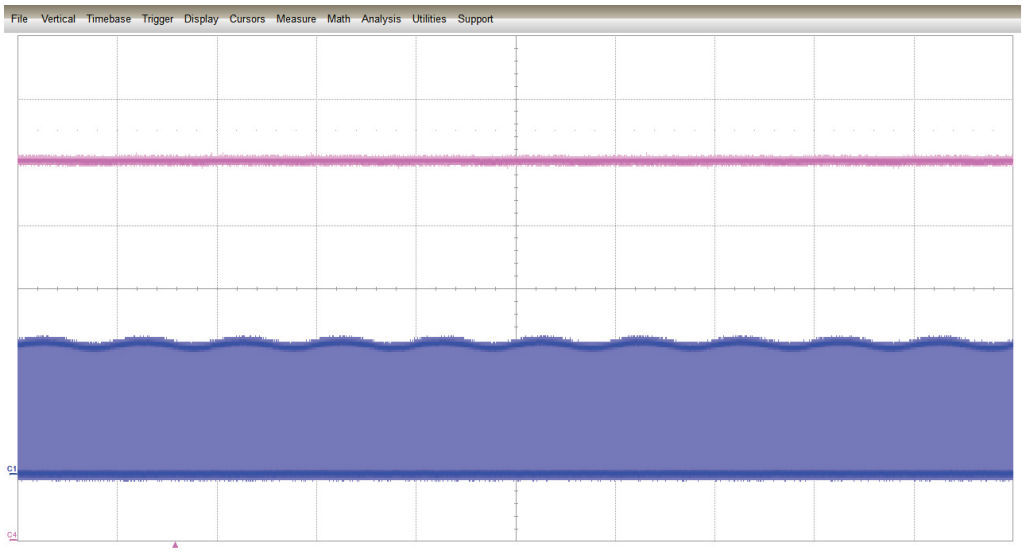
Without RC Filter



I_{OUT} Ripple pk-pk = 1.7 A

C1-V_HB, 200 V/div
C4-I_out, 2 A/div
Time division: 10 ms/div

With RC Filter

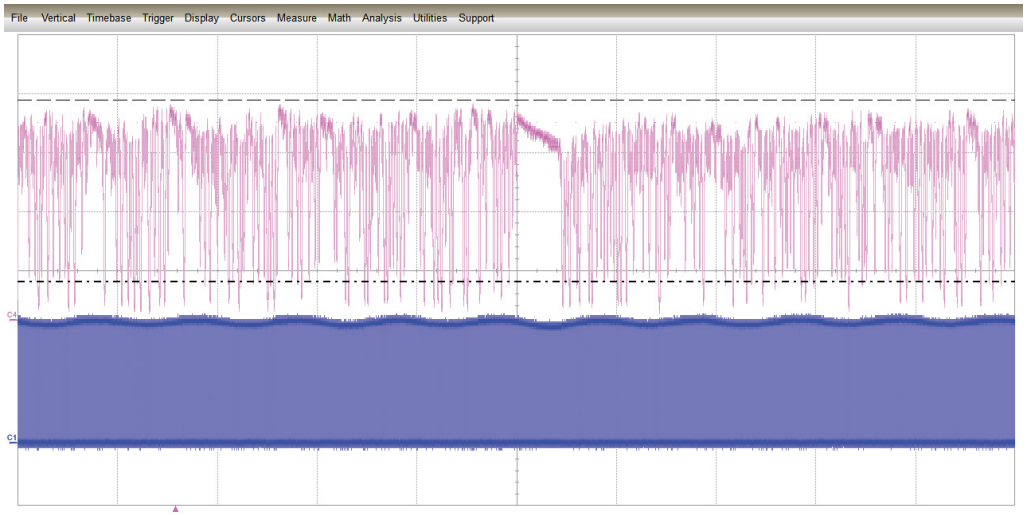


I_{OUT} Ripple pk-pk = 465 mA

C1-V_HB, 200 V/div
C4-I_out, 2 A/div
Time division: 10 ms/div

Figure 34. Output Ripple Current with E-load (55 V_12 A).

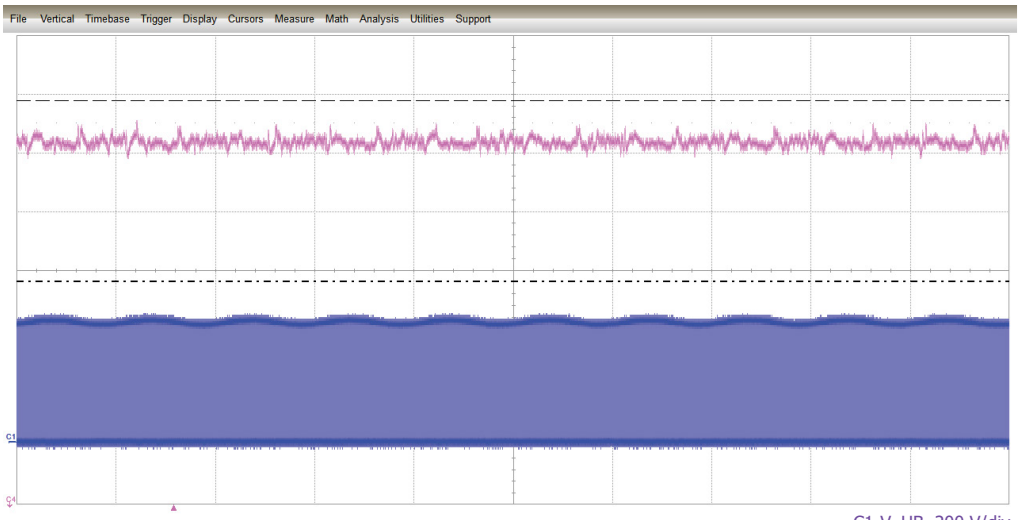
Without RC Filter



I_{OUT} Ripple pk-pk = 17.8 A

C1-V_HB, 200 V/div
C4-I_out, 5 A/div
Time division: 10 ms/div

With RC Filter

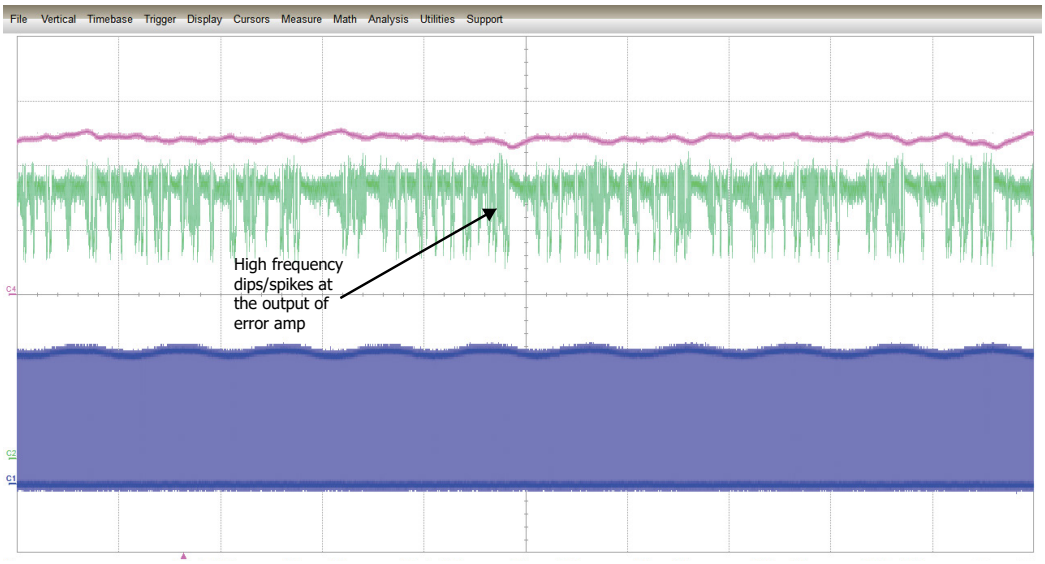


I_{OUT} Ripple pk-pk = 630 mA

C1-V_HB, 200 V/div
C4-I_out, 1 A/div
Time division: 10 ms/div

Figure 35. Output Ripple Current with Battery Load (46 V_12 A).

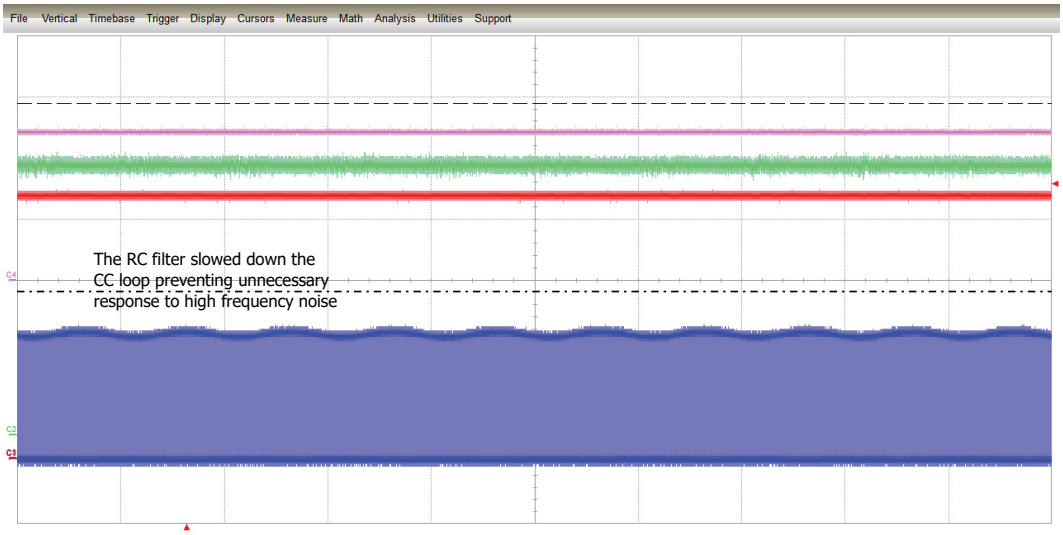
Without RC Filter



I_{OUT} Ripple pk-pk = 1.7 A

C1-V_HB, 200 V/div
C2-Verr_raw, 1 V/div
C4-Iout, 5 A/div
Time division: 10 ms/div

With RC Filter



I_{OUT} Ripple pk-pk = 540 mA

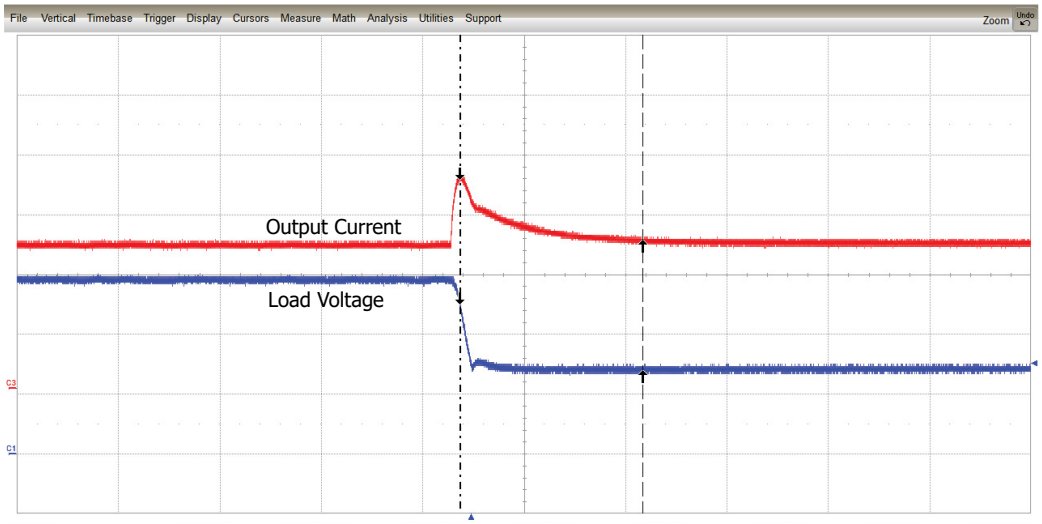
C1-V_HB, 200 V/div
C2-Verr_raw, 1 V/div
C3-Verr_filter, 1 V/div
C4-Iout, 1 A/div
Time division: 10 ms/div

Figure 36. Output Ripple Current with E-load (55 V_12 A).

Transient Response of the CC Loop

Good CC loop stability can be demonstrated by performing a dynamic load test. Changing the load voltage from 55 V (high end of output voltage for a typical 60 V charger design) going down to 26 V (worst-case deep discharge state of a 48 V battery) creates a sudden load change. In real-world applications, batteries will not typically experience a sudden jump in voltage, but the aim of this test is to show the stability of the loop.

Figure 37 below shows the stability of the CC loop after a load transient step of 55 V to 26 V voltage transient at 12 A CC load. The load current overshoots and is heavily influenced by the output capacitor. When the load voltage changed from 55 V to 26 V, the charge stored in the output capacitors delivered current to the load until it discharged to the new load voltage of 26 V.



C1: Load Voltage, 20 V/div
C3: Output Current, 5 A/div
Time division: 10 ms/div

Figure 37. Load Transient Response Waveform.

Improving Output Ripple Current

With resistive loads, the output ripple current is typically very low, as most of the switching current ripple filtered out by low impedance of the output bulk capacitors compared to the load impedance. However, for battery charger applications or applications with a highly capacitive load, the impedance of the load may be lower than the impedance of the output capacitance. Current ripple will appear on the path with the lowest impedance which in this case is the load, causing output current ripple to rise.

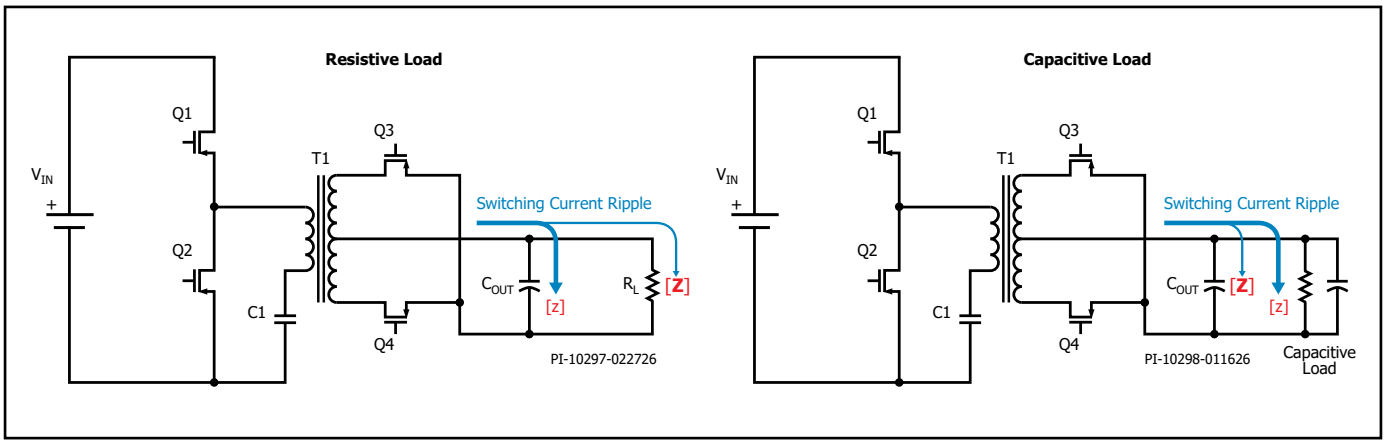
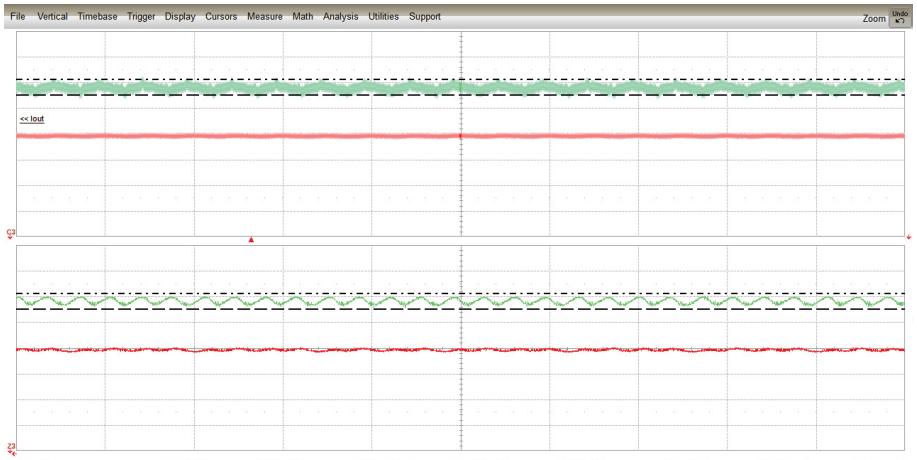


Figure 38. Diagram Showing the Effect of Capacitive Load on Output Current Ripple.

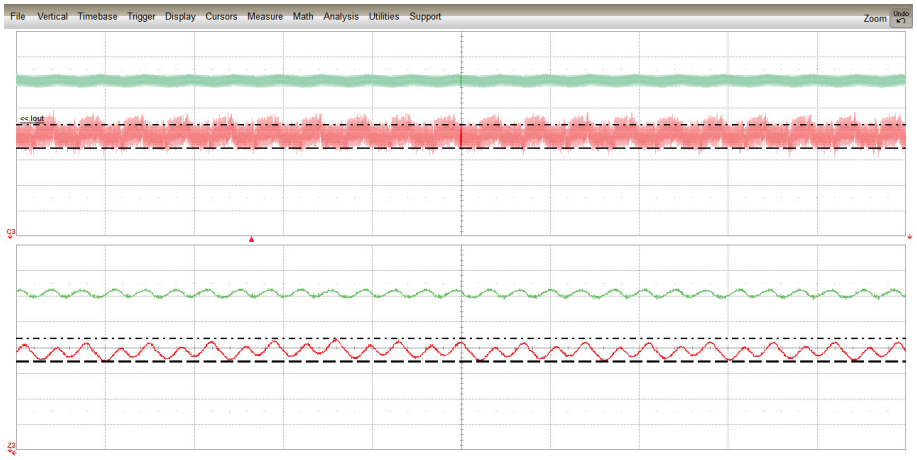
Resistive Load (58 V / 12 A)



Switching Current Ripple < 100 mA
Overall Current Ripple = 266 mA

C2: V_out, 500 mV/div
C3: I_load, 1 A/div
Time division: 20 ms/div
Zoom time division: 17.8 µsec/div

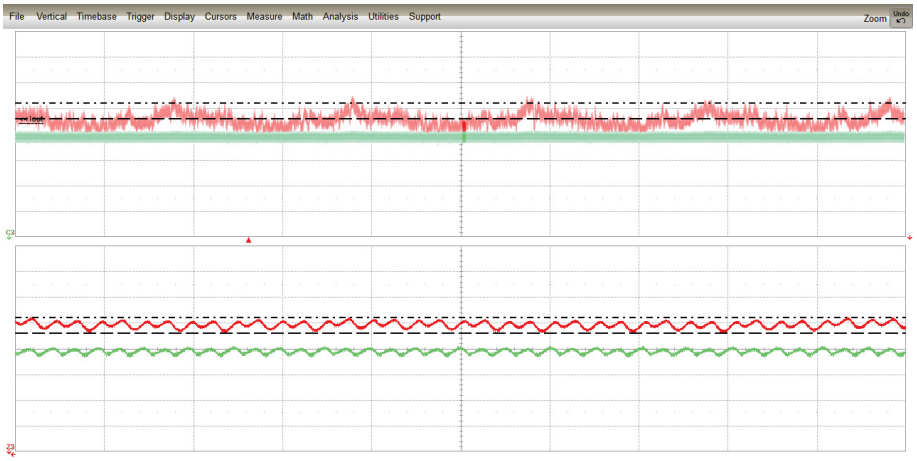
12 mF Capacitive Load (58 V / 12 A)



Switching Current Ripple < 900 mA
Overall Current Ripple = 1.83 A

C2: V_out, 500 mV/div
C3: I_load, 1 A/div
Time division: 20 ms/div
Zoom time division: 17.8 µsec/div

48 V / 60 Ah NMC Battery Load (48 V / 12 A)



Switching Current Ripple < 300 mA
Overall Current Ripple = 946 mA

C2: V_out, 500 mV/div
C3: I_load, 1 A/div
Time division: 5 ms/div
Zoom time division: 21.5 µsec/div

Figure 39. Output Current Ripple with Different Load Types.

To minimize switching current ripple coming from power supply going into the load, an LC post filter was added (as shown in Figure 40) to direct ripple current into the output filter capacitors.

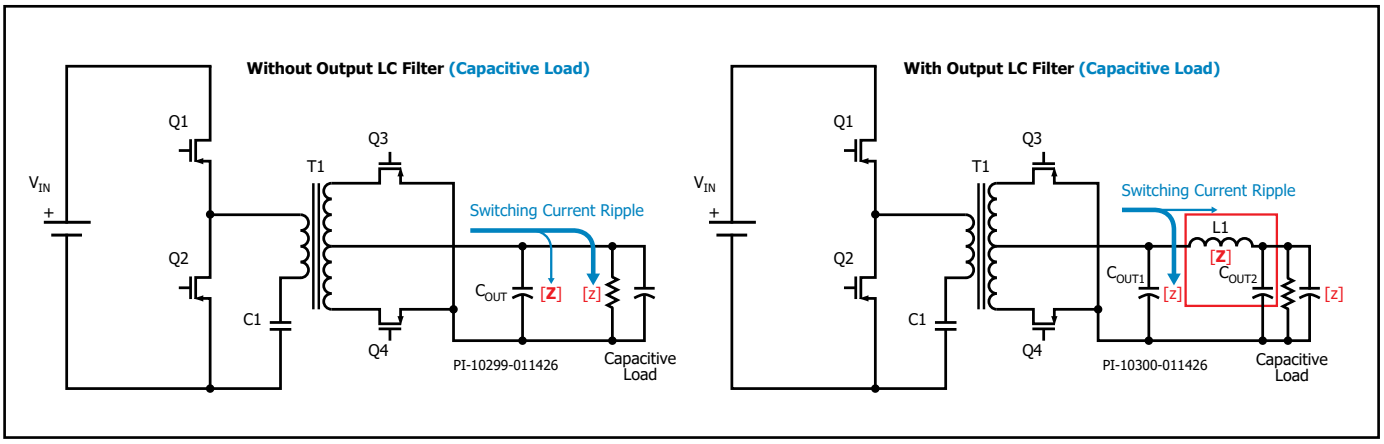


Figure 40. Diagram Showing the Effect of Adding a Two-Stage Filter.

The size of the post filter will depend on the switching frequency ripple-current specification. Using the formula for inductor voltage, the ripple current induced by the desired output ripple voltage can be estimated.

$$L_{FILTER} = V_{RIPPLE} \frac{dt}{di}$$

Where,

V_{RIPPLE}: output voltage ripple

di: target output current ripple

dt: period of the peak to peak ripple current. This is 2x the LLC switching frequency

Example: A 60 V/12 A power supply switching at 85 kHz, pk-pk output with a current ripple limit of less than 1 A. For margin, target 0.5 A to calculate the inductance required. The next step is either to measure the actual output voltage ripple or assume 0.5% for a typical power supply that requires <1% voltage ripple.

$$L_{FILTER} = V_{RIPPLE} \frac{dt}{di}$$

$$L_{FILTER} = 0.5\% \times 60\,V \frac{5.9\,\mu s}{0.5\,A} \qquad (14)$$

$$L_{FILTER} = 3.5\,\mu H$$

Next, calculate filter capacitor that will determine the cutoff frequency. The power supply switching frequency (f_{SW}) is 85 kHz.

Set cutoff frequency in the range of 1/10 to 1/20 of f_{SW}. In this case a 1/20 multiplier is used.

$$f_C = \frac{f_{SW}}{20}$$

Deriving C from the cutoff frequency formula:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

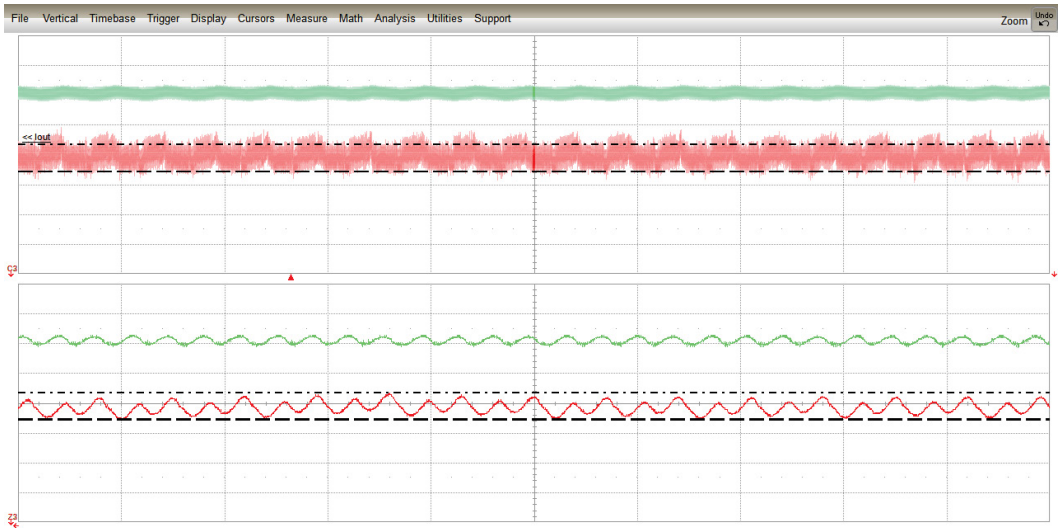
$$C = \frac{1}{(2\pi f_C)^2 L} = \frac{1}{\left(2\pi \frac{f_{SW}}{20}\right)^2 L}$$

$$C = \frac{1}{(2\pi \times 85\,kHz/20)^2 \times 3.5\,\mu H} = 400\,\mu F$$

Figure 41 shows measurement results, for an off-the-shelf 4.7 µH inductor, and 390 µF capacitor.

Comparison on a 12,000 µF Capacitive load:

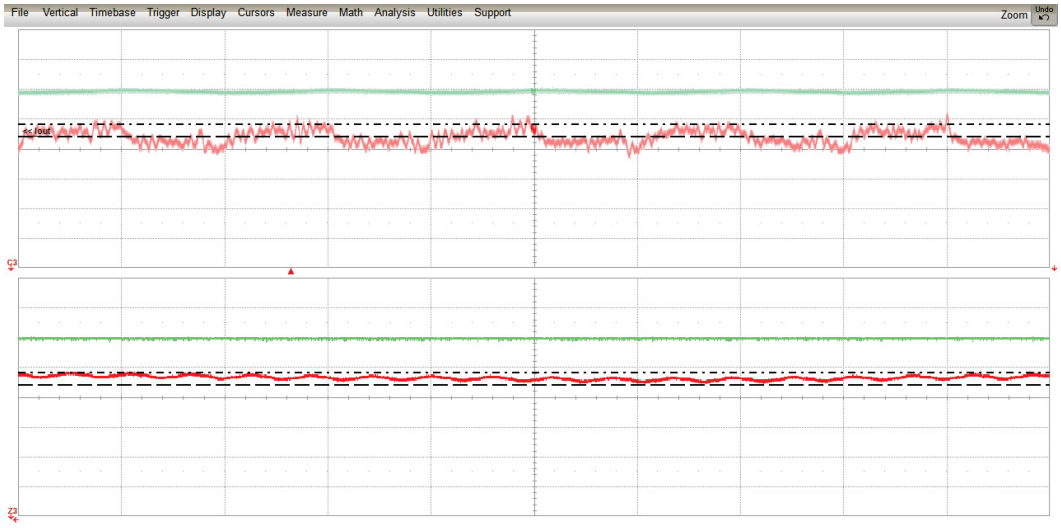
Capacitive Load without LC Filter



Switching Current Ripple ~ 900 mA
Overall Current Ripple = 1.83 A

C2: V_out, 500 mV/div
C3: I_load, 1 A/div
Time division: 20 ms/div
Zoom time division: 17.8 µsec/div

Capacitive Load with LC Filter



Switching Current Ripple ~ 210 mA
Overall Current Ripple = 764 mA

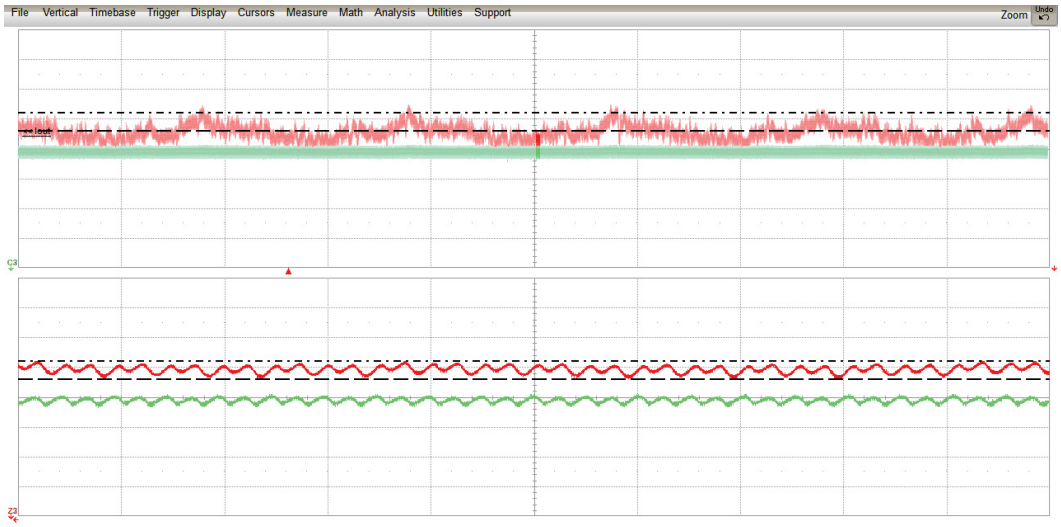
C2: V_out, 500 mV/div
C3: I_load, 1 A/div
Time division: 5 ms/div
Zoom time division: 21. 5 µsec/div

Figure 41. Comparison of Output Current Ripple with and without Second Stage Filter (cont. next page).

Figure 42 shows measurement results, for an off-the-shelf 4.7 µH inductor, and 390 µF capacitor.

Comparison on Battery load:

Battery Load without LC Filter



Switching Current Ripple ~ 300 mA
Overall Current Ripple = 946 mA

C2: V_out, 500 mV/div
C3: I_load, 500 mA/div
Time division: 5 ms/div
Zoom time division: 21.5 µsec/div

Battery Load with LC Filter

Switching Current Ripple ~ 105 mA
Overall Current Ripple = 764 mA

C2: V_out, 500 mV/div
C3: I_load, 500 mA/div
Time division: 5 ms/div
Zoom time division: 21.5 µsec/div

Figure 42. Comparison of Output Current Ripple with and without Second Stage Filter.

Comparing Measured Current Ripple on a Battery Versus Calculated Value

From the equation (14), calculate ripple current from known switching frequency (hence dt) and our measured output voltage ripple before adding the LC filter. From measurement above, V_{RIPPLE} = 266 mV, dt = 5.5 µs, L_{FILTER} = 4.7 µH

$$L_{FILTER} = V_{RIPPLE} \frac{dt}{di}$$

$$di = V_{RIPPLE} \frac{dt}{L_{FILTER}} = 0.266\,V \times \frac{5.5\,\mu s}{4.7\,\mu H} = 311\,mA$$

Measured ripple current is around 100 mA <1% of the rated current.

Effect of LC Filter on Small Signal Analysis

Adding an LC filter may have negative effect on the overall loop. Phase starts to drop at the resonant frequency of the LC filter. So when choosing the LC values, it is important to be aware that the resonant frequency of the filter must be higher than the crossover frequency. In this case, provided that the resonant frequency of the post filter is >1 kHz, adding the post filter will not have an impact on phase margin. >1 kHz is safe for charger designs.

Transformer Guidelines

Construction

The HiperLCS-2 IC chipset can support the use of an integrated LLC transformer, utilizing the leakage flux to form the resonant inductor. Generally, the transformer consists of 2 chambers, primary and secondary to generate a suitable leakage inductance.

All bias windings must be coupled to the secondary chamber. For a bias winding coupled to the primary, the bias voltage will be unpredictable as it will be highly dependent on the magnitude of half-bridge current.

IS winding must always be tightly coupled to the primary chamber. If the IS winding is coupled to the secondary, the primary current information that is crucial for control will be lost.

For battery charger applications, the LLC operates from CCM to deep DCM. In DCM operations, ring behavior may influence switching frequency variation, which can, in turn, affect output ripple. Optimized IS winding construction is required to eliminate this effect.

Recommended IS winding Construction:

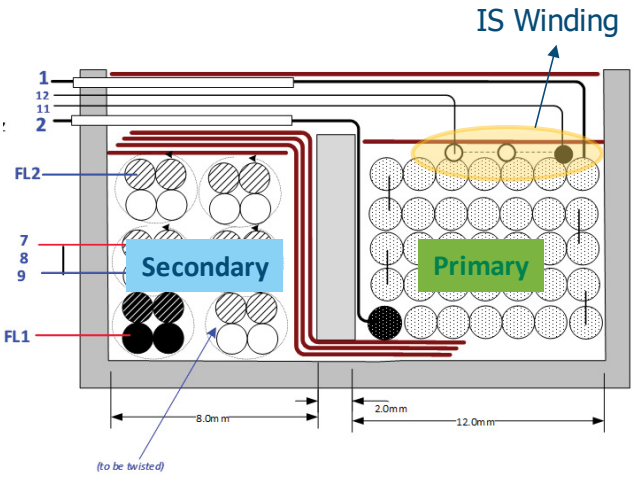


Figure 43. IS Winding Build Diagram.

1. Primary and secondary are separated by a divider to create primary and secondary chambers. Apply with at least one turn to ensure a complete final turn and to ensure consistent termination position.

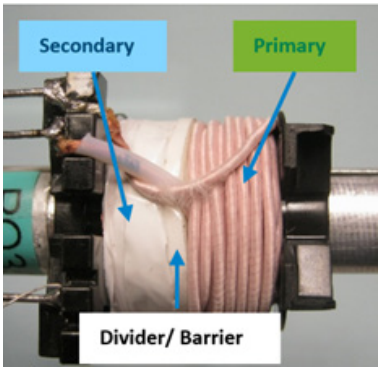


Figure 44. Transformer Showing Primary, Secondary and Barrier.

2. Add tape or marker that is half of the primary chamber width. This serves as a marker and indicates that the IS winding should be positioned as only on the half of the primary chamber winding- window that is away from the barrier.

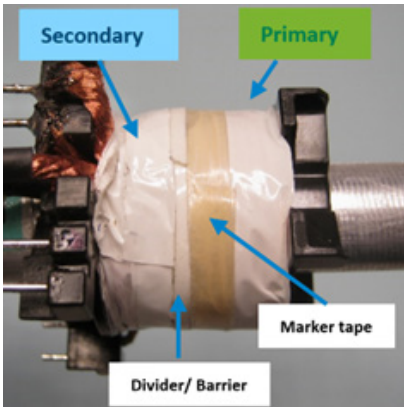


Figure 45. Transformer Showing Placement of Marker Tape.

3. Wind the IS winding. Spread the turns across the allocated window defined by the marker tape. Avoid placing the turns of IS on top of each other.

4. Twist the IS winding start and finish before terminating to the pins.

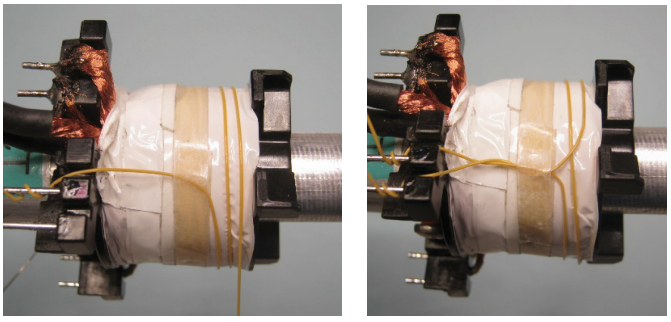


Figure 46. IS Winding Construction.

Figure 47 shows ideal IS waveform, the circled portions on the right image shows the DCM ring. This is inherent to the transformer but by following the recommended IS winding positioning, the likelihood of DCM ring pickup is greatly reduced.

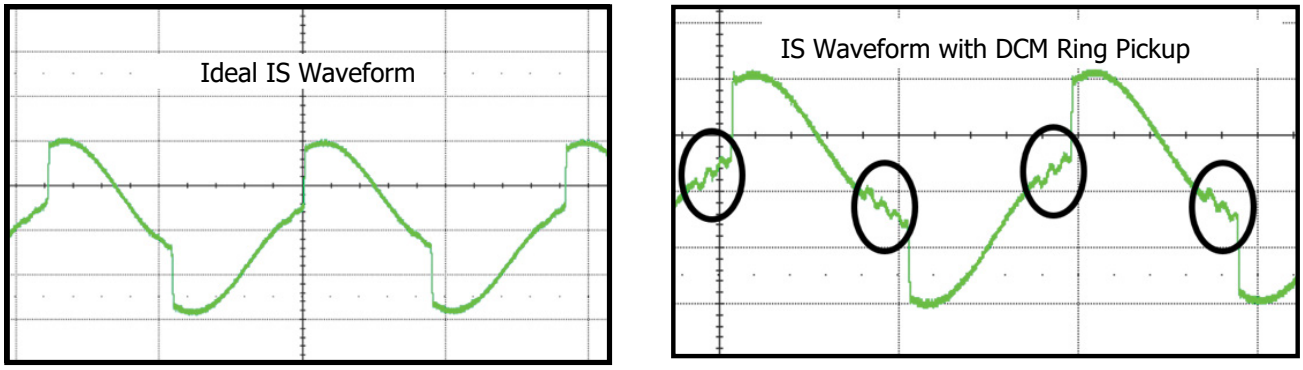


Figure 47. IS Waveform Comparison with and without DCM Ring.

Core Selection

A transformer that features a long center leg is recommended. This allows room for primary and secondary windings to be positioned side-by-side generating suitable leakage inductance. Examples are EFD, ETD and PQ.

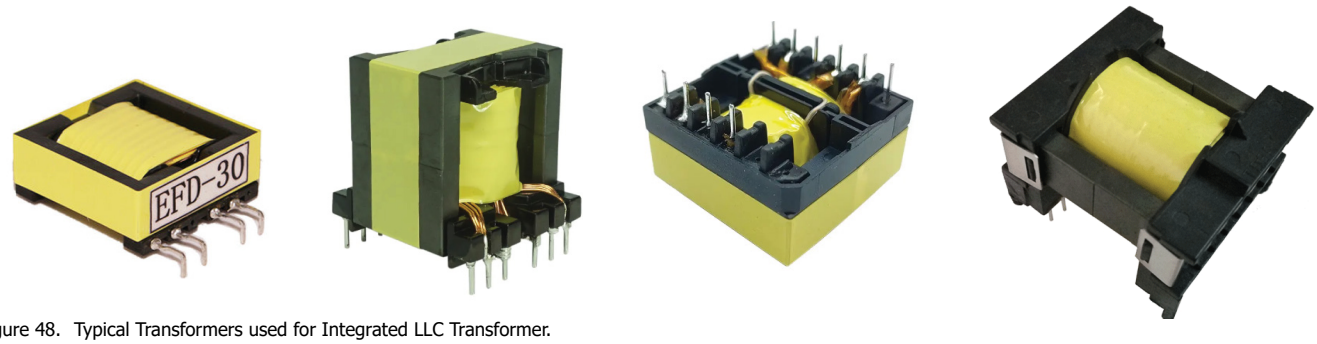


Figure 48. Typical Transformers used for Integrated LLC Transformer.

Using Horizontal Transformer: Simplify IS Winding Termination

If horizontally oriented bobbins similar to image shown in Figure 49 are used, it is possible to simplify IS winding termination. In a vertically oriented bobbin, where the IS winding is wound in the primary chamber and always has to cross the isolation barrier to reach the secondary-side. For a horizontally oriented bobbin, the IS winding wound in the primary chamber can be terminated to the primary side pins of the bobbin which will go down to the PCB. On the PCB, 2 signal traces routed differentially go to the IS components. It is important to ensure creepage and clearance are maintained on the layout.

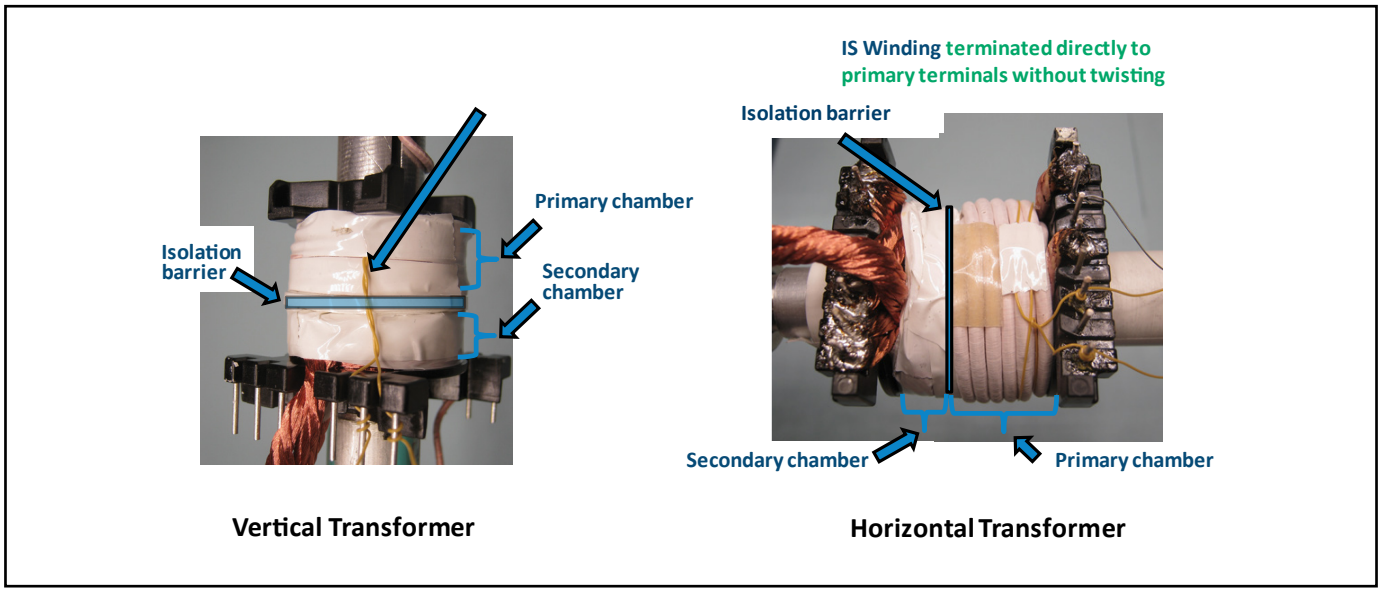


Figure 49. Diagram Showing use of Horizontal Transformer can Simplify IS Construction.

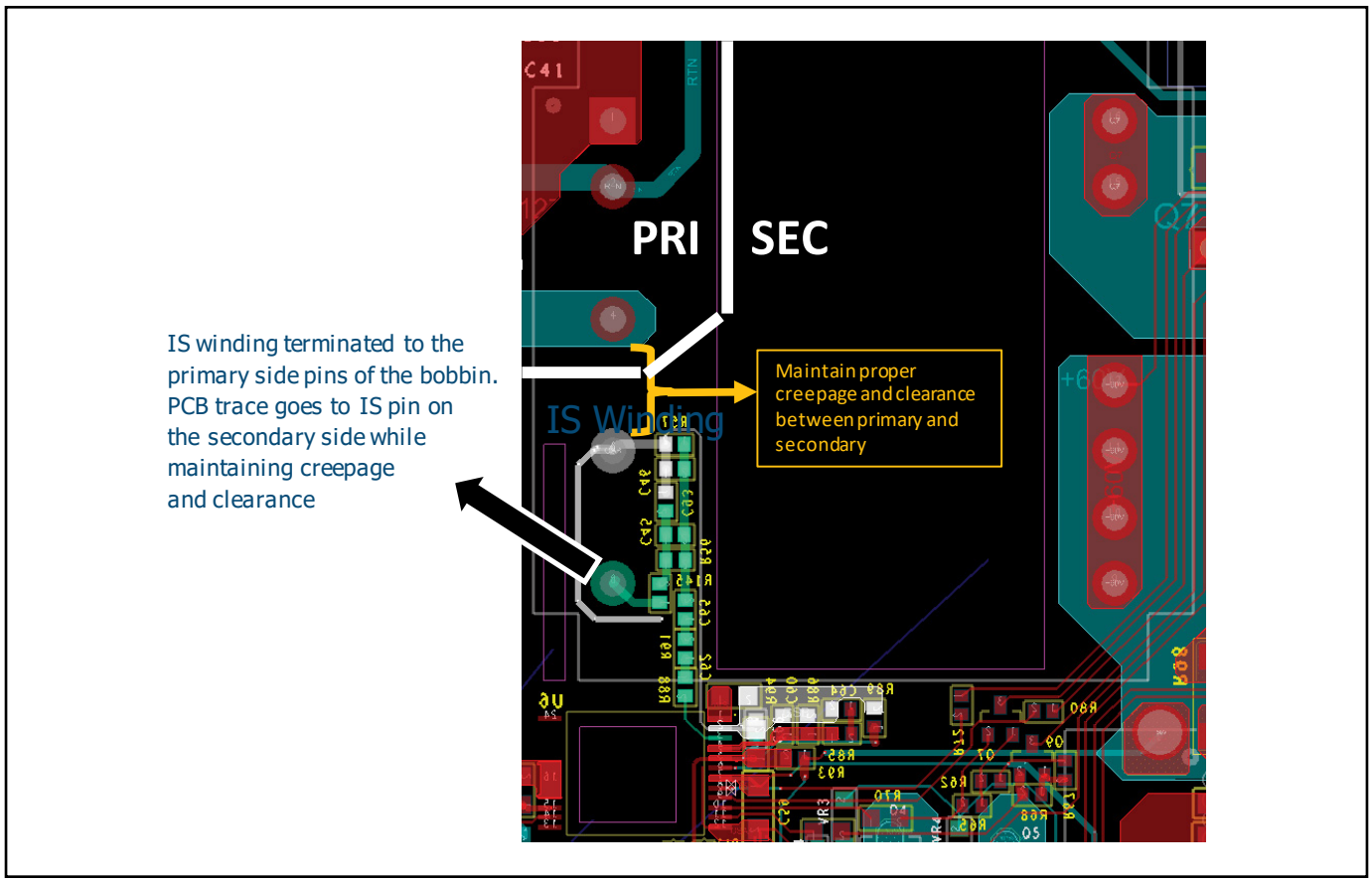


Figure 50. Sample PCB Layout using Horizontal Transformer with IS Winding Terminated in Primary Side.

Using a Signal Transformer in Place of an IS Winding

Another approach is to separate the windings and employ a signal transformer, this will eliminate the need for special IS winding techniques. This can be implemented by placing a small transformer in parallel with the main LLC transformer shown in Figure 51.

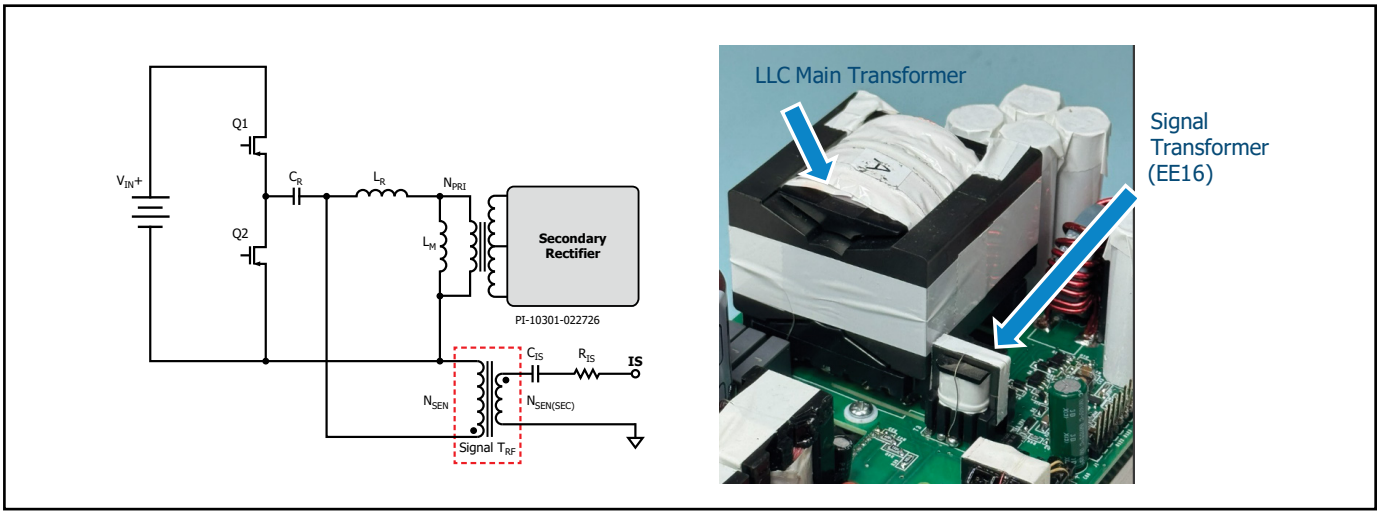


Figure 51. LLC Design using a Signal Transformer.

Guidelines for Design of Signal Transformer

Calculate the number of turns needed to match the core area of the signal transformer. Equation (15) can be used to ensure in the same flux density for the signal transformer as for the main LLC transformer avoiding the possibility of saturation.

$$N_{SEN} = \frac{N_{PRI} A_{PRI}}{A_{SEN}} \quad (15)$$

Where,

N_{SEN}: Signal transformer number of turns

N_{PRI}: Main LLC transformer primary number of turns

A_{PRI}: Main LLC transformer core area

A_{SEN}: Signal transformer core area

Equation 16 shows the calculation of the secondary number or turns. The 30 V value limits the voltage on the secondary winding to prevent unwanted noise due to high dv/dt.

$$N_{SEN(SEC)} = \frac{30\ V \times N_{SEN}}{V_{IN}} \quad (16)$$

Because of the difference between high frequency and low frequency HiperLCS2-HB parts, there is a slight difference in IS current requirement between these when calculating the IS resistor value.

For high frequency devices H003, H004 and H005 use equation (17.1):

$$R_{IS} = \frac{V_{IN} \times N_{SEN(SEC)}}{17\,\mu A \times N_{SEN}} \quad (17.1)$$

For low frequency devices H001 and H002 use equation (17.2):

$$R_{IS} = \frac{V_{IN} \times N_{SEN(SEC)}}{27\,\mu A \times N_{SEN}} \quad (17.2)$$

Where,

R_{IS}: IS resistor value

$N_{SEN(SEC)}$: Number of turns for the signal transformer secondary winding

Note: Calculated R_{IS} value is only the initial value as it may require tuning to match burst threshold requirements. Increasing R_{IS} will increase burst threshold and power limit and vice versa.

R_{IS} Tuning Example

To fine tune the IS resistor value, once the power supply has been built, measure the IS signal waveform directly at the signal transformer secondary winding at nominal input voltage and nominal output power. Measure the step voltage shown in Figure 52 to calculate the IS resistor value.

$$R_{IS} = \frac{V_{STEP}}{17\ \mu A} \quad \text{(for high frequency parts H003, H004 and H005)}$$

$$R_{IS} = \frac{V_{STEP}}{27\ \mu A} \quad \text{(for low frequency parts H001, and H002)}$$

In this example, the step voltage is 22.9 V for an H002 device

$$R_{IS} = \frac{V_{STEP}}{27\ \mu A} = \frac{22.9\ V}{27\ \mu A} \approx 850\ k\Omega$$

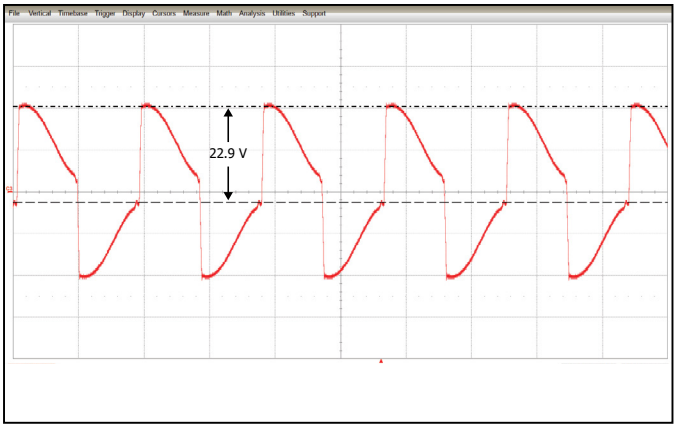


Figure 52. Sample IS Winding Waveform.

To check the burst threshold, monitor the half-bridge voltage with an oscilloscope, start at a load where the LLC is switching at full frequency or continuous switching (i.e. no off-time in the half-bridge voltage). Then, gradually decrease the load until the LLC starts to operate in burst mode. This is easily spotted and will appear as gaps in switching, (use ~5 msec/ div oscilloscope setting)

Figure 53 shows the actual burst threshold results on the example. Full load current is 9.2 A. Burst threshold is typically 10 – 25% of full load, depending on the application:

1st iteration (850 kΩ): Using the calculated 850 kΩ IS resistor resulted on 0.1 A or ~1% burst threshold which is lower than the desired value.

2nd iteration (935 kΩ): increasing IS resistor value by 10% increases burst threshold to 0.2 A (2%) burst threshold which is still low.

3rd iteration (980 kΩ): gives us burst threshold of 1.3 A or 14% which is in the desired range. As shown in Figure 53, decreasing the load from 1.4 A to 1.3 A shows the transition from normal (full frequency) operation to burst mode.

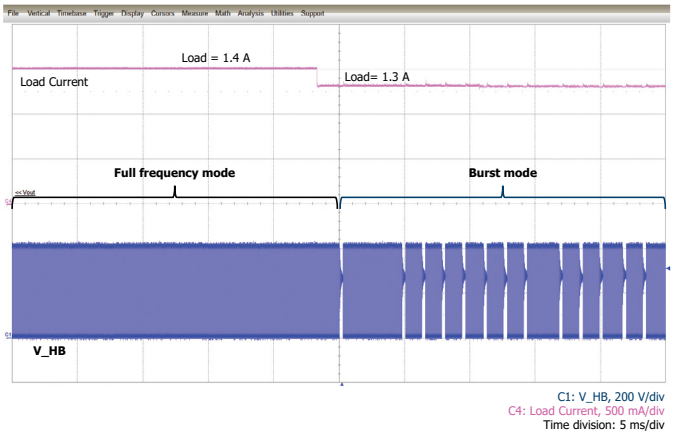


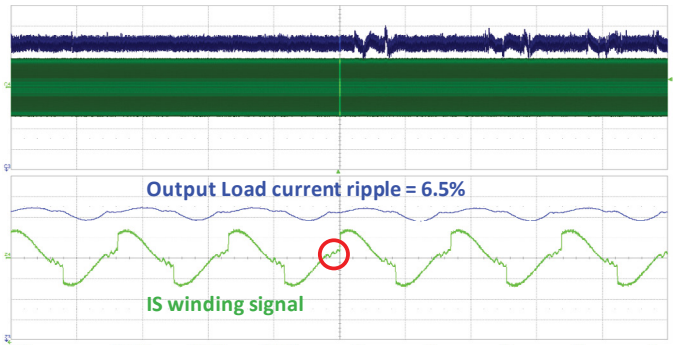
Figure 53. Waveform Showing Transition from Full Frequency to Burst Mode.

Note: When fine tuning the IS resistor values, the PS pin resistor must be 75 kΩ, adjust the IS resistor until burst threshold is ~15% of full load. For applications where <2% threshold is desired, follow the same procedure, but once IS resistor and burst threshold is ~15%, PS pin resistor can be increased from 75 kΩ to 255 kΩ, which this will provide a burst threshold of approximately 2%. This method ensures that the IS pin receives the appropriate operating current.

When using H005 for charger applications, a 255 kΩ PS resistor can be used directly. The IS resistor can be calculated using the equation $R_{IS} = V_{STEP} / 17\ \mu A$. Fine-tune the R_{IS} value as needed to optimize P_{MAX} and the burst threshold.

Figure 54 shows an example of ripple current and IS signal with the conventional IS winding and signal transformer arrangement. Following the IS winding method will result in good ripple performance by adding a small signal transformer (EE16 in this example). It is possible to further reduce ripple current, making this approach suitable for applications requiring very low output ripple. It will also simplify construction of the main transformer.

Using Integrated Current Sense Winding:



Using EE16 Signal transformer:

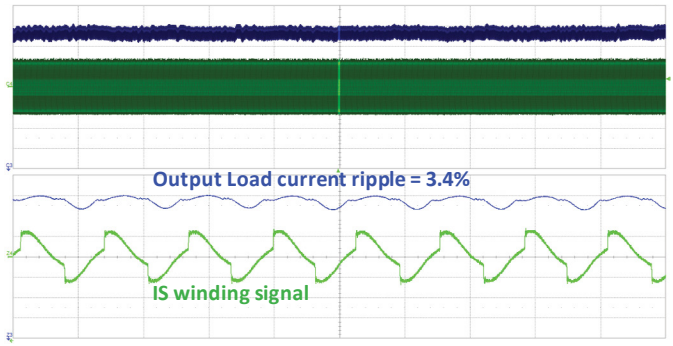


Figure 54. IS Signal Comparison between Typical IS Winding Construction and a Design Employing an IS Signal Transformer.

Layout Guidelines

A good PCB layout will minimize debugging.

Refer to Figure 55 for ground connections. Each ground pin is intended for a different part of the circuit to improve noise immunity. All ground pins are star-connected internally within the device.

Primary-Side Schematic

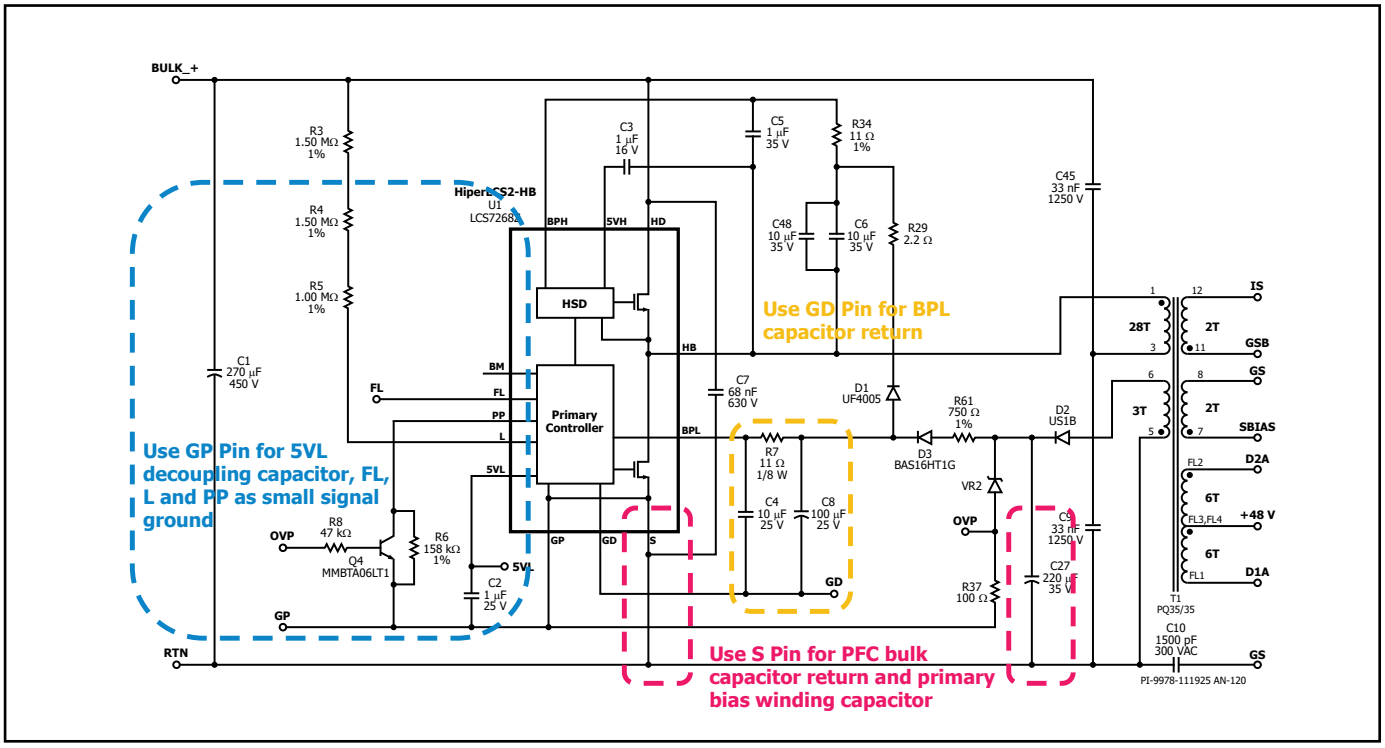


Figure 55. Primary-Side Schematic Recommended Grounding.

Secondary-Side Schematic

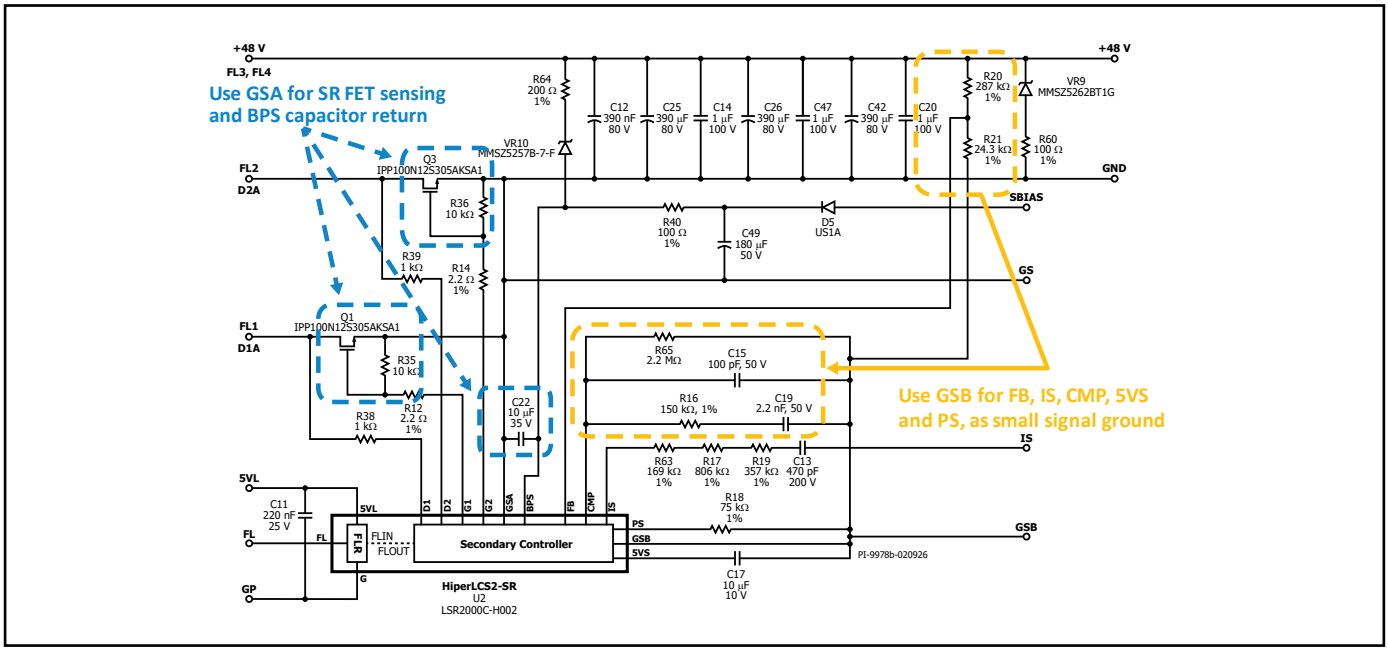


Figure 56. Secondary-Side Schematic Recommended Grounding.

SR MOSFET

The length of the power traces for the 2 phases of the SR MOSFETs should be routed such that they are equal in length. This ensures equal current distribution between the 2 phases resulting in balanced thermal performance. Figure 57 shows the recommended method of sensing the drain voltage of each SR MOSFET. Differential measurement must be implemented, sensing directly at the drain and source of the MOSFET, before going into D1/D2 and GSA pins. Differential sensing improves signal integrity for SR control and minimizes noise due to high dv/dt signals.

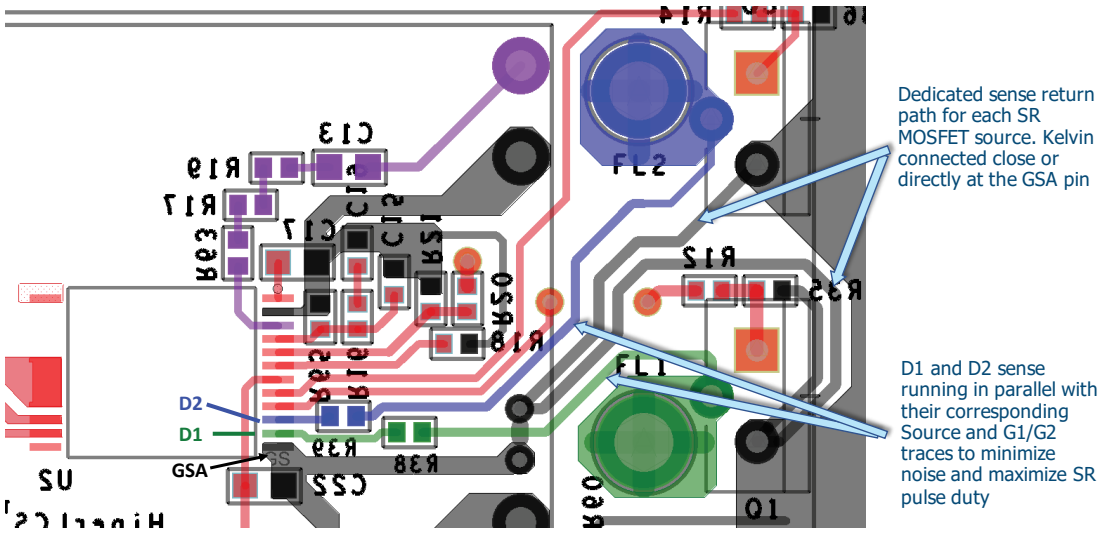


Figure 57. SR MOSFET PCB Layout Guidelines.

IS Signal

The IS signal is a critical control input. Minimizing IS pin noise is a key layout requirement. Route the IS signal trace and components such that there is a short direct path between the controller and the IS pins of the transformer.

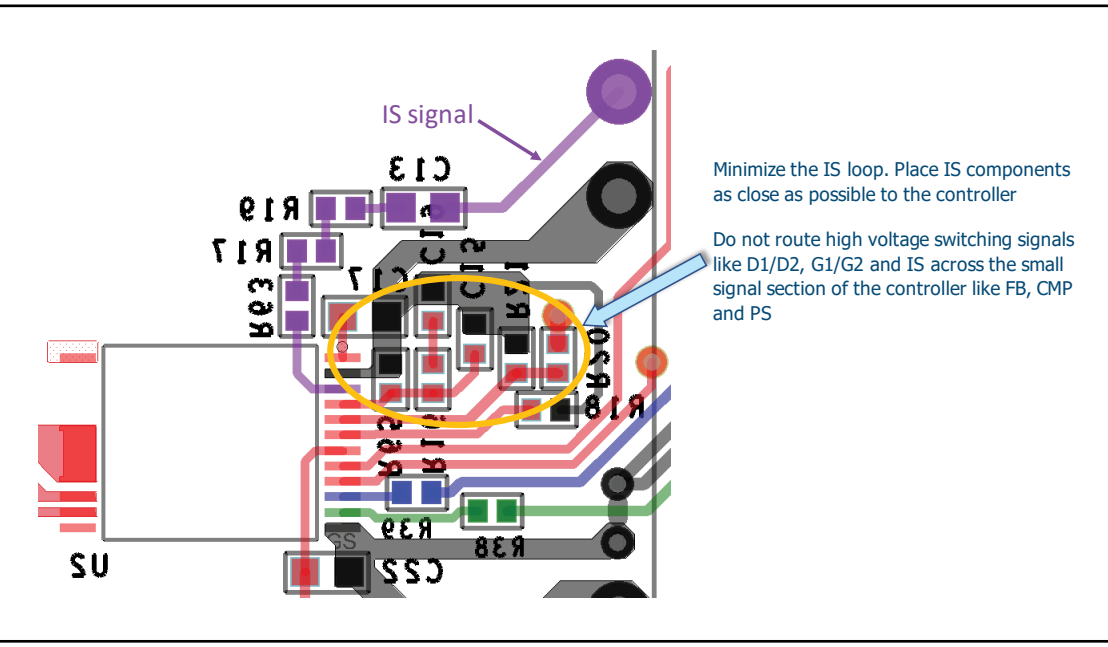


Figure 58. IS Signal PCB Layout Guidelines.

Secondary Signals General Notes

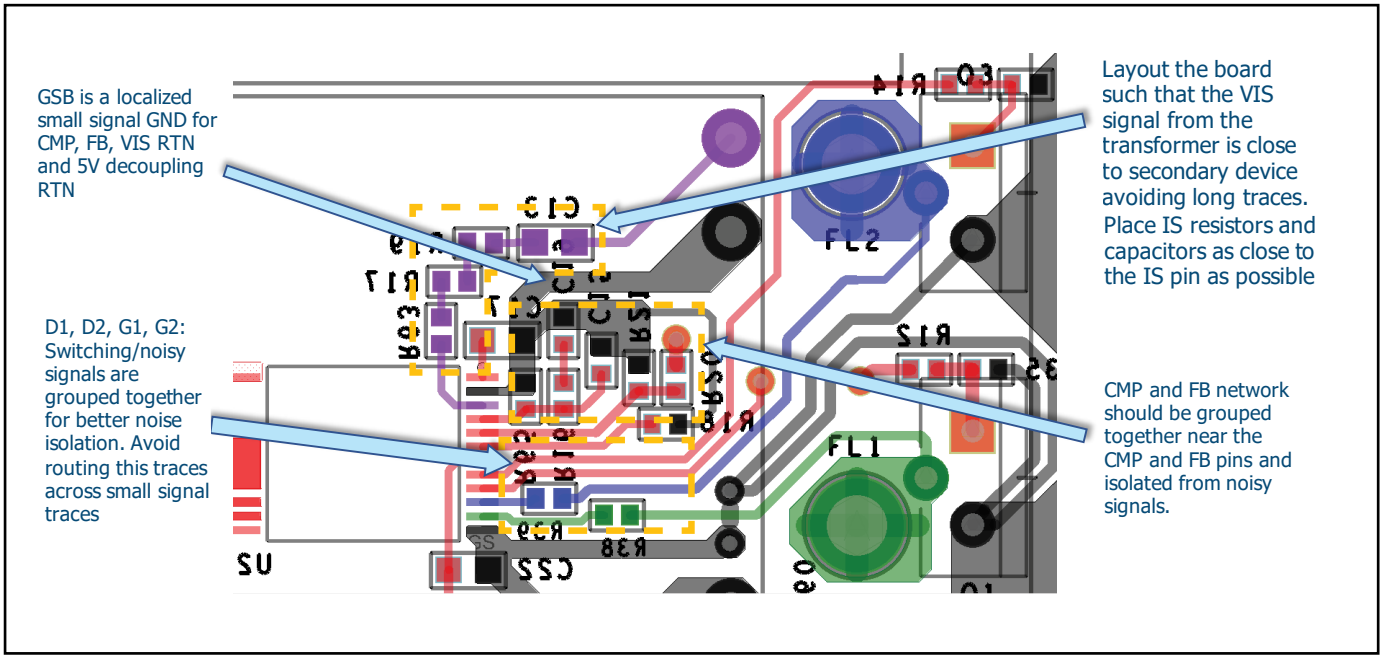


Figure 59. Signal Traces PCB Layout Guidelines.

Placement of Decoupling Capacitors

Place decoupling capacitors as close as possible to the device pins.

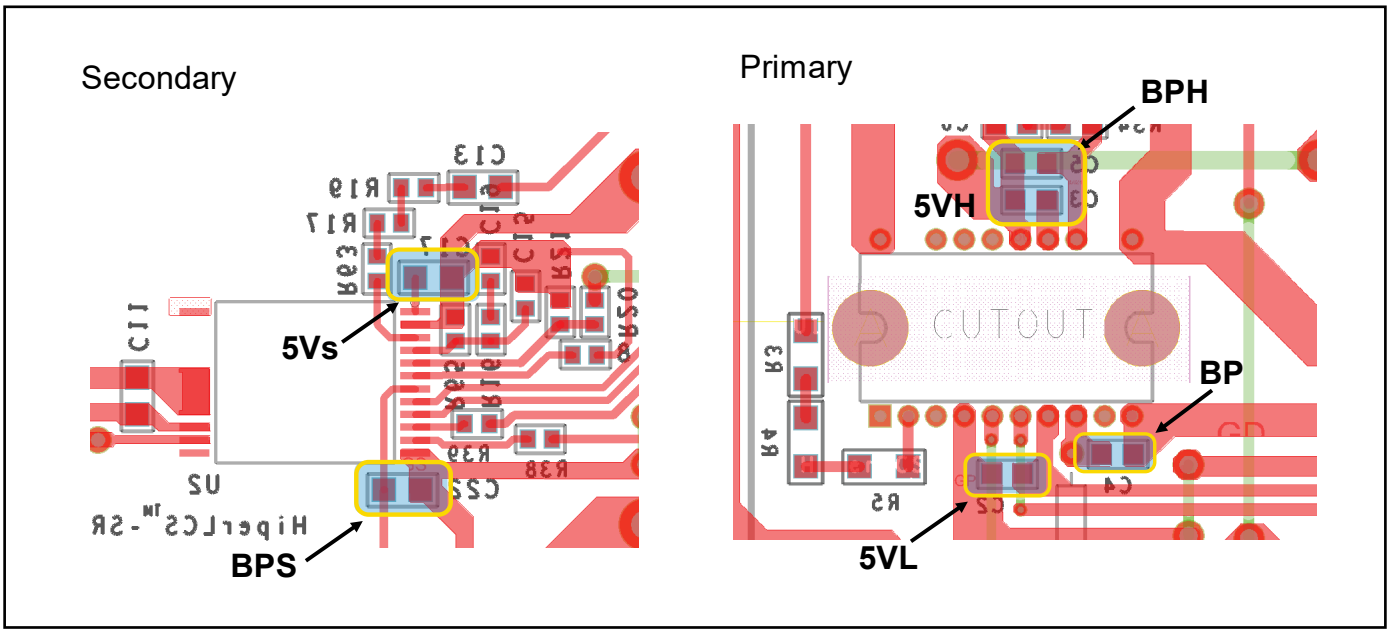


Figure 60. Placement of Decoupling Capacitors on PCB Layout.

Using Horizontal Bobbins

When using horizontal bobbins do not put the controller (LSR2000C) under the transformer, as it would be exposed to fringing flux which could potentially interfere with the secondary-primary FluxLink™ communication.

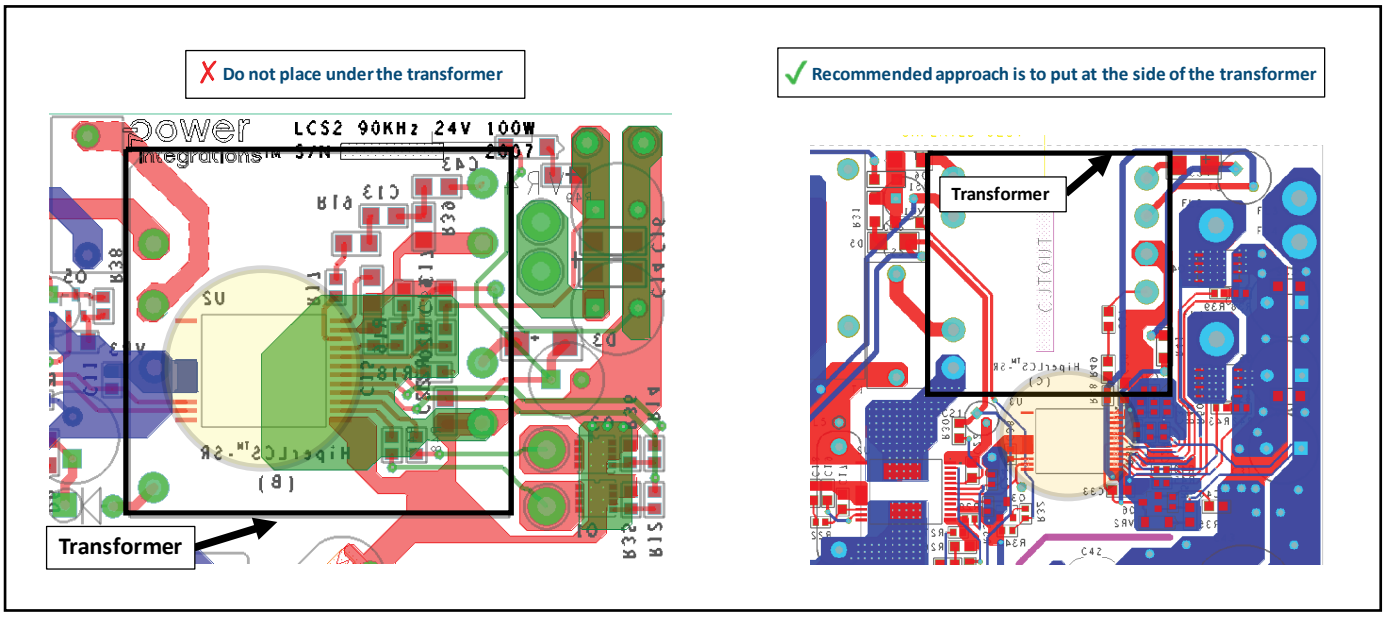


Figure 61. PCB Layout Guidelines on placing LSR2000C with Respect to the Transformer.

Do not Place a Half Bridge Plane on Top of High-Side Drain and/or Ground Plane

Placing a plane connected to HB node on top of a ground plane or drain plane will cause high currents because of the capacitance formed between the 2 planes.

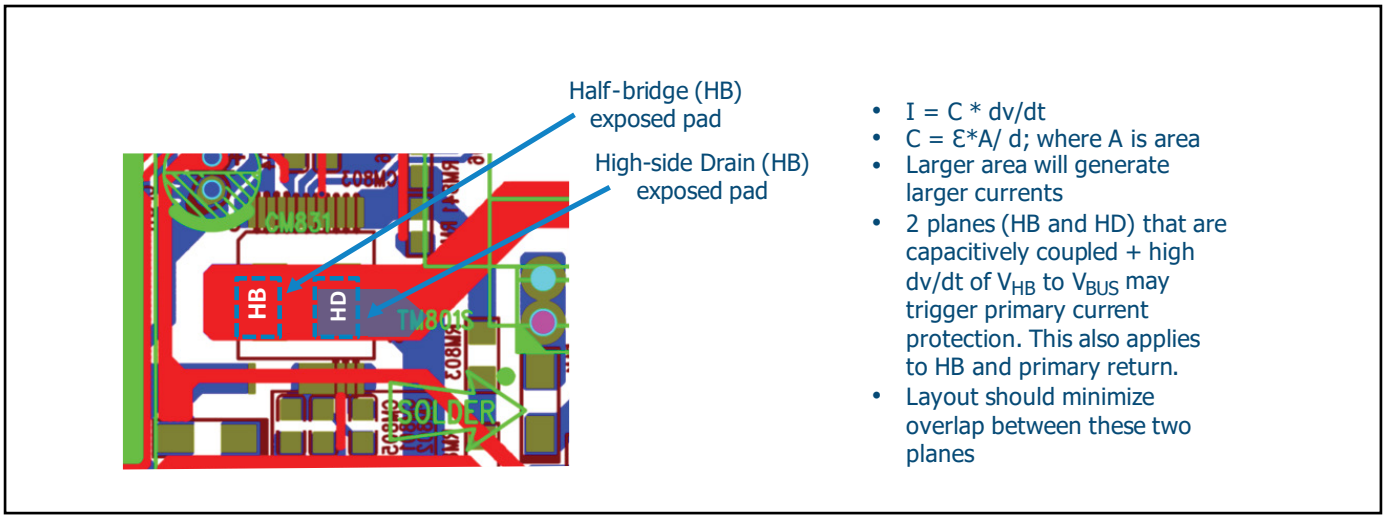


Figure 62. Poor Layout showing Capacitively Coupled Switching Nodes.

L Pin and PP Pin

The L pin is a high impedance pin, and is prone to noise. If noise is coupled into this trace then it can mistrigger Line OV/UV which can momentarily terminate switching midcycle and if sustained it will trigger a shutdown. To avoid this keep the trace as short as possible and away from any noisy traces.

Similarly the PP pin is a high impedance pin, keep it away from noisy signals as this may corrupt PP discovery during start up which will cause the primary controller to select a different frequency mode triggering a frequency confirmation error.

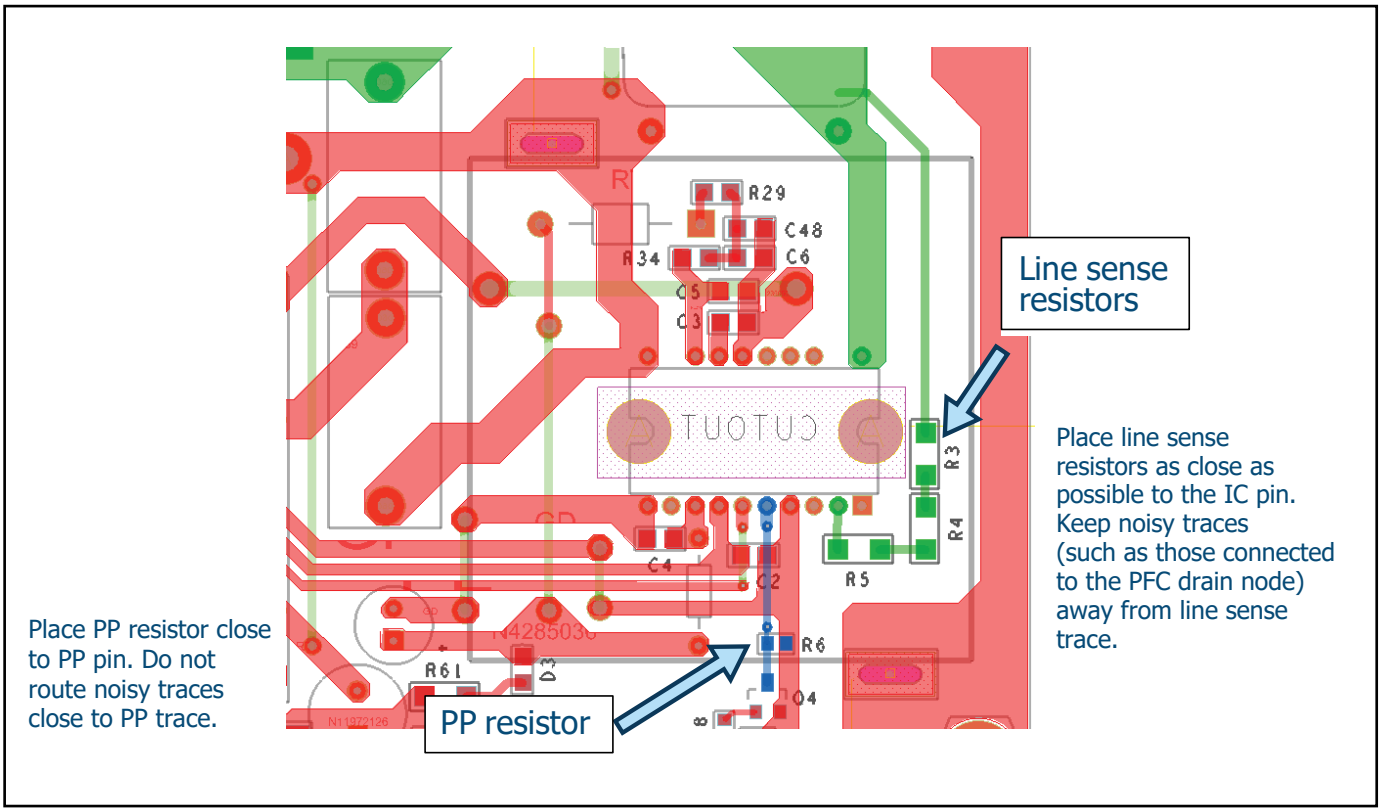


Figure 63. Layout Guidelines for Positioning the L Pin and PP Pin Resistors.

Revision	Notes	Date
A	Initial release.	02/26
B	Additional updates made to equations and Figures.	03/26

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