# Application Note AN-113
# InnoMux2-EP & BL Family

Design Guide

## InnoMux-2 PSU Design Guidelines and Considerations

This application note provides design guidelines and key considerations for using the InnoMux™-2 product family. It should be read in conjunction with Application Note AN-72: InnoSwitch™-3 family, as the primary-side circuit of InnoMux-2 shares the same architecture as the InnoSwitch3 IC family.

## Design Specifications

### Configuration Selection

#### CV + CC Configurations

The circuit in Figure 1 illustrates a single-stage, multi-output flyback converter with one constant voltage (CV) and one constant current (CC) output. This configuration is suitable for applications requiring display functionality. The InnoMux-2 architecture enables high-efficiency by eliminating downstream DC-DC converters, while independently and accurately regulating both CV and CC outputs. High output accuracy is achieved by controlling the selection MOSFET (Q1) on the CV1 output to direct power only to the output which requests it. The CC output supports various 2-pin dimming modes, including straight PWM dimming, analog/hybrid dimming and filtered PWM/hybrid dimming.

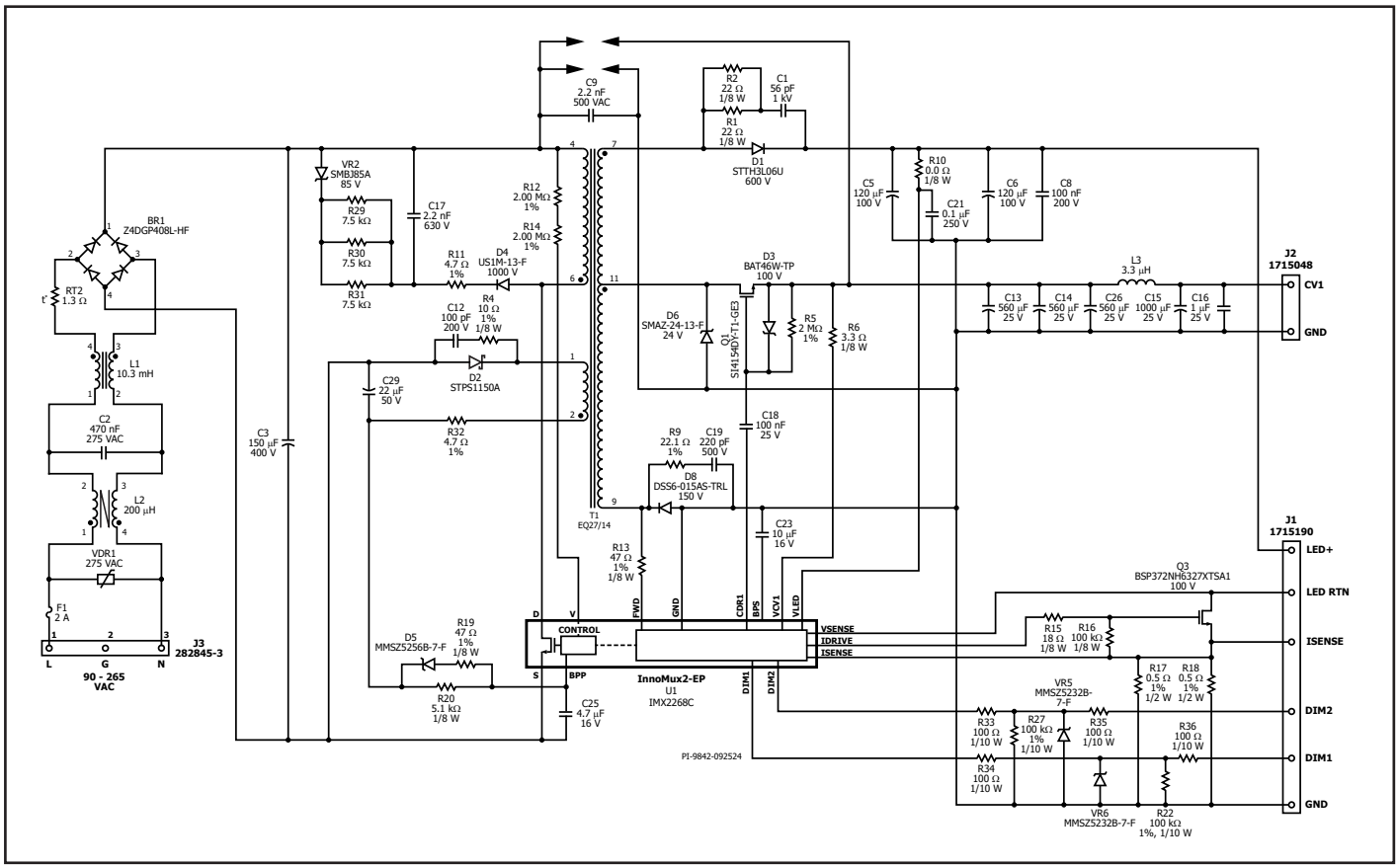



Figure 1. Application Example Schematic (1 CV + 1 CC).

For a comprehensive design example report, refer to DER-714: 52 $W_{NOM}$ and 82 $W_{PK}$ Power Multi-Output Flyback Converter with One CV and One CC Using InnoMuxTM2-EP IMX2268C.

https://www.power.com/design-support/design-examples/der-714-52-w-nominal-82-w-peak-multi-output-flyback-power-supply-32-tv-using-innomux2-ep

The circuit in Figure 2 demonstrates an application with one CV and four CC (LED) outputs using the InnoMux-2 companion chip IMX204DG for accurate current matching between the LED outputs.

This configuration can be expanded to 1 CV + 8 CC by incorporating an additional IMX204DG IC. The application employs a 1-pin dimming mode and supports various dimming configurations, including straight PWM dimming, analog dimming, and filtered PWM dimming.

For a comprehensive design example report, refer to DER-715: 24 W Multi-Output Flyback Converter with One CV and Four CC Outputs Using InnoMuxTM2-BL IMX2065C and the LED Backlight Controller IC IML204DG

https://www.power.com/design-support/design-examples/der-715-24-w-multi-output-flyback-power-supply-pc-monitor-using-innomux2-bl

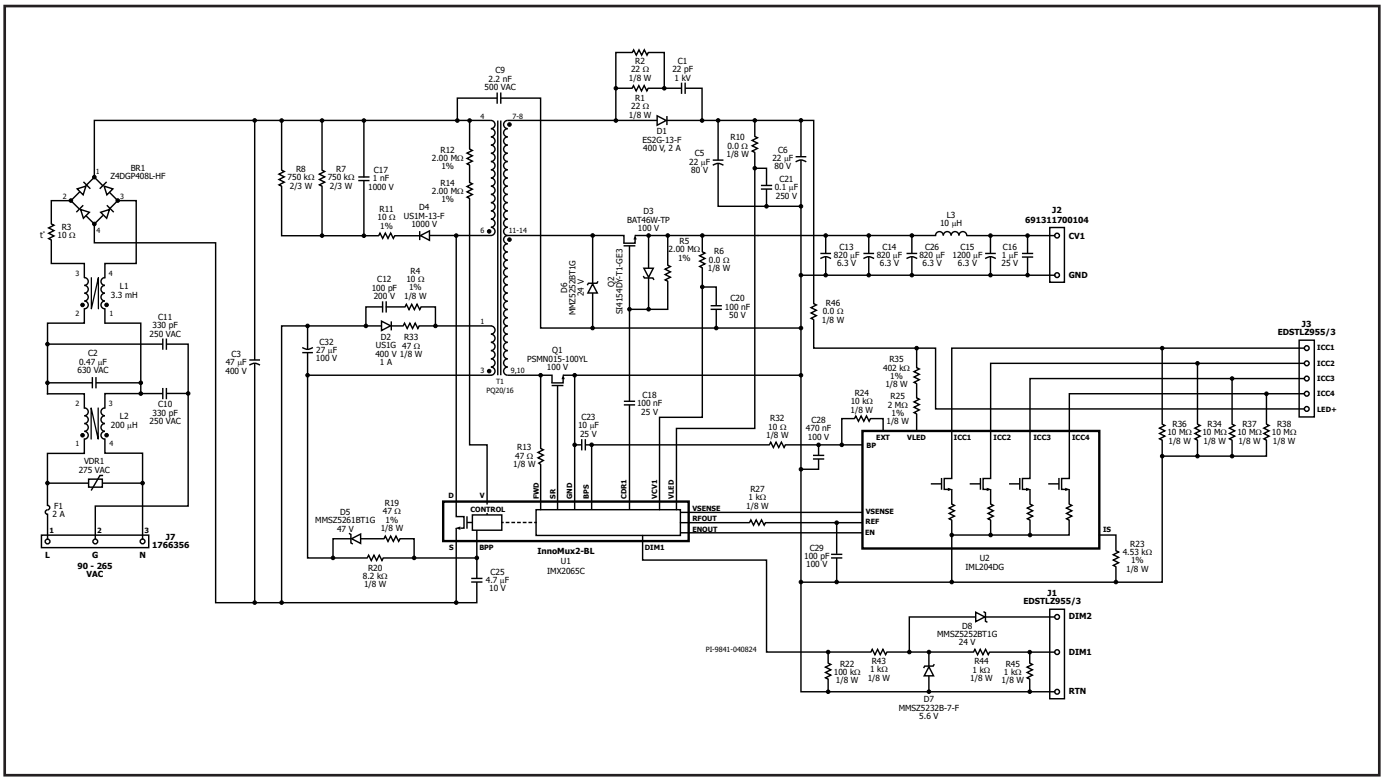



Figure 2. Application Example Schematic (1 CV + 4 CC).

### Multi-CV Output Configurations (Up to 3 CV Outputs)

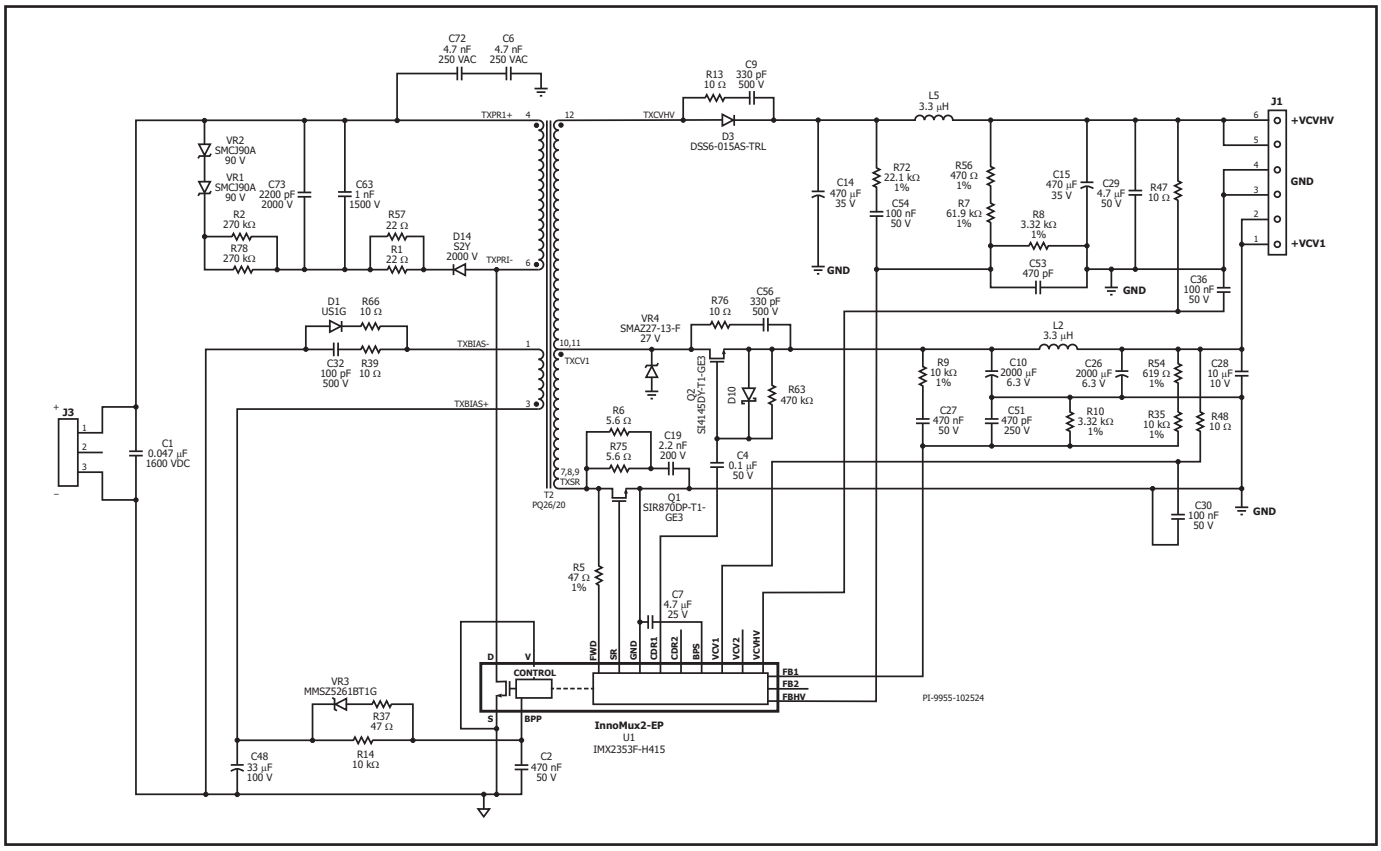



Figure 3. Application Example Schematic (2 CV).

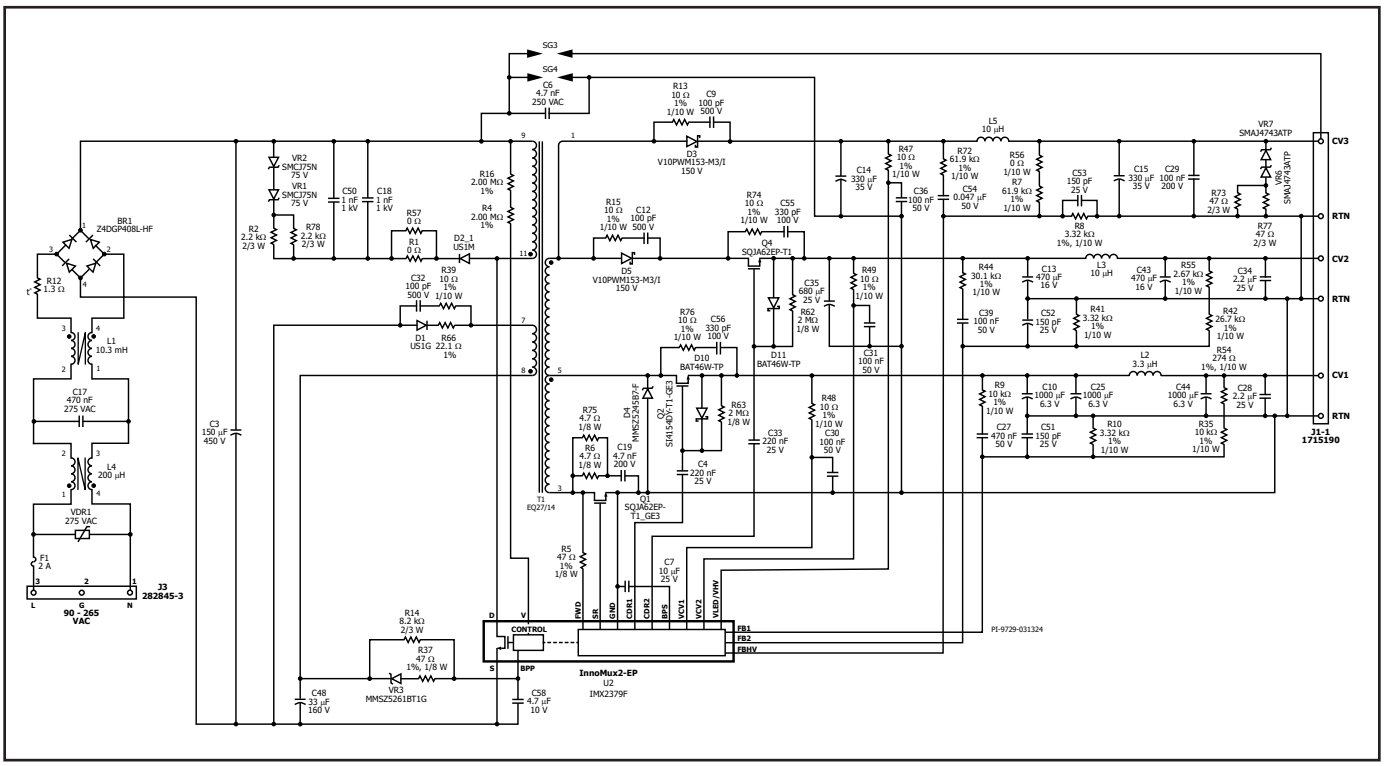



Figure 4. Application Example Schematic (3 CV).

Figure 3 and Figure 4 illustrate CV-only configurations supporting up to three independently regulated CV outputs. As shown in Figure 4, rectifier diodes are inserted on the CV2 and CVHV outputs. When these outputs operate at low voltage and high current, the power loss across the diodes can reduce system efficiency. To maximize efficiency, CV1 should be designated as the lowest voltage, high-power output to ensure that most secondary conduction loss occurs on MOSFETs rather than diodes.

For comprehensive design example reports, refer to RDR-1053: 60 W Flyback Converter with Two Independently Regulated Outputs Using InnoMuxTM2-EP IMX2353F-H415

https://www.power.com/design-support/design-examples/rdr-1053-60-w-dual-output-flyback-power-supply-1000-vdc-industrial-using-innomux2-ep-1700v-powigan

DER-716: 62 W Multi Output Flyback Converter with 3 CV Outputs Using InnoMuxTM2-EP IMX2379F and

https://www.power.com/design-support/design-examples/der-716-62-w-nominal-power-multi-output-flyback-power-supply-appliances-using-innomux2-ep

## LED Maximum and Minimum Voltages

LED maximum and minimum voltages are critical parameters in transformer design. Some applications specify only the typical LED string voltage $V_{LED\_TYP}$ at the maximum LED current. However, due to LED string tolerances, the actual maximum LED voltage can be 10% higher than the typical value. To account for this, the suggested maximum LED voltage should be set to 110% of $V_{LED\_TYP}$. The minimum LED voltage depends on the minimum load current through the LED string, which can reduce the LED string voltage by up to 20%. Unless otherwise specified, the minimum LED voltage is recommended to be 80% of $V_{LED\_TYP}$.

$$V_{LED\_MAX} = 110\% \times V_{LED\_TYP}$$
$$V_{LED\_MIN} = 80\% \times V_{LED\_TYP}$$

## VSENSE Voltage

VSENSE Voltage is the regulation target across the drain and source of the LED drive MOSFET. To ensure optimal performance and efficiency, the specified $V_{SENSE}$ voltage must always exceed the MOSFET's on-state voltage drop. This prevents the MOSFET from entering its saturation region, ensuring proper LED driver operation.

## Feedback Configuration

InnoMux-2 supports both internal and external feedback configurations. For configurations with LED outputs (IMX22xxC/F or IMX20xxC), the CV1, CV2 and VLED outputs do not have dedicated feedback pins and their voltages are predefined as shown in Table 1 and Table 2.

For 2CV and 3CV standard parts, external feedback is used for design flexibility, but these can also be trimmed to internal feedback to reduce standby power consumption. To extend power range, the 2CV parts (IMX2174/5/6/7F) can be trimmed to function as 3CV, while the 3CV parts (IMX2378/9/0F) can be trimmed to function as 2CV parts. For more details on trim options, please contact the local Power Integrations sales office.

## Configuration Options

| Part Number | BV Rating | Continuous Power[1] | Output with IML204DG | CV1 | Maximum $V_{LED}$ | $V_{SENSE}$ Voltage | SR MOSFET Driver | Dimming Interface | Package |
|---|---|---|---|---|---|---|---|---|---|
| IMX2065C | 650 V | 22 W | 1 CV, 4 CC | 5 V | 60 V | 0.3 V | Yes | 1-Pin Filtered PWM Dimming | InSOP-24D |
| IMX2066C | 650 V | 27 W | 1 CV, 4 CC | 5 V | 60 V | 0.3 V | Yes | 1-Pin Filtered PWM Dimming | InSOP-24D |

Table 1. InnoMux2-BL Configuration Options.

1. 85 – 265 VAC.

## Configuration Options

| Part Number | Switch Rating | Continuous Power | Peak Power | Output | CV1 | Maximum $V_{LED}$ | $V_{SENSE}$ Voltage | SR MOSFET Driver | Dimming Interface | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| IMX2267C | 650 V | 36 W | 57 W | 1 CV, 1 CC | 12 V | 80 V | 0.8 V | No | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-24B |
| IMX2268C | 650 V | 50 W | 80 W | 1 CV, 1 CC | 12 V | 80 V | 0.8 V | No | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-24B |
| IMX2278F | 750 V | 60 W | 94 W | 1 CV, 1 CC | 12 V | 140 V | 0.9 V | Yes | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-T28B |
| IMX2279F | 750 V | 70 W | 110 W | 1 CV, 1 CC | 12 V | 150 V | 1.0 V | Yes | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-T28B |
| IMX2270F | 750 V | 80 W | 130 W | 1 CV, 1 CC | 12 V | 170 V | 1.0 V | Yes | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-T28B |
| IMX2079C | 750 V | 70 W | 110 W | 1 CV, 1 CC | 12 V | 150 V | 1.0 V | Yes | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-24D |
| IMX2070C | 750 V | 80 W | 130 W | 1 CV, 1 CC | 12 V | 170 V | 1.0 V | Yes | 2-Pin Filtered PWM/ Hybrid Dimming | InSOP-24D |

Table 2. InnoMux2-EP Configuration Options.

### Peak Load in TV Applications

In TV applications, peak current capability is essential for driving audio loads such as speaker. As shown in Figure 5, a typical 50" TV power supply unit (PSU) with an average load current of 2.4 A on the 12 V output can experience peak currents reaching 5.3 A. Transformer design must account for this peak current to prevent core saturation. Additionally, maximum switching frequency and voltage stress tests should be conducted under peak load conditions to endure reliable operation.

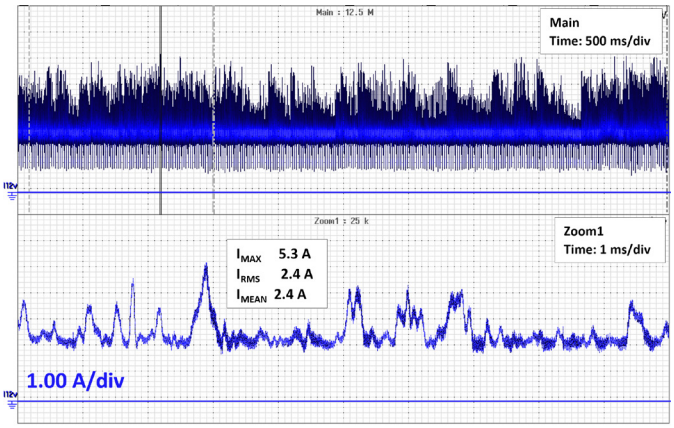



Figure 5. Peak Current on Speaker Application.

### Transformer Turns Design Principle

The transformer can be designed with independent secondary windings, stacked windings, or a combination of both. To ensure power is delivered only to one output at a time, the induced voltage on the top output $V_{CVHV/LED}$ must be high enough when the selection FET is turned on to keep the top diode reverse-biased. This condition is critical for proper operation of the topology and requires the turns ratio of the transformer to meet the following condition:

$$\frac{V_{CV1}}{N_{CV1}} \leq \frac{V_{CV2}}{N_{CV2}} < \frac{V_{CVHV/LED}}{N_{CVHV/LED}}$$

Where $V_{CV1}$, $V_{CV2}$, $V_{CVHV/LED}$ represent the voltages across the CV1, CV2 and CVHV/LED windings during their respective conduction intervals; $N_{CV1}$, $N_{CV2}$, $N_{CVHV/LED}$ are the number of turns in each winding. For PSUs designed to support LED strings with a wide voltage range, or those intended for use with multiple LED string configurations, $V_{CVHV/LED}$ should be set to the minimum LED voltage across the range. Additionally, to minimize audible noise, $V_{CV2}/N_{CV2}$ should be kept as close to $V_{CV1}/N_{CV1}$ as possible. This reduces flux density deviation in each switching cycle.

## Reflected Voltages of Multiple Outputs

### Peak Drain Voltage Considerations

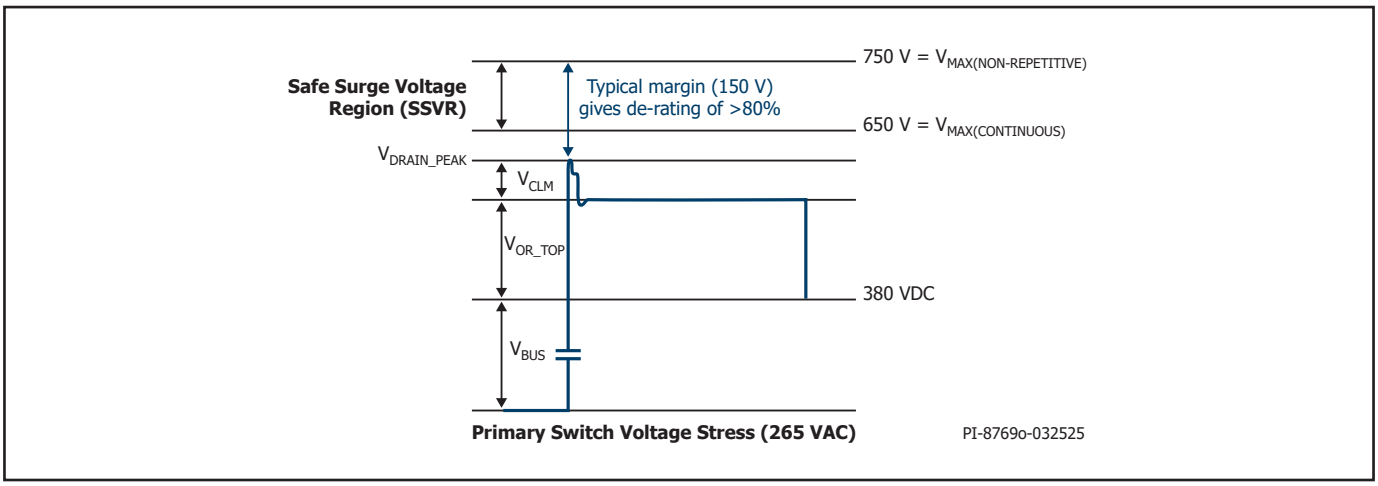



Figure 6. Peak Drain Voltage for 265 VAC Input Voltage using 750 V PowiGaN Switch.

Figure 6 illustrates the peak drain voltage $V_{DRAIN\_PEAK}$ for a 265 VAC input using a 750 V PowiGaN switch. The reflected voltage of the top output $V_{OR\_TOP}$ appears across the primary winding when the secondary is conducting, while $V_{BUS}$ is the rectified DC rail voltage.

In addition to $V_{BUS}$ + $V_{OR\_TOP}$, the primary switch drain experiences a voltage spike $V_{CLM}$ at turn-off due to the energy stored in the leakage inductance of the primary winding. A clamp circuit across the primary winding is required to prevent the drain voltage from exceeding its maximum continuous rating. The forward recovery of the clamp diode can also introduce a momentary spike at the moment of primary switch turn-off. The total peak drain voltage is therefore given by:

$$V_{DRAIN\_PEAK} = V_{BUS} + V_{OR\_TOP} + V_{CLM}$$

To ensure long-term reliability and robustness, $V_{OR}$ and $V_{CLM}$ should be selected such that the peak drain voltage remains below $V_{MAX(CONTINUOUS)}$ under all normal operating conditions. This provides sufficient margin to handle voltage surges, ensuring the peak drain voltage stays below $V_{MAX(NON-REPETITIVE)}$ during abnormal transient conditions.

### Recommended $V_{OR}$ and $\Delta V_{OR}$

The choice of $V_{OR}$ not only affects voltage margin on primary switch but also impacts system efficiency.

Table 3 shows the typical recommended range of $V_{OR}$ based on the output voltage:

| Output Voltage | Recommended Range for $V_{OR\_CV1/CV2}$ | Recommended Range for $V_{OR\_CVHV/LED}$ |
|---|---|---|
| 5 ~ 12 V | 45 – 70 V | |
| 12 V ~ 24 V | 60 – 100 V | 100 – 130 V |
| >24 V | | 135 – 180 V |

Table 3. Recommended $V_{OR}$ Selection Range.

During transient conditions, if the voltage spike on the CVHV/LED winding exceeds the output voltage, a momentary flow of current (known as overspill) may occur in the CVHV/LED winding, even when CV1 output is selected (CV1 selection FET on).

The difference in $V_{OR}$ between LED/CVHV and CV1 or CV2 is referred to as $\Delta V_{OR}$. To minimize overspill effect, a sufficient $\Delta V_{OR}$ is recommended. This allows the overspill current to be quickly redirected from LED/CVHV to CV1 or CV2 output. This also helps avoid primary turn-on while the secondary current is still flowing through the LED/CVHV diode, thereby reducing the risk of large reverse recovery currents in the top diode.

| Configuration | Required $V_{OR}$ | Recommended $\Delta V_{OR}$ |
|---|---|---|
| 2CV | $V_{OR\_CV1} < V_{OR\_CVHV}$ | $\Delta V_{OR} = V_{OR\_CVHV} - V_{OR\_CV1}$ = (30% ~ 60%) $V_{OR\_CVHV}$ |
| 3CV | $V_{OR\_CV1} \leq V_{OR\_CV2} < V_{OR\_CVHV}$ | $\Delta V_{OR} = V_{OR\_CVHV} - V_{OR\_CV2}$ = (30% ~ 60%)$V_{ORCVHV}$ |
| 1CV1CC or 1CV4CC | $V_{OR\_CV1} < V_{OR\_LED\_MIN} < V_{OR\_LED\_MAX}$ | $\Delta V_{OR} = V_{OR\_LED\_MIN} - V_{OR\_CV1}$ = (5% ~ 40%) $V_{OR\_LED\_MAX}$ |

Table 4. Recommended $\Delta V_{OR}$ for Various Configurations.

### Key Considerations for $V_{OR}$ Design

1. Higher $V_{OR}$ allows increased power delivery at $V_{MIN}$.
2. Higher $V_{OR\_CV1}$ reduces the voltage stress on the SR MOSFET.
3. Higher $V_{OR\_CV2}$ reduces the voltage stress on the CV2 output diode.
4. Higher $V_{OR\_CVHV}$ reduces the voltage stress on the CVHV output diode.
5. For a given $V_{OR\_CVHV/LED}$, a larger $\Delta V_{OR}$ reduces overspill power and improves CVHV/LED regulation accuracy.
6. Higher $V_{OR}$ may increase leakage inductance, reducing efficiency.
7. Higher $V_{OR}$ increases peak and RMS current on the secondary winding, which can increase copper and diode losses.
8. For a given $V_{OR\_CVHV/LED}$, a larger $\Delta V_{OR}$ reduces $V_{OR\_CV1}$ and $V_{OR\_CV2}$, which may lead to Continuous Conduction Mode (CCM) at high input voltages.

## Synchronous Rectifier (SR) MOSFET

In the InnoMux-2 circuit, the Synchronous Rectifier (SR) MOSFET plays a crucial role in replacing traditional diode rectifiers, significantly improving efficiency and thermal performance. The InnoMux-2 SR driver introduces two key features: FWD voltage regulation and Zero Voltage Switching (ZVS).

### FWD Voltage Regulation with SR Gate Voltage Control

As shown in Figure 1, SR drain-source voltage is sensed via the FWD pin of InnoMux-2. To ensure optimal performance and prevent early turn-off of the SR MOSFET, FWD voltage regulation control is implemented. This feature not only improves noise immunity on the FWD pin but also allows designers to select an SR MOSFET with a lower $R_{DS(ON)}$, improving power efficiency.

At the beginning of secondary discharge, current initially flows through the body diode of the SR MOSFET. InnoMux-2 then turns on the SR gate drive, redirecting current through the MOSFET's low $R_{DS(ON)}$ path. InnoMux-2 regulates the FWD voltage to -25 mV, improving the noise immunity of the FWD signal. Consequently, the SR gate voltage decreases from its maximum (~5 V) to near the threshold voltage (~2 V) to maintain this $V_{FWD}$ regulation voltage. As illustrated in Figure 7, $I_{SEC}$ is the secondary discharge current through the SR MOSFET.

- From t0 to t1: The discharge current flows through the CVHV/LED outputs.
- At t1: The current is redirected to the lower output. $I_{SEC}$ increases due to the transformer turns ratio difference between the outputs. This causes the SR gate voltage to increase, maintaining the -25 mV FWD voltage.
- From t1 to t2: As the discharge current decreases, the gate voltage gradually reduces, ensuing -25 mV regulation on the FWD pin until the end of the secondary discharge.

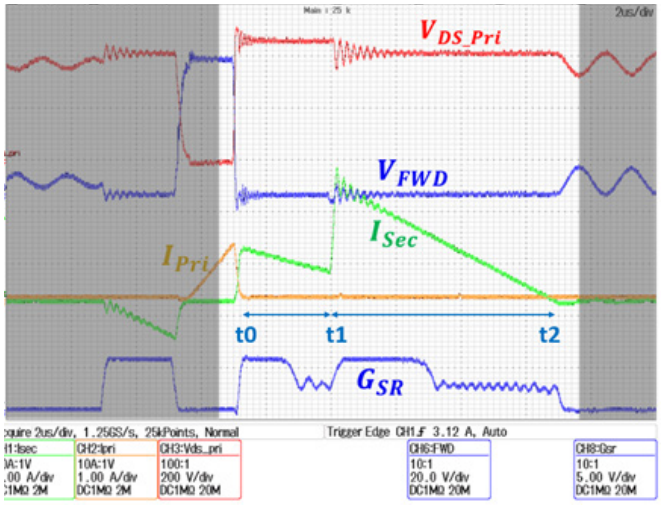



Figure 7. FWD Pin Regulation With SR Gate Voltage Control.

## Zero Voltage Switching (ZVS) Operation

Zero Voltage Switching on the primary switch is achieved by leveraging the existing SR, known as SR-ZVS. Before the primary switch turns on, the SR MOSFET is briefly turned on, generating a reverse discharge current through the bottom output winding (CV1). After the SR MOSFET turns off, this current is commutated back to the primary side, flowing from the source to the drain of the primary switch and discharging the voltage across its body capacitance. As illustrated in Figure 8, the drain-source voltage of the primary switch $V_{DS\_Pri}$ rings down to nearly zero just as the primary switch turns on, effectively eliminating turn-on losses and improving power efficiency by more than 1% in certain applications. Notably, SR-ZVS is only available when the PSU operates in Discontinuous Conduction Mode (DCM) due to the necessity of the reverse current.

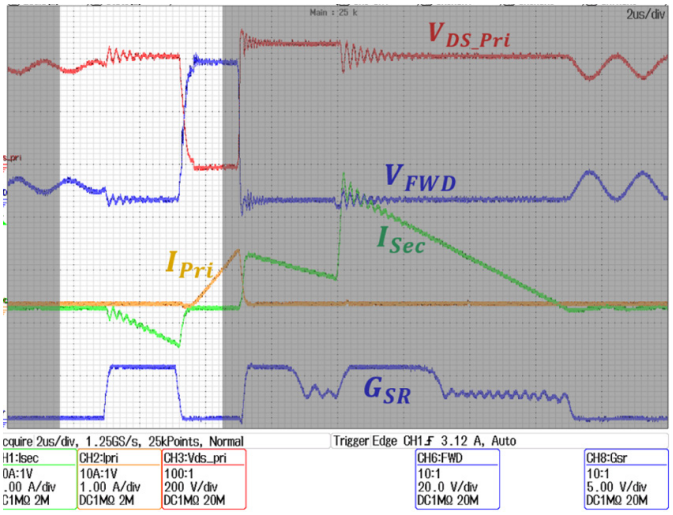



Figure 8. SR-ZVS Operation.

In 1CV1CC or 1CV4CC applications, VLED is not actively regulated by InnoMux-2 when the LED string is not enabled. Instead, $V_{LED}$ is determined by the transformer turns ratio and $V_{CV1}$. To optimize standby power consumption, SR-ZVS is disabled in this state, preventing secondary reverse current from charging the LED output. For 2CV or 3CV applications using a MOSFET primary switch, ZVS is paused when the primary switching frequency drops below 15 kHz. However, when using a GaN primary switch, ZVS remains enabled at all times.

SR turn-on time and primary switch discharge duration depend on multiple factors, including input voltage, transformer magnetizing inductance and system equivalent capacitance. SR-ZVS utilizes an adaptive control method, with InnoMux-2 continuously calculating and adjusting parameters to maintain optimal operation. Users do not need to modify any settings, as InnoMux-2 automatically controls the SR-ZVS operation for optimal performance. To ensure accurate ZVS implementation, the following conditions must be met:

- The FWD plateau voltage should be less than 100 V to ensure accurate measurement by InnoMux-2. The minimum primary on-time must exceed 500 ns to ensure the plateau is large enough to measure. The minimum on-time can be measured under no-load operation with maximum input voltage.
- SR-ZVS can only be implemented in DCM operation. It is recommended that the steady-state $K_{RP}$ be greater than 1.2 at high mains input.

### SR FET Selection and Snubber Circuit Design

When the primary switch turns on, the transformer winding polarity reverses, and the leakage inductance of the output windings, combined with the SR FET's capacitance ($C_{OSS}$), produces ringing across the SR FET's drain-source. This ringing can be suppressed by an RC snubber across the SR FET. A snubber resistor in the range of 4.7 Ω to 22 Ω is recommended. Higher resistance values may lead to a noticeable drop in efficiency. A snubber capacitance between 1 nF and 4.7 nF is typically suitable for most designs.

When the primary switcher turns on, a fast-rising voltage is transferred to the secondary winding via the transformer, appearing across the drain- source of the SR FET. This high dv/dt, coupled with a high $C_{GD}/C_{GS}$ ratio in the MOSFET capacitances, can induce an unwanted gate-source voltage on the SR FET. If the induced gate voltage exceeds the minimum gate threshold voltage $V_{GS(TH)}$, it maybe turn on the SR FET, causing cross-conduction and potentially leading to catastrophic failure. To mitigate this risk, the recommended $C_{GD}$ ($C_{RSS}$) should be less than 35 pF, and the ratio of $C_{RSS}/C_{ISS}$ should remain below 2%.

Another critical factor in SR FET selection is the reverse recovery time ($T_{RR}$) of its body diode. The reverse recovery characteristics of the SR FET's body diode significantly impact the voltage stress on the drain when the primary MOSFET switches on. An SR FET with a slow body diode (i.e., $T_{RR}$ > 40 ns) will experience considerably higher voltage stress compared to one with a fast body diode. Therefore, the recommended maximum reverse recovery time for the body diode is 40 ns or less.

## LED Driver MOSFET

### LED Control Diagram and Waveforms

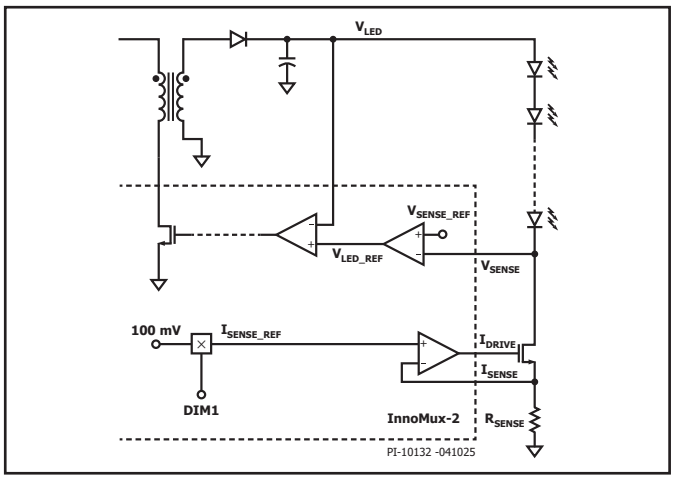



Figure 9. Block Diagram of the LED Driver.

For a 1CV1CC application, the LED string is driven by a current source through an external N-channel MOSFET. This MOSFET regulates the current through the LED string regardless of any ripple or transient voltages on the VLED output and the MOSFET needs to operate in linear mode. As shown in Figure 9, the LED driver consists of two main control blocks: the LED current source and the VSENSE voltage regulator. The LED current is regulated by an external MOSFET. The current information can be derived from the voltage across the $R_{SENSE}$ resistor, which is measured via the $I_{SENSE}$ pin. The LED current reference is set by the dimming input DIM1, which supports analog dimming, PWM dimming or filtered PWM dimming. The closed-loop current regulation is fast enough to ensure that the ripple voltage and switching noise on $V_{LED}$ do not significantly affect the LED current.

InnoMux-2 also regulates the minimum voltage on the $V_{SENSE}$ pin to a low target value (0.3 V ~ 1.0 V), minimizing power dissipation in the LED driver MOSFET. The $V_{SENSE}$ voltage is continuously measured and compared against its reference, dynamically adjusting the $V_{LED}$ reference voltage accordingly. The response time of the $V_{LED}$ controller can vary from several milliseconds to tens of milliseconds, depending on factors such as the capacitance at the LED output and the maximum power the PSU can supply.


Figure 10. LED Current Regulation by the Driver MOSFET.

As shown in Figure 10, although ripple is present on both $V_{LED}$ and $V_{SENSE}$, it does not directly affect the LED string current, as current regulation is managed by the external driver MOSFET. However, excessive ripple on $V_{SENSE}$ can increase power dissipation in the LED driver MOSFET and introduce additional ripple on the LED current. To minimize these effects, it is recommended to reduce the ripple voltage at the LED output by using low ESR capacitors.

### Driver MOSFET Maximum Voltage Rating

As shown in the data sheet, maximum $V_{LED}$ is the trimmed maximum LED voltage set by InnoMux-2 and the overvoltage protection (OVP) threshold is 116% of the maximum $V_{LED}$. The actual LED voltage will depend on the LED string characteristics. The overspill effect can cause the LED voltage to rise, and in the event of a shorted LED string, before the OVP is triggered, 116% $V_{LED}$ will be directly applied to the drain of the LED driver MOSFET. To ensure reliable operation under these conditions, the LED driver MOSFET should have a voltage rating exceeding 116% of $V_{LED}$.

### Drain-Source On-State Resistance ($R_{DS(ON)}$)

To effectively regulate the LED current to the target value, the $R_{DS(ON)}$ of the LED driver MOSFET must be sufficiently low to ensure operation within the linear region. The maximum $R_{DS(ON)}$ is defined as:

$$R_{DS(ON)\_MAX} < 0.7 \times \frac{V_{SENSE} - 100\,mV}{I_{LED}}$$

where 100 mV is the full-scale voltage across the current sensing resistor ($R_{SENSE}$); and $R_{DS(ON)}$ is the maximum resistance at the maximum junction temperature; 0.7 accounts for tolerance variations in the MOSFET's $R_{DS(ON)}$ characteristics.

As the LED driver MOSFET operates in the linear region, the drain-source voltage is determined by the $V_{SENSE}$ setting. Selecting an LED MOSFET with a lower $R_{DS(ON)}$ will not necessarily reduce its power dissipation.

### Logic-Level Gate Voltage

The maximum gate voltage supplied by InnoMux-2 is $V_{BPS}$, which can be as low as 4.5 V. To ensure that the LED driver MOSFET operates within the linear region, the LED output is disabled when the gate voltage reaches 85% of $V_{BPS}$, which is 3.8 V in worst-case scenarios. For a given driver FET drain-source voltage ($V_{SENSE}$ – 100 mV) and maximum LED current, the required gate voltage should remain below 3.8 V to ensure proper operation. Most logic-level MOSFETs meet this requirement, and designers are advised to verify compliance with the MOSFET supplier.

### Gate Capacitance ($C_{ISS}$)

The gate capacitance ($C_{ISS}$) of the MOSFET introduces additional delay on the LED constant current (CC) control. This delay is compensated by the internal control circuit, and the recommended $C_{ISS}$ range is between 200 pF and 1500 pF.

In many designs, LED current control can become highly sensitive to switching noise, leading to a significant increase in LED current ripple. In extreme cases, the current closed-loop control may lose stability, causing the LED current to oscillate at high frequencies, typically in the several MHz range. A suitable resistor ($R_G$) can be added to the MOSFET gate to quickly dampen the switching noise oscillations. However, the value of $R_G$ must be carefully selected – if too high, it may lead to excessive overshoot when the LED current turns on.

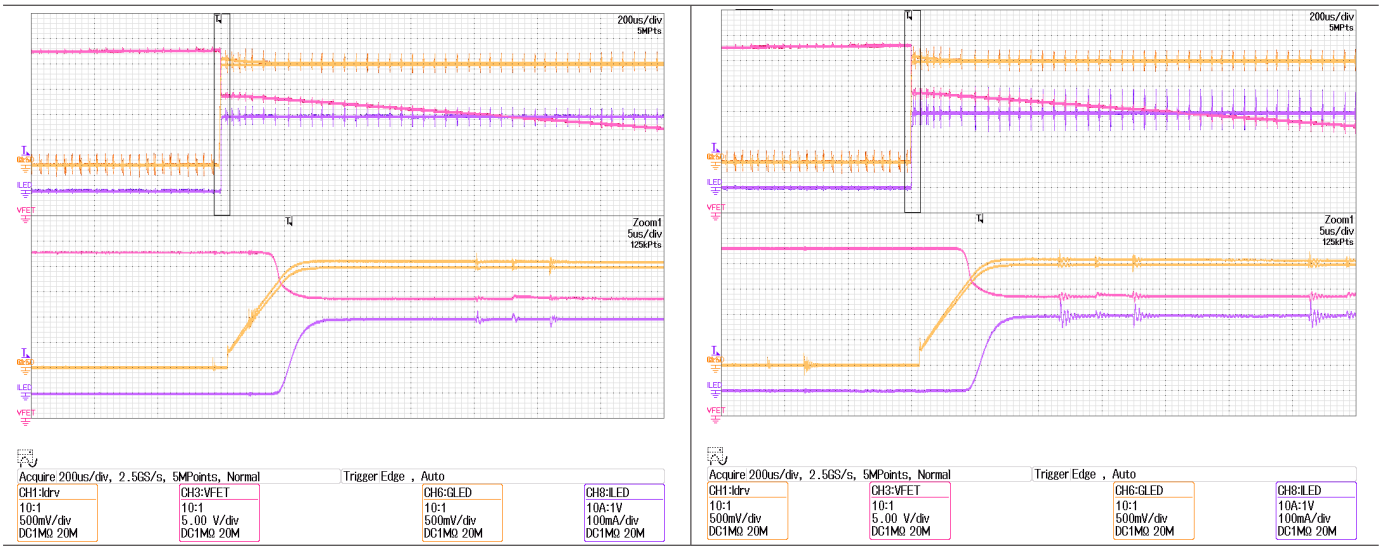



Figure 11. LED Current Oscillation Due to Switching Noise.

As shown in Figure 11, when $R_G$ = 10 Ω, oscillations are more pronounced, whereas increasing $R_G$ to 100 Ω significantly reduces LED current oscillations. If $C_{ISS}$ exceeds 1500 pF, the resulting phase delay cannot be fully compensated by the LED controller, leading to severe disturbances in LED current regulation due to ripple voltage at the LED output.

## Power Dissipation Considerations

The power dissipation of the LED driver MOSFET is effectively managed by regulating the $V_{SENSE}$ voltage to 0.6 ~ 1.0 V. However, transient power dissipation can be significantly higher than the average power dissipation. During start-up or LED turn-on, the MOSFET remains off while $V_{LED}$ ramps up to its trimmed maximum value. Once the LED string turns on, $V_{LED}$ gradually decreases from its trimmed maximum voltage to match the actual LED string voltage.

As shown in Figure 12, during this transient period (10 ms ~ 100 ms), the voltage across the LED driver MOSFET exceeds its steady-state regulation value. This transient high power must be checked against the Safe Operating Area (SOA) chart provided in the MOSFET's data sheet, which is largely dependent on its package and thermal characteristics.

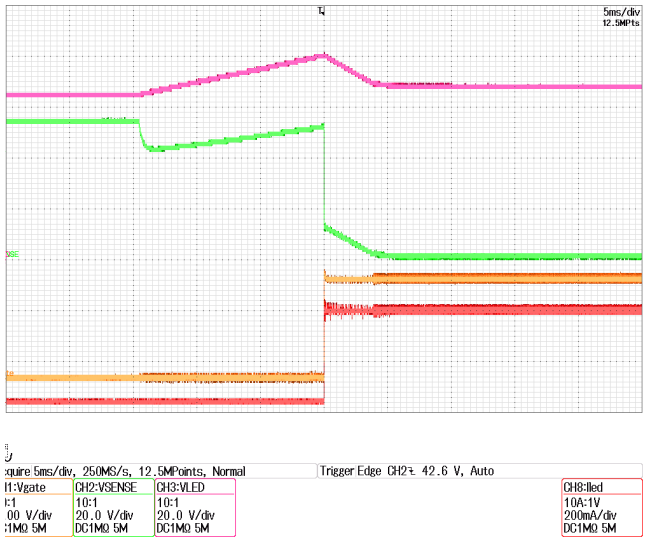



Figure 12. At LED Turn-On, LED Voltage Ramps up to Maximum Trimmed $V_{LED}$.

## $R_{SENSE}$ Calculation

The voltage across $R_{SENSE}$ is fed back to the regulator through the $I_{SENSE}$ pin, which has a full-scale voltage range of 100 mV, corresponding to the maximum LED current. The required $R_{SENSE}$ value can be calculated as follows:

$$R_{SENSE} = \frac{100\,mV}{I_{LED(MAX)}}$$

To achieve higher LED current accuracy, $R_{SENSE}$ should have a tolerance of less than 1%. The PCB trace connecting $R_{SENSE}$ resistor to the $I_{SENSE}$ pin should be kept away from high dv/dt noisy signals to minimize interference. Additionally, $R_{SENSE}$ should be connected to the same ground as the InnoMux-2 controller ground to prevent noise from the power ground plane being coupled to the $I_{SENSE}$ signal.

## IMX204DG Circuit Design

For 1CV4CC applications, the four LED strings are driven by the InnoMux-2 companion IC IMX204DG. This IC ensures accurate current matching across all LED strings, provides fast response to LED current changes, and incorporates protection features for all strings.

### Circuit Setup

The maximum LED voltage for IMX204DG must be selected to match the maximum $V_{LED}$ set by InnoMux-2. This is achieved using the $R_{LED}$ resistor, which is connected to the VLED pin of IMX204DG and is calculated as follows:

$$R_{LED} = \frac{85\% \times V_{LED}}{20\ \mu A}$$

The full-scale current for each LED string is determined by the pull-down resistor on the IS pin, given by:

$$R_S = \frac{320 \times 1.5\ V}{I_{LED\_PER\ STRING}}$$

### Design Tips

To expand a 1CV4CC application into a 1CV8CC application, the $V_{SENSE}$ pin of the second IMX204DG IC must be connected to the EXT pin of the existing IMX204DG IC. The $V_{SENSE}$ pin of the first IMX204DG should already be directly connected to InnoMux-2. IMX204DG is powered by the BPS rail of InnoMux-2, and a 10 Ω is recommended in series to dampen the noise on the BPS rail.

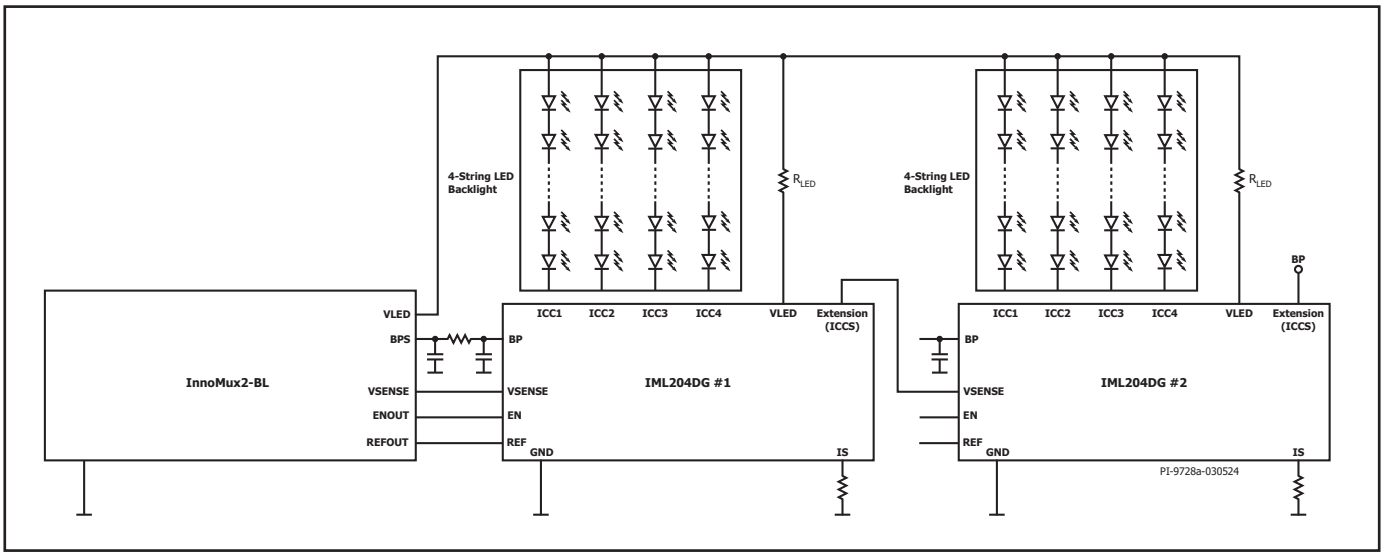



Figure 13. 1CV8CC Circuit Configuration.

The maximum voltage on ICCx pins is 50 V. In application where $V_{LED}$ > 50 V, a suitable pull-down resistor should be added to each ICCx pin to limit the voltage. Since the ICCx pin must remain below 50 V, it may not withstand an LED short-circuit test if $V_{LED}$ > 50 V.

The ground planes of IMX204DG and InnoMux-2 should be STAR-connected to minimize ground noise interference. If "string open fault" or "ICC short to ground fault" detection fails, it may be due to a noisy ground plane. In such cases, adding a 100 pF capacitor to the VLED pin can help decouple noise.

The standard IMX204DG part supports a maximum LED string current of 120 mA, with $V_{SENSE}$ = 0.3 V to optimize power consumption. Maximum LED string current can be extended to 160 mA to allow higher peak currents on the LED strings. However, in such cases, the $V_{SENSE}$ setting of InnoMux-2 must be increased from 0.3 V to 0.4 V. For these modifications, contact PI-Sales for further assistance.

## LED Dimming

In filtered PWM dimming mode, the PWM duty cycle on DIM1 serves as the LED current reference, providing a simple interface between the MCU and the dimming input of InnoMux-2, as shown in Figure 14.

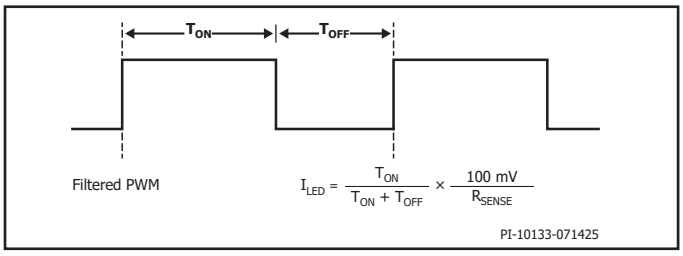



Figure 14. Filtered PWM Dimming Mode

The LED current is determined by the following equation:

$$I_{LED} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times \frac{100\ mV}{R_{SENSE}}$$

Since the duty cycle is derived from the logic "High" and "Low" time duration on DIM1, fast rising and falling edges are essential for accurate dimming control. To maintain proper functionality, it's recommended to not connect any capacitor in parallel to DIM1 pin, and the series input resistance should be kept below 1 kΩ.

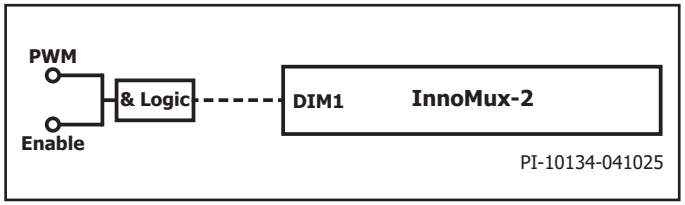



Figure 15. Filtered PWM Dimming Mode with Additional Enable Signal.

As illustrated in Figure 15, an additional "Enable" input can be added to control LED current on/off operation. This is achieved using an "AND" logic gate, which combines the PWM and Enable signals before they are applied to the DIM1 pin. Similar to standard filtered PWM dimming, maintaining fast rising and falling edges on the DIM1 pin is critical for proper operation.

## Overspill Effect: Mitigation and Elimination

### Overspill Effect

InnoMux-2 is designed to regulate multiple outputs in a flyback circuit by controlling the selection MOSFET (SEL1). When SEL1 is turned on, the secondary current should ideally be directed only to the CV1 output. However, as illustrated in Figure 16, if CVHV operates under no load or a very light load while CV1 is fully loaded, and if SEL1 turns on before the secondary discharge begins, a small amount of unintended energy may spill into the CVHV output. This phenomenon is referred to as "overspill".

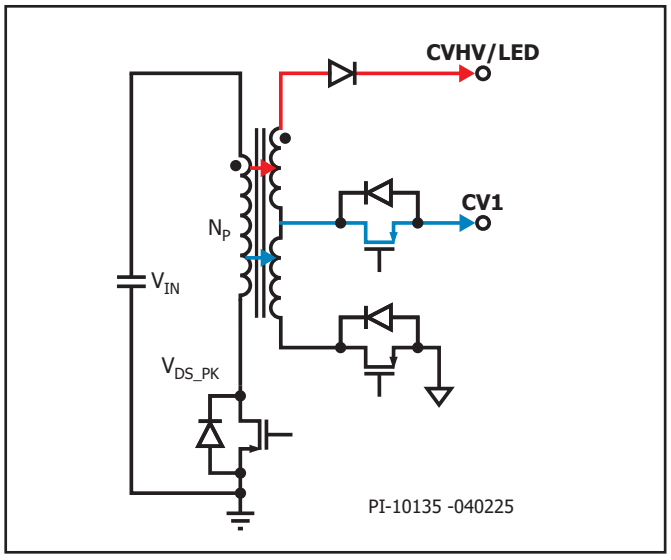



Figure 16. InnoMux-2 Circuit Diagram with Overspill Effect

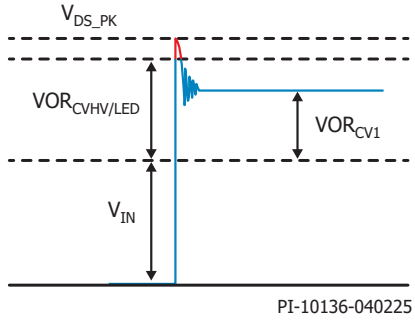



Figure 17. Peak Drain-Source Voltage on the Primary Switch when SEL FET is On.

As shown in Figure 16 and Figure 17, when the transient voltage across the primary winding ($V_{DS\_PK - VIN}$) exceeds the reflected voltage of the CVHV/LED output ($VOR_{CVHV/LED}$), the transient voltage spike coupled to the secondary winding will exceed ($V_{CVHV} + V_{D1\_FWD}$), making D1 forward-biased. As a result, a portion of the secondary current spills into CVHV/LED. This condition can be expressed as:

$$\frac{N_{CVHV/LED}}{N_P} \times (V_{DS\_PK} - V_{IN}) > V_{CVHV/LED} + V_{D1\_FWD}$$

$$V_{OR\_CVHV/LED} = \frac{N_P}{N_{CVHV/LED}} \times (V_{CVHV/LED} + V_{D1\_FWD})$$

Where $V_{DS\_PK}$ is the voltage spike across the primary switch drain-source; $V_{IN}$ is the input voltage; $V_{OR\_CVHV/LED}$ is the reflected voltage of the CVHV/LED output; $N_P$ is the transformer primary turns; $N_{CVHV/LED}$ is the transformer turns for the CVHV/LED output and $V_{CVHV/LED}$ is the voltage of the CVHV/LED output.

The overspill effect is less critical for LED applications as the Constant Current (CC) is the primary regulation target. However, in 2CV or 3CV applications, CVHV regulation accuracy can be significantly affected by overspill. The top output voltage increases due to overspill until the internal shunt activates to clamp the voltage, at 104% of $V_{CVHV}$ and 108% of $V_{LED}$. In some cases, the overspill power exceeds the capacity of the internal shunt, causing the top output to continue rising until the overvoltage protection (OVP) is triggered. The OVP threshold is set to 120% for CVHV and 116% for the LED output.

An external Zener diode can be used to clamp the top output voltage below its OVP threshold, but this increases circuit complexity and cost. The following sections introduce alternative solutions to reduce or eliminate the overspill effect without adding extra component costs.

### Single Secondary Winding in 2CV Applications

For a 2CV application, when the output voltage ratio satisfies:

$$\frac{V_{CVHV}}{V_{CV1}} < 2.5$$

It is possible for CV1 and CVHV to share the same secondary winding, as demonstrated in RDR-761 and RDR-1043. However, in some cases, depending on the loading conditions, even if the ratio is met, dual windings may still be required.

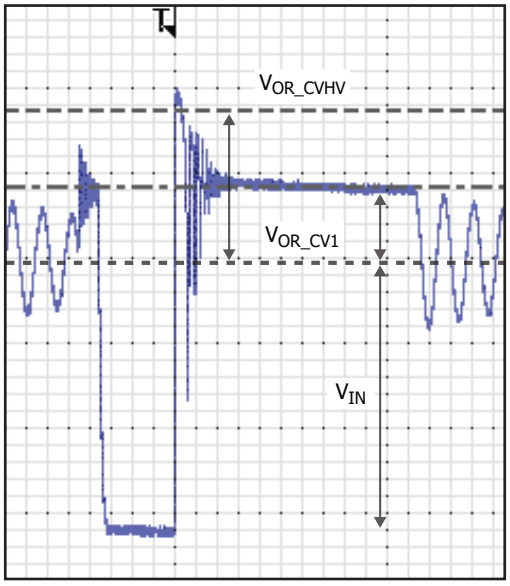
This configuration eliminates the overspill effect and ensures excellent regulation accuracy. However, in 2CV circuits with a single winding, if $V_{CV1}$ is much lower than $V_{CVHV}$, the reflected voltage of CV1 becomes very low. The low reflected voltage limits the maximum loading capability, potentially forcing the circuit into Continuous Conduction Mode (CCM) even under high line input (180-265 VAC). This could lead to excessive component stress and increased switching losses. Generally, 2CV applications with outputs like 12 V / 24 V or 5 V / 12 V are well-suited for a single winding configuration. However, applications with 5 V / 24 V or 12 V / 48 V are not suitable unless the power demand of CV1 is significantly lower than that of the total output power.

### Eliminating the Overspill Effect

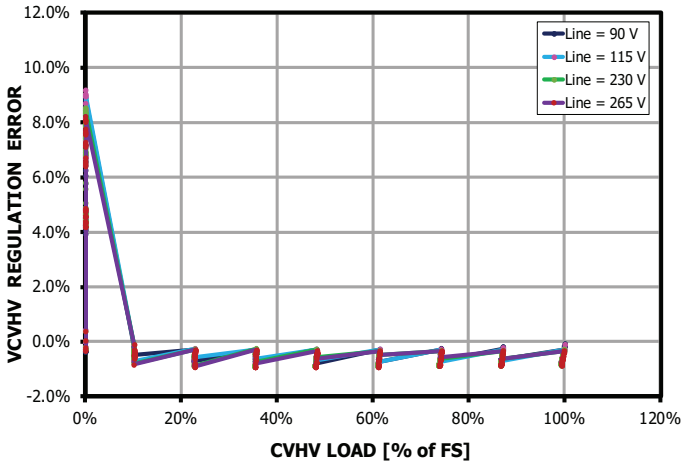
To eliminate overspill, with transformer having ≥2 secondary windings the transient voltage across the primary winding should be kept below $VOR_{CVHV/LED}$ when SEL1 FET is on, satisfying the following condition:

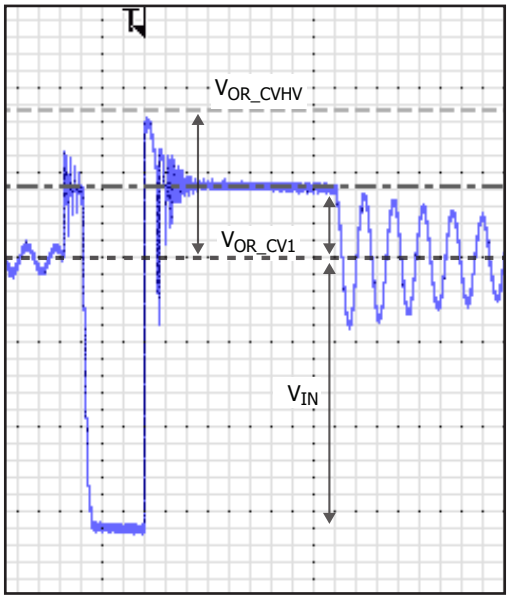
$$V_{DS\_PK} - V_{IN} < V_{ORCVHV/LED}$$

The accuracy of this equation may be affected by transformer parasitics. However, it remains a useful guideline for reducing or eliminating the overspill effect.




(a) ($V_{DS\_PK} - V_{IN}$) > $V_{OR\_CVHV}$, With Overspill




(b) ($V_{DS\_PK} - V_{IN}$) < $V_{OR\_CVHV}$, No Overspill

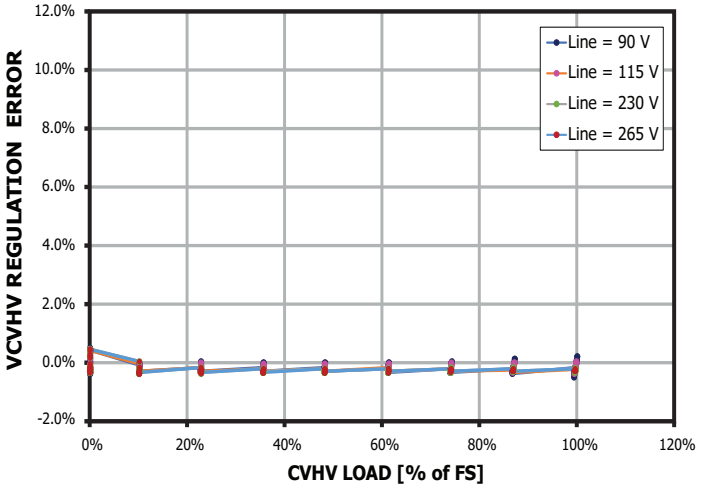



Figure 18. Comparison of Primary Switch Drain-Source Voltage and Output Regulation With and Without Overspill Effect.

## Reducing the Overspill Effect

To mitigate the overspill effect, the transient voltage across the primary winding ($V_{DS\_PK} - V_{IN}$) should be reduced by optimizing transformer and snubber design. One effective approach is to minimize leakage inductance using techniques such as the sandwiched winding method. Additionally, recycling stored energy in the primary snubber capacitor by using a standard or fast recovery diode, rather than an ultra-fast recovery diode, can help limit $V_{DS\_PK}$ and further mitigate overspill.

Another method to reduce overspill is to increase the reflected voltage ($V_{OR\_CVHV/LED}$) and the voltage difference (ΔVOR) between CV1 and CVHV/LED. A higher $V_{OR\_CVHV/LED}$ shortens the CVHV/LED diode conduction time, reducing the energy spilled into CVHV/LED. Additionally, higher ΔVOR reduces the overspill energy with respect to the overall secondary discharge energy. While increasing $V_{OR\_CVHV/LED}$ is effective in reducing overspill, it also increases voltage stress on the primary switch and raises RMS secondary current, potentially affecting overall system efficiency. These trade-offs must be carefully evaluated to ensure an optimal design.

## External Feedback Network in 2CV and 3CV Applications

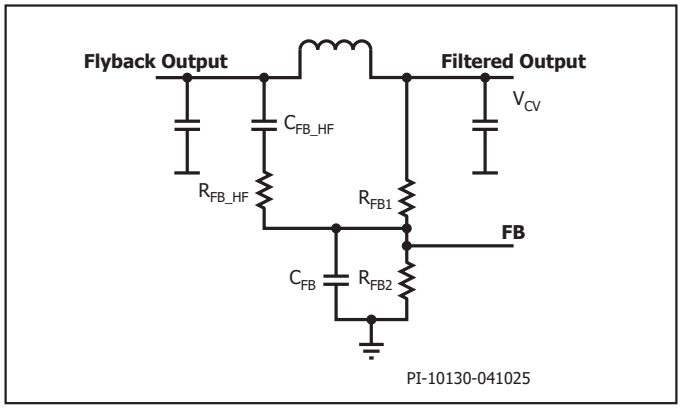



Figure 19. Output Feedback Circuit.

### External Feedback Circuit

As shown in Figure 19, this is a typical feedback circuit for InnoMux-2 with an external feedback pin (FB). External feedback pins are used only for 2CV and 3CV applications, whereas LED applications rely on internal feedback circuits. An inductor is used to reduce ripple and noise caused by switching transiens. The feedback ratio is determined by $R_{FB1}$ and $R_{FB2}$, and the output voltage is calculated as:

$$V_{CV} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times V_{FB(REG)}$$

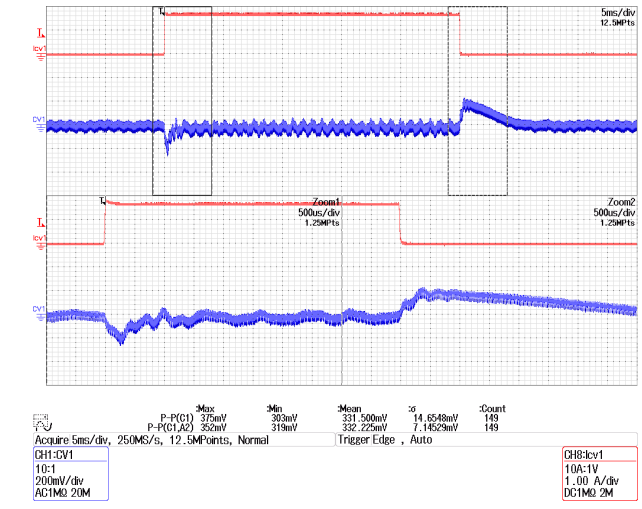
$$V_{FB(REG)} = 1.22\ V$$

$C_{FB}$ is connected in parallel with $R_{FB2}$ to decouple noise on the FB pin. To maintain the ripple term in the feedback signal, the RC time constant for $R_{FB2}$ and $C_{FB}$ should be less than the inverse of the maximum switching frequency. The recommended value for $C_{FB}$ ranges from 47 pF to 470 pF, with a default value of 100 pF.

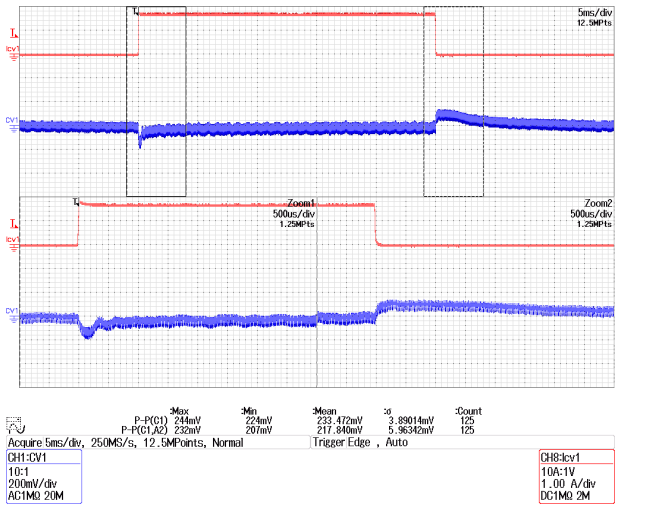
### Optimizing Ripple and Load Step Performance Using Feedback Circuit

In most cases, switching ripple on the feedback signal is required to stabilize the closed-loop control and prevent pulse grouping. To achieve this, $R_{FB\_HF}$ and $C_{FB\_HF}$ are added as a high-pass filter (HPF) to couple the ripple voltage into the feedback signal without affecting its steady-state voltage.

Reducing $R_{FB\_HF}$ increases the ripple voltage in the feedback signal, helping to minimize overshoot and undershoot during load steps. However, if $R_{FB\_HF}$ is too low, excessive dv/dt from the output may be coupled onto the FB pin, potentially exceeding its OVP or UVP threshold, causing the PSU to shut down. By default, $R_{FB\_HF} = R_{FB1}$, but it can be adjusted to optimize ripple performance and load step response.




$R_{FB\_HF} = R_{FB}$




$R_{FB\_HF} = R_{FB} / 3$

Figure 20. Load Step and Ripple with Different $R_{FB\_HF}$ (RDK-1043).

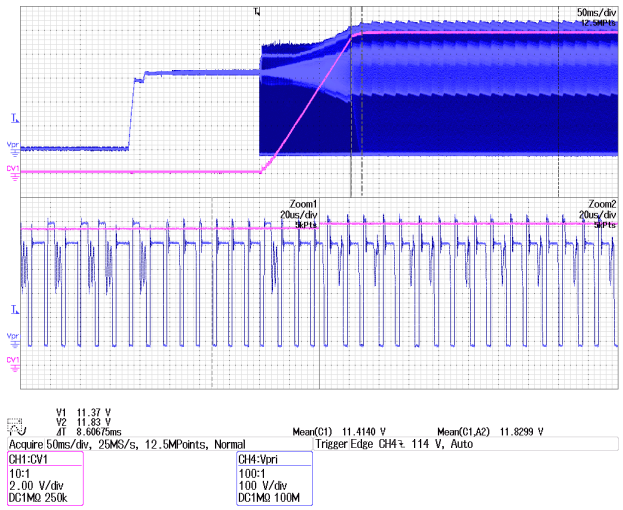
$C_{FB\_HF}$ is responsible for bypassing the dv/dt terms of the output voltage. The dominant low-frequency dv/dt term on the output voltage is ~1 kHz. Therefore, its high-frequency (HF) impedance can be calculated as:

$$Z_{C_{FB\_HF}} = \frac{1}{2\pi f_{RIPPLE} \times C_{FB\_HF}}$$

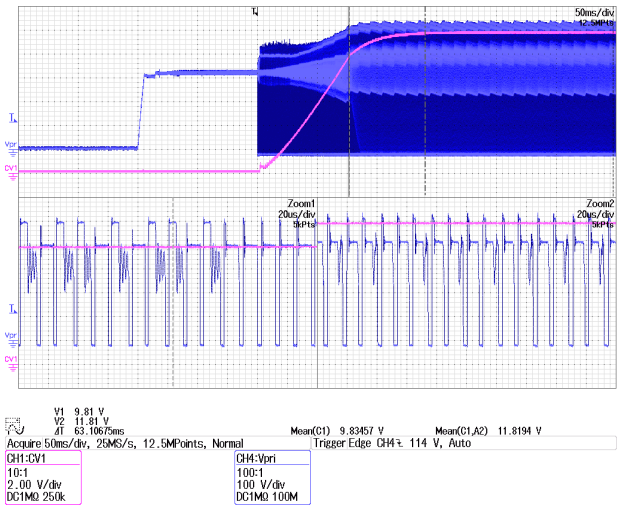
To allow the high-pass filter to effectively couple the necessary ripple voltage into the feedback signal without disturbing the closed-loop stability, $Z_{CFB\_HF}$ must be significantly lower than $R_{FB\_HF}$, such that the impact on the feedback loop's phase delay is minimized.

### Soft Start with Large Feedback Capacitor ($C_{FB\_HF}$)

At start-up, $C_{FB\_HF}$ needs to be charged to the corresponding output voltage, which can slow down the output voltage ramp-up. As a result, a larger $C_{FB\_HF}$ increases the maximum load that the PSU can successfully start with.




$C_{FB\_HF}$ = 100 nF




$C_{FB\_HF}$ = 470 nF

Figure 21. CV Output Ramp-up with Different $C_{FB\_HF}$ (RDK-1043).

## Power Consumption of the Feedback Circuit

Power consumption of the feedback circuit can be minimized by increasing the resistances of the feedback network. However, $R_{FB2}$ must be low enough to prevent onboard noise from interfering with the feedback signals on the FB pins. For 2CV and 3CV configurations, InnoMux-2 can be trimmed to use internal feedback, significantly reducing power consumption while avoiding unwanted noise on the FB signals. The below table shows the power consumption of the feedback circuit at different output voltae levels, comparing external and internal feedback settings.

Note: The default data sheet configuration is trimmed for external feedback to maximize output voltage flexibility. Please contact the local PI sales team for information on internal feedback options.

| $V_{CVX}$ [V] | Power Consumption of Feedback Circuit, $P_{FB}$, [mW] | | | |
|---|---|---|---|---|
| | **External Feedback** | | **Internal Feedback** | |
| | $R_S$ = 1 kΩ | $R_S$ = 3.3 kΩ | CV1 & CV2 | CVHV |
| 5 | 6.0 | 1.8 | < 0.1 | |
| 12 | 14.4 | 4.4 | 0.2 | |
| 24 | 28.8 | 8.7 | 0.8 | < 0.1 |
| 36 | 43.2 | 13.1 | | 0.2 |
| 48 | 57.6 | 17.5 | | 0.3 |
| 60 | 72.0 | 21.8 | | 0.5 |
| 100 | | | | 1.5 |
| 150 | | | | 3.4 |
| 200 | | | | 6.1 |

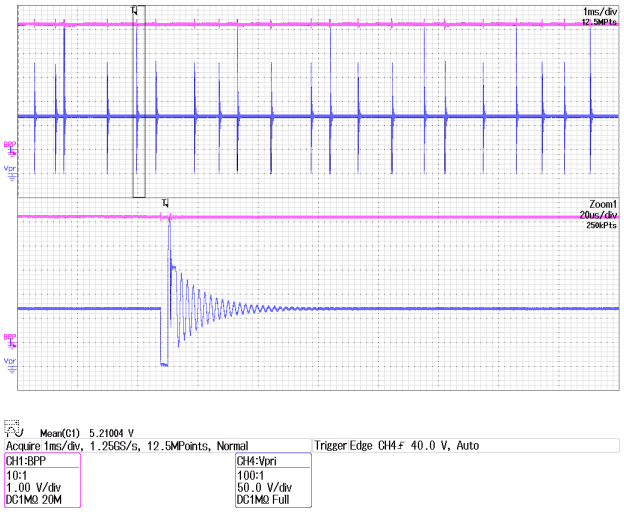
## Primary Bias Winding

### Bias Turns

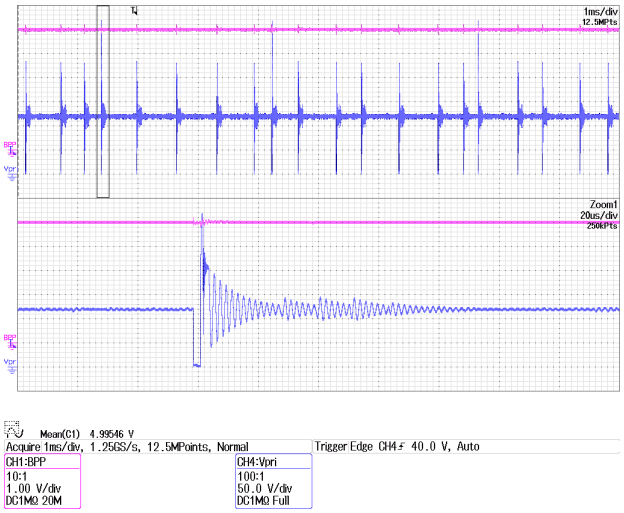
For a multi-output power supply using InnoMux-2, reflected voltages are different for each output. As a result, the bias voltage varies depending on the load condition. The number of bias winding turns should be determined based on the worst-case scenario, where CVHV/LED has no load, and the bias voltage is determined by $V_{CV1}$:

$$N_{BIAS} = \frac{V_{BIAS}}{V_{CV1}} \times N_{CV1}$$

However, due to the leakage inductance within the flyback transformer, the actual minimum bias voltage may be lower than the value calculated using the equation above. In standby mode or no-load conditions, if the bias winding voltage drops too low, it may trigger drain tap pulses, where InnoMux-2's primary-side is powered directly from the drain node referred to as Drain Tap, which is highly inefficient. To prevent this, additional testing is required to ensure that the bias voltage remains above 8 V under all operating conditions.




(a) Without Drain Tap Pulses




(b) With Drain Tap Pulses

Figure 22. Primary Waveforms in Standby Mode With / Without Drain Tap Pulses.

The bias winding turns are designed based on the required minimum bias voltage $V_{BIAS\_MIN}$ when CVHV/LED output has no load. However, the maximum bias voltage can be much higher when the CVHV/LED output is fully loaded.

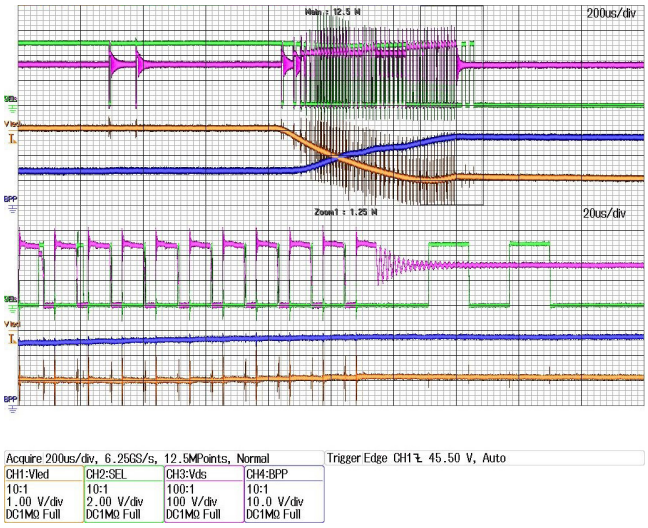
$$V_{BIAS} = \begin{cases} V_{BIAS\_MIN} = \frac{N_{BIAS}}{N_{CV1}} \times V_{CV1} \ldots\ldots \text{CVHV/LED has no load} \\ V_{BIAS\_MAX} = \frac{N_{BIAS}}{N_{CVHV}} \times V_{CVHV} \ldots\ldots \text{CVHV/LED is fully loaded} \end{cases}$$

A suitable $R_{BPP}$ (R20) resistance should be chosen to limit the BPP current below its protection threshold, which is typically 7.5 mA.

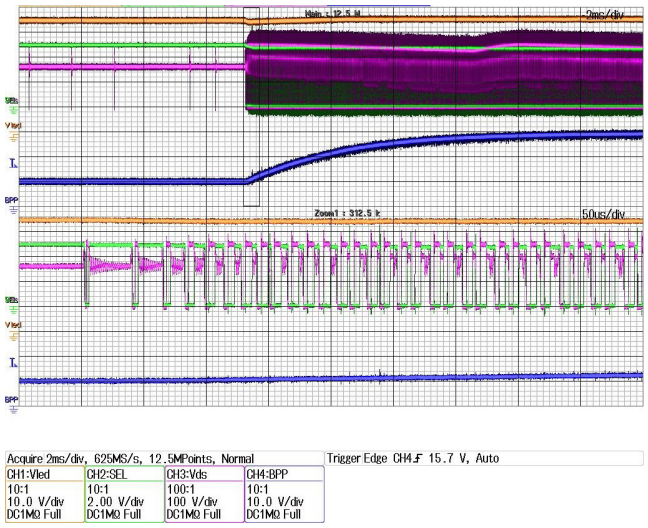
### Serial Resistor $R_{BIAS}$ for Current Limiting During Load Steps

When a load step is applied to the CVHV/LED output from no load to full load, the bias voltage is initially at its minimum. Due to the large voltage difference ($V_{OR\_BIAS}$ << $V_{OR\_CVHV}$), the secondary current tends to discharge into the bias output rather than CVHV/LED. Although this transient condition lasts only a few hundred microseconds, it may still cause CVHV/LED to lose regulation and trigger over-power protection. As shown in Figure 23(a), during the load step transient, a significant portion of the secondary current is discharged into the bias winding instead of CVHV/LED output, leading to voltage collapse and loss of regulation.

To address this issue, add a resistor $R_{BIAS}$ (10 Ω ~ 47 Ω) in series with the bias winding is recommended (eg. R33 in Figure 2). This resistor limits the discharge current in the bias winding, ensuring that most of the energy is directed to CVHV/LED instead of the bias circuit. By reducing the discharge current to the bias output, the increase in bias output voltage is effectively slowed down, preventing the CVHV/LED output from losing regulation. However, the bias discharge current flowing through $R_{BIAS}$ introduces additional power loss in the bias circuit, which should be considered in the design. Therefore, the resistance value should be carefully selected to minimize power loss while still providing effective current limiting.




(a) No Series Resistor $R_{BIAS}$

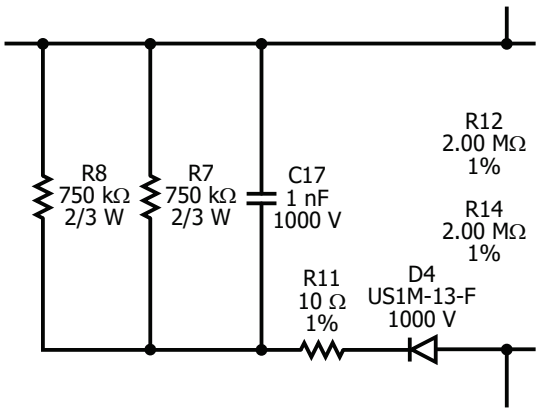



(b) With Series Resistor $R_{BIAS}$

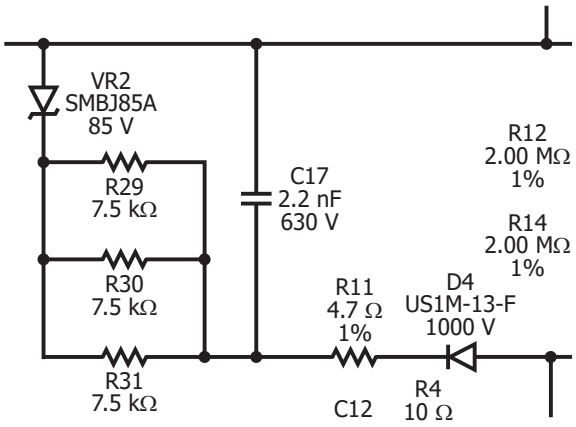
Figure 23. CVHV/LED Load Step With/Without Series Resistor $R_{BIAS}$.

## Primary Snubber Circuit

The primary snubber circuit is an essential component in a flyback converter, designed to control voltage spikes caused by leakage inductance and to ensure that drain-source voltage of the primary switch remains within its rated voltage. Additionally, the primary snubber should be optimized to minimize power consumption during both normal operation and standby mode.




(a) RC (DER-715)




(b) RCZ (DER-714)

Figure 24. Primary Snubber Circuit.

In applications where leakage inductance is low, the RC-type primary clamp shown in Figure 24(a) is sufficient to keep standby power consumption at acceptable levels. To achieve even lower standby power consumption, a Zener diode (VR2) can be added as shown in Figure 24(b). This Zener diode ensures that during standby mode, the clamp capacitor $C_{CLM}$ (C17) is not discharged below the threshold voltage of the Zener, thereby minimizing standby power consumption. The large serial resistor (R29//R30//R31=2.5 kΩ) limits the transient current through the Zener diode. By reducing the transient current through the Zener diode, the overall reliability of the RCZ circuit is significantly improved.

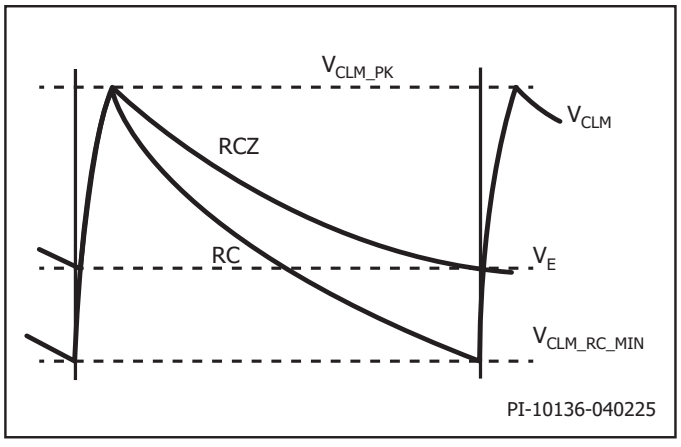



Figure 25. Clamp Voltage of RC and RCZ Snubber Circuits.

The power consumption of the snubber circuits can be calculated as:

$$P_{SNB\_LOSS} = \frac{1}{2} \times \frac{L_{LK} \times I_{PEAK}^2 \times V_{CLM} \times F_{SW}}{V_{CLM} - VOR}$$

In RCD clamp, resistor and capacitor values can be calculated as ;

$$R_{SNB} = \frac{V_{CLM}^2 \times (V_{CLM} - VOR)}{\frac{1}{2} \times L_{LK} \times I_{PEAK}^2 \times V_{CLM} \times F_{SW}}$$

$$C_{SNB} = \frac{V_{CLM}}{R_{SNB} \times F_{SW} \times \Delta V_{SNB}}$$

Where;

$L_{LK}$ is leakage inductance
$I_{PEAK}$ is peak switching current
$V_{CLM}$ is voltage across clamp circuits
$F_{SW}$ is switching frequency
$V_{OR}$ is reflected output voltage
$\Delta V_{SNB}$ is ripple voltage across clamp capacitor
$R_{SNB}$ is snubber resistor

Measure the voltage across clamp at low line and full load.

## Selection MOSFET & CV1 Output

### Bootstrap Circuit

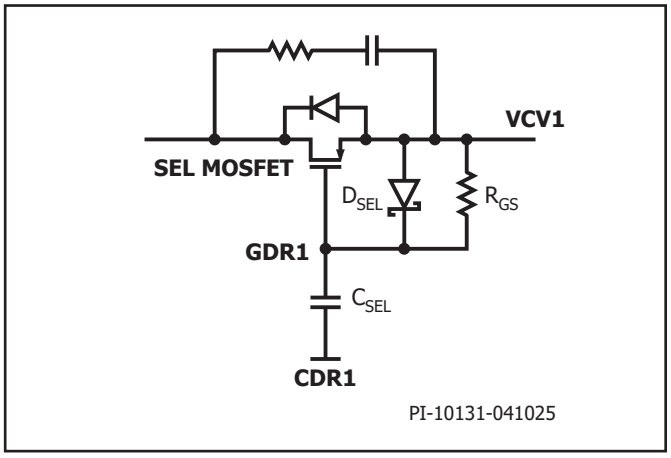



Figure 26. CV1 Output and Selection MOSFET.

The gate drive voltage of the selection FETs is VBPS (~5 V). It is therefore essential to select logic level MOSFETs with typically $V_{GS(th)}$ < 3.5 V. The source of the selection MOSFET is connected to the CV1 output, requiring the gate drive signal CDR1 to be boosted through a bootstrap circuit consisting of $C_{SEL}$, $D_{SEL}$ and $R_{GS}$. When CDR1 is at 0 V, $C_{SEL}$ charges up to nearly $V_{CV1}$ (taking into account the forward voltage drop across $D_{SEL}$). A Schottky diode is recommended for $D_{SEL}$ to minimize the voltage drop. To turn on the selection MOSFET, CDR1 is increased to $V_{BPS}$, and GDR1 rises to approximately $V_{CV1}$ + $V_{BPS}$, creating ~$V_{BPS}$ voltage difference across the MOSFET gate-source.

The gate drive voltage is shared between $C_{SEL}$ and the input capacitance ($C_{ISS}$) of the selection MOSFET. To ensure minimal voltage variation on $C_{SEL}$ during switching, it is crucial that:

$$C_{SEL} > 10 \times C_{ISS}$$

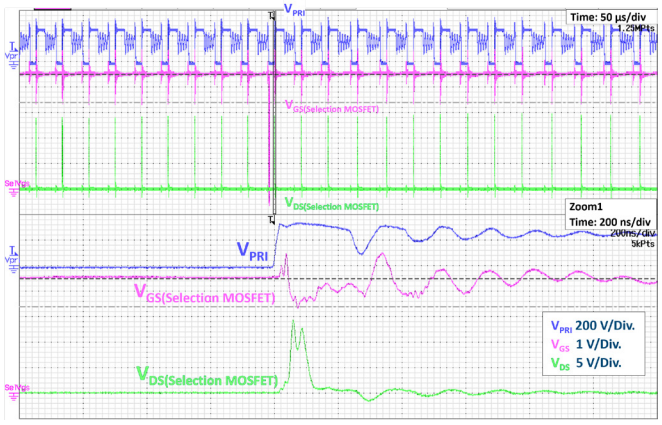
The recommended range for $C_{SEL}$ is 47 nF to 220 nF, providing adequate charge storage for stable operation and minimal voltage drop during transitions.

$R_{GS}$ is used to discharge the gate-source voltage, and the suitable resistance range is 100 kΩ to 2 MΩ. When only CV1 is loaded while CVHV/LED has no load, CDR1 remains continuously high. This causes the voltage across $C_{SEL}$ to gradually decrease over time. To maintain proper operation, a refresh pulse is applied approximately every 0.8 ms to recharge $C_{SEL}$. During standby mode, this refresh pulse frequency can be further reduced to a few hundred Hz. Hence it is essential to verify that the minimum gate voltage remains above the MOSFET's gate threshold voltage under all operating conditions.

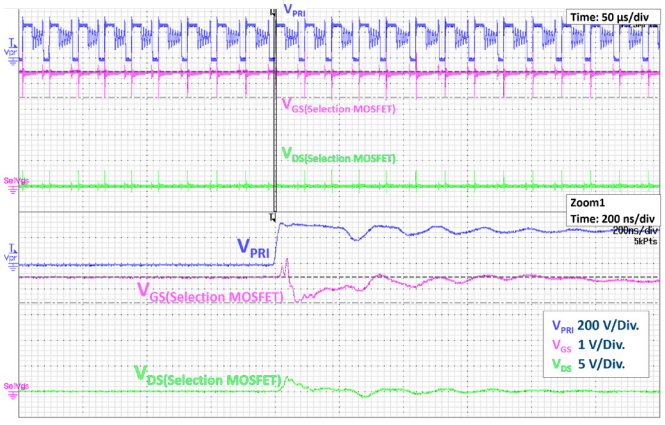
### MOSFET Selection

When the secondary current starts discharging through the selection MOSFET into the output capacitor, the voltage at the MOSFET's source may rise due to the equivalent series resistance (ESR) of the capacitor. This ripple voltage can cause the gate-source voltage ($V_{GS}$) of the MOSFET to decrease toward its threshold voltage ($V_{GS(th)}$), leading to an increase in the MOSFET's drain-source resistance ($R_{DS(ON)}$).

In 2CV or 3CV applications, this initial increase in $R_{DS(ON)}$ can redirect a portion of the secondary discharge current from CV1/CV2 to CVHV/LED, causing an increase in the CVHV/LED output voltage. As a result, the regulation error on CVHV/LED becomes significant, even in single-winding 2CV configurations. To mitigate this issue, it is recommended to select a MOSFET with a lower $V_{GS(TH)}$ and a larger gate-to-drain capacitance ($C_{RSS}$). A higher $C_{RSS}$ helps sustain the MOSFET in its "ON" state at the beginning of the secondary discharge, preventing premature turn-off and maintaining proper output regulation.




Selection MOSFET (SQJA62EP, $C_{RSS}$ = 50 pF)

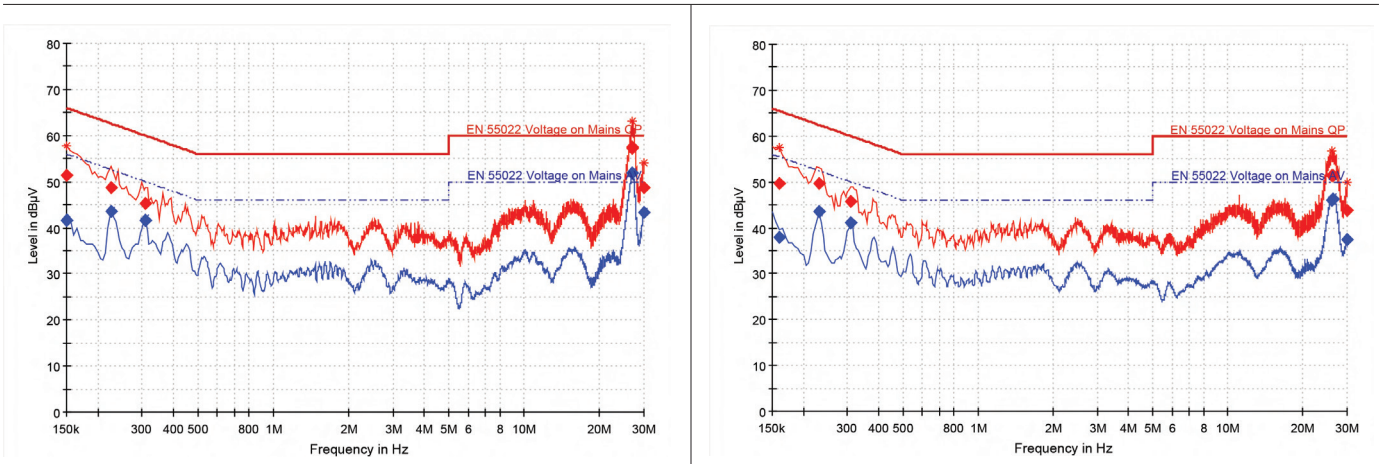



Selection MOSFET (PSMN4R1-60YL, $C_{RSS}$ = 276 pF)

Figure 27. Choosing Selection MOSFET to Avoid Turn-Off Transient (RDK-1043).

### Snubber Circuit Across Selection MOSFET

When the selection MOSFET turns off, parasitic oscillations within the transformer can generate high-frequency noise. This is typically observed in the 10 MHz to 30 MHz range and may cause the EMI spectrum to exhibit a noise level several dB higher than expected. To mitigate this issue, an RC snubber circuit can be placed in parallel with the selection MOSFET to suppress high-frequency oscillations. For example, in the DER-716 3CV application, the recommended snubber values are 330 pF for the capacitor and 10 Ω for the resistor, as shown in Figure 28.




No Snubber

Snubber = 330 pF + 10 Ω

Figure 28. Snubber for Selection MOSFET to reduce EMI noise.

### Maximum Voltage on Selection MOSFET

The maximum transient voltage on the selection MOSFET occurs at the beginning of secondary discharge and can be estimated based on the transient primary voltage and the turns ratio between the primary and CV1 windings:

$$V_{CV1\_TRANS} = \frac{N_{CV1}}{N_P} \times (V_{DS\_PK} - V_{IN})$$

Where $V_{DS\_PK}$ is the voltage spike across the primary switch drain-source; $V_{IN}$ is the input voltage; $N_P$ is the transformer primary turns; $N_{CV1}$ is the transformer turns for CV1 output; The value of $V_{CV1\_TRANS}$ is significantly influenced by parasitic parameters within the transformer and other circuit components. Therefore, it should only be used as a guideline to estimate the maximum voltage stress on the selection MOSFET.

When determining the voltage rating for the MOSFET, the plateau voltage at the MOSFET drain when CVHV / LED is conducting should be considered. This voltage can be calculated as:

$$V_{CV1\_PLATEAU} = \frac{N_{CV1}}{N_{CVHV/LED}} \times (V_{CVHV/LED} + V_{D1\_FWD}) - V_{CV1}$$

Where $N_{CVHV/LED}$ is the transformer turns for the CVHV/LED output; $V_{D1\_FWD}$ is the forward voltage of the rectifier diode on the CVHV/LED output. In the InnoMux-2 configuration, a Zener diode is recommended to clamp the maximum voltage at the selection MOSFET drain. The suggested Zener voltage is 1.5 × $V_{CV1\_PLATEAU}$ to provide adequate margin. However, the Zener clamp can be removed to reduce circuit cost and complexity. In such cases, the selection MOSFET must have a higher voltage rating to withstand potential voltage spikes. Additionally, extensive testing is required to ensure that $V_{CV1\_TRANS}$ remains within the MOSFET's voltage rating. An avalanche-rated MOSFET is recommended to enhance protection against transient voltages.

### BPS Power Source

The secondary circuit of InnoMux-2 is powered by BPS, which is derived from a 5 V regulator. The BPS regulator can derive its input from CV1, CV2 or CVHV/LED. During start-up, before CV1 and CV2 begin ramping up, CVHV/LED is regulated at approximately 9 V, serving as the initial input for the BPS regulator. Once CV1 or CV2 exceed their respective BPS input thresholds (7.9 V for CV1 and 5.5 V for CV2), the BPS regulator switches to the available source. When both CV1 and CV2 qualify as BPS inputs, CV1 is prioritized to minimize power loss, given that VCV1 < VCV2. In direct power mode, when CV1 voltage is within 4.5 V to 5.5 V, BPS is directly supplied from CV1, and the BPS regulator remains disabled, significantly reducing power loss. In 2CV applications, when BPS operates in direct power mode, the uVCC option can be enabled to supply 3.3 V. For more information, please contact local PI-Sales office.

While CVHV/LED is designed to power BPS during start-up, it is not suitable for continuous operation as a BPS supply. However, in 1CV1CC and 2CV applications, if the CVHV / LED voltage is below 24 V, it can be connected to the AS pin as an input to the BPS regulator.

To limit transient currents caused by ESD strikes, resistors ranging from 2 Ω to 10 Ω should be inserted on the CV1, CV2, and CVHV/LED pins. When CV1 and CV2 serve as inputs to the BPS regulator, the voltage drop across these resistors is typically several tens of millivolts. This voltage drop is not an issue if CV1 and CV2 have dedicated external feedback pins. However, in cases where CV1 and CV2 are configured with internal feedback, excessive serial resistance may disrupt the closed-loop stability, potentially causing unexpected pulse skipping. Thus, the series resistors on CV1, CV2, and CVHV/LED should be minimized to maintain stability.

## Diagnostic in Fault Protection

In the event of an auto-restart or latch-off protection, the secondary circuit can identify the fault condition by sequentially transmitting a series of bits to the CDR1 pin. These bits indicate the fault source, providing diagnostic information that can help with troubleshooting.

| CDR1 code | Description |
|---|---|
| 000-000 | Fault reporting disabled |
| 010-001 | Output overvoltage |
| 010-010 | FB pin open or short |
| 010-011 | LED fault |
| 010-100 | Request Not Clear - over power protection |
| 010-101 | Over temperature |
| 010-110 | CVHV/LED fails to reach $V_{STAYALIVE}$ at start-up |
| 010-111 | SR pin open or short |

Each bit in the diagnostic code has a duration of 12.8 µs, as illustrated in Figure 29. The waveform in Figure 29 corresponds to a scenario where the output fails to deliver the requested power, triggering the Request Not Clear - Over Power Protection fault, represented by the 010-100 fault code.

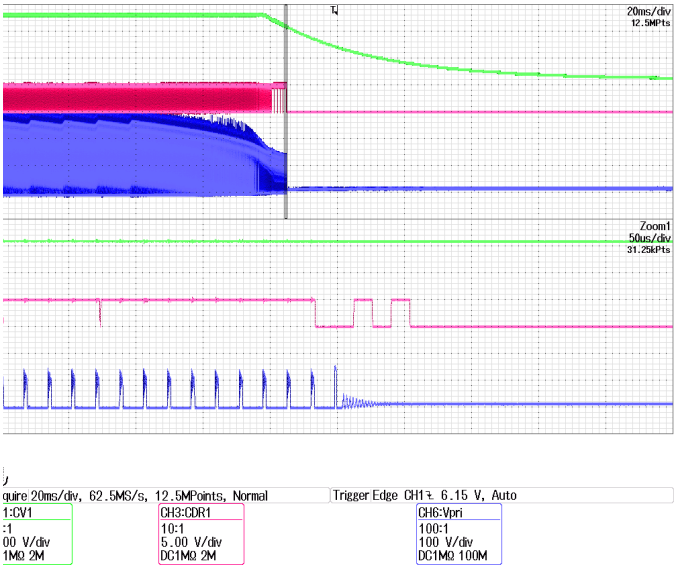



Figure 29. Request Not Clear Over Power Protection Fault Code (010-100).

## Guidelines for PCB Layout

### Primary Circuit

To optimize thermal performance and minimize noise, follow these layout guidelines:

- Maximize the copper area of the primary source pin to enhance heat dissipation for InnoMux-2. Refer to the data sheet for recommended thermal design practices.
- Minimize the loop area of the primary clamp circuit and place it close to the drain pin to reduce noise.
- Keep the drain pin conductor away from the BPP and V pins to prevent unwanted coupling and interference.
- Keep the primary bias capacitor close to the BPP pin.
- Keep the V pin resistors close to InnoMux-2.
- Use a single-point connection from the bulk capacitor to the copper area of the source pin.

### Secondary Circuit

Proper layout of the secondary circuit is essential for isolation, ESD immunity, and performance optimization:

- Avoid placing traces beneath the InnoMux-2 IC to enhance isolation and ESD immunity.
- Ensure that the FWD trace, which has a high dv/dt, is kept away from sensitive signals such as FB, $I_{SENSE}$ and $V_{SENSE}$.
- Position the FWD resistor close to InnoMux-2.
- Minimize the area of the secondary discharge loop, consisting of SR MOSFET, selection MOSFET, CVHV/LED diode and output capacitors.
- Place the secondary bias capacitor near the BPS pin.
- Keep feedback resistors and their decoupling capacitors close to the FB pins.
- Maximize copper areas for SR MOSFET, selection MOSFET, CVHV/LED diode and CV2 output diode.
- Use a star-ground connection from the InnoMux-2 IC to the source of the SR MOSFET or the anode of the SR diode.
- Ensure that current sense resistors for the LED driver MOSFET share the same ground reference as InnoMux-2 to avoid unwanted voltage offsets.

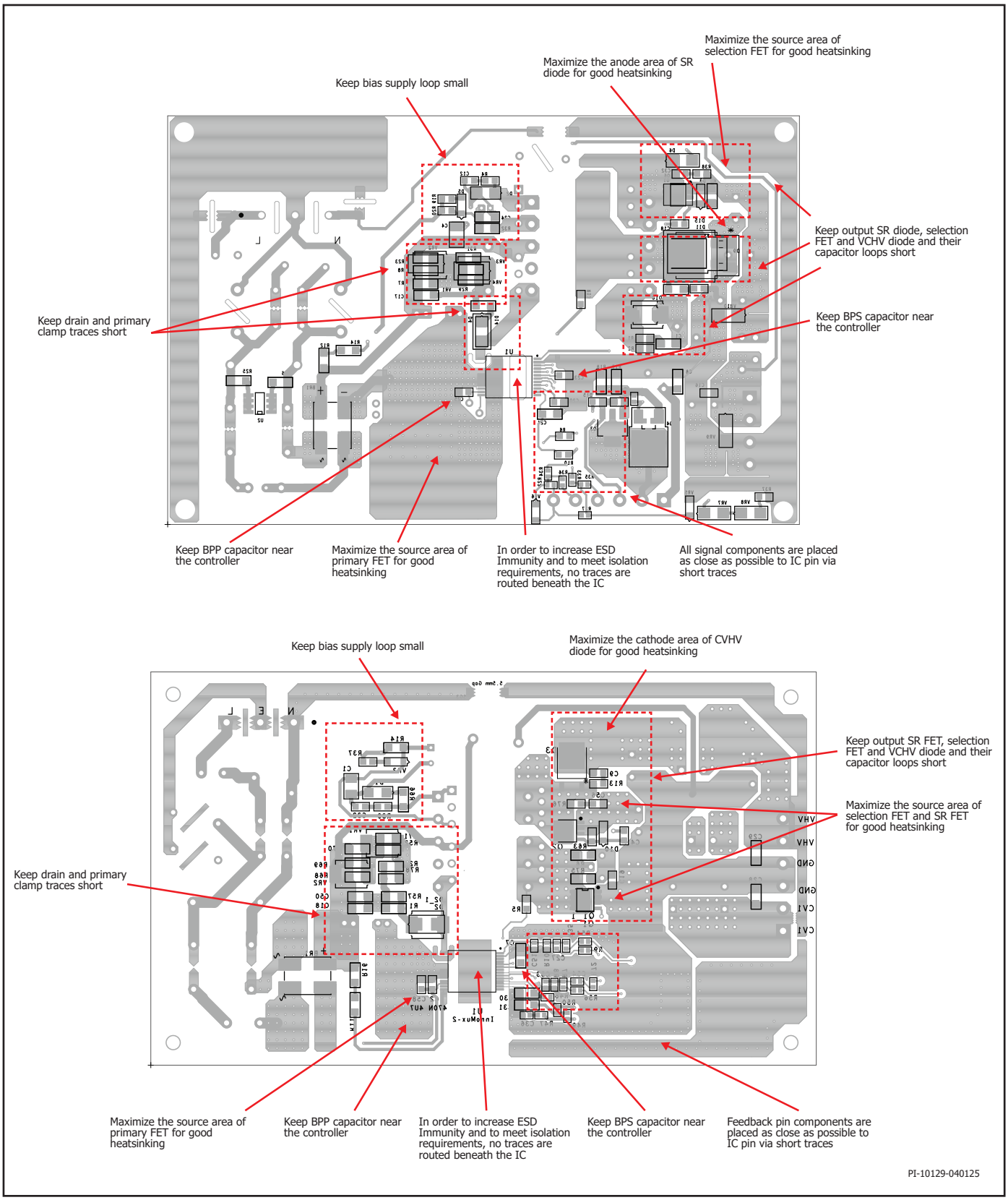



Figure 30. PCB Layout.

## Recommendations to Reduce Power Consumption

To optimize efficiency and minimize power loss, consider the following recommendations:

- InnoMux-2's primary side is powered from the BPP pin. Select resistor $R_{BP}$ (e.g., R20 in Figure 1) appropriately to achieve the lowest no-load/low-load input power.
- Use a Schottky or ultrafast diode for bias supply.
- Select a low-ESR capacitor for bias supply.
- Minimize the primary clamp capacitor value.
- Use low-value snubber capacitors for the SR MOFET and SEL MOSFETs.
- Adjust the FB resistor values to achieve lowest no-load/low-load input power.
- Use a secondary rectifying diode with a low forward voltage drop ($V_F$).
- Use direct-power mode.

## Recommendations to Reduce Conducted EMI

- Optimize component placement and minimize loop areas in both primary and secondary power circuits to reduce radiated and conducted EMI.
- Use common-mode chokes at the input to effectively attenuate common-mode noise. Alternatively, shield windings in the transformer may provide similar noise suppression.
- Adjust the RC snubber component values of the SR MOSFET, selection MOSFET, and rectifying diode to mitigate high-frequency radiated and conducted EMI.
- Place a 1 μF ceramic capacitor at the output to help suppress radiated EMI.
- Utilize the bulk capacitor's characteristic impedance and common mode choke leakage inductance to reduce differential mode noise below 1 MHZ.

## Recommendations to Improve ESD Immunity

- Maintain sufficient clearance between the primary-side and secondary-side circuits to prevent ESD breakdown. For an over-molded package, a minimum clearance of 8 mm is recommended, while for an exposed-pad package, the clearance should be at least 7.5 mm, particularly underneath the InSOP package and the transformer. Placing a spark gap near or across the InSOP package is not recommended.
- Use two spark gaps connected to the secondary terminals (CV output return and CV output positive) and one at the AC input side after the fuse. A minimum gap of 5.4 mm is generally sufficient to meet creepage and clearance requirements in compliance with safety standards.
- Place a spark gap across the common-mode choke to provide a low-impedance discharge path, preventing high-energy discharge buildup due to ESD or common-mode surge events.
- Use a Y capacitor between either positive or negative output terminals and the input bulk capacitor's positive terminal.
- Apply multi-layer insulation tape between the bias and secondary windings, as well as between the primary and secondary windings, to improve dielectric strength and ESD resistance.
- Ensure sufficient clearance between GND and DIM1 , DIM2 and FB signals.
- Insert low-value resistors (recommended between 2 Ω and 10 Ω) before the VCV1, VCV2, VCVHV/LED pins to enhance ESD immunity by limiting transient currents.

| Revision | Notes | Date |
|---|---|---|
| A | Introduction release. | 07/25 |

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