TOPSwitchGaN Family

Integrated Off-Line Switcher with EcoSmart Technology for Highly Efficient Power Supplies

Product Highlights

Highly Integrated, Compact Footprint
- 90% average efficiency between 20% and 100% load
- Robust 800 V PowiGaN™ switch provides excellent surge withstand
- Switching frequency up to 150 kHz minimizes transformer size

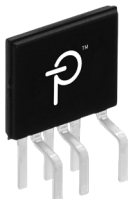
EcoSmart™ – Energy Efficient
- No-load consumption below 50 mW at 230 VAC
- Up to 200 mW output power for 300 mW input at 230 VAC

Reduced Part Count, Design Flexibility
- Frequency jitter and source potential cooling reduces EMI filter size
- Integrated soft-start reduces start-up stress
- Programmable switching frequency increases design flexibility

Extensive Protection Features
- Output short-circuit, overload, over-current and overvoltage
- Auto-restart limits power delivery to <3% during output short circuit faults
- Line undervoltage (UV) prevents turn-off glitches
  - Simple fast AC reset
- Line overvoltage (OV) shutdown increases protection against line surge
- Accurate thermal shutdown with large hysteresis (OTP)

Typical Applications
- Appliances
- Tools, EV chargers and industrial power supplies

eSOP™-12 Package (K Suffix)
- Low profile surface mount package for ultra-slim designs
- Supports wave or reflow soldering
- PCB cooling via SOURCE pin and exposed pad



eSIP™-7 Package (E Suffix)
- Vertical orientation minimizes PCB footprint
- Simple heatsink mounting using clip
- Thermal impedance equivalent to TO-220 package
- Provides extended power range

Figure 2. Packages.

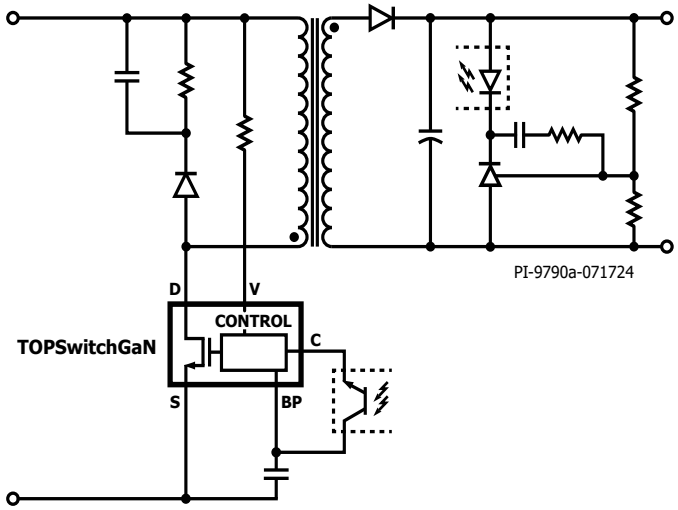


Figure 1. Typical Flyback Schematic.

Output Power Table[1,2]

Product[3]	PCB Copper Area		
	400 VDC	230 VAC ±15%	85-265 VAC
	Peak or Open Frame	**Peak or Open Frame**	**Peak or Open Frame**
TOP7074K	90 W	85 W	70 W
TOP7075K	105 W	95 W	85 W
TOP7078K	180 W	170 W	135 W
Product[3]	**Metal Heat Sink**		
	400 VDC	230 VAC ±15%	85-265 VAC
	Peak or Open Frame	**Peak or Open Frame**	**Peak or Open Frame**
TOP7074E	200 W	185 W	130 W
TOP7075E	240 W	210 W	165 W
TOP7078E	440 W	400 W	300 W

Table 1. Output Power Table.

Notes:
1. Maximum practical continuous output power based on the following:
   a. Maximum output current of 10 A.
   b. Schottky or high efficiency output diode.
   c. 130 V reflected voltage (V_{OR}) and 85% efficiency.
   d. A 100 VDC minimum DC bus voltage for 85-265 VAC and 300 VDC bus voltage for 230 VAC.
   e. Sufficient heat sinking to keep device temperature ≤110 °C.
   f. Power levels shown for the K package device assume 19.4 cm^2 of 610 g/m^2 copper heat sink area.
   g. Maximum continuous power for an open frame design operating in a +50 °C ambient temperature.
2. Minimum peak power capability.
3. Packages: E: eSIP-7C, K: eSOP-12B.

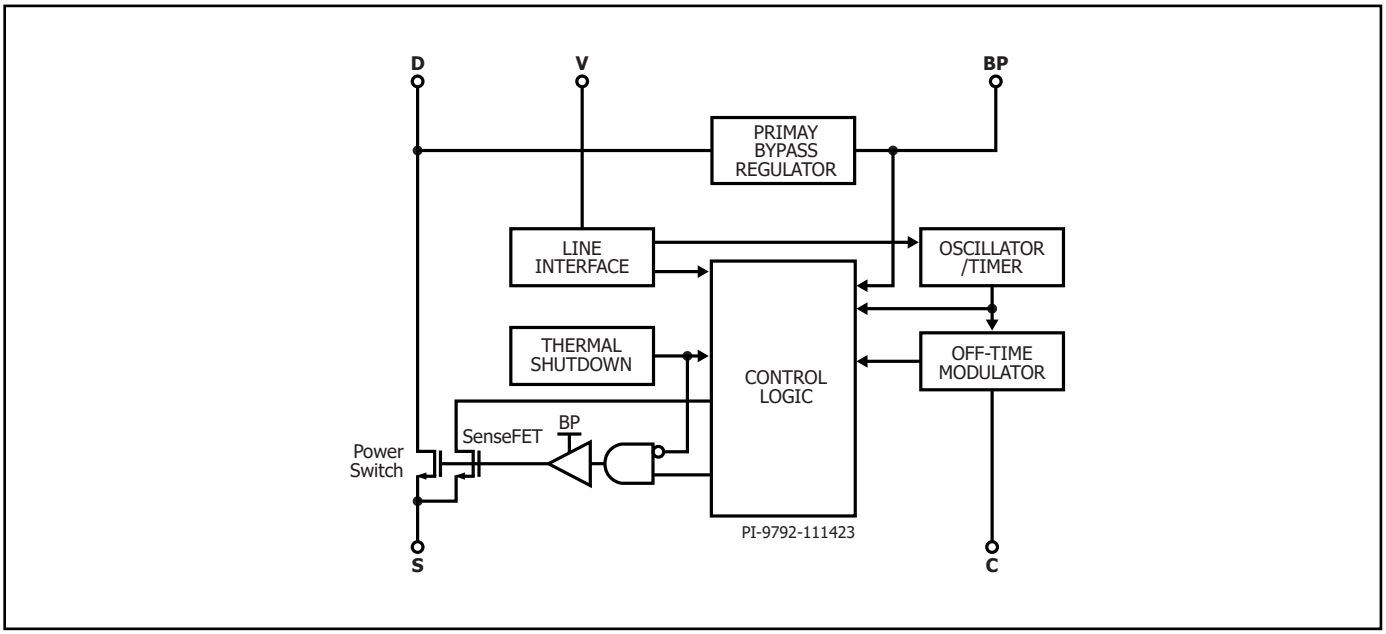


Figure 3. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin
Power switch drain connection.

SOURCE (S) Pin
These pin(s) are the power switch source connection. Also ground reference for BYPASS pin.

BYPASS (BP) Pin
The connection point for an external bypass capacitor for the controller supply.

VOLTAGE MONITOR (V) Pin
Pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

CONTROL (C) Pin
Feedback control current input pin.

SIGNAL GROUND (SG) Pin
SG pin must be connected to Source.

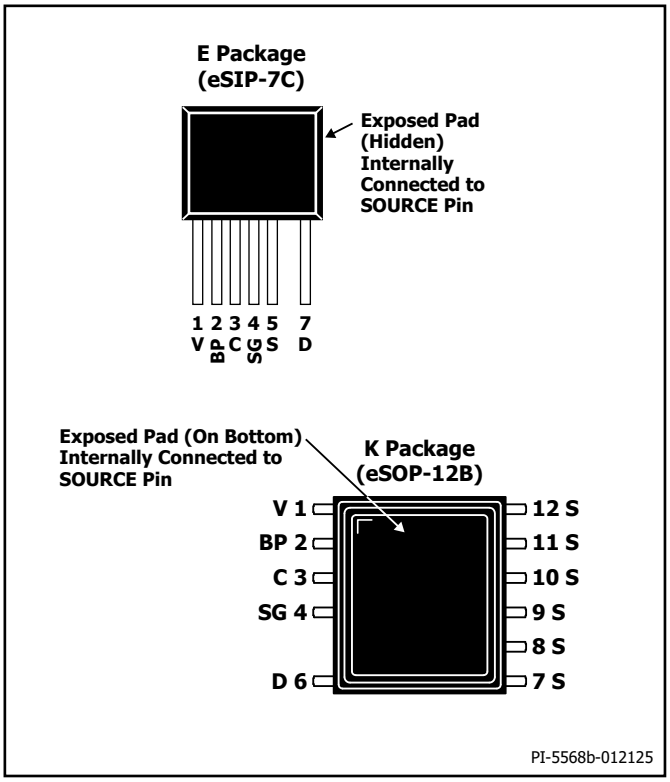


Figure 4. Pin Configuration (Top View).

TOPSwitchGaN Functional Description

The TOPSwitchGaN™ IC is an integrated switched-mode power-supply that monitors an analog feedback current at the control input to modulate the variable-frequency variable-current control.

The TOPSwitchGaN flyback controller can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The controller consists of a frequency-jitter oscillator, a current-limit controller, 5 V regulator on the BYPASS pin, BYPASS undervoltage and overvoltage detection circuit, an input-line sensing circuit, current -limit selection circuitry, over-temperature protection, leading-edge blanking, and a PowiGaN power switch.

BYPASS Pin Regulator

The BYPASS-pin has an internal regulator that charges the BYPASS-pin capacitor to V_{BP} by drawing current from the DRAIN pin whenever the power switch is off. The BYPASS-pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the BYPASS-pin capacitor.

In addition, a shunt regulator clamps the BYPASS-pin voltage to V_{SHUNT} when current is provided to the BYPASS-pin through an external resistor. This allows the TOPSwitchGaN IC to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Bypass Undervoltage Threshold

The BYPASS-pin undervoltage circuitry disables the power switch when the BYPASS-pin voltage drops below ~4.5 V (V_{BP} – $V_{BP(H)}$) in steady-state operation. Once the BYPASS pin voltage falls below this threshold, it must rise to V_{BP} to re-enable turn-on of the power switch.

Bypass Output Overvoltage Function

The BYPASS-pin has an auto-restart OV protection feature. A Zener diode in parallel with the resistor in series with the BYPASS-pin capacitor is typically used to detect an overvoltage on the bias winding and activate the protection mechanism. In the event that the current into the BYPASS pin exceeds I_{SD}, the device will disable switching.

Over-Temperature Protection

The thermal-shutdown circuitry senses the integrated switch die temperature. The threshold is set to T_{SD} with a hysteretic response.

Hysteresis response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent overheating of the PCB due to a continuous fault condition.

Off-Time Modulator

The off-time modulator converts the analog feedback current to off-time duration, which is proportional to the feedback current. This algorithm produces longer off-time as the output load decreases.

At the end of off-time cycle, the off-time modulator initiates an on-cycle request to turn on the integrated power switch.

Current Limit Operation

The current-limit threshold is proportional to the time between the termination of the previous switching cycle (when the power switch turns off) and the next switching request.

This characteristic produces a current limit that increases as the switching frequency (load) increases as shown in Figure 5.

At high load, switching cycles have a maximum current that approaches 100% I_{LIM}. This gradually decreases to 30% of the full current limit as load decreases. Once the 30% current-limit level is reached, there is no further reduction in current limit. The time between switching cycles will continue to increase as load decreases.

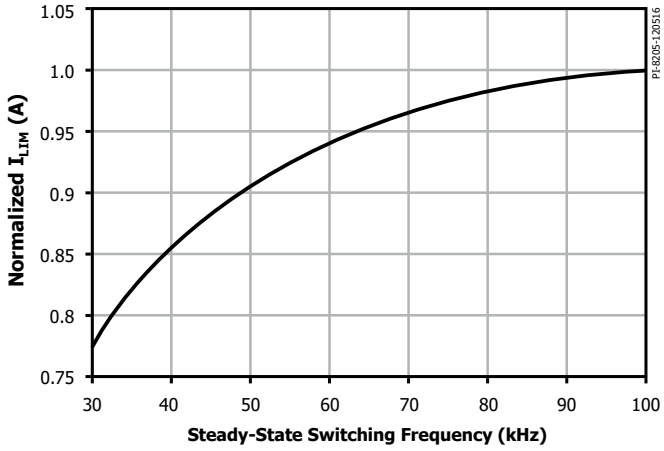


Figure 5. Normalized Current Limit vs Frequency.

Jitter

The normalized current limit is modulated between 100% and 94.5% at a modulation frequency of f_M.

SOA Protection

After two consecutive cycles where the 110% I_{LIM} (100% of I_{LIM} corresponds to the I_{LIM} value at 100 kHz) is reached between t_{LEB_SOA} ~ 250 ns and t_{SOA_ON} ~ 400 ns, the controller interrupts switching for approximately 40 µs, which is equivalent to approximately 6 cycles at the maximum 150 kHz switching frequency. This provides sufficient time for the transformer to reset when delivering power to large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The VOLTAGE MONITOR (V) pin is used for input undervoltage and overvoltage sensing and protection.

An 8 MΩ resistor is connected between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier along with suitable diode rectification for fast AC reset) and the VOLTAGE MONITOR pin to enable this functionality. This function can be disabled by shorting the VOLTAGE MONITOR pin to the SOURCE pin.

At power-up, after the BYPASS (BP) capacitor is charged and the I_{LIM} state is latched, the state of the VOLTAGE MONITOR pin current is checked to confirm that it is above the brown-in (I_{UV+}) and below the overvoltage shutdown thresholds (I_{OV+}) (prior to switching).

During normal operation, if the VOLTAGE MONITOR-pin current falls below the brown-out threshold (I_{UV-}) and remains below brown-out for longer than t_{UV-}, switching is interrupted. Once the VOLTAGE MONITOR-pin current rises above the brown-in threshold (I_{UV+}), the controller initiates a soft start.

During normal operation, if the VOLTAGE MONITOR pin current rises above the overvoltage threshold (I_{OV+}) for longer than t_{OV+}, switching is interrupted. A soft-start is initiated once the VOLTAGE MONITOR-pin current falls below the recovery threshold.

Maximum On-Time Extension
On-time extension keeps the cycle on until the current limit is reached. If the current limit is not reached by $t_{ONEXT(MAX)}$ = 15 µs, the controller terminates the switching cycle.

This feature reduces the minimum input voltage required to maintain regulation, extending hold-up time and minimizing the size of the required bulk capacitor.

Maximum Switching Frequency
The maximum switching frequency of the controller is f_{OSC}.

Minimum Off-Time
The off-time modulator initiates a cycle request to turn on the integrated PowiGaN switch. The maximum request frequency of off-time modulator is limited by a minimum off time period, $t_{OFF(MIN)}$. This ensures sufficient reset time after the integrated switch conduction interval to deliver energy to the load.

Maximum Duty Cycle
The PowiGaN switch is turned off when the drain current reaches the current limit or when the $t_{ONEXT(MAX)}$ limit is reached.

The controller monitors the on-time of the PowiGaN switch $t_{GaN(ON)}$ and measures the timer $t_{DC(MAX)} = DC_{MAX}/f_{OSC}$ starting from when the PowiGaN switch turns on. If:

- $t_{GaN(ON)} \geq t_{DC(MAX)}$, the off-time modulation starts after the PowiGaN switch is turned off.
- $t_{GaN(ON)} < t_{DC(MAX)}$, the off-time modulation starts after $t_{DC(MAX)}$ timer ends.

Frequency Soft-Start
At start-up, the controller linearly ramps up the switching frequency by reducing the off-time from $T_{OFF(STARTUP)}$ to $T_{OFF(MIN)}$ over the t_{SOFT} time period.

If the CONTROL-pin current I_C rises above the $I_{C(TH)}$ threshold within the t_{SOFT} time period, the frequency ramp is immediately aborted and the controller is permitted to go full frequency. This allows the controller to maintain regulation in the event of a sudden transient loading shortly after regulation is achieved.

If a short-circuit or overload occurs at start-up, and the CONTROL-pin current IC does not rise above the $I_{C(TH)}$ threshold before the t_{AR} interval expires, the controller enters auto-restart (AR) mode.

Application Examples

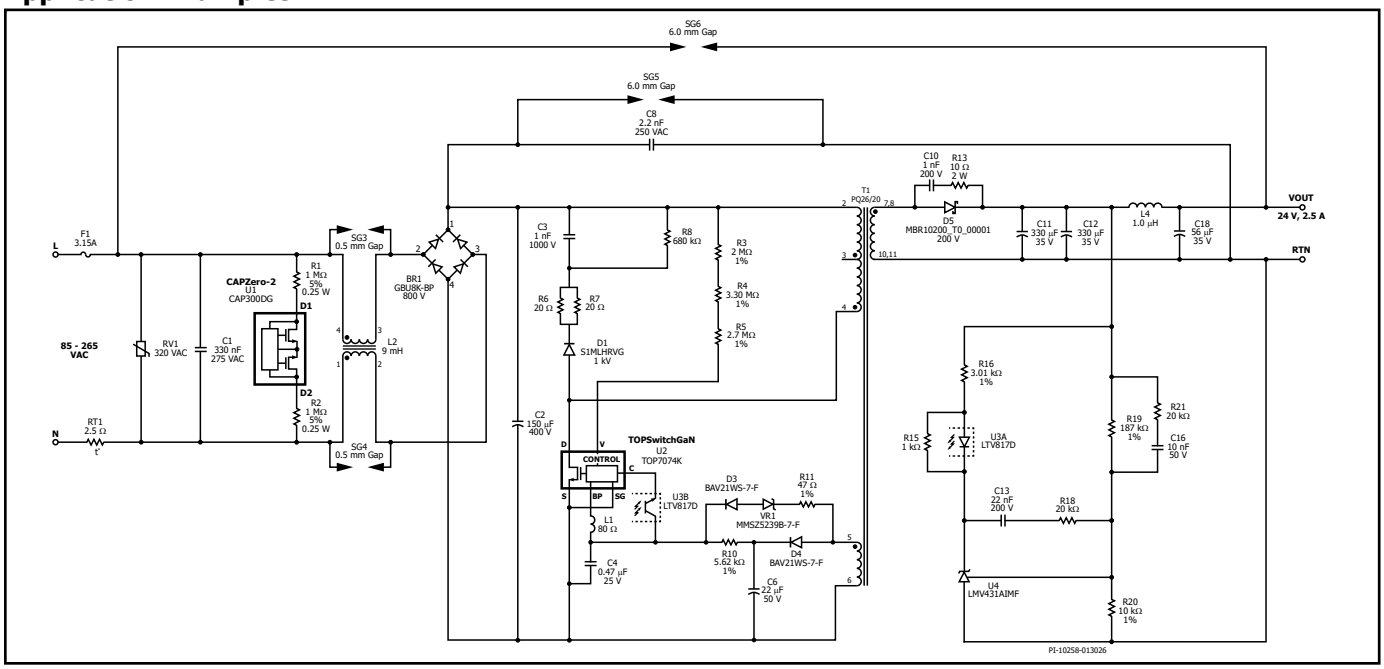


Figure 6. Schematic of DER-1079 60 W, Single Output Power Supply, 24 V / 2.5 A using TOP7074K.

High-Efficiency, 60 W Single Output Power Supply

The circuit shown in Figure 6 delivers 60 W (24 V / 2.5 A) from 85 VAC to 265 VAC using TOP7074K.

The power supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage auto-restart protection, output short-circuit protection, high 115 VAC full load efficiency (>90%), high average efficiency (>88%) and low no-load input power consumption (<100 mW at 230 VAC). Output voltage regulation is accomplished using an optocoupler and a shunt regulator (LM431) feedback.

Fuse F1 isolates the circuit and provides protection from component failure. X-capacitor C1 together with common mode choke (CMC) forms an EMI filter that attenuates both common mode and differential mode conducted EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across bulk capacitor C2. The CAPZero™-2 IC (U1) along with bleed resistors, R1 and R2, discharges the stored energy in X capacitor C1 when AC is disconnected, meeting safety requirements. When AC is connected the resistors are disconnected, reducing no-load power consumption.

The TOP7074K device (U2) integrates an oscillator, a switch controller, start-up and protection circuitry, and PowiGaN switch, all on one monolithic IC. One side of the power transformer (T1) primary winding is connected to the positive side of the bulk capacitor C2, and the other side is connected to the DRAIN pin (D pin) of U2. When the PowiGaN switch turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The spike amplitude is limited by an RCD clamp network that consists of D1, R6, R7, C3 and R8. Resistors R6 and R7 are used together with capacitor C3 and resistor R8 to damp high frequency ringing and improve EMI. This arrangement was selected to reduce clamp losses under light and no-load conditions. Y capacitor C8, connected between the primary and secondary side helps improve EMI.

The TOP7074K regulates the output by adjusting the power PowiGaN switch off-time duration in proportion to the current into its CONTROL pin. The power supply output voltage is sensed on the secondary side by shunt regulator U4 and provides a feedback signal to the primary side through optocoupler U3.

Line undervoltage and overvoltage thresholds are determined by the current supplied from resistors R3, R4 and R5 to the V pin. R11, D3, and VR1 provide output overvoltage protection (OVP). An increase in output voltage causes an increase in the bias winding voltage, sensed by VR1. Once VR1 is activated, it will inject current to the BP pin causing the IC U2 to shut down and enter auto-restart (AR).

At start-up, bypass capacitor C4 is charged through the DRAIN (D) pin, which is placed as close as possible to U2. Once it is charged, U2 begins to switch. Capacitor C4 stores enough energy to ensure the TOPSwitchGaN IC is powered until the output reaches regulation. After start-up, the bias winding delivers current via diode D4 and R10 to charge capacitor C6 which in turn powers the controller. Resistor R10 is used to set the typical bias current of the IC U4. Ferrite bead L1 minimizes the noise on the BP.

Schottky diode D5 rectifies the secondary winding output of T1. The output voltage is filtered by C11, C12, C18 and L4. Resistor R13 and capacitor C10 snubs the voltage spike caused by the commutation of D5. Low ESR capacitors C11, C12 and LC filter L4 and C18 help in minimizing output voltage ripple.

The reference IC, U4 (LMV431AIMF), is used to set the output voltage programmed via the feedback resistor divider composed of R19 and R20. The LMV431AIMF varies its cathode voltage to keep its input voltage constant (1.24 V, ±1%). As the cathode voltage changes, the current through the optocoupler LED and corresponding photo-transistor within U2 changes. R16, C13, R18, R21 and C16 ensure stable operation, while resistor R15 maintains minimum bias to U3.

Key Applications Design Considerations

Output Power Table

The output power table in the data sheet (Table 1) represents the maximum practical continuous output power that can be obtained under the following conditions:

1. Minimum DC input voltage is 85 V or higher for 85 VAC input, and 220 V or higher for 230 VAC input. The input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on input voltage range. Universal input voltage or low-line input assumes efficiency >85% increasing to >89% for a high-line input. The assumed efficiency is based on the lowest voltage of the input range.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain KP > 0.4 at a minimum input voltage to provide the maximum power. At high-line nominal, it recommended to design KP between 1 and 1.1 to increase efficiency.
5. Use low forward voltage drop (V_F) Schottky O/P diode for efficiency improvements.
6. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to maintain the device temperature at or below 110 °C at the required highest ambient temperature.
7. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters is assumed.
8. A unique feature of TOPSwitchGaN IC that a designer can set the operating switching frequency, between 25 kHz to 142 kHz depending on the transformer design. One effective way to lower U2 temperature is to design the transformer to operate at a lower switching frequency, with a good starting point being 66 kHz. If smaller size transformer is needed, the operating switching frequency can be increased to 130 kHz.

Overvoltage Protection

The output overvoltage protection provided by TOPSwitchGaN IC uses an internal protection that is triggered by a threshold current of I_{SD} flowing into the BYPASS pin. In addition to an internal filter the BYPASS pin capacitor forms an external filter, providing noise immunity and preventing inadvertent triggering. To ensure the bypass capacitor is effective as a high-frequency filter, it should be placed as close as possible to the SGND and BYPASS pins of the device.

The primary sensed output OVP can be achieved by connecting a series combination of a Zener diode (VR1), a resistor (R11), and a blocking diode (D3) connected from the bias winding output to the BYPASS pin capacitor (as shown in Figure 6).

The Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered should be selected. A forward voltage drop of 1 V can be assumed for the blocking diode, and a small signal standard recovery diode is recommended. The blocking diode prevents any reverse current from discharging the bias capacitor during start-up. Resistor value must be tuned to filter out ringing spike voltage on the winding. Higher leakage spike on the bias winding will require higher resistance value.

Reducing No-load Consumption

The TOPSwitchGaN IC starts in a self-powered mode, drawing energy from the BYPASS pin capacitor, which is charged from the internal current source. Once the TOPSwitchGaN IC begins switching, a bias winding is required to provide supply current to the BYPASS pin. This bias winding supply enables power supplies to achieve no-load power consumption. The value of resistor R_{BIAS} should be adjusted to achieve the lowest no-load input power.

Additional techniques to further reduce no-load consumption include:

1. Using a low value primary clamp capacitor (C_{PRI_SNUB}).
2. Employing a Schottky or ultrafast diode for the bias supply rectifier (D_{BIAS}).
3. Employing high Current Transfer Ratio optocoupler with a CTR of 300-600% (OPTO)
4. Selecting a low ESR capacitor for bias supply filter capacitor (C_{BIAS}).
5. Selecting low ESR for input bulk capacitor (C_{BULK}) and output filter capacitor (C_{OUT}).
6. Utilizing a low value secondary rectifier diode RC snubber capacitor (C_{SEC_SNUB}).
5. Applying tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter-winding capacitance.

Component Selection

Figure 7 shows the key external components required for a practical single output TOPSwitchGaN design.

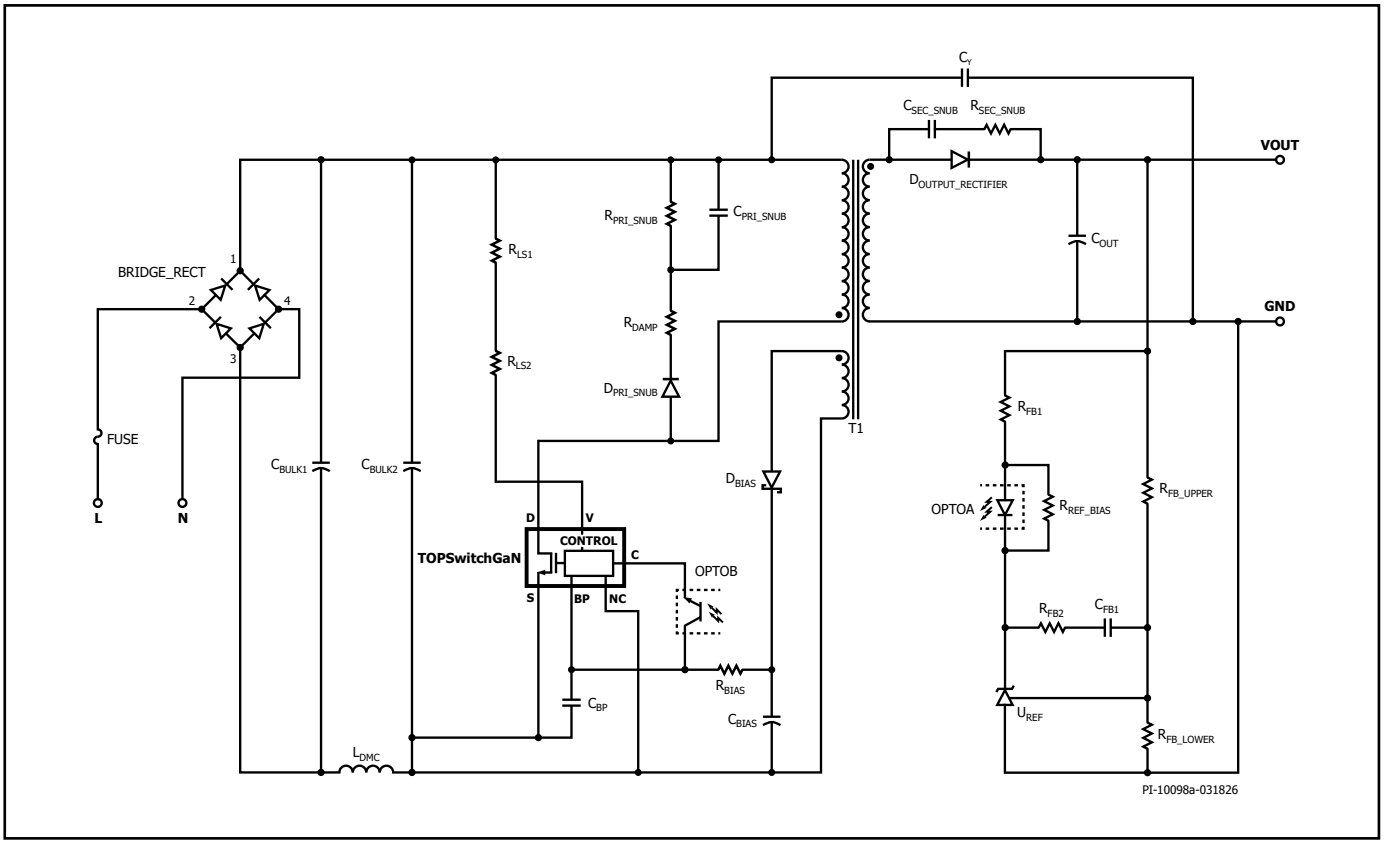


Figure 7. Typical Power Supply Schematic using a TOPSwitchGaN device with Line Undervoltage Lockout and Line Overvoltage Shutdown.

BYPASS Pin Capacitor (C_{BP})

A capacitor connected from the BYPASS pin (BP) of the TOPSwitchGaN IC to SGND provides decoupling for the primary controller and selects the current limit. A 0.47 µF capacitor may be used. While electrolytic capacitors are an option, surface mount multi-layer ceramic capacitors are often preferred for double-sided boards as they can be placed close to the IC. Their small size also makes them ideal for compact power supplies. At least 10 V, 0805 or larger size X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met. Note that ceramic capacitor type designations, such as X7R and X5R, can vary in voltage coefficients across different manufacturers or product families. It is advisable to review capacitor data sheets to ensure the selected capacitor does not experience more than a 20% drop in capacitance at 5 V. Avoid using Y5U or Z5U / 0603 rated MLCCs, as they have poor voltage and temperature coefficient characteristics.

V Pin Line Sense Resistors (R_{LS1} and R_{LS2})

Resistors connected from the V pin to the DC bus enable input voltage sensing for line undervoltage and overvoltage protection. For a typical universal input application, a total resistor value of 8 MΩ is recommended. For high-line input, it is advisable to use two 0.25 W SMD 1206 resistors or leaded resistors in series, each with a value of 4 MΩ. Connecting the V pin to SOURCE disables the line sensing function. It is not recommended to leave the V pin floating.

Primary Clamp (D_{PRI_SNUB}, R_{DAMP}, R_{PRI_SNUB}, C_{PRI_SNUB})

Refer to Figure 7. An RRCD clamp is a commonly used clamp in low-power power supplies. For higher power designs, a Zener clamp or RRCD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 90% of the device absolute DRAIN voltage rating under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit).

The clamp diode (D_{PRI_SNUB}) must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of less than 500 ns. Using standard recovery glass passivated diodes allows recovery of some of the clamped energy in each switching cycle, improving light-load and average efficiency. The diode conducts momentarily each time the MOSFET inside TOPSwitchGaN turns off, transferring the stored energy from the leakage reactance and the clamp capacitor C_{PRI_SNUB} to the output.

Resistor R_{DAMP}, in the series path, provides damping preventing excessive ringing due to resonance between the leakage inductance and the MOSFET switch output capacitance C_{OSS}. Resistor R_{PRI_SNUB} bleeds-off energy stored in the capacitor C_{PRI_SNUB}. Power supplies using different TOPSwitchGaN devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor C_{PRI_SNUB} and resistor R_{PRI_SNUB} and R_{DAMP} must therefore be optimized for each design.

As a general rule, it is advisable to minimize the value of capacitor C_{PRI_SNUB} and maximize the value for R_{PRI_SNUB} and R_{DAMP}, while ensuring the MOSFET DRAIN voltage remains below 90% of its absolute maximum limit at the highest input voltage and maximum load. The value of R_{DAMP} should be large enough to damp the ringing within the required time. However, as the value of R_{DAMP} increases the DRAIN peak voltage and its power dissipation also increase. Therefore, care must be taken to keep the DRAIN voltage below 90% of its maximum absolute limit. The recommended range for R_{DAMP} is 47 Ω to 100 Ω. While the recommended range for R_{PRI_SNUB} is 100 kΩ to 470 kΩ.

Using a disc ceramic capacitor with dielectric such as Z5U in the clamp circuit for C_{PRI_SNUB} may generate audible noise, therefore a polyester film type or a ceramic capacitor with X7R as a dielectric, 1 kV rating, 1206 size is commonly used. The recommended range for C_{PRI_SNUB} is 470 pF to 1 nF.

Bias Winding and External Bias Supply Circuit (D_{BIAS}, C_{BIAS}, R_{BIAS})

The internal primary bypass regulator connected from the DRAIN pin to the BYPASS pin of the TOPSwitchGaN device charges the capacitor C_{BP} connected to the BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can supply at least 1.7 mA of current to the BYPASS pin and C pin.

A bias voltage of 12 V is recommended at full load. Higher voltage will increase no-load input power. To reduce no-load consumption and improve standby input efficiency, ultrafast or Schottky diodes are recommended for the bias winding rectifier. The turns ratio for the bias winding should be selected such that 10 V is developed across the bias winding at the lowest rated output voltage of the power supply under the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to slightly higher than I_{S1} of 355 µA to achieve the lowest no-load power consumption when operating the power supply at 230 VAC input. This can be achieved by fine tuning the value of R_{BIAS} resistor. After tuning the resistor, check VBP voltage across load condition. V_{BP} level should be near V_{SHUNT} to ensure that enough bias current is supplied to the device during switching condition. If V_{BP} level is less than V_{SHUNT}, drain tap circuit can turn-on during and will cause increase in case temperature rise of the device.

A glass-passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes, which can lead to higher radiated EMI.

An aluminum low ESR electrolytic capacitor of at least 47 µF and 25 V rating is recommended for the bias filter capacitor C_{BIAS}. A 47 µF low ESR electrolytic capacitor will help to improve the no-load input power and standby input power efficiency. The use of ceramic surface mount capacitors is not recommended, as they can cause audible noise due to the piezoelectric effect in their mechanical structure.

Secondary Output Rectifier Diode ($D_{OUTPUT\_RECTIFIER}$)

The output diode is selected based on peak inverse voltage, output current, and thermal conditions in the application, including heatsinking and air circulation. The higher DC_{MAX} of the TOPSwitchGaN device, combined with an appropriate transformer turns ratio, allows the use of an 80 V Schottky diode for higher efficiency at output voltages up to 15 V.

Considerations for selecting an output rectifier diode:

- Ensure the reverse voltage rating (V_R) is at least 1.25 times the peak inverse voltage (PIV).
- Select a diode with a current rating (I_D) that is at least twice the output current (I_{OUT}).

Output Filter Capacitance (C_{OUT})

A low ESR electrolytic capacitors is one of the key requirements in smoothing output ripple voltage. Other parameters to be considered are the RMS ripple current rating, DC working voltage and ESR. The actual capacitance value is of less importance.

Considerations for Selection of Output Capacitor:

- Ensure the capacitor ripple is specified @ 105 ºC, 100 kHz must be larger than the expected ripple current (IS_{RIPPLE}).
- Use a low ESR (Equivalent Series Resistance) electrolytic capacitor to minimize output switching ripple voltage, which is calculated using $V_{RIPPLE} = IS_{RIPPLE}$ x ESR.
- Select a capacitor with a voltage rating such that the rated voltage is at least 1.25 times the output voltage (V_{OUT}).

Output Post Filter Components (L_{PF} and C_{PF}):

A post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple.

Considerations for Adding a Post Filter:

- The inductor (L_{PF}) should have an inductance value in the range of 1 µH to 3.3 µH and a current rating that exceeds the peak output current.
- The capacitor (C_{PF}) should have a capacitance value in the range of 100 µF to 330 µF and a voltage rating that is at least 1.25 times the output voltage (V_{OUT}).
- If a post filter is used, ensure that the output voltage sense resistor and optocoupler are connected before the post filter inductor. See Figure 9.

Recommendations for Circuit Board Layout

For this section refer to Figures 8 to 11

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. The C_{BIAS} ground should have a dedicated trace that is star-connected to the input filter capacitor ground pin.

Bypass Capacitors
The BYPASS pin decoupling capacitor (C_{BP}) must be located directly adjacent to the BYPASS and SOURCE pins. Ensure the connections should be routed via short traces.

Critical Loop Area
Circuits with high dv/dt or di/dt should be kept as small as possible. Minimize the area of the primary loop that connects the input filter capacitor, transformer primary, and IC. Similarly, reduce the area of the loop connecting the secondary winding, output rectifier diode, and output filter capacitor.

Ensure that no loop area is placed inside another loop to minimize crosstalk between circuits.

Drain Node
The drain switching node is the dominant noise generator. Therefore, components connected to the drain node should be placed close to the IC and away from sensitive primary control circuits. The clamp circuit components should be physically located away from the BYPASS pin.

Power Trace Routing
Current will flow through the path of least resistance. Even if the trace is connected to the capacitors, there is a possibility that the current may bypass them, rendering the capacitors ineffective. For effective filtering and noise immunity, it is recommended that power signal traces be star-connected to the capacitor's pads.

Primary Clamp Circuit
A clamp is used to limit the peak voltage on the DRAIN pin during turn-off. This can be achieved by using an R2CD or R2CDZ clamp across the primary winding. To reduce EMI, minimize the loop area between the clamp components, the transformer, and the IC.

Y Capacitor
The Y capacitor should be placed directly from the positive terminal of the primary input filter capacitor to the output positive or return terminal of the transformer secondary. This placement will route high-magnitude common mode surge currents away from the IC. If an input π EMI filter (C_{BULK1}, L_{DMC}, C_{BULK2}) is used, the inductor should be placed between the negative terminals of the input filter capacitors.

ESD Immunity
Sufficient clearance should be maintained between the primary-side and secondary-side circuits to ensure compliance with ESD and hi-pot isolation requirements. The spark gap should be placed between the output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration, a 6.4 mm spark gap (5.5 mm is acceptable, depending on customer requirements) is sufficient to meet the creepage and clearance requirements of most safety standards for a universal input power supply. For effective ESD immunity, the spark gap spacing should be the closest distance between the primary and secondary sections.

A spark gap across the common-mode choke or inductor provides a low impedance path for high-energy discharges due to ESD or common-mode surges.

Secondary Rectifier Diode
For optimal performance, the loop area connecting the secondary winding, secondary rectifier diode, and output filter capacitor should be minimized. When using SMD diodes, ensure sufficient copper area at the terminals of the secondary rectifier diode for heat dissipation. A heatsink may be required for the secondary diode.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and exposed pad at the bottom of the IC for K package which serves as the main path for heat removal. It is recommended to maximize the source pad area in the PCB for effective heat dissipation without causing EMI issues.

For E packages, the exposed pad at the back of the IC is used to attach a heatsink. A heatsink is necessary to ensure the IC operates safely below the absolute maximum junction temperature limit.

Sufficient copper area or a heatsink should be provided on the board to maintain the IC temperature safely below absolute maximum limits. It is recommended that the copper area or heatsink keeps the IC temperature below 110°C when operating the power supply at full rated load, the lowest rated input AC supply voltage, and system's maximum operating ambient temperature. Further de-rating can be applied as needed.

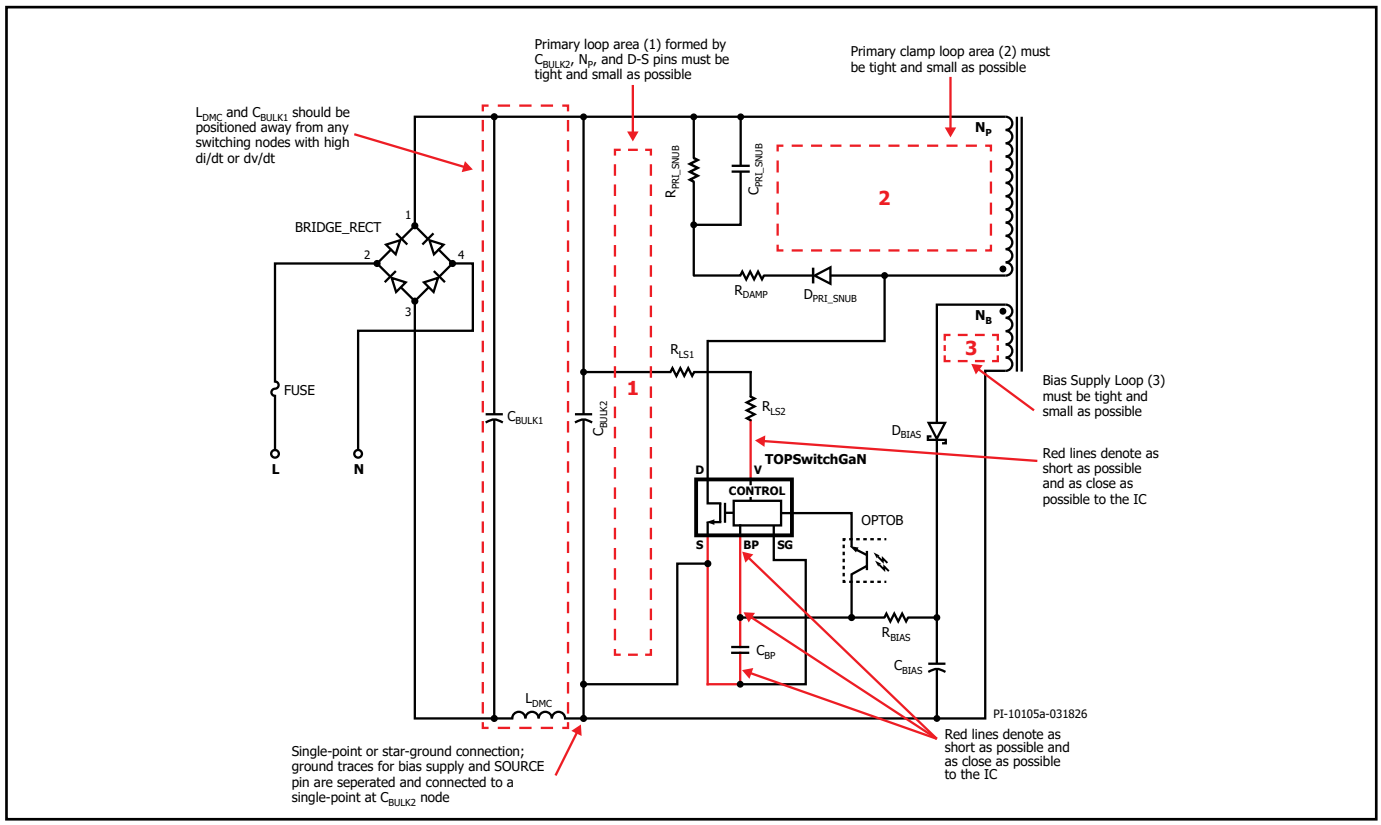


Figure 8. Typical Schematic of TOPSwitchGaN device Primary-Side Showing Critical Loops Areas, Critical Component Traces, and Single-Point or Star Grounding.

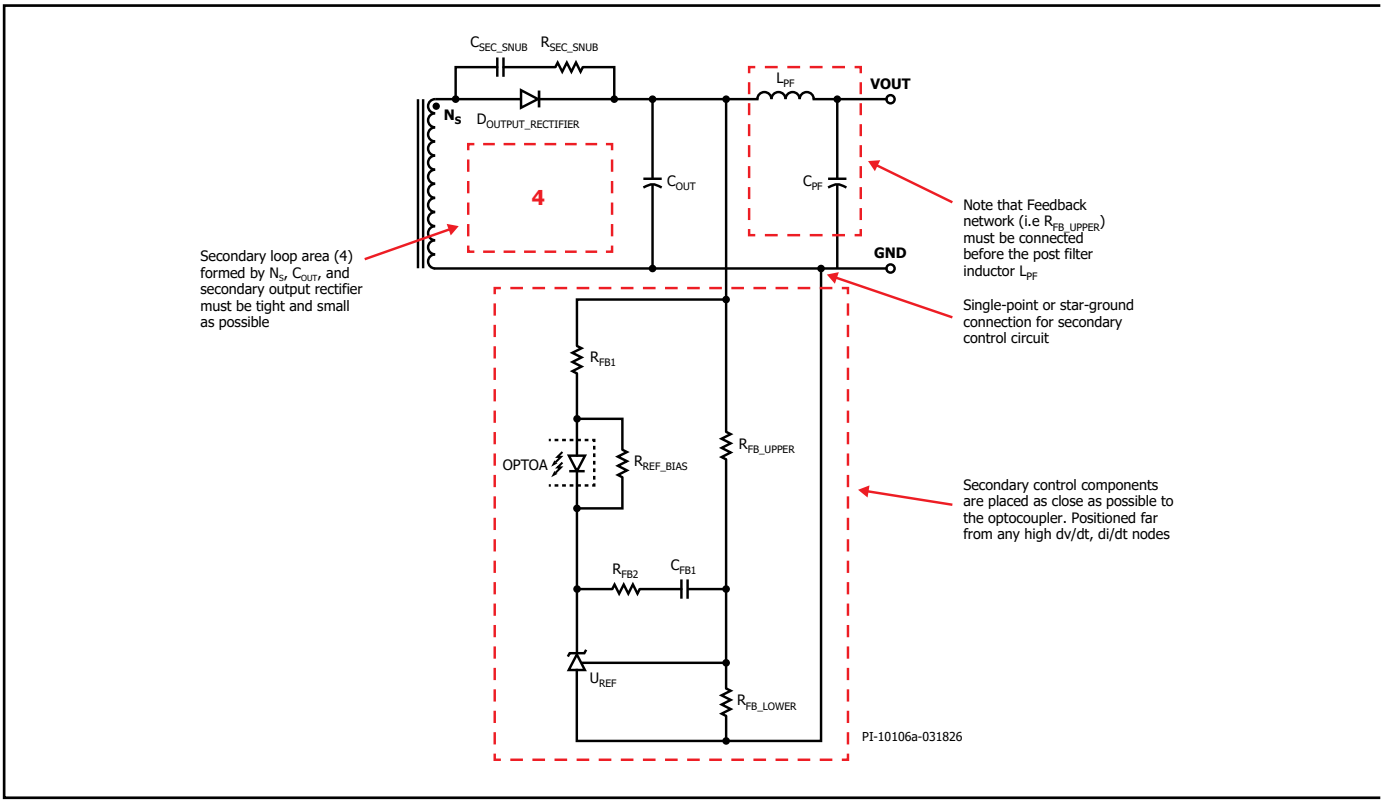


Figure 9. Typical Schematic of TOPSwitchGaN device Secondary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding. Optional Post LC filter included.

Layout Example

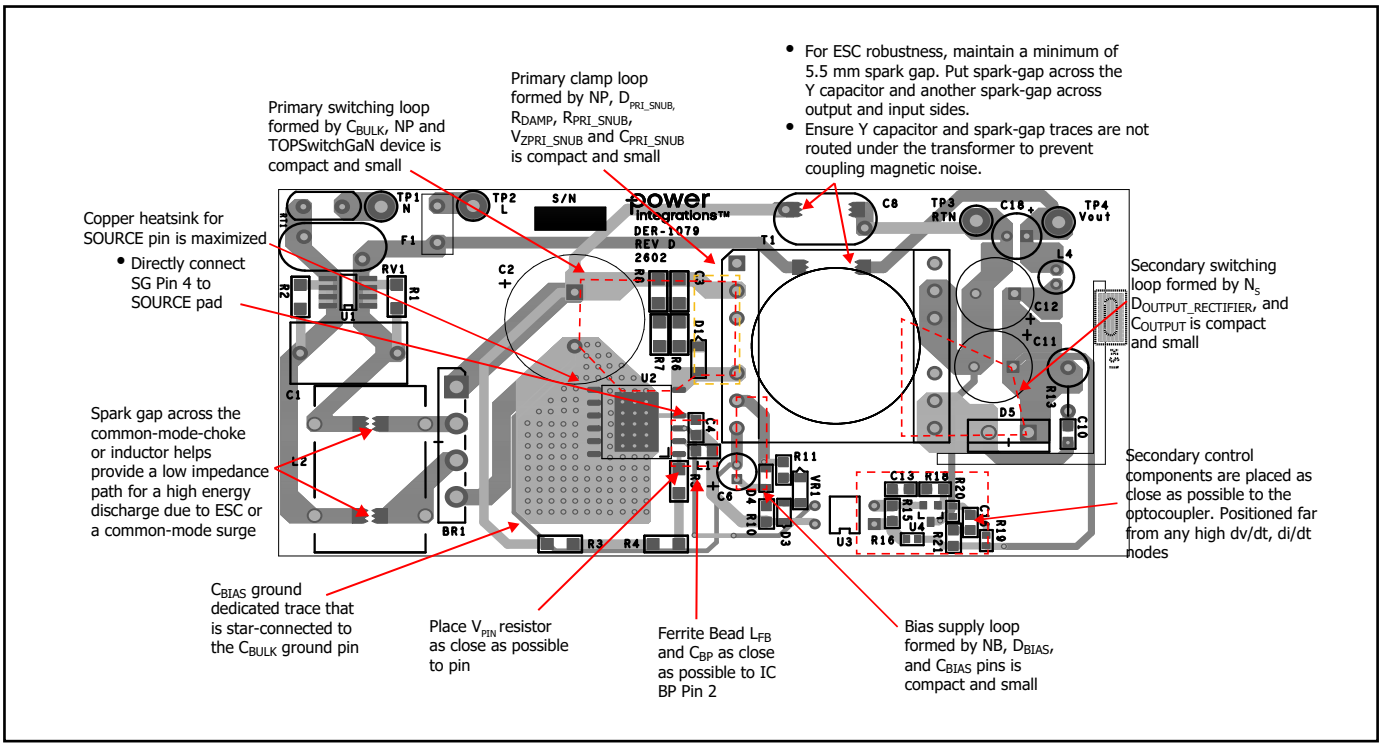


Figure 10. TOP and BOTTOM Sides – Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TOPSwitchGaN device K-package.

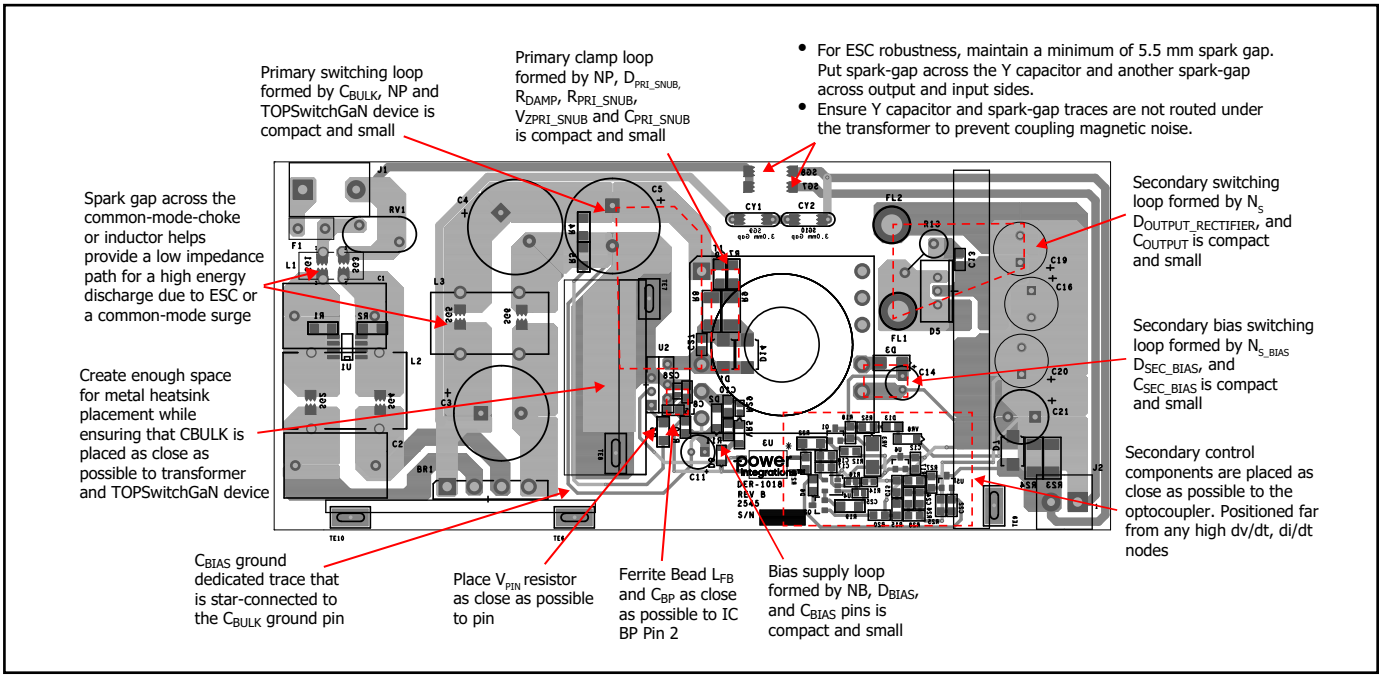


Figure 11. TOP and BOTTOM Sides – Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TOPSwitchGaN device E-package.

Special Notes on PCB Layout

- Ensure all loops are separated, with no loop inside another loop, to avoid ground impedance noise coupling.
- Minimize the surface area and length of high dv/dt nodes, such as the Drain, to reduce RFI (Radio Frequency Interference) generation.
- Avoid routing quiet signal traces, such as those for Y capacitors and feedback returns, near or across noisy nodes (high dv/dt or di/dt), such as the Drain, underneath the transformer belly, the switching side of any winding, or the output rectifier diode. This helps prevent capacitive or magnetic noise coupling.

Recommendation for EMI Reduction

1. Ensure appropriate component placement and minimize loop areas of the primary and secondary power circuits to reduce radiated and conducted EMI. Aim for a compact loop area.
2. Adding a small capacitor in parallel with the clamp diode on the primary side can help reduce radiated EMI.
3. A resistor in series with the bias winding can help reduce radiated EMI.
4. Common mode chokes (CMC) are often required at the power supply input to attenuate common mode noise. Alternatively, shield windings on the transformer can achieve similar performance. Shield windings can also be used with common mode filter inductors at the input to improve conducted and radiated EMI margins.
5. Adjusting the RC snubber component values of the secondary rectifier diode can help reduce high frequency radiated and conducted EMI.
6. Use a pi-filter comprising differential inductors and capacitors in the input rectifier circuit to reduce low-frequency differential EMI.
7. Connecting a 1 μF ceramic capacitor at the power supply output helps reduce radiated EMI.

Recommendation for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the bulk capacitor used. It is recommended to use at least 2 μF/W to maintain the DC bus voltage above 90 V, though 3 μF/W provides the typical margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

Reflected Output Voltage, VOR (V)

This parameter represents the secondary winding voltage during the diode conduction time, reflected to the primary through the transformer's turns ratio. The default value is 120 V, but VOR can be adjusted to achieve a design that adheres to design rules. For design optimization, consider the following factors:

- Higher VOR allows increased power delivery at VMIN, minimizing the value of the input capacitor and maximizing power delivery.
- Higher VOR reduces voltage stress on the output diodes, potentially allowing for a lower voltage rating and higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary side, potentially increasing secondary side copper and diode losses, thereby reducing efficiency.

It should be noted that there are exceptions to this guidance, especially for very high output currents where the VOR should be reduced to achieve the highest efficiency. For higher output voltages (above 15 V), a higher VOR should be employed to maintain an acceptable peak inverse voltage (PIV) across the output diode.

Optimal selection of the VOR value depends on the specific application and involves a compromise between the factors mentioned above.

Ripple to Peak Current Ratio (KP)

A KP below 1 indicates continuous-conduction mode, where KP is the ratio of ripple current to peak primary current (Figure 13).

$$KP = K_{RP} = \frac{I_R}{I_P}$$

A KP value higher than 1 indicates discontinuous conduction mode. In this case, KP is the ratio of primary switch off-time to secondary diode conduction time.

$$KP = K_{DP} = \frac{(1 - D) \times T}{t} = \frac{VOR \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

It is recommended to use a KP close to 0.9 at the minimum expected DC bus voltage for most TOPSwitchGaN device designs. A KP value of less than 1 results in higher transformer efficiency by lowering the primary RMS current but leads to higher switching losses in the primary-side switch, resulting in a higher TOPSwitchGaN device temperature.

The PIXls spreadsheet can be used to effectively optimize the selection of KP, the inductance of the primary winding, the transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

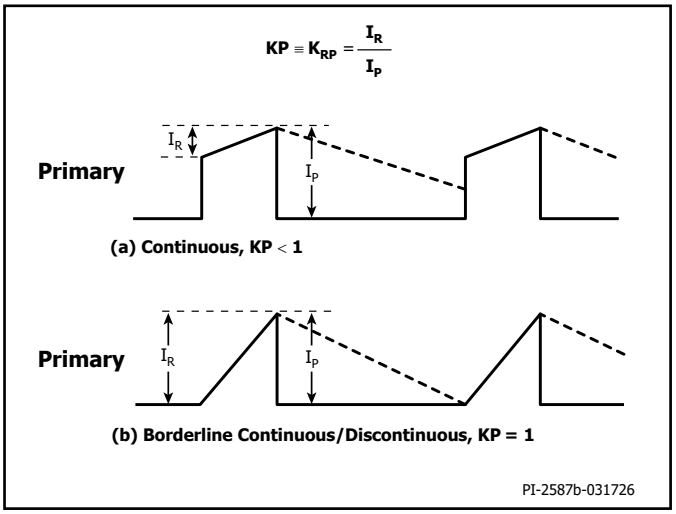


Figure 12. Continuous Conduction Mode Current Waveform, KP < 1.

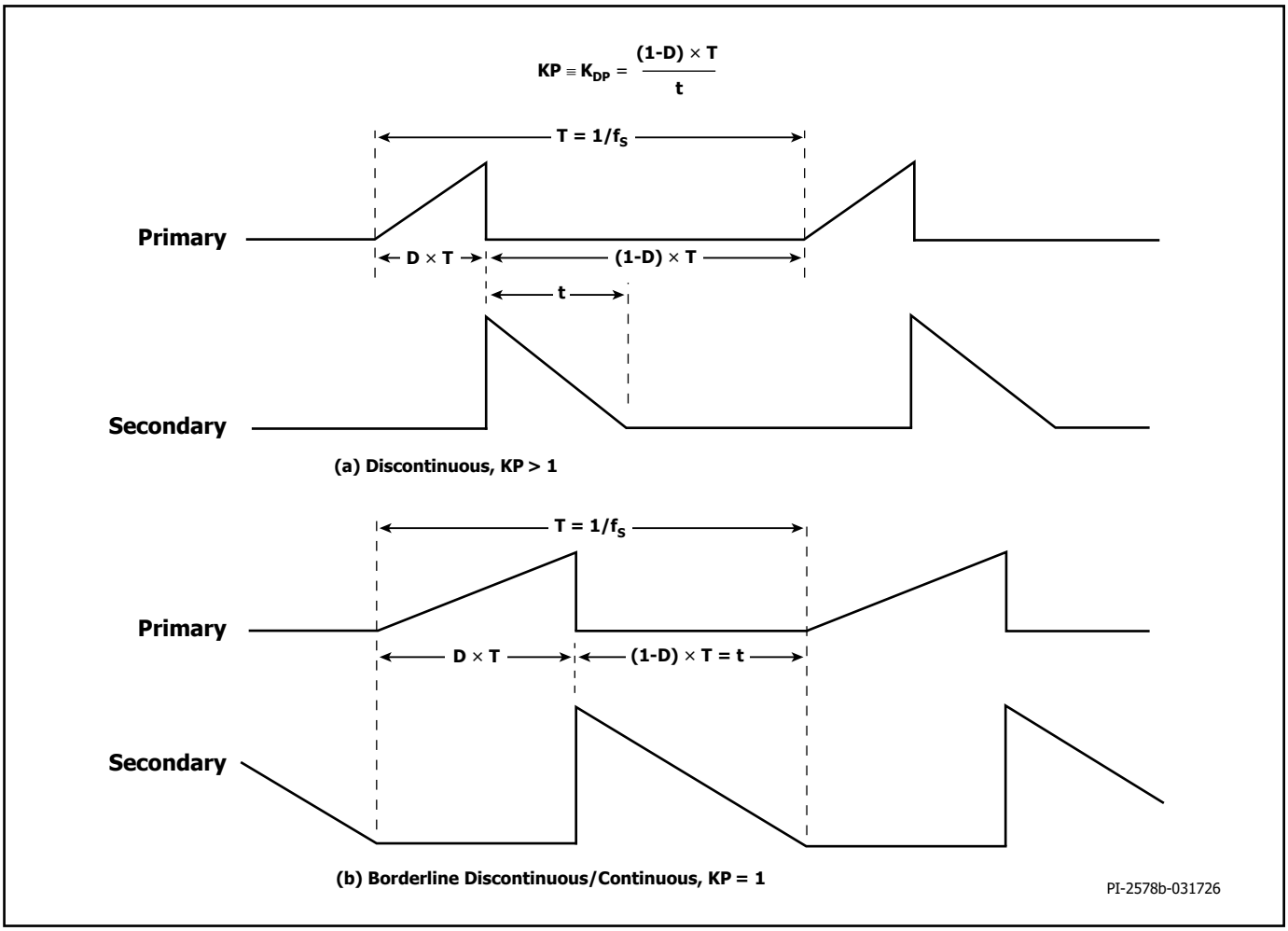


Figure 13. Discontinuous Conduction Mode Current Waveform, KP > 1.

Maximum Flux Density, B_M (Gauss)
A maximum value of 3800 gauss at the peak device current limit is recommended to limit the peak flux density during start-up and under output short-circuit conditions. Under these conditions, the output voltage is low, and there is minimal reset of the transformer during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device, combined with the built-in protection features of the TOPSwitch IC, provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions

Transformer Primary Inductance, L_P
Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

Core Type
The choice of a suitable core depends on the physical constraints of the power supply enclosure. It is recommended to use only low-loss cores to minimize thermal challenges.

Safety Margin, MARGIN (mm)
For designs that require safety isolation between primary and secondary but are not using triple insulated wire the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical; however, if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin were only present on one side of the bobbin. For designs using triple insulated wire it may still be necessary to enter a small margin to meet the required safety creepage distances. Typically, several bobbins exist for each core size, and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required.

Margin reduces the available area for the windings, marginated construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero-margin approach using triple insulated wire.

Primary Layers, L
Primary layers should be in the range of 1 to 3, with the lowest number that meets the primary current density limit (CMA) being preferred. A value of ≥200 Circular-mils/Amp can be used as a starting point for most designs, though higher values may be required due to thermal constraints. Designs with more than three layers are possible, but increased leakage inductance and the physical fit of the windings should be considered.

A split primary construction may be beneficial for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. However, this arrangement can be disadvantageous for low power designs as it typically increases common mode noise and adds cost to the input filtering.

Quick Design Checklist

As with any power supply, the operation of all TOPSwitchGaN designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage
Verify that V_{DS} of TOPSwitchGaN device does not exceed 650 V during normal operating condition. TOPSwitchGaN V_{DS} and reverse voltage of the secondary rectifier diode should not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current
At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review Drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB\ (MIN)}$. Under all conditions, the maximum Drain current for the primary MOSFET should be below the specified absolute maximum ratings.

Thermal Check
At the specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for TOPSwitchGaN IC, transformer, bridge rectifier, secondary rectifier Diode, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of MOSFET $R_{DS(ON)}$. At low-line, maximum power, a maximum TOPSwitchGaN IC temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

Design Support
Up-to-date information on design support can be found at the Power Integrations website: www.power.com

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: TOP7074, TOP7075, TOP7078 ..... -0.3 V to 800 V
DRAIN Pin Peak Current: TOP7074 ..... 6.50 A[3]
TOP7075 ..... 10.0 A[3]
TOP7078 ..... 26.0 A[3]
BP Pin Voltage ..... -0.3 to 6 V
BP Pin Current ..... 100 mA
V Pin Voltage ..... -0.3 V to 6 V
C Pin Voltage ..... -0.3 V to 6 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Maximum Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and SIGNAL GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. TBD.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for 5 seconds.
6. Maximum drain voltage (non-repetitive pulse); for derating Calculation ..... -0.3 V to 800 V
Maximum continuous drain voltage ..... -0.3 V to 650 V

Thermal Resistance

Thermal Resistance: E Package
(θ_{JA}) ..... 105 °C/W[1]
(θ_{JC}) ..... 2 °C/W[2]
K Package
(θ_{JA}) ..... 45 °C/W[3], 38 °C/W[4]
(θ_{JC}) ..... 2 °C/W[2]

Notes:
1. Free standing with no heat sink.
2. Measured at the back surface of tab.
3. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
4. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 1 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Start-Up Off-Time	$T_{OFF(STARTUP)}$	T_J = 25 °C		30	45	µs
Maximum Operating Frequency	f_{OSC}	T_J = 25 °C	139	150		kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 150 kHz		0.22		kHz
Maximum Duty Cycle	DC_{MAX}	T_J = 25 °C	59	69		%
Maximum On-Time Extension	$T_{ONEXT(MAX)}$	T_J = 25 °C	12.5	15		µs
Minimum Off-Time	$T_{OFF(MIN)}$	T_J = 25 °C	1.32	2.2	2.70	µs
Soft-Start Time	T_{SOFT}	T_J = 25 °C		6.26		ms
CONTROL Current No Switching	$I_{C(NOSWITCHING)}$	T_J = 25 °C		290	450	µA
C Pin Voltage	V_C	T_J = 25 °C I_C = 300 µA		2.04	2.20	V
CONTROL Current Auto-Restart and End Soft-Start Threshold	$I_{C(TH)}$	T_J = 25 °C See Note B		18		µA

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BP Supply Current	I_{S1}	$V_{BP} = V_{BP} + 0.1$ V (Switch not Switching) T_J = 25 °C			258	355	µA
	I_{S2}	$V_{BP} = V_{BP} + 0.1$ V (Switch Switching at 150 kHz) T_J = 25 °C	TOP7074		1.70	2.04	mA
			TOP7075		2.49	3.00	
			TOP7078		3.77	4.53	
BP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-2.55	-1.49	-1.05	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-6.1	-4.60	-4.1	
BP Pin Voltage	V_{BP}	T_J = 25 °C		4.75	4.95	5.15	V
BP Pin Voltage Hysteresis	$V_{BP(H)}$	T_J = 25 °C			0.5		V
BP Shunt Voltage	V_{SHUNT}	I_{BP} = 2 mA T_J = 25 °C		5.15	5.36	5.65	V
BP Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$	T_J = 25 °C		2.5	3.2	3.8	V
V Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		10.9	12.3	13.3	µA
V Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		9.2	10.4	11.4	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			36		ms
V Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		53.2	55.8	58.6	µA
V Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			3.9		µA
V Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		49			µA
Line Fault Protection							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
V Pin Voltage	V_V	T_J = 25 °C I_V = 45 µA		2.2	2.6	3.0	V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Standard Current Limit (BP) Capacitor 0.47 µF See Note C	I_{LIMIT} (Switch Switching at 150 KHz)	di/dt = 475 mA/µs T_J = 25 °C	TOP7074K	1760	1900	2040	mA
		di/dt = 532 mA/µs T_J = 25 °C	TOP7075K	1980	2130	2280	
		di/dt = 953 mA/µs T_J = 25 °C	TOP7078K	3543	3810	4077	
		di/dt = 875 mA/µs T_J = 25 °C	TOP7074E	3255	3500	3745	
		di/dt = 1125 mA/µs T_J = 25 °C	TOP7075E	4185	4500	4815	
		di/dt = 2125 mA/µs T_J = 25 °C	TOP7078E	7900	8500	9100	
Auto-Restart On-Time	t_{AR}	T_J = 25 °C			66		ms
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C			1.2		sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note B			0.35		sec
BYPASS Pin Fault Shut-Down Threshold Current	I_{SD}	T_J = 25 °C TOP7074		5.47	7.51	9.54	mA
		T_J = 25 °C TOP7075		5.60	7.68	9.76	
		T_J = 25 °C TOP7078		6.00	8.08	10.00	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	TOP7074 $I_D = I_{LIMIT}$	T_J = 25 °C		0.52	0.68	Ω
			T_J = 100 °C		0.78	1.02	
		TOP7075 $I_D = I_{LIMIT}$	T_J = 25 °C		0.35	0.46	
			T_J = 100 °C		0.49	0.64	
		TOP7078 $I_D = I_{LIMIT}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.34	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BP} = V_{BP} + 0.1$ V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BP} = V_{BP} + 0.1$ V V_{DS} = 80% Peak Drain Voltage T_J = 25 °C			15		µA
Drain Supply Voltage		See Note A		30			V
Thermal Shutdown	T_{SD}	See Note B, D		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note B, D			70		°C

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF capacitors are used. In addition, the BP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The operation of the device with the minimum and maximum capacitor values shown are guaranteed by characterization.
D. Refer to the switch temperature.

Nominal BP Pin Capacitor Value	BP Capacitor Minimum	Value Tolerance Maximum
0.47 µF	-60%	+100%

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

Typical Performance Curves

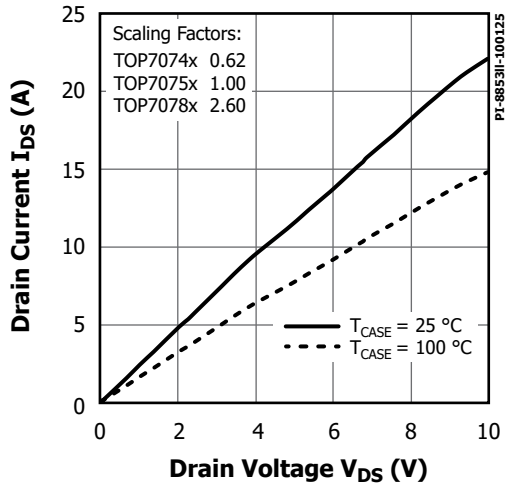


Figure 14. Output Characteristics.

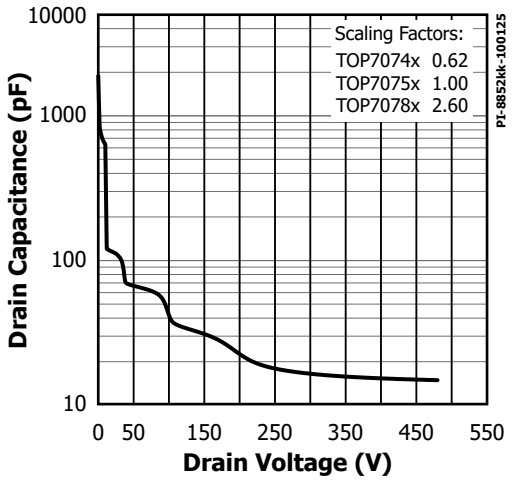


Figure 15. C_{OSS} vs. Drain Voltage.

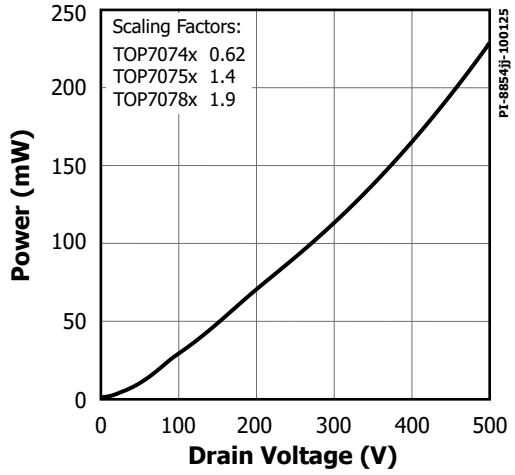


Figure 16. Drain Capacitance Power.

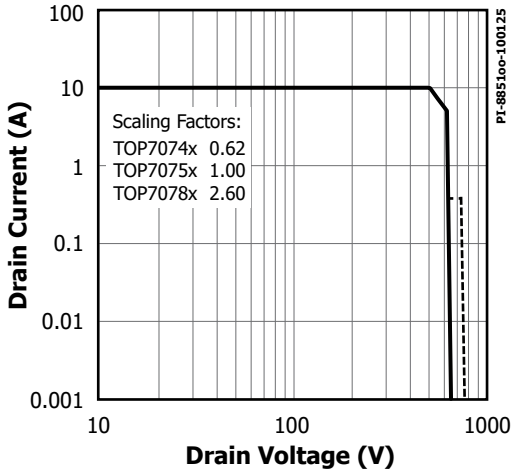
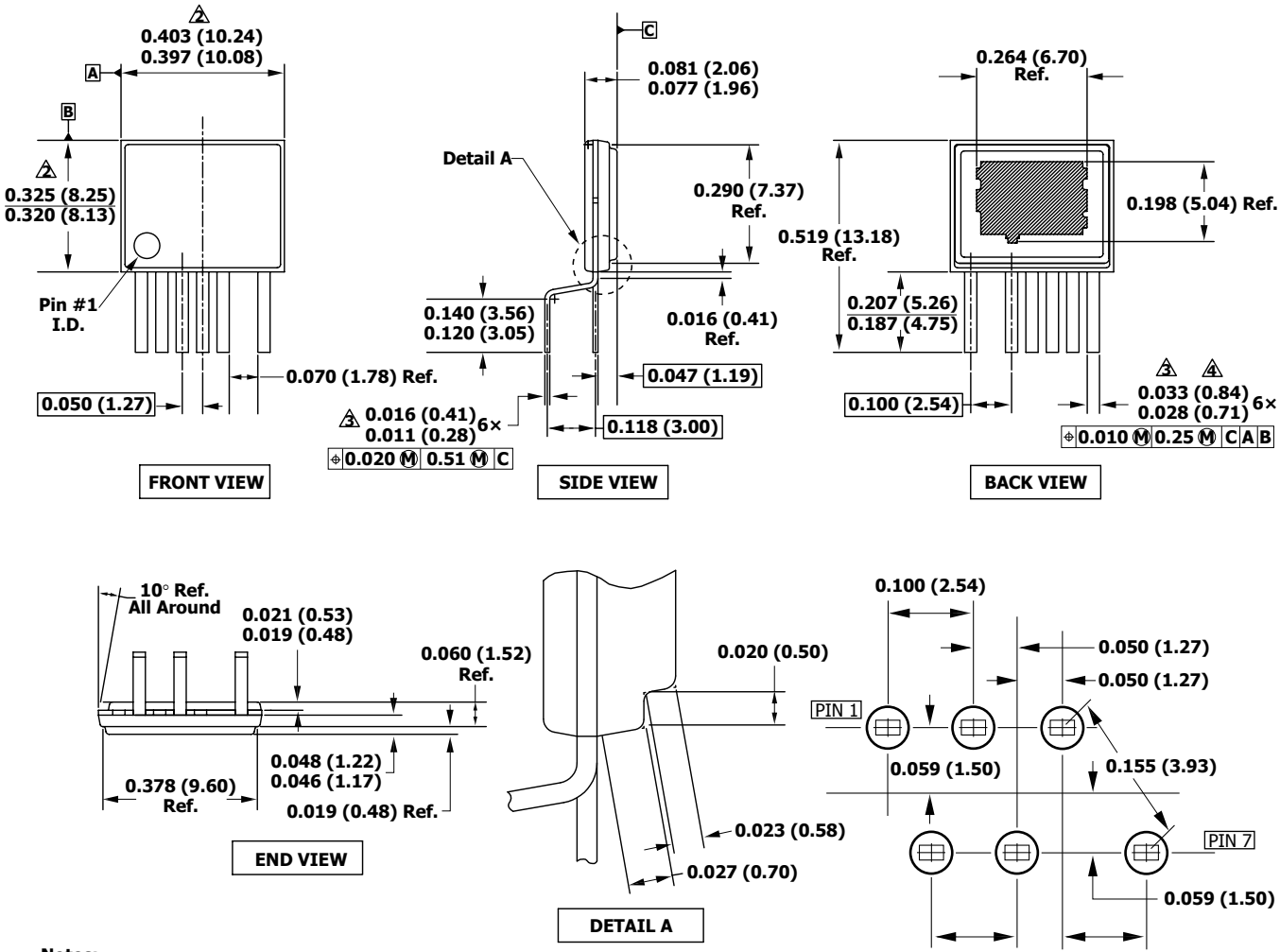


Figure 17. Maximum Allowable Drain Current vs. Drain Voltage.

eSIP-7C (E Package)

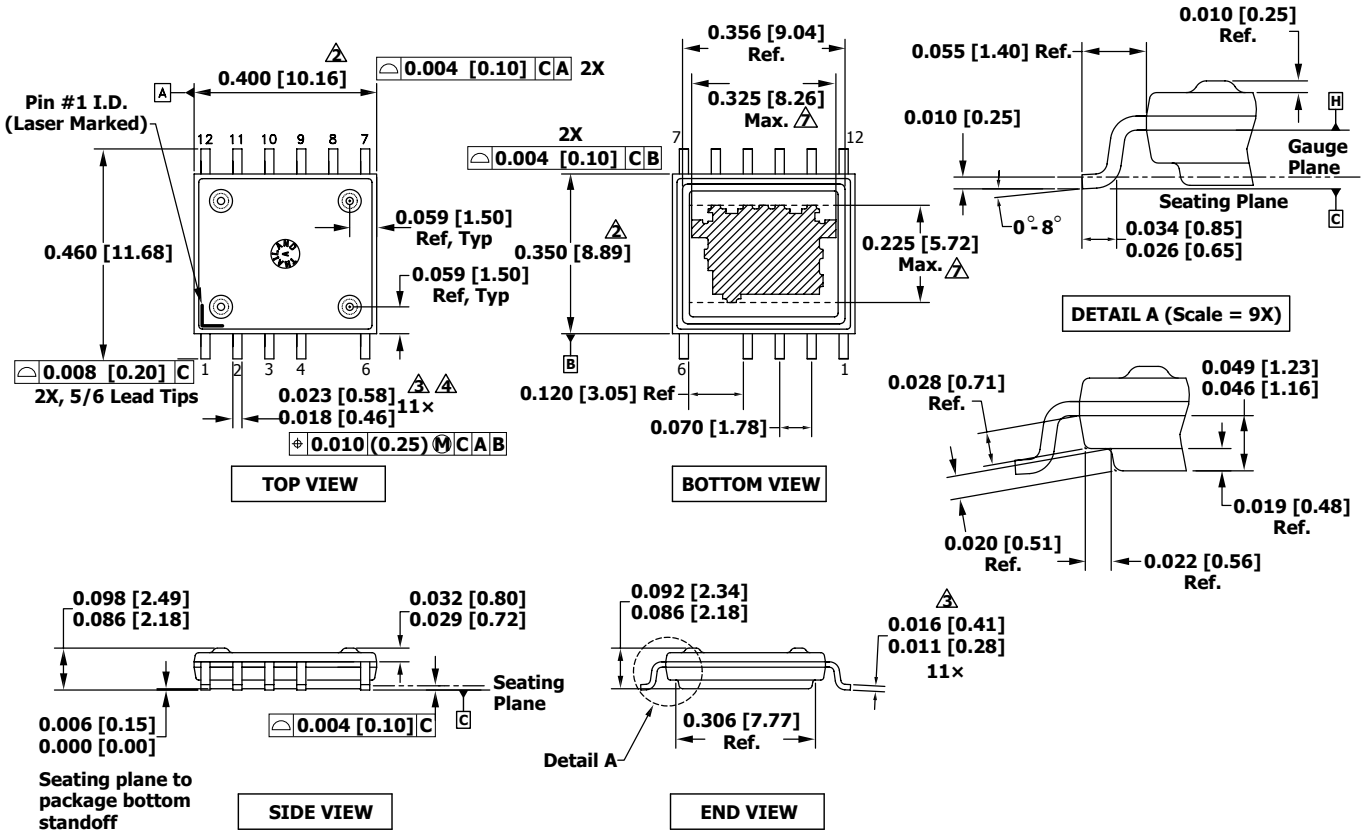


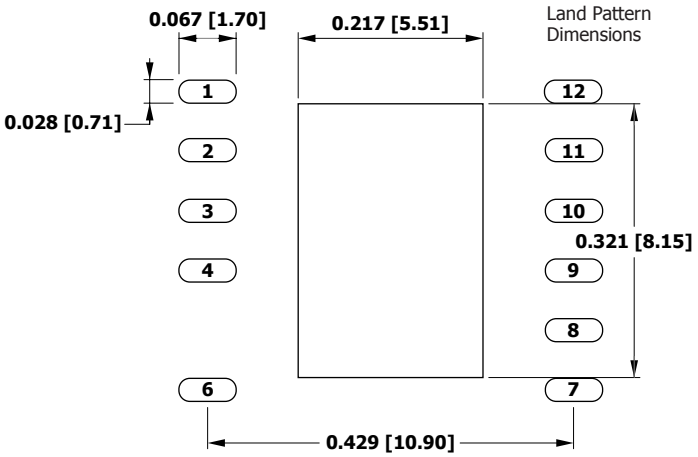
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-020515

eSOP-12B (K Package)



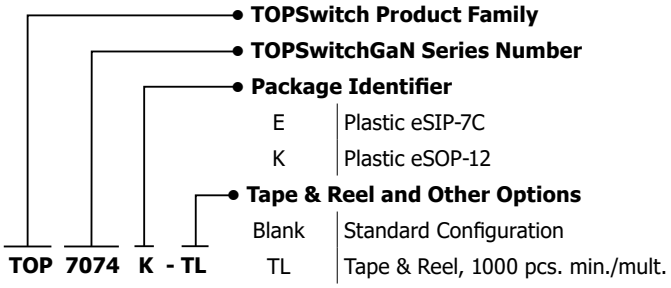


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5748a-020515

Part Ordering Information



Revision	Notes	Date
A	(PROVISIONAL) Production release.	03/26

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

https://www.power.com/company/sales/sales-offices