
Reference Design Report

Title	12 W, Wide Range 3-Phase Input, Isolated Flyback Power Supply with Anti-Magnetizing Interference Using INN3624C-H606 – An InnoSwitch3-EP IC with a 1250 V PowiGaN Switch
Specification	57 VAC – 580 VAC, 3 Φ , 4-Wire Input; 12 V / 1 A Output
Application	Metering, Industrial Applications
Product family	InnoSwitch3-EP
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Summary and Features

- Wide-range 3-phase, 4-wire input from 57 VAC to 580 VAC line-to-line
- Off-line CV/CC QR flyback integrated switcher IC with 1250 V PowiGaN™ switch
- Built in synchronous rectification for high efficiency at nominal AC input
 - Full-load efficiency of >90.3% at 200 VAC, and >87.8% at 400 VAC
 - Average efficiency of >89.3% at 200 VAC, and >85.1% at 400 VAC
- < 70 mW no-load input power across input voltage range
- FluxLink™ barrier crossing technology means that no optocoupler is required
 - Increases reliability and reduces part-count
- All the benefits of secondary side control with the simplicity of primary side regulation
 - Insensitive to transformer variation and extremely fast transient response
- Meets EN550022 and CISPR-22 Class B conducted EMI with ≥ 6 dB margin
- Resistance to external magnetizing interference
 - Can withstand up to 57% reduction in primary inductance on full input range
- Low component count: 71 components

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1 Introduction

This engineering report describes a 12 V / 1 A power supply using the InnoSwitch™3-EP (INN3624C-H606) IC with an integrated 1250 V PowiGaN switch, designed to withstand external magnetizing interference for metering applications. This design demonstrates the efficiency and reduced component count that can be achieved due to the high level of integration of the InnoSwitch-3 IC. Excellent efficiency across load and line is provided by the control algorithm, synchronous rectification, and the use of a PowiGaN switch.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

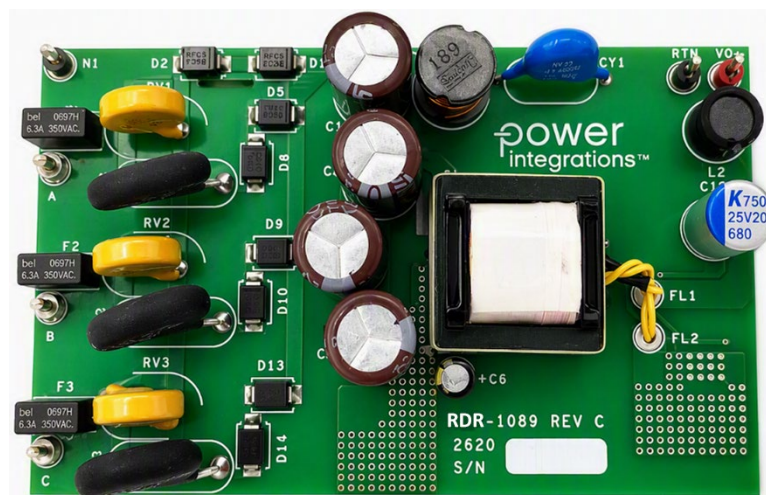


Figure 1 – Populated Circuit Board, Top View

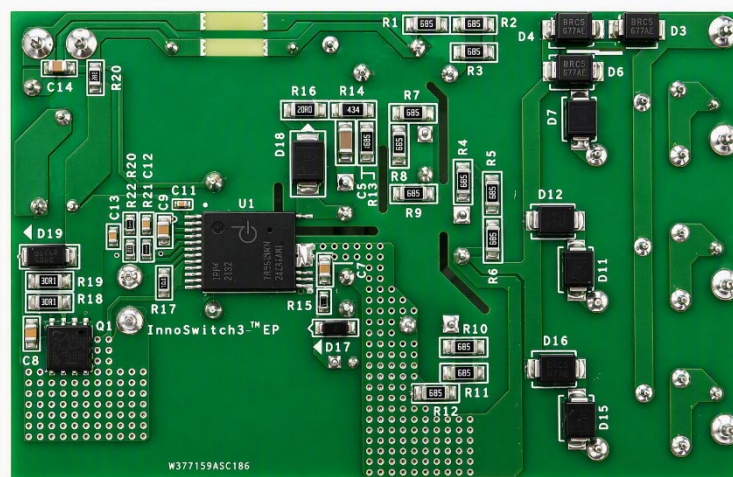


Figure 2 – Populated Circuit Board, Bottom View

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min.	Typical	Max.	Units	Comment
Input						
Voltage	V_{IN}	57	200/400	580	VAC	3-Phase/4-Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				<75	mW	V_{IN} : 57 VAC – 580 VAC
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	±5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth, at 25 °C
Output Current	I_{OUT}		1		A	Ambient
Total Output Power						
Continuous Output Power	P_{OUT}		12		W	
Efficiency	η		86 89 90 90 88 83			Full-load @ 57 VAC Full-load @ 90 VAC Full-load @ 200 VAC Full-load @ 230 VAC Full-load @ 400 VAC Full-load @ 580 VAC
Environmental		Meets CISPR22B/EN55022B				
Conducted EMI				6	kV	1.2/50 μ s Surge, IEC 61000-4-5,
Surge (Differential)						Impedance: 2 Ω Class A
EFT				4	kV	IEC-61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level

Table 1 – Power Supply Specifications



3 Schematic

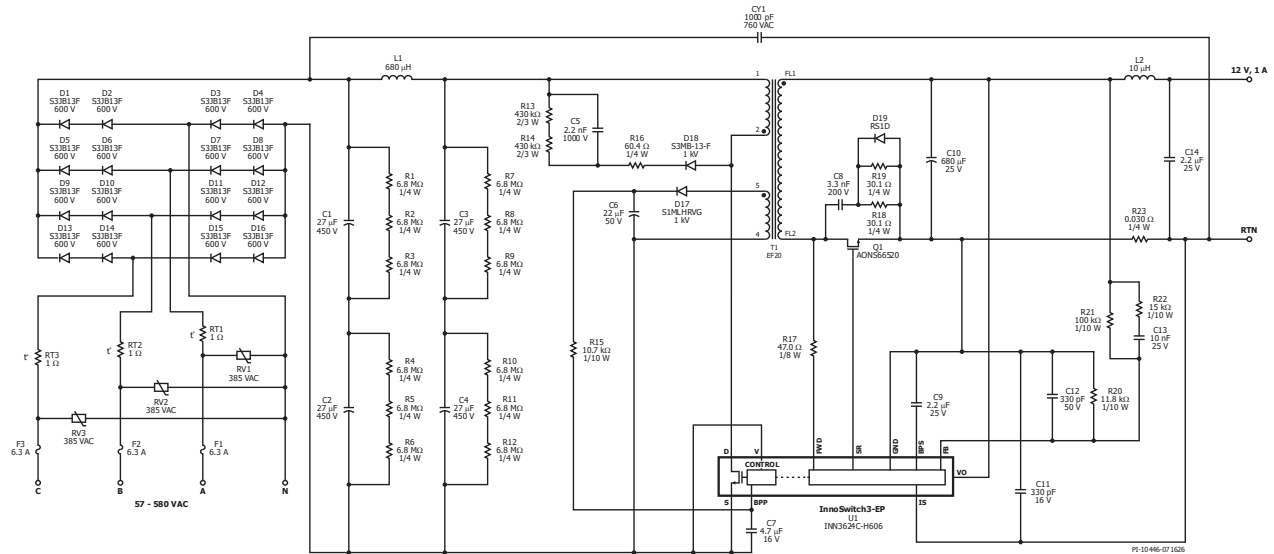


Figure 3 – Power Supply Schematic

4 Circuit Description

The InnoSwitch-3 combines primary, secondary, isolation, and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates a 1250 V PowiGaN primary switch, primary-side controller, secondary-side controller for synchronous rectification, and FluxLink™ technology which eliminates the optocoupler typically required for secondary-side control. The InnoSwitch-3 also employs quasi-resonant switching to achieve high efficiency.

4.1 EMI Filtering and AC Rectifier Stage

Fuses F1, F2, and F3 isolate the circuit and provide protection in the event of a component failure. Thermistors RT1, RT2, and RT3 reduce inrush current. Varistors RV1, RV2, and RV3 clamp any input voltage spike generated by abnormal surge events. Bridge rectifier diodes D1 to D16 rectify the 3-phase AC line voltage and provide a full-wave rectified DC across the input filter capacitors C1, C2, C3, and C4. Inductor L1 connected between the input filter capacitors C1, C2 and C3, C4 forms a π -filter – attenuating both common mode and differential mode noise. Capacitor CY1 reduces common mode electromagnetic interference (EMI). Resistors R1 to R12 balance the voltage across the input filter capacitors.

4.2 InnoSwitch3-EP IC Primary

The primary winding of the flyback transformer T1 starts on pin 2 and ends on pin 1. Pin 1 of transformer T1 is connected to the rectified DC bus while pin 2 of T1 is connected to the drain terminal of the power switch – located inside the InnoSwitch3-EP IC U1 through the DRAIN pin. The V pin of the IC U1 is tied to the SOURCE pin to disable the UV/OV protection feature.

The InnoSwitch3-EP IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C7 when AC input voltage is first applied. During normal operation, the primary-side block of the IC is powered from an auxiliary or bias winding on transformer T1. The output of the bias winding is rectified by diode D17 and filtered by capacitor C6. Resistor R15 limits the current supplied by capacitor C6 to the BPP pin of the InnoSwitch3-EP IC U1.

4.3 The InnoSwitch3-EP IC also controls the Output Stage

The secondary side of the InnoSwitch3-EP IC U1 provides output voltage and output current sensing and controls the operation of the Synchronous Rectification Field-Effect Transistor (SR FET).

The output from the secondary winding of the transformer T1 is rectified by the SR FET Q1 and filtered by the output capacitor C10. The inductor L2 along with capacitor C14 form a second-stage filter that significantly attenuates the high-frequency ripple and noise on the output voltage.



The capacitor C8, resistors R18 and R19, and diode D19 form an RCD snubber network that damps the high-frequency ringing across the SR FET Q1. The ringing comes from the resonance of the transformer leakage inductance and secondary trace inductances with parasitic circuit capacitances – which would have otherwise created radiated EMI if not damped properly.

The gate pin of Q1 is controlled by the secondary-side controller inside the IC U1, based on the secondary winding voltage sensed via resistor R17 into the FWD pin of the IC.

In continuous conduction mode (CCM) operation, the SR FET is turned off just prior to the secondary-side controller requesting a new switching cycle from the primary. During discontinuous conduction mode (DCM) operation, the SR FET is turned off once the voltage drop across the SR FET falls below a threshold voltage $V_{SR(TH)}$. Secondary-side control of the primary switching cycle ensures that the primary power switch is never simultaneously on with the secondary SR FET. The SR FET Q1 drive signal is provided by the SR pin of the IC U1.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (via the FWD pin) or the output voltage. Capacitor C9 connected to the BPS pin of the IC U1 provides energy storage and decoupling for the internal circuitry.

Output current is sensed between the IS pin and GND pin by monitoring the voltage drop across the resistor R23. The voltage drop is limited to approximately 36 mV to reduce losses. Capacitor C11 provides filtering for the IS pin of U1 to protect it from external noise.

The InnoSwitch3-EP IC operates in constant voltage mode before reaching the current limit. During normal operation, output voltage regulation is achieved through sensing the output voltage via a voltage divider made up of feedback resistors R21 and R20. The voltage across resistor R20 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated such that the output of the voltage divider feedback network matches the internal reference voltage. Capacitor C12 provides decoupling from high-frequency noise, while capacitor C13 and resistor R22 form a feed-forward circuit to speed up response time and reduce output voltage ripple.

5 PCB Layout

PCB copper thickness is 2.0 oz.

PCB Material Thickness is 1.6 mm.

PCB Material is FR4.

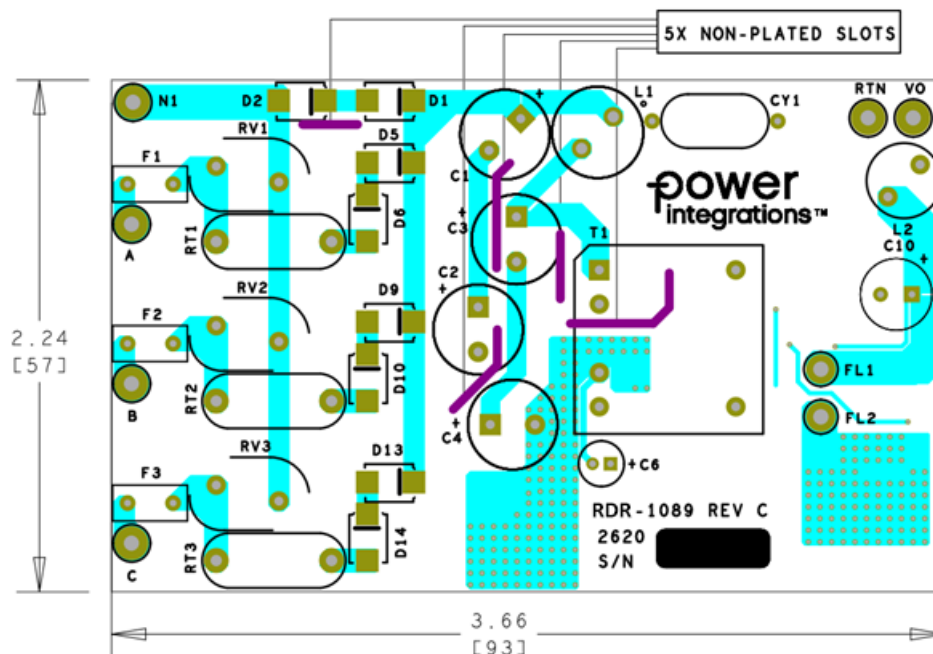


Figure 4 – Printed Circuit Board, Top

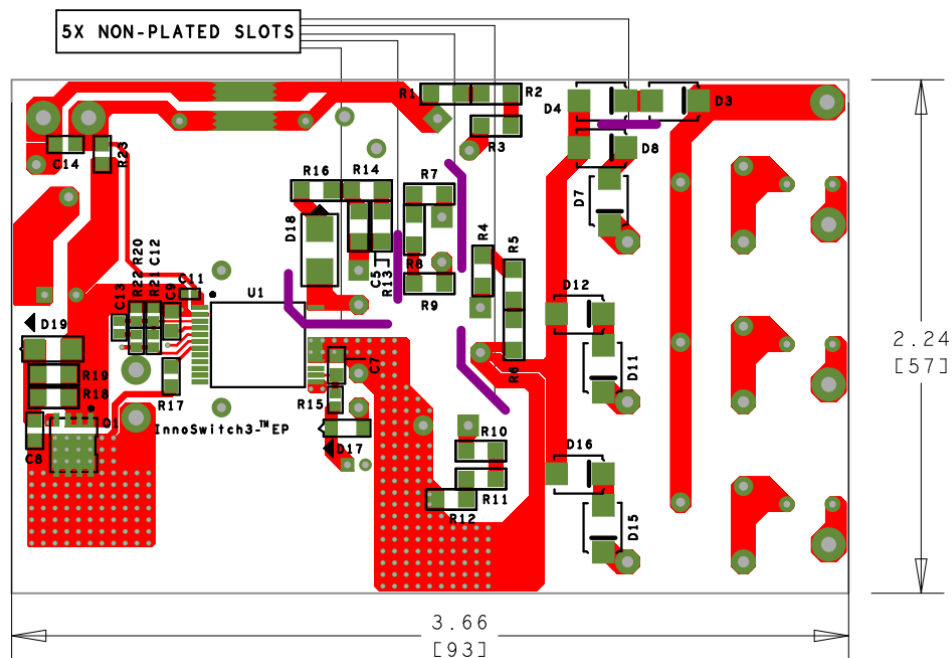


Figure 5 – Printed Circuit Board, Bottom



6 Performance Data

1. All performance data were measured on the board unless otherwise noted.
2. List of Equipment Used for Testing.

Equipment Type	Model Number	Specifications	Manufacturer
Three-Phase Power Supply	IT7800 3U	15 kVA/350 V L-N AC/DC 3-phase PSU	ITECH
Three-Phase Power Meter	66203	600 V/20 A Digital Power Meter	Chroma
Output Power Meter	WT310E	600 V/40 A Digital Power Meter	Yokogawa
Electronic Load	63113A	300 V/20 A/300 W DC Electronic Load	Chroma
Oscilloscope	RTO64	6 GHz/20 GS/s Multi-Channel	Rohde & Schwarz
Thermal Chamber	T2	-68 °C to 180 °C Temp/Humidity	Tenney
Thermocouple Measurement	GL840	20-Channel Data Logger	Graphtec
Passive Voltage Probe	4910-2RA	100x 200 MHz Passive Voltage Probe	Probe Master
Passive Voltage Probe	4905-1	10x 250 MHz Passive Voltage Probe	Probe Master
Differential Voltage Probe	PT-8001	10x/70 V, 100x/700 V Differential Probe	PINTECH
Current Probe	RT-ZC20B	0.1 V/A, 100 MHz/ 30 A Current Probe	Rohde & Schwarz

Table 2 – List of Equipment Used for Testing

6.1 Full Load Efficiency vs. Line

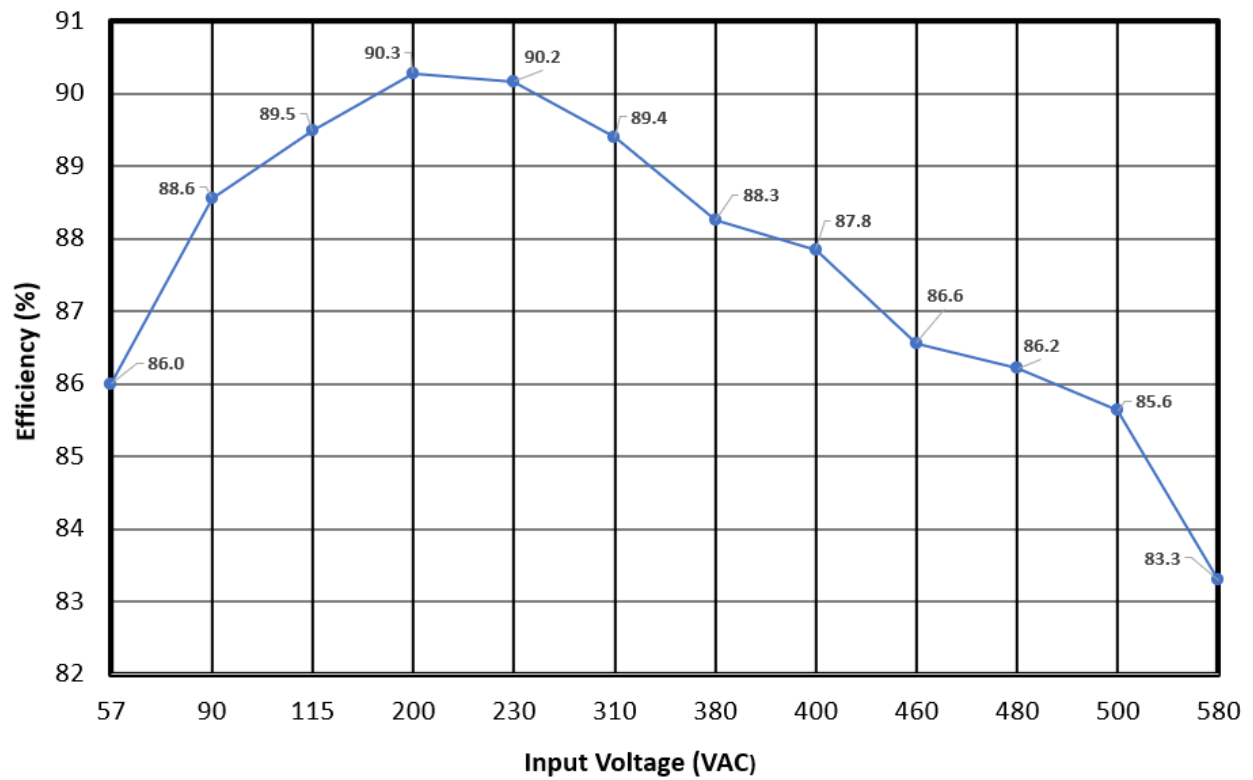


Figure 6 – Full-load Efficiency vs. Line, Room Temperature

6.2 Efficiency vs. Load

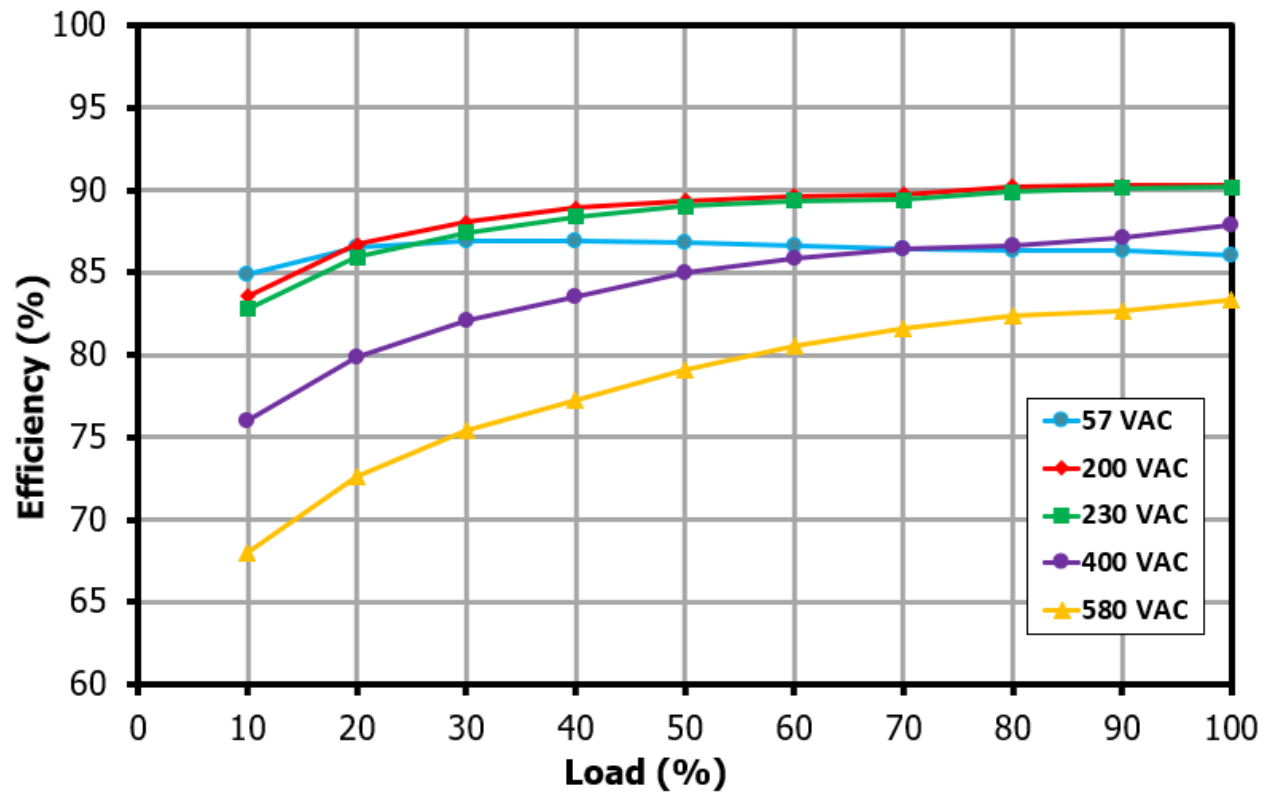


Figure 7 – Efficiency vs. Load, Room Temperature

6.3 Average Efficiency

6.3.1 Average and 10% Efficiency at 57 VAC Input

% Load	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	13.7	11.8	86.0	86.5
75	10.3	8.9	86.4	
50	6.87	5.97	86.9	
25	3.45	2.99	86.8	
10	1.41	1.20	84.9	

Table 3 – Average and 10% Efficiency at 57 VAC

6.3.2 Average and 10% Efficiency at 200 VAC Input

% Load	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	13.3	12.0	90.3	89.3
75	10.0	8.99	90.0	
50	6.71	5.99	89.4	
25	3.43	3.00	87.5	
10	1.44	1.20	83.6	

Table 4 – Average and 10% Efficiency at 200 VAC



6.3.3 Average and 10% Efficiency at 230 VAC Input

% Load	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	13.3	12.0	90.2	88.9
75	10.1	9.00	89.5	
50	6.74	5.99	89.0	
25	3.46	3.00	86.8	
10	1.45	1.20	82.8	

Table 5 – Average and 10% Efficiency at 230 VAC

6.3.4 Average and 10% Efficiency at 400 VAC Input

% Load	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	13.7	12.0	87.8	85.1
75	10.4	9.01	86.6	
50	7.06	6.00	84.9	
25	3.70	3.00	81.1	
10	1.58	1.20	76.0	

Table 6 – Average and 10% Efficiency at 400 VAC

6.3.5 Average and 10% Efficiency at 580 VAC Input

% Load	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	14.4	12.0	83.3	79.6
75	11.0	9.01	81.9	
50	7.60	6.01	79.1	
25	4.05	3.01	74.2	
10	1.77	1.20	67.9	

Table 7 – Average and 10% Efficiency at 580 VAC

6.4 No-Load Input Power

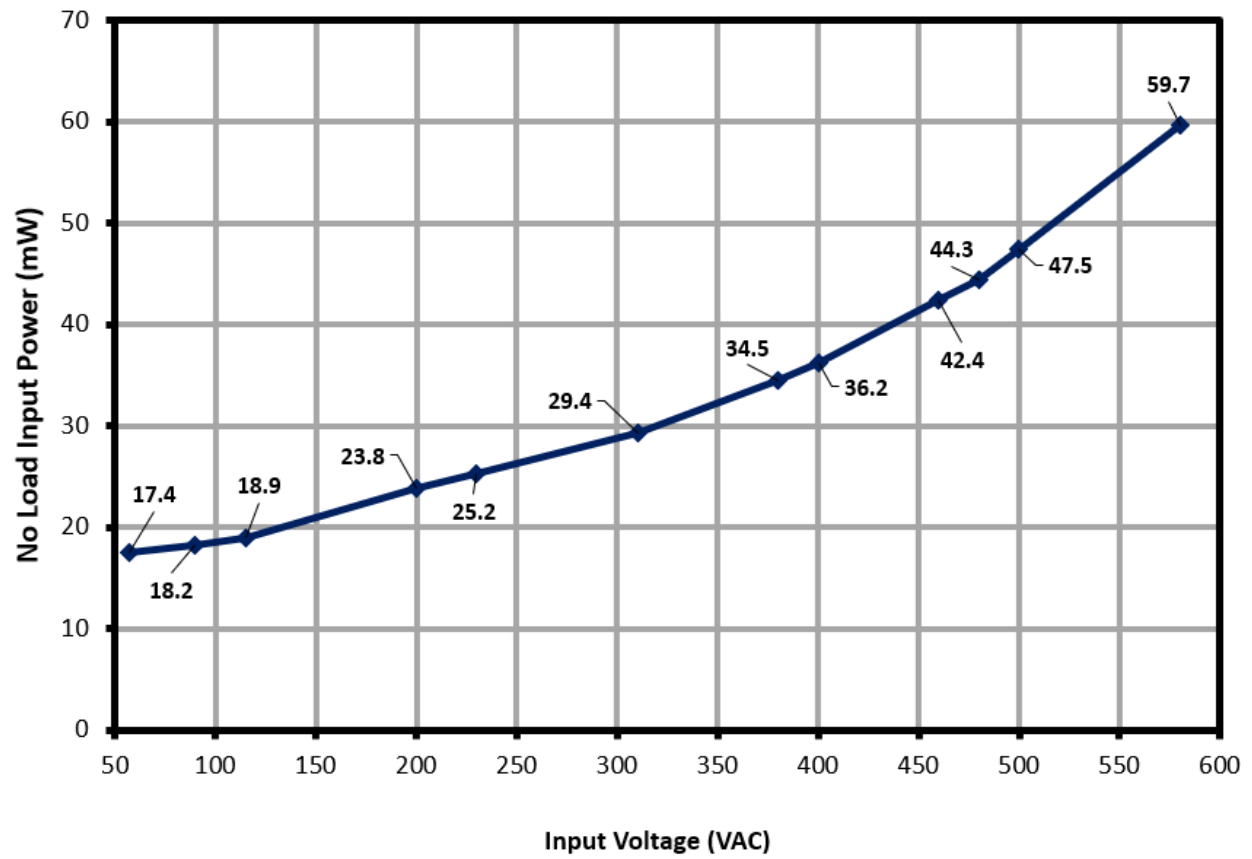


Figure 8 – No-Load Input Power vs. Input Line Voltage, Room Temperature

6.5 Line Regulation (Full Load)

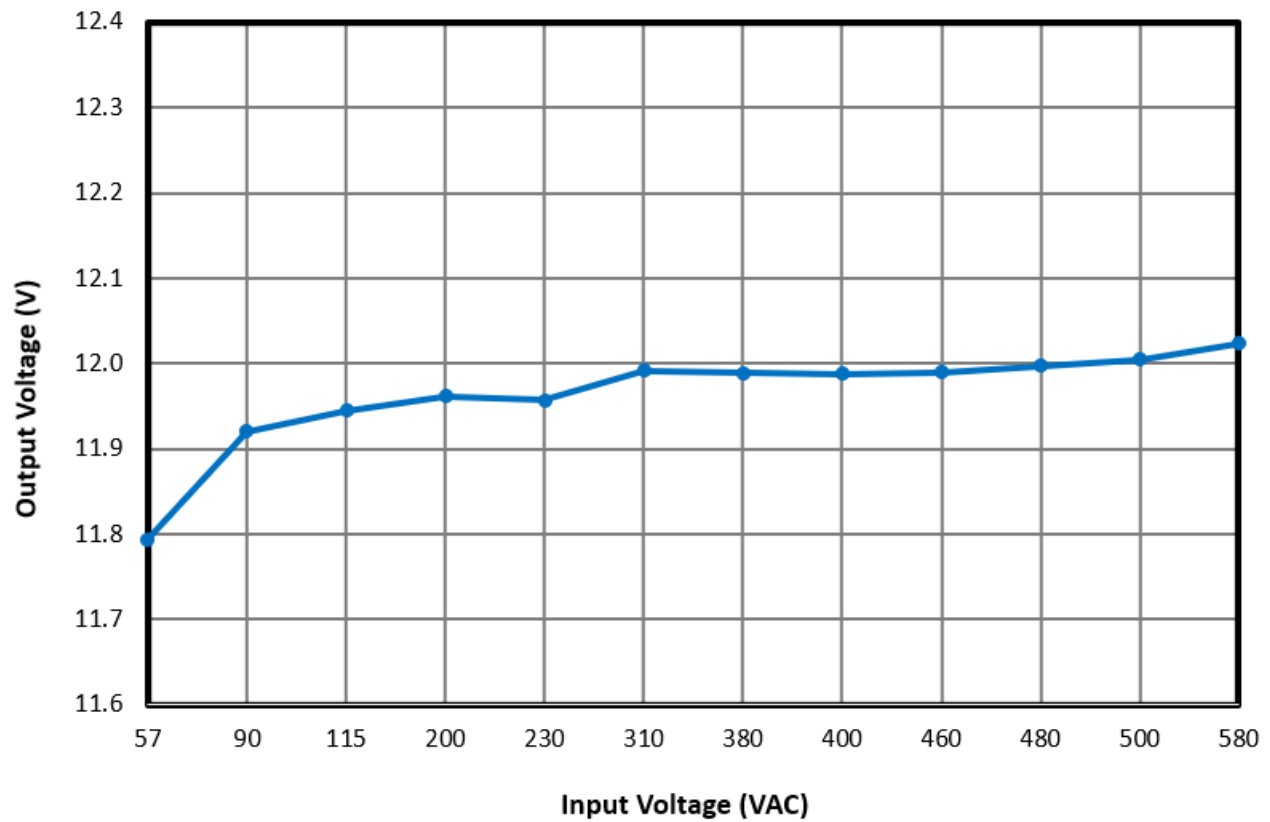


Figure 9 – Line Regulation – Full Load

6.6 Load Regulation

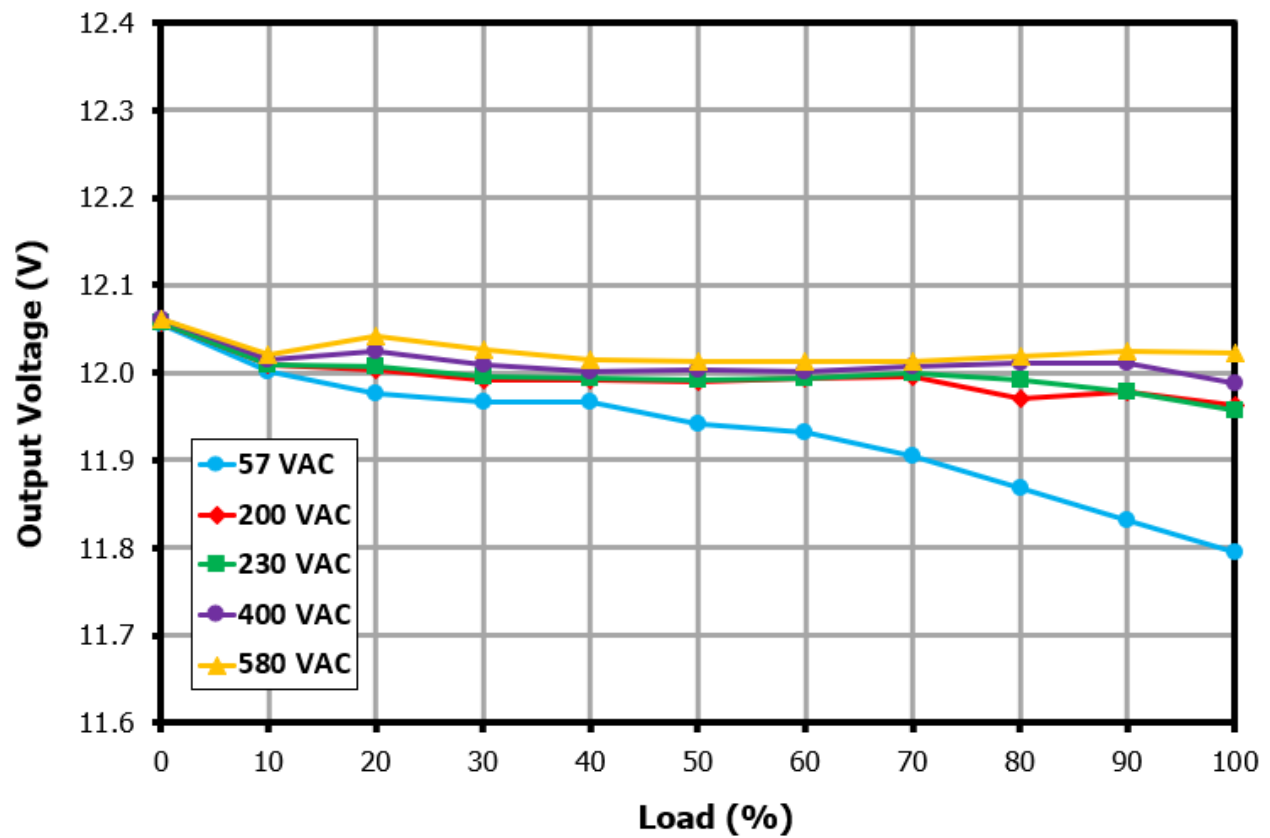


Figure 10 – Load Regulation

7 Thermal Performance

The temperature of key components was measured with the power supply positioned inside a thermal chamber at ambient temperatures of 0 °C, 25 °C, and 40 °C. Temperatures were recorded over time using a data logger. The test continued until thermal equilibrium was achieved.

7.1 57 VAC, 12 W at 0 °C Ambient

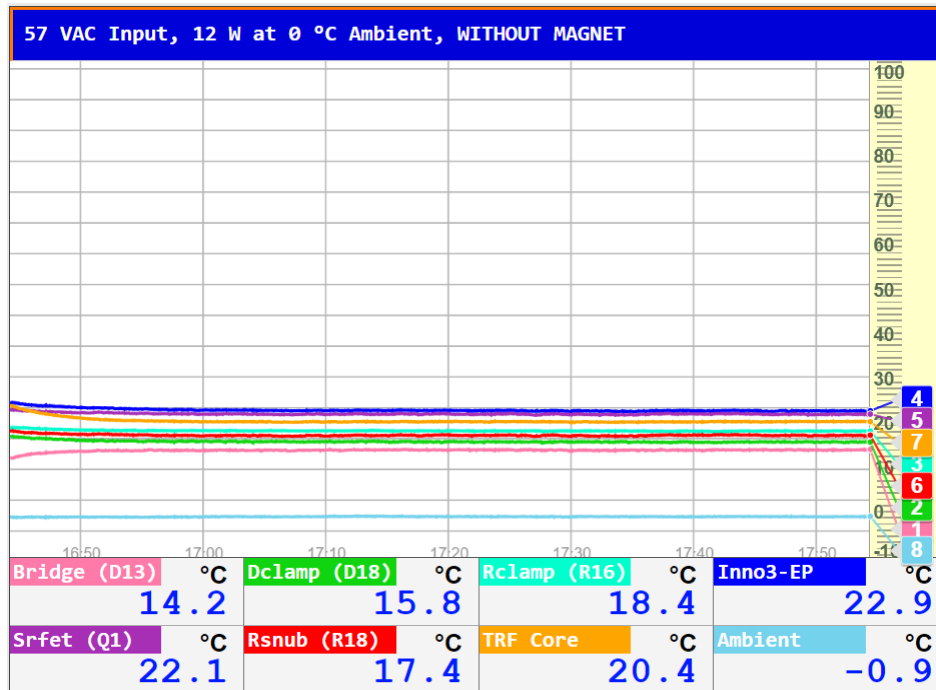


Figure 11 – Thermal Performance at 57 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	14.2
Primary Clamp Diode (D18)	15.8
Primary Clamp Series Resistor (R16)	18.4
InnoSwitch3-EP (U1)	22.9
SR FET (Q1)	22.1
Secondary Rectifier Snubber Resistor (R18)	17.4
Transformer Core (T1)	20.4
Ambient	-0.9

Table 8 – Temperature Measurement of Critical Components at 0 °C

7.2 580 VAC, 12 W at 0 °C Ambient

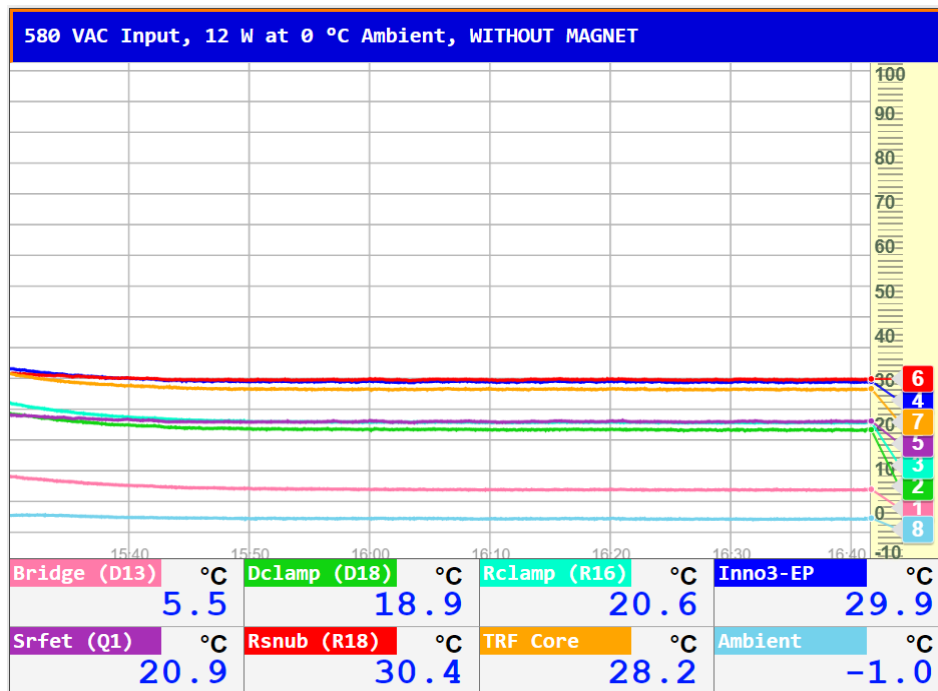


Figure 12 – Thermal Performance at 580 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	5.5
Primary Clamp Diode (D18)	18.9
Primary Clamp Series Resistor (R16)	20.6
InnoSwitch3-EP (U1)	29.9
SR FET (Q1)	20.9
Secondary Rectifier Snubber Resistor (R18)	30.4
Transformer Core (T1)	28.2
Ambient	-1.0

Table 9 – Temperature Measurement of Critical Components at 0 °C

7.3 57 VAC, 12 W at 25 °C Ambient

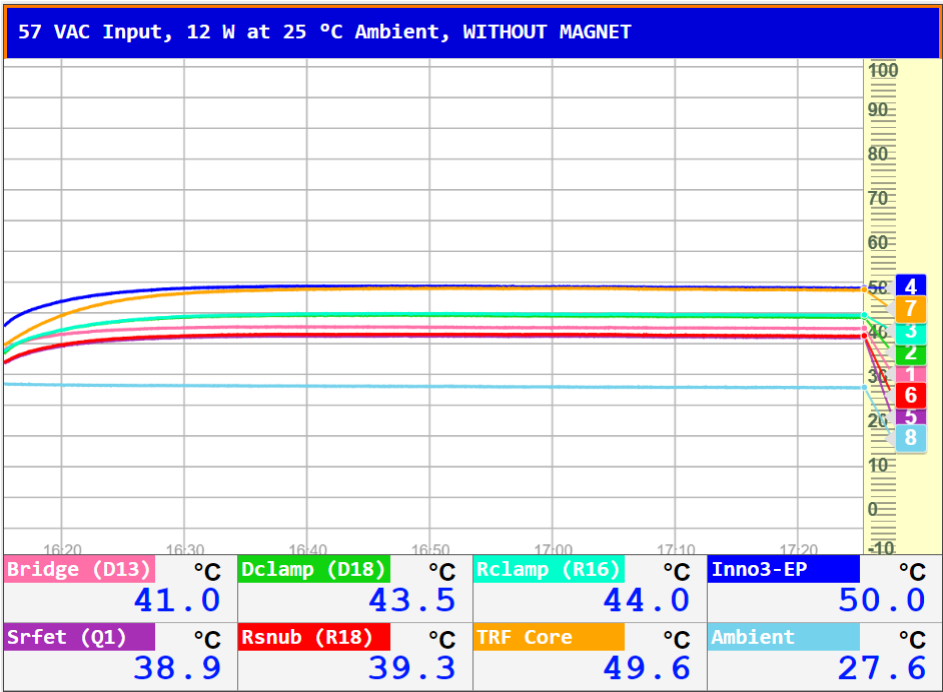


Figure 13 – Thermal Performance at 57 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	41.0
Primary Clamp Diode (D18)	43.5
Primary Clamp Series Resistor (R16)	44.0
InnoSwitch3-EP (U1)	50.0
SR FET (Q1)	38.9
Secondary Rectifier Snubber Resistor (R18)	39.3
Transformer Core (T1)	49.6
Ambient	27.6

Table 10 – Temperature Measurement of Critical Components at 25 °C

7.4 580 VAC Input, 12 W at 25 °C Ambient

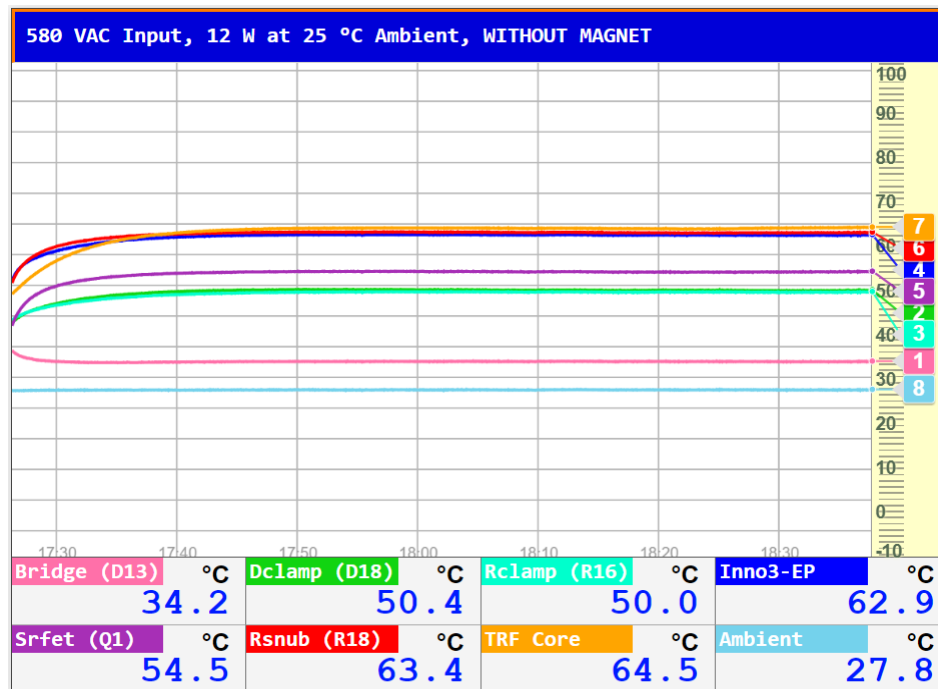


Figure 14 – Thermal Performance at 580 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	34.2
Primary Clamp Diode (D18)	50.4
Primary Clamp Series Resistor (R16)	50.0
InnoSwitch3-EP (U1)	62.9
SR FET (Q1)	54.5
Secondary Rectifier Snubber Resistor (R18)	63.4
Transformer Core (T1)	64.5
Ambient	27.8

Table 11 – Temperature Measurement of Critical Components at 25 °C

7.5 57 VAC Input, 12 W at 40 °C Ambient

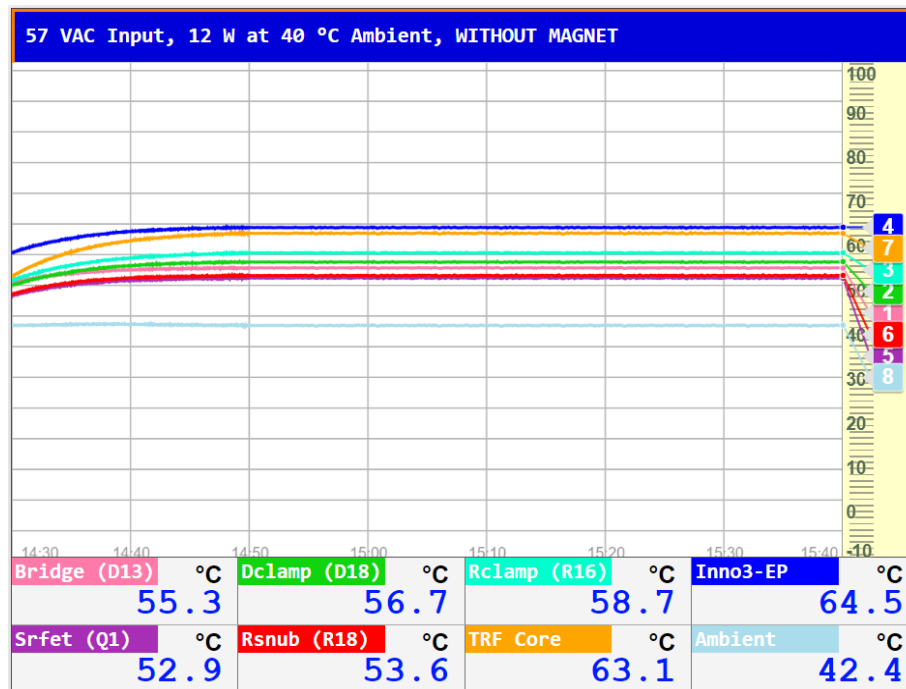


Figure 15 – Thermal Performance at 57 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	55.3
Primary Clamp Diode (D18)	56.7
Primary Clamp Series Resistor (R16)	58.7
InnoSwitch3-EP (U1)	64.5
SR FET (Q1)	52.9
Secondary Rectifier Snubber Resistor (R18)	53.6
Transformer Core (T1)	63.1
Ambient	42.4

Table 12 – Temperature Measurement of Critical Components at 40 °C

7.6 580 VAC Input, 12 W at 40 °C Ambient

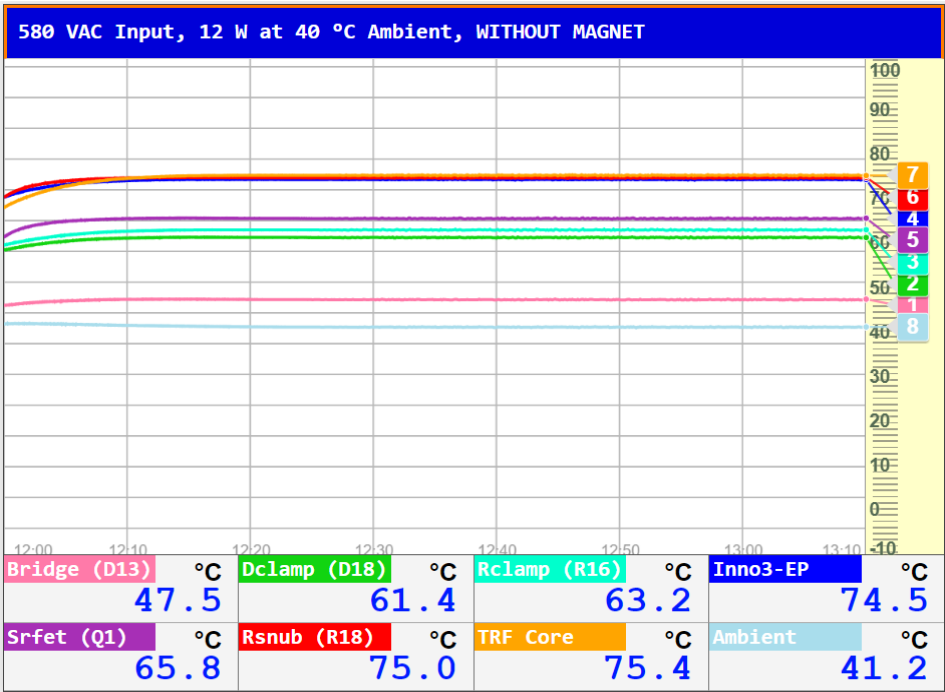


Figure 16 – Thermal Performance at 480 VAC Input

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	47.5
Primary Clamp Diode (D18)	61.4
Primary Clamp Series Resistor (R16)	63.2
InnoSwitch3-EP (U1)	74.5
SR FET (Q1)	65.8
Secondary Rectifier Snubber Resistor (R18)	75.0
Transformer Core (T1)	75.4
Ambient	41.2

Table 13 – Temperature Measurement of Critical Components at 40 °C

8 Waveforms

8.1 Output Voltage Start-up Waveforms at Room Temperature

The input voltage at CH1 is measured only across one L-N of the 3-phase, 4-wire input line.

8.1.1 CC Load

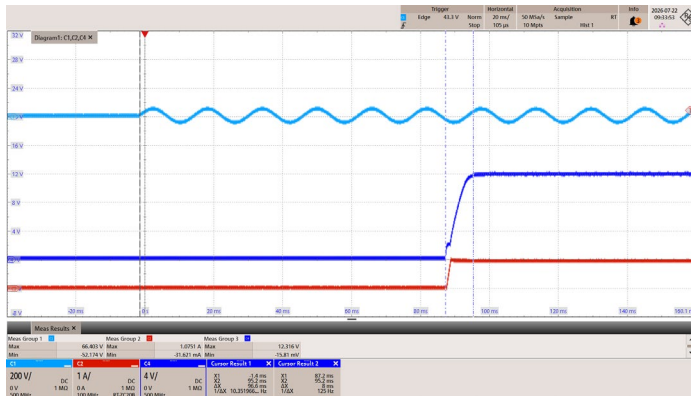


Figure 17 – 57 VAC, 60 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.3 V

Output Voltage, Rise Time = 8 ms

Start-up Time = 96.6 ms

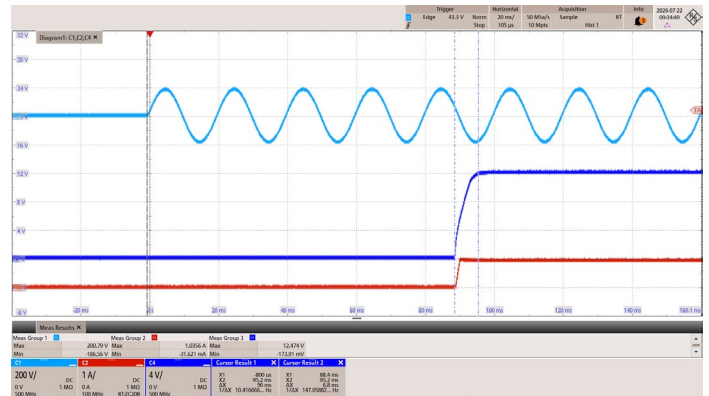


Figure 18 – 230 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 6.8 ms

Start-up Time = 96 ms

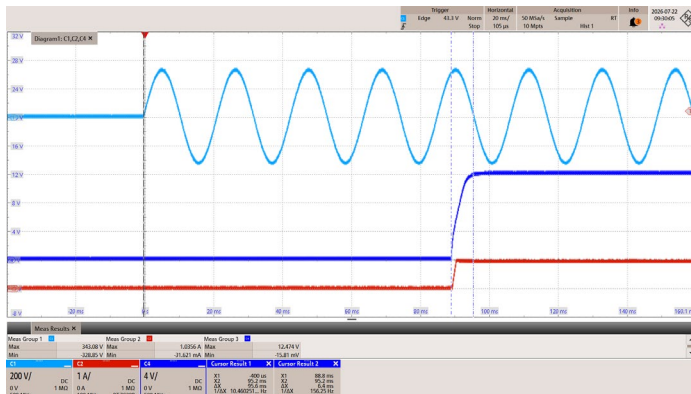


Figure 19 – 400 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 6.4 ms

Start-up Time = 95.6 ms

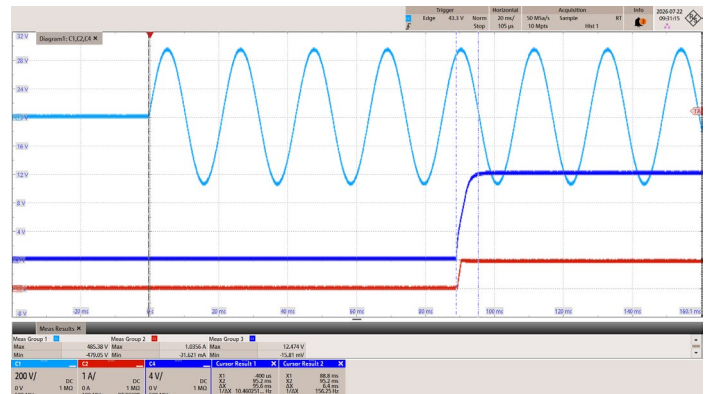


Figure 20 – 580 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 6.4 ms

Start-up Time = 95.6 ms

8.1.2 CR Load

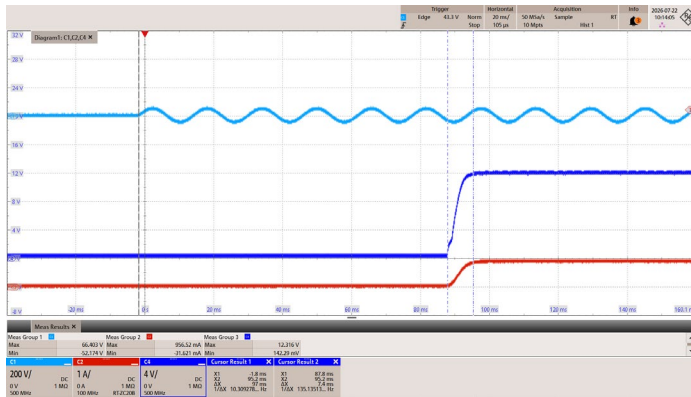


Figure 21 – 57 VAC, 60 Hz, $R_o = 12 \Omega$ (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.3 V

Output Voltage, Rise Time = 7.4 ms

Start-up Time = 97 ms

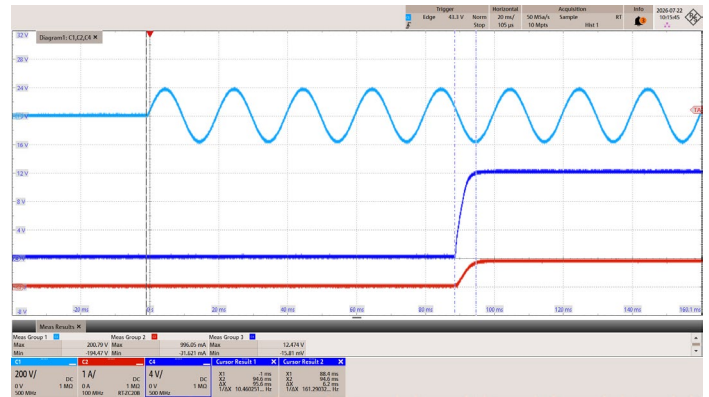


Figure 22 – 230 VAC, 50 Hz, $R_o = 12 \Omega$ (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 6.2 ms

Start-up Time = 95.6 ms

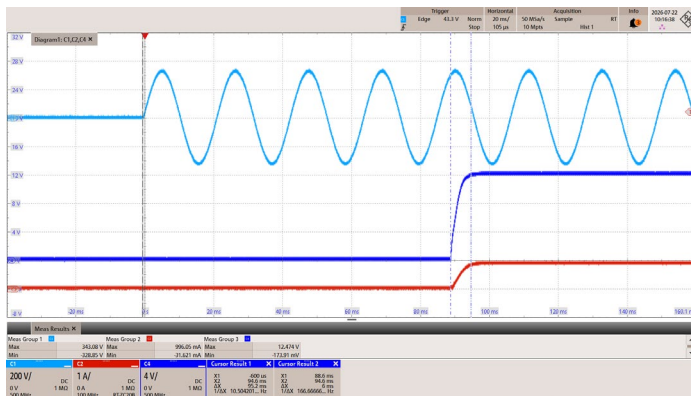


Figure 23 – 400 VAC, 50 Hz, $R_o = 12 \Omega$ (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 6 ms

Start-up Time = 95.2 ms

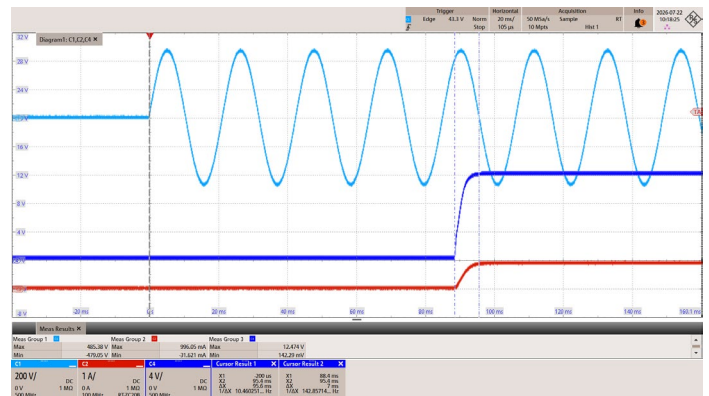


Figure 24 – 580 VAC, 50 Hz, $R_o = 12 \Omega$ (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 7 ms

Start-up Time = 95.6 ms

8.2 Load Transient Response

8.2.1 0 – 100% Load Step

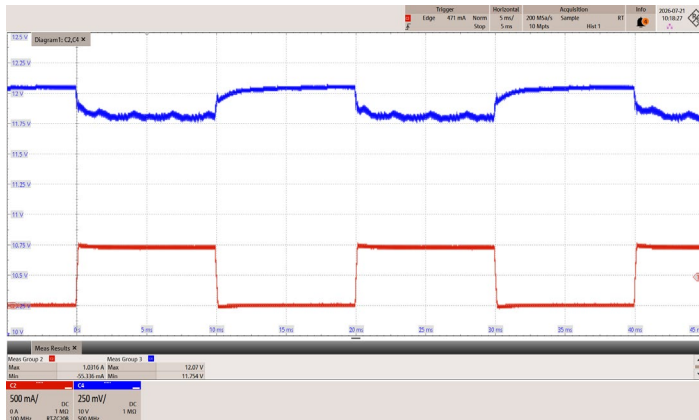


Figure 25 – 57 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.8 V

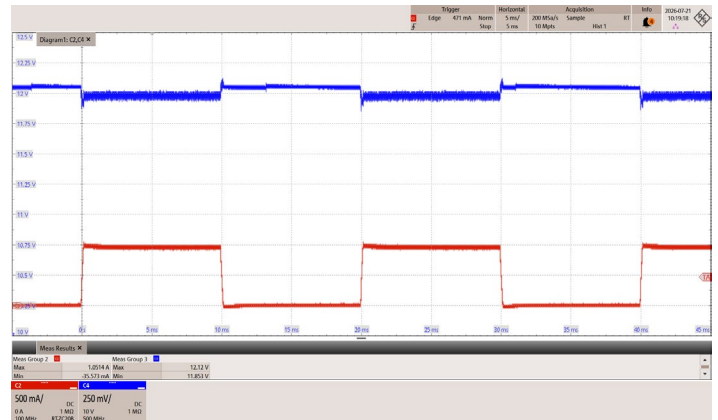


Figure 26 – 230 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

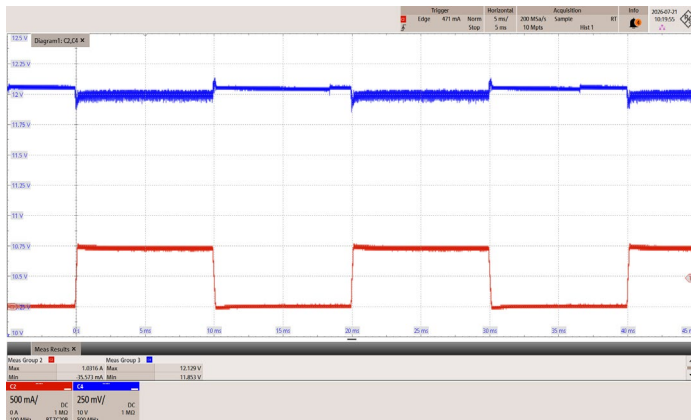


Figure 27 – 400 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

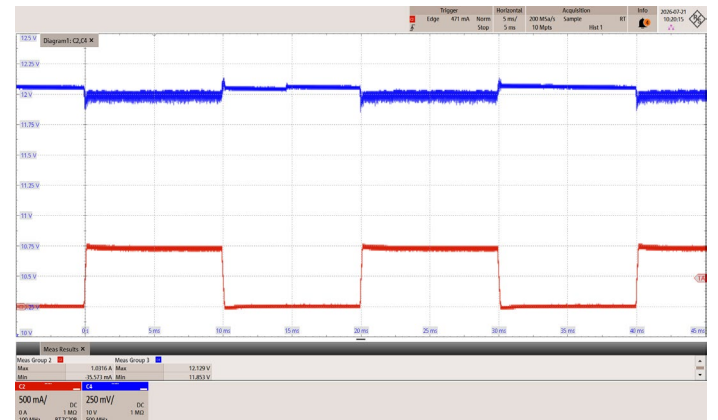


Figure 28 – 580 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

8.2.2 50% – 100% Load Step

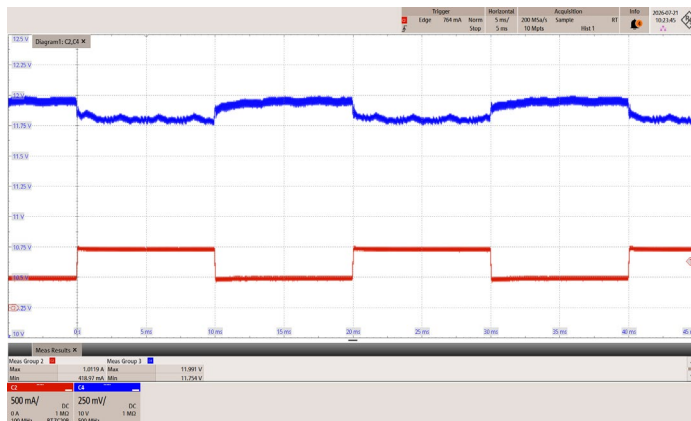


Figure 29 – 57 VAC; $I_O = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.0 V
 V_{MIN} : 11.8 V

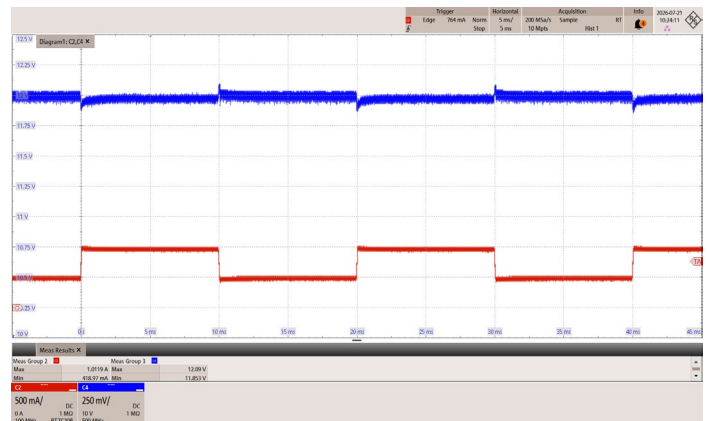


Figure 30 – 230 VAC; $I_O = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

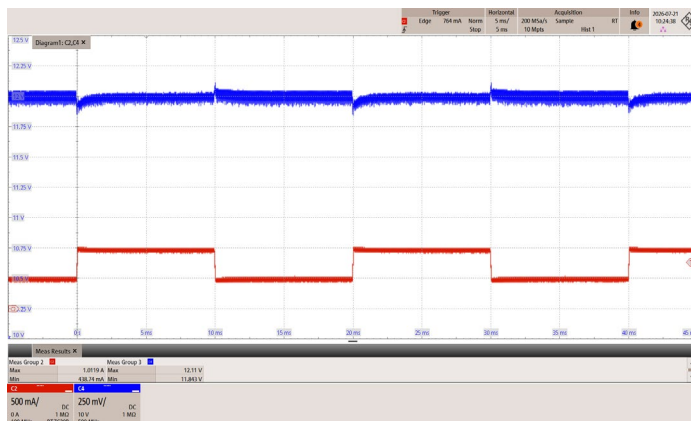


Figure 31 – 400 VAC; $I_O = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.8 V

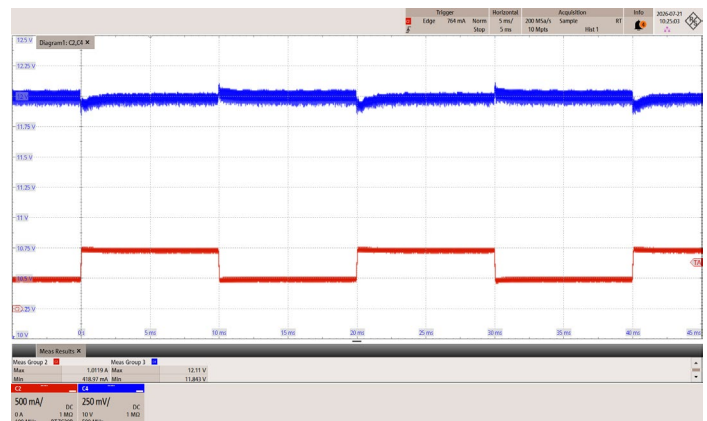


Figure 32 – 580 VAC; $I_O = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.8 V

8.3 InnoSwitch Switching Waveforms

8.3.1 Drain Voltage and Current at Start-up (100% Load)

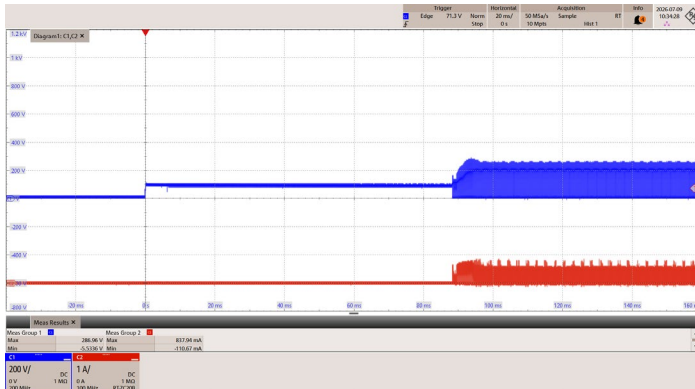


Figure 33 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 287 V

Drain current, Max. = 0.838 A

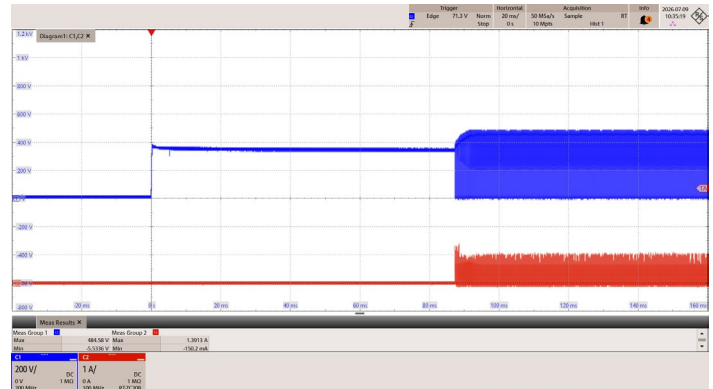


Figure 34 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 485 V

Drain current, Max. = 1.39 A

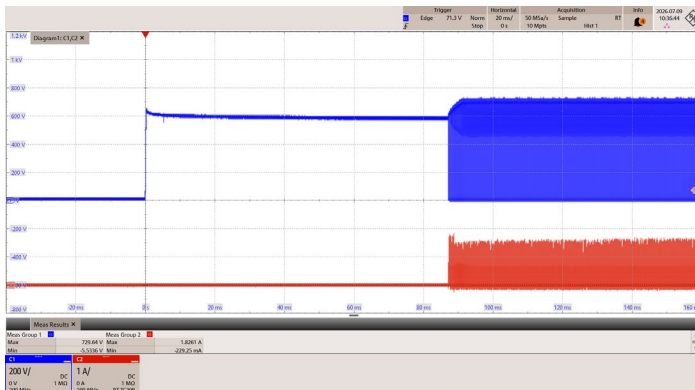


Figure 35 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 730 V

Drain current, Max. = 1.83 A

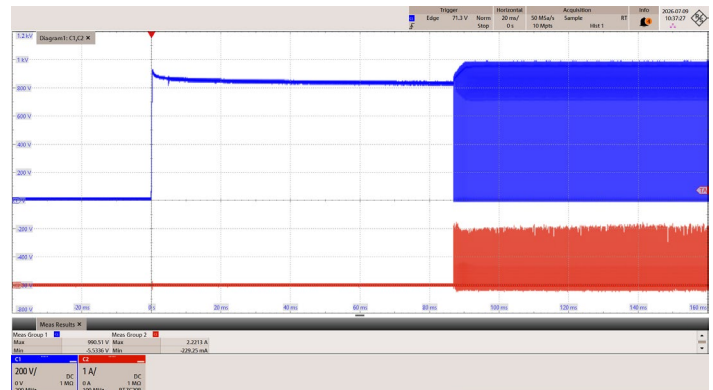


Figure 36 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 991 V

Drain current, Max. = 2.22 A

8.3.2 Drain Voltage and Current at Start-up (0% Load)

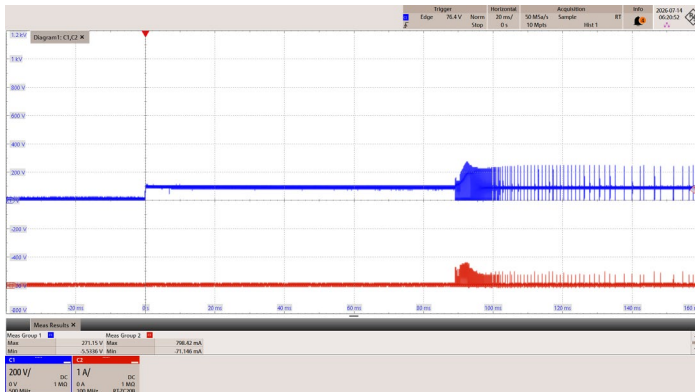


Figure 37 – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 271 V

Drain current, Max. = 0.798 A

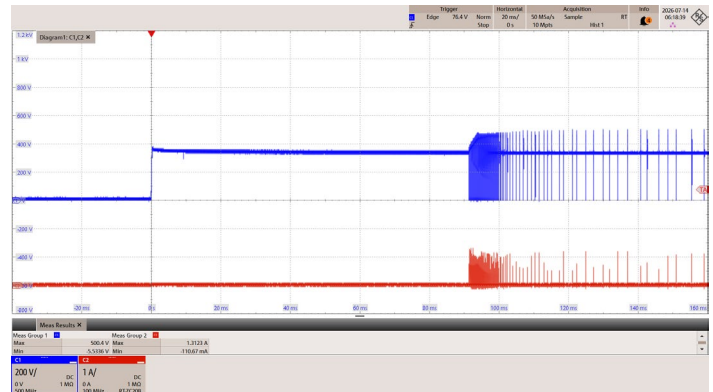


Figure 38 – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 500 V

Drain current, Max. = 1.31 A

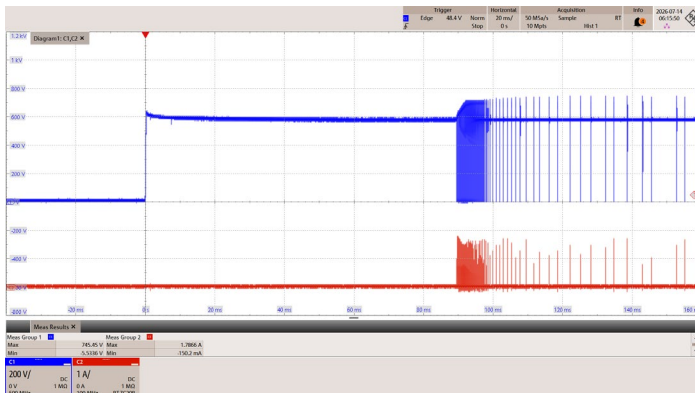


Figure 39 – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 746 V

Drain current, Max. = 1.79 A

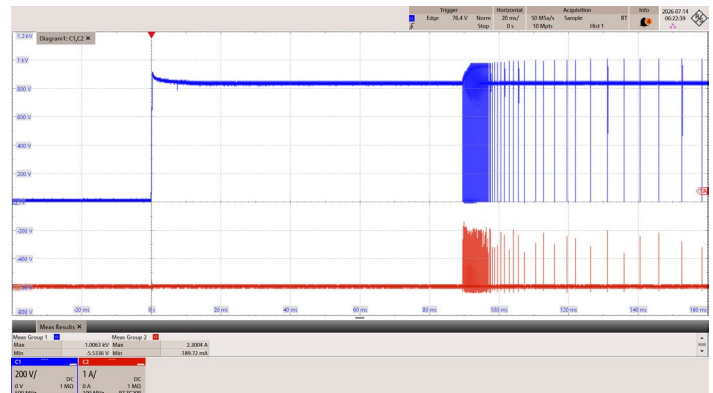


Figure 40 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 1006 V

Drain current, Max. = 2.30 A

8.3.3 Drain Voltage and Current at Normal Operation (100% Load)

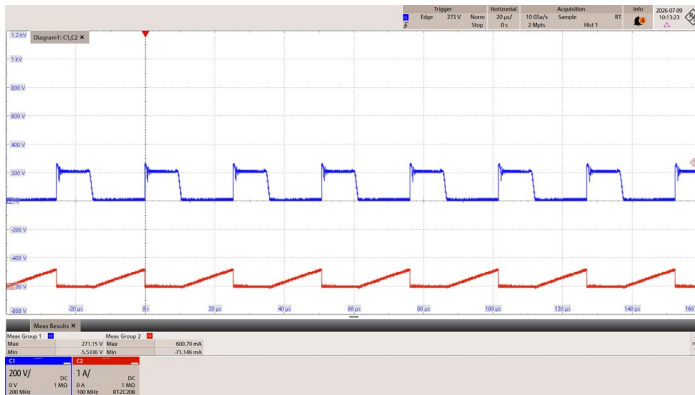


Figure 41 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 271 V

Drain current, Max. = 0.601 A

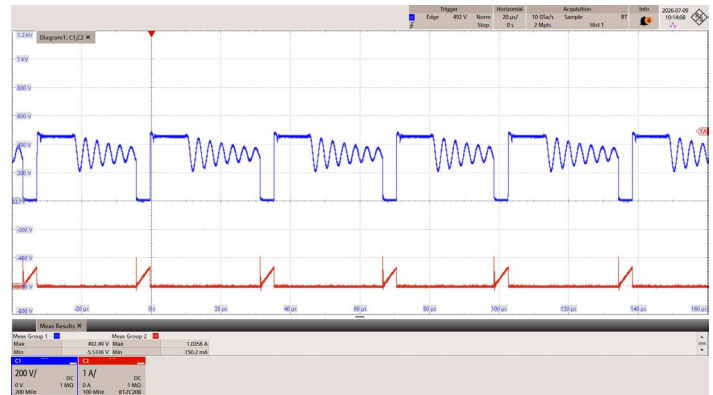


Figure 42 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 493 V

Drain current, Max. = 1.04 A

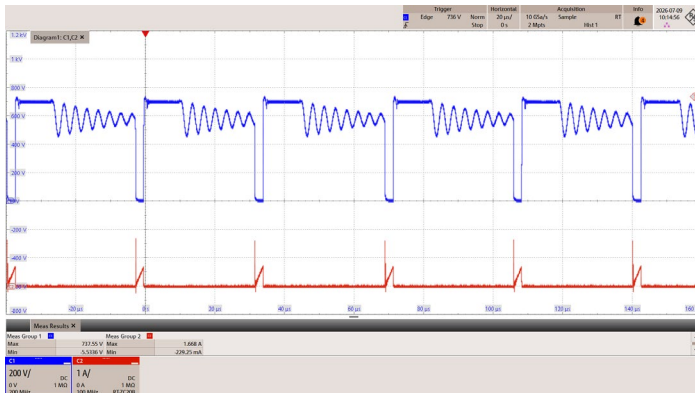


Figure 43 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 738 V

Drain current, Max. = 1.67 A

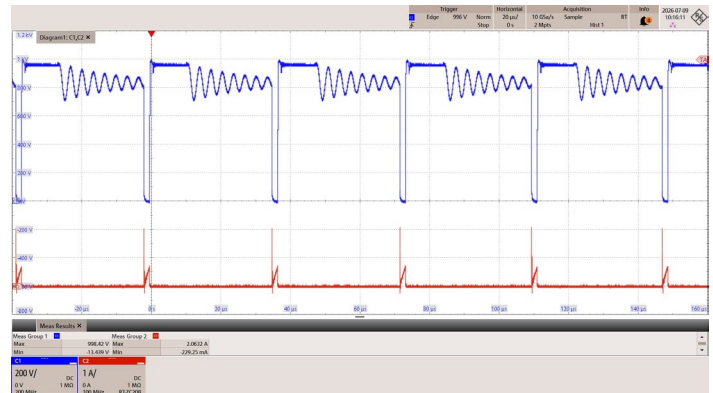


Figure 44 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 998 V

Drain current, Max. = 2.06 A

8.3.4 Drain Voltage and Current at Normal Operation (0% Load)

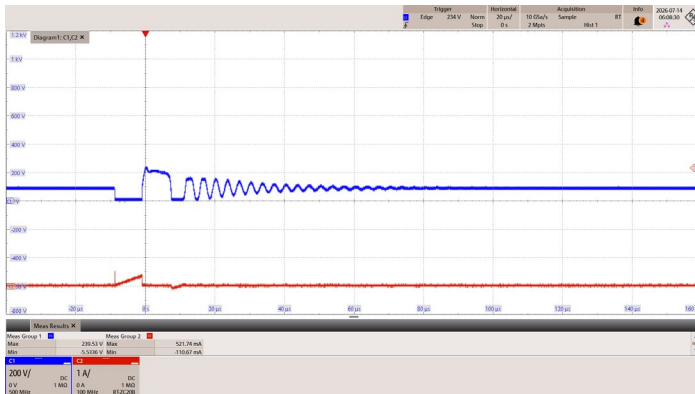


Figure 45 – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 240 V

Drain current, Max. = 0.522 A

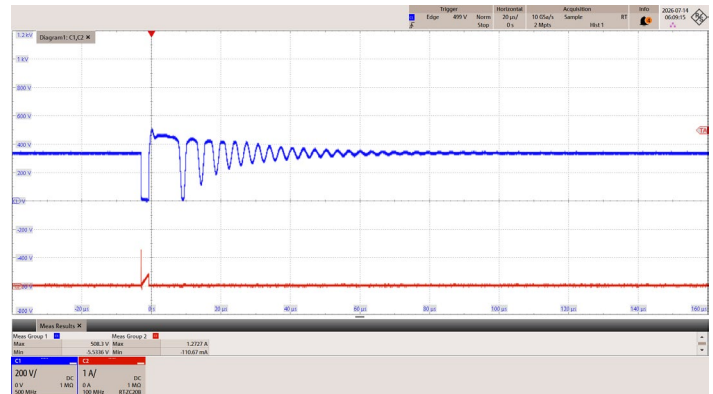


Figure 46 – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 508 V

Drain current, Max. = 1.27 A

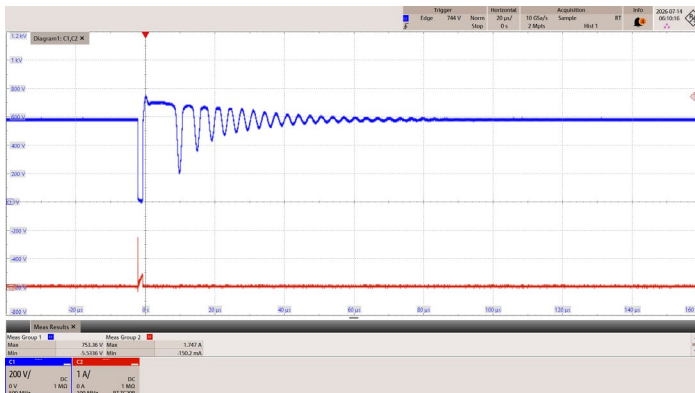


Figure 47 – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 753 V

Drain current, Max. = 1.75 A

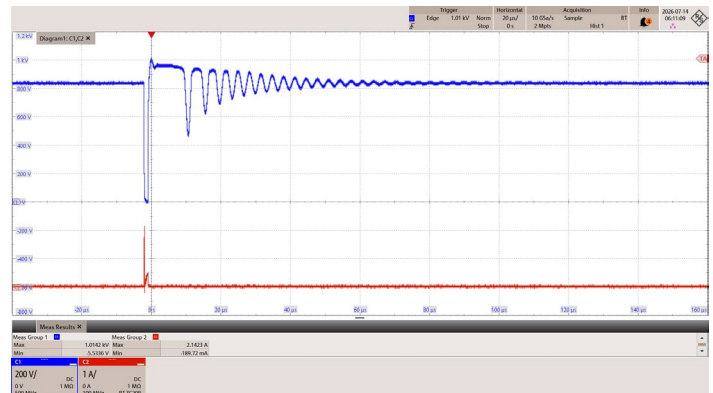


Figure 48 – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 1014 V

Drain current, Max. = 2.14 A

8.3.5 Drain Voltage and Current with Output Short

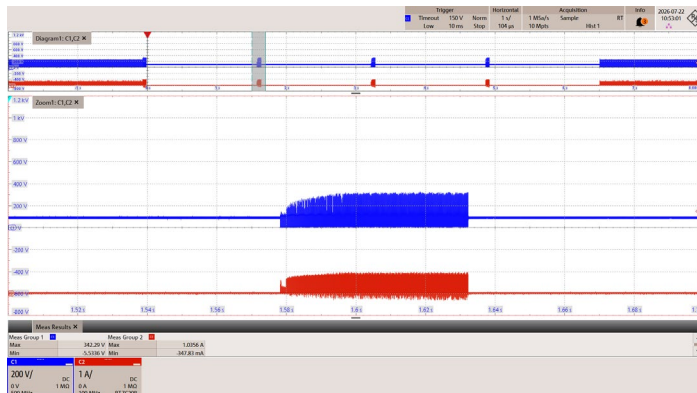


Figure 49 – 57 VAC, 60 Hz

CH1: Drain Voltage: 200 V / div, 1 s/div

CH2: Drain Current: 1 A / div, 1 s/div

Zoom: 20 ms / div

Drain voltage, Max. = 342 V

Drain current, Max. = 1.04 A

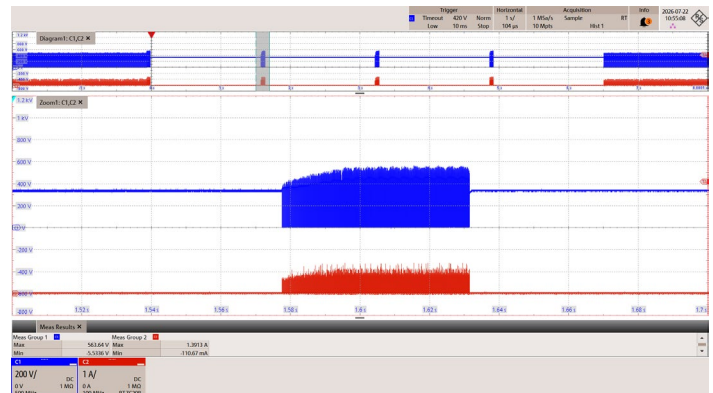


Figure 50 – 230 VAC, 50 Hz

CH1: Drain Voltage: 200 V / div, 1 s/div

CH2: Drain Current: 1 A / div, 1 s/div

Zoom: 20 ms / div

Drain voltage, Max. = 564 V

Drain current, Max. = 1.39 A

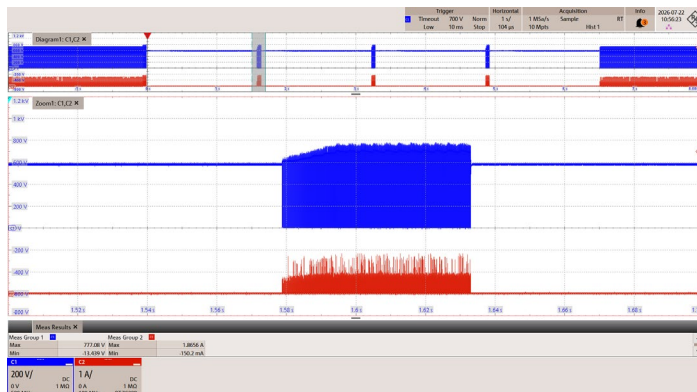


Figure 51 – 400 VAC, 50 Hz

CH1: Drain Voltage: 200 V / div, 1 s/div

CH2: Drain Current: 1 A / div, 1 s/div

Zoom: 20 ms / div

Drain voltage, Max. = 777 V

Drain current, Max. = 1.87 A

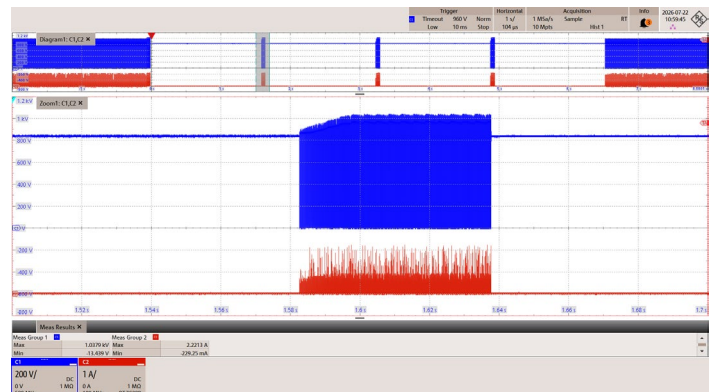


Figure 52 – 580 VAC, 50 Hz

CH1: Drain Voltage: 200 V / div, 1 s/div

CH2: Drain Current: 1 A / div, 1 s/div

Zoom: 20 ms / div

Drain voltage, Max. = 1038 V

Drain current, Max. = 2.22 A

8.4 SR FET Switching Waveforms

8.4.1 SR FET Voltage and Current at Start-up (100% Load)

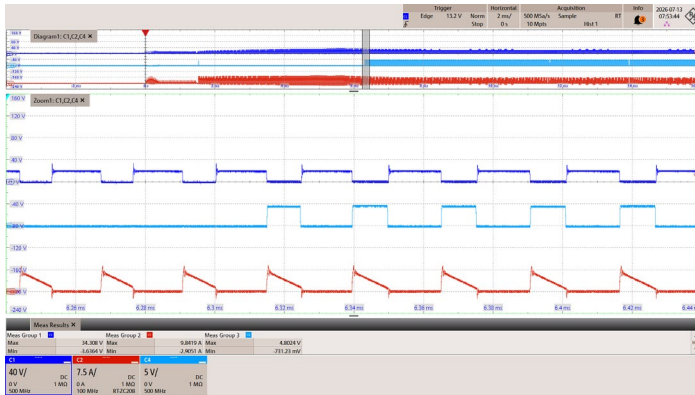


Figure 53 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 34.3 V

Secondary Winding Current, Max. = 9.8 A

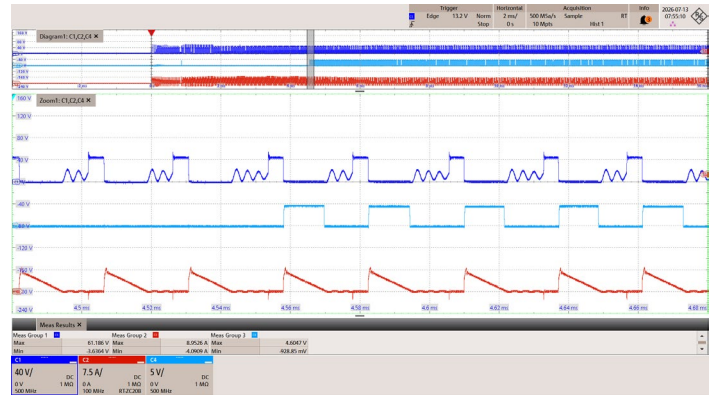


Figure 54 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 61.2 V

Secondary Winding Current, Max. = 9.0 A

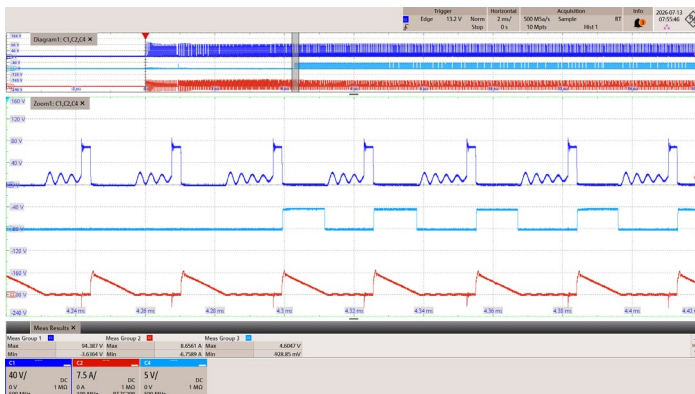


Figure 55 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 94.4 V

Secondary Winding Current, Max. = 8.7 A

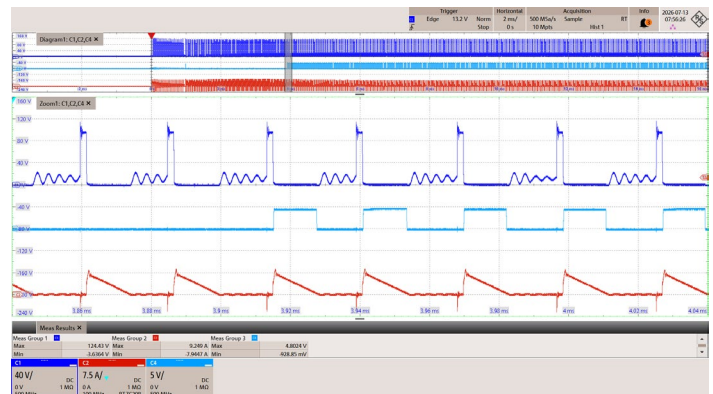


Figure 56 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

CH2: Winding Current: 7.5 A / div, 2 ms / div

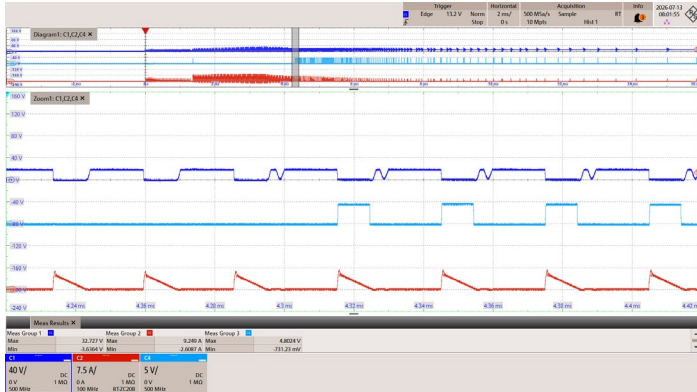
CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 124 V

Secondary Winding Current, Max. = 9.2 A

8.4.2 SR FET Voltage and Current at Start-up (0% Load)

**Figure 57** – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

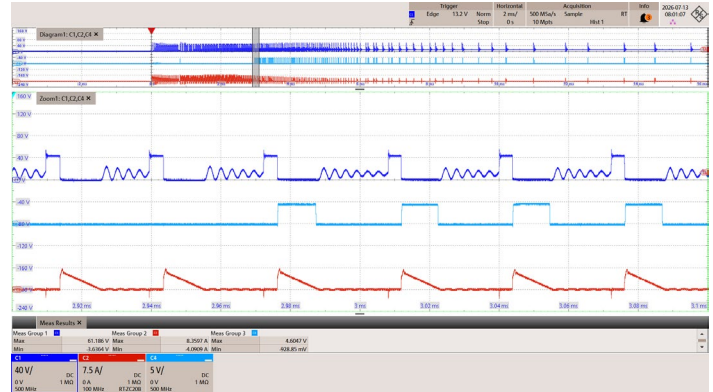
CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 32.7 V

Secondary Winding Current, Max. = 9.25 A

**Figure 58** – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

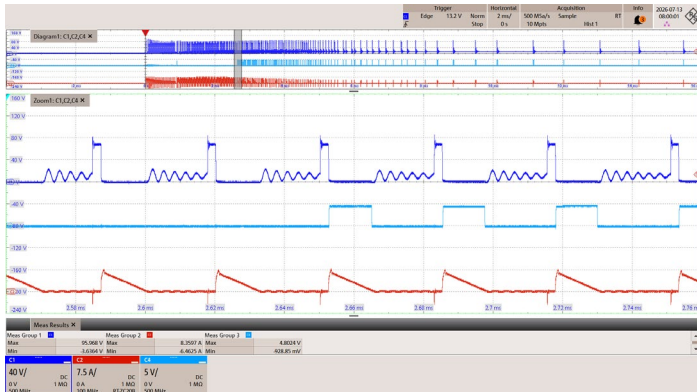
CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 61.2 V

Secondary Winding Current, Max. = 8.36 A

**Figure 59** – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

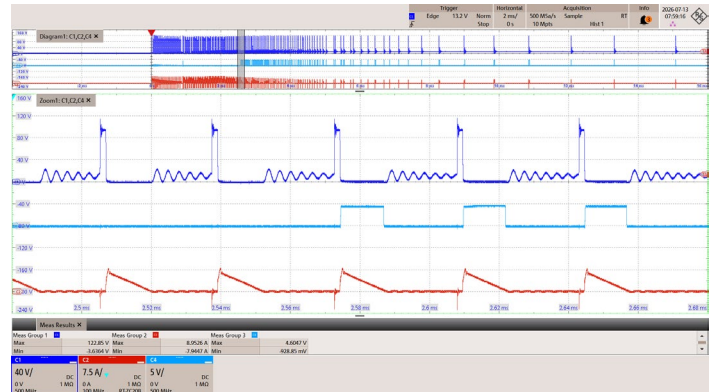
CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 96 V

Secondary Winding Current, Max. = 8.36 A

**Figure 60** – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div

CH2: Winding Current: 7.5 A / div, 2 ms / div

CH4: Gate Voltage: 5 V / div, 2 ms / div

Zoom: 20 μ s

SR FET Drain Voltage, Max. = 123 V

Secondary Winding Current, Max. = 8.95 A

8.4.3 SR FET Voltage and Current at Normal Operations (100% Load)

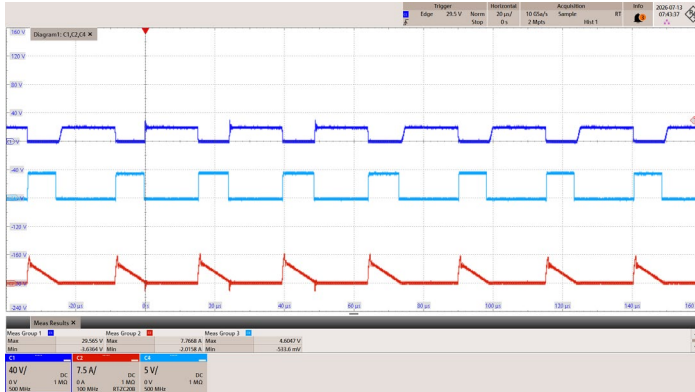


Figure 61 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 29.6 V
 Secondary Winding Current, Max. = 7.77 A

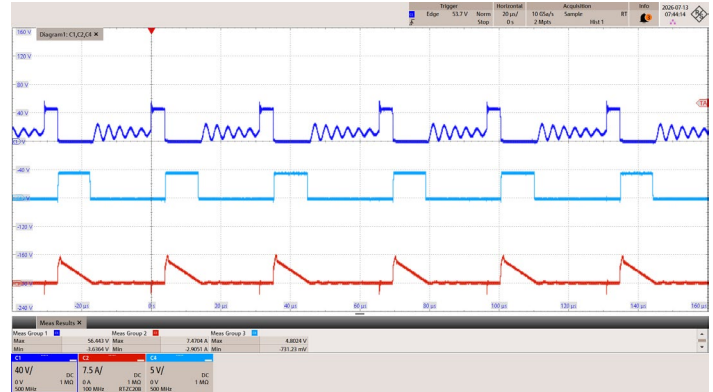


Figure 62 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 56.4 V
 Secondary Winding Current, Max. = 7.47 A

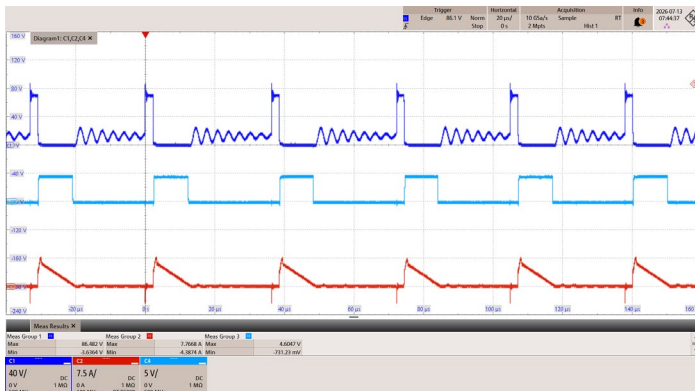


Figure 63 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 86.5 V
 Secondary Winding Current, Max. = 7.77 A

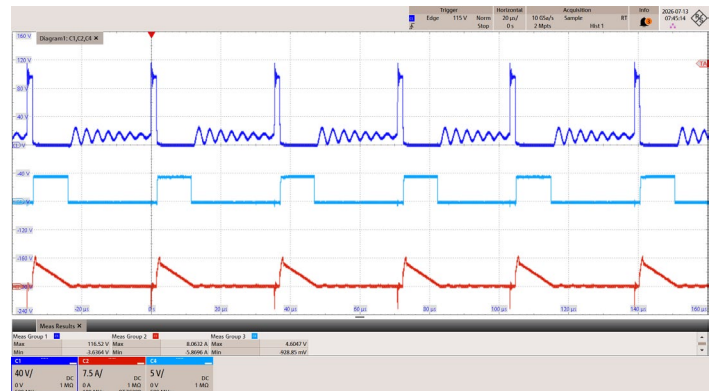


Figure 64 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 117 V
 Secondary Winding Current, Max. = 8.06 A

8.4.4 SR FET Voltage and Current at Normal Operations (0% Load)

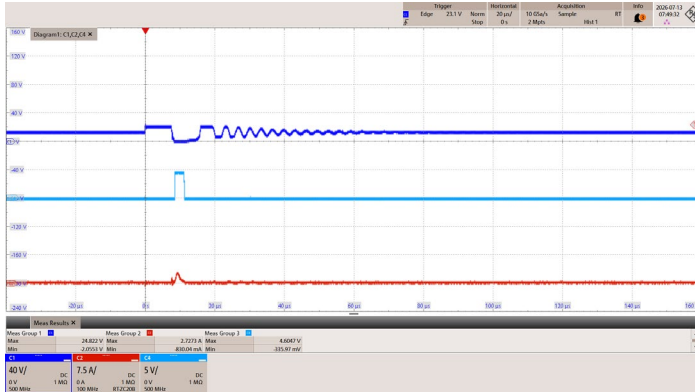


Figure 65 – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 24.8 V
 Secondary Winding Current, Max. = 2.72 A

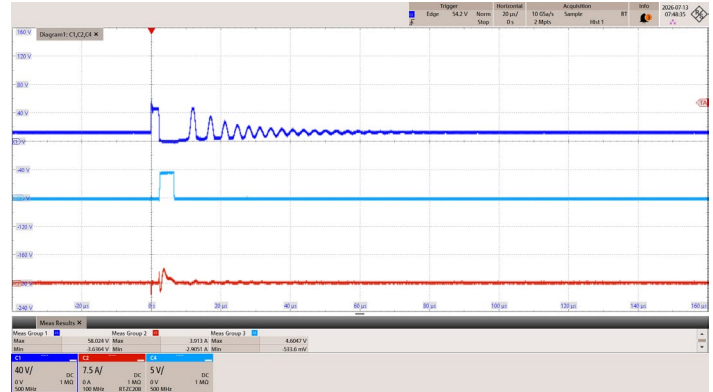


Figure 66 – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 58 V
 Secondary Winding Current, Max. = 3.91 A

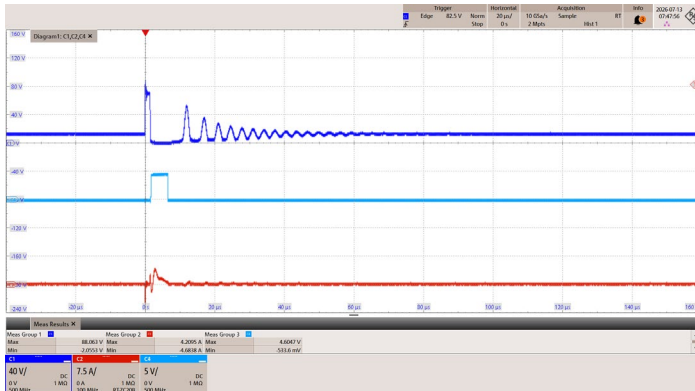


Figure 67 – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 88.1 V
 Secondary Winding Current, Max. = 4.21 A

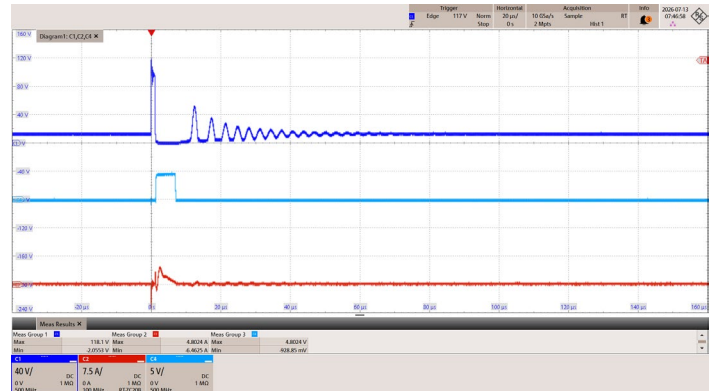


Figure 68 – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 20 μ s / div
 CH2: Winding Current: 7.5 A / div, 20 μ s / div
 CH4: Gate Voltage: 5 V / div, 20 μ s / div
 SR FET Drain Voltage, Max. = 118 V
 Secondary Winding Current, Max. = 4.8 A

8.5 Output Ripple Measurements

8.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in figures 69 and 70.

The 4905-1 probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors are one 0.1 μF /50 V ceramic and one 47 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

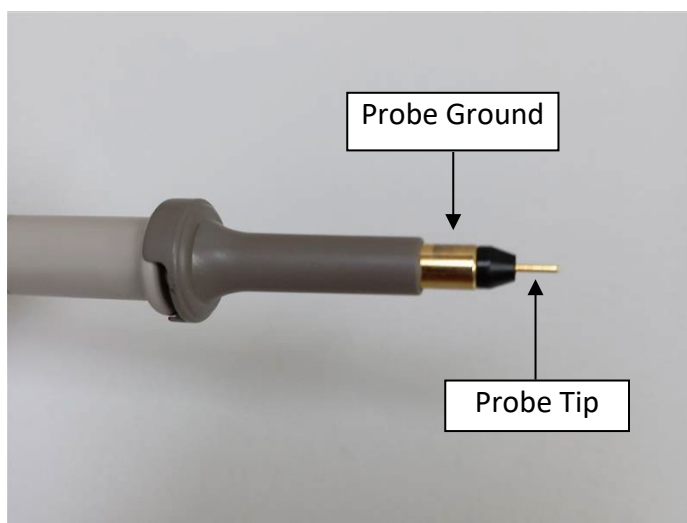


Figure 69 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

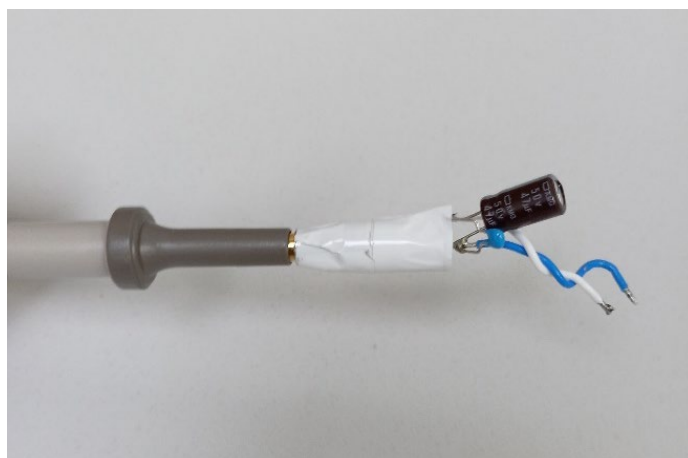


Figure 70 – Oscilloscope Probe with BNC Adapter.
(<https://probemaster.com/4900-oscilloscope-probe-basic-kit-150-300-mhz/>)

8.5.2 Ripple Waveforms (Measured on Board)

8.5.2.1 100% Load

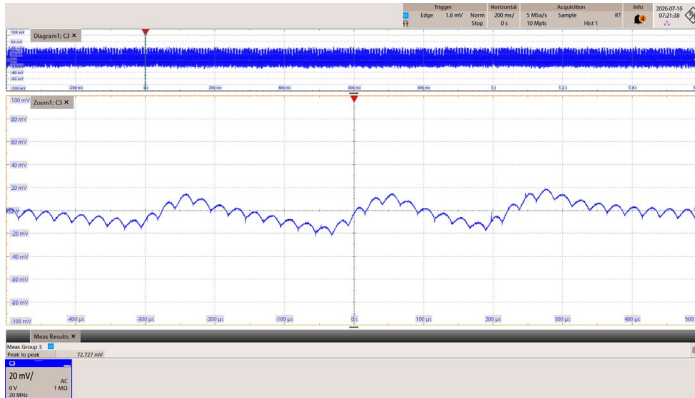


Figure 71 – 57 VAC, 60 Hz, $I_o = 1$ A (100% Load)

CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div

Zoom: 100 μs

Voltage Ripple: 72.7 mV_{pp}

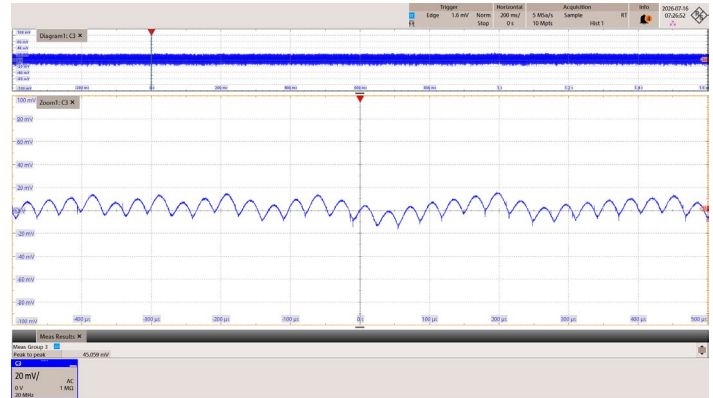


Figure 72 – 230 VAC, 50 Hz, $I_o = 1$ A (100% Load)

CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div

Zoom: 100 μs

Voltage Ripple: 45.1 mV_{pp}

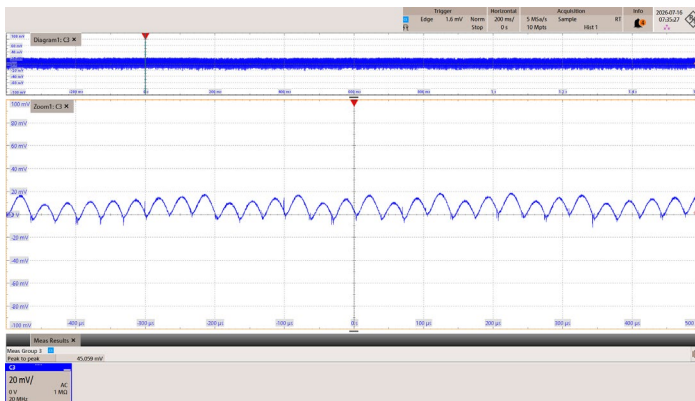


Figure 73 – 400 VAC, 50 Hz, $I_o = 1$ A (100% Load)

CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div

Zoom: 100 μs

Voltage Ripple: 45.1 mV_{pp}

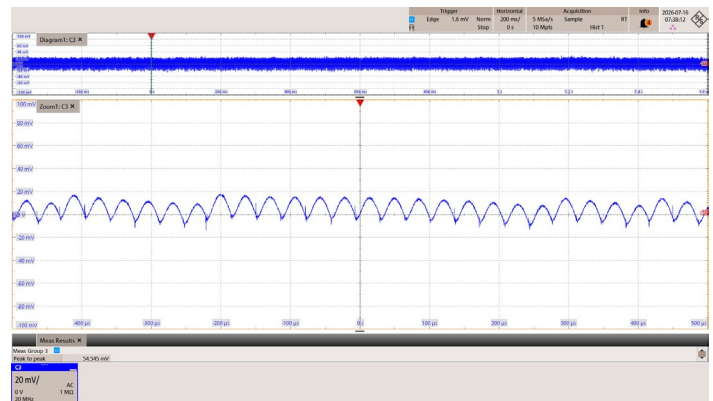


Figure 74 – 580 VAC, 60 Hz, $I_o = 1$ A (100% Load)

CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div

Zoom: 100 μs

Voltage Ripple: 54.5 mV_{pp}

8.5.2.2 50% Load

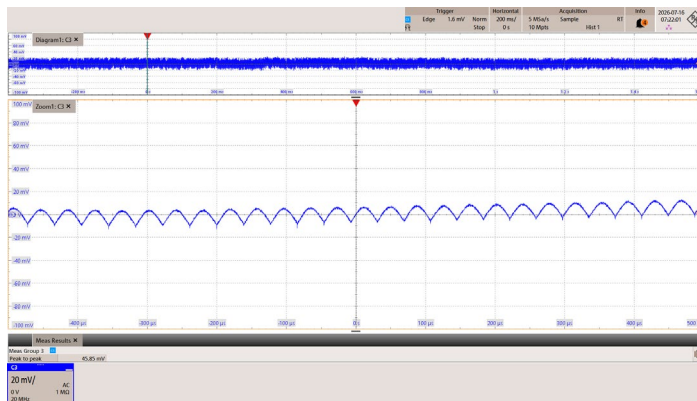


Figure 75 – 57 VAC, 60 Hz, $I_o = 0.5$ A (50% Load)
 CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div
 Zoom: 100 μ s
 Voltage Ripple: 45.9 mV_{pp}

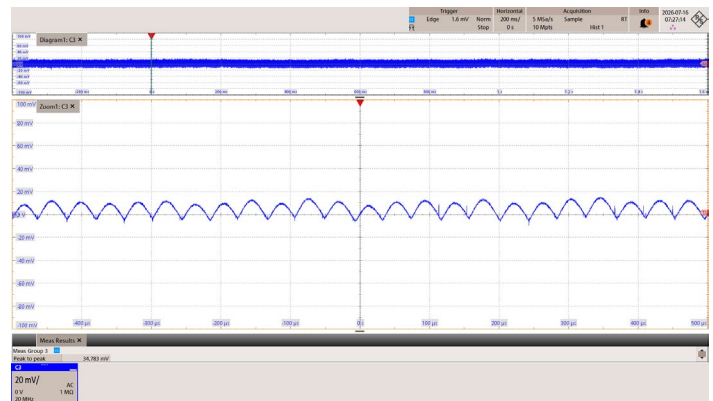


Figure 76 – 230 VAC, 50 Hz, $I_o = 0.5$ A (50% Load)
 CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div
 Zoom: 100 μ s
 Voltage Ripple: 34.8 mV_{pp}

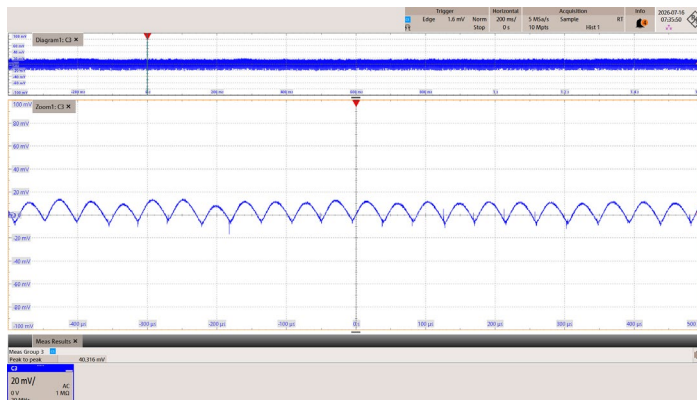


Figure 77 – 400 VAC, 50 Hz, $I_o = 0.5$ A (50% Load)
 CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div
 Zoom: 100 μ s
 Voltage Ripple: 40.3 mV_{pp}

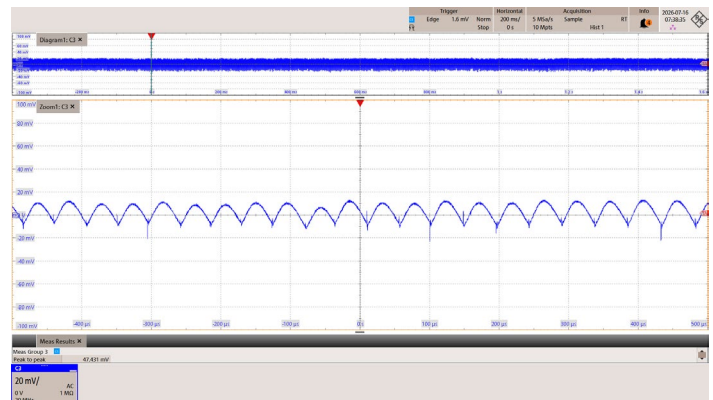
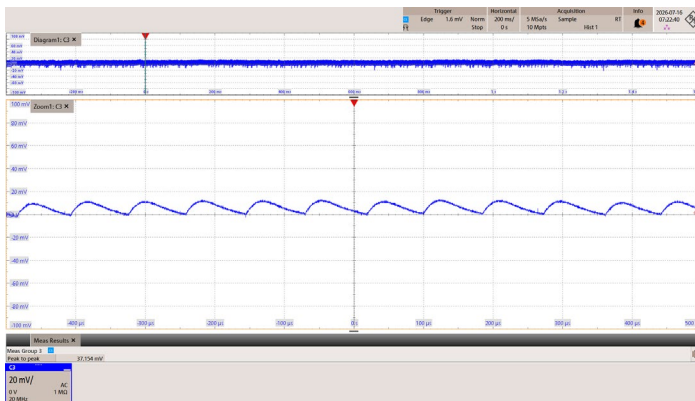
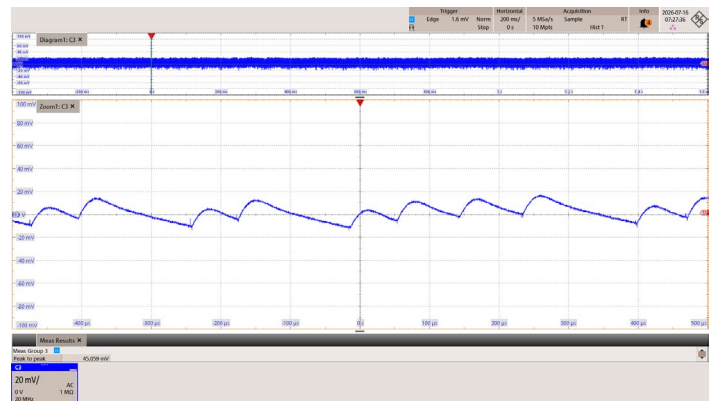
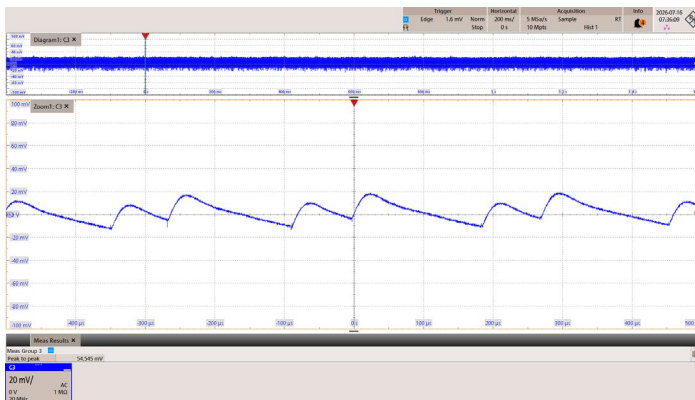
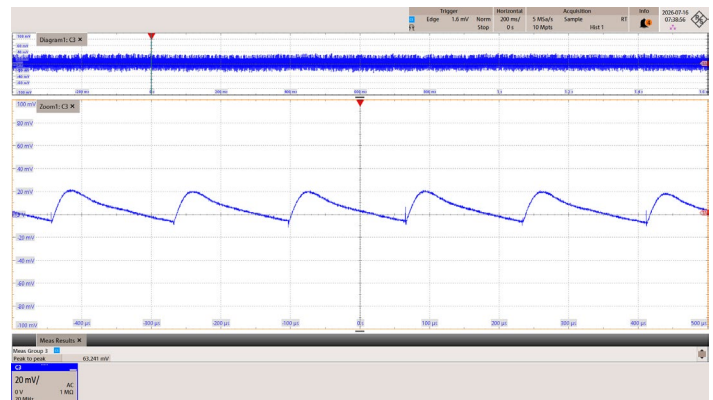


Figure 78 – 580 VAC, 60 Hz, $I_o = 0.5$ A (50% Load)
 CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / div
 Zoom: 100 μ s
 Voltage Ripple: 47.4 mV_{pp}

8.5.2.3 10% Load

**Figure 79** – 57 VAC, 60 Hz, $I_o = 0.1$ A (10% Load)CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / divZoom: 100 μ sVoltage Ripple: 37.2 mV_{pp}**Figure 80** – 230 VAC, 50 Hz, $I_o = 0.1$ A (10% Load)CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / divZoom: 100 μ sVoltage Ripple: 45.1 mV_{pp}**Figure 81** – 400 VAC, 50 Hz, $I_o = 0.1$ A (10% Load)CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / divZoom: 100 μ sVoltage Ripple: 54.5 mV_{pp}**Figure 82** – 580 VAC, 60 Hz, $I_o = 0.1$ A (10% Load)CH3: V_{OUT} Ripple: 20 mV / div, 200 ms / divZoom: 100 μ sVoltage Ripple: 63.2 mV_{pp}

8.5.3 Output Voltage Ripple

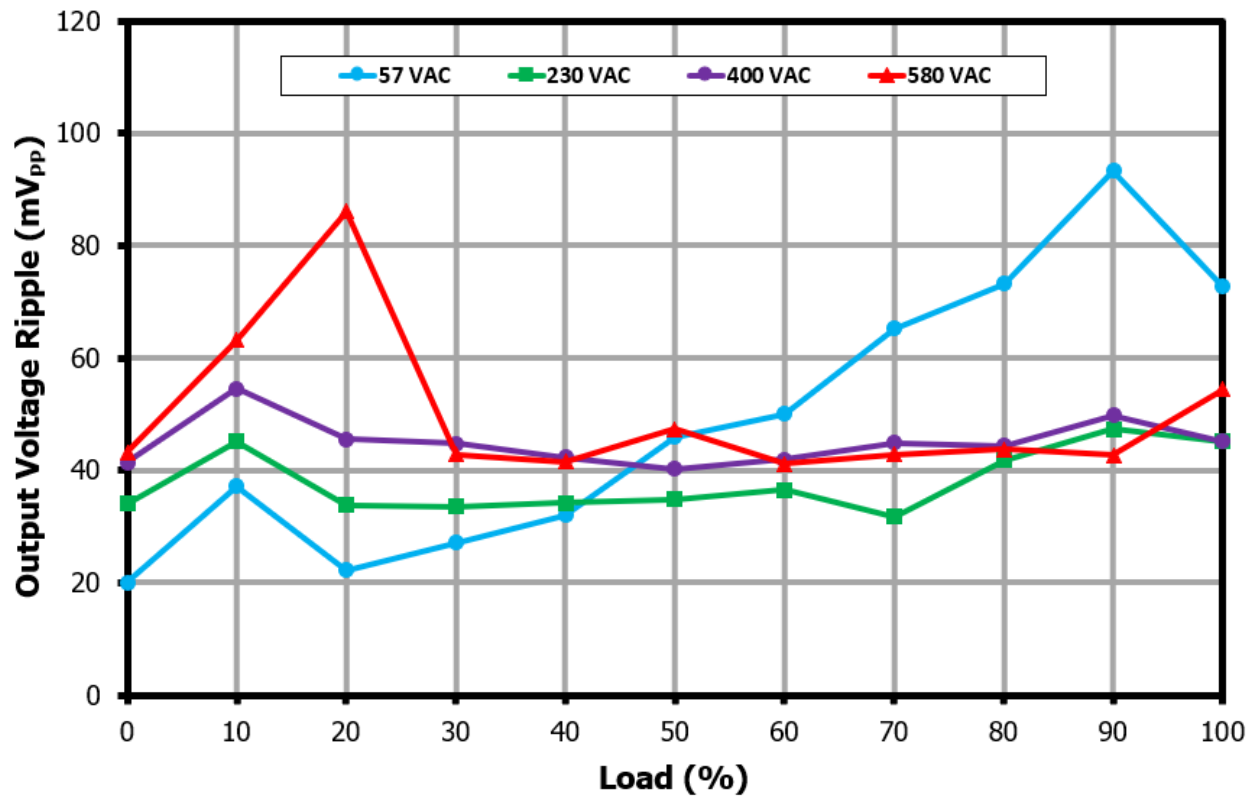


Figure 83 – Output Voltage Ripple

9 Conducted EMI

EMI Equipment and DUT Load

1. Rohde and Schwarz ENV216 two-line V-network
2. Rohde and Schwarz EPL EMI test receiver
3. Resistor load with value of 12 ohms

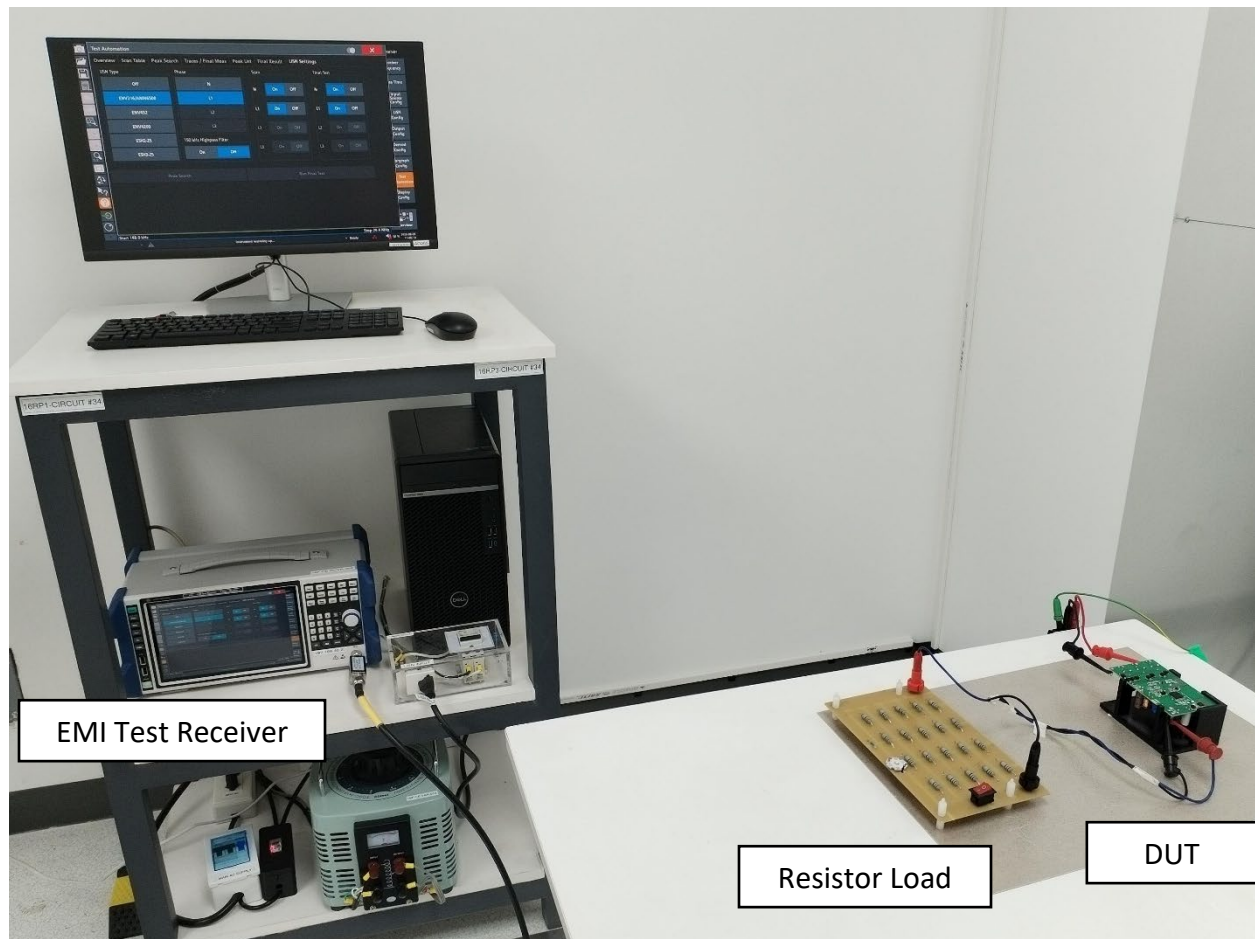


Figure 84 – Conducted EMI Test Set-up

9.1 Neutral

9.1.1 VIN: 115 VAC

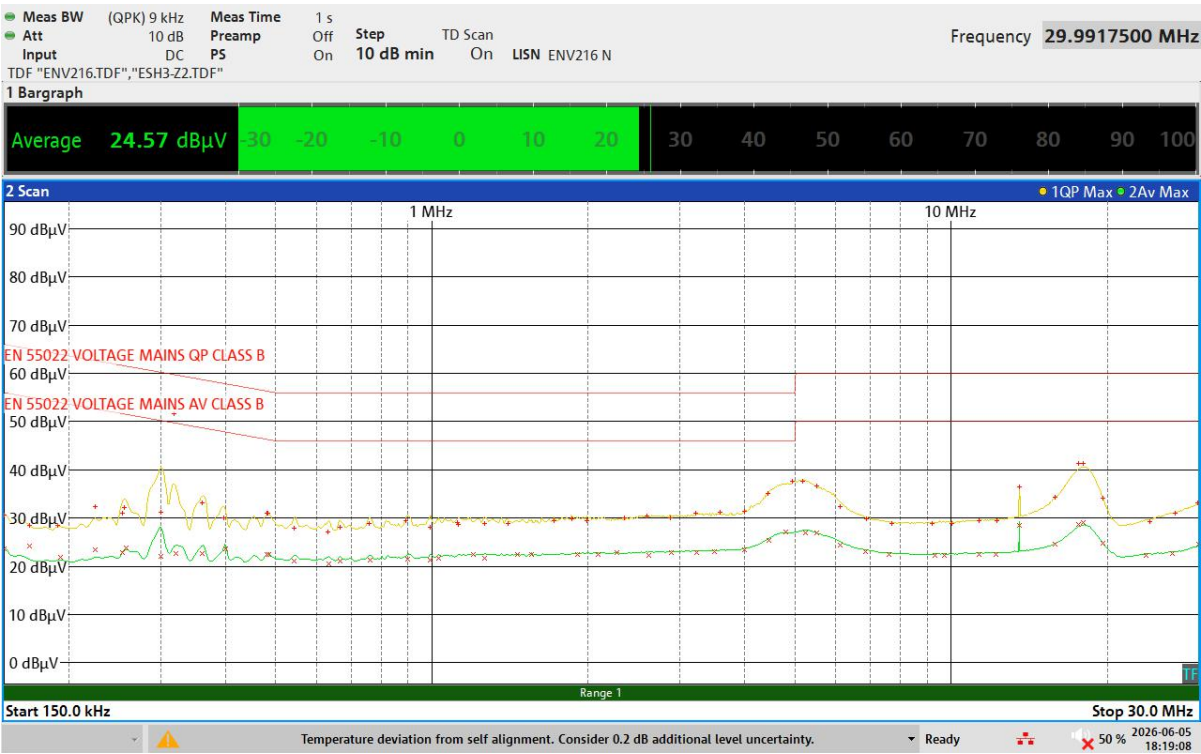


Figure 85 – Floating Ground EMI at 115 VAC b/w Input Lines A and B, Neutral

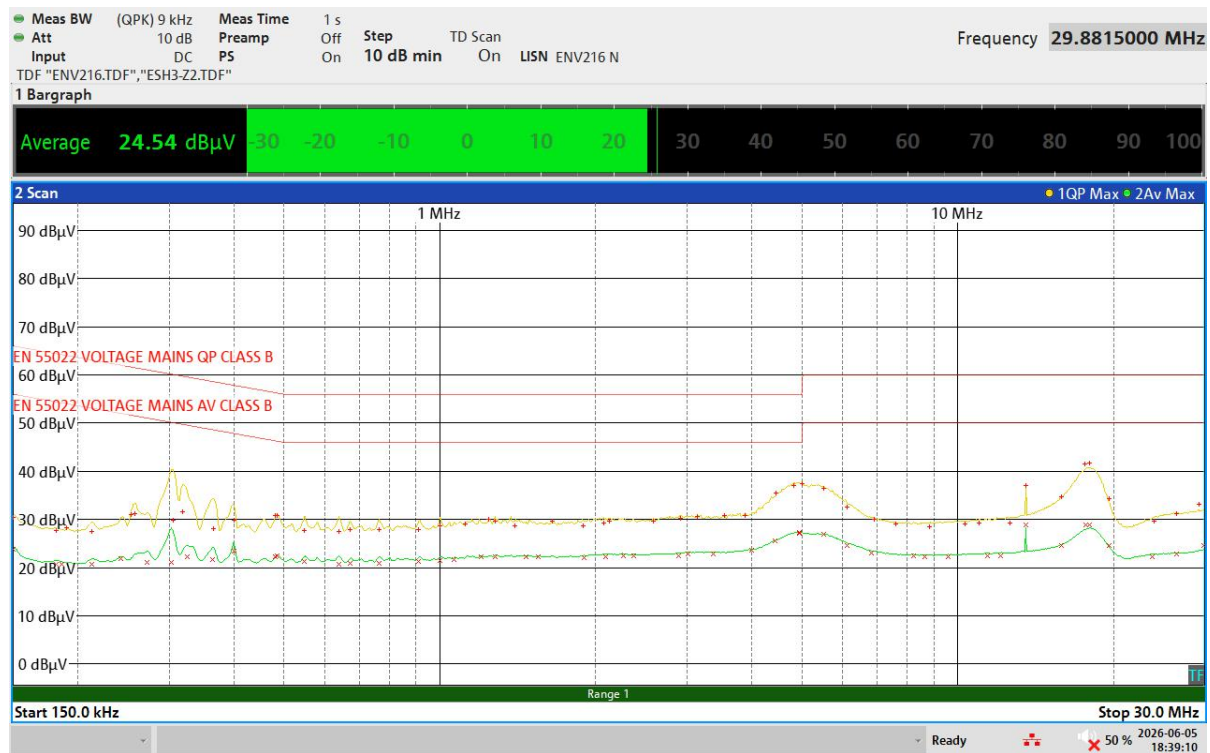


Figure 86 – Floating Ground EMI at 115 VAC b/w Input Lines B and C, Neutral

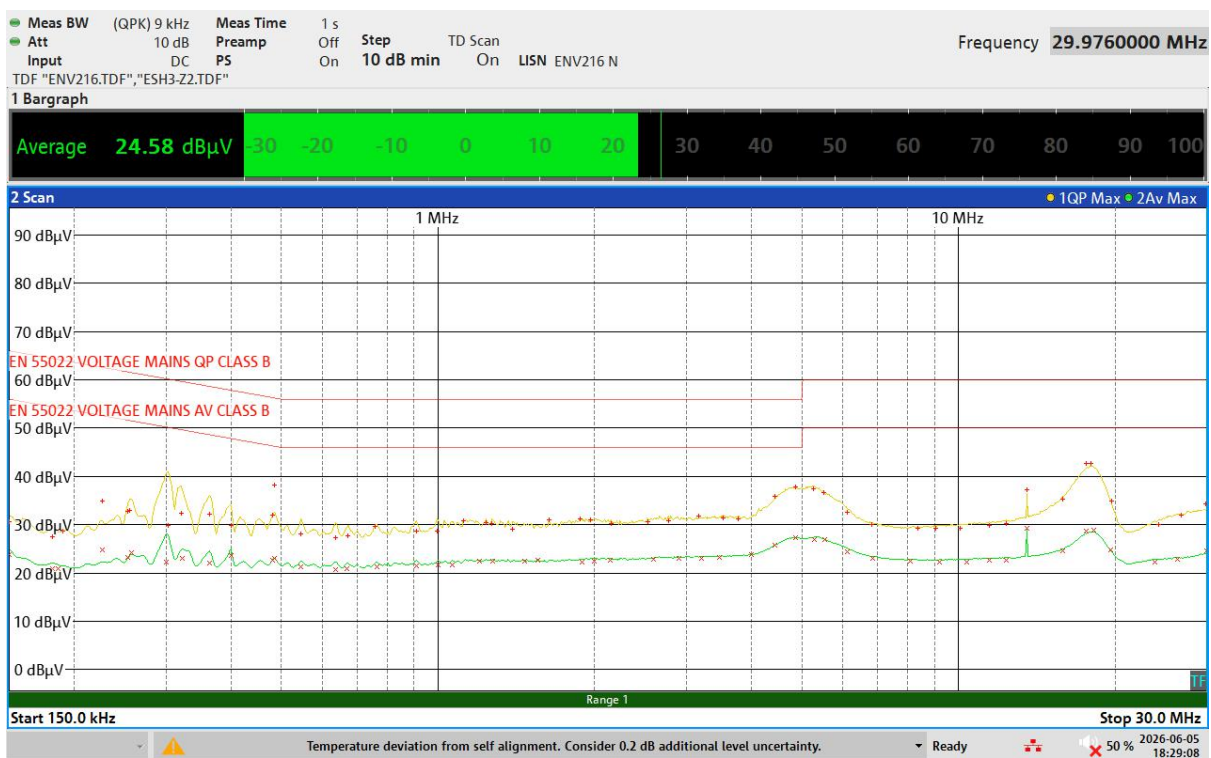


Figure 87 – Floating Ground EMI at 115 VAC b/w Input Lines A and C, Neutral



9.1.2 VIN: 230 VAC



Figure 88 – Floating Ground EMI at 230 VAC b/w Input Lines A and B, Neutral

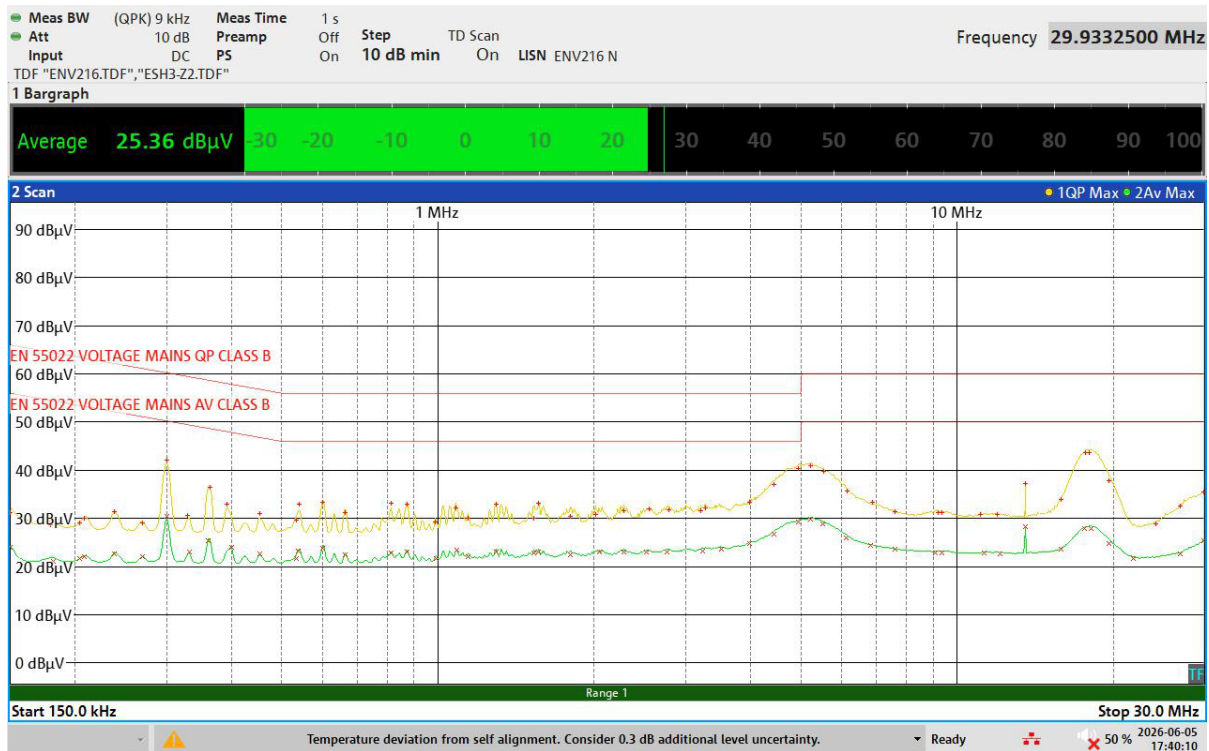


Figure 89 – Floating Ground EMI at 230 VAC b/w Input Lines B and C, Neutral

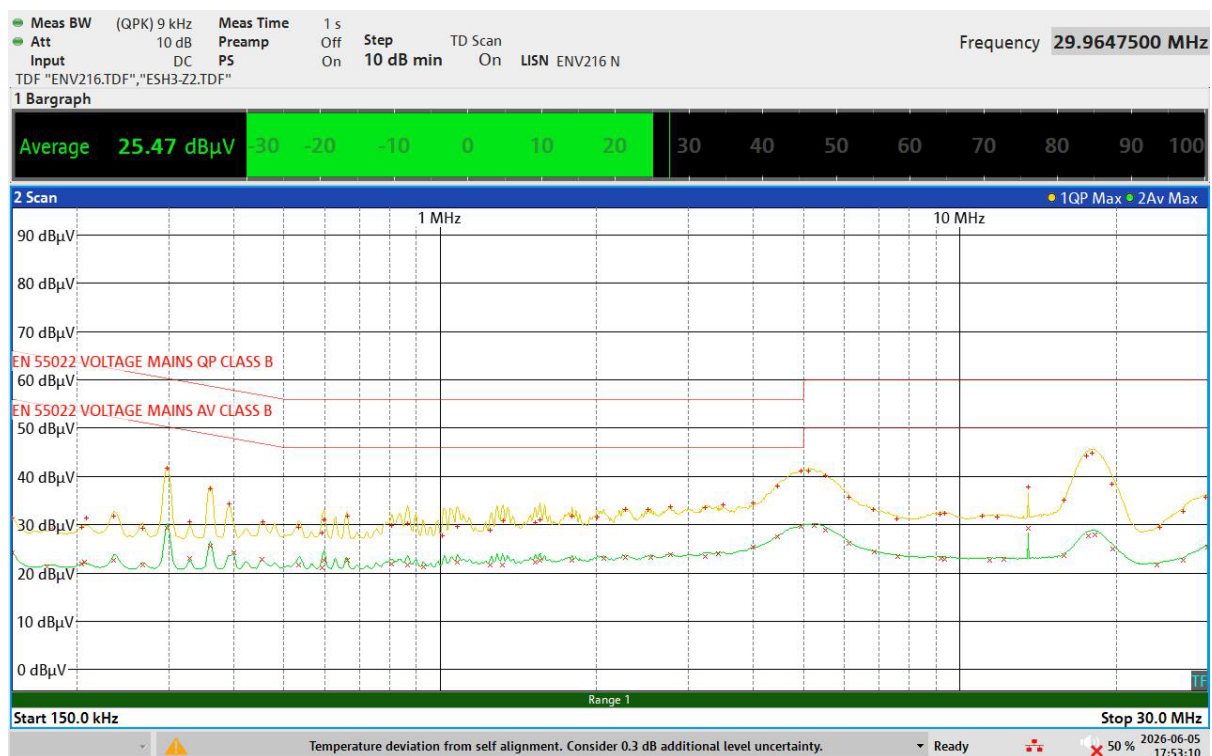


Figure 90 – Floating Ground EMI at 230 VAC b/w Input Lines A and C, Neutral

9.2 Line

9.2.1 VIN: 115 VAC

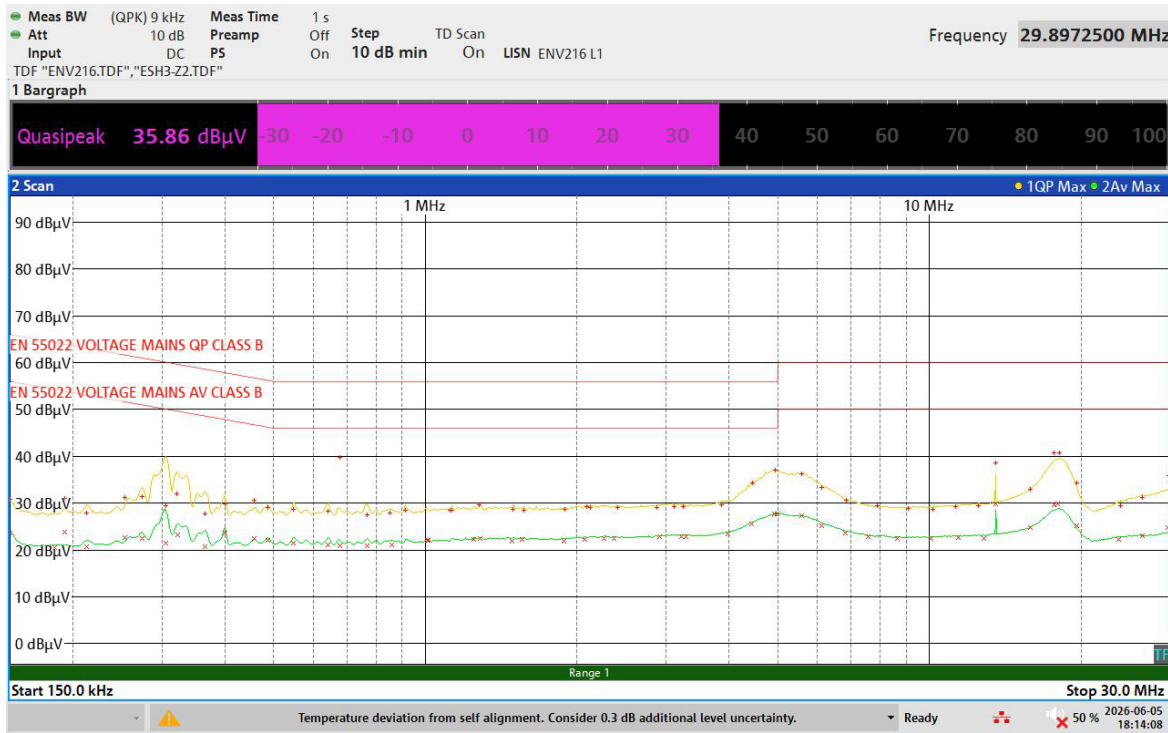


Figure 91 – Floating Ground EMI at 115 VAC b/w Input Lines A and B, Line

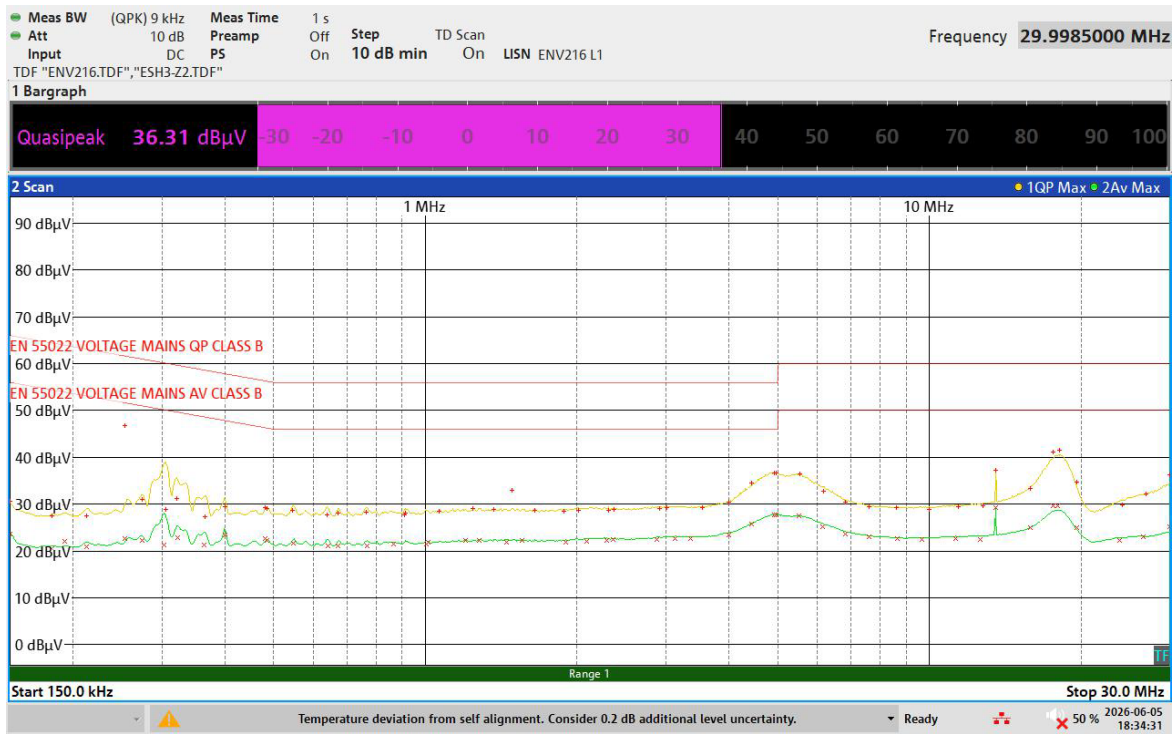


Figure 92 – Floating Ground EMI at 115 VAC b/w Input Lines B and C, Line

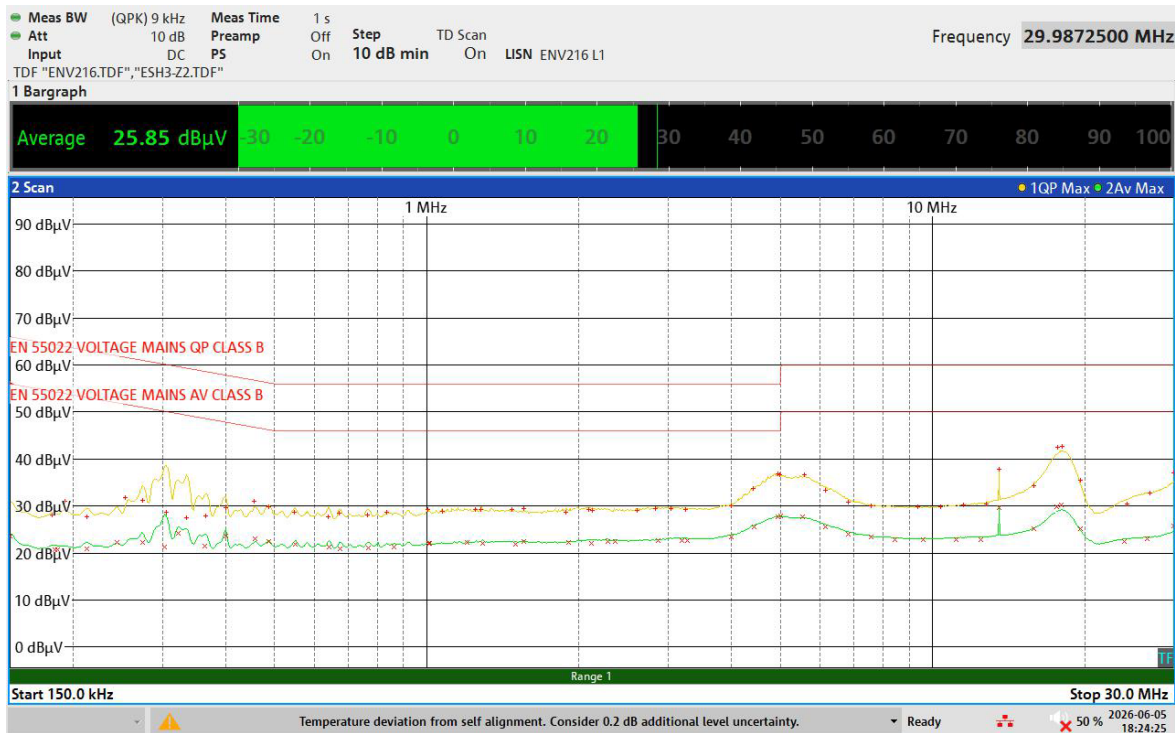


Figure 93 – Floating Ground EMI at 115 VAC b/w Input Lines A and C, Line



9.2.2 VIN: 230 VAC

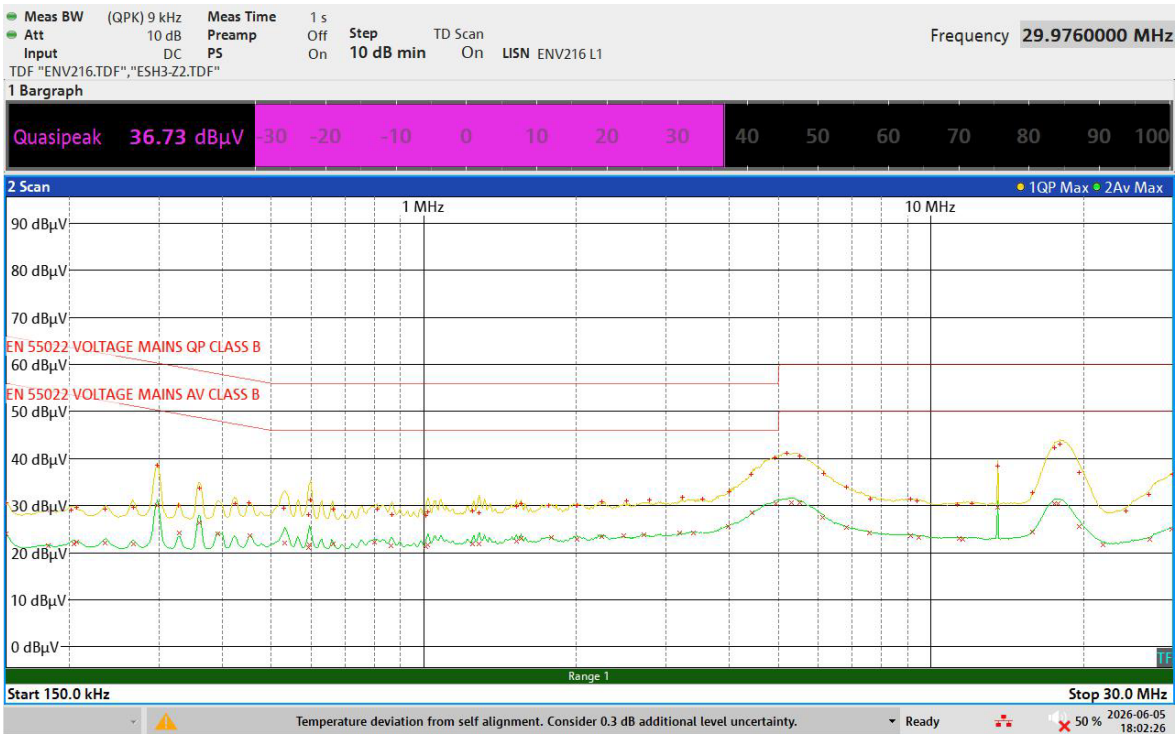


Figure 94 – Floating Ground EMI at 230 VAC b/w Input Lines A and B, Line

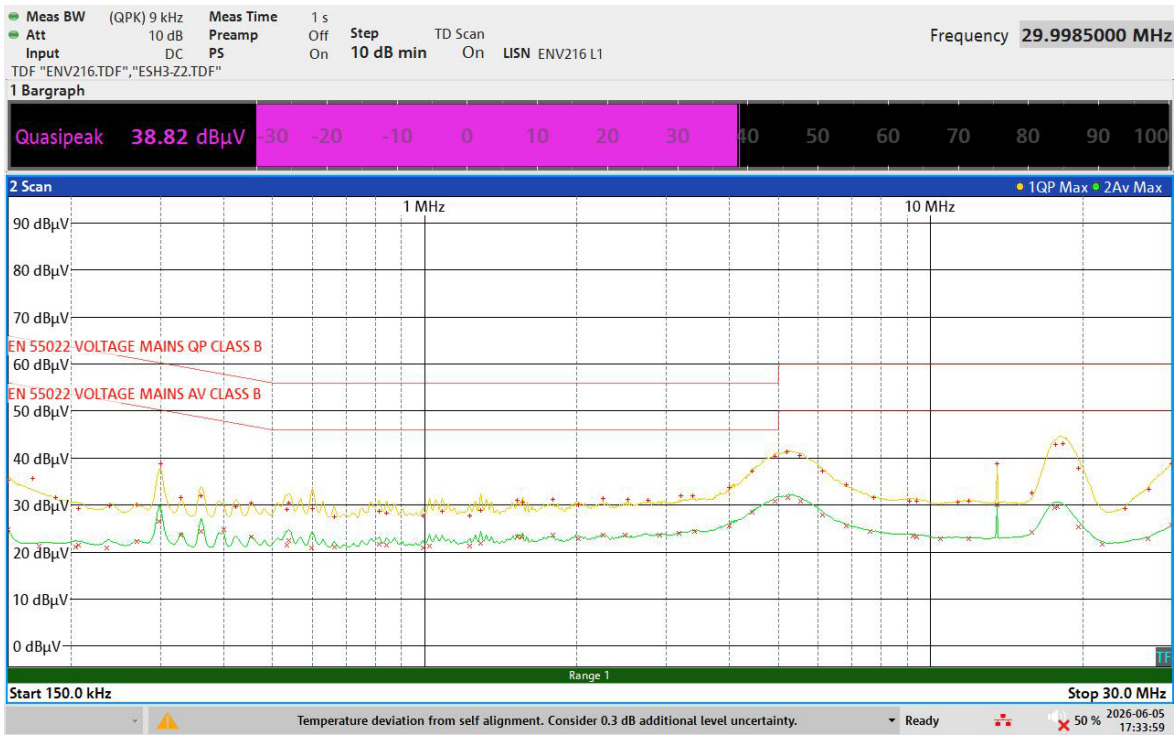


Figure 95 – Floating Ground EMI at 230 VAC b/w Input Lines B and C, Line

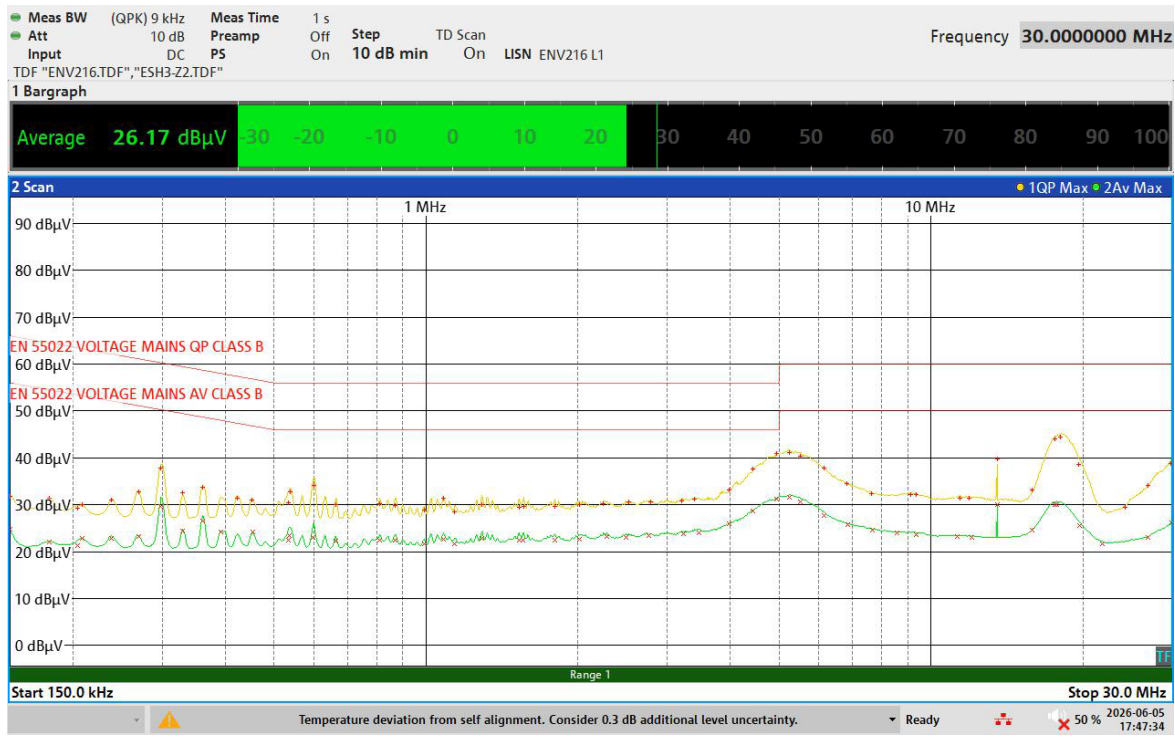


Figure 96 – Floating Ground EMI at 230 VAC b/w Input Lines A and C, Line



10 Line Surge

10.1 Differential Mode Test

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	Line A, N	2	10	Pass
−6000	90	Line A, N	2	10	Pass
+6000	180	Line A, N	2	10	Pass
−6000	180	Line A, N	2	10	Pass
+6000	270	Line A, N	2	10	Pass
−6000	270	Line A, N	2	10	Pass
+6000	90	Line B, N	2	10	Pass
−6000	90	Line B, N	2	10	Pass
+6000	180	Line B, N	2	10	Pass
−6000	180	Line B, N	2	10	Pass
+6000	270	Line B, N	2	10	Pass
−6000	270	Line B, N	2	10	Pass
+6000	90	Line C, N	2	10	Pass
−6000	90	Line C, N	2	10	Pass
+6000	180	Line C, N	2	10	Pass
−6000	180	Line C, N	2	10	Pass
+6000	270	Line C, N	2	10	Pass
−6000	270	Line C, N	2	10	Pass

Table 14 – Test Data at 6 kV Differential Surge



11 EFT

Surge Voltage (V)	Phase Angle (°)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	90	Line A, N - PE	5	15 ms	300	120	Pass
-4000	90	Line A, N - PE	5	15 ms	300	120	Pass
+4000	180	Line A, N - PE	5	15 ms	300	120	Pass
-4000	180	Line A, N - PE	5	15 ms	300	120	Pass
+4000	270	Line A, N - PE	5	15 ms	300	120	Pass
-4000	270	Line A, N - PE	5	15 ms	300	120	Pass
+4000	90	Line A, N - PE	100	750 µs	300	120	Pass
-4000	90	Line A, N - PE	100	750 µs	300	120	Pass
+4000	180	Line A, N - PE	100	750 µs	300	120	Pass
-4000	180	Line A, N - PE	100	750 µs	300	120	Pass
+4000	270	Line A, N - PE	100	750 µs	300	120	Pass
-4000	270	Line A, N - PE	100	750 µs	300	120	Pass
+4000	90	Line B, N - PE	5	15 ms	300	120	Pass
-4000	90	Line B, N - PE	5	15 ms	300	120	Pass
+4000	180	Line B, N - PE	5	15 ms	300	120	Pass
-4000	180	Line B, N - PE	5	15 ms	300	120	Pass
+4000	270	Line B, N - PE	5	15 ms	300	120	Pass
-4000	270	Line B, N - PE	5	15 ms	300	120	Pass
+4000	90	Line B, N - PE	100	750 µs	300	120	Pass
-4000	90	Line B, N - PE	100	750 µs	300	120	Pass
+4000	180	Line B, N - PE	100	750 µs	300	120	Pass
-4000	180	Line B, N - PE	100	750 µs	300	120	Pass
+4000	270	Line B, N - PE	100	750 µs	300	120	Pass
-4000	270	Line B, N - PE	100	750 µs	300	120	Pass

+4000	90	Line C, N - PE	5	15 ms	300	120	Pass
-4000	90	Line C, N - PE	5	15 ms	300	120	Pass
+4000	180	Line C, N - PE	5	15 ms	300	120	Pass
-4000	180	Line C, N - PE	5	15 ms	300	120	Pass
+4000	270	Line C, N - PE	5	15 ms	300	120	Pass
-4000	270	Line C, N - PE	5	15 ms	300	120	Pass
+4000	90	Line C, N - PE	100	750 μ s	300	120	Pass
-4000	90	Line C, N - PE	100	750 μ s	300	120	Pass
+4000	180	Line C, N - PE	100	750 μ s	300	120	Pass
-4000	180	Line C, N - PE	100	750 μ s	300	120	Pass
+4000	270	Line C, N - PE	100	750 μ s	300	120	Pass
-4000	270	Line C, N - PE	100	750 μ s	300	120	Pass

Table 15 – Test Data at 4 kV EFT

12 Electrostatic Discharge (ESD)

The power supply passed ± 16.5 kV air discharge and ± 8.8 kV contact discharge at both output positive and negative terminals, under full load condition for both 115 VAC and 230 VAC line input on each L-N input combination.

12.1 Contact Discharge at 115 VAC and 230 VAC

Contact Discharge Voltage (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 2	V _{OUT} (+)	10	0/10	PASS
- 2		10	0/10	PASS
+ 2	V _{OUT} (-)	10	0/10	PASS
- 2		10	0/10	PASS
+ 4	V _{OUT} (+)	10	0/10	PASS
- 4		10	0/10	PASS
+ 4	V _{OUT} (-)	10	0/10	PASS
- 4		10	0/10	PASS
+ 6	V _{OUT} (+)	10	0/10	PASS
- 6		10	0/10	PASS
+ 6	V _{OUT} (-)	10	0/10	PASS
- 6		10	0/10	PASS
+ 8	V _{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V _{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8.8	V _{OUT} (+)	10	0/10	PASS
- 8.8		10	0/10	PASS
+ 8.8	V _{OUT} (-)	10	0/10	PASS
- 8.8		10	0/10	PASS

Table 16 – Test Data at 115 VAC and 230 VAC



12.2 Air Discharge at 115 VAC and 230 VAC

Contact Discharge Voltage (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 8	V _{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V _{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 10	V _{OUT} (+)	10	0/10	PASS
- 10		10	0/10	PASS
+ 10	V _{OUT} (-)	10	0/10	PASS
- 10		10	0/10	PASS
+ 12	V _{OUT} (+)	10	0/10	PASS
- 12		10	0/10	PASS
+ 12	V _{OUT} (-)	10	0/10	PASS
- 12		10	0/10	PASS
+ 14	V _{OUT} (+)	10	0/10	PASS
- 14		10	0/10	PASS
+ 14	V _{OUT} (-)	10	0/10	PASS
- 14		10	0/10	PASS
+ 15	V _{OUT} (+)	10	0/10	PASS
- 15		10	0/10	PASS
+ 15	V _{OUT} (-)	10	0/10	PASS
- 15		10	0/10	PASS
+ 16.5	V _{OUT} (+)	10	0/10	PASS
- 16.5		10	0/10	PASS
+ 16.5	V _{OUT} (-)	10	0/10	PASS
- 16.5		10	0/10	PASS

Table 17 – Test Data at 115 and 230 VAC



13 Performance with External Magnetizing Interference

13.1 Test Set-up

An N42 grade Neodymium (NdFeB) disc magnet with a diameter of 25.4 mm and thickness of 12.7 mm, and a surface strength of 4667 Gauss was placed near the transformer core such that the typical primary inductance was reduced by at least 57%.

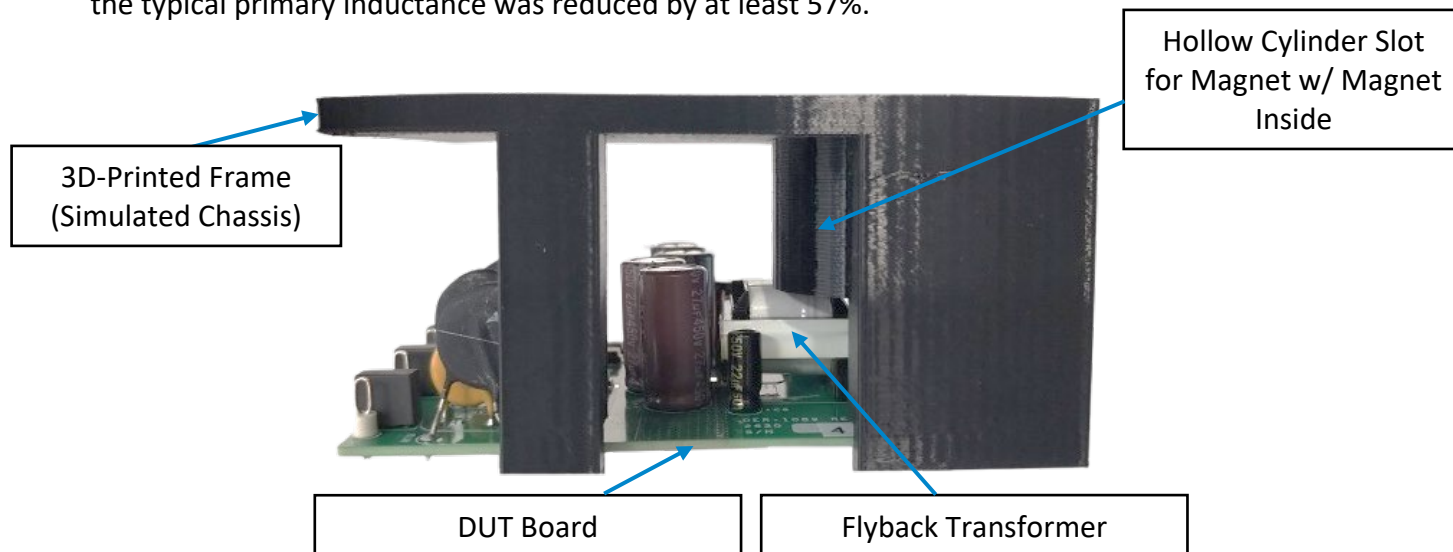


Figure 97 – Performance with External Magnetizing Interference Test Set-up

The magnet position was evaluated in two directions: the in-plane position parallel to the PCB and the out-of-plane separation perpendicular to the PCB. In the plane parallel to the PCB, the greatest reduction in typical primary inductance was observed when the center of the neodymium disc magnet was offset 10 mm to the right and 10 mm below the center of the transformer.

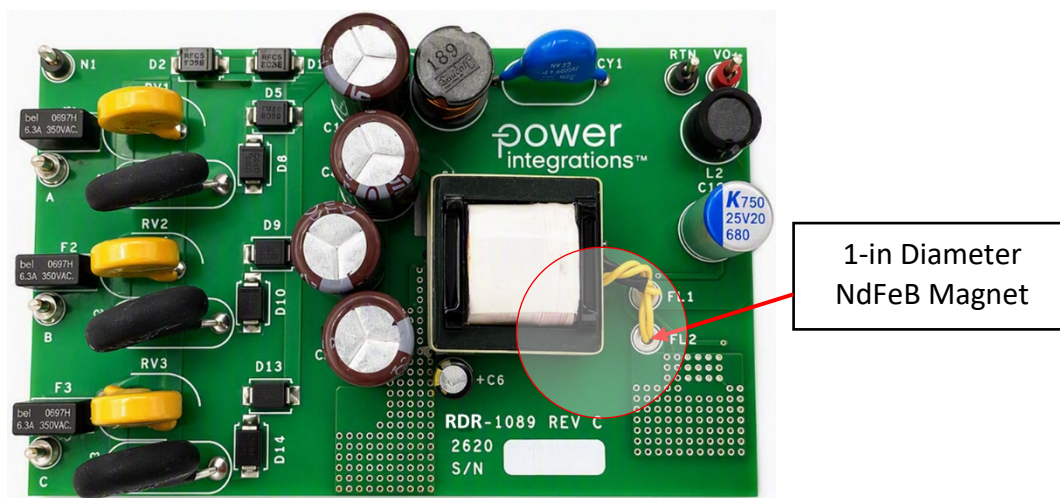


Figure 98 – Board Top Image Showing Test Position of Neodymium Magnet



A horizontal-bobbin transformer was used so that the magnet could approach the transformer most closely along the direction perpendicular to the PCB. Because the transformer is centered on the PCB, the PCB edges act as physical barriers that limit the magnet's lateral approach. Therefore, once the optimal in-plane position was established, the perpendicular magnet-to-transformer separation became the primary parameter of interest. The typical primary inductance decreased as this separation was reduced. At a perpendicular separation of 10 mm, measured from the top surface of the transformer to the nearest surface of the magnet, the typical primary inductance was reduced by at least 57%.

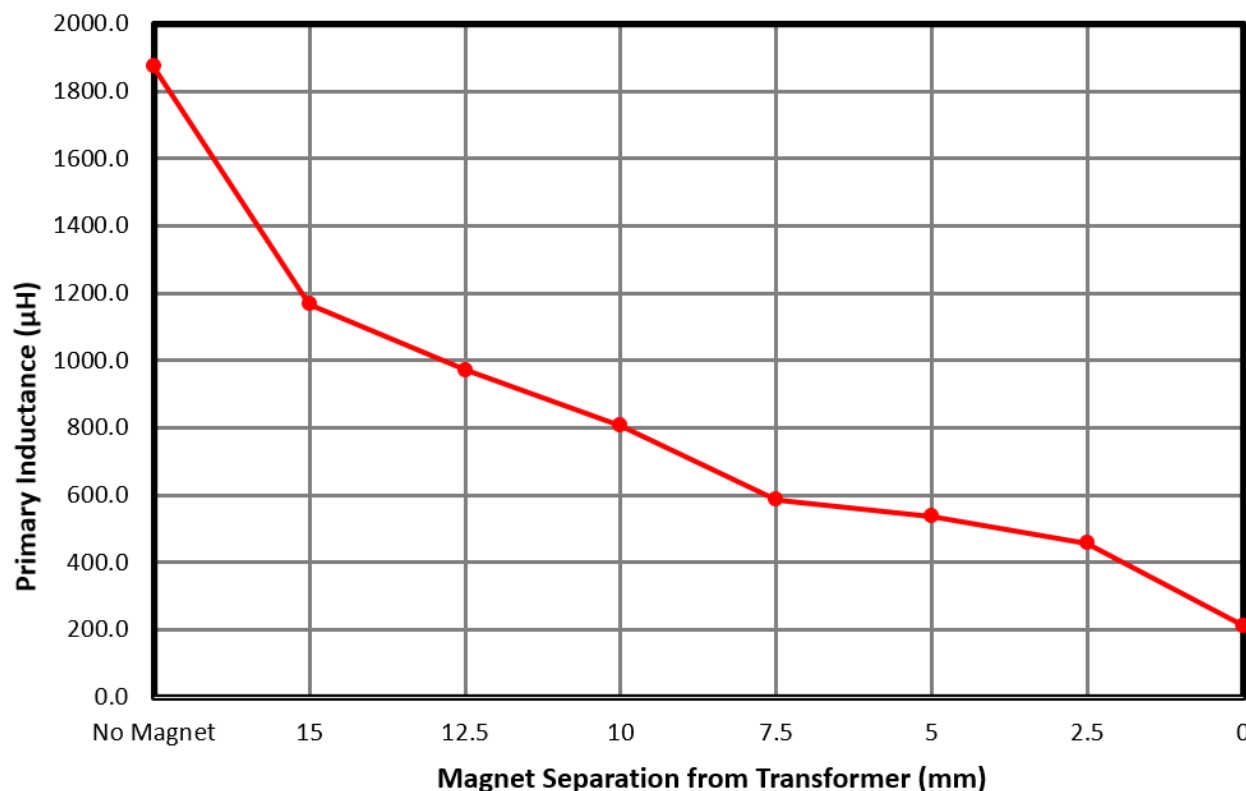


Figure 99 – Primary Inductance vs. Perpendicular Magnet-to-Transformer Separation

Although a perpendicular magnet separation of 10 mm was used for this report, it does not represent the minimum separation at which the power supply can remain operational. The magnet can be moved closer to the transformer while the board continues to deliver the full rated output of 12 V, 1 A. However, decreasing the magnet separation further reduces the primary inductance, causing the InnoSwitch3-EP controller to operate at a higher switching frequency and increasing component temperatures.

At the 10 mm magnet separation, corresponding to a primary-inductance reduction of at least 57%, the board can operate continuously over the full specified input-voltage range of 57 VAC to 580 VAC. At an ambient temperature of 40 °C, the highest measured component temperature was 106 °C at the transformer core.

As shown in Figure 99 when the separation is reduced to 5 mm, the primary inductance decreases by approximately 70% relative to its nominal value. Although the board can still deliver full power at this separation, the maximum allowable input voltage is reduced to approximately 520 VAC because of thermal limitations.

At even smaller separations, full-power operation may remain possible over a further reduced input-voltage range, but thermal limitations and reduced margin against transformer core saturation become increasingly significant. Therefore, 10 mm represents the closest magnet separation at which the power supply can meet its full specification of 12 V, 1 A over the complete input-voltage range of 57 VAC to 580 VAC. The 10 mm magnet separation from the transformer core is thus a full-specification limit rather than the absolute functional limit of the power supply.

13.2 Full-Load Efficiency vs. Line with External Magnetizing Interference

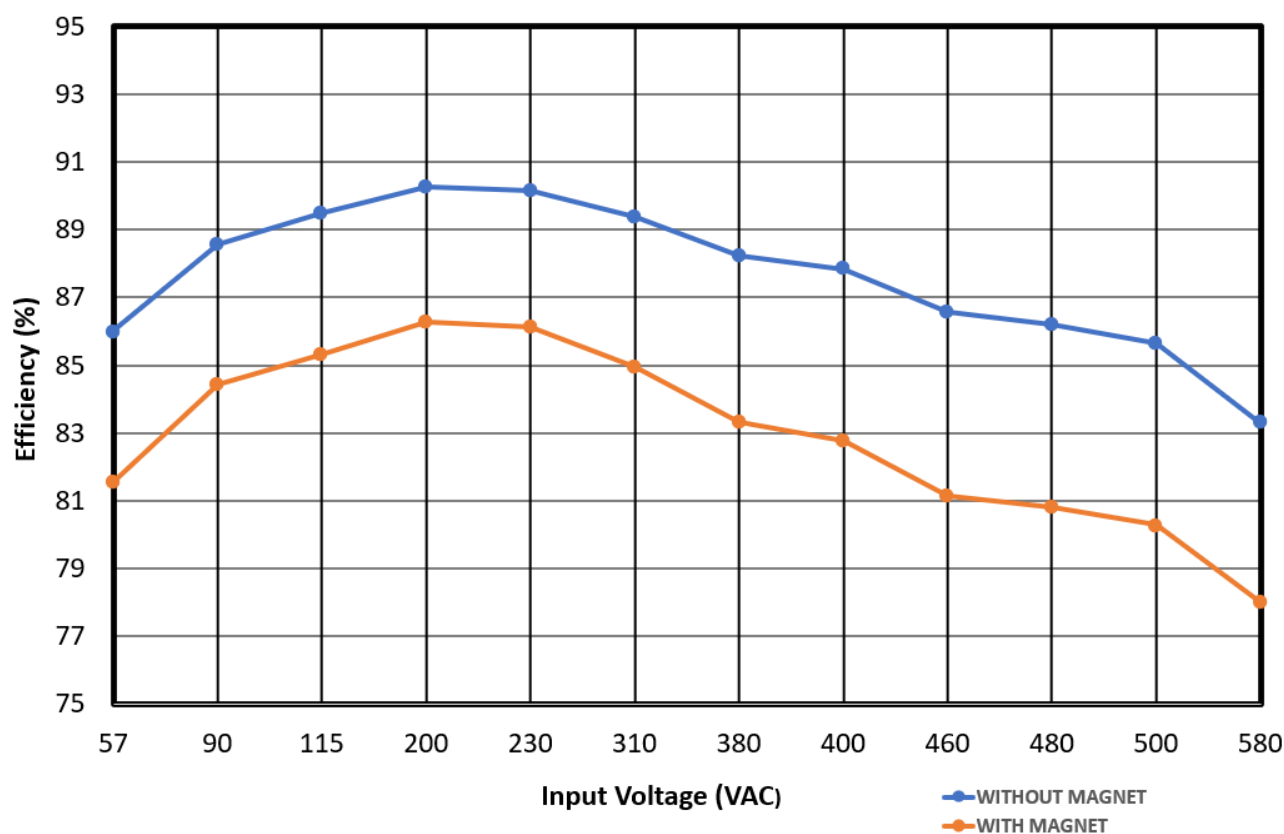


Figure 100 – Full-load Efficiency vs. Line, With and Without Magnetizing Interference

13.3 Efficiency vs. Load with External Magnetizing Interference

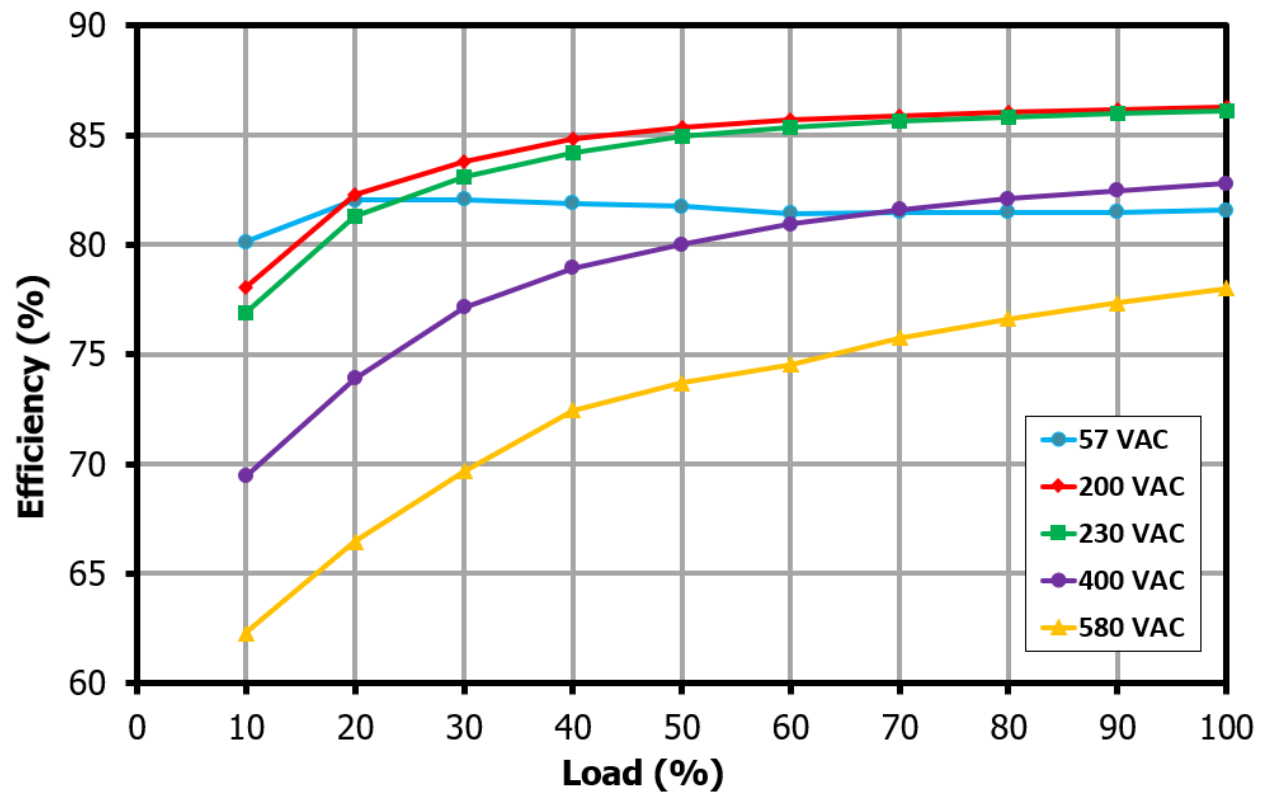


Figure 101 – Efficiency vs. Load, With External Magnetizing Interference

13.4 No-Load Input Power with External Magnetizing Interference

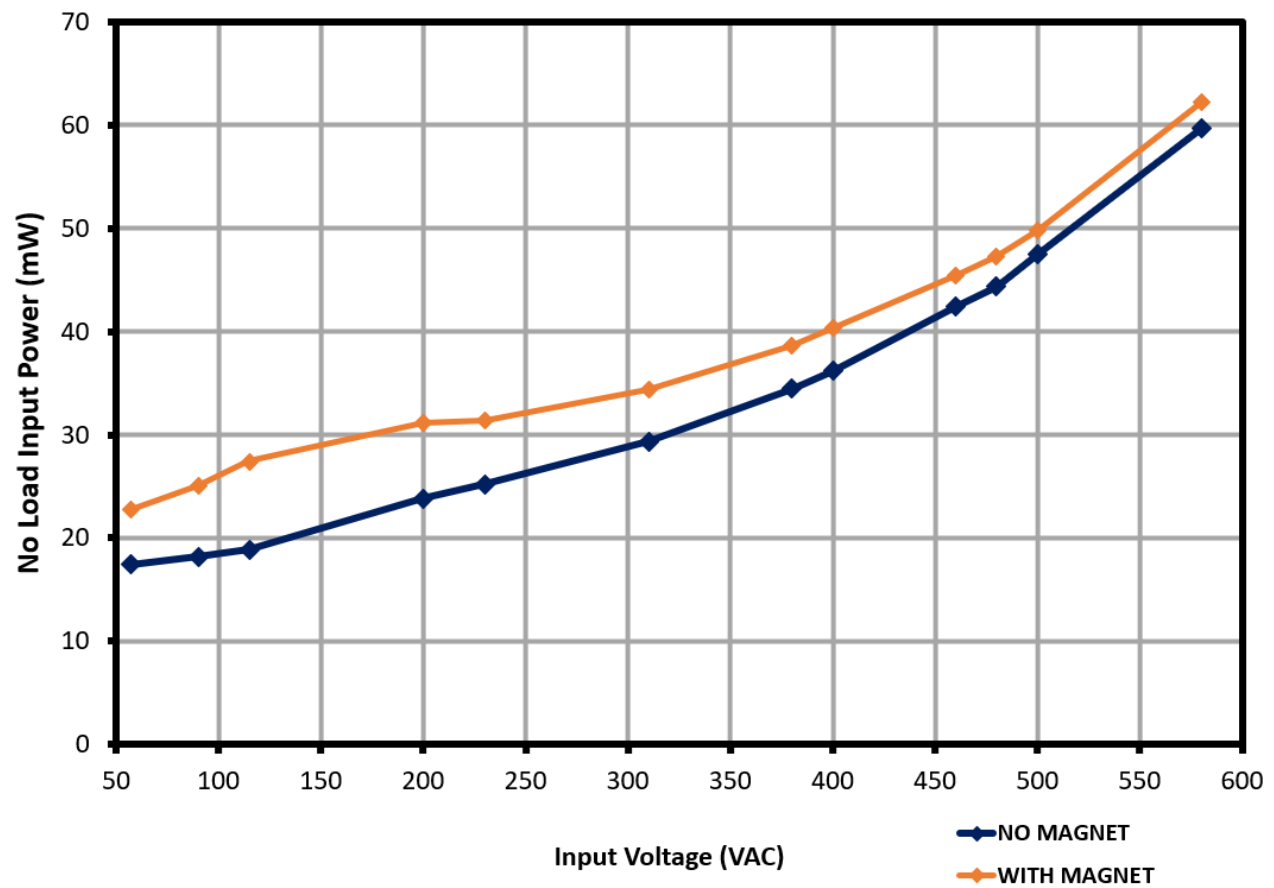


Figure 102 – No-Load Input Power vs. Input Line Voltage, With and Without Magnetizing Interference

13.5 Load Regulation with External Magnetizing Interference

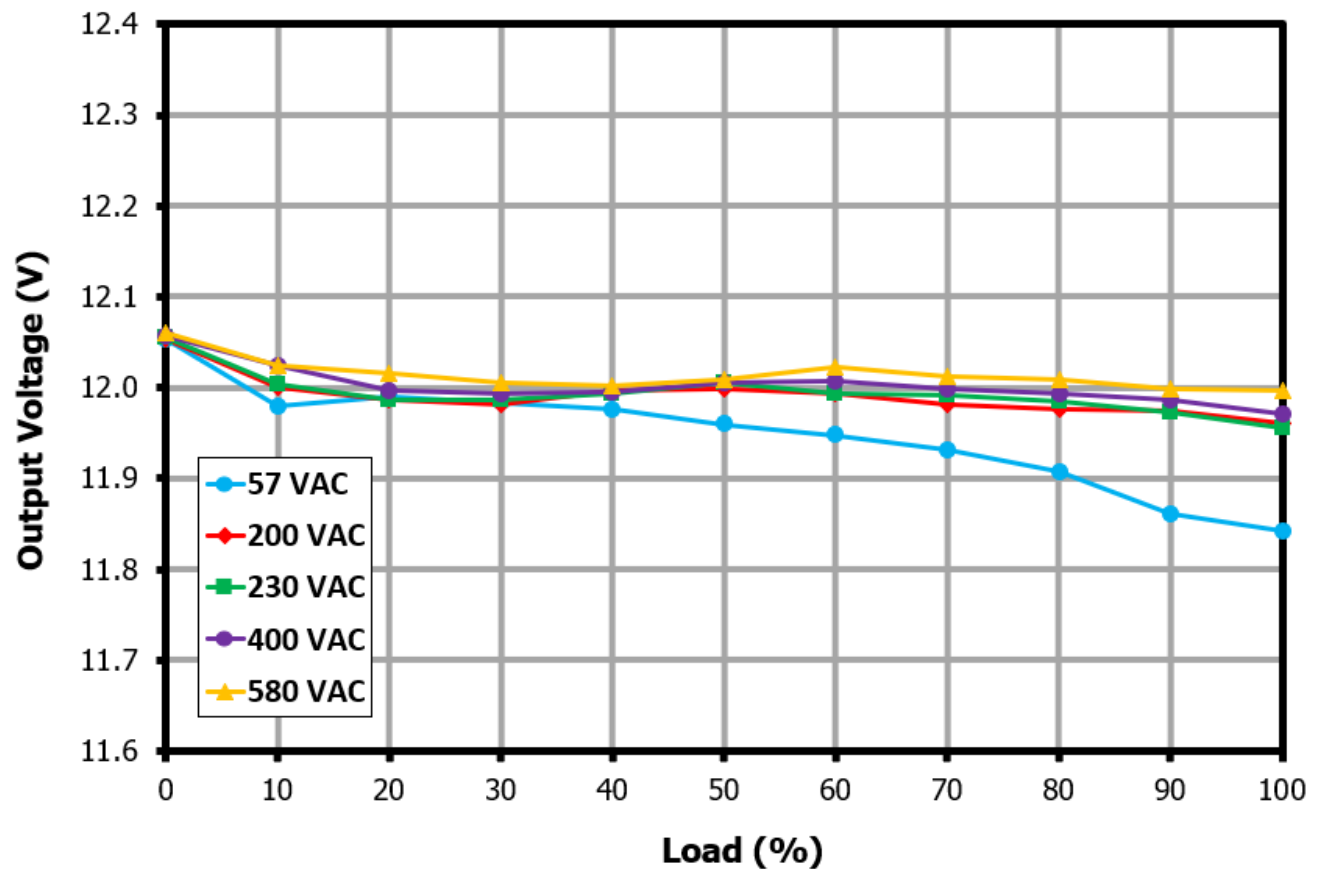


Figure 103 – Load Regulation with External Magnetizing Interference

13.6 Line Regulation with External Magnetizing Interference

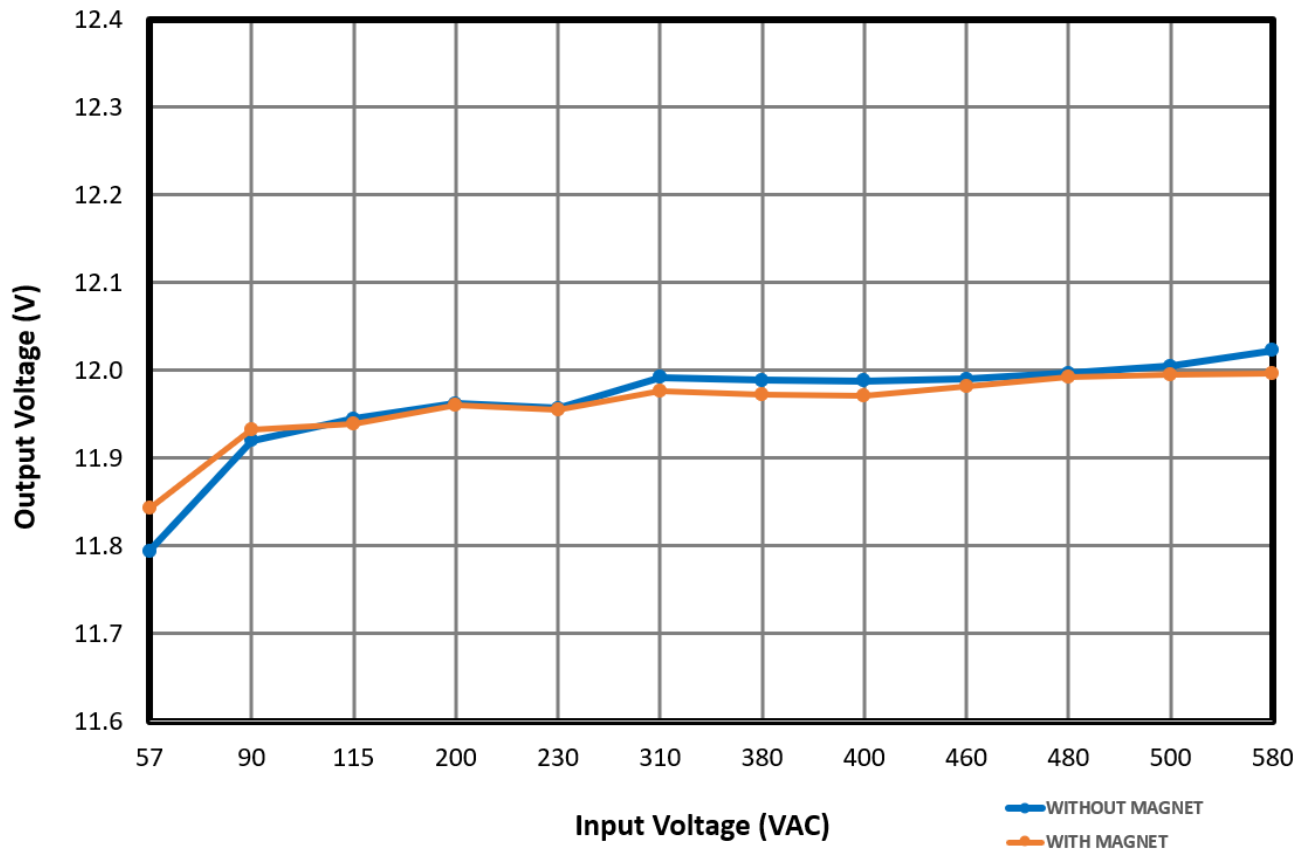


Figure 104 – Line Regulation, With and Without Magnetizing Interference, Full Load

13.7 Thermal Performance with External Magnetizing Interference

13.7.1 57 VAC, 12 W at 0 °C Ambient, With Magnet

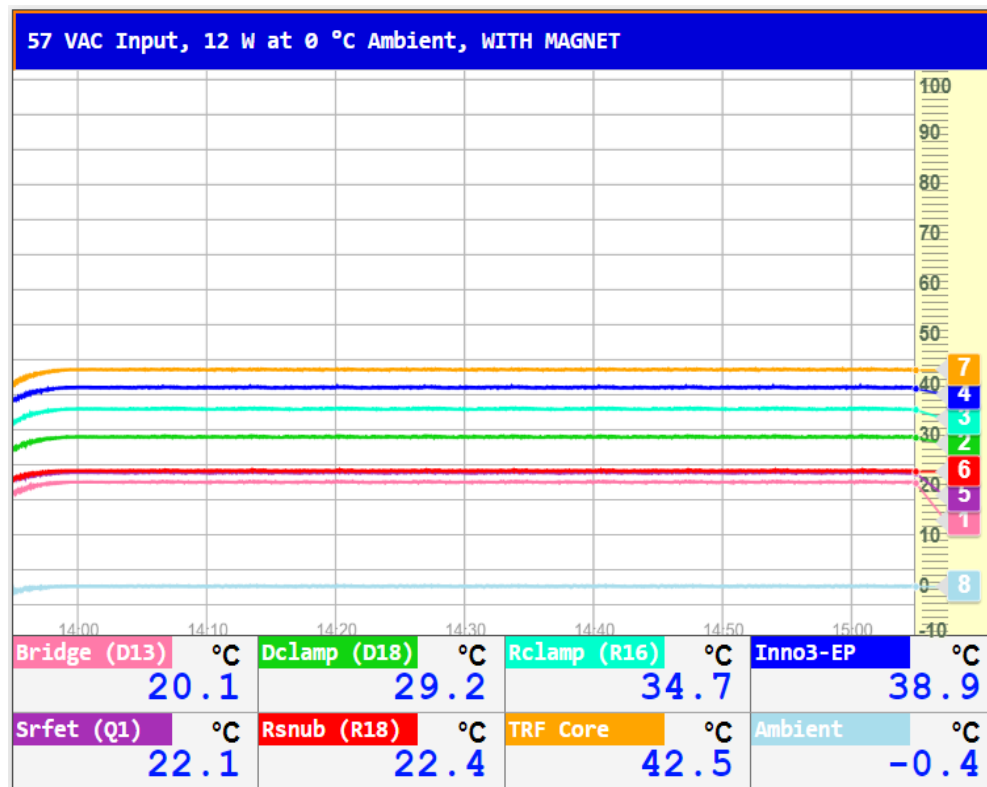


Figure 105 – Thermal Performance at 57 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	20.1
Primary Clamp Diode (D18)	29.2
Primary Clamp Series Resistor (R16)	34.7
InnoSwitch3-EP (U1)	38.9
SR FET (Q1)	22.1
Secondary Rectifier Snubber Resistor (R18)	22.4
Transformer Core (T1)	42.5
Ambient	-0.4

Table 18 – Temperature Measurement of Critical Components at 0 °C, With Magnet

13.7.2 580 VAC, 12 W at 0 °C Ambient, With Magnet

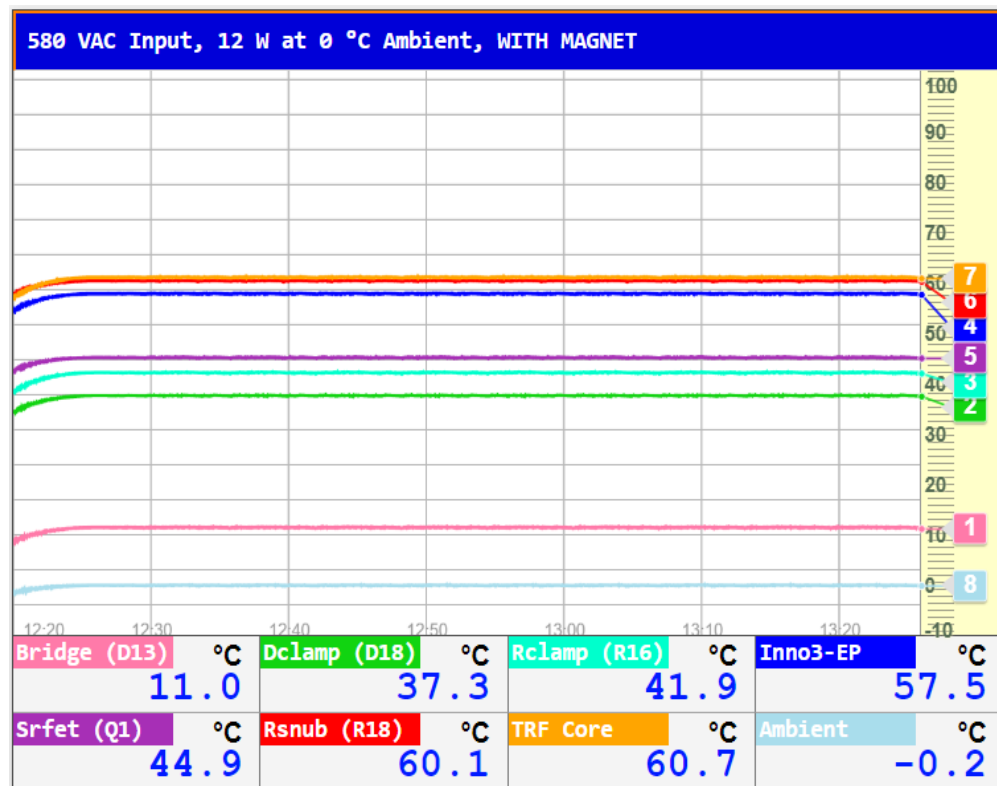


Figure 106 – Thermal Performance at 580 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	11.0
Primary Clamp Diode (D18)	37.3
Primary Clamp Series Resistor (R16)	41.9
InnoSwitch3-EP (U1)	57.5
SR FET (Q1)	44.9
Secondary Rectifier Snubber Resistor (R18)	60.1
Transformer Core (T1)	60.7
Ambient	-0.2

Table 19 – Temperature Measurement of Critical Components at 0 °C, With Magnet

13.7.3 57 VAC, 12 W at 25 °C Ambient, With Magnet

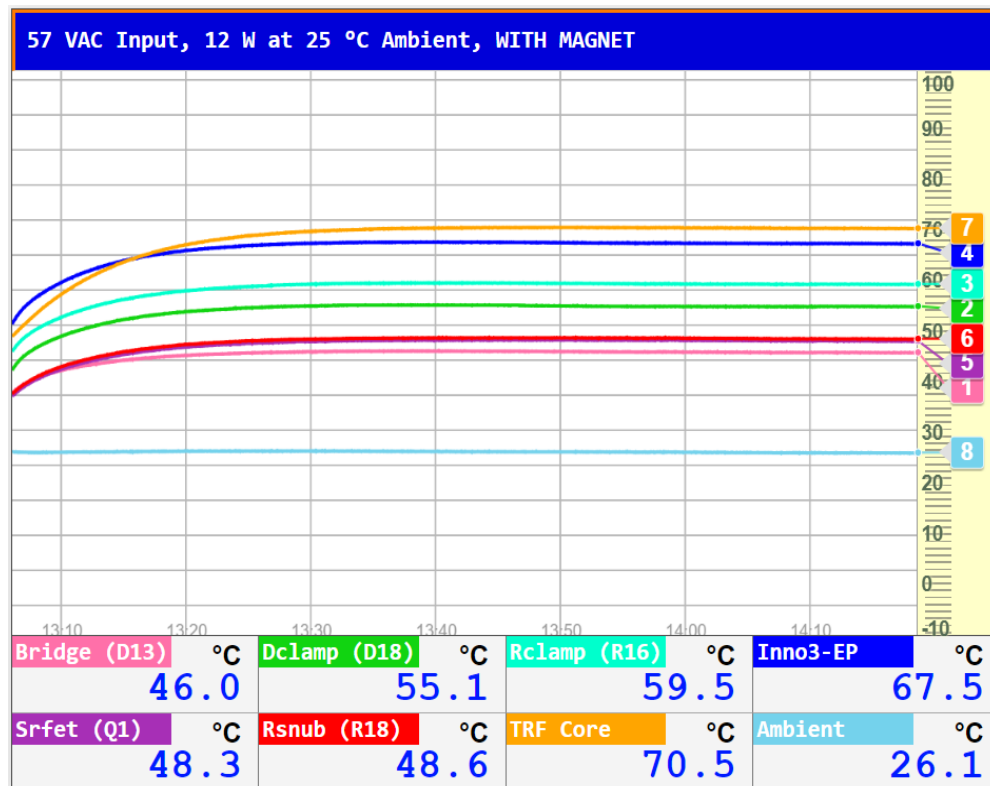


Figure 107 – Thermal Performance at 57 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	46.0
Primary Clamp Diode (D18)	55.1
Primary Clamp Series Resistor (R16)	59.5
InnoSwitch3-EP (U1)	67.5
SR FET (Q1)	48.3
Secondary Rectifier Snubber Resistor (R18)	48.6
Transformer Core (T1)	70.5
Ambient	26.1

Table 20 – Temperature Measurement of Critical Components at 25 °C, With Magnet

13.7.4 580 VAC, 12 W at 25 °C Ambient, With Magnet

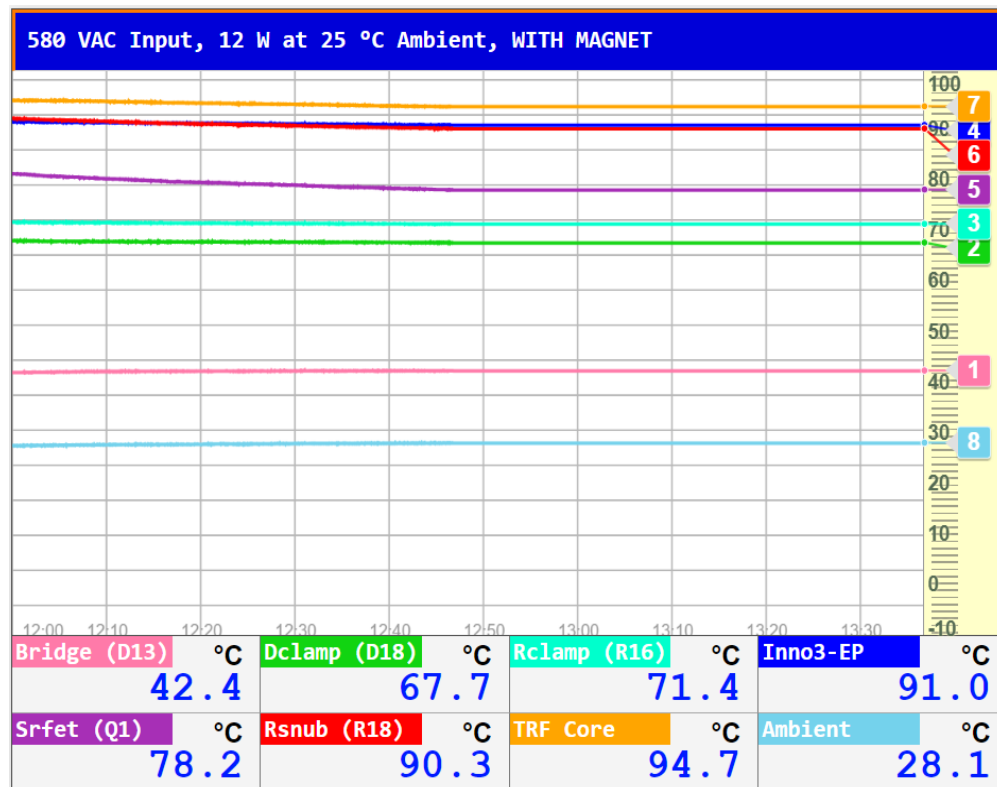


Figure 108 – Thermal Performance at 580 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	42.4
Primary Clamp Diode (D18)	67.7
Primary Clamp Series Resistor (R16)	71.4
InnoSwitch3-EP (U1)	91.0
SR FET (Q1)	78.2
Secondary Rectifier Snubber Resistor (R18)	90.3
Transformer Core (T1)	94.7
Ambient	28.1

Table 21 – Temperature Measurement of Critical Components at 25 °C, With Magnet

13.7.5 57 VAC, 12 W at 40 °C Ambient, With Magnet

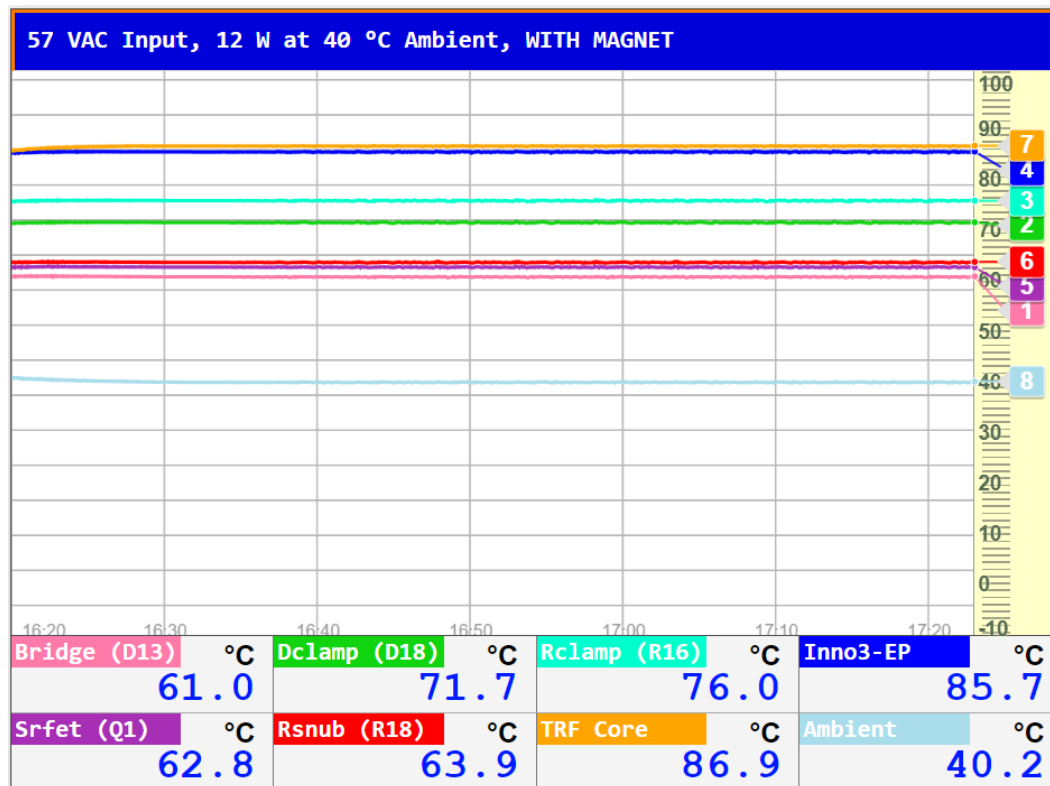


Figure 109 – Thermal Performance at 57 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	61.0
Primary Clamp Diode (D18)	71.7
Primary Clamp Series Resistor (R16)	76.0
InnoSwitch3-EP (U1)	85.7
SR FET (Q1)	62.8
Secondary Rectifier Snubber Resistor (R18)	63.9
Transformer Core (T1)	86.9
Ambient	40.2

Table 22 – Temperature Measurement of Critical Components at 40 °C, With Magnet

13.7.6 580 VAC, 12 W at 40 °C Ambient, With Magnet

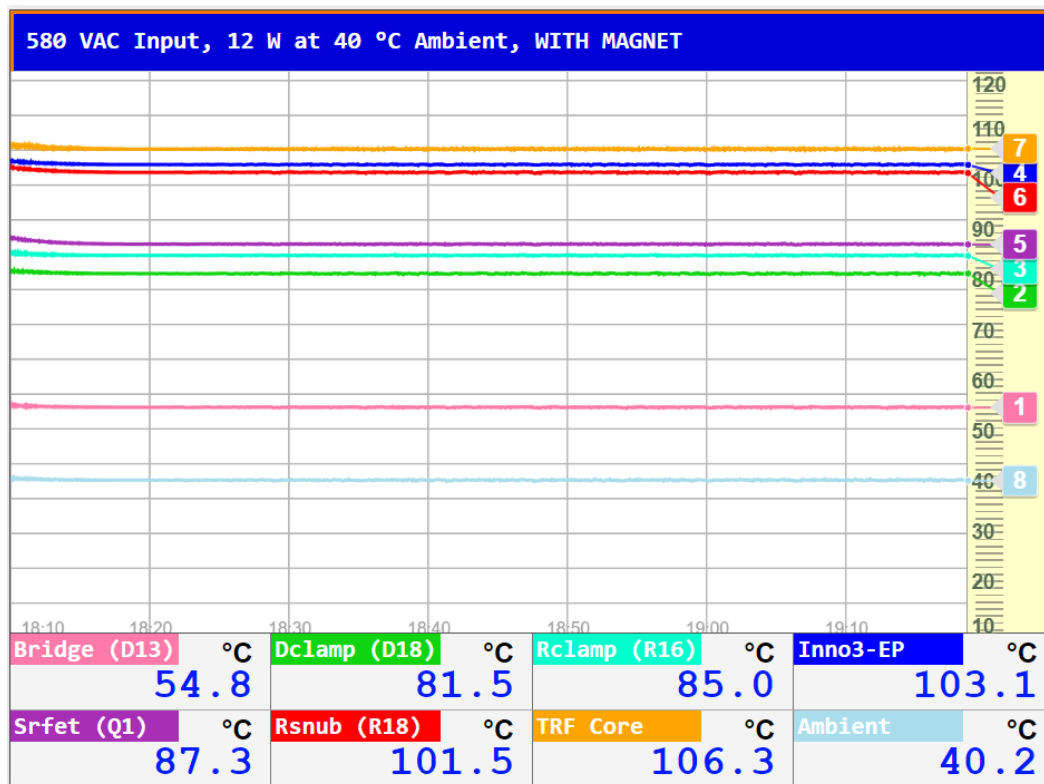


Figure 110 – Thermal Performance at 580 VAC Input, With Magnet

Component	Temperature (°C)
Bridge Rectifier Diode (D13)	54.8
Primary Clamp Diode (D18)	81.5
Primary Clamp Series Resistor (R16)	85.0
InnoSwitch3-EP (U1)	103.1
SR FET (Q1)	87.3
Secondary Rectifier Snubber Resistor (R18)	101.5
Transformer Core (T1)	106.3
Ambient	40.2

Table 23 – Temperature Measurement of Critical Components at 40 °C, With Magnet

13.8 Waveforms with External Magnetizing Interference

13.8.1 Output Voltage Start-up Waveforms at Room Temperature

The input voltage at CH1 is measured across one L-N of the 3-phase, 4-wire input line.

13.8.1.1 CC Load

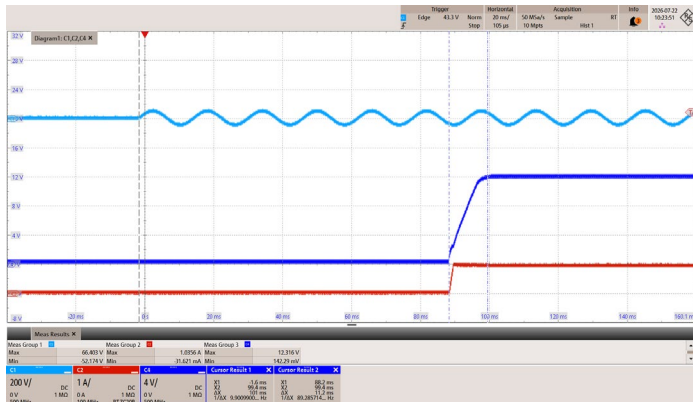


Figure 111 – 57 VAC, 60 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.3 V

Output Voltage, Rise Time = 11.2 ms

Start-up Time = 101 ms

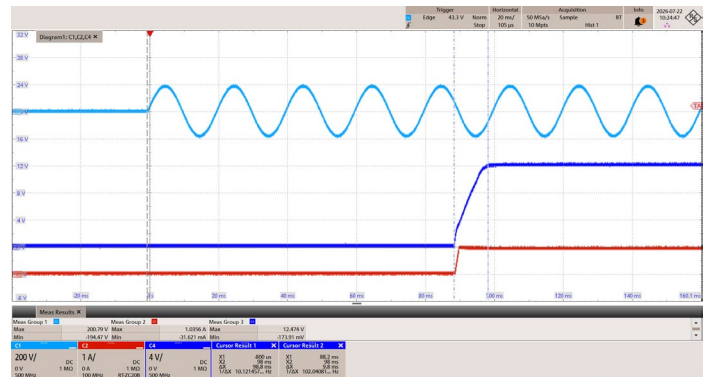


Figure 112 – 230 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 9.8 ms

Start-up Time = 98.8 ms

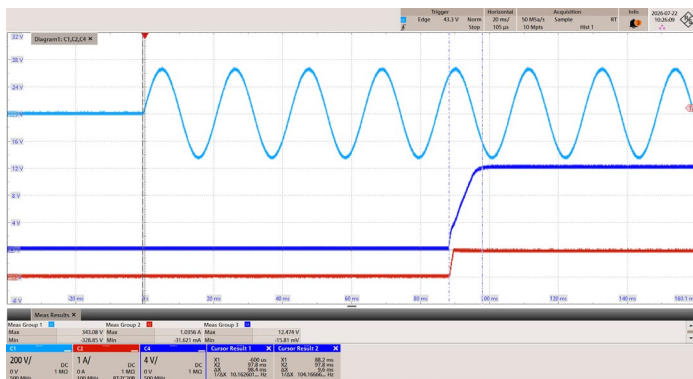


Figure 113 – 400 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 9.6 ms

Start-up Time = 98.4 ms

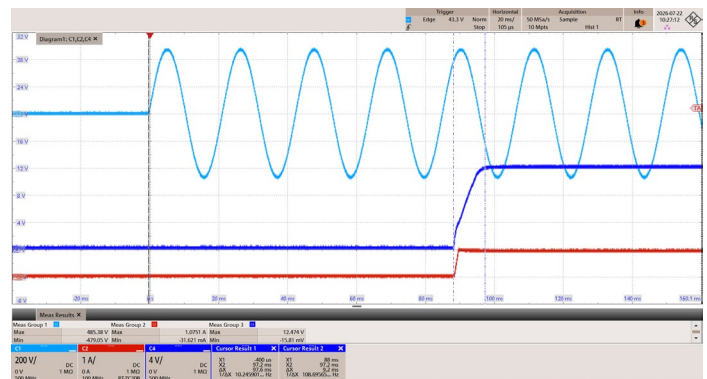


Figure 114 – 580 VAC, 50 Hz, $I_o = 1$ A

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

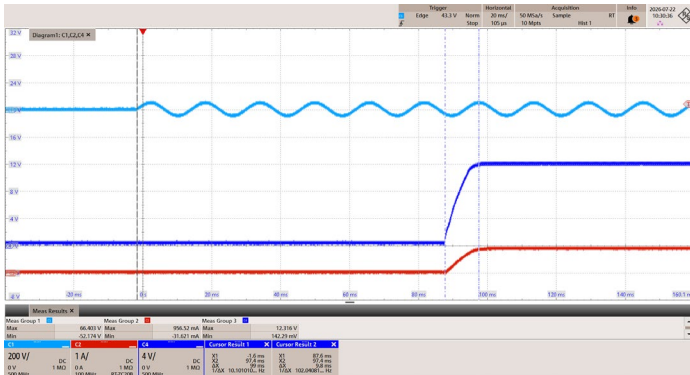
CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 9.2 ms

Start-up Time = 97.6 ms

13.8.1.2 CR Load

Figure 115 – 57 VAC, 60 Hz, $R_o = 12$ W (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

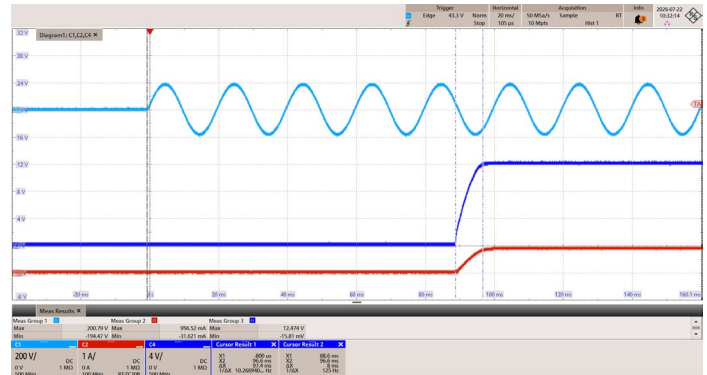
CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.3 V

Output Voltage, Rise Time = 9.8 ms

Start-up Time = 99 ms

Figure 116 – 230 VAC, 50 Hz, $R_o = 12$ W (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

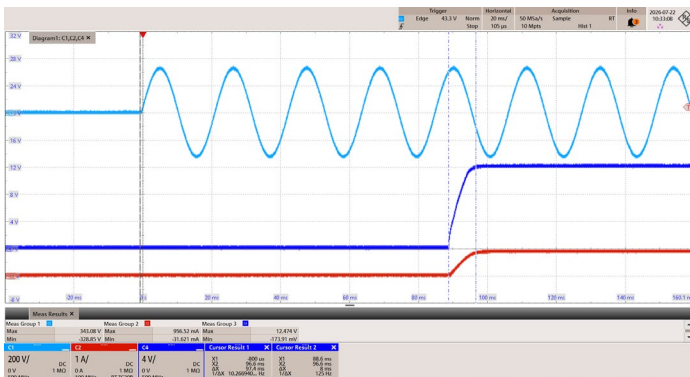
CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 8 ms

Start-up Time = 97.4 ms

Figure 117 – 400 VAC, 50 Hz, $R_o = 12$ W (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

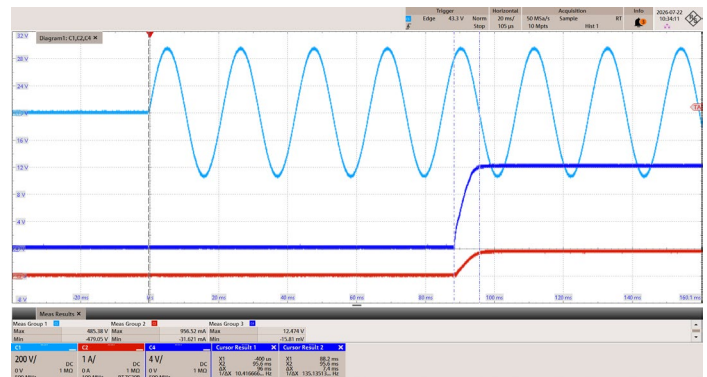
CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 8 ms

Start-up Time = 97.4 ms

Figure 118 – 580 VAC, 50 Hz, $R_o = 12$ W (Full-Load, CR)

CH1: Input Voltage: 200 V / div., 20 ms / div

CH2: Output Current: 1 A / div., 20 ms / div

CH4: Output Voltage: 4 V / div., 20 ms / div

Output Voltage, Max. = 12.5 V

Output Voltage, Rise Time = 7.4 ms

Start-up Time = 96 ms

13.8.2 Load Transient Response with External Magnetizing Interference

13.8.2.1 0 – 100% Load Step

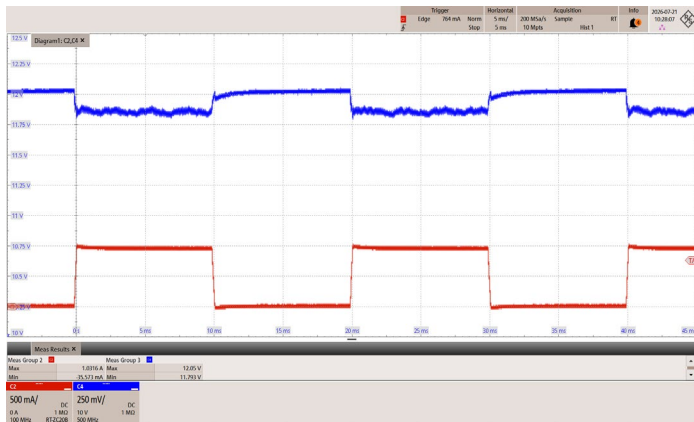


Figure 119 – 57 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step

CH2: Output Current: 500 mA / div, 5 ms / div

CH4: Output Voltage: 250 mV / div, 5 ms / div

V_{MAX} : 12.1 V

V_{MIN} : 11.8 V

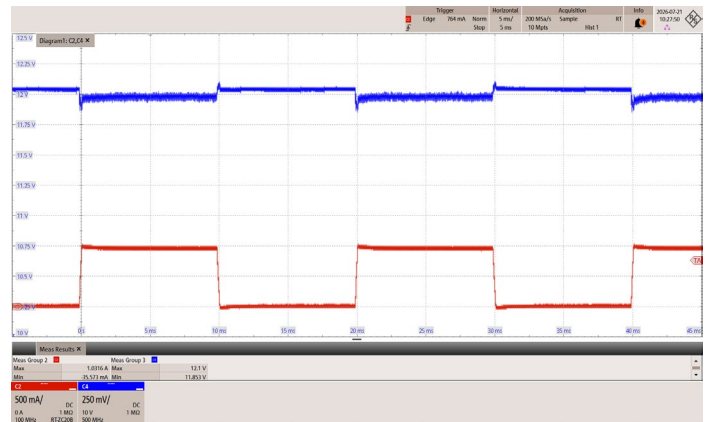


Figure 120 – 230 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step

CH2: Output Current: 500 mA / div, 5 ms / div

CH4: Output Voltage: 250 mV / div, 5 ms / div

V_{MAX} : 12.1 V

V_{MIN} : 11.9 V

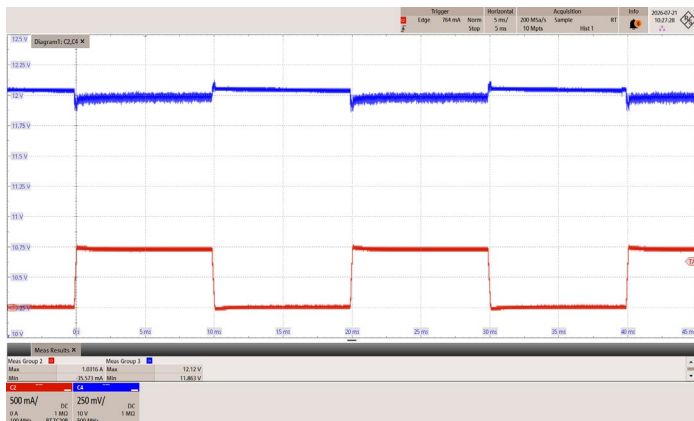


Figure 121 – 400 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step

CH2: Output Current: 500 mA / div, 5 ms / div

CH4: Output Voltage: 250 mV / div, 5 ms / div

V_{MAX} : 12.1 V

V_{MIN} : 11.9 V

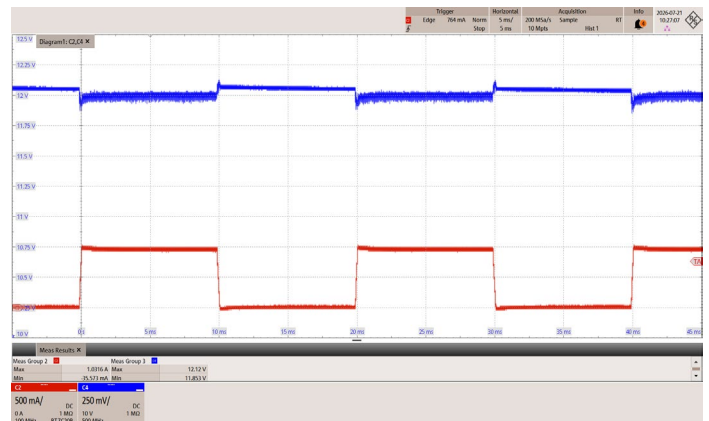


Figure 122 – 580 VAC; $I_o = 0\text{ A} - 1\text{ A}$ (0-100%) Load Step

CH2: Output Current: 500 mA / div, 5 ms / div

CH4: Output Voltage: 250 mV / div, 5 ms / div

V_{MAX} : 12.1 V

V_{MIN} : 11.9 V

13.8.2.2 50% – 100% Load Step

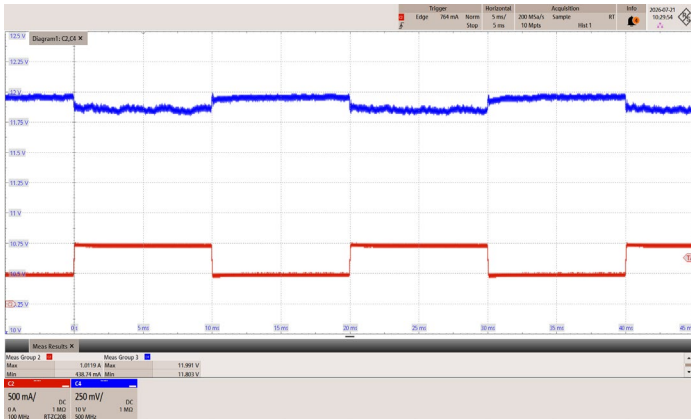


Figure 123 – 57 VAC; $I_o = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.0 V
 V_{MIN} : 11.8 V

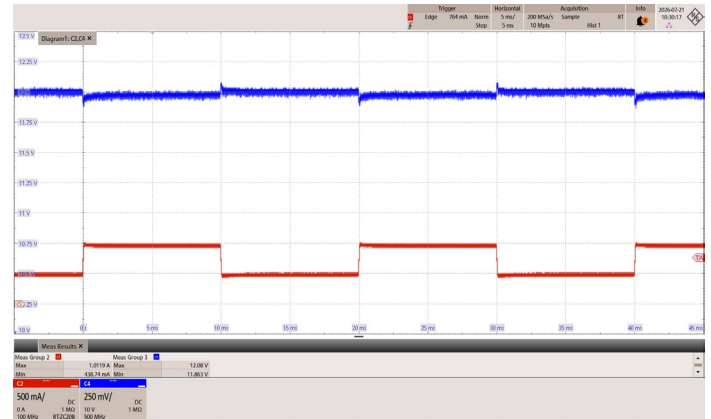


Figure 124 – 230 VAC; $I_o = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

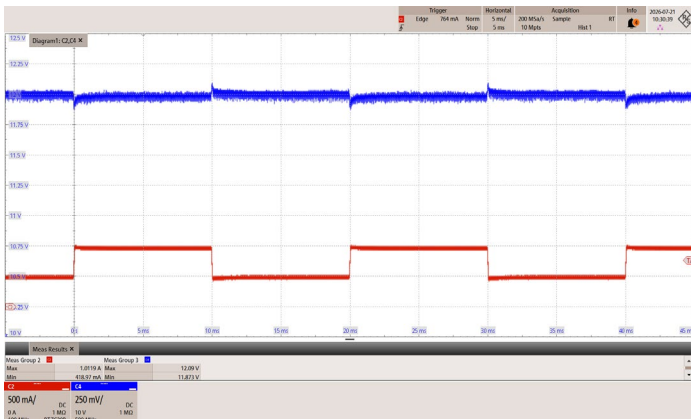


Figure 125 – 400 VAC; $I_o = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

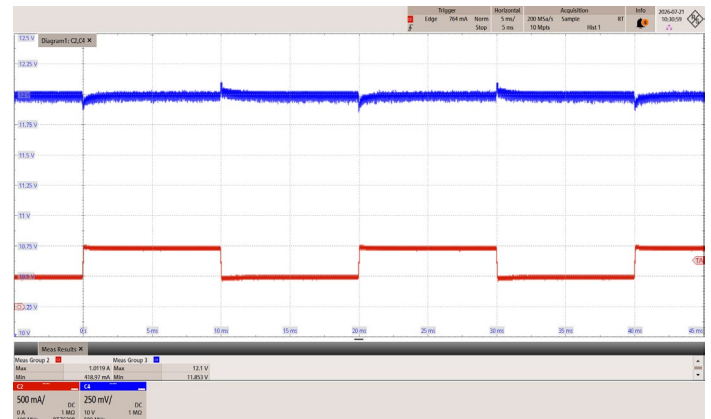


Figure 126 – 580 VAC; $I_o = 0.5\text{ A} - 1\text{ A}$ (50-100%) Load Step
 CH2: Output Current: 500 mA / div, 5 ms / div
 CH4: Output Voltage: 250 mV / div, 5 ms / div
 V_{MAX} : 12.1 V
 V_{MIN} : 11.9 V

13.8.3 InnoSwitch Switching Waveforms with External Magnetizing Interference

13.8.3.1 Drain Voltage and Current at Start-up (100% Load)

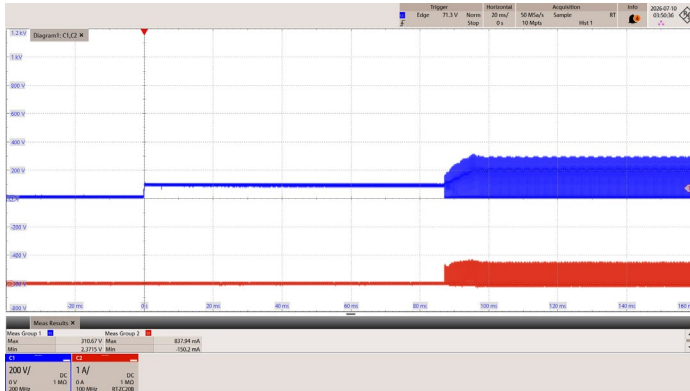


Figure 127 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 311 V

Drain current, Max. = 0.838 A

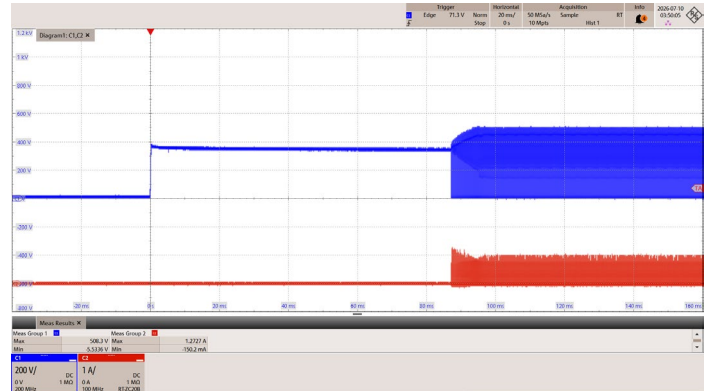


Figure 128 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 508 V

Drain current, Max. = 1.27 A

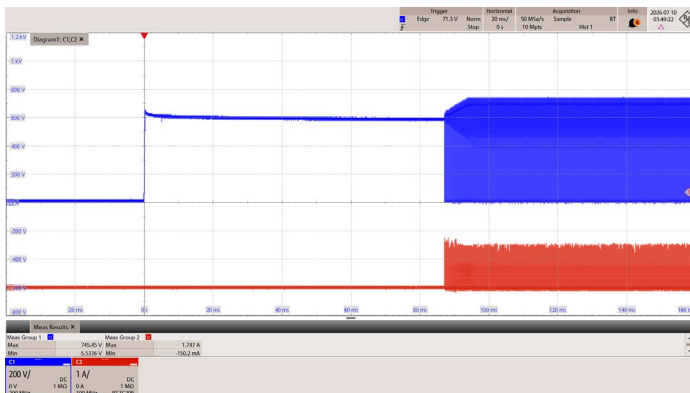


Figure 129 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 745 V

Drain current, Max. = 1.75 A

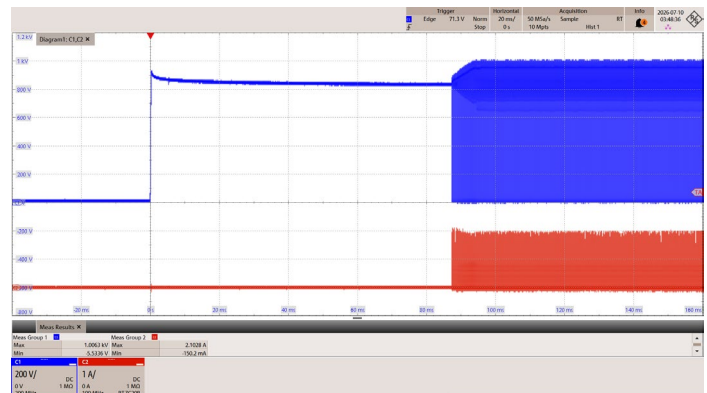


Figure 130 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

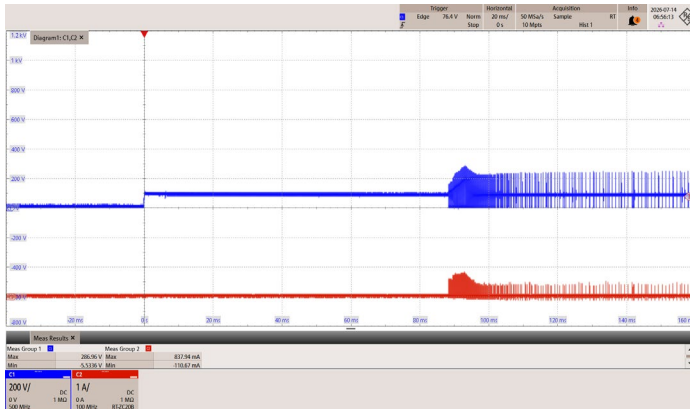
CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 1006 V

Drain current, Max. = 2.10 A

13.8.3.2 Drain Voltage and Current at Start-up (0% Load)

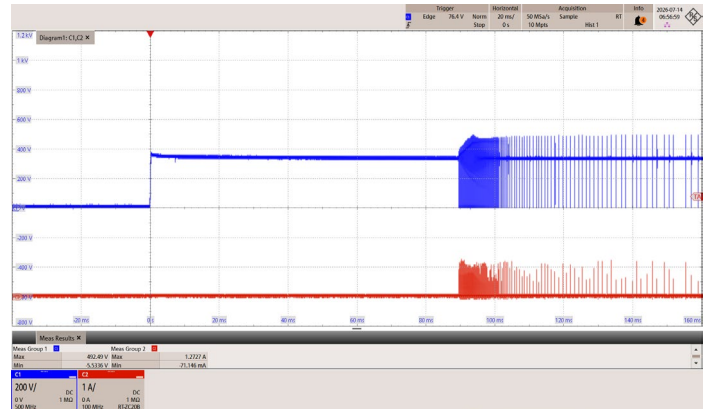
**Figure 131** – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 287 V

Drain current, Max. = 0.838 A

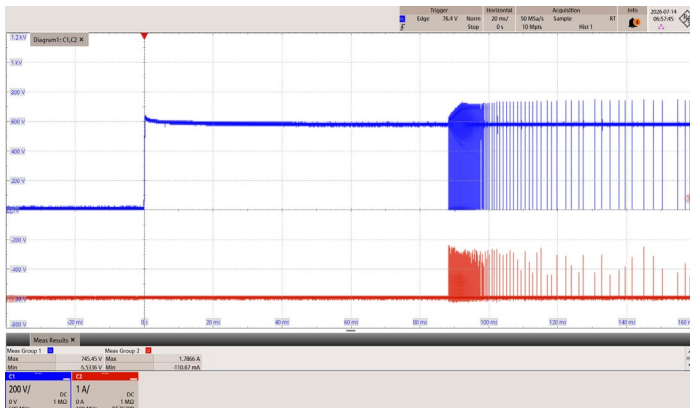
**Figure 132** – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 492 V

Drain current, Max. = 1.27 A

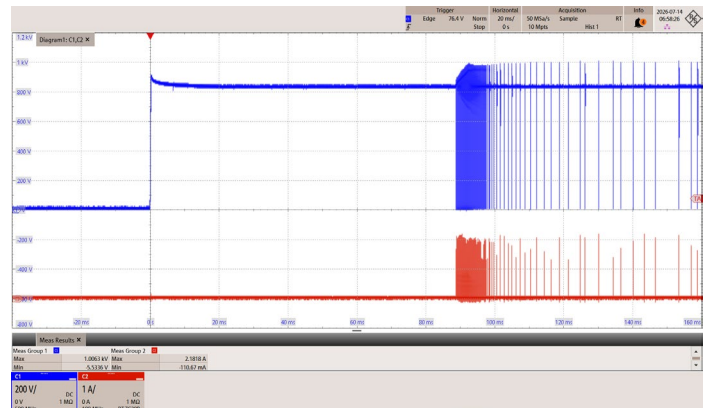
**Figure 133** – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 745 V

Drain current, Max. = 1.79 A

**Figure 134** – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 ms / div

CH2: Drain Current: 1 A / div, 20 ms / div

Drain voltage, Max. = 1006 V

Drain current, Max. = 2.18 A

13.8.3.3 Drain Voltage and Current at Normal Operation (100% Load)

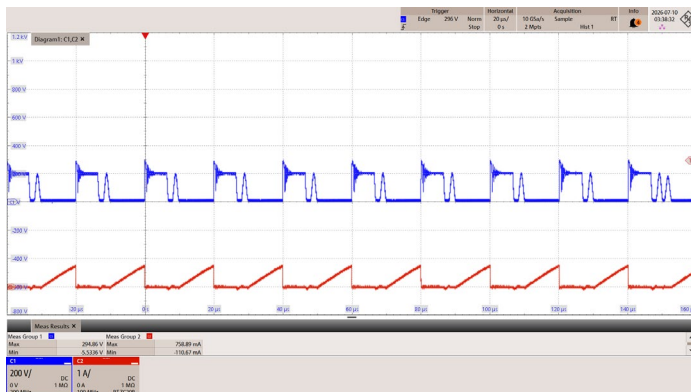


Figure 135 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 295 V

Drain current, Max. = 0.759 A

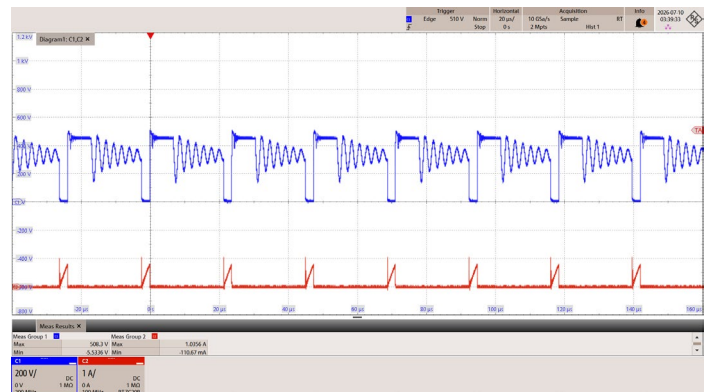


Figure 136 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 508 V

Drain current, Max. = 1.04 A

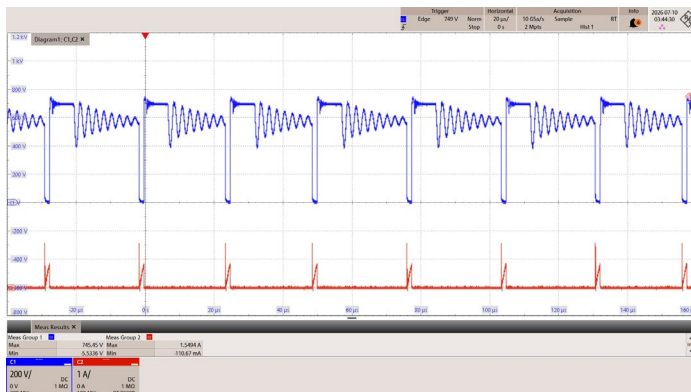


Figure 137 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 745 V

Drain current, Max. = 1.55 A

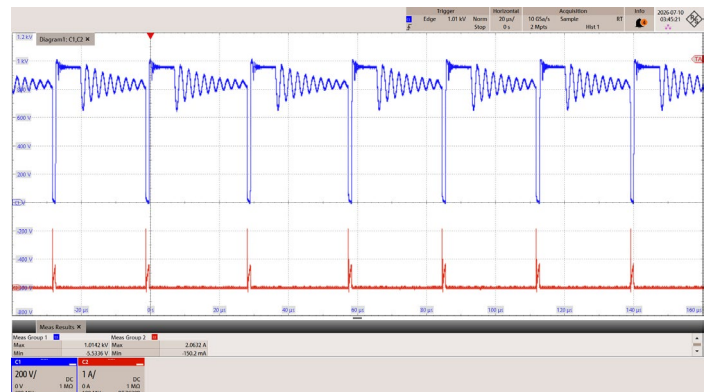


Figure 138 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

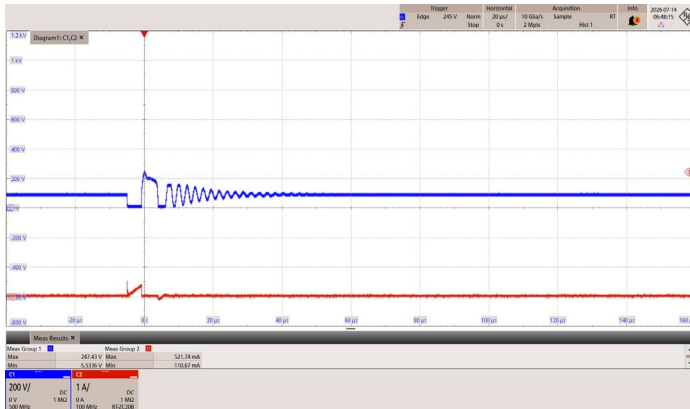
CH1: Drain Voltage: 200 V / div, 20 μ s / div

CH2: Drain Current: 1 A / div, 20 μ s / div

Drain voltage, Max. = 1014 V

Drain current, Max. = 2.06 A

13.8.3.4 Drain Voltage and Current at Normal Operation (0% Load)

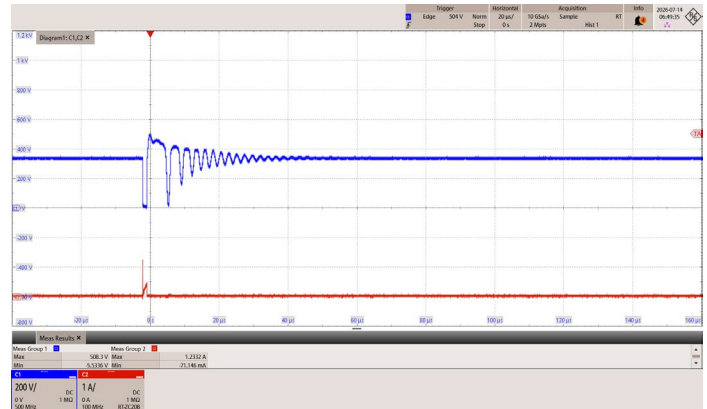
**Figure 139** – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μs / div

CH2: Drain Current: 1 A / div, 20 μs / div

Drain voltage, Max. = 247 V

Drain current, Max. = 0.522 A

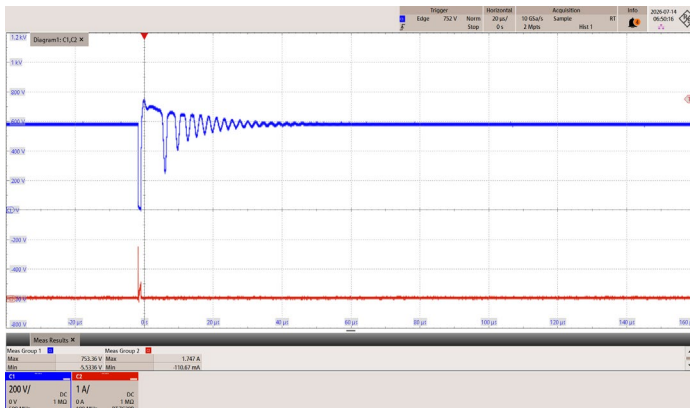
**Figure 140** – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μs / div

CH2: Drain Current: 1 A / div, 20 μs / div

Drain voltage, Max. = 508 V

Drain current, Max. = 1.23 A

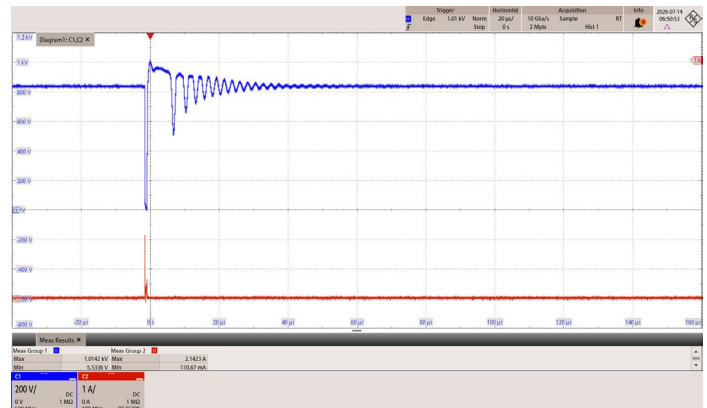
**Figure 141** – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μs / div

CH2: Drain Current: 1 A / div, 20 μs / div

Drain voltage, Max. = 753 V

Drain current, Max. = 1.75 A

**Figure 142** – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)

CH1: Drain Voltage: 200 V / div, 20 μs / div

CH2: Drain Current: 1 A / div, 20 μs / div

Drain voltage, Max. = 1014 V

Drain current, Max. = 2.14 A

13.8.4 SR FET Switching Waveforms with External Magnetizing Interference

13.8.4.1 SR FET Voltage and Current at Start-up (100% Load)

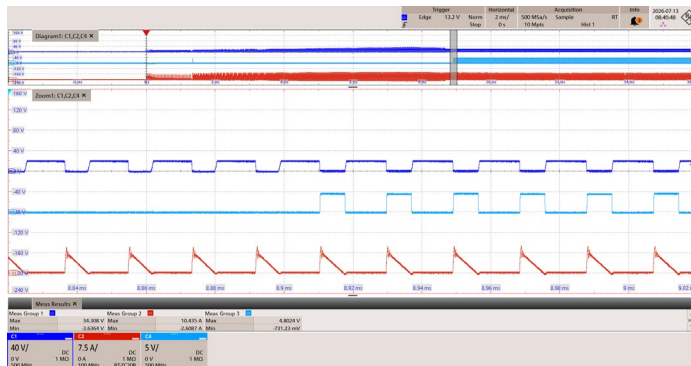


Figure 143 – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 34.3 V
 Secondary Winding Current, Max. = 10.4 A

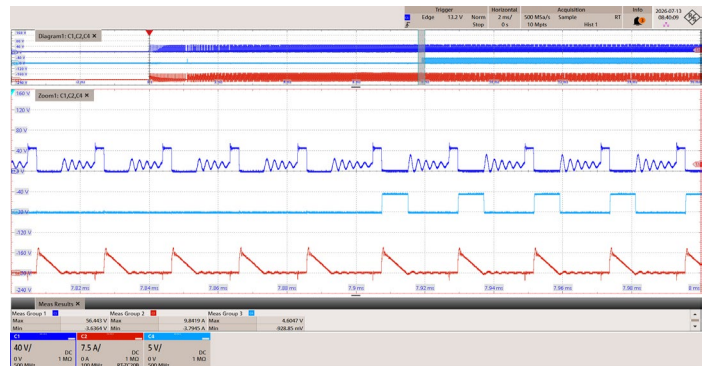


Figure 144 – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 56.4 V
 Secondary Winding Current, Max. = 9.84 A

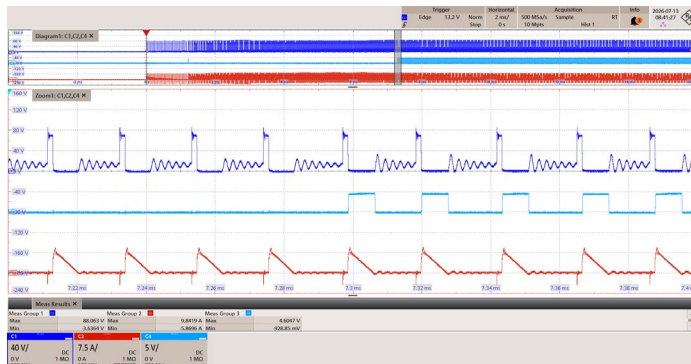


Figure 145 – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 88.1 V
 Secondary Winding Current, Max. = 9.84 A

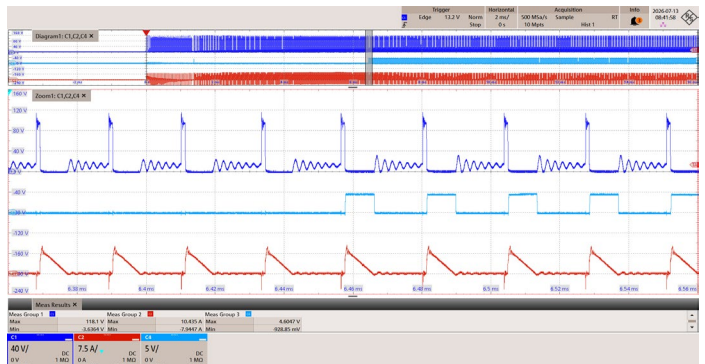


Figure 146 – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)

CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 118 V
 Secondary Winding Current, Max. = 10.4 A

13.8.4.2 SR FET Voltage and Current at Start-up (0% Load)

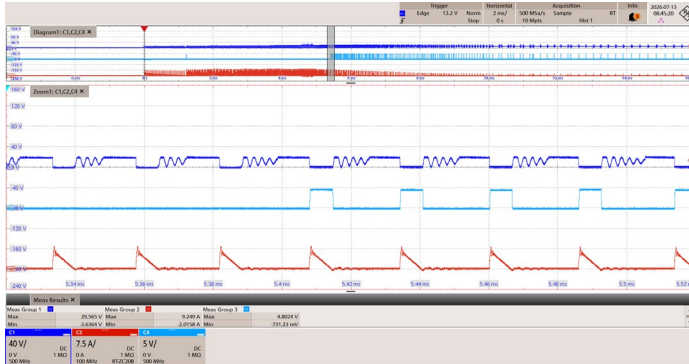


Figure 147 – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 29.6 V
 Secondary Winding Current, Max. = 9.25 A

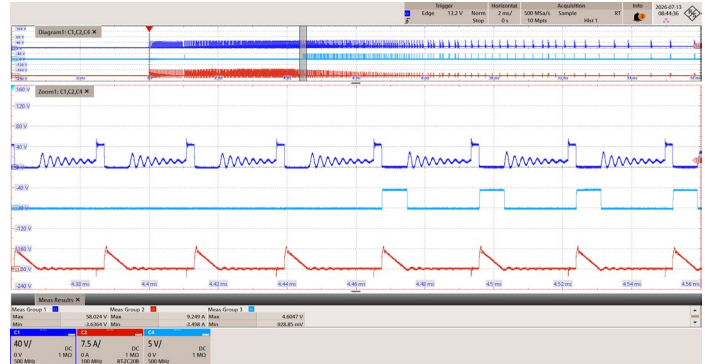


Figure 148 – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 58.0 V
 Secondary Winding Current, Max. = 9.25 A

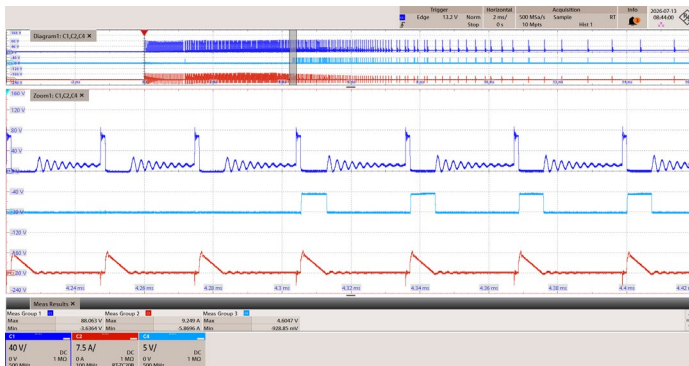


Figure 149 – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 88.1 V
 Secondary Winding Current, Max. = 9.25 A

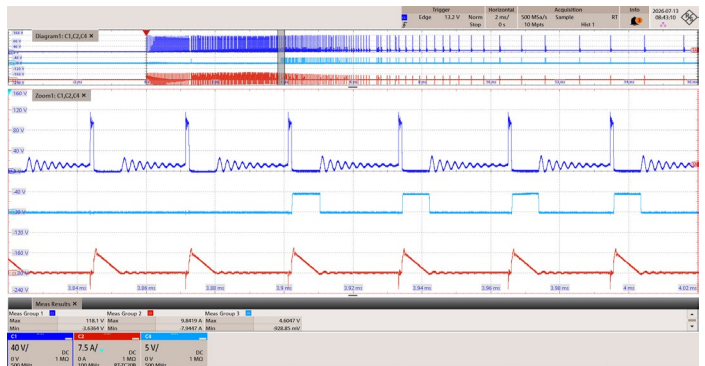
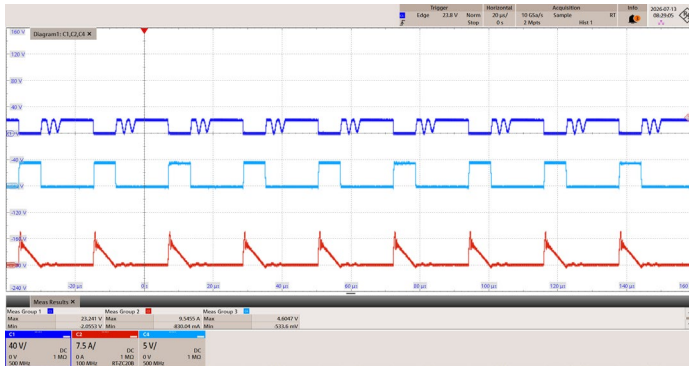


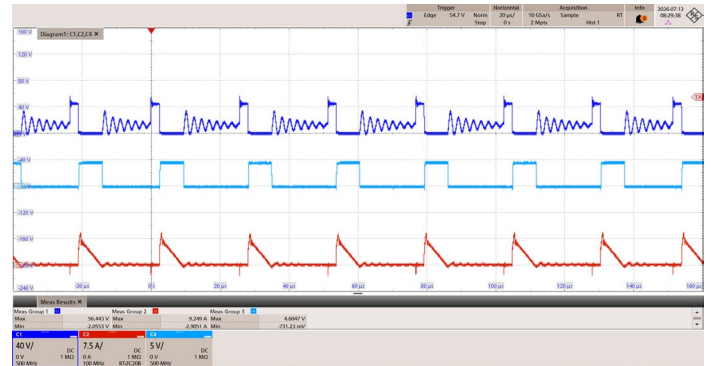
Figure 150 – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)
 CH1: Drain Voltage: 40 V / div, 2 ms / div
 CH2: Winding Current: 7.5 A / div, 2 ms / div
 CH4: Gate Voltage: 5 V / div, 2 ms / div
 Zoom: 20 μ s
 SR FET Drain Voltage, Max. = 118 V
 Secondary Winding Current, Max. = 9.84 A

13.8.4.3 SR FET Voltage and Current at Normal Operation (100% Load)

**Figure 151** – 57 VAC, 60 Hz, $I_o = 1$ A (Full-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

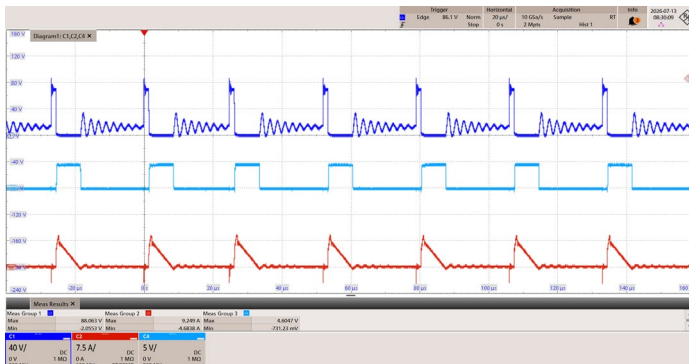
SR FET Drain Voltage, Max. = 23.2 V

Secondary Winding Current, Max. = 9.55 A

**Figure 152** – 230 VAC, 50 Hz, $I_o = 1$ A (Full-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

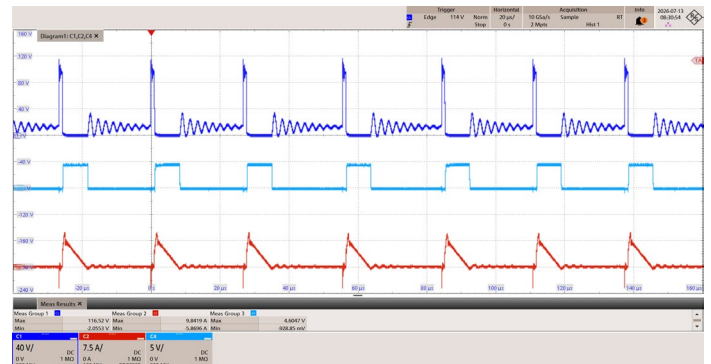
SR FET Drain Voltage, Max. = 56.4 V

Secondary Winding Current, Max. = 9.25 A

**Figure 153** – 400 VAC, 50 Hz, $I_o = 1$ A (Full-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

SR FET Drain Voltage, Max. = 88.1 V

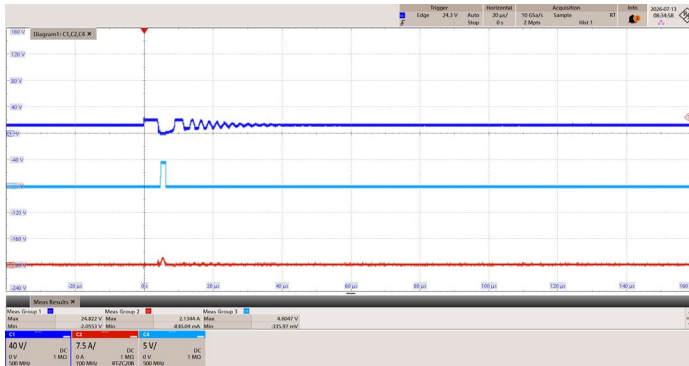
Secondary Winding Current, Max. = 9.25 A

**Figure 154** – 580 VAC, 50 Hz, $I_o = 1$ A (Full-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

SR FET Drain Voltage, Max. = 117 V

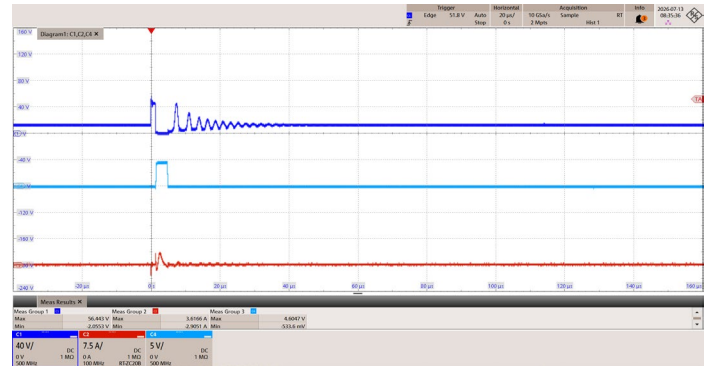
Secondary Winding Current, Max. = 9.84 A

13.8.4.4 SR FET Voltage and Current at Normal Operation (0% Load)

**Figure 155** – 57 VAC, 60 Hz, $I_o = 0$ A (No-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

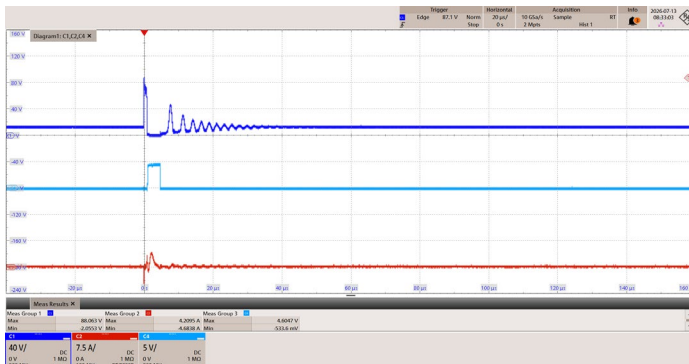
SR FET Drain Voltage, Max. = 24.8 V

Secondary Winding Current, Max. = 2.13 A

**Figure 156** – 230 VAC, 50 Hz, $I_o = 0$ A (No-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

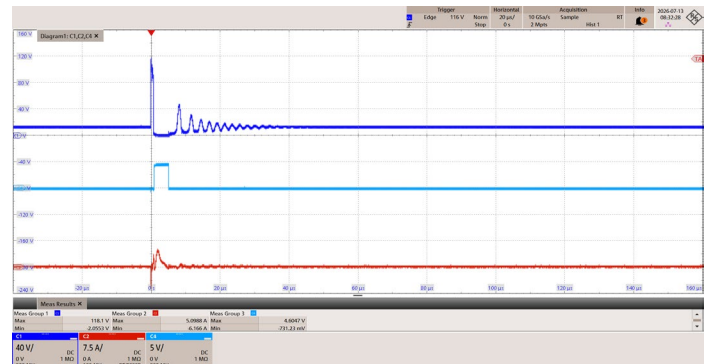
SR FET Drain Voltage, Max. = 56.4 V

Secondary Winding Current, Max. = 3.62 A

**Figure 157** – 400 VAC, 50 Hz, $I_o = 0$ A (No-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

SR FET Drain Voltage, Max. = 88.1 V

Secondary Winding Current, Max. = 4.21 A

**Figure 158** – 580 VAC, 50 Hz, $I_o = 0$ A (No-Load)CH1: Drain Voltage: 40 V / div, 20 μ s / divCH2: Winding Current: 7.5 A / div, 20 μ s / divCH4: Gate Voltage: 5 V / div, 20 μ s / div

SR FET Drain Voltage, Max. = 118 V

Secondary Winding Current, Max. = 5.10 A

13.9 Conducted EMI with External Magnetizing Interference

13.9.1 Neutral

13.9.1.1 VIN: 115 VAC

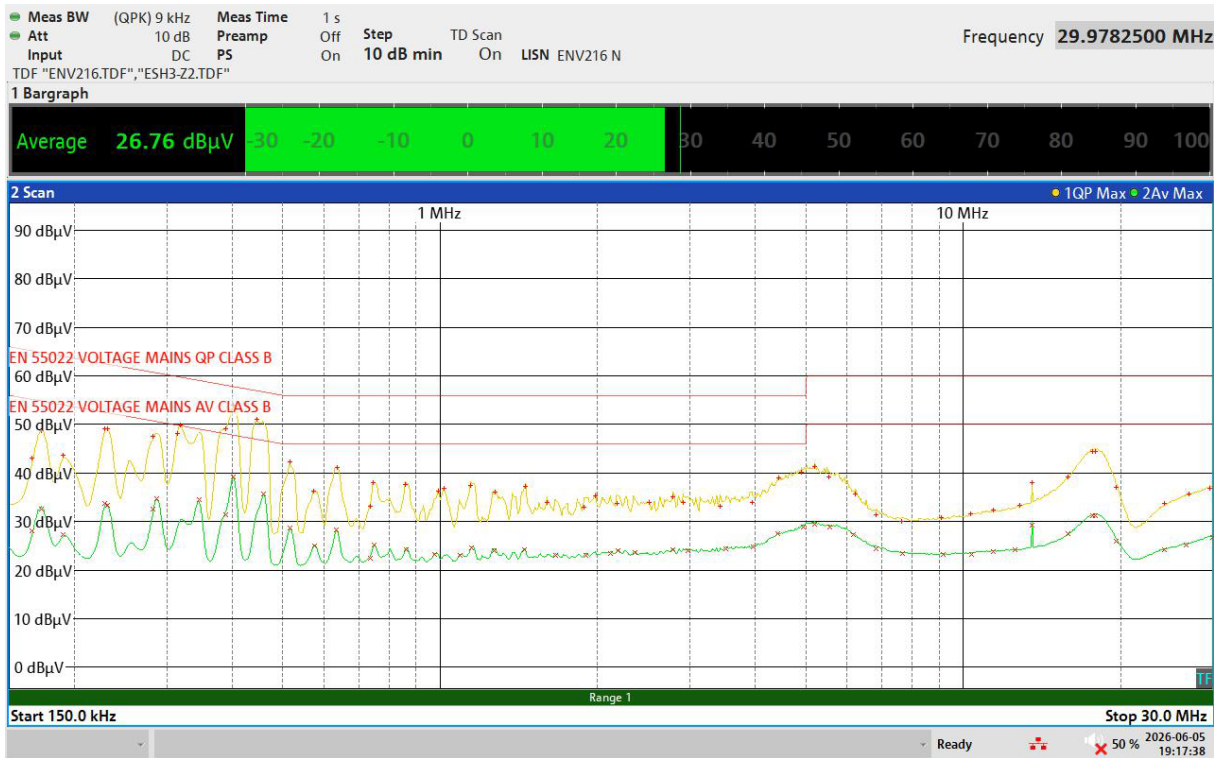


Figure 159 – Floating Ground EMI at 115 VAC b/w Input Lines A and B, Neutral

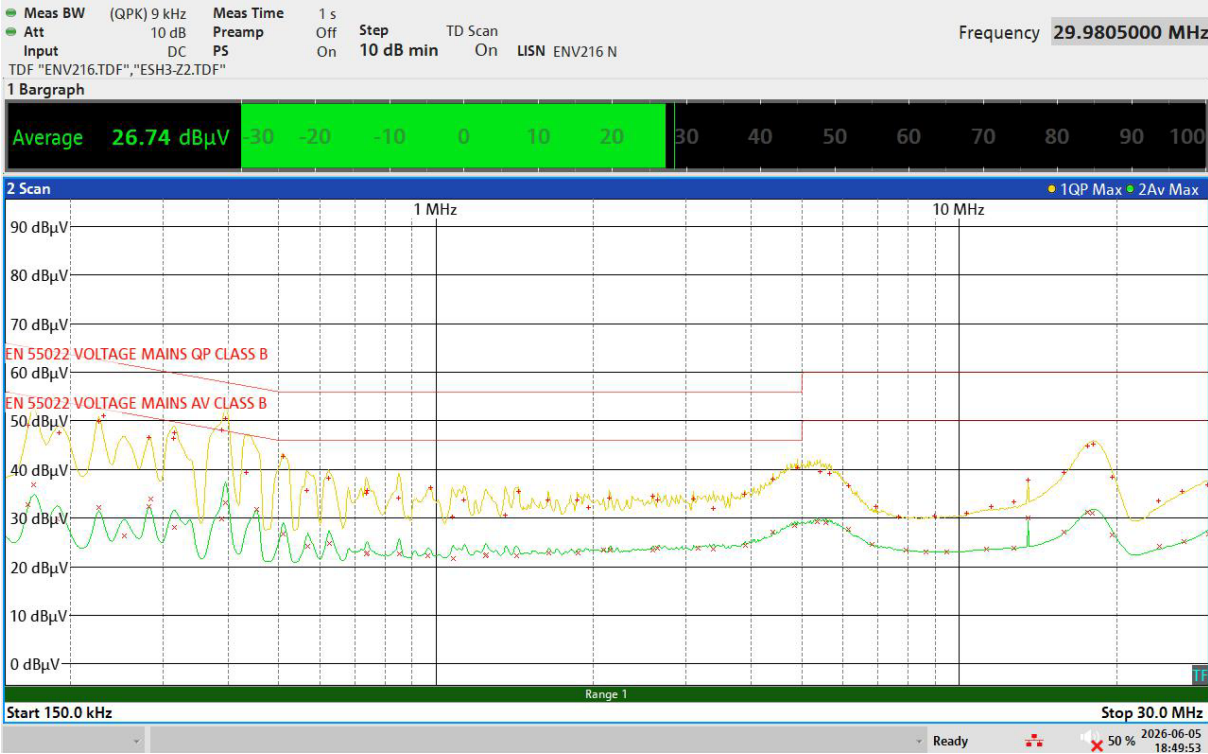


Figure 160 – Floating Ground EMI at 115 VAC b/w Input Lines B and C, Neutral

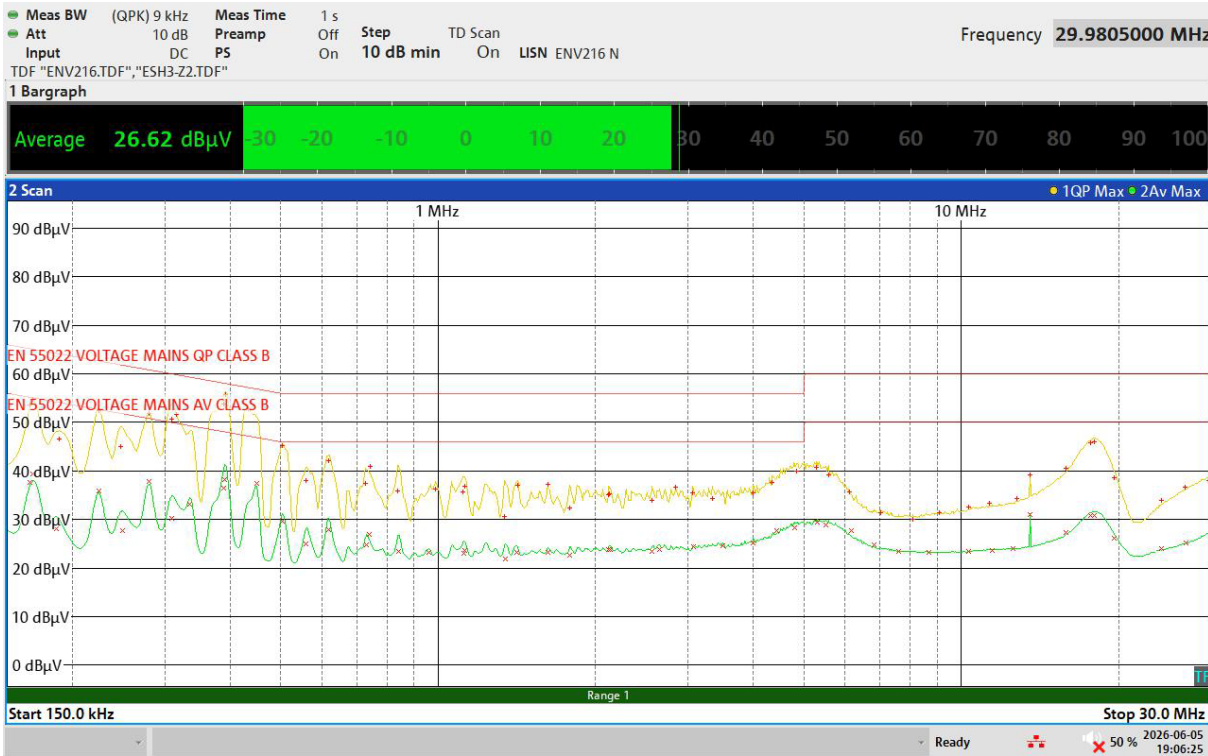


Figure 161 – Floating Ground EMI at 115 VAC b/w Input Lines A and C, Neutral

13.9.1.2 VIN: 230 VAC

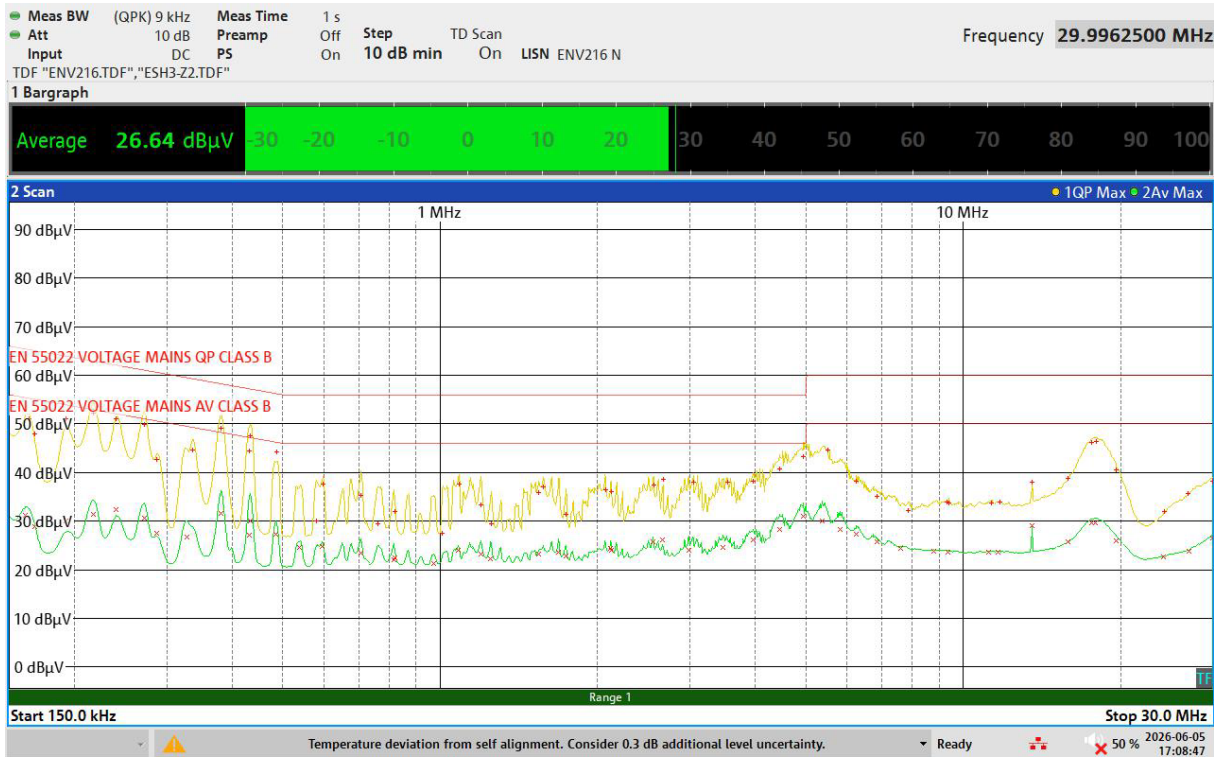


Figure 162 – Floating Ground EMI at 230 VAC b/w Input Lines A and B, Neutral

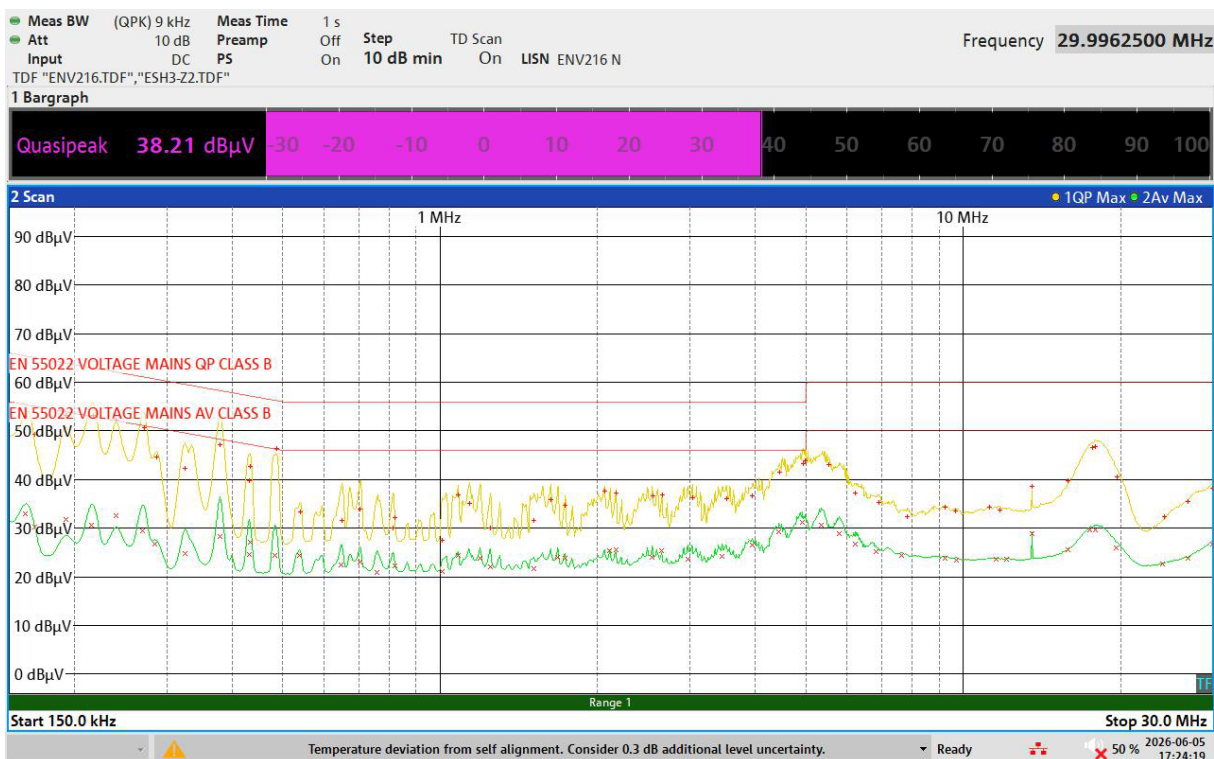


Figure 163 – Floating Ground EMI at 230 VAC b/w Input Lines B and C, Neutral

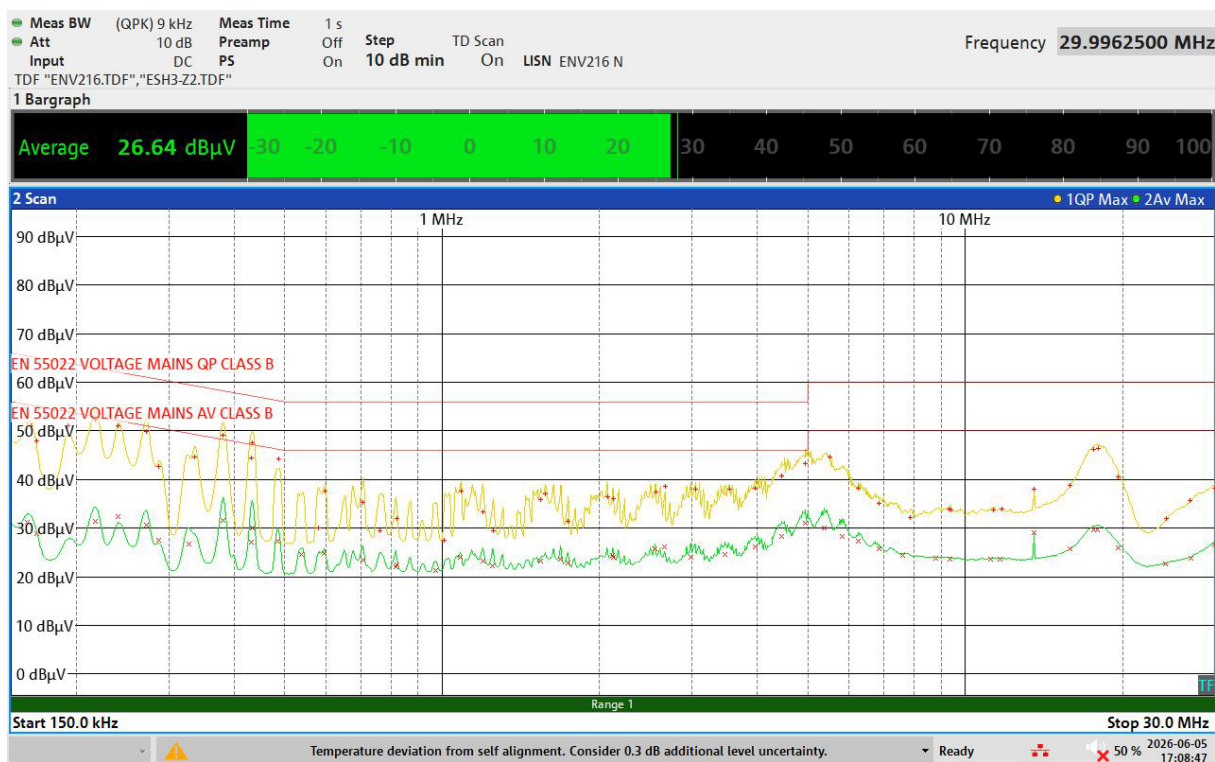


Figure 164 – Floating Ground EMI at 230 VAC b/w Input Lines A and C, Neutral

13.9.2 Line

13.9.2.1 VIN: 115 VAC

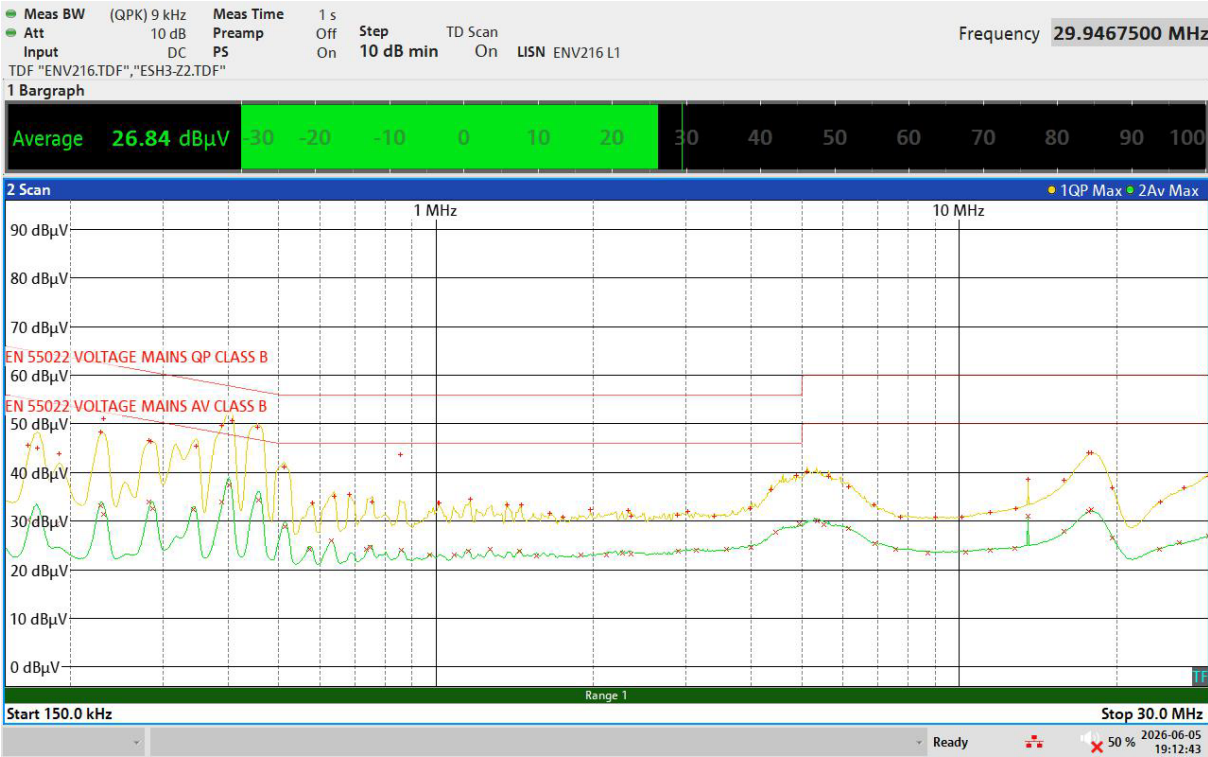


Figure 165 – Floating Ground EMI at 115 VAC b/w Input Lines A and B, Line

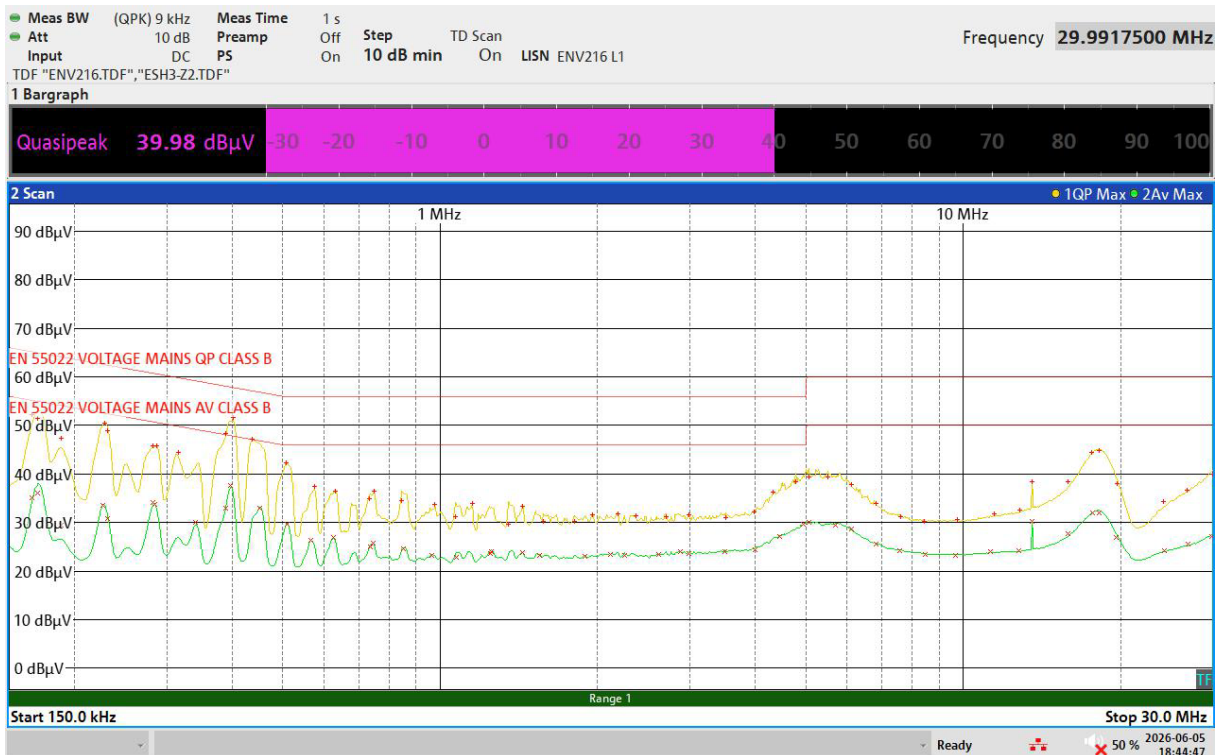


Figure 166 – Floating Ground EMI at 115 VAC b/w Input Lines B and C, Line

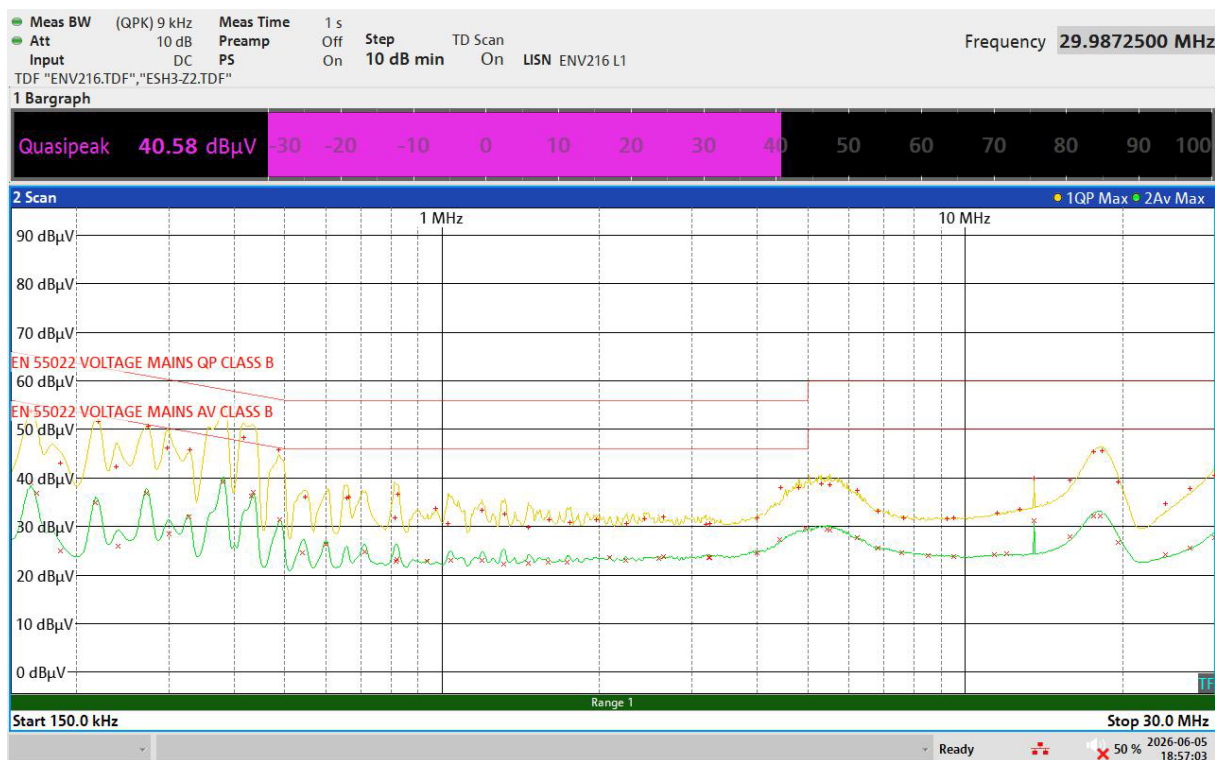


Figure 167 – Floating Ground EMI at 115 VAC b/w Input Lines A and C, Line



13.9.2.2 VIN: 230 VAC

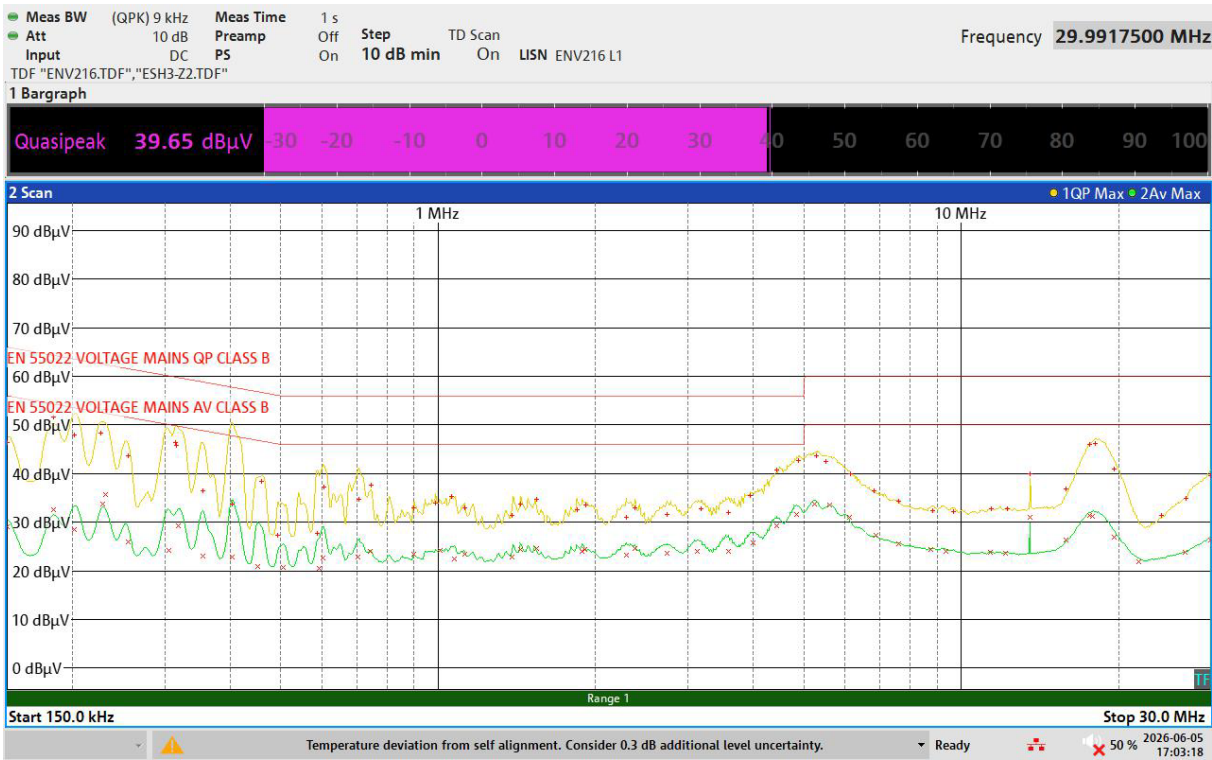


Figure 168 – Floating Ground EMI at 230 VAC b/w Input Lines A and B, Line

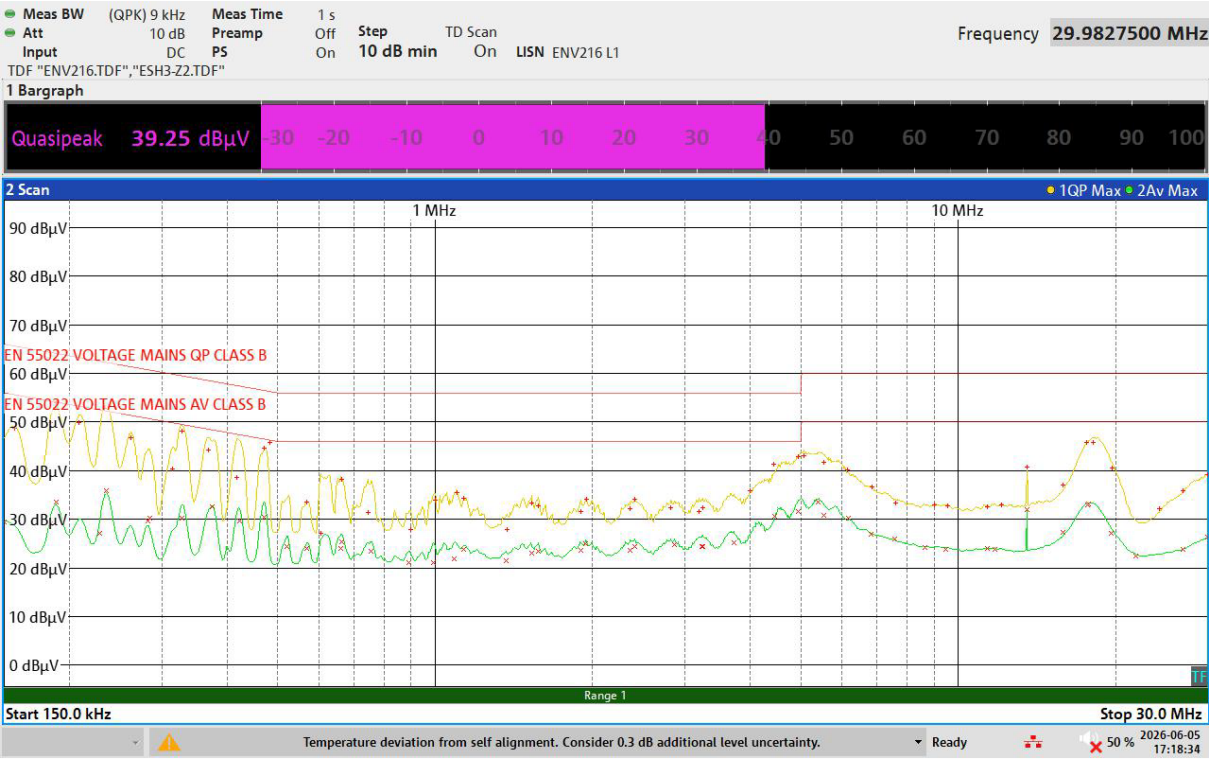


Figure 169 – Floating Ground EMI at 230 VAC b/w Input Lines B and C, Line

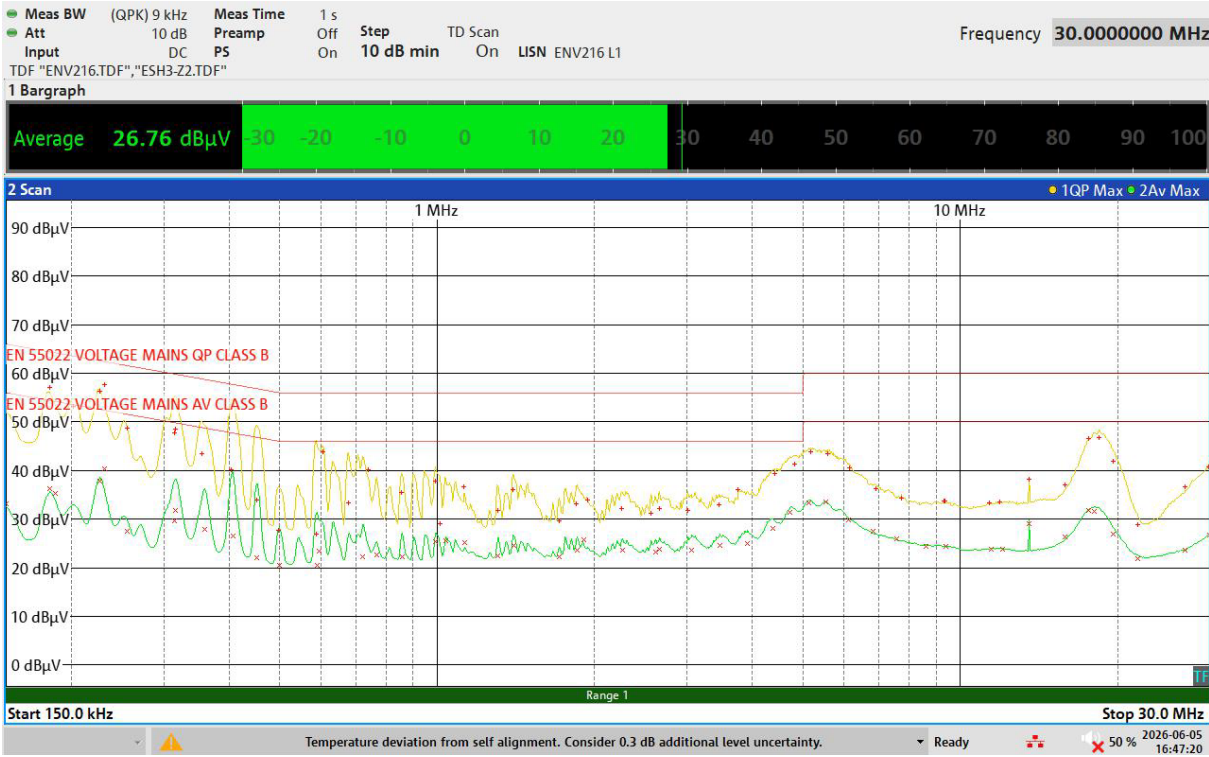


Figure 170 – Floating Ground EMI at 230 VAC b/w Input Lines A and C, Line

14 Bill of Materials

14.1 Bill of Materials: Electrical Components

Item	Quantity	Designator	Description	Manufacturer Part Number	Manufacturer
1	4	C1 C2 C3 C4	27 μ F, 450 V, Aluminum Electrolytic Capacitors, Radial, Can, (10 x 20 mm)	YMIN KCX 450V 27uF	Ymin
2	1	C5	2200 pF $\pm$ 10%, 1000 V (1 kV), Ceramic Capacitor, COG, NPO, 1206 (3216 Metric)	C1206C222KDGACAUTO	KEMET
3	1	C6	22 μ F, 50 V, Aluminum Electrolytic Capacitors, Radial, Can 2000 Hrs @ 85 °C, (5 x 11), LS 2 mm	EEU-FM1H220H	Panasonic
4	1	C7	4.7 μ F, 16 V, Ceramic, X70805 (2012 Metric)	CL21B475KOFNNNE	Samsung Electro-Mechanics
5	1	C8	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX Corp
6	1	C9	2.2 μ F, $\pm$ 10%, 25 V, Ceramic Capacitor X7R, 0805 (2012 Metric)	CL21B225KAFNFNE	Samsung Electro-Mechanics
7	1	C10	680 μ F, $\pm$ 20%, 25 V, Aluminum - Polymer Capacitors Radial, Can 16 mOhm 2000 Hrs @ 105 °C (8 mm x 16 mm)	A750KW687M1EAAE016	KEMET
8	1	C11	330 pF, $\pm$ 10%, 16 V, Ceramic Capacitor X7R, 0402 (1005 Metric), Automotive, AEC-Q200	VJ0402Y331KLJAJ32	Vishay
9	1	C12	330 pF, 50 V, Ceramic Capacitor, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C13	10 nF (10000 pF), 25 V, Ceramic Capacitor, X7R, 0603	CCC0603KRX7R8BB103	Yageo
11	1	C14	2.2 μ F, $\pm$ 10%, 25 V, X7R, r, -55 °C ~ 125 °C, 0805 (2012 Metric)	CL21B225KAFVPNE	Samsung Electro-Mechanics
12	1	CY1	1 nF (1000 pF), 760 VAC, Ceramic Capacitor, Y5U (E) Radial	WKP102MCPED0KR	Vishay
13	16	D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16	Diode, Standard, 600 V, 3 A, Surface Mount, SMB, DO-214AA	S3JB-13-F	Diodes Inc.
14	1	D17	Diode, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
15	1	D18	Diode, General Purpose, 1000 V (1 kV), 3 A, Surface Mount SMB, DO-214AA SMC	S3MB-13-F	Diodes Inc.

16	1	D19	Diode, 200 V, 1 A, Fast Recover, 150 ns, SMA	RS1D	Diodes Inc.
17	3	F1 F2 F3	FUSE BRD MNT, 6.3 A, 350 VAC, 72 VDC	0697H6300-02	Bel Fuse Inc.
18	1	L1	680 μ H, Unshielded Wirewound Inductor, 900 mA, 790 mOhm Max, Radial, Vertical Cylinder (Open)	7447480681	Würth Electronics Inc.
19	1	L2	10 μ H, Unshielded Wirewound Inductor, 3.1 A, 45 mOhm, Radial, Vertical Cylinder	RLB0913-100K	Bourns Inc.
20	1	Q1	MOSFET, N-Channel 150 V 17 A (Ta), 100 A (Tc), 6.2 W (Ta), 215 W (Tc), Surface Mount 8-DFN (5 x 6)	AONS66520	Alpha & Omega Semiconductor Inc.
21	12	R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12	RES, 6.8 M, 5%, 1/4 W, Thick Film, 1206	RC1206JR-076M8L	Yageo
22	2	R13 R14	RES, 430 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J434V	Panasonic
23	1	R15	RES, 10.7 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1072V	Panasonic
24	1	R16	RES, 60.4 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF60R4V	Panasonic
25	1	R17	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
26	2	R18 R19	RES, 30.1 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF30R1V	Panasonic
27	1	R20	RES, 11.8 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1182V	Panasonic
28	1	R21	RES, 100 k, $\pm$ 1%, 0.1 W, 1/10 W, Chip Resistor 0603 (1608 Metric), Anti-Sulfur, Thick Film	560112116004	Würth Electronics Inc.
29	1	R22	RES, 15 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ153V	Panasonic
30	1	R23	RES, 30 mOhms, $\pm$ 1%, $\pm$ 200 ppm/ $^{\circ}$ C, 0.25 W, 1/4 W, Chip Resistor, 0805 (2012 Metric) Current Sense Thick Film	CSR0805FK30L0	Stackpole Electronics Inc.
31	3	RT1 RT2 RT3	NTC Thermistor, 1 Ohm, 9 A	B57237S109M	Epcos (TDK)
32	3	RV1 RV2 RV3	385 VAC, 67 J, 7 mm, RADIAL	VDRS10P385BSE	Vishay
33	1	T1	Bobbin, EF20, Horizontal, 10 pins	T-H Bobbin EF-20	Pin Shine Industrial Co. Ltd.
34	1	U1	INN3624C-H606, INNO3 Switch Integrated Circuit, InnoSwitch-3EP_1250V, InSOP24D	INN3624C-H606	Power Integrations

Table 24 – Bill of Materials, Electrical parts



14.2 Bill of Materials: Mechanical Components

Item	Quantity	Designator	Description	Manufacturer Part Number	Manufacturer
1	3	A B C	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	2	N RTN	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

Table 25 – Bill of Materials, Mechanical parts

15 Transformer (T1) Specification

15.1 Electrical Diagram

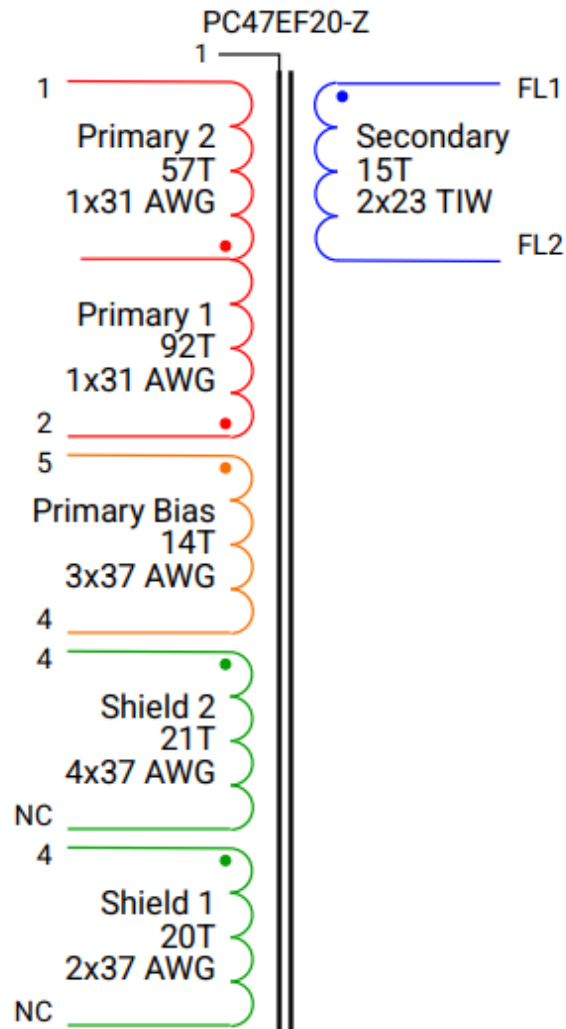


Figure 171 – Transformer Electrical Diagram

15.2 Electrical Specifications

Parameter	Condition	Specification
Nominal Primary Inductance	Measured at 1 V _{PK-PK} , typical switching frequency, between pin 2 to pin 1, with all other Windings open.	1836 μ H $\pm$ 5.0%
Electrical Strength	60 Hz, 1 second, from pins 1, 2, 4, 5 to pins FL1, FL2.	3000 VAC
Primary Leakage Inductance	Measured between pin 2 to pin 1, with all other windings shorted.	32 μ H (Max)

Table 26 – Transformer Electrical Specifications

15.3 List of Materials

Item	Description
[1]	Core: PC47EF20-Z, PC47, gapped for ALG of 83 nH / T ² .
[2]	Bobbin: EF20-Horizontal-10 pins (5/5); PI#: 25-00834-00.
[3]	Magnet wire: #31 AWG, double coated.
[4]	Magnet wire: #37 AWG, double coated.
[5]	Magnet wire: #23 AWG, Triple Insulated Wire.
[6]	Bus wire: #28 AWG, Alpha wire, tinned copper.
[7]	Tape: 3M 13450-F, Polyester film, 1 mil thickness, 12.5 mm wide.
[8]	Varnish: Dolph BC-359.

Table 27 – Transformer Material List

15.4 Transformer Build Diagram

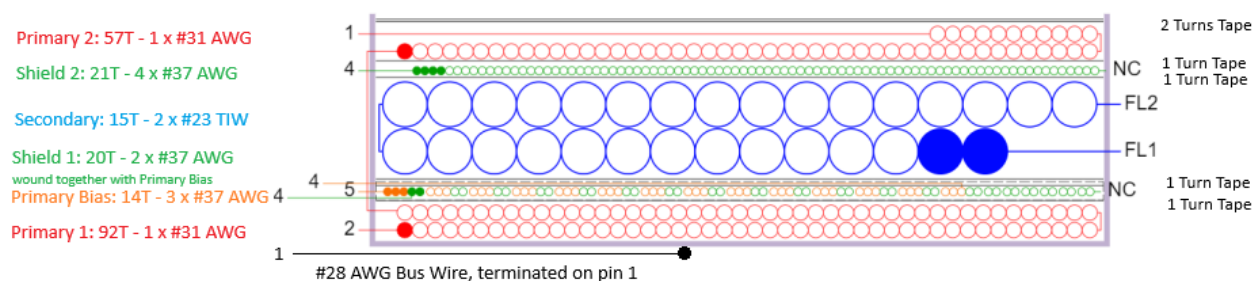


Figure 172 – Transformer Build Diagram

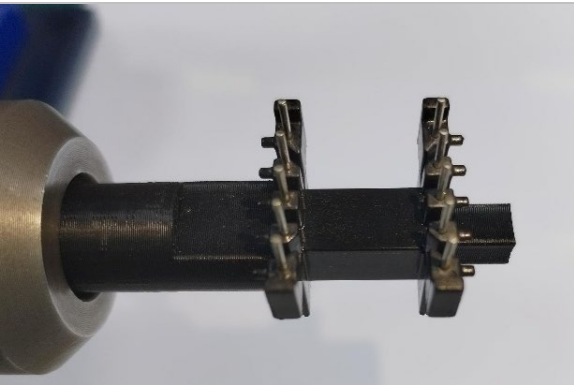
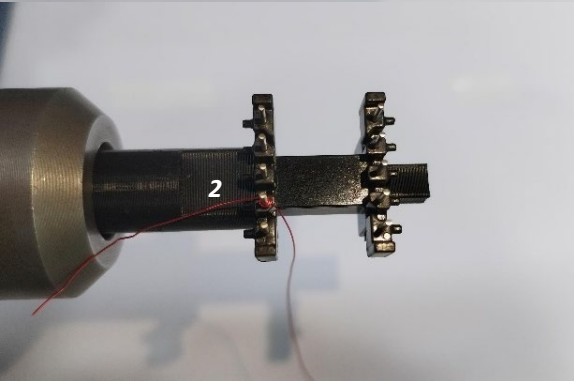
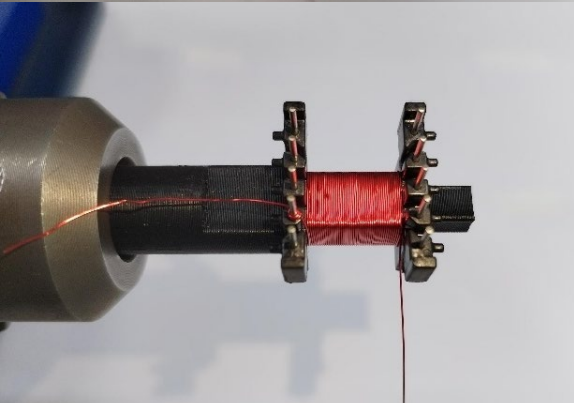
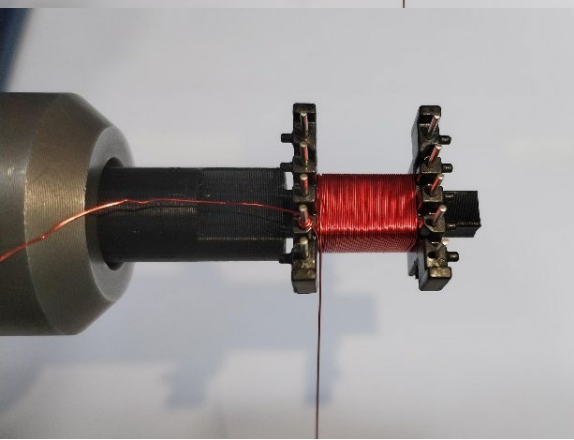
15.5 Transformer Instructions

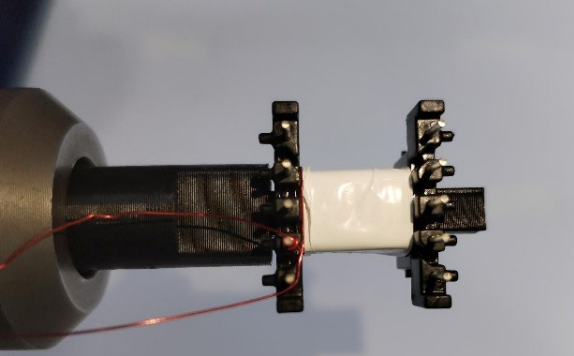
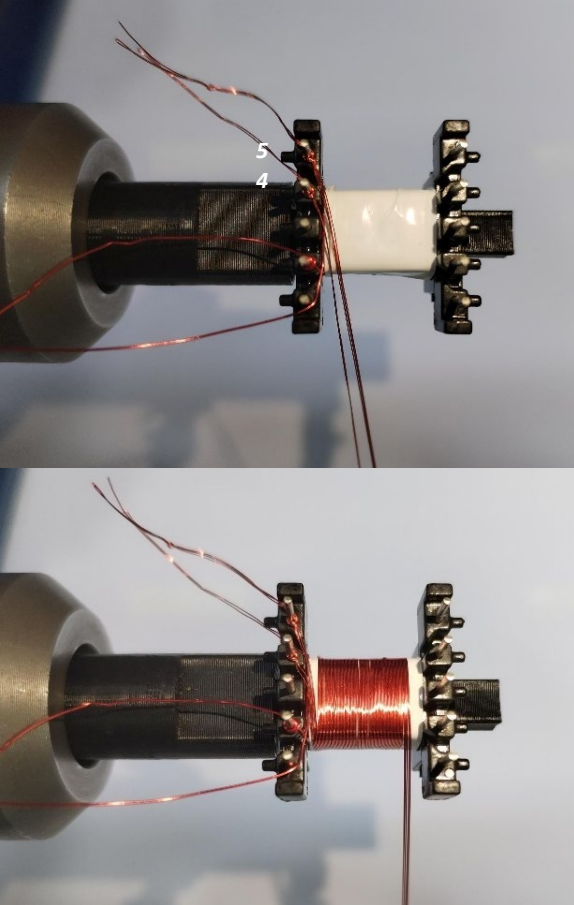
Winding Preparation	Position the bobbin, Item [2], on the mandrel such that the primary side of the bobbin is on the left side.
Primary 1	Start with 1 lead of Item [3] from Pin 2, and wind 92 turns in a clockwise direction for a total of 2 layers. Wind the 1st layer from left to right. At the end of 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding as flying lead to the left with enough length to be able to complete the second part of the split winding.
Insulation	Add 1 layer of tape, Item [7], on the top.
Primary Bias & Shield 1	Start with Primary Bias, using Item [4] (x3 leads) from Pin 5, together with Shield 1, using Item [4] (x2 leads) from Pin 4, and wind them together in a clockwise direction. Wind 14 turns (1 layer) for the Primary Bias and 20 turns (1 layer) for Shield 1, from left to right. After making 14 turns for the Primary Bias, add 1 layer of tape, Item [7], between the exit lead and the winding. Finish this winding on Pin 4 and continue winding Shield 1 for 6 turns. Spread the winding evenly across the entire bobbin. For Shield 1, leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation	Add 1 layer of tape, Item [7], on the top.
Secondary	Start with 2 leads of Item [5] marked as FL1 from the right, and wind 15 turns in a clockwise direction for a total of 2 layers. Wind the 1st layer from right to left. At the end of the 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding as flying lead marked as FL2 to the right.
Insulation	Add 1 layer of tape, Item [7], on the top.
Shield 2	Start with 4 leads of Item [4] from Pin 4, and wind 21 turns in a clockwise direction for a total of 1 layer, from left to right. Spread the winding evenly across the entire bobbin. Leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation	Add 1 layer of tape, Item [7], on the top.
Primary 2	Use the rest of the Primary 1 winding, and wind 57 turns in a clockwise direction for total of 2 layers, from left to right. At the end of the 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding on Pin 1.
Insulation	Add 2 layers of tape, Item [7], on the top.
Finish	Cut short FL1 and FL2 to 25.0 mm. Gap the core halves to get $1835.7 \mu\text{H} \pm 5.0\%$. Solder the bus wire, Item [6], to pin 1, then solder to the nearest core half and wrap around the two core halves. Use 2 layers of tape, Item [7], to secure and tie the core halves together. Remove pins 7, 8, and 9. Varnish with Item [8].

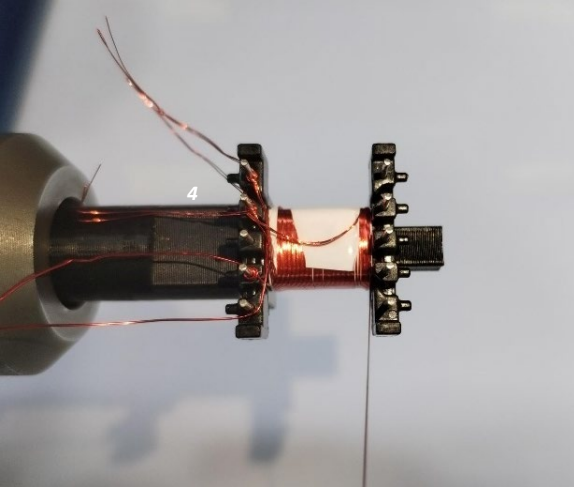
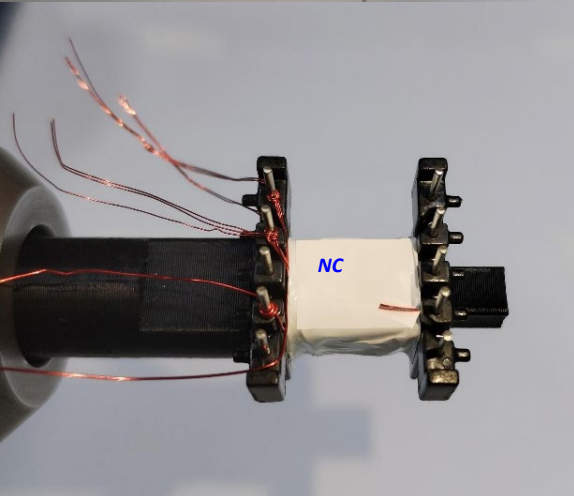
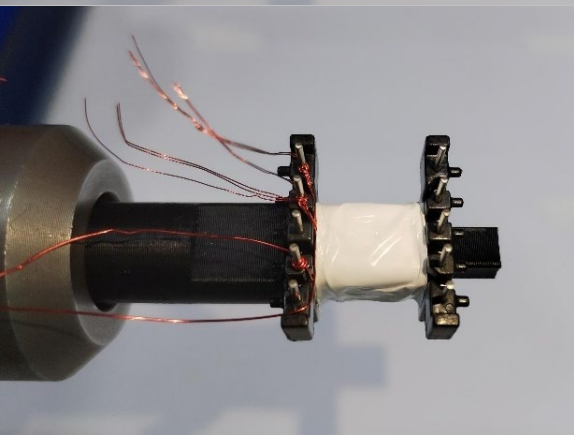
Table 28 – Transformer Instructions



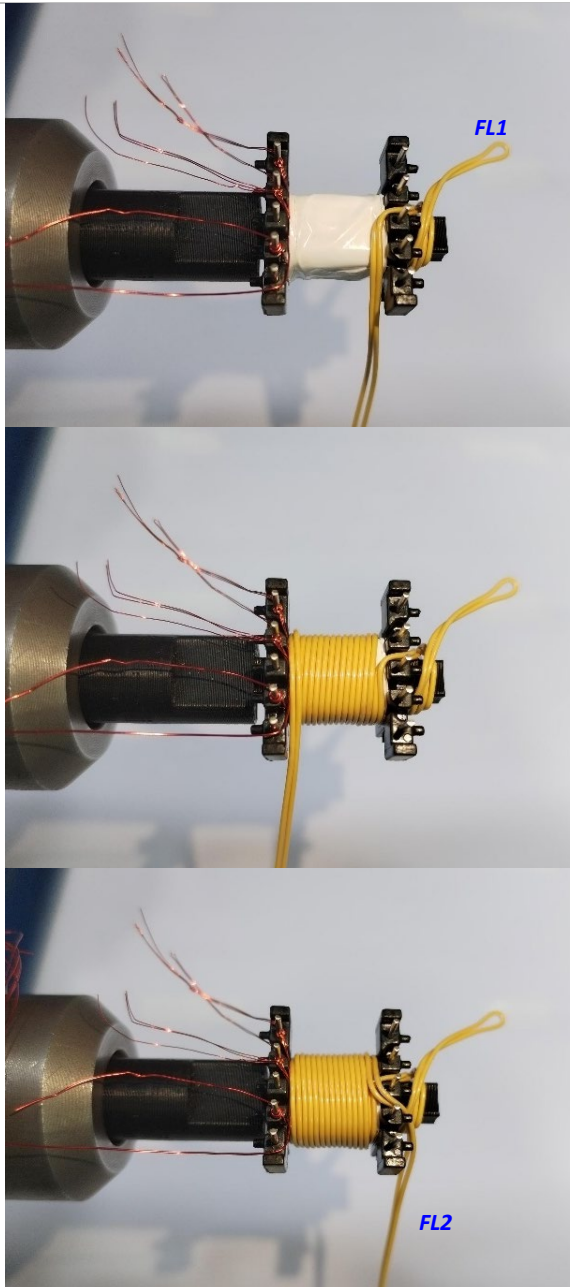
15.6 Winding Illustrations

Winding Preparation		Position the bobbin, Item [2], on the mandrel such that the primary side of the bobbin is on the left side.
Primary 1	  	Start with 1 lead of Item [3] from Pin 2, and wind 92 turns in a clockwise direction for a total of 2 layers. Wind one layer from left to right. At the end of the 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding as flying lead to the left with enough length to be able to complete the second part of the split winding.

Insulation		Add 1 layer of tape, Item [7], on the top.
Primary Bias & Shield 1		Start with Primary Bias, using Item [4] (x3 leads) from Pin 5, together with Shield 1, using Item [4] (x2 leads) from Pin 4, and wind them together in a clockwise direction. Wind 14 turns (1 layer) for the Primary Bias and 20 turns (1 layer) for Shield 1, from left to right. After making 14 turns for the Primary Bias, add 1 layer of tape, Item [7], between the exit lead and the winding.

		Finish this winding on Pin 4 and continue winding Shield 1 for 6 turns. Spread the winding evenly across the entire bobbin.
		For Shield 1, leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.
Insulation		Add 1 layer of tape, Item [7], on the top.

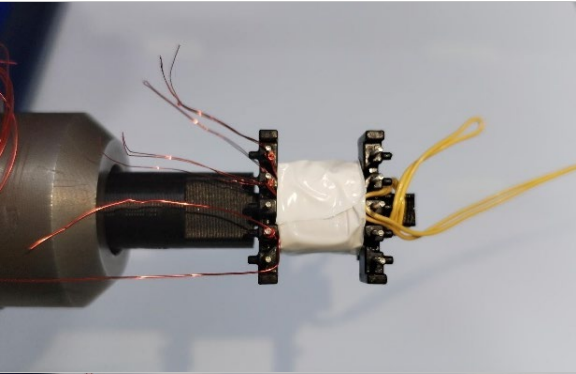
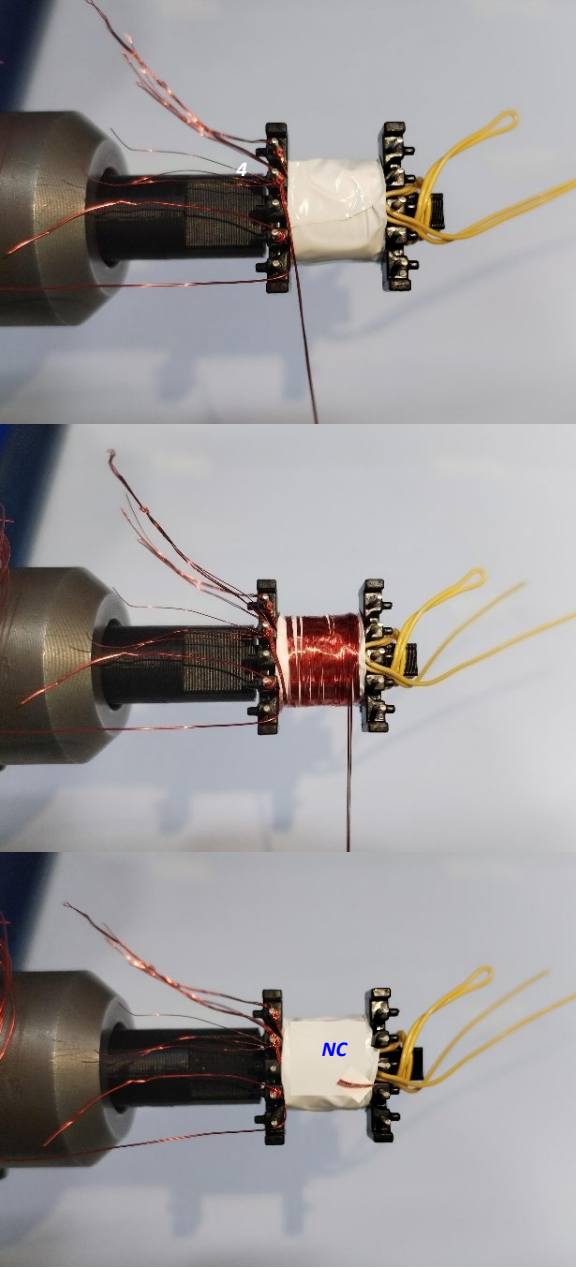
Secondary

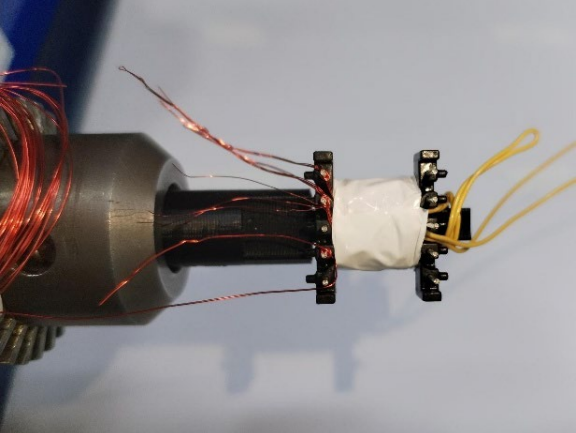
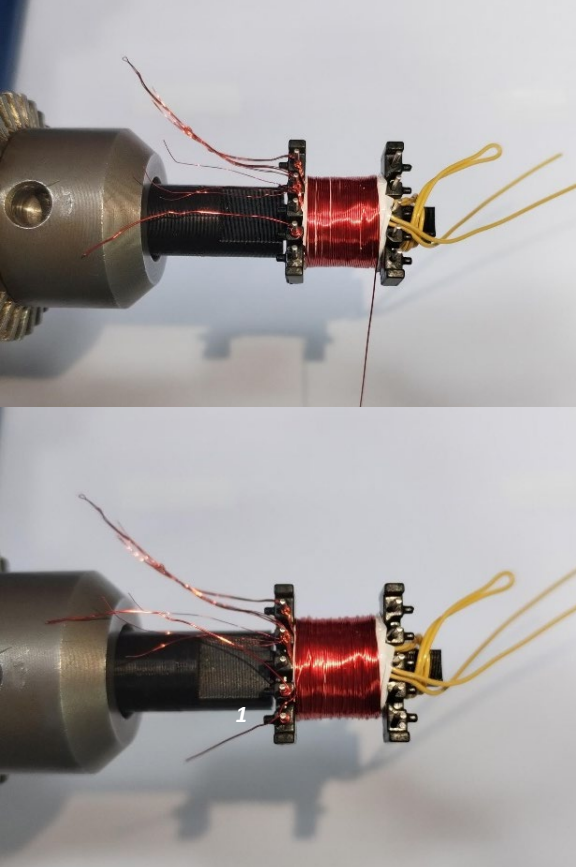


Start with 2 leads of Item [5] marked as FL1 from the right, and wind 15 turns in a clockwise direction for a total of 2 layers. Wind one layer from right to left.

At the end of 1st layer, continue to wind the next layer towards the beginning of the previous layer.

Finish this winding as flying lead marked as FL2 to the right.

Insulation		Add 1 layer of tape, Item [7], on the top.
Shield 2		Start with 4 leads of Item [4] from Pin 4, and wind 21 turns in a clockwise direction for a total of 1 layer, from left to right. Spread the winding evenly across the entire bobbin. Leave this end of the winding not connected. Bend the end 90 degrees and cut the wire as close as possible to the end of the last turn.

Insulation		Add 1 layer of tape, Item [7], on the top.
Primary 2		Use the rest of the Primary 1 winding, and wind 57 turns in a clockwise direction for total of 2 layers, from left to right. At the end of the 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding on Pin 1.

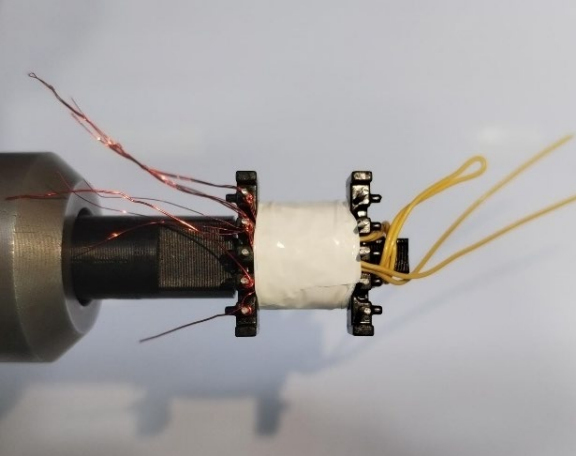
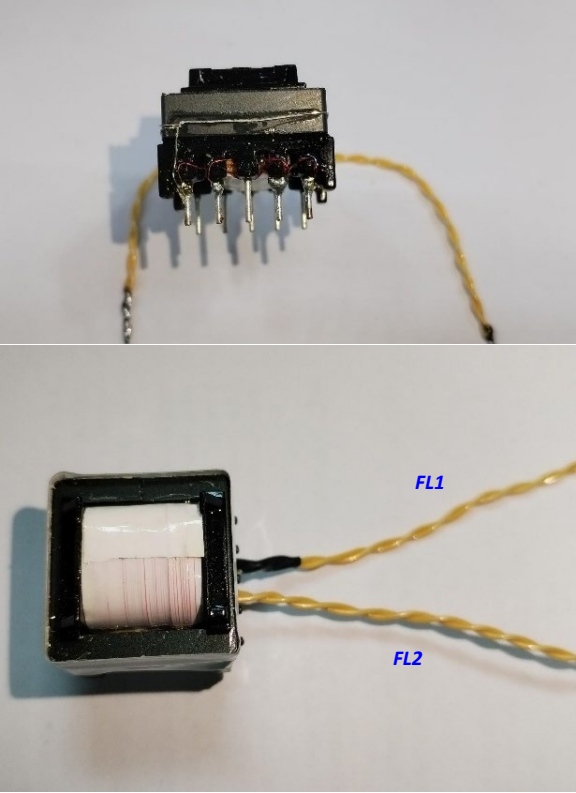
Insulation		Add 2 layers of tape, Item [7], on the top
Finish		Cut short FL1 and FL2 to 25.0 mm. Gap the core halves to get $1835.5 \mu\text{H} \pm 5.0\%$. Solder the bus wire, Item [6], to pin 1, then solder to the nearest core half and wrap around the two core halves. Use 2 layers of tape, Item [7], to secure and tie the core halves together. Remove pins 7, 8, and 9. Varnish with Item [8].

Table 29 – Transformer Winding Instructions

16 Transformer Design Spreadsheet

16.1 PIXIs Design Spreadsheet

1	Parameter Name ¹	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-EP 1250 V Flyback Design Spreadsheet
2	APPLICATION VARIABLES					Design Title
3	VIN_MIN	57		57	V	Minimum AC input voltage
4	VIN_MAX	580		580	V	Maximum AC input voltage
5	VIN_RANGE			Custom		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	27		27	μF	Input capacitor
8	VOUT			12.00	V	Output voltage at the board
9	PERCENT_CDC			0		Cable drop compensation desired at full load
10	IOUT	1.000		1.000	A	Output current
11	POUT			12.00	W	Output power
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
18	PRIMARY CONTROLLER SELECTION					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	INN3624C		INN3624C		Generic device code
21	DEVICE_CODE			INN3624C		Actual device code
22	POUT_MAX			20	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			5.80	Ω	Primary switch on time drain resistance at 100 °C
24	ILIMIT_MIN			0.884	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			0.950	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.017	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			1250	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			0.97	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW			963.8	V	Peak drain voltage on the primary switch during turn-off
33	WORST CASE ELECTRICAL PARAMETERS					
34	FSWITCHING_MAX	30550		30550	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	120.0		120.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN	77.00		77.00	V	Valley of the minimum input AC voltage at full load
37	KP			1.61		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation
39	DUTYCYCLE			0.496		Primary switch duty cycle
40	TIME_ON_MIN			1.481	μs	Minimum Primary switch on-time
41	TIME_ON			18.41	μs	Maximum primary switch on-time has been capped at 12.4 μs, resulting in an increased controller switching frequency of 49368 Hz (>30548 Hz):
42	TIME_OFF			16.87	μs	Primary switch off-time
43	LPRIMARY_MIN			1743.7	μH	Minimum primary inductance
44	LPRIMARY_TYP			1835.5	μH	Typical primary inductance

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45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			1927.3	μH	Maximum primary inductance
48	PRIMARY CURRENT					
49	IPEAK_PRIMARY			0.745	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	Iavg_PRIMARY			0.168	A	Primary switch average current
52	IRIPPLE_PRIMARY			0.745	A	Primary switch ripple current
53	IRMS_PRIMARY			0.288	A	Primary switch RMS current
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			7.399	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.00	A	Secondary winding current pedestal
58	IRMS_SECONDARY			2.281	A	Secondary winding RMS current
62	TRANSFORMER CONSTRUCTION PARAMETERS					
63	CORE SELECTION					
64	CORE	EF20		EF20		Core selection
65	CORE CODE			PC40EF20-Z		Core code
66	AE			33.50	mm^2	Core cross sectional area
67	LE			44.90	mm	Core magnetic path length
68	AL			1570	nH/turns^2	Ungapped core effective inductance
69	VE			1500.0	mm^3	Core volume
70	BOBBIN			B66206		Bobbin
71	AW			39.38	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
72	BW			12.50	mm	Bobbin width
73	BH			3.15	mm	Bobbin height
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
76	PRIMARY WINDING					
77	NPRIMARY			149		Primary turns
78	BPEAK			4018	Gauss	Peak flux density
79	BMAX			2804	Gauss	Maximum flux density
80	BAC			1402	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			83	nH/turns^2	Typical gapped core effective inductance
89	SECONDARY WINDING					
90	NSECONDARY	15		15		Secondary turns
96	BIAS WINDING					
97	NBIAS			14		Bias turns
101	PRIMARY COMPONENTS SELECTION					
114	BIAS DIODE					
115	VBIAS	10.0		10.0	V	Rectified bias voltage
116	VF_BIAS			0.70	V	Bias winding diode forward drop
117	VREVERSE_BIASDIODE			86.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
118	CBIAS			22	μF	Bias winding rectification capacitor
119	CBPP			4.70	μF	BPP pin capacitor
123	SECONDARY COMPONENTS					
124	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
125	RFB_LOWER			11.80	kΩ	Lower feedback resistor
126	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
130	MULTIPLE OUTPUT PARAMETERS					
131	OUTPUT 1					
132	VOUT1			12.00	V	Output 1 voltage
133	IOUT1			1.00	A	Output 1 current
134	POUT1			12.00	W	Output 1 power



135	IRMS_SECONDARY1			2.281	A	Root mean squared value of the secondary current for output 1
136	IRIPPLE_CAP_OUTPUT1			2.050	A	Current ripple on the secondary waveform for output 1
141	NSECONDARY1			15		Number of turns for output 1
142	VREVERSE_RECTIFIER1			94.43	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
143	SRFET1	AONS66520		AONS66520		Secondary rectifier (Logic MOSFET) for output 1
144	VF_SRFET1			0.7	V	SR FET on-time drain voltage for output 1
145	VBREAKDOWN_SRFET1			150	V	SR FET breakdown voltage for output 1
146	RDSN_SRFET1			9.5	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1

Table 30 – Transformer Design Spreadsheet for Set-up Without External Magnetizing Interference

16.2 PIXIs Spreadsheet for Set-up With External Magnetizing Interference

Note: The PIXIs spreadsheet below represents the state of the transformer inductance when the external magnetizing interference is present.

1	Parameter Name ²	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-EP 1250 V Flyback Design Spreadsheet
2	APPLICATION VARIABLES					Design Title
3	VIN_MIN	57		57	V	Minimum AC input voltage
4	VIN_MAX	580		580	V	Maximum AC input voltage
5	VIN_RANGE			Custom		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	27		27	μF	Input capacitor
8	VOUT			12.00	V	Output voltage at the board
9	PERCENT_CDC			0		Cable drop compensation desired at full load
10	IOUT	1.000		1.000	A	Output current
11	POUT			12.00	W	Output power
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
18	PRIMARY CONTROLLER SELECTION					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	INN3624C		INN3624C		Generic device code
21	DEVICE_CODE			INN3624C		Actual device code
22	POUT_MAX			20	W	Power capability of the device based on thermal performance
23	RDSO_N_100DEG			5.80	Ω	Primary switch on time drain resistance at 100 °C
24	ILIMIT_MIN			0.884	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			0.950	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.017	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			1250	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			0.97	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW			963.8	V	Peak drain voltage on the primary switch during turn-off
33	WORST CASE ELECTRICAL PARAMETERS					
34	FSWITCHING_MAX	52250		52250	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	120.0		120.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN	77.00		77.00	V	Valley of the minimum input AC voltage at full load
37	KP			2.16		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation
39	DUTYCYCLE			0.422		Primary switch duty cycle
40	TIME_ON_MIN			0.743	μs	Minimum Primary switch on-time
41	TIME_ON			9.52	μs	Maximum primary switch on-time
42	TIME_OFF			11.19	μs	Primary switch off-time
43	LPRIMARY_MIN			749.7	μH	Minimum primary inductance

² ACDC_InnoSwitch3-EP1250V_Flyback_080726; Rev.2.0



44	LPRIMARY_TYP			789.2	μH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			828.7	μH	Maximum primary inductance
48	PRIMARY CURRENT					
49	IPEAK_PRIMARY			0.888	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.168	A	Primary switch average current
52	IRIPPLE_PRIMARY			0.888	A	Primary switch ripple current
53	IRMS_PRIMARY			0.315	A	Primary switch RMS current
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			8.824	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.00	A	Secondary winding current pedestal
58	IRMS_SECONDARY			2.491	A	Secondary winding RMS current
62	TRANSFORMER CONSTRUCTION PARAMETERS					
63	CORE SELECTION					
64	CORE	EF20		EF20		Core selection
65	CORE CODE			PC40EF20-Z		Core code
66	AE			33.50	mm^2	Core cross sectional area
67	LE			44.90	mm	Core magnetic path length
68	AL			1570	nH/turns^2	Ungapped core effective inductance
69	VE			1500.0	mm^3	Core volume
70	BOBBIN			B66206		Bobbin
71	AW			39.38	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
72	BW			12.50	mm	Bobbin width
73	BH			3.15	mm	Bobbin height
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
76	PRIMARY WINDING					
77	NPRIMARY			149		Primary turns
78	BPEAK			1727	Gauss	Peak flux density
79	BMAX			1449	Gauss	Maximum flux density
80	BAC			725	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			36	nH/turns^2	Typical gapped core effective inductance
89	SECONDARY WINDING					
90	NSECONDARY	15		15		Secondary turns
96	BIAS WINDING					
97	NBIAS			14		Bias turns
101	PRIMARY COMPONENTS SELECTION					
114	BIAS DIODE					
115	VBIAS	10.0		10.0	V	Rectified bias voltage
116	VF_BIAS			0.70	V	Bias winding diode forward drop
117	VREVERSE_BIASDIODE			86.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
118	CBIAS			22	μF	Bias winding rectification capacitor
119	CBPP			4.70	μF	BPP pin capacitor
123	SECONDARY COMPONENTS					
124	RFB_UPPER			100.00	$\text{k}\Omega$	Upper feedback resistor (connected to the first output voltage)
125	RFB_LOWER			11.80	$\text{k}\Omega$	Lower feedback resistor
126	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
130	MULTIPLE OUTPUT PARAMETERS					
131	OUTPUT 1					
132	VOUT1			12.00	V	Output 1 voltage
133	IOUT1			1.00	A	Output 1 current



134	POUT1			12.00	W	Output 1 power
135	IRMS_SECONDARY1			2.491	A	Root mean squared value of the secondary current for output 1
136	IRIPPLE_CAP_OUTPUT1			2.281	A	Current ripple on the secondary waveform for output 1
141	NSECONDARY1			15		Number of turns for output 1
142	VREVERSE_RECTIFIER1			94.43	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
143	SRFET1	AONS66520		AONS66520		Secondary rectifier (Logic MOSFET) for output 1
144	VF_SRFET1			0.7	V	SR FET on-time drain voltage for output 1
145	VBREAKDOWN_SRFET1			150	V	SR FET breakdown voltage for output 1
146	RDSON_SRFET1			9.5	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1

Table 31 – Transformer Design Spreadsheet for Set-up With External Magnetizing Interference

Table 30 shows the design spreadsheet for the set-up without external magnetizing interference, while Table 31 shows the spreadsheet for the set-up with external magnetizing interference. Table 31 reflects the 57% drop in typical primary inductance, increased switching frequency, and higher primary and secondary current peaks.

In this report, external magnetizing interference refers to an externally applied magnetic field that affects the magnetic operating condition and primary inductance of the flyback transformer. External magnetizing interference reduces the primary inductance of the flyback transformer. The magnitude of this reduction increases as the magnetic-field strength increases or as the source of the interference moves closer to the transformer.

In response to the reduced primary inductance, the InnoSwitch3-EP controller increases the switching frequency as necessary to maintain reliable power delivery. Therefore, to improve the power supply's resilience to external magnetizing interference, the transformer should be designed with as high a nominal primary inductance as practicable, while the power supply should operate at as low a nominal switching frequency as practicable. These parameters must be selected while maintaining sufficient margin between the maximum operating flux density and the saturation flux density of the transformer core.

The PC40 core has a specified saturation flux density of approximately 3,900 G, while the transformer was designed to maintain a maximum operating flux density below 3,000 G. This design provides adequate saturation margin while allowing operation at a relatively low nominal switching frequency. Together, the high nominal primary inductance, low nominal switching frequency, and adequate saturation margin provide sufficient operating headroom for the controller to compensate for reductions in primary inductance, thereby improving the power supply's resilience to external magnetizing interference.

17 Revision History

Revision	Notes	Author	Date
A	Initial Release	AU	9/10/2026

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.



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