

Reference Design Report

Title	16 W Multiple Output Flyback Using InnoSwitch3-AQ INN3947FQ for Inverter Gate Drive Power
Specification	200 VDC – 1000 VDC Input; 14.0 V / 714 mA Regulated Output; Three 23.0 V / 87 mA Unregulated Outputs; 16 W Peak Output Power
Application	Inverter Gate Driver / Auxiliary Equipment Power Supply
Author	Automotive Systems Engineering Department
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Revision	C

Summary and Features

- Ultra-compact design for 800 VDC automotive BEV applications
- Low component count (only 72 electrical components)¹
- Uses new InSOP28 (F) package which provides 5 mm Drain to Source pin spacing
- Wide-range start-up and operating voltage from 200 VDC to 1000 VDC
- Automotive grade transformer with reinforced isolation
- $\geq 75\%$ full load efficiency across the input voltage range
- Accurate secondary-side regulation without optocouplers
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface-mount (SMD) components²
- Low profile, 18.6 mm high

¹ Power conversion stage only, excluding unpopulated components, input and output ports.

² Excluding customized transformer.

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Disclaimer:

The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. Parameters, numbers, values, and other technical data included in the technical information were calculated and determined, to our best knowledge, to be in accordance with the relevant technical norms (if any). They may be based on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein.

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1 Introduction

This engineering report describes a 16 W quad output automotive power supply. It is intended for use in 800 V battery powered electric vehicles and supports a wide input range of 200 VDC to 1000 VDC. This design uses the 1700 V rated INN3947FQ IC from the InnoSwitch™3-AQ family of IC's.

In a typical configuration, the 14 V output provides an emergency backup power rail for the control power of the main traction inverter. The 23 V outputs will be post-regulated into +18 / -5 V dual outputs power stages to provide power for gate drivers.

The design provides reinforced isolation between the High Voltage DC (HVDC) input and the 14 V and 23 V outputs by observing the creepage and clearance requirements described in IEC 60664 parts 1 and 4. Basic isolation is provided between 14 V and 23 V outputs.

The report contains the power supply design specifications, schematic, bill of materials (BOM), specification for the magnetics, printed circuit board (PCB) layout, and performance data.



Figure 1 – Populated Circuit Board, Entire Assembly.

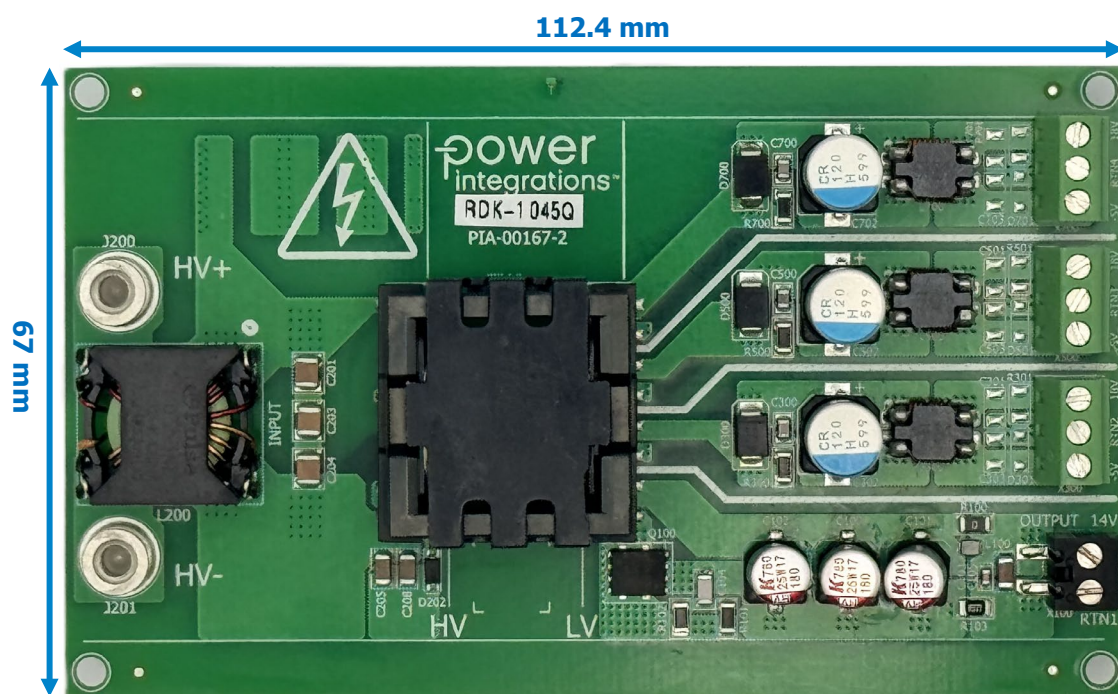


Figure 2 – Populated Circuit Board, Top.

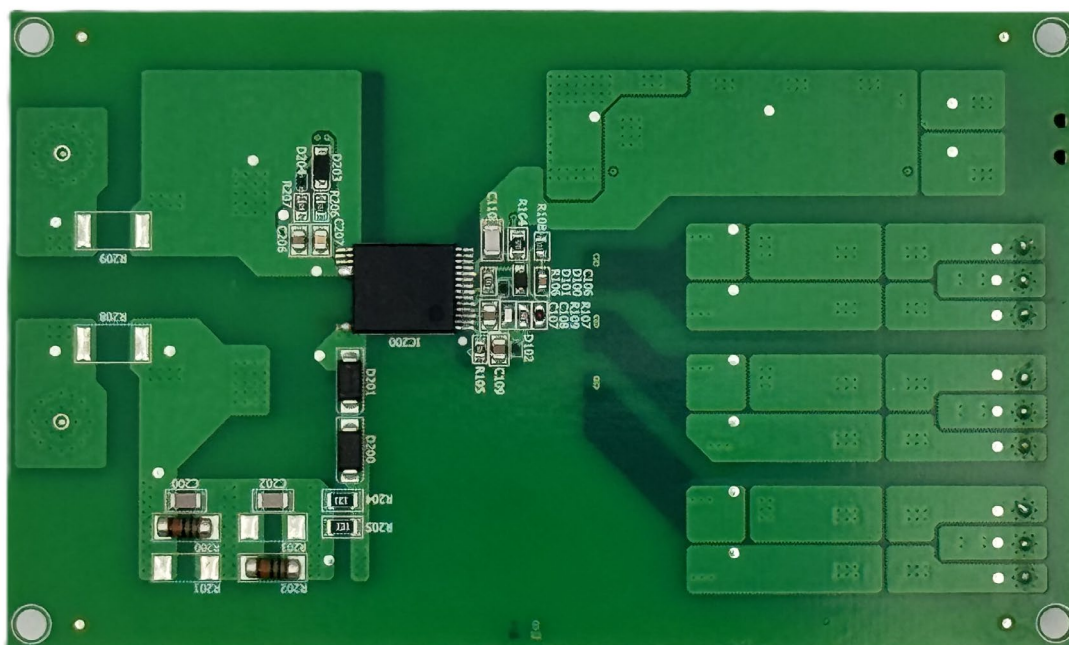


Figure 3 – Populated Circuit Board, Bottom.



Figure 4 – Populated Circuit Board, Side.

The regulated 14 V output can deliver 10 W continuously across an input voltage range of 200 VDC to 1000 VDC which can be used to provide gate power for the current generation of SiC or IGBT MOSFETs.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also simplifies the implementation of synchronous rectification improving overall efficiency (compared to diode rectification) - saving cost and space and eliminating the need for heat sinks.

2 Design Specification

The following tables represent the minimum acceptable performance for the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC-Link Input Voltage Referenced to HV-	HV	200	800	1000	V _{DC}
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage 1	14 V _{AUX}	13.3	14	14.7	V _{DC}
Voltage Load and Line Regulation for Output Voltage 1	14 V _{REG}	-5		+5	%
Ripple Voltage 1 Measured on Board	14 V _{RIPPLE}		250		mV
Unregulated Output Voltages 2 to 4	23 V _{CCx}	20.7	23	25.3	V _{DC}
Voltage Load and Line Regulation for Output Voltages 2 to 4 (with minimum load of 15 mA)	23 V _{REG}	-10		+10 ³	%
Ripple Voltage 2 to 4 Measured on Board	23 V _{RIPPLE}		500		mV
Output Current Parameters					
Output Current 1	I _{OUT1}		714		mA
Output Current 2 to 4	I _{OUT2} – I _{OUT4}		87		mA
Output Power Parameters					
Continuous Output Power at 200 V _{DC} – 900 V _{DC} Input	P _{OUT}		16		W
Output Overshoot and Undershoot During Dynamic Load Condition					
0% - 50% - 0% Transient Load	Δ V _{OUT1}	-5		+5	%
50% - 100% - 50% Transient Load					
10% - 90% - 10% Transient Load					
0% - 50% - 0% Transient Load	Δ V _{OUT2} – V _{OUT4}	-10		+10	%
50% - 100% - 50% Transient Load					
10% - 90% - 10% Transient Load					
Operating Parameters					
Operating Switching Frequency	f _{sw}			35	kHz

Table 1 – Electrical Specifications.

³ For tighter load regulation, a post-regulation circuit may be added at the output. At light load conditions, load regulation may go as high as 26%. See Section 9.3.



2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3947FQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1400	V
Working Voltage	V_{WORKING}	200	800	1000	V
Pollution Degree	PD			2	
CTI for FR4	CTI	175		399	
Rated Impulse Voltage	V_{IMPULSE}			2.50	kV
Altitude Correction Factor for h _a	C_{ha}			1.59	mm
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	CLR_{REINFORCED}	4.8			mm
Basic Creepage Distance Requirement for PCB	CPG_{BASIC(PCB)}	5.0			mm
Reinforced Creepage Distance Requirement for PCB	CPG_{REINFORCED(PCB)}	10.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	V_{ISO}	3536			V _{RMS}
Partial Discharge Test Voltage	V_{PD_TEST}	2100			V _{PK}

Table 2 – Isolation Coordination⁴.

2.3 Environmental Specification

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T _a	-40		85	°C
Altitude of Operation	h _a			5500	m

Table 3 – Environmental Specifications.

⁴ Clearance and creepage distances were calculated according to IEC 60664-1 and IEC 60664-4.

3 Schematic

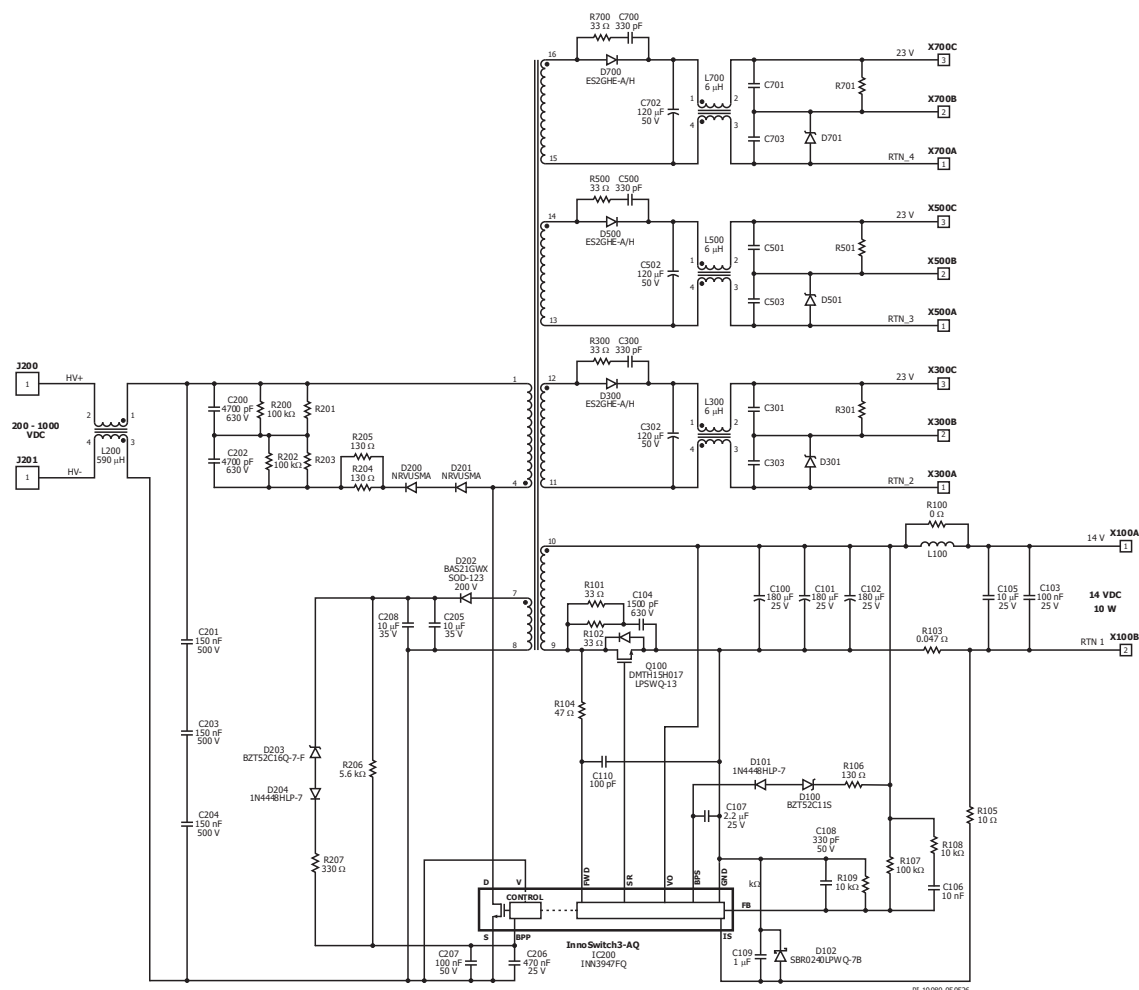


Figure 5 – RDR-1045Q Schematic⁵.

⁵ Provision for additional LC filter (L100) is added if there is a need for lower output ripple voltage.

4 Circuit Description

4.1 Input Filter

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. These transient events can create high levels of electrical noise that can interfere with the power supply's operation. The bypass capacitors C201, C203, and C204 and input common-mode choke L200 reduce the noise entering the power supply and prevent it from affecting the overall performance of the design. These capacitors also minimize the primary-side current loop. The capacitors are selected so as to not exceed 65% of their voltage rating and to maintain enough pad separation to enable a design that meets creepage and clearance requirements.

Common-mode inductor L200 was selected to enable the reference board to improve common-mode transient immunity.

4.2 High-Voltage Circuit

The power supply is a flyback converter topology that provides four isolated low voltage outputs from the high-voltage input. The primary winding of flyback transformer T200 is connected between the high-voltage DC input and the drain terminal of 1700 V SiC power switch which is internal to the InnoSwitch3-AQ IC (IC200).

An RCD across snubber circuit is placed across the primary winding, to limit the drain-source voltage peak across the primary switch during turn-off. Two super-fast diodes D200 and D201 were placed in series to meet creepage and clearance requirements and ensure that the reverse voltage across the diodes would not exceed 70% of their maximum rating. Capacitors C200 and C202 captures energy from the leakage inductance of transformer T200. The capacitor values were selected to minimize the voltage ripple across the snubber resistor network and maintain nearly constant power dissipation through the switching cycle. Resistors R200 to R202 dissipate the energy stored in the snubber capacitors. The resistor values were selected such that the voltage across each did not exceed 80% of their maximum rating and was below 50% of their maximum power rating.

During normal operation, the primary-side block is powered by an auxiliary winding on transformer T200. This improves efficiency and reduces the heating of the InnoSwitch3-AQ IC. The output of the auxiliary winding is rectified and DC filtered using diode D202 and capacitors C205 and C208. The InnoSwitch3-AQ is self-starting, using an internal high-voltage current source to charge the BPP capacitors, C206 and C207. Current is injected into the BPP capacitors through resistor R206. Diodes D203, D204, and resistor R207 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) as long as the fault is present. In this design, line undervoltage (UV) and overvoltage (OV) features were disabled by shorting the V pin to the SOURCE pin. This allows the design to operate at inputs as low as 30 VDC.



4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing and gate drive for the secondary MOSFET providing synchronous rectification (SR). The voltage across the secondary winding of the transformer T200 is rectified by the synchronous rectifier MOSFETs Q100 then DC filtered by capacitors C100, C101, and C102. High frequency ringing during switching is reduced by the RC snubber formed by resistors R101, R102, and capacitor C104 across the Drain-Source nodes of the SR FET.

The secondary-side controller inside the InnoSwitch3-AQ IC controls the switching of the SR FETs. Control timing is based on the negative edge voltage transition detected on the FWD pin via resistor R104. Capacitor C110 and resistor R104 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded.

In discontinuous conduction mode (DCM), the SR MOSFET is turned off when the voltage across it rises above $V_{SR(TH)}$. Secondary-side control of the primary-side switch prevents cross-conduction, ensuring reliable SR operation.

The secondary-side of the InnoSwitch3-AQ IC is self-powered from either the secondary winding (through R104 and the FWD pin) or the output voltage (through the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C107 via an internal regulator.

Diodes D100, D101, and resistor R106 form the secondary-side output overvoltage protection circuit. During output overvoltage events, the diodes turn on, and current is injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR.

The InnoSwitch3-AQ IC has an internal reference of 1.265 V presented to the FB pin. Resistors R107 and R109 form the feedback voltage divider network. Capacitor C108 provides decoupling of high-frequency noise. RC network C106 and R108 improves the transient response and lowers output ripple.

The output current sense resistor R103 sets the output current limit. The voltage across R103 is compared to an internal threshold of approximately 35 mV. Once reached, secondary requests will be inhibited, causing output voltage to drop. The IC will enter auto-restart (AR) when the output voltage falls 10% below regulation during CC mode and recovers when the load current is reduced below the CC limit.

The voltage across the 23 V cross regulated windings of the transformer T200 are rectified by the freewheeling diodes D300, D500, and D700 and filtered by the capacitors C302, C502, and C702. Regulation of the 23 V outputs depends on good coupling (low leakage inductance) to the 14 V output. This is addressed in the transformer design.



5 PCB Layout

5.1 Main Board PCB

Layers: Four (4)
Board Material: FR4
Board Thickness: 1.8 mm
Copper Weight: 2 oz

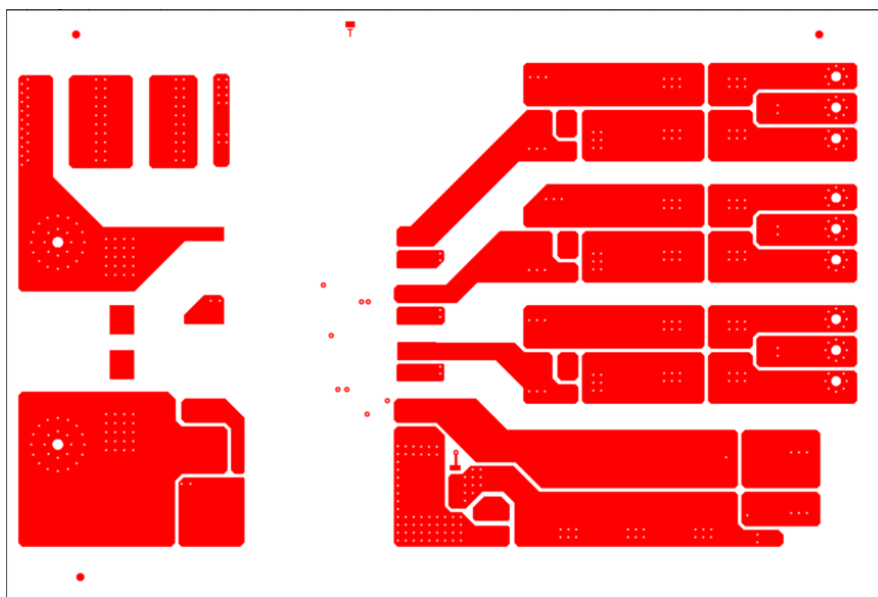


Figure 6 – RDR-1045Q Main Board Top Layer PCB Layout.

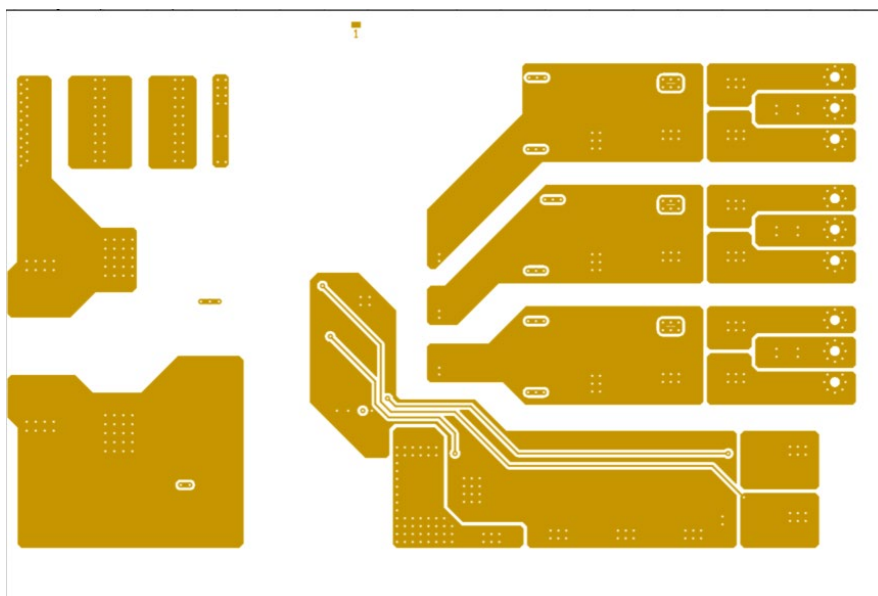


Figure 7 – RDR-1045Q Main Board Mid-Layer 1 PCB Layout.

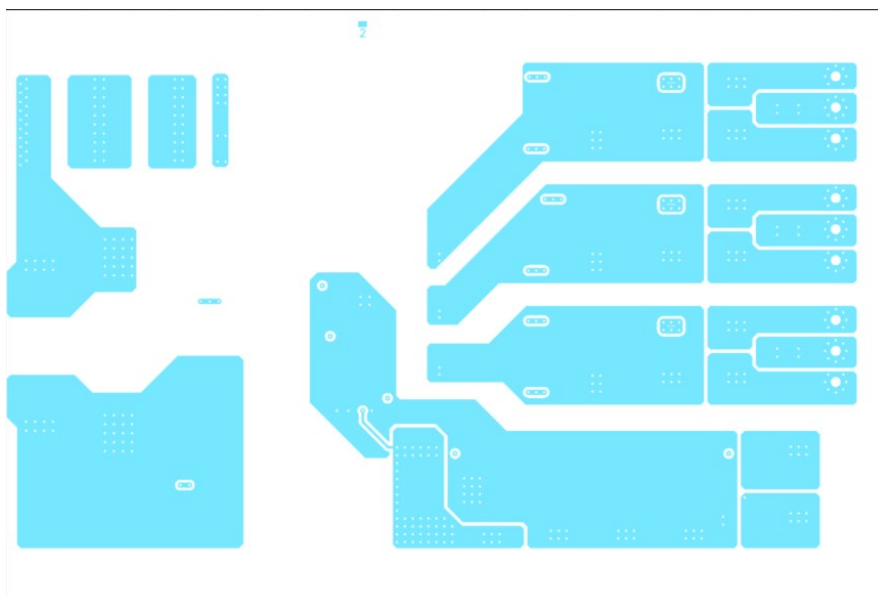


Figure 8 – RDR-1045Q Main Board Mid-Layer 2 PCB Layout.

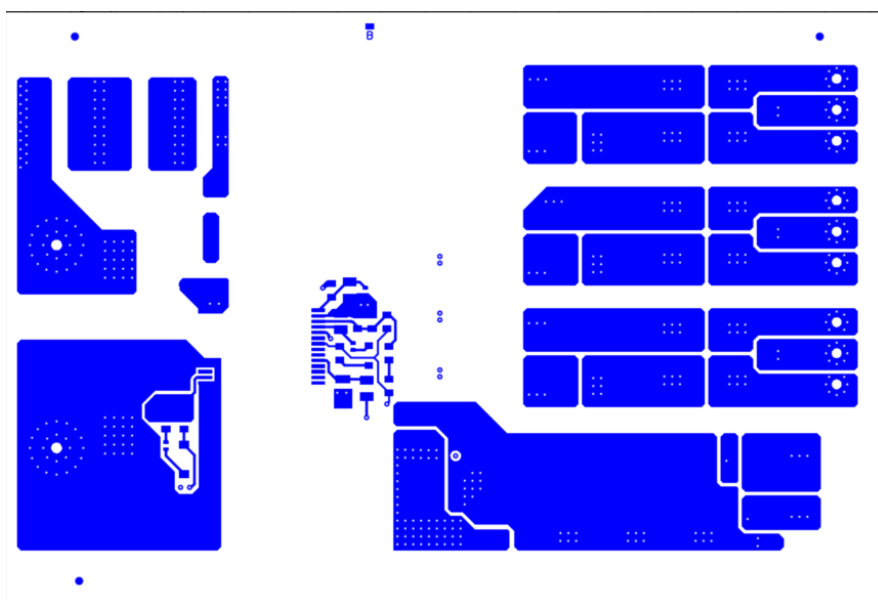


Figure 9 – RDR-1045Q Main Board Bottom Layer PCB Layout.

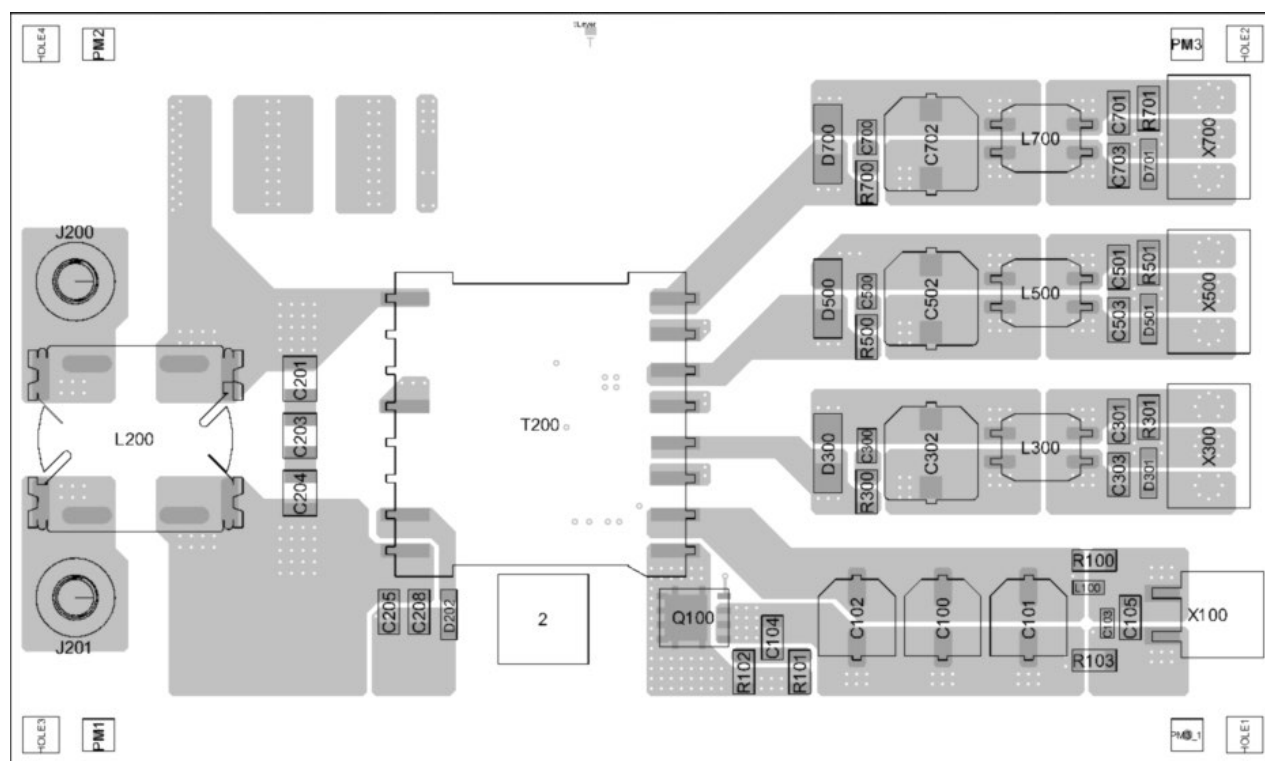


Figure 11 - RDR-1045Q Main Board PCB Assembly (Top).

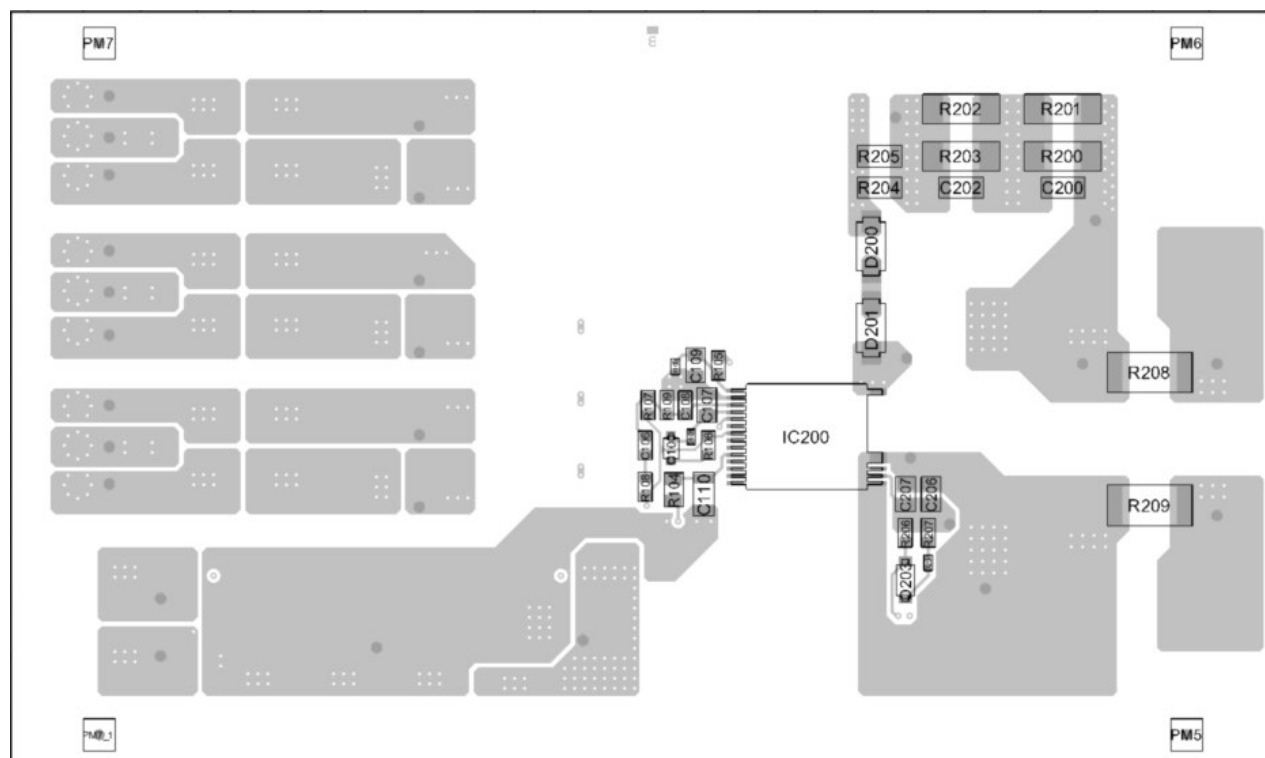


Figure 12 – RDR-1045Q Main Board PCB Assembly (Bottom).

6 Bill of Materials

Item	Quantity	Designator	Description	Mfr. Part Number	Manufacturer
1	3	C100, C101, C102	180 μ F 25 V Aluminum - Polymer Capacitors Radial, Can - SMD 30 mOhm 4000 Hrs at 125 °C	EEH-ZKE181XUP	Panasonic
2	1	C103	CAP CER 0.1 μ F 25 V X7R 0603	CGA3E2X7R1E104K080AA	TDK
3	1	C104	CAP CER 1500 pF 630 V C0G 1206	CGA5H4C0G2J152J115AA	TDK
4	3	C105, C205, C208	CAP CER 10 μ F 2.5 V X7R 1206	TMK316AB7106KLHT	Taiyo Yuden
5	1	C106	CAP CER 10000PF 25V C0G/NP0 0603	GRT1885C1E103FA02D	Murata
6	1	C107	CAP CER 2.2 μ F 25 V X7R 0805	TMK212B7225KGHT	Taiyo Yuden
7	1	C108	CAP CER 330 pF 50 V C0G/NP0 0603	C0603C331J5GACAUTO	KEMET
8	1	C109	CAP CER 1 μ F 35 V X7R 0805	GMK212B7105KGHT	Taiyo Yuden
9	1	C110	CAP CER 100 pF 630 V C0G 1206	CGA5C4C0G2J101J060AA	TDK
10	2	C200, C202	CAP CER 4700 pF 630 V C0G 1206	CGA5F4C0G2J472J085AA	TDK
11	3	C201, C203, C204	CAP CER 0.15 μ F 500 V X7R 1210	C1210X154KCRACAUTO	KEMET
12	1	C206	CAP CER 0.47 μ F 25 V X7R 0805	CGA4J2X7R1E474K125AA	TDK
13	1	C207	CAP CER 0.1 μ F 50 V X7R 0805	08055C104K4Z2A	KYOCERA AVX
14	3	C300, C500, C700	CAP CER 330 pF 450 V C0G 0805	CGA4C4C0G2W331J060AA	TDK
15	3	C302, C502, C702	CAP ALUM POLY 120 μ F 20% 50 V SMD	PCR1H121MCL2GS	Nichicon
16	1	D100	DIODE ZENER 11 V 500 mW SOD323	BZT52C11S	Good-Ark
17	1	D102	DIODE SBR 40 V 200 mA X1DFN10062	SBR0240LPWQ-7B	Diodes Incorporated
18	2	D101, D204	DIODE STD 80 V 125 mA X1DFN10062	1N4448HLP-7	Diodes Incorporated
19	2	D200, D201	DIODE STD 1000 V 1.5 A DO214AC	NRVUS2MA	onsemi
20	1	D202	DIODE STANDARD 200 V 225 mA SOD123	BAS21GWX	Nexperia
21	1	D203	DIODE ZENER 16 V 370 mW SOD123	BZT52C16Q-7-F	Diodes Incorporated
22	3	D300, D500, D700	DIODE STANDARD 300 V 2 A DO214AA	ES2GHE3_A/H	Vishay
23	1	IC200		INN3947FQ	
24	2	J200, J201	TERM REDCUBE M4 1 PIN SMD	7466104R	Wurth Elektronik
25	1	L100	FIXED IND 330 nH 1.13 A 180 mOhm SM	LQH2MPZR33NGRL	Murata
26	1	L200	CMC 5.6 A 2 LN SMD	P0353NL	Pulse
27	3	L300, L500, L700	6 uH Common-Mode Choke 7.00mm x 6.00mm	ACSR0906S060NT	SunLord
28	1	Q100	MOSFET BVDSS: 101 V~250 V POWERDI5	DMTH15H017LPSWQ-13	Diodes Incorporated
29	1	R100	RES SMD 0 Ω JUMPER ¼ W 1206	AF1206JR-070RL	YAGEO
30	5	R101, R102, R300, R500, R700	RES SMD 33 Ω 1% ¼ W 1206	CRCW120633R0FKEA	Vishay
31	1	R103	RES 0.047 Ω 1% ¼ W 1206	WSL1206R0470FEA	Vishay
32	1	R104	RES 47 Ω 5% 1/8 W 0805	RMCF0805JT47R0	Stackpole
33	1	R105	RES 10 Ω 5% 1/10 W 0603	CRGCQ0603J10R	TE Connectivity
34	1	R106	RES SMD 130 Ω 5% 1/10 W 0603	ERJ-3GEYJ131V	Panasonic
35	1	R107	RES 100 kOhm 0.5% ¼ W 0603	ERJ-UP3D1003V	Panasonic
36	1	R108	RES 10 kOhm 1% 1/8W 0603	RNCP0603FTD10K0	Stackpole
37	1	R109	RES SMD 10 kOhm 5% 1/10 W 0603	ERJ-3GEYJ103V	Panasonic
38	2	R200, R202	RES SMD 100 kOhm 1% 1 W 0207	MMB02070C1003FB200	Vishay
39	2	R204, R205	RES SMD 130 Ω 5% 2/3 W 1206	ERJ-P08J131V	Panasonic
40	1	R206	RES 5.6 kOhm 5% 1/10 W 0603	RMCF0603JT5K60	Stackpole
41	1	R207	RES SMD 330 Ω 5% 1/10 W 0603	AC0603JR-07330RL	YAGEO



42	1	T200	16 W Power Transformer		Power Integrations
43	1	T200-Core	3C95 Ferrite Core	EFD25/13/9-3C96	Ferroxcube
44	1	T200-Bobbin	Bobbin		Sunlord
45	1	X100	TERMI-BLOK SMD MOUNT 180_2P_3.81	2383945-2	TE Connectivity
46	3	X300, X500, X700	TERM BLK 3POS SIDE ENT 3.5 mm PCB	1751251	Phoenix Contact

Table 4 – RDR-1045Q Bill of Materials⁶.

⁶ All components are AEC-Q qualified except the connectors and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

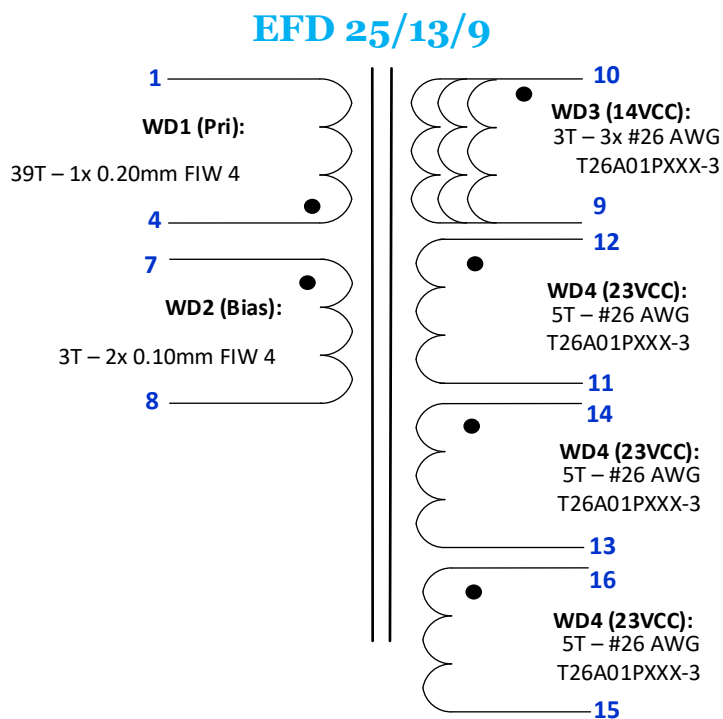


Figure 13 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side		16		W
Input voltage V_{DC}	Flyback topology	200	800	1000	V
Switching frequency				35	kHz
Duty cycle				13.3	%
Turns Ratio ($N_P:N_S$)			13		
Primary Winding Resistance ($R_{DC,PRI}$)	All windings open			891	mΩ
Primary Winding Resistance ($R_{DC,BIAS}$)				212	mΩ
Secondary Winding Resistance ($R_{DC,SEC1}$)				12	mΩ
Secondary Winding Resistance ($R_{DC,SEC2}$)				41	mΩ
Secondary Winding Resistance ($R_{DC,SEC3}$)				40	mΩ
Secondary Winding Resistance ($R_{DC,SEC4}$)				42	mΩ
Coupling capacitance	Primary side to bias side, Measured at 1 V_{PK-PK} , 100 kHz frequency, between pin 1 to pin 7, with pins 1 - 4 shorted and pins 7 - 8 shorted at 25 °C			15.8	pF
	Primary side to 14 VCC (Sec 1) side Measured at 1 V_{PK-PK} , 100 kHz frequency, between pin 1 to pin 9, with pins 1 - 4 shorted and pins 9 - 10 shorted at 25 °C			11.2	pF
	Primary side to 23 VCC (Sec 2) side Measured at 1 V_{PK-PK} , 100 kHz frequency, between pin 1 to pin 11, with pins 1 - 4 shorted and pins 11 - 12 shorted at 25 °C			7.9	pF
	Primary side to 23 VCC (Sec 3) side Measured at 1 V_{PK-PK} , 100 kHz frequency, between pin 1 to pin 13, with pins 1 - 4 shorted and pins 13 - 14 shorted at 25 °C			8.8	pF
	Primary side to 23 VCC (Sec 4) side Measured at 1 V_{PK-PK} , 100 kHz frequency, between pin 1 to pin 15, with pins 1 - 4 shorted and pins 15 - 16 shorted at 25 °C			9.2	pF
Primary inductance	Measured at 1 V_{PK-PK} , 100 kHz frequency, between node 1 to node 2, with all other windings open at 25 °C		436.7		μH
Part-to-part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between node 1 to node 2, with all other windings shorted.			9	μH

Table 5 – Transformer (T200) Electrical Specifications.

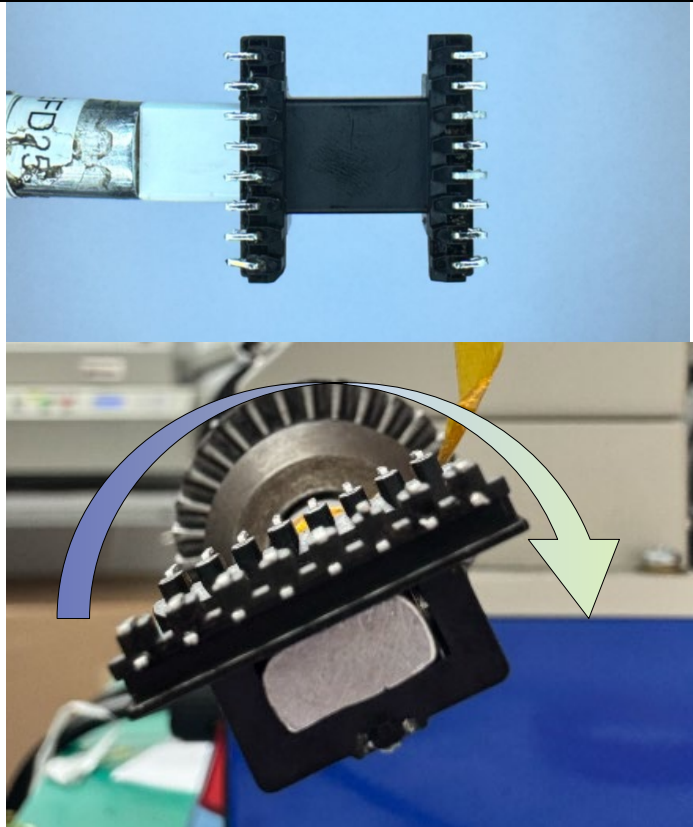
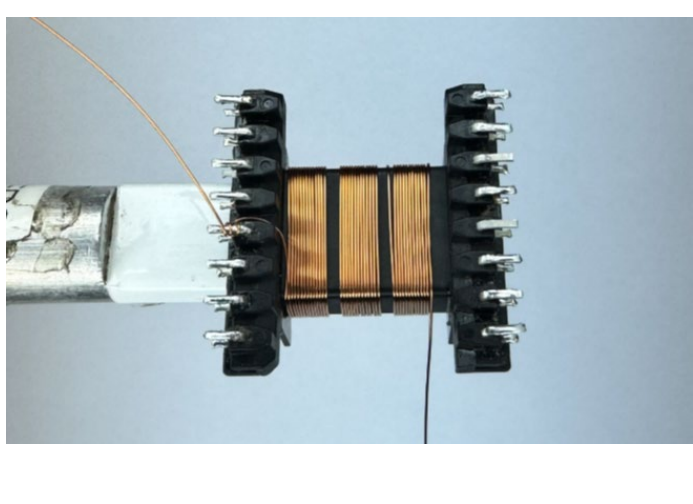


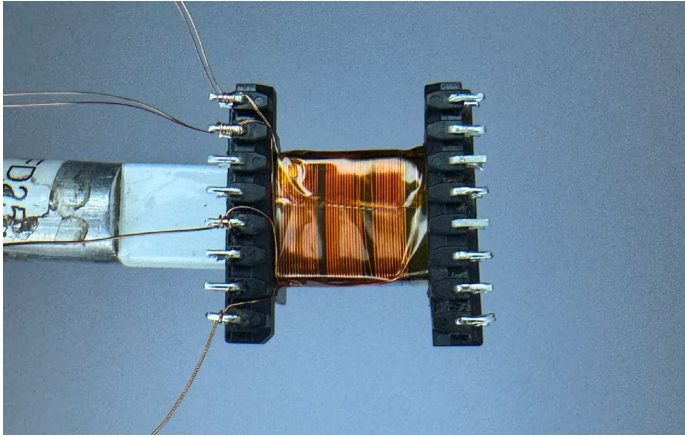
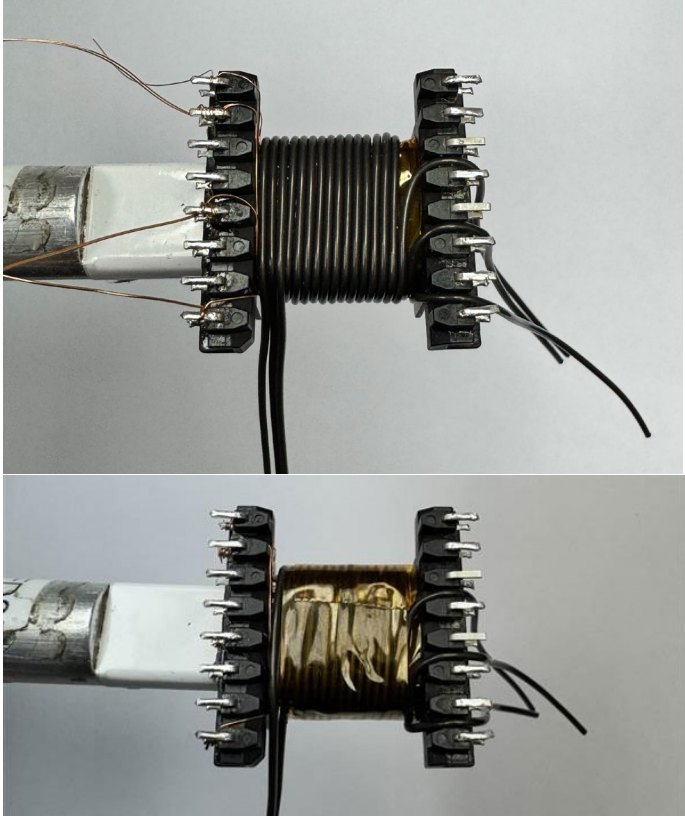
7.3 Material List

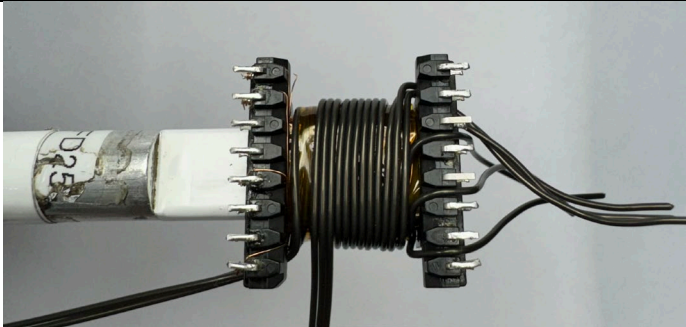
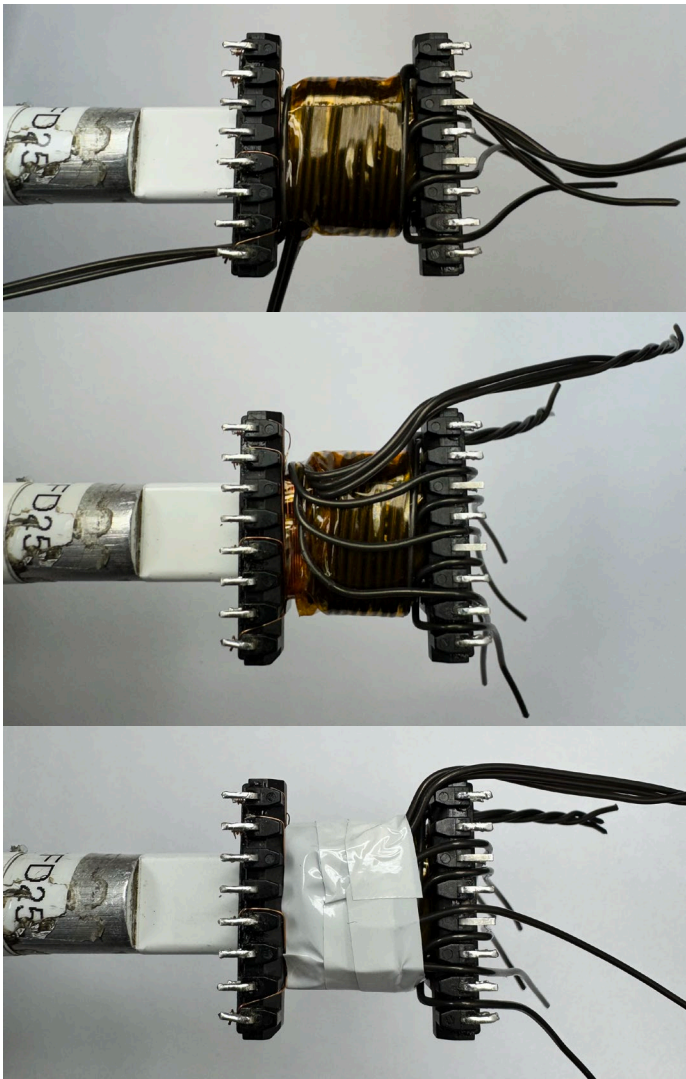
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Core: EFD25	2	PC	3C95 (or equivalent)	Ferroxcube
[2]	3M Polyimide Film Tape 5413, width: 0.625in (15.9mm)		mm	3M 5413 3/4" X 36YD (or equivalent)	3M
[3]	WD1 (Pri) 0.20 mm FIW 4, Class F	2600	mm	Copper Wire	Elektrisola
[4]	WD2 (Bias) 0.10 mm FIW 4, Class F	250	mm		Elektrisola
[5]	WD2 (Bias) 0.10 mm FIW 4, Class F	250	mm		Elektrisola
[6]	WD3 (14 VCC) T26A01PXXX-3	400	mm		Rubadue
[7]	WD3 (14 VCC) T26A01PXXX-3	400	mm		Rubadue
[8]	WD3 (14 VCC) T26A01PXXX-3	400	mm		Rubadue
[9]	WD3 (23 VCC) T26A01PXXX-3	500	mm		Rubadue
[10]	WD3 (23 VCC) T26A01PXXX-3	500	mm		Rubadue
[11]	WD3 (23 VCC) T26A01PXXX-3	500	mm		Rubadue

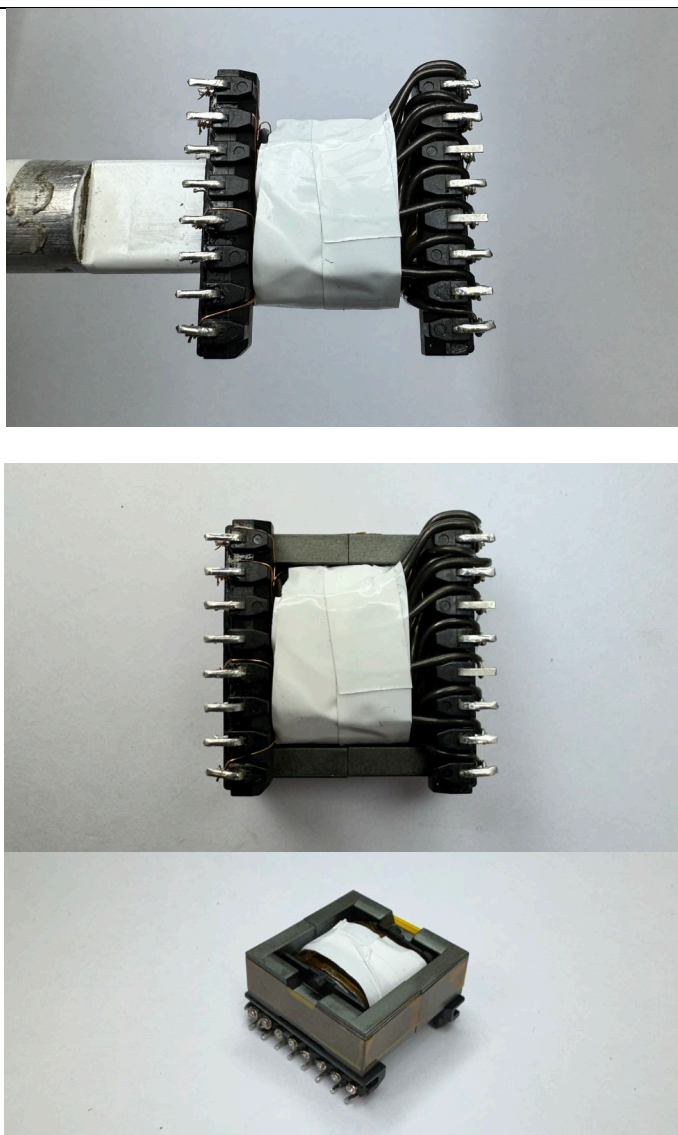
Table 6 – Transformer (T200) Material List.

7.4 Transformer Assembly Instructions

Transformer Assembly		#1 Position the bobbin on the mandrel such that the primary side (pins 1 and 4) is on the left side. Winding direction is clockwise direction.
WD1: Primary		#2 Route the start lead from pin 4 going to the bobbin thru slot 4 and then wind 39 turns of wire Item[3] with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Leave three spaces spread out evenly for the 3 turns of the bias winding. #3 The finish lead of the primary winding should be left unslotted for the mean time. Make sure the tension is still tight

WD2: Bias		#4 Route two filars of start lead of wire Item[4] from pin 7 from left to right with tight tension. Place the windings on the open spaces in between the primary winding. #5 Place 1 layer of tape Item[2] between the windings and the finish leads. #6 Terminate the finish lead of WD1 on pin 1 and the finish lead of WD2 on pin 8. Place 1 layer of tape Item[2].
WD3: Sec		#7 Place the Item[9-11] wires for the unregulated outputs on pins 12, 14, and 16. Wind the wires simultaneously for 5 turns. Place one layer of tape. #8 Place 3 filars of Item[6-8] on pin 10 for the regulated output secondary winding. Wind 3 turns. The finish lead should remain unslotted for the mean time.

		
Finishing		#9 Place 1 layer of tape Item[2] over the secondary windings. Terminate the finish leads of the unregulated output windings on pins 11, 13, and 15. Then, terminate the 3 filars of finish lead of the regulated output winding on pin 9. Place another layer of tape Item[2] over the windings.



8 Transformer Design Spreadsheet⁷

1	DCDC_InnoSwitch3AQ_Flyback_092324; Rev.4.0; Copyright Power Integrations 2024	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VOUT	14.00		14.00	V	Output Voltage
4	OPERATING CONDITION 1					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	0.714		0.714	A	Output current 1
7	POUT1			10.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	OPERATING CONDITION 2					
12	VINDC2	200.00		200.00	V	Input DC voltage 2
13	IOUT2	0.714		0.714	A	Output current 2
14	POUT2			10.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
67	TEMPERATURE_AMBIENT			40.0	°C	System ambient temperature
71	PRIMARY CONTROLLER SELECTION					
72	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
73	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
74	DEVICE_GENERIC			INN39X7		Device selection
75	DEVICE_CODE	INN3947FQ		INN3947FQ		Device code
76	PDEVICE_MAX			50	W	Device maximum power capability
77	RDSON_25DEG			1.53	Ω	Primary switch on-time resistance at 25 °C
78	RDSON_125DEG			3.12	Ω	Primary switch on-time resistance at 125 °C
79	ILIMIT_MIN			1.488	A	Primary switch minimum current limit
80	ILIMIT_TYP			1.600	A	Primary switch typical current limit
81	ILIMIT_MAX			1.712	A	Primary switch maximum current limit
82	VDRAIN_ON_PRSW			0.17	V	Primary switch on-time voltage drop
83	VDRAIN_OFF_PRSW			1212	V	Peak drain voltage on the primary switch during turn-off at maximum input DC voltage and allowable leakage ring
84	VCLAMP			212.0	V	Voltage across clamp circuit
85	CU_AREA_INNO			1.00	in ²	Primary switch copper cooling area
86	TEMP_INNO_MIN			49.98	°C	Device minimum operating temperature with respect to ambient, observed at 1000 V VINDC
87	TEMP_INNO_MAX			50.93	°C	Device maximum operating temperature with respect to ambient, observed at 200 V VINDC
88						
91	WORST CASE ELECTRICAL PARAMETERS					
92	FSWITCHING_MAX	35000		35000	Hz	Maximum switching frequency at full load and minimum DC input voltage
93	VOR	182.0		182.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
94	KP			9.122		Measure of continuous/discontinuous mode of operation
95	MODE_OPERATION			DCM		Mode of operation
96	DUTYCYCLE			0.091		Primary switch duty cycle
97	TIME_ON_MIN		Info	0.565	us	Minimum primary switch on-time has been capped at 565ns

⁷ All warnings may be ignored since a 400 V rated diode were used as secondary rectifier instead of MOSFETs for the unregulated outputs.



98	TIME_ON_MAX			2.97	us	Maximum primary switch on-time
99	TIME_OFF			26.03	us	Primary switch off-time
100	LPRIMARY_MIN			414.8	uH	Minimum primary magnetizing inductance
101	LPRIMARY_TYP			436.7	uH	Typical primary magnetizing inductance
102	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
103	LPRIMARY_MAX			458.5	uH	Maximum primary magnetizing inductance
105	PRIMARY CURRENT					
106	IAVG_PRIMARY			0.054	A	Primary switch average current
107	IPEAK_PRIMARY			1.362	A	Primary switch peak current
108	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
109	IRIPPLE_PRIMARY			1.362	A	Primary switch ripple current
110	IRMS_PRIMARY			0.219	A	Primary switch RMS current
114	TRANSFORMER CONSTRUCTION PARAMETERS					
115	CORE SELECTION					
116	CORE	EFD25		EFD25		Core selection
117	CORE NAME			EFD25/13/9-3C96		Core code
118	AE			58.0	mm^2	Core cross sectional area
119	LE			57.0	mm	Core magnetic path length
120	AL			2000	nH	Ungapped core effective inductance per turns squared
121	VE			3300	mm^3	Core volume
122	BOBBIN NAME			EFD25/13/9-2 (P5-S5)		Bobbin name
123	AW			40.2	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
124	BW			16.40	mm	Bobbin width
125	BH			3.11	mm	Bobbin height
126	MARGIN			0.0	mm	Bobbin safety margin
128	PRIMARY WINDING					
129	NPRIMARY			39		Primary winding number of turns
130	BPEAK			3552	Gauss	Peak flux density
131	BMAX			2628	Gauss	Maximum flux density
132	BAC			1314	Gauss	AC flux density (0.5 x Peak to Peak)
133	ALG			287	nH	Typical gapped core effective inductance per turns squared
134	LG			0.217	mm	Core gap length
136	SECONDARY WINDING					
137	NSECONDARY	3		3		Secondary winding number of turns
139	BIAS WINDING					
140	NBIAS			3		Bias winding number of turns
144	PRIMARY COMPONENTS SELECTION					
145	LINE UNDERVOLTAGE/OVERVOLTAGE					
146	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
147	UNDERVOLTAGE PARAMETERS					
148	BROWN-IN REQUIRED			190.00	V	Required DC bus brown-in voltage threshold
149	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
150	VZ			9.10	V	Zener diode reverse voltage
151	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
152	ILKG			2.00	uA	Zener diode maximum reverse leakage current (at high ambient temperatures, typically 125 °C)



153	ILKG_MIN			0.10	uA	Zener diode minimum reverse leakage current (at low ambient temperatures, typically 25 °C)
154	BROWN-IN ACTUAL			127.96 - 189.94	V	Actual brown-in voltage range using standard resistors considering tolerances due to part and temperature variations
155	BROWN-OUT ACTUAL			114.26 - 170.13	V	Actual brown-out voltage range using standard resistors considering tolerances due to part and temperature variations
156	OVERVOLTAGE PARAMETERS					
157	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
158	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
159	VF				V	OV diode forward voltage
160	VRRM				V	OV diode reverse voltage
161	PIV				V	OV diode peak inverse voltage
162	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
163 DC BUS SENSE RESISTORS						
164	RLS_H			5.64	MΩ	Connect seven 806 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
165	RLS_L			124.00	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
168 BIAS WINDING						
169	VBIAS			9.00	V	Rectified bias voltage
170	VF_BIAS			0.70	V	Bias winding diode forward drop
171	VREVERSE_BIASDIODE			85.92	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
172	CBIAS			22	uF	Bias winding rectification capacitor
173	CBPP			0.47	uF	BPP pin capacitor
177 SECONDARY COMPONENTS SELECTION						
178 FEEDBACK COMPONENTS						
179	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
180	RFB_LOWER			10.00	kΩ	Lower feedback resistor
181	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
185 MULTIPLE OUTPUT PARAMETERS						
186 OUTPUT 1						
187	VOUT1			14.00	V	Output 1 voltage
188	IOUT1			0.714	A	Output 1 current
189	POUT1			10.00	W	Output 1 power
190	IRMS_SECONDARY1			3.028	A	Root mean squared value of the secondary current for output 1
191	IRIPPLE_CAP_OUTPUT1			2.943	A	Current ripple on the secondary waveform for output 1
192	NSECONDARY1			3		Number of turns for output 1
193	VREVERSE_RECTIFIER1			90.92	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
194	SRFET1	DMT15H01 7LPS-13		DMT15H01 7LPS-13		Secondary rectifier (Logic MOSFET) for output 1
195	NUM_SRFET1	1		1		Number of SRFETs in parallel for output 1
196	VF_SRFET1			0.80	V	SRFET typical on-time drain voltage for output 1
197	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
198	RDSON_SRFET1			37.0	mΩ	SRFET estimated on-time drain resistance at 100°C and VGS=4.4V for output 1
199	RTHJA_SRFET1			53.00	°C/W	SRFET max. thermal impedance for output 1



200	TEMP_SRFET1_MIN			57.4	°C	SRFET minimum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 200 V VINDC
201	TEMP_SRFET1_MAX			59.3	°C	SRFET maximum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 1000 V VINDC
203	OUTPUT 2					
204	VOU2	23.00		23.00	V	Output 2 voltage
205	IOUT2	0.087		0.087	A	Output 2 current
206	POU2			2.00	W	Output 2 power
207	IRMS_SECONDARY2			0.369	A	Root mean squared value of the secondary current for output 2
208	IRIPPLE_CAP_OUTPUT2			0.359	A	Current ripple on the secondary waveform for output 2
209	NSECONDARY2			5		Number of turns for output 2
210	VREVERSE_RECTIFIER2		Warning ⁸	151.21	V	Taking into consideration the parasitic voltage ring and assuming this output is connected to the Vo/FWD pin, then the actual stress across the SRFET/FWD pin would be 198.46 V. Given that the absolute maximum FWD pin voltage rating is 150 V, increase the VO
211	SRFET2	AUTO	Info	SQJ454EP		Expected voltage stress (including parasitic ring) has exceeded the 85% derating of 170 V: consider replacing with higher voltage rated MOSFET or increase VoR.
212	NUM_SRFET2	1		1		Number of SRFETS in parallel for output 2
213	VF_SRFET2			0.83	V	SRFET typical on-time drain voltage for output 2
214	VBREAKDOWN_SRFET2			200	V	SRFET breakdown voltage for output 2
215	RDSON_SRFET2			217.5	mΩ	SRFET on-time drain resistance at 100 °C and VGS=4.4 V for output 2
216	RTHJA_SRFET2			68.00	°C/W	SRFET max. thermal impedance for output 2
217	TEMP_SRFET2_MIN			44.8	°C	SRFET minimum operating temperature for output 2 (for each SRFET in parallel) with respect to ambient, observed at 1000 V VINDC
218	TEMP_SRFET2_MAX			45.4	°C	SRFET maximum operating temperature for output 2 (for each SRFET in parallel) with respect to ambient, observed at 200V VINDC
220	OUTPUT 3					
221	VOU3	23.00		23.00	V	Output 3 voltage
222	IOUT3	0.087		0.087	A	Output 3 current
223	POU3			2.00	W	Output 3 power
224	IRMS_SECONDARY3			0.369	A	Root mean squared value of the secondary current for output 3
225	IRIPPLE_CAP_OUTPUT3			0.359	A	Current ripple on the secondary waveform for output 3
226	NSECONDARY3			5		Number of turns for output 3
227	VREVERSE_RECTIFIER3		Warning	151.21	V	Taking into consideration the parasitic voltage ring and assuming this output is connected to the Vo/FWD pin, then the actual stress across the SRFET/FWD pin would be 198.46 V. Given that the absolute maximum FWD pin voltage rating is 150 V, increase the VO
228	SRFET3	AUTO	Info	SQJ454EP		Expected voltage stress (including parasitic ring) has exceeded the 85% derating of 170

⁸ There is no option in PI XIs to choose a 400 V diode for the secondary rectifier. This warning must be ignored.



						V: consider replacing with higher voltage rated MOSFET or increase VoR.
229	NUM_SRFET3	1		1		Number of SRFETS in parallel for output 3
230	VF_SRFET3			0.83	V	SRFET typical on-time drain voltage for output 3
231	VBREAKDOWN_SRFET3			200	V	SRFET breakdown voltage for output 3
232	RDSON_SRFET3			217.5	mΩ	SRFET on-time drain resistance at 100 °C and VGS=4.4 V for output 3
233	RTHJA_SRFET3			68.00	°C/W	SRFET max. thermal impedance for output 3
234	TEMP_SRFET3_MIN			44.8	°C	SRFET minimum operating temperature for output 3 (for each SRFET in parallel) with respect to ambient, observed at 200 V VINDC
235	TEMP_SRFET3_MAX			45.4	°C	SRFET minimum operating temperature for output 3 (for each SRFET in parallel) with respect to ambient, observed at 1000 V VINDC
236	OUTPUT 4					
237	VOU4	23.00		23.00	V	Output 4 voltage
238	IOU4	0.087		0.087	A	Output 4 current
239	POU4			2.00	W	Output 4 power
240	IRMS_SECONDARY4			0.369	A	Root mean squared value of the secondary current for output 4
241	IRIPPLE_CAP_OUTPUT4			0.359	A	Current ripple on the secondary waveform for output 4
242	NSECONDARY4			5		Number of turns for output 4
243	VREVERSE_RECTIFIER4		Warning	151.21	V	Taking into consideration the parasitic voltage ring and assuming this output is connected to the Vo/FWD pin, then the actual stress across the SRFET/FWD pin would be 198.46 V. Given that the absolute maximum FWD pin voltage rating is 150V, increase the VO
244	SRFET4	AUTO	Info	SQJ454EP		Expected voltage stress (including parasitic ring) has exceeded the 85% derating of 170V: consider replacing with higher voltage rated MOSFET or increase VoR.
245	NUM_SRFET4	1		1		Number of SRFETS in parallel for output 4
246	VF_SRFET4			0.83	V	SRFET typical on-time drain voltage for output 4
247	VBREAKDOWN_SRFET4			200	V	SRFET breakdown voltage for output 4
248	RDSON_SRFET4			217.5	mΩ	SRFET on-time drain resistance at 100 °C and VGS=4.4 V for output 4
249	RTHJA_SRFET4			68.00	°C/W	SRFET max. thermal impedance for output 4
250	TEMP_SRFET4_MIN			44.8	°C	SRFET minimum operating temperature for output 4 (for each SRFET in parallel) with respect to ambient, observed at 200 V VINDC
251	TEMP_SRFET4_MAX			45.4	°C	SRFET minimum operating temperature for output 4 (for each SRFET in parallel) with respect to ambient, observed at 1000 V VINDC
252	PO_TOTAL		Info	16.00	W	The total power of all outputs does not add up to the total power of the design
253	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Table 7 – RDR-1045Q PIXIs Spreadsheet.



9 Performance data

- Note:** 1. Measurements were taken with the unit-under-test positioned in a thermal chamber.
2. The RDR-1045Q board was placed in a box inside the thermal chamber to eliminate the effects of airflow.

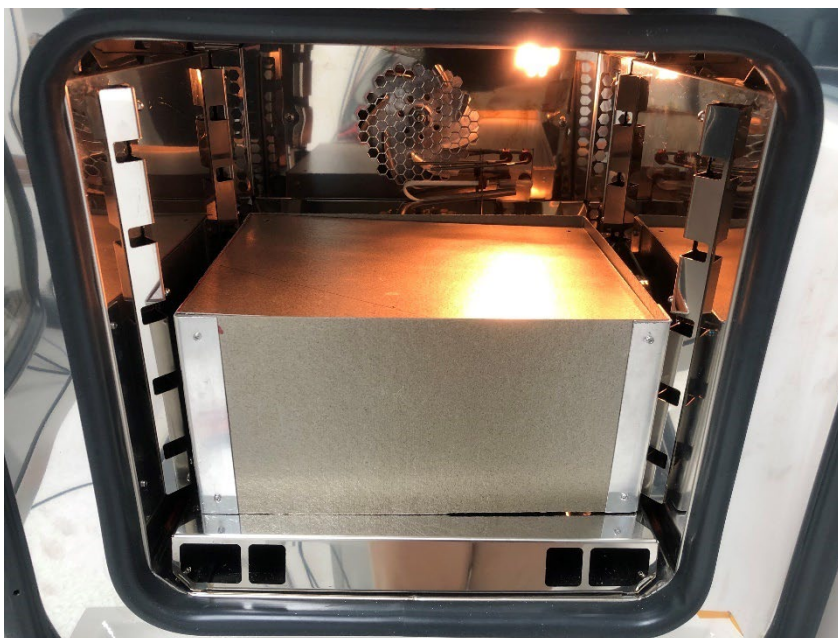


Figure 14 – Unit under test placed inside a box to eliminate the effect of airflow.

3. For each loading condition, the RDR-1045Q test board was allowed to stabilize for 1 minute before measurements were taken.

4. List of Equipment Used for Testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	HP _P 20 757 152	2 kV / 750 mA / 1.5 kW Programmable DC PSU	BK Precision
Electronic Load	PEL-2002A	80 V / 20 A / 100 W DC ELoad	GW Instek
Power Meter	66205	600 V / 30 A Digital Power Meter	Chroma
Power Meter	WT310E	600 V / 20 A Digital Power Meter	Yokogawa
High-Voltage Measurement	TT-SI 9010A	70 MHz 7000 V Differential Probe	Testec
High-Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low-Voltage Measurement	PHT 312	400 V Passive Probe Extended Temperature	PMK
Low-Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Current Measurement	701928	100 MHz 30 A _{rms} Current Probe	Yokogawa
Current Measurement	CWTUM/015/B	30 MHz 30 A _{peak} Rogowski Coil	CWT
Current Measurement	CWTUM/06/R	30 MHz 120 A _{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20-Channel Data Logger	Graphtec
Thermal Image	TiX580	1000 °C Thermal Imaging Camera	Fluke
Thermal Chamber	SH-242	Temperature & Humidity Chamber	Espec
Oscilloscope	DLM5058	2.5 GS/s 500 MHz Mixed Signal	Yokogawa

Table 8 – List of Equipment Used for Testing.

9.1 No-Load Input Power

Figure 15 shows the test circuit used for no-load input power measurement. The voltmeter was placed before the ammeter; this was done to prevent the voltmeter bias current from affecting the input current measurements. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

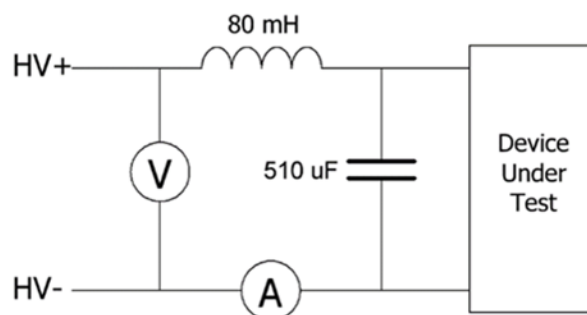


Figure 15 – No-Load Input Power Measurement Diagram.

The unit was allowed to stabilize for ten minutes for each test before measurements were started. The leakage current through the DC-Link capacitor was also measured before testing and was subtracted from the measured no-load input current. The average voltage across the inductor was assumed to be negligible due to the inductor's very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible since the input current was DC.

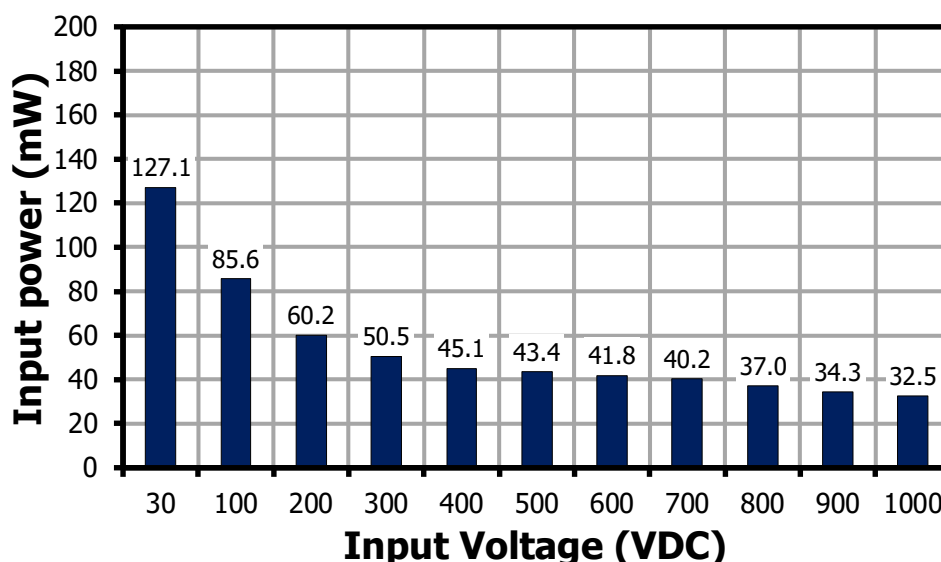


Figure 16 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Efficiency Across Line

Efficiency across line describes how input voltage affects the unit's overall efficiency. The points in the graph were taken at 100% load.

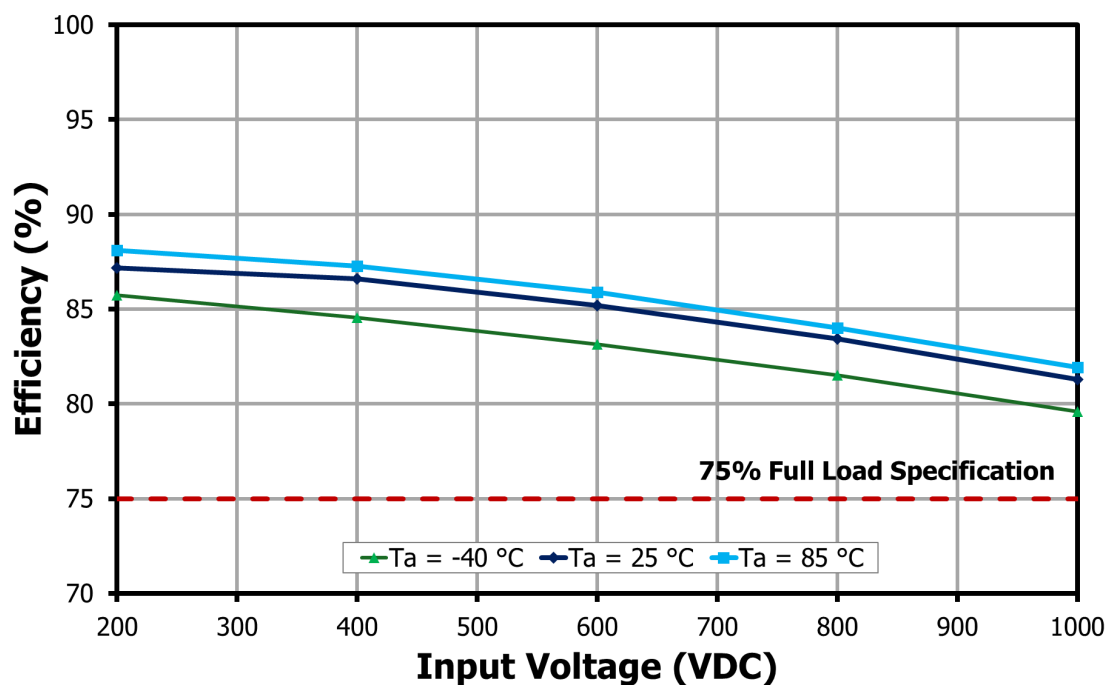


Figure 17 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Efficiency Across Load

Efficiency across load describes how output loading affects the overall efficiency of the power supply. Each line on the graph represents the efficiency vs. load percentage of the specific output terminal under test. For the three 23 V outputs, only one output (VOUT2) was chosen to represent the unregulated output voltage performance. Both the 14 V and 23V output load were varied from minimum to maximum loading condition. All 23 V outputs have the same loading.

9.2.2.1 Efficiency Across Load at -40 °C Ambient

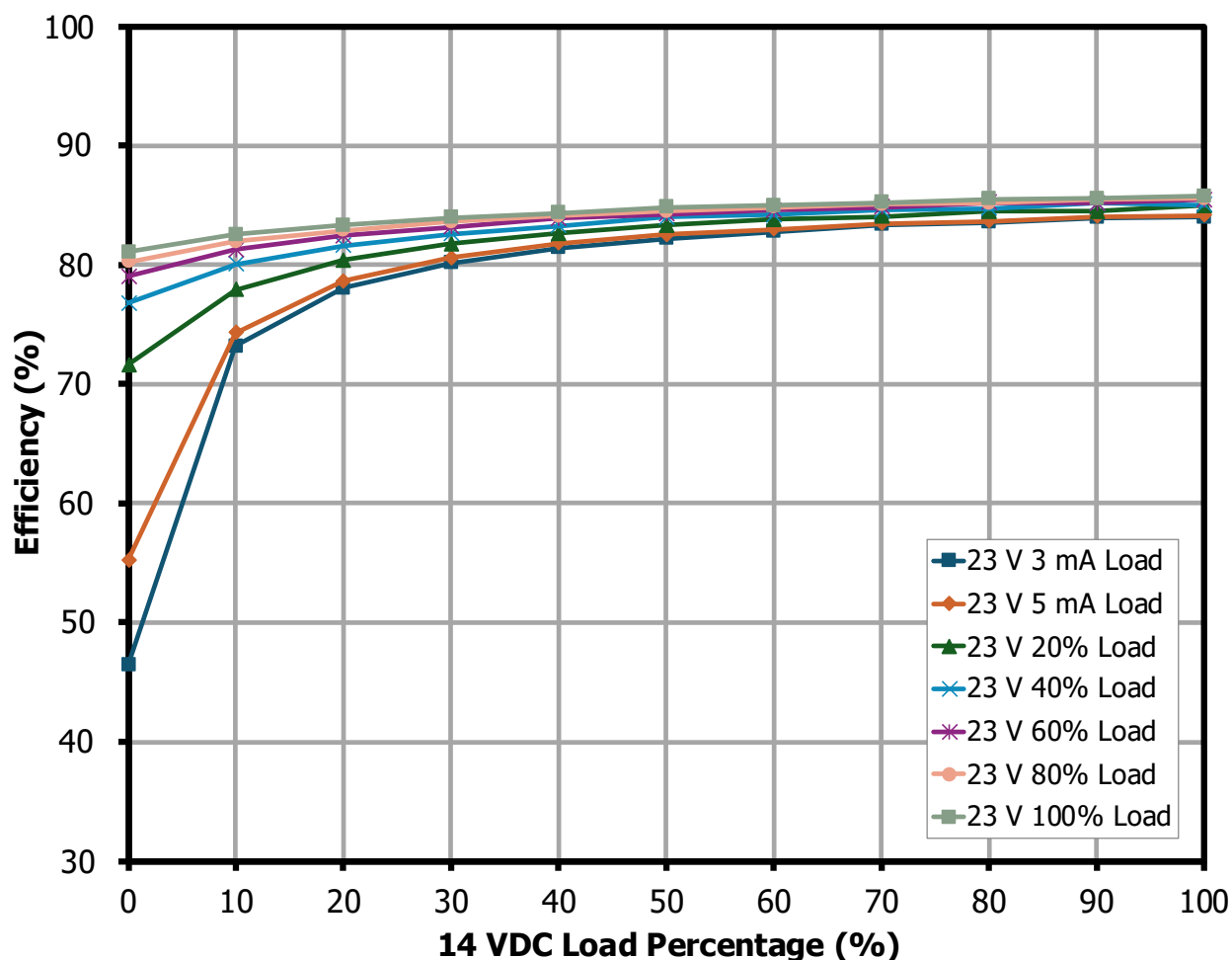


Figure 18 – Efficiency vs. Load at 200 V Input Voltage (-40 °C Ambient).

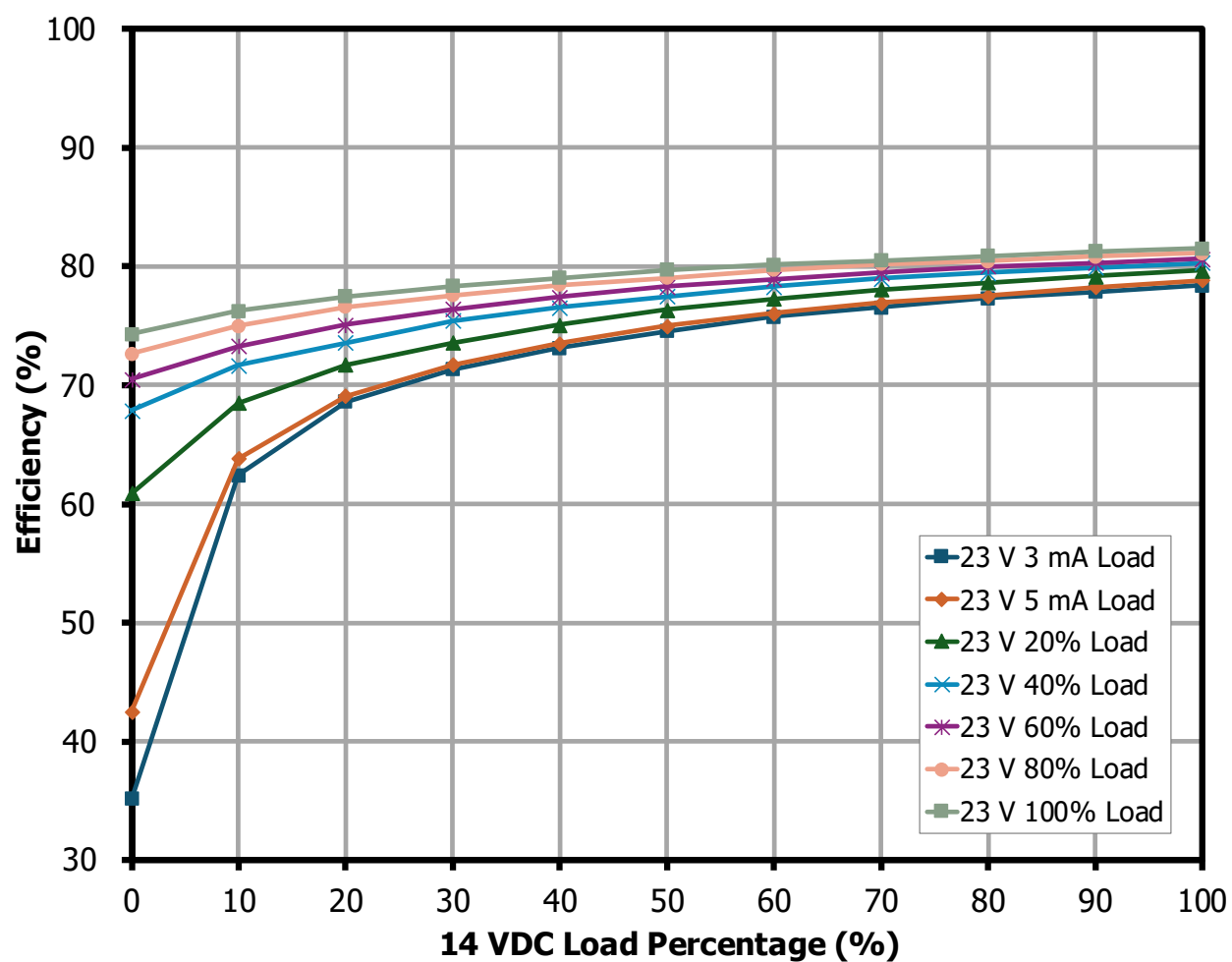


Figure 19 – Efficiency vs. Load at 800 V Input Voltage (-40 °C Ambient).

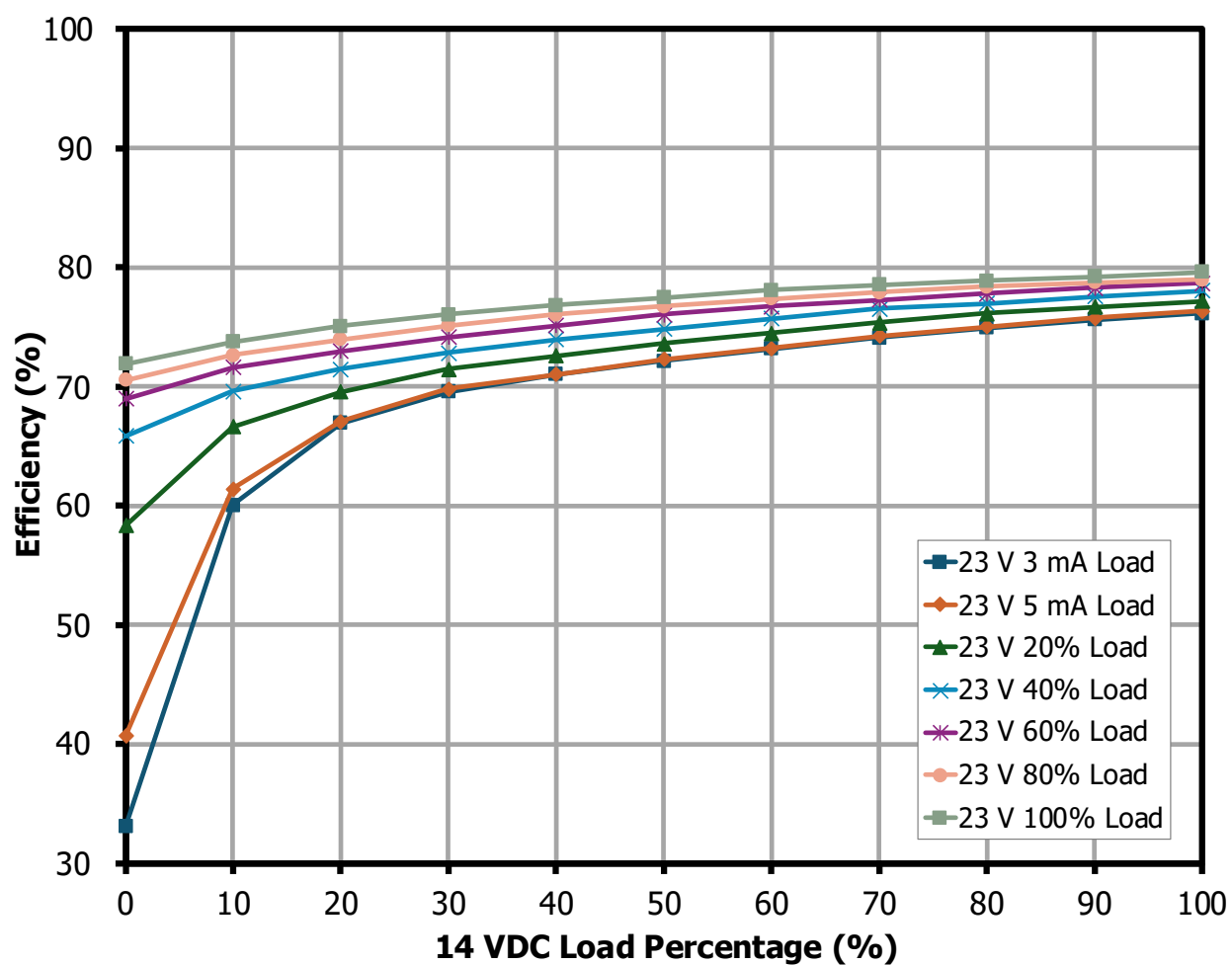


Figure 20 – Efficiency vs. Load at 1000 V Input Voltage (-40 °C Ambient).

9.2.2.2 Efficiency Across Load at 25 °C Ambient

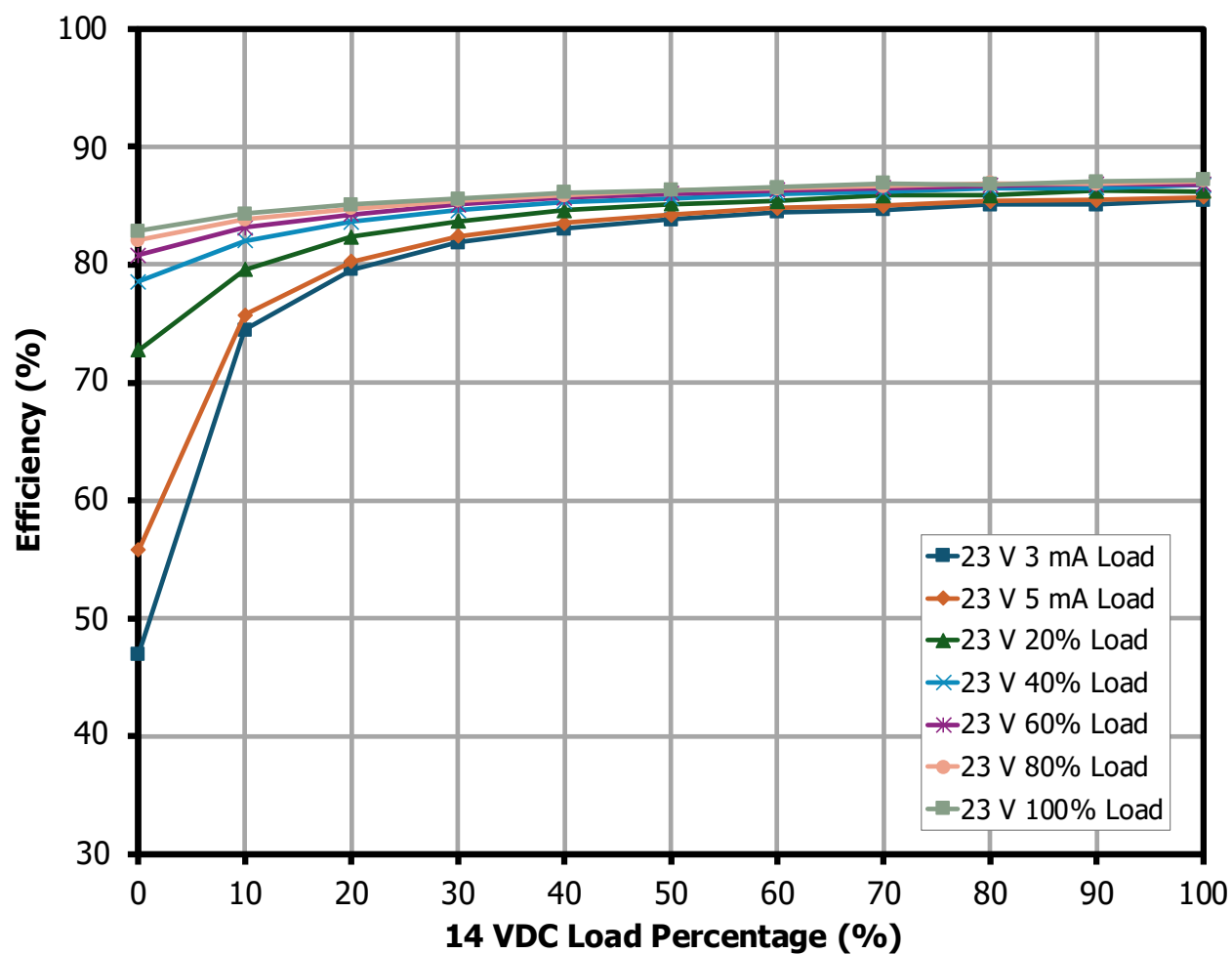


Figure 21 – Efficiency vs. Load at 200 V Input Voltage (25 °C Ambient).

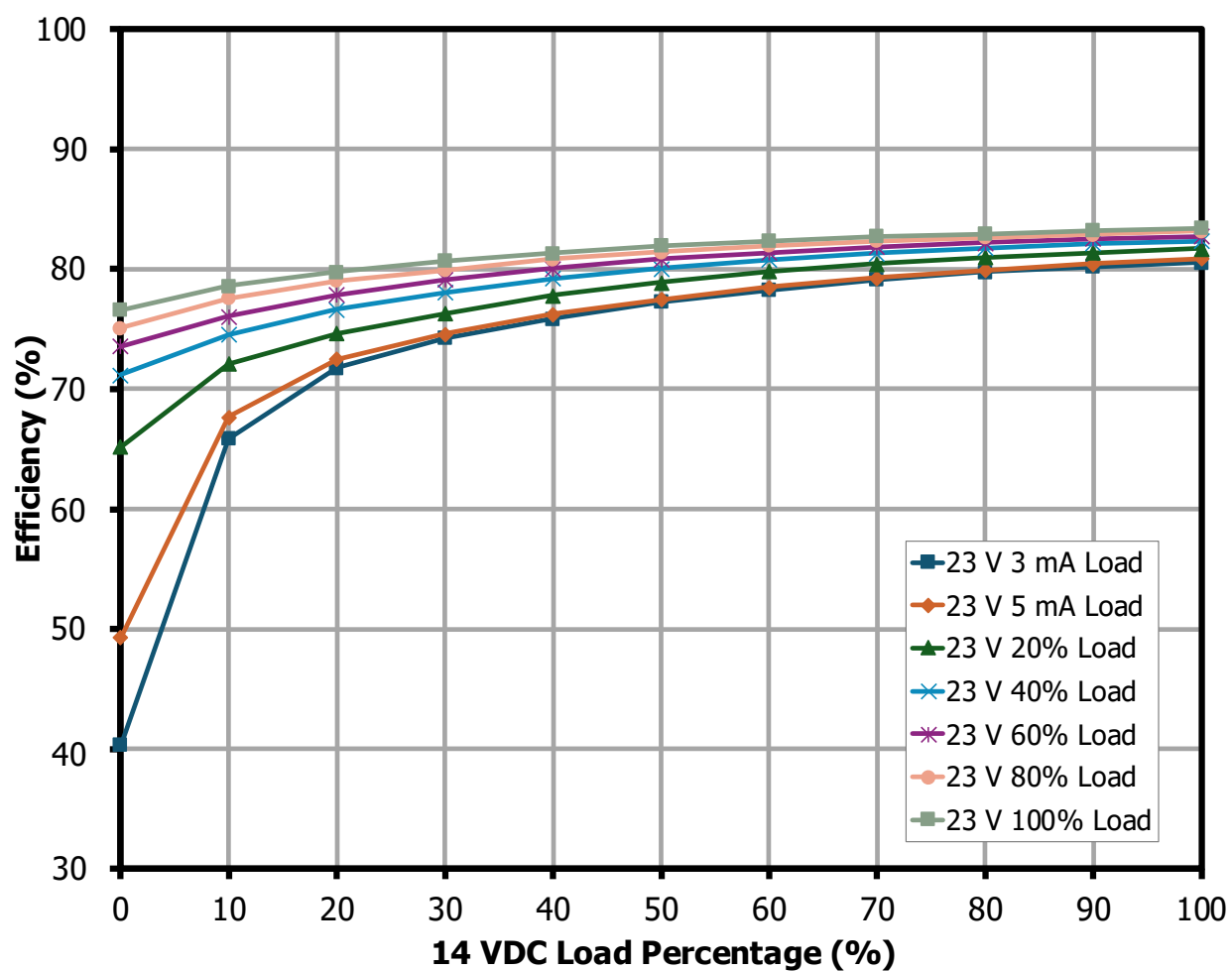


Figure 22 – Efficiency vs. Load at 800 V Input Voltage (25 °C Ambient).

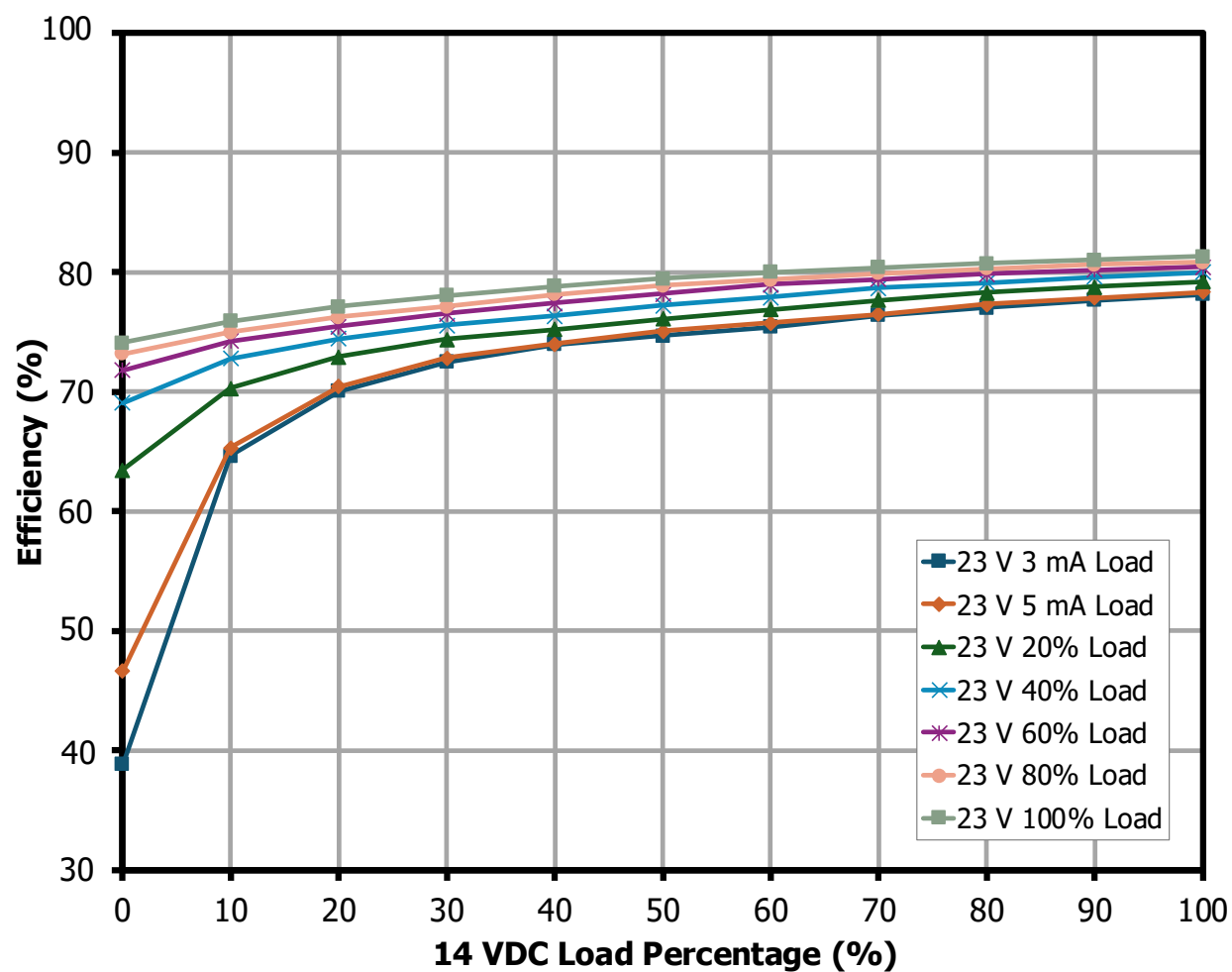


Figure 23 – Efficiency vs. Load at 1000 V Input Voltage (25 °C Ambient).

9.2.2.1 Efficiency Across Load at 85 °C Ambient

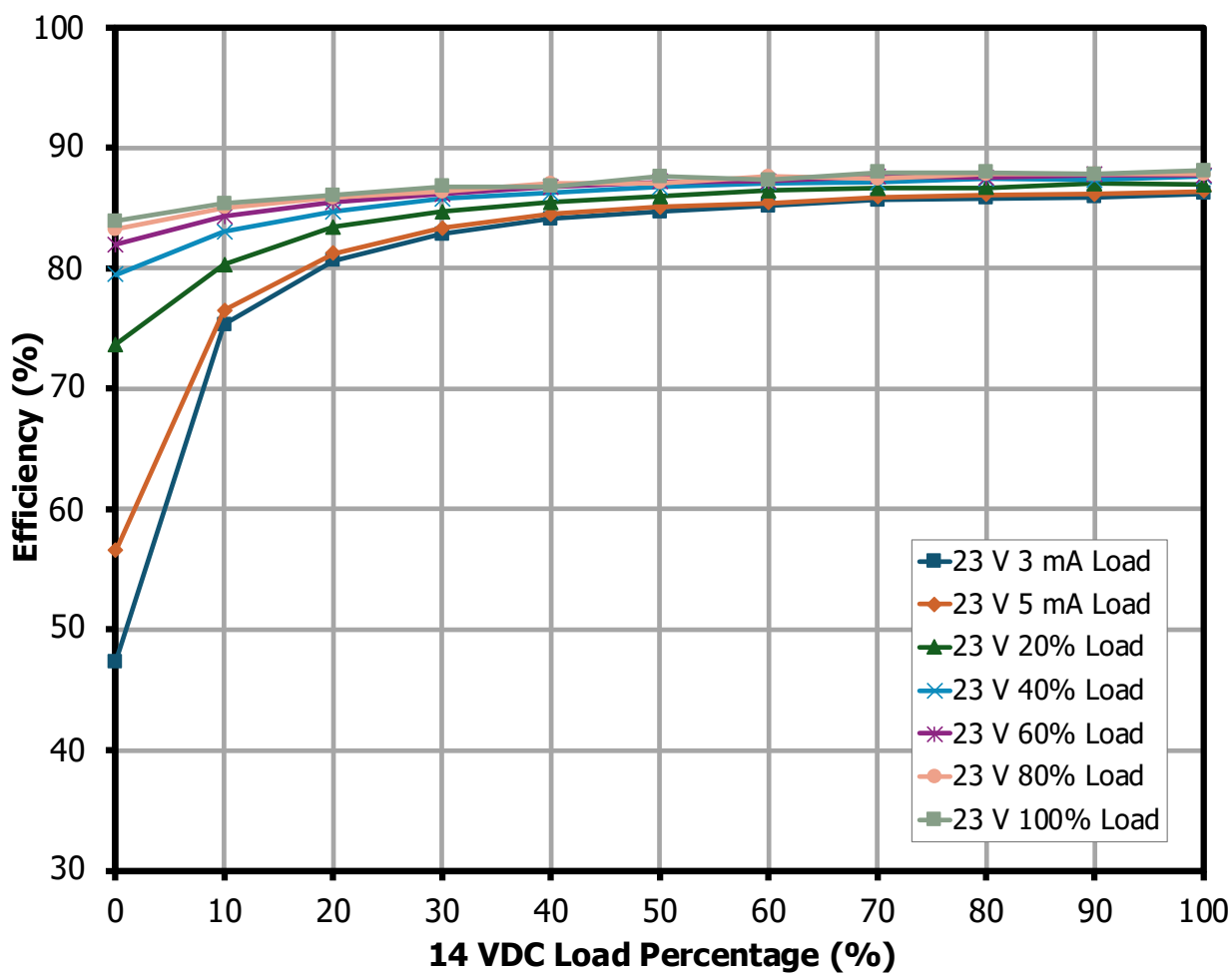


Figure 24 – Efficiency vs. Load at 200 V Input Voltage (85 °C Ambient).

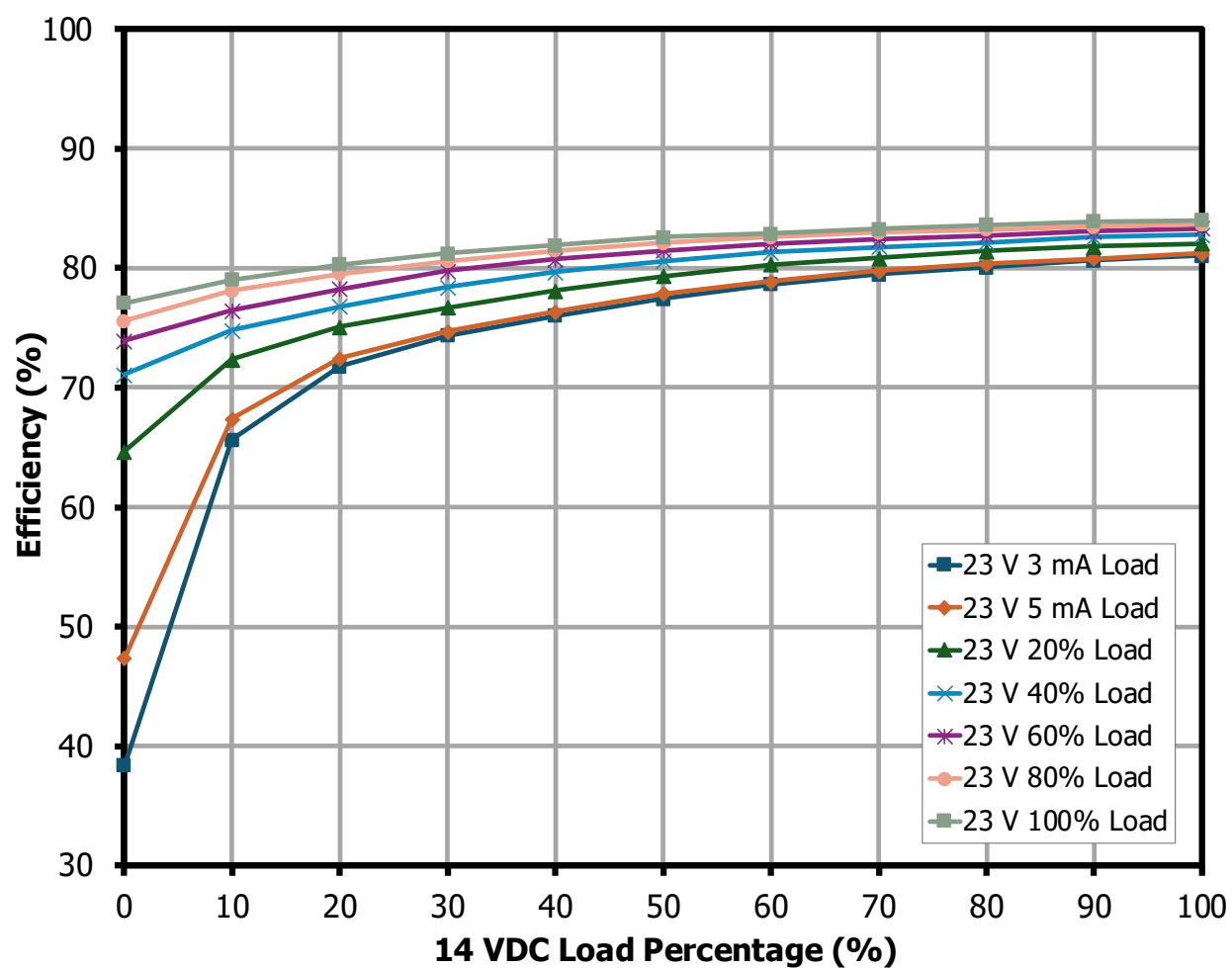


Figure 25 – Efficiency vs. Load at 800 V Input Voltage (85 °C Ambient).

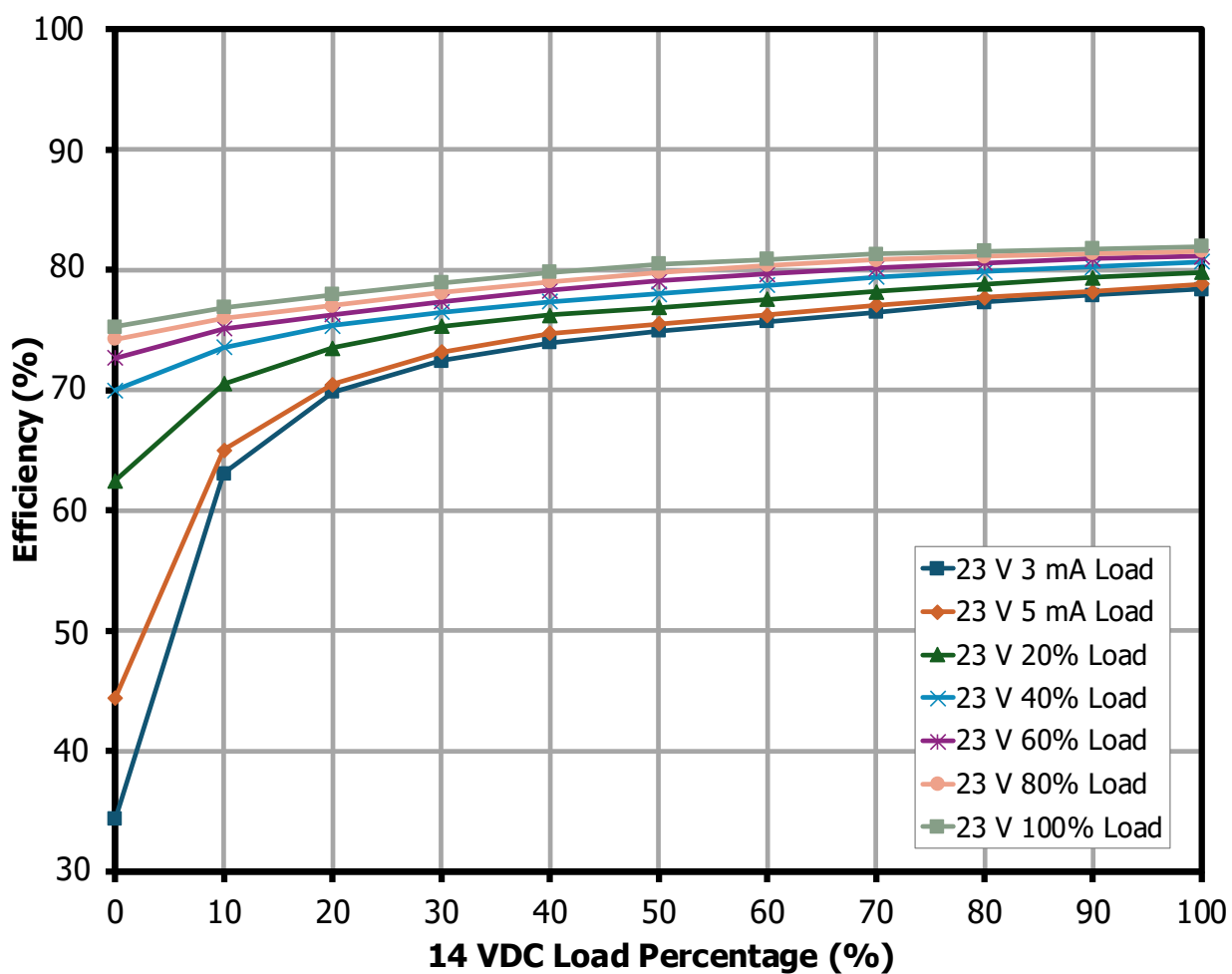


Figure 26 – Efficiency vs. Load at 1000 V Input Voltage (85 °C Ambient).

9.3 Line and Load Regulation

9.3.1 Load Regulation

Load regulation describes how a change in load affects output voltage. Each line on the graph represents the load regulation vs. the load percentage of the specific output under test. For the three 23 VDC outputs, only one output (V_{OUT2}) was chosen to represent the load regulation. Both the 14 VDC and 23 VDC output loads were varied.

9.3.1.1 Load Regulation at -40 °C Ambient

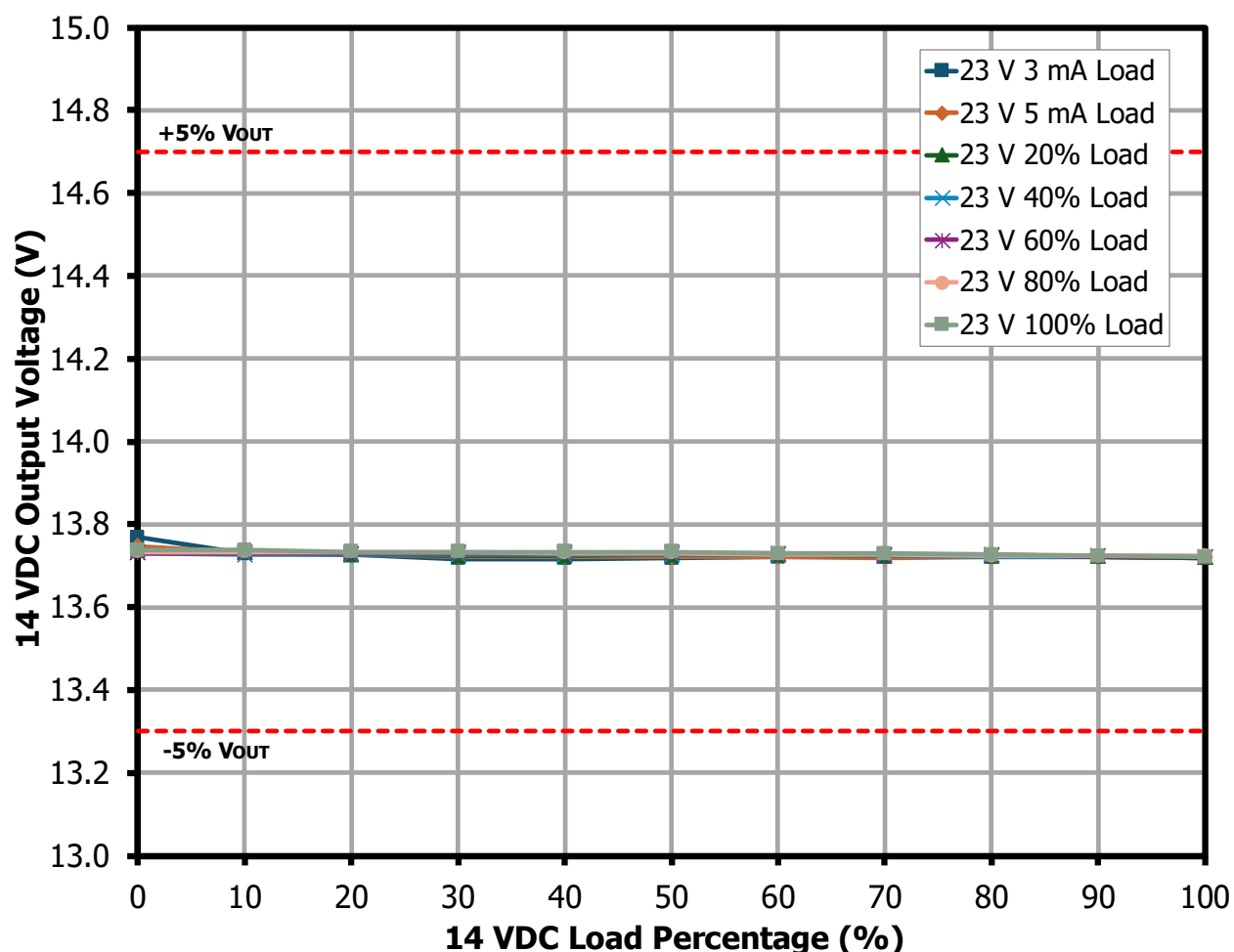


Figure 27 – 14 VDC Output Regulation vs. Load at 200 V Input Voltage (-40 °C Ambient).

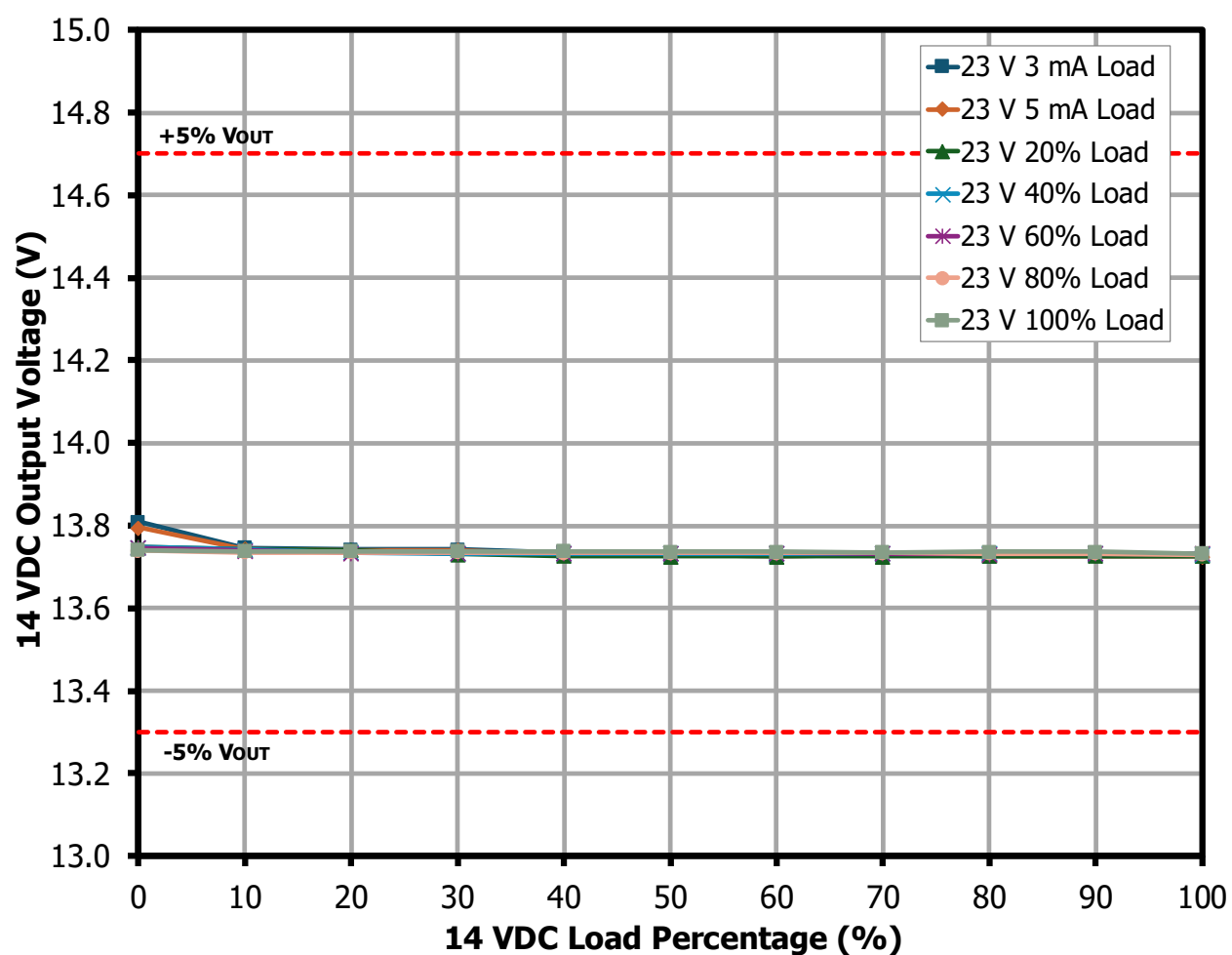


Figure 28 – 14 VDC Output Regulation vs. Load at 800 V Input Voltage (-40 °C Ambient).

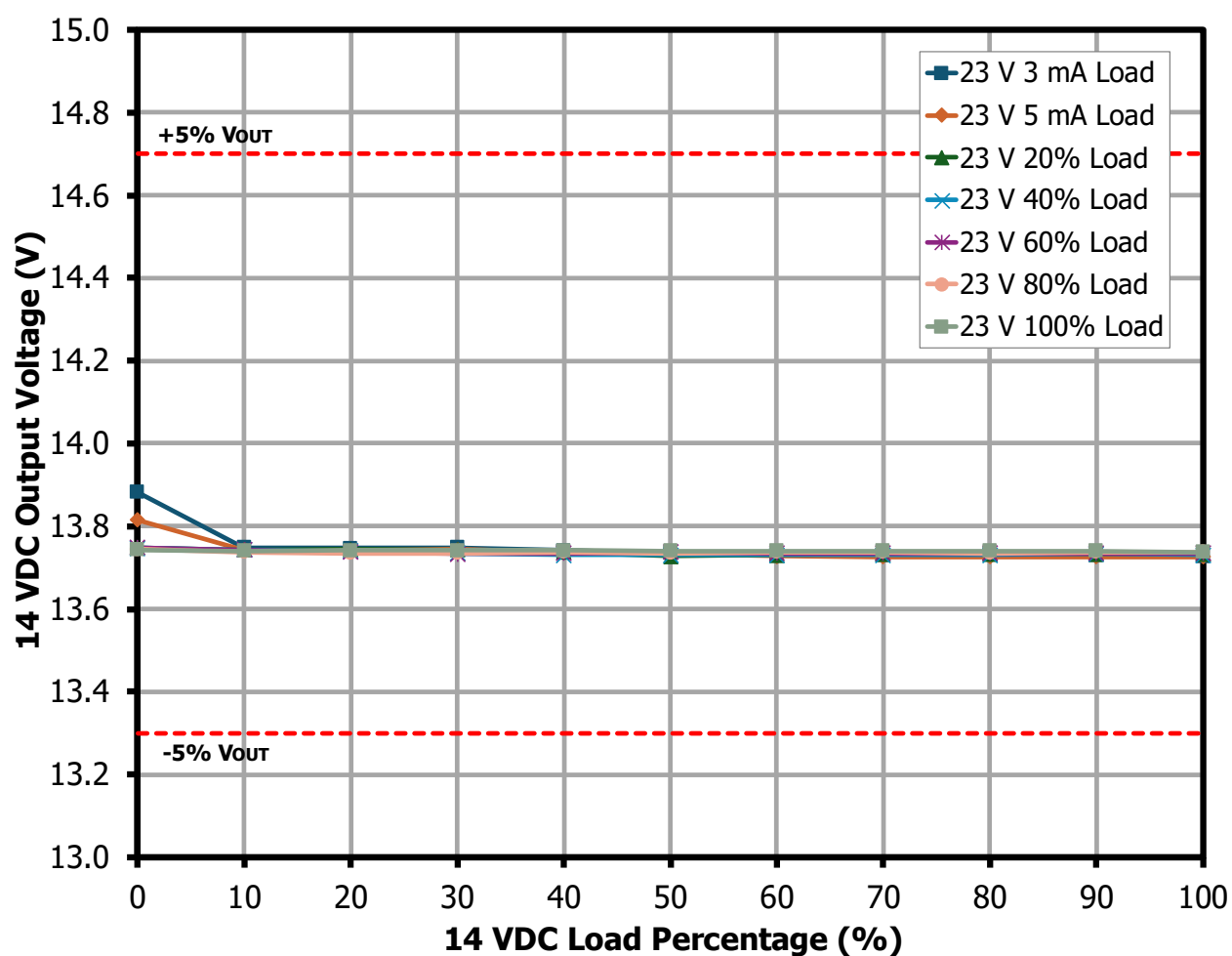


Figure 29 – 14 VDC Output Regulation vs. Load at 1000 V Input Voltage (-40 °C Ambient).

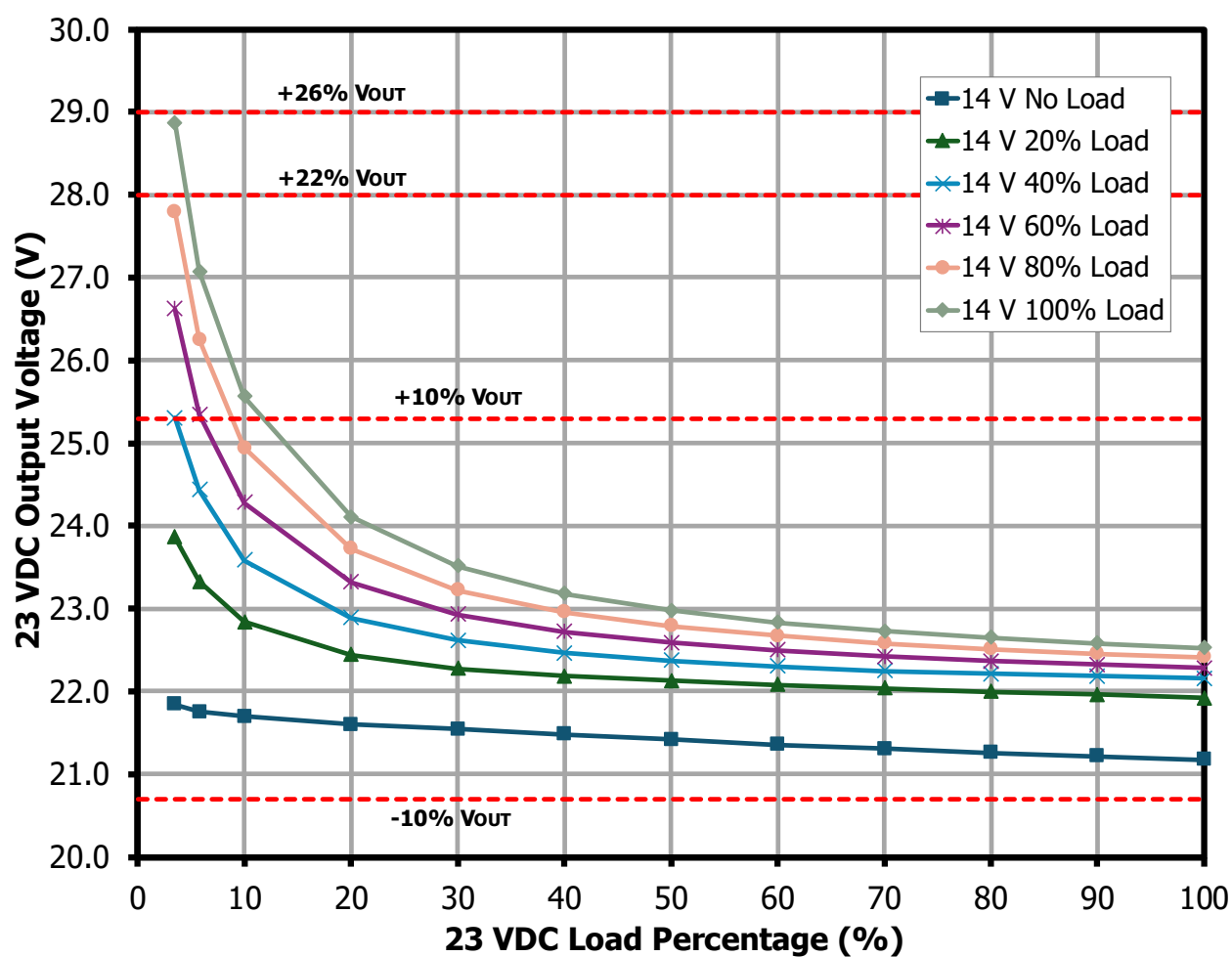


Figure 30 – 23 VDC Output Regulation vs. Load at 200 V Input Voltage (-40 °C Ambient).

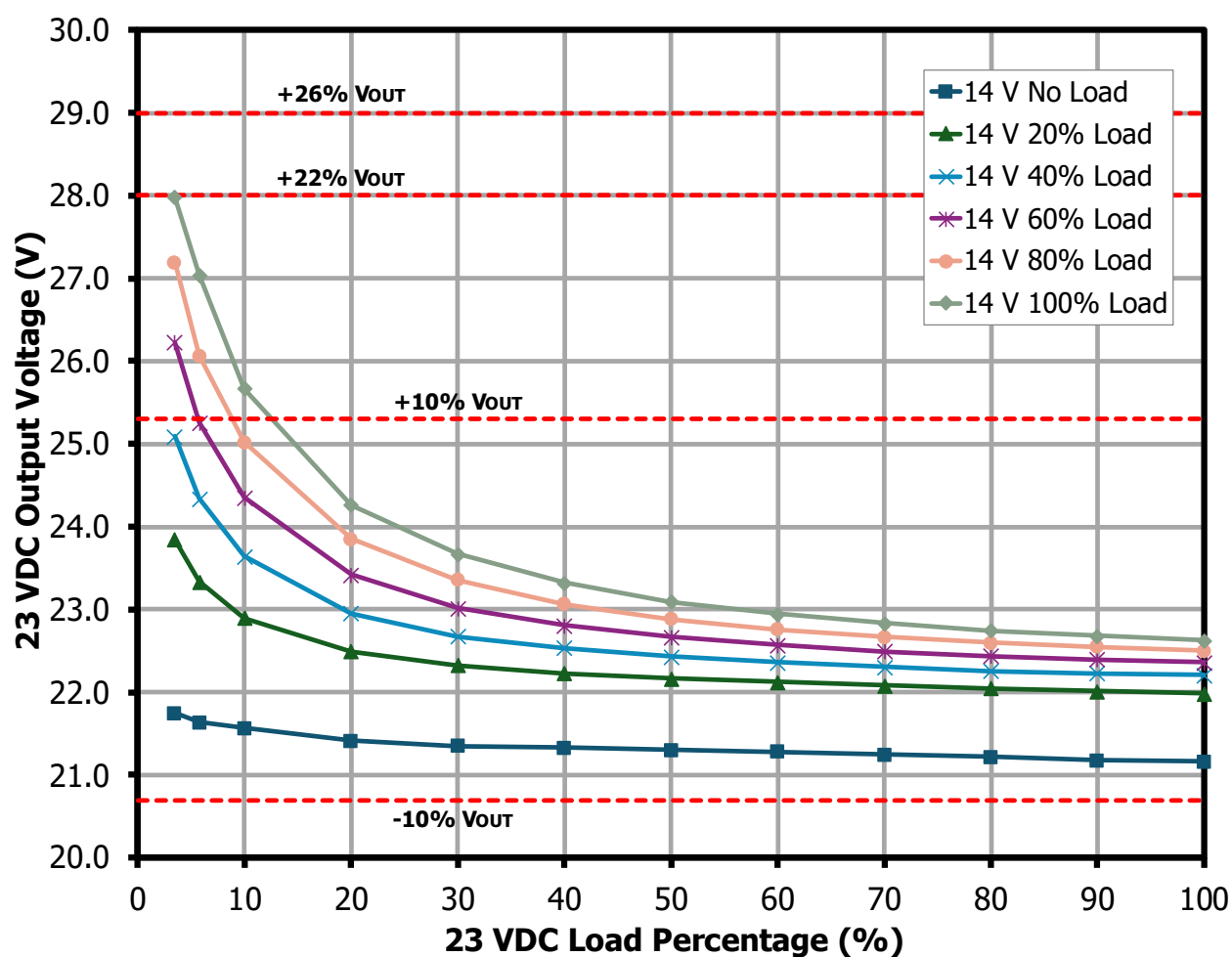


Figure 31 – 23 VDC Output Regulation vs. Load at 800 V Input Voltage (-40 °C Ambient).

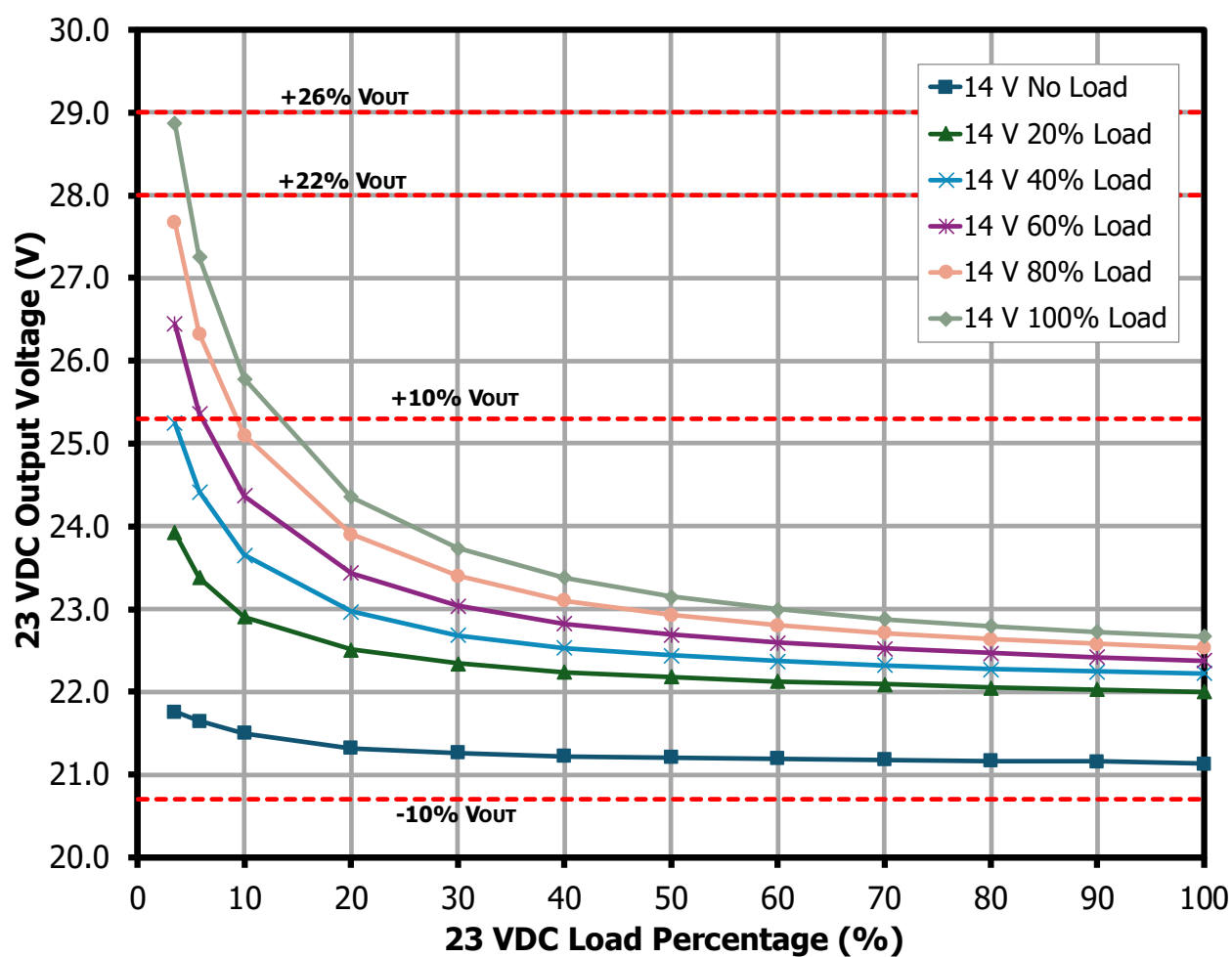


Figure 32 – 23 VDC Output Regulation vs. Load at 1000 V Input Voltage (-40 °C Ambient).

9.3.1.1 Load Regulation at 25 °C Ambient

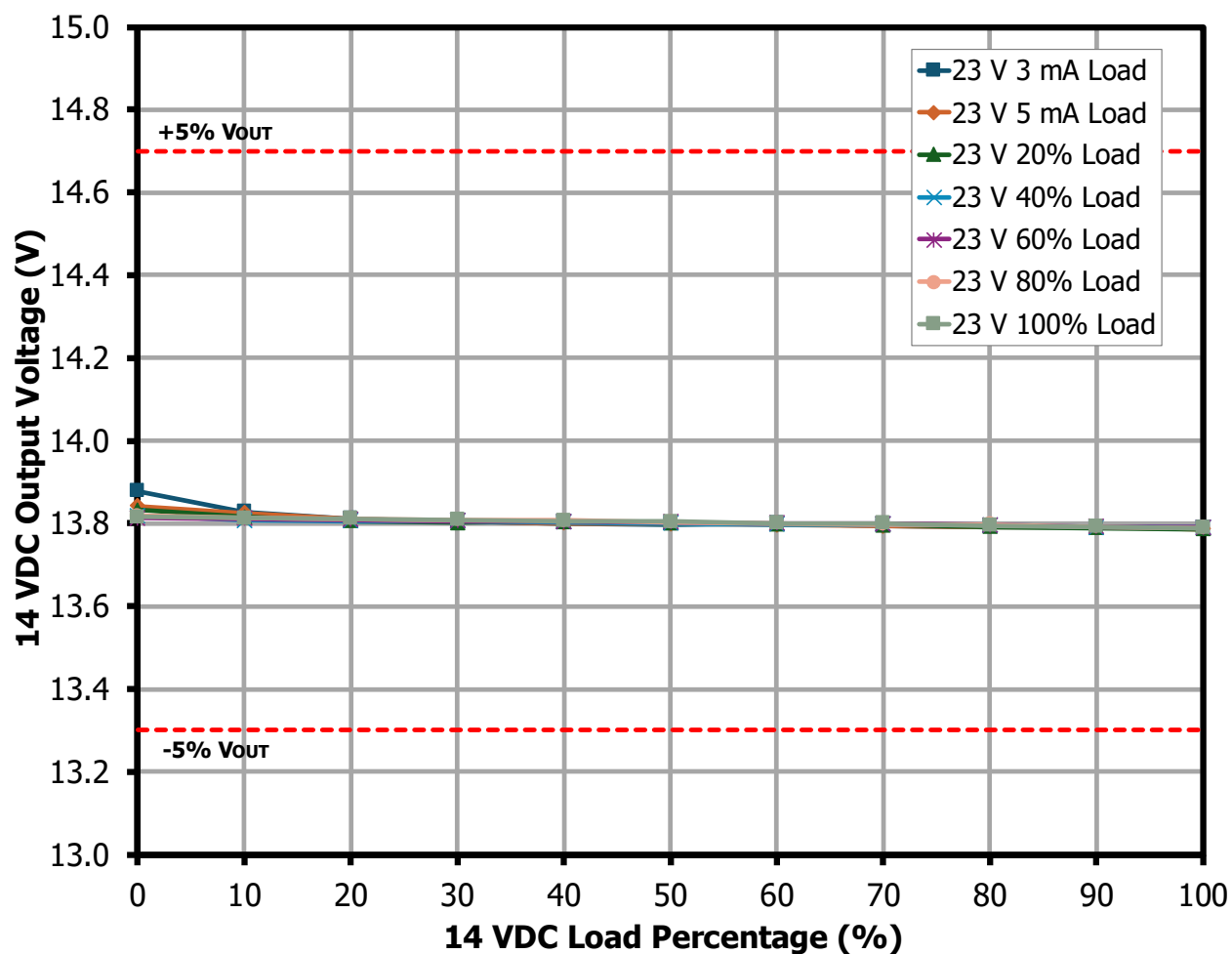


Figure 33 – 14 VDC Output Regulation vs. Load at 200 V Input Voltage (25 °C Ambient).

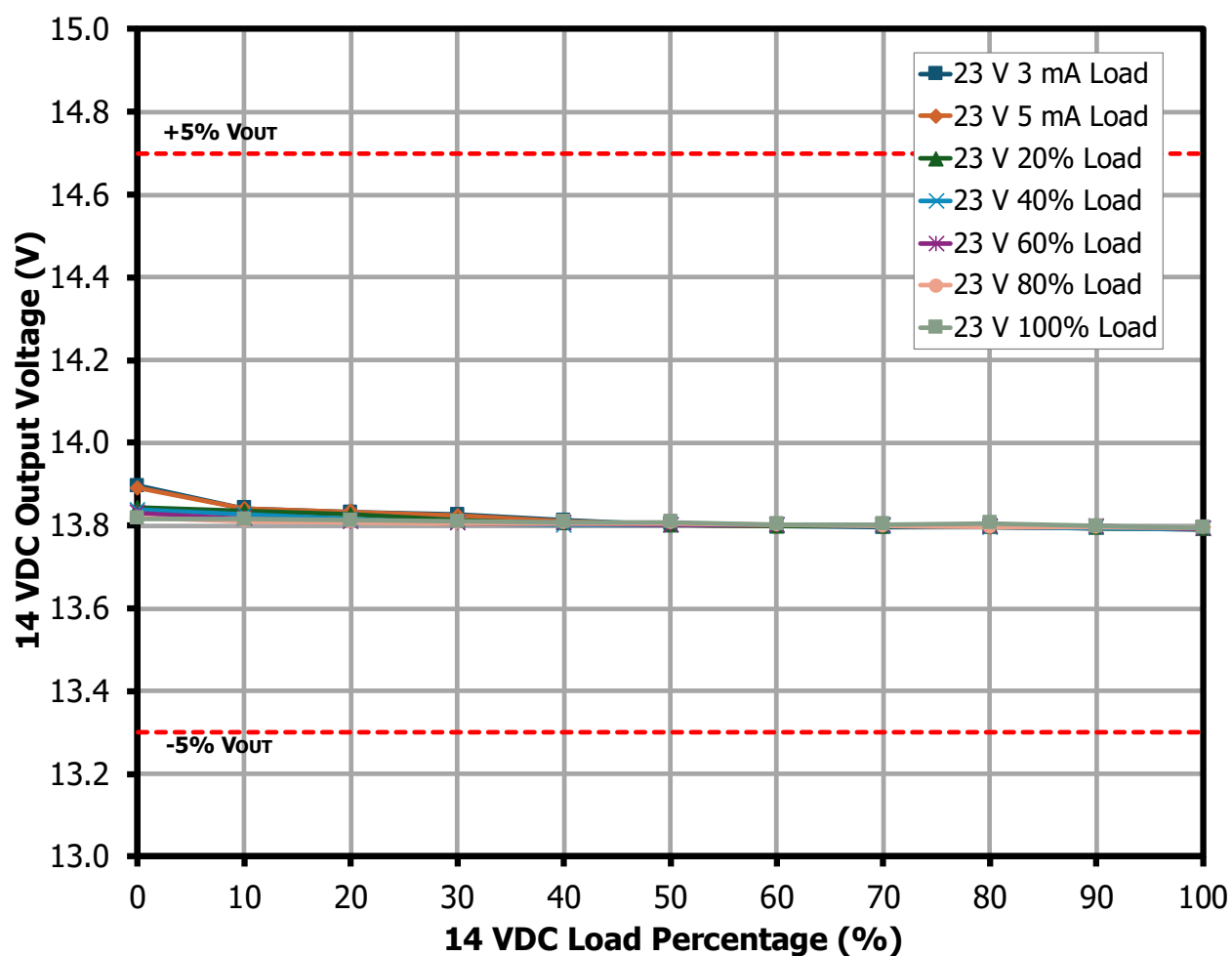


Figure 34 – 14 VDC Output Regulation vs. Load at 800 V Input Voltage (25 °C Ambient).

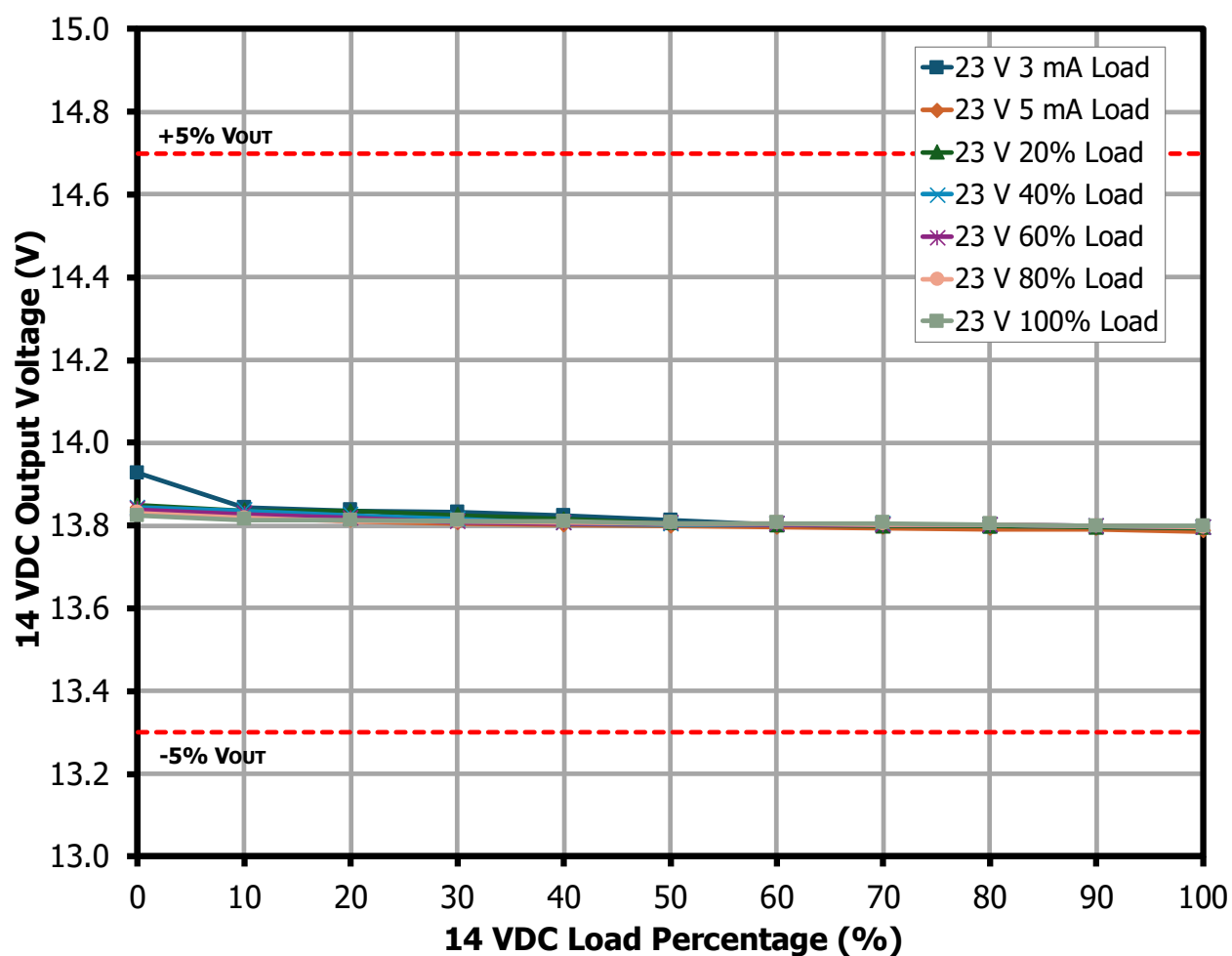


Figure 35 – 14 VDC Output Regulation vs. Load at 1000 V Input Voltage (25 °C Ambient).

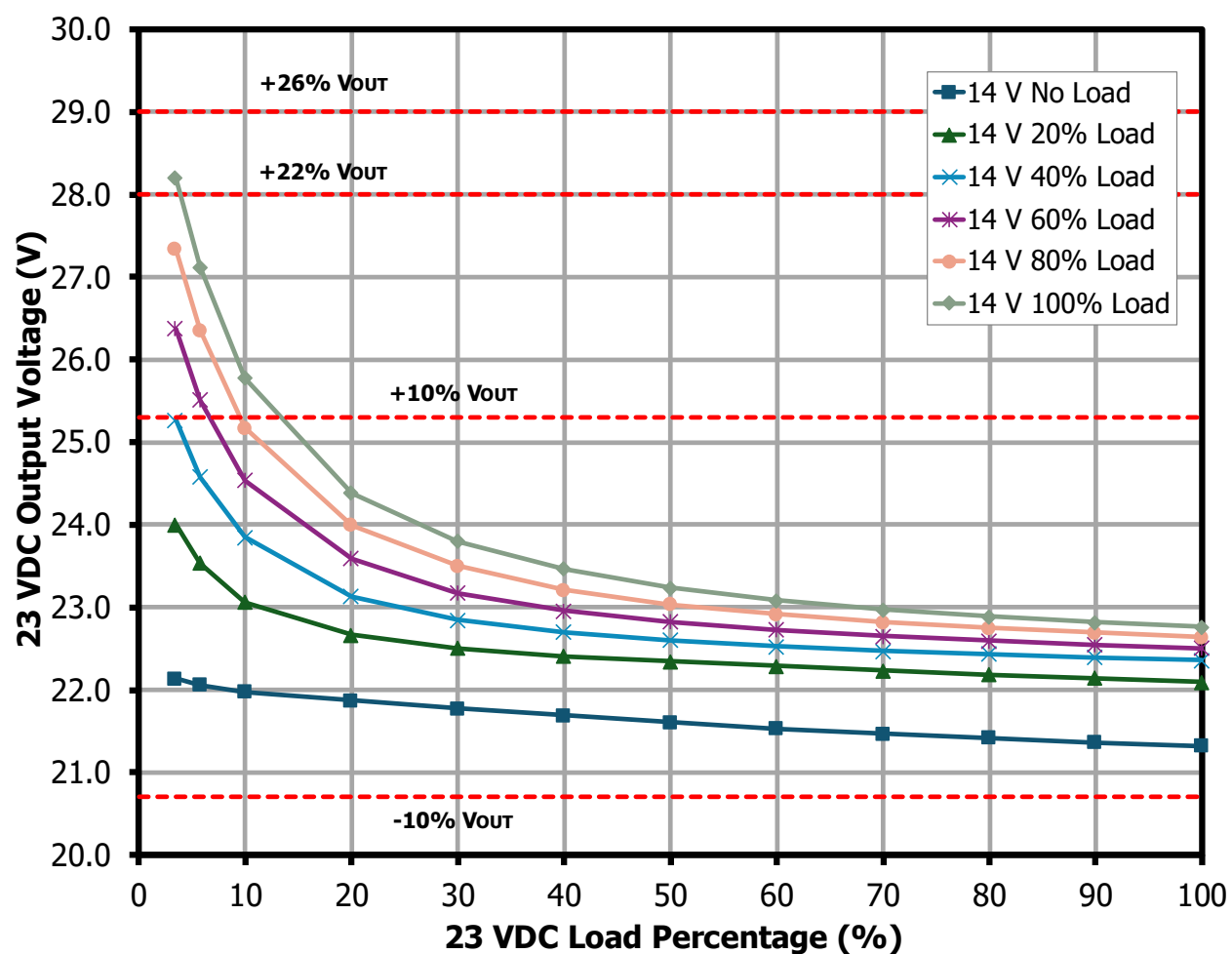


Figure 36 – 23 VDC Output Regulation vs. Load at 200 V Input Voltage (25 °C Ambient).

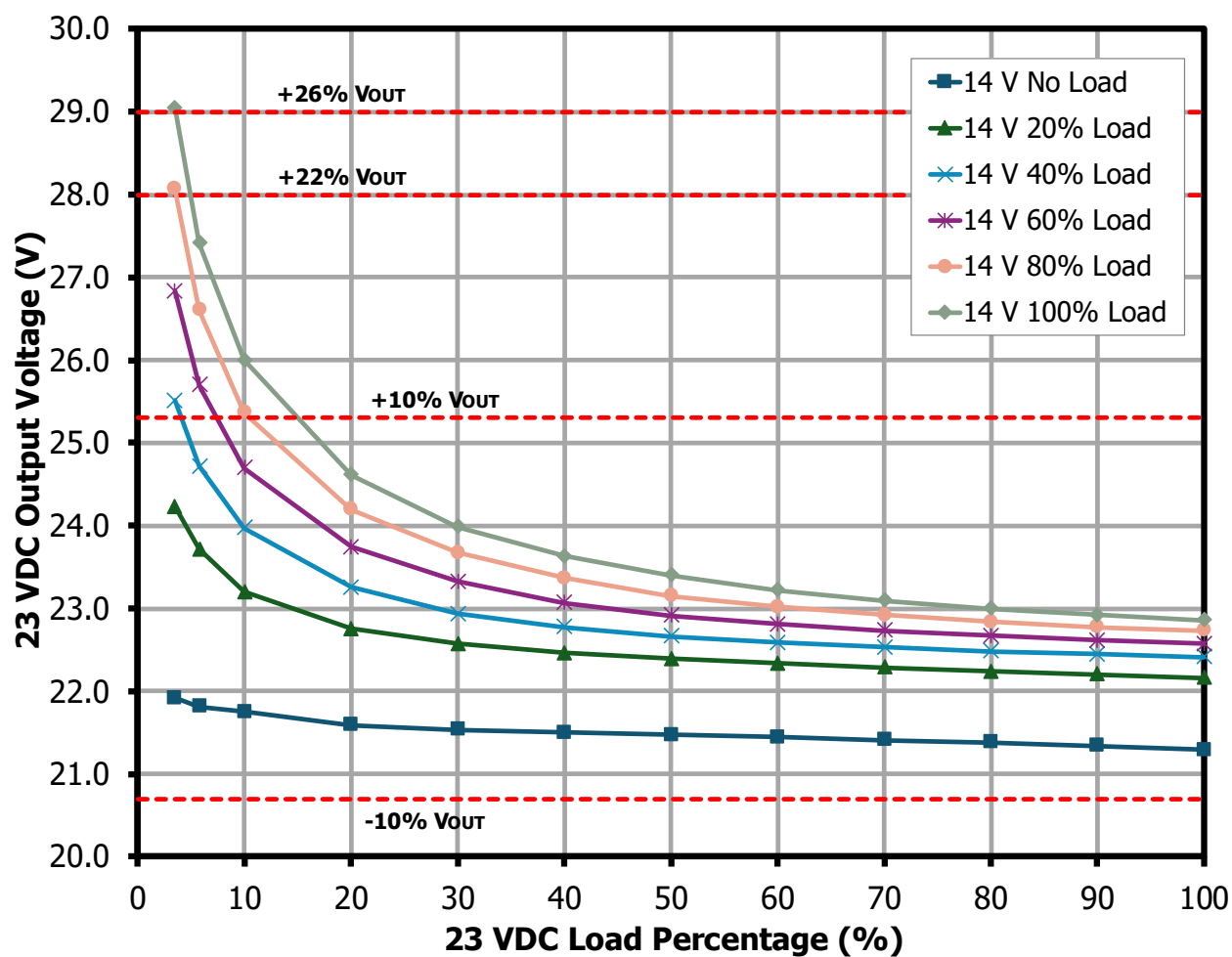


Figure 37 – 23 VDC Output Regulation vs. Load at 800 V Input Voltage (25 °C Ambient).

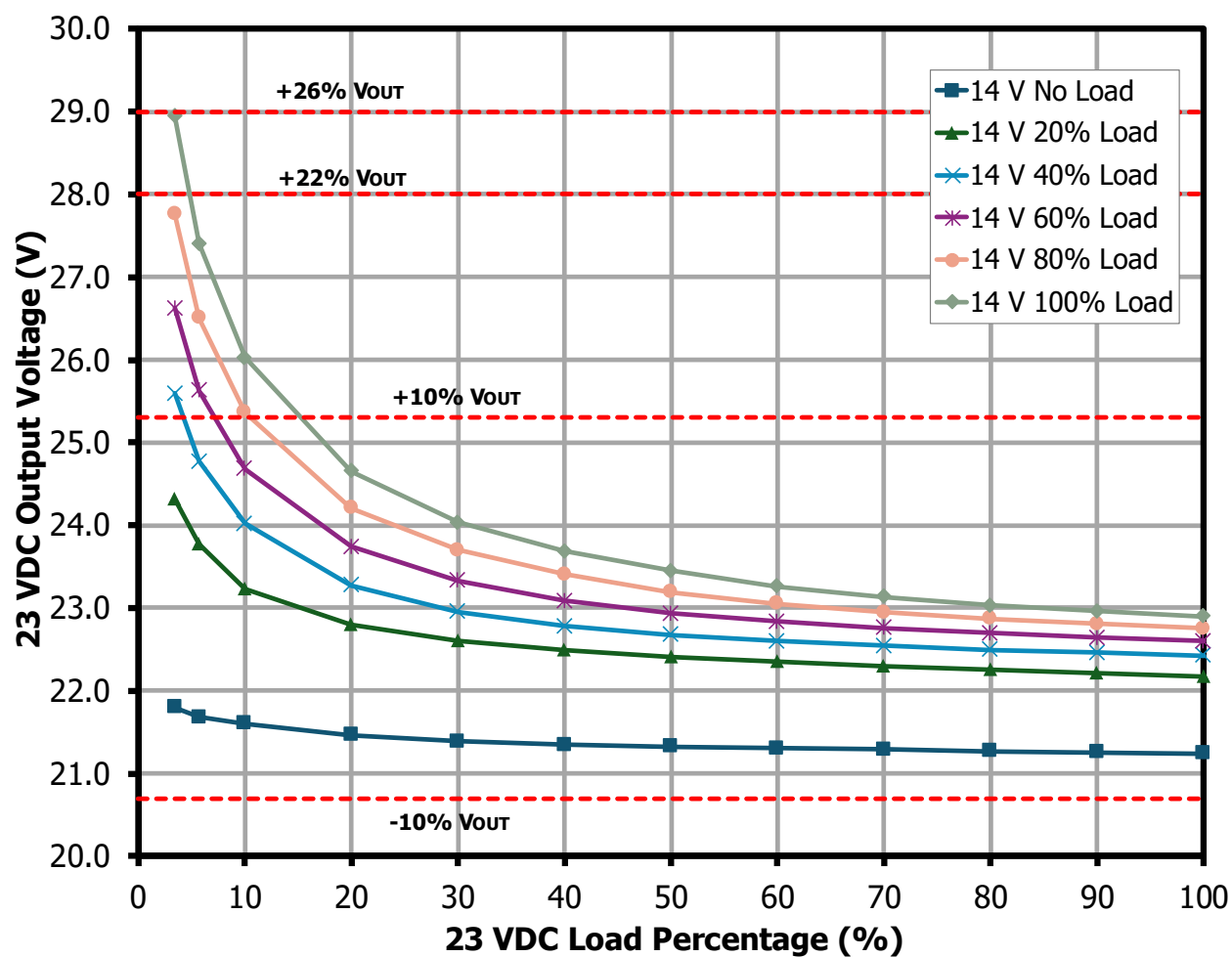


Figure 38 – 23 VDC Output Regulation vs. Load at 1000 V Input Voltage (25 °C Ambient).

9.3.1.2 Load Regulation at 85 °C Ambient

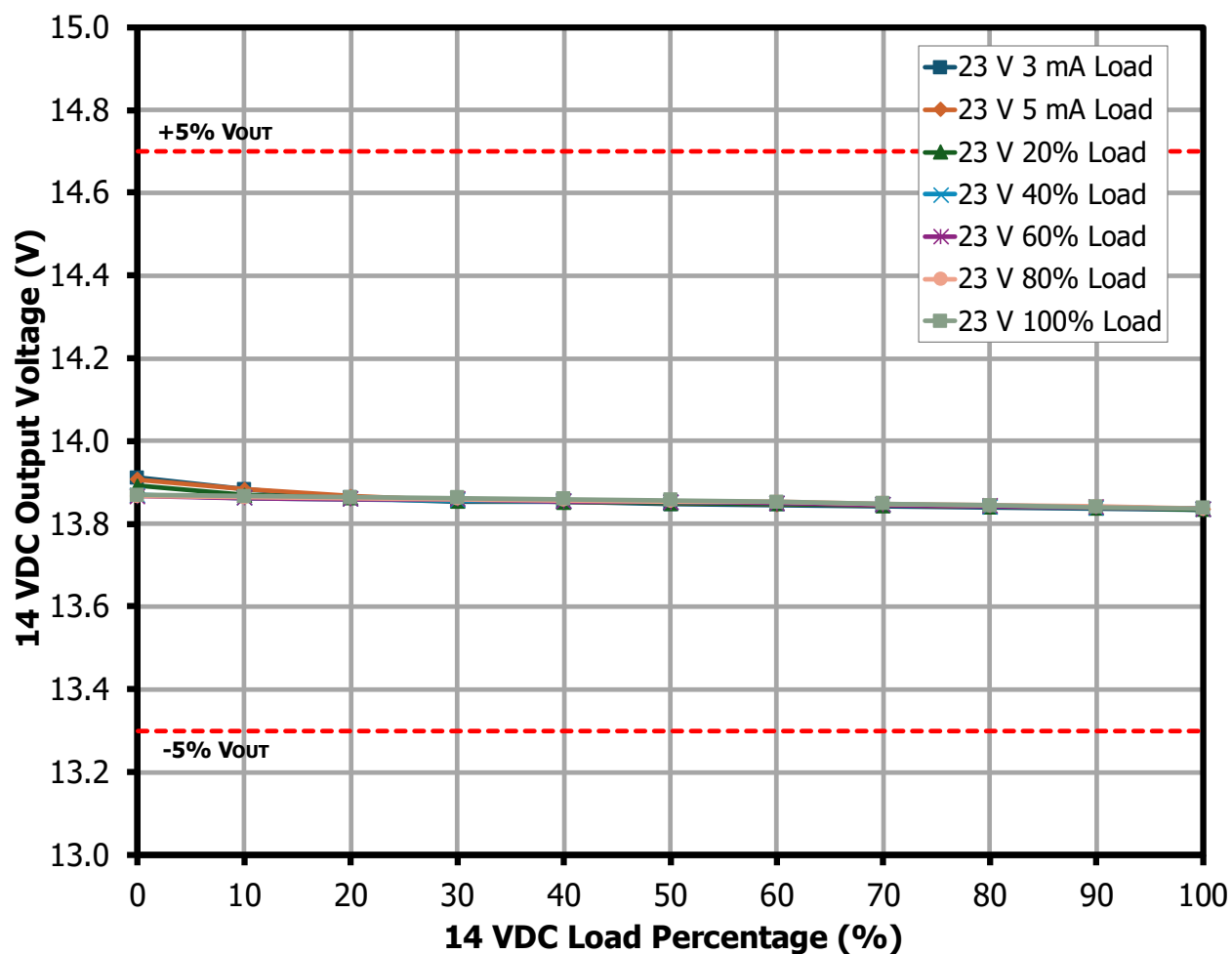


Figure 39 – 14 VDC Output Regulation vs. Load at 200 V Input Voltage (85 °C Ambient).

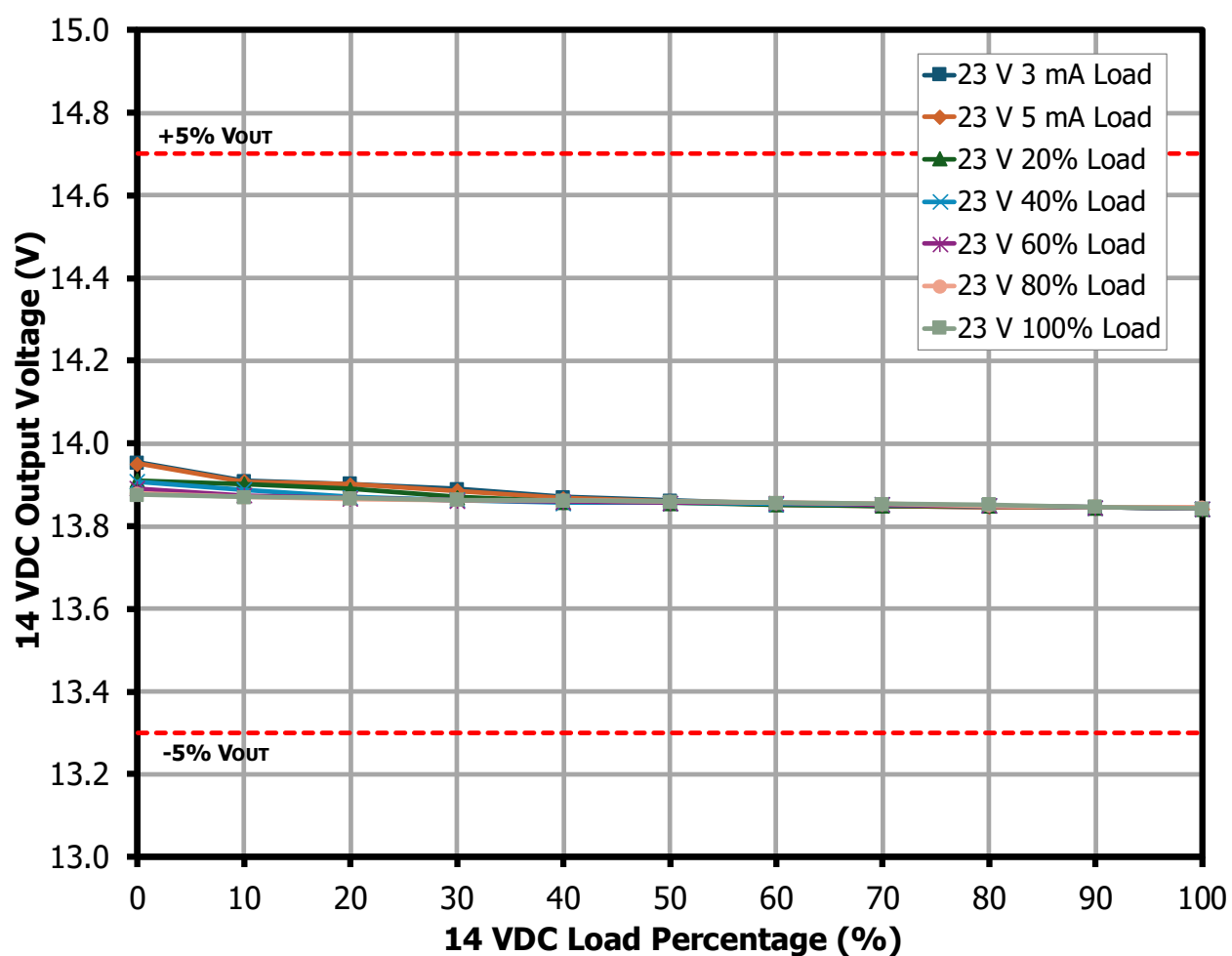


Figure 40 – 14 VDC Output Regulation vs. Load at 800 V Input Voltage (85 °C Ambient).

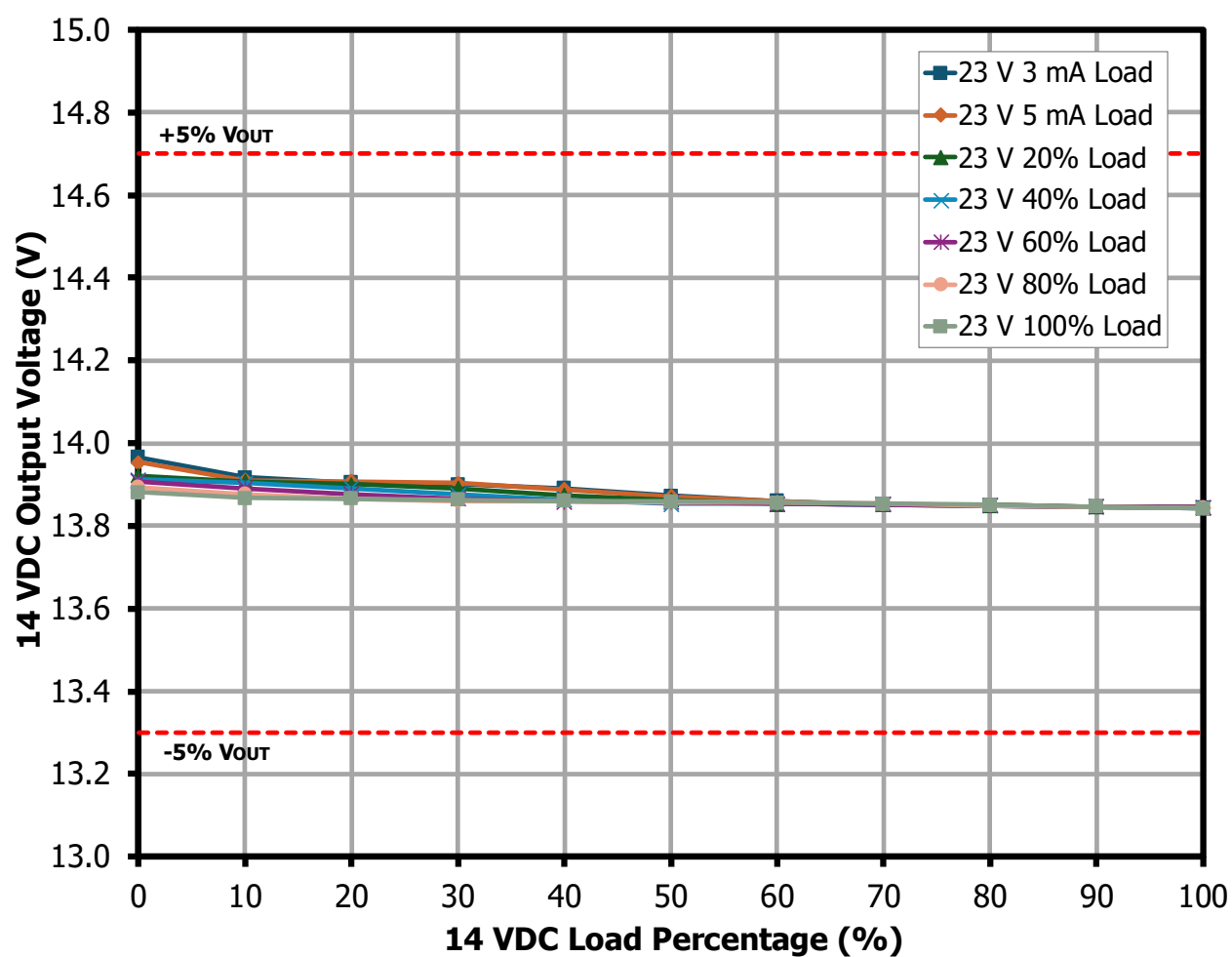


Figure 41 – 14 VDC Output Regulation vs. Load at 1000 V Input Voltage (85 °C Ambient).

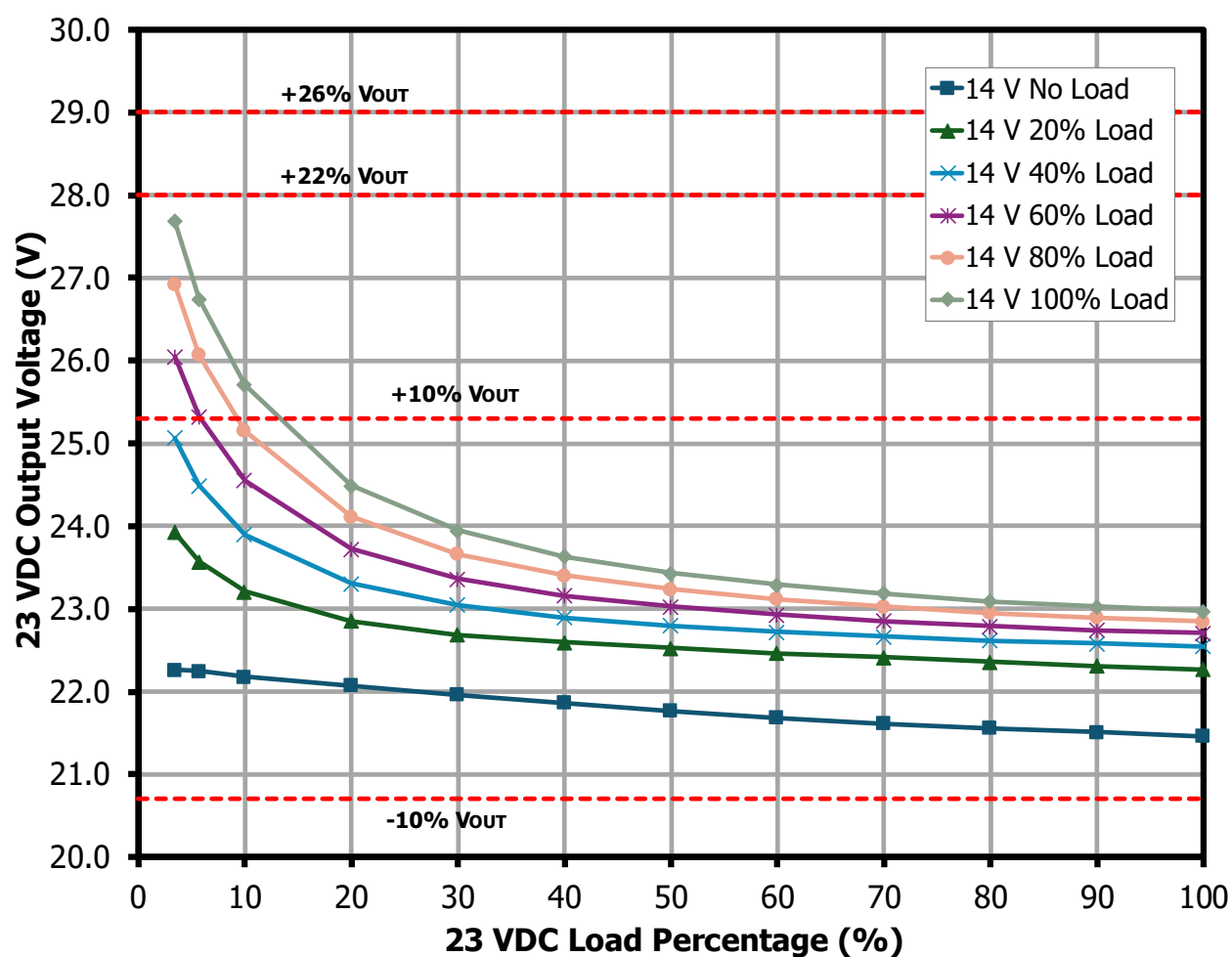


Figure 42 – 23 VDC Output Regulation vs. Load at 200 V Input Voltage (85 °C Ambient).

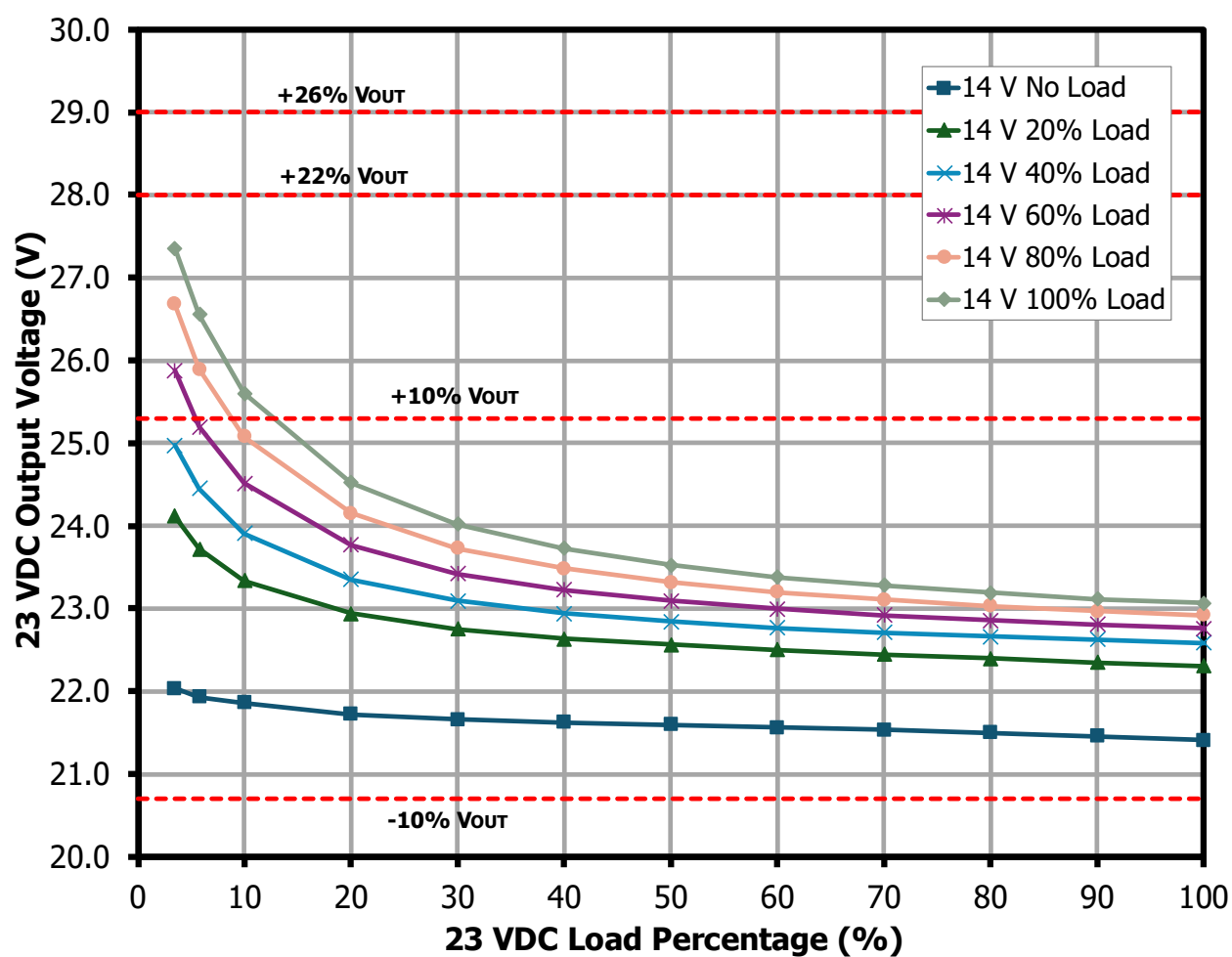


Figure 43 – 23 VDC Output Regulation vs. Load at 800 V Input Voltage (85 °C Ambient).

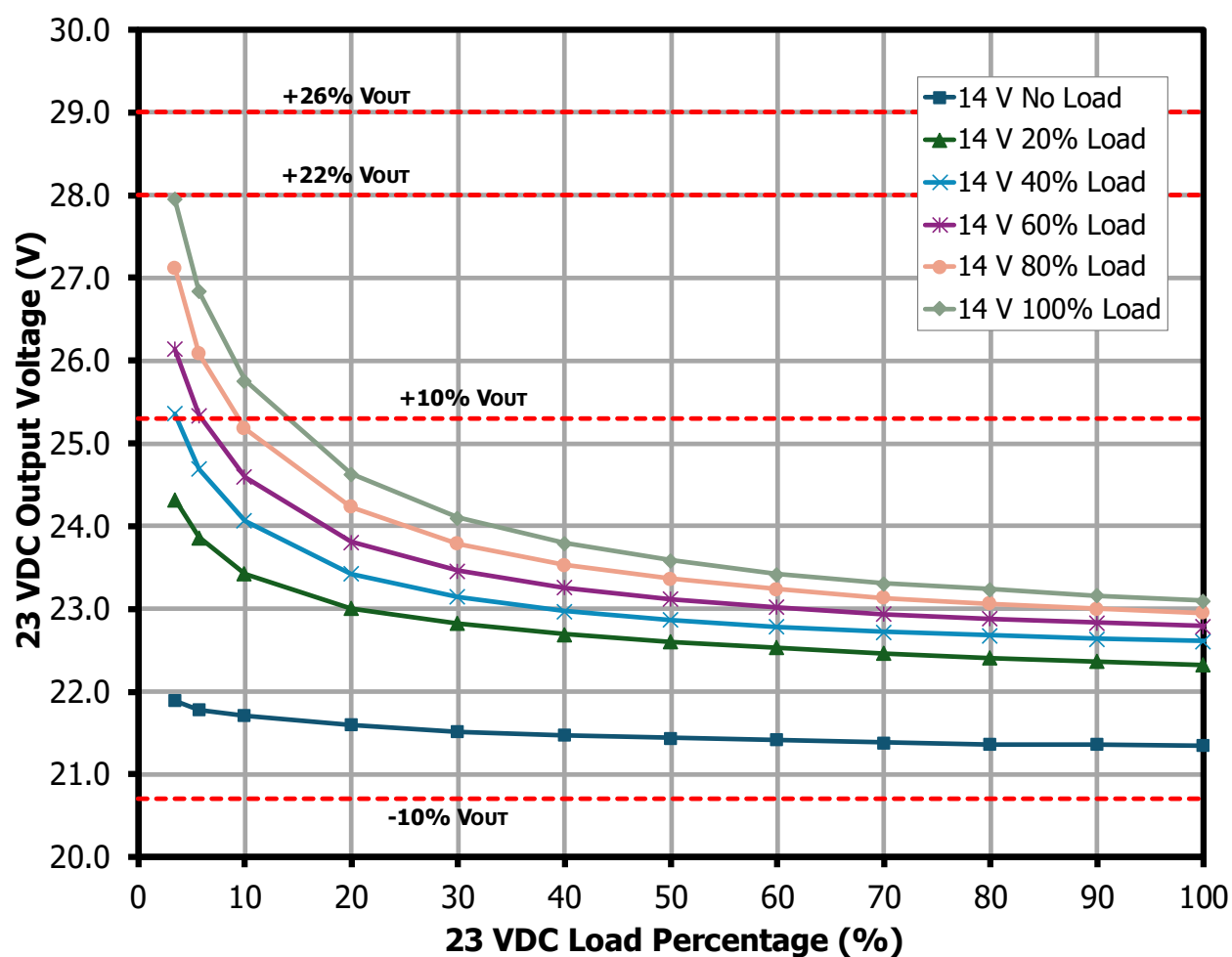


Figure 44 – 23 VDC Output Regulation vs. Load at 1000 V Input Voltage (85 °C Ambient).

9.3.2 Line Regulation

Line regulation describes how a change in input voltage affects the output voltage.

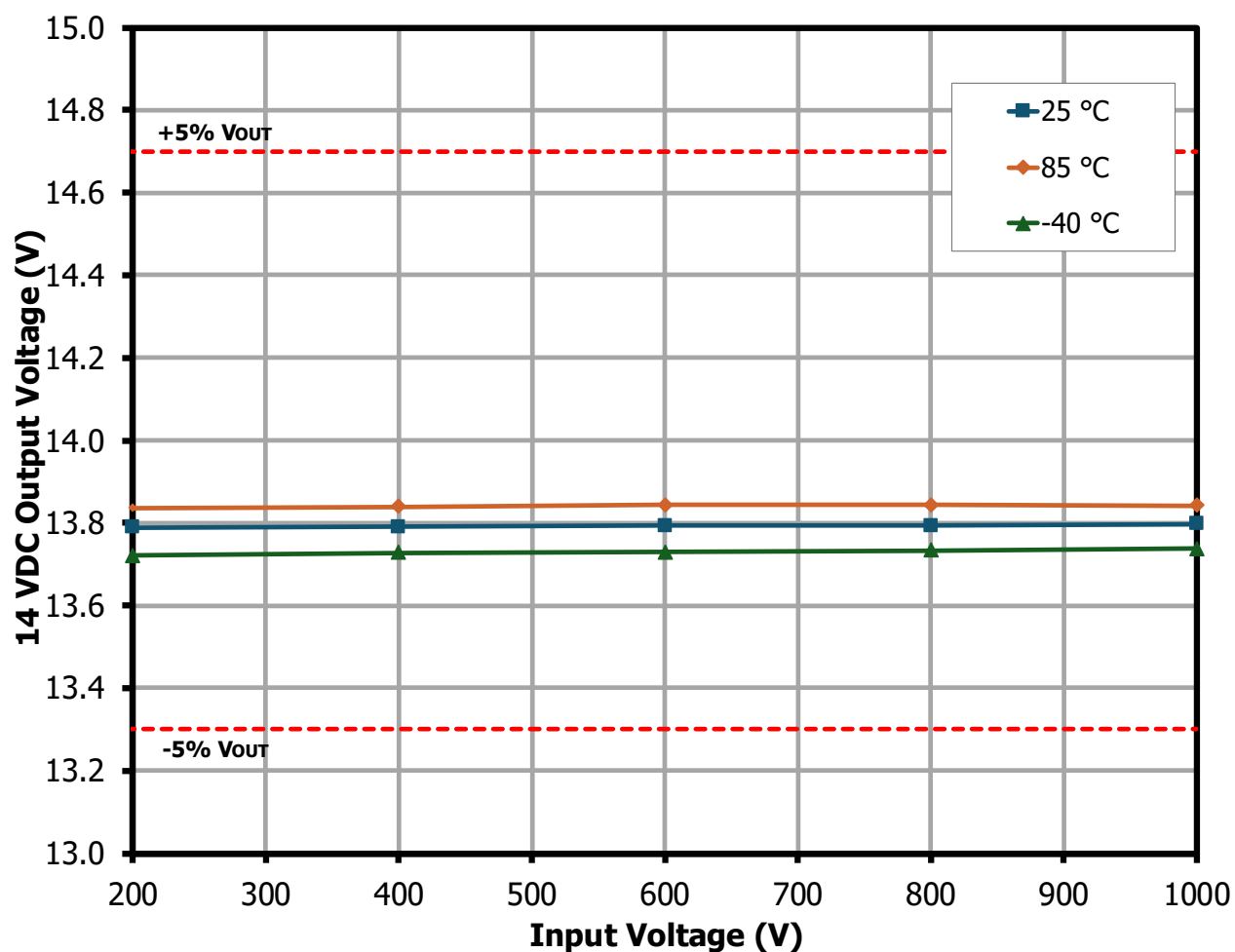


Figure 45 – 14 VDC Output Voltage vs Input Voltage at Full Load.

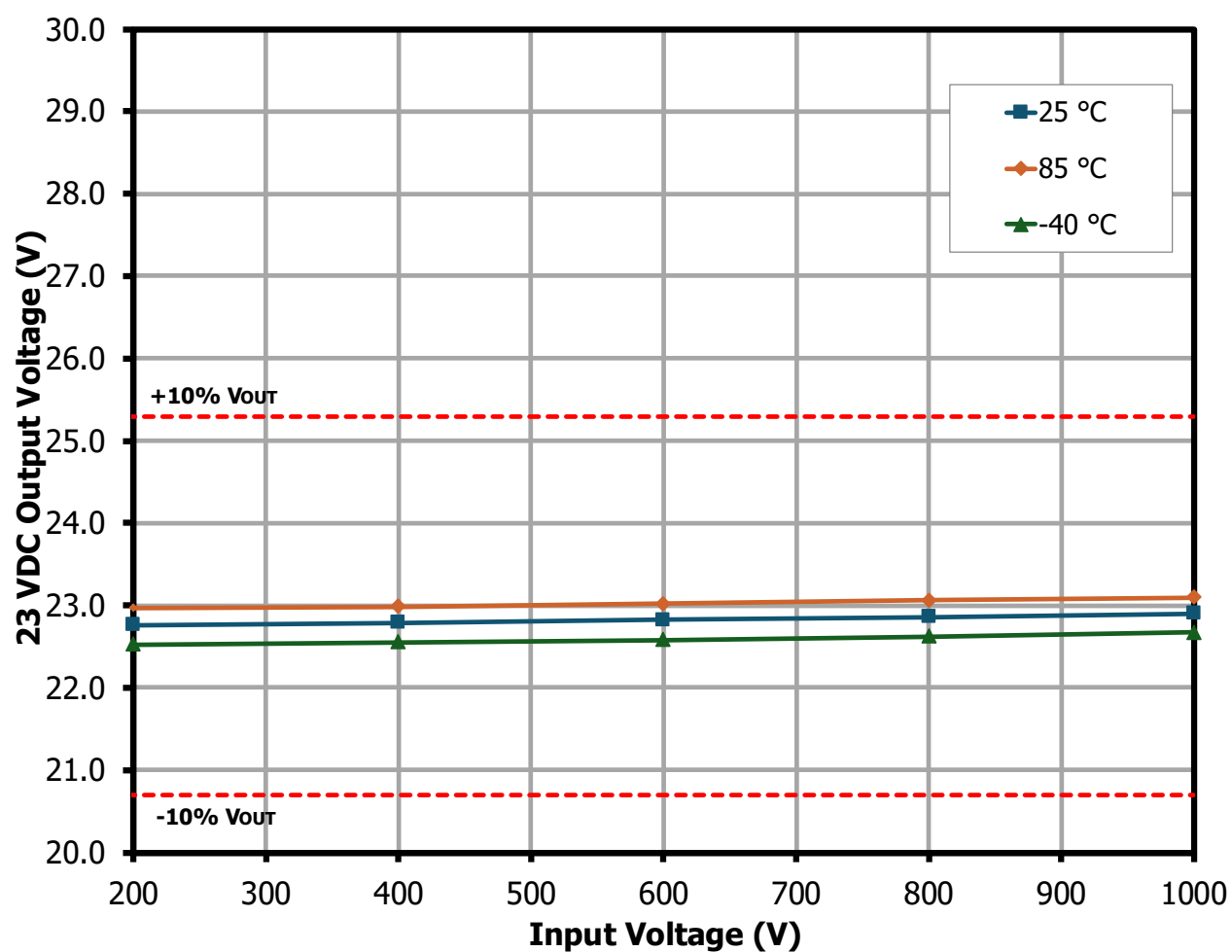


Figure 46 – 23 VDC Output Voltage vs Input Voltage at Full Load.

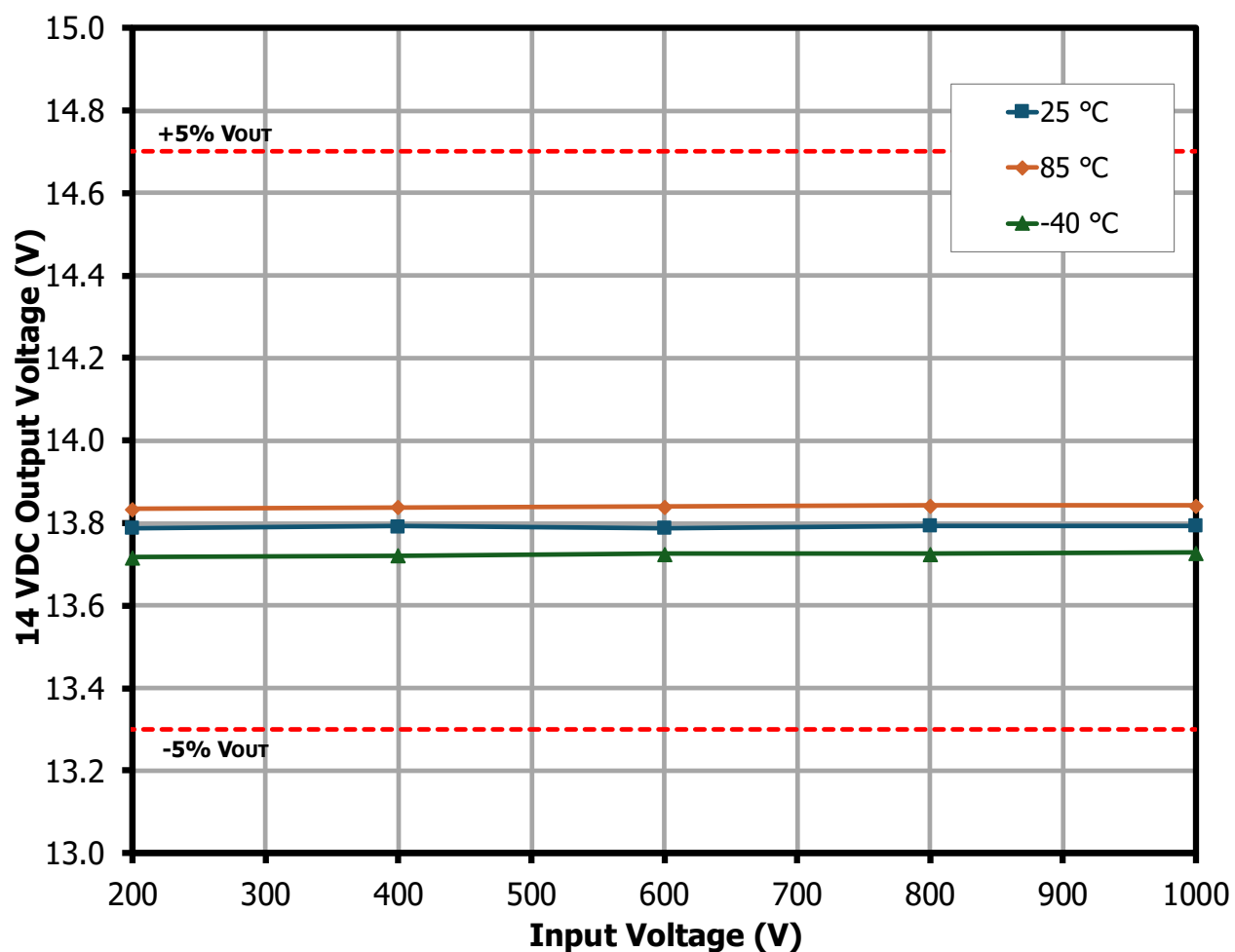


Figure 47 – 14 VDC Output Voltage vs Input Voltage at 14 VDC maximum load and 23 VDC minimum load.

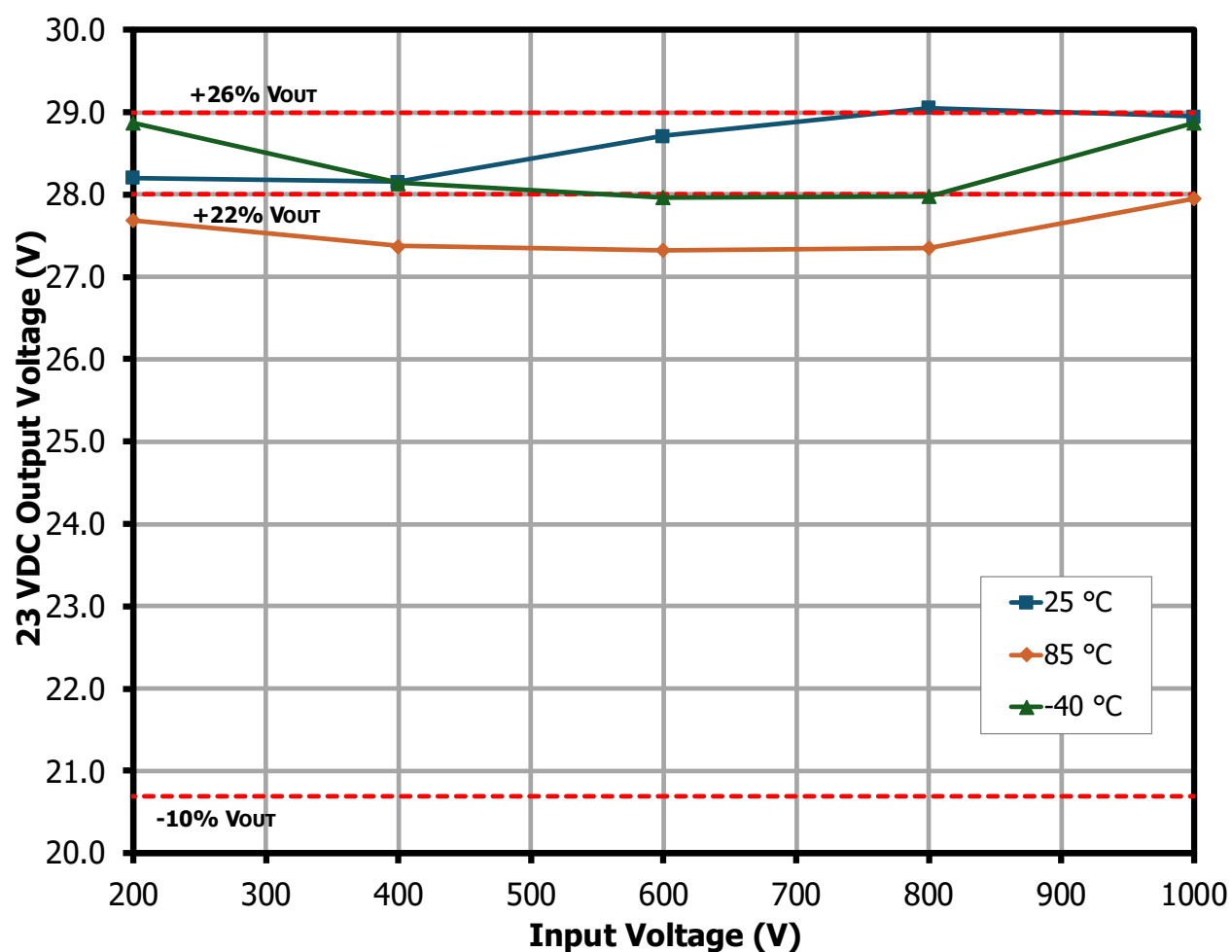


Figure 48 – 23 VDC Output Voltage vs Input Voltage at 14 VDC maximum load and 23 VDC 3 mA load.

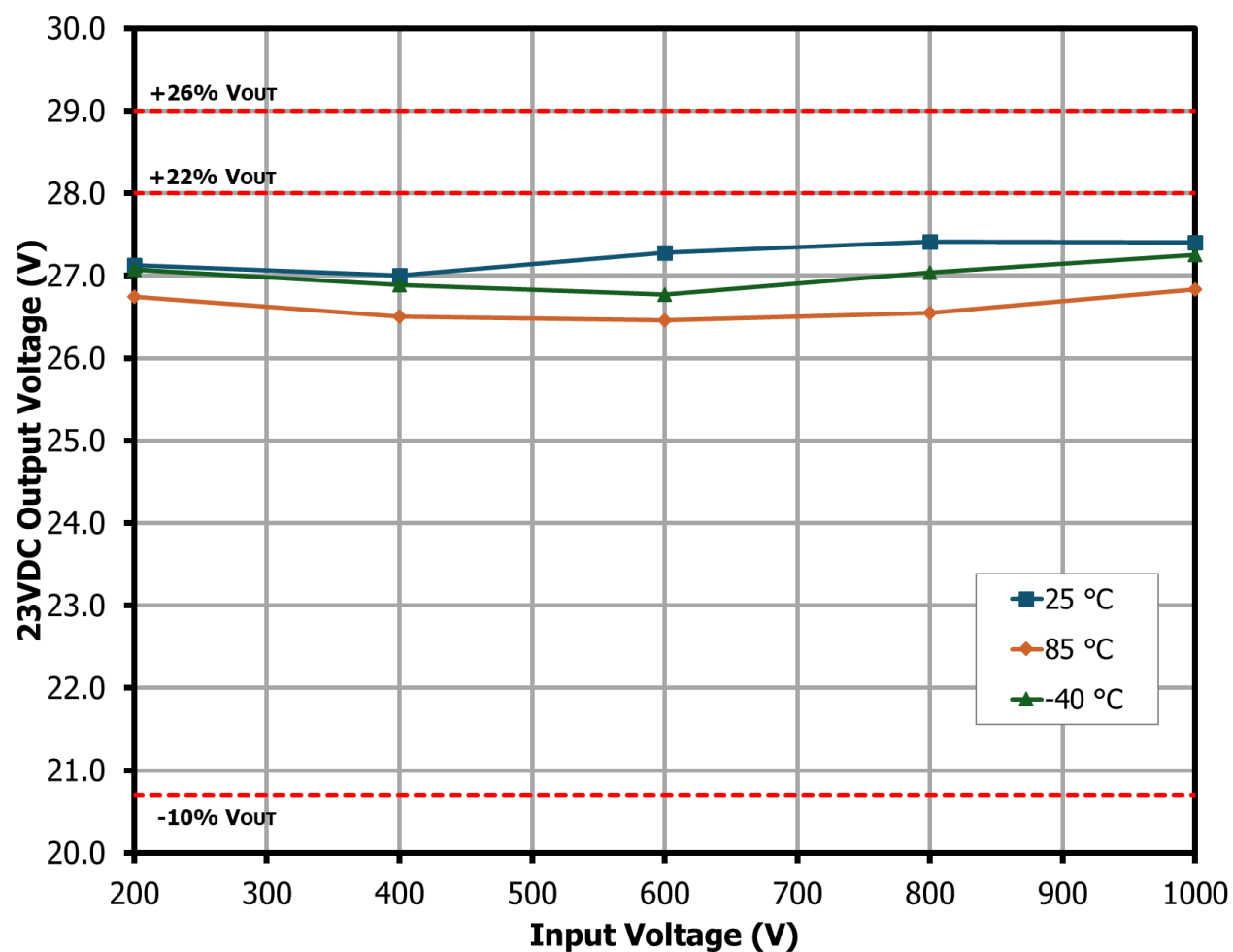


Figure 49 – 23 VDC Output Voltage vs Input Voltage at 14 VDC maximum load and 23 VDC 5 mA load.

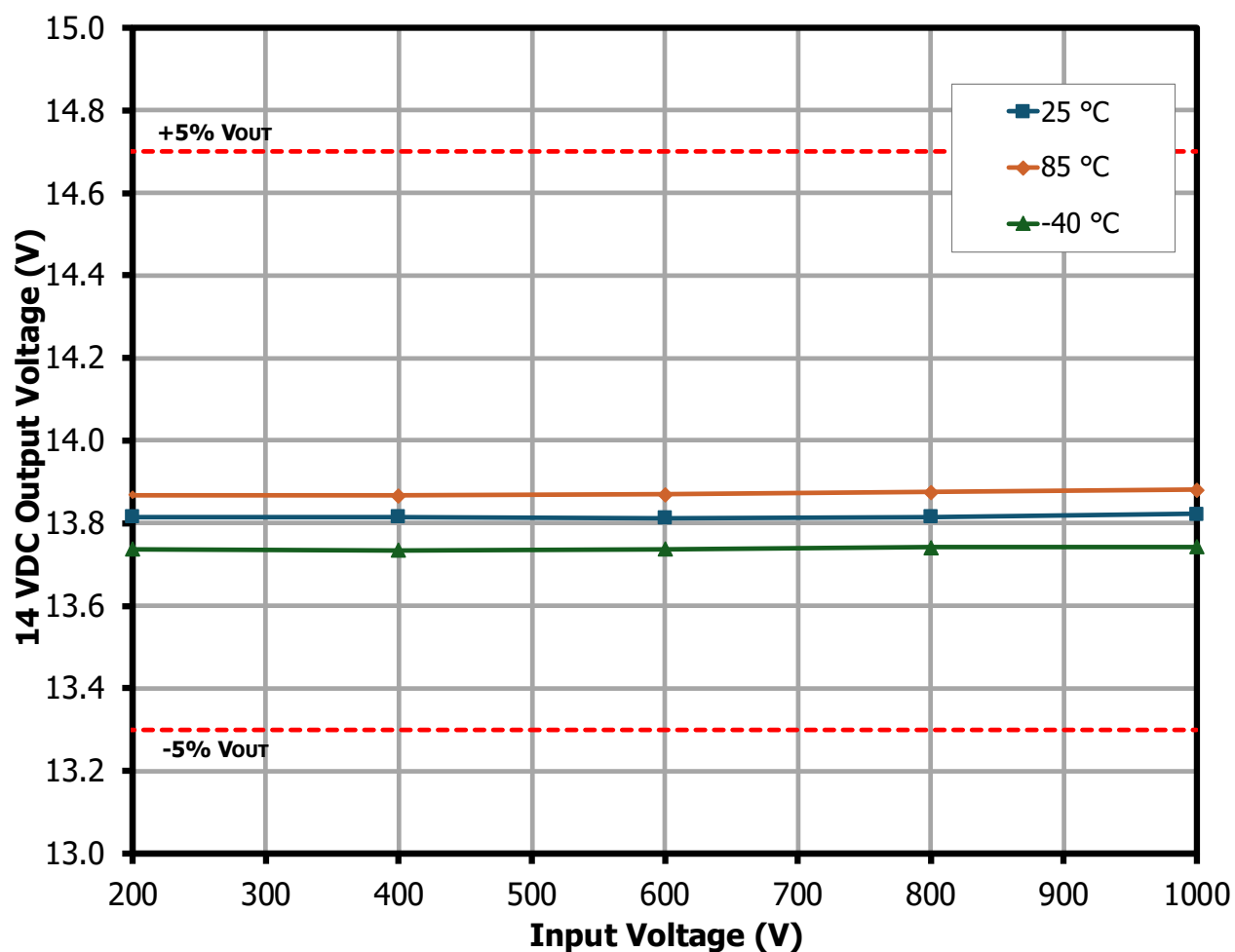


Figure 50 – 14 VDC Output Voltage vs Input Voltage at 14 VDC no load and 23 VDC maximum load.

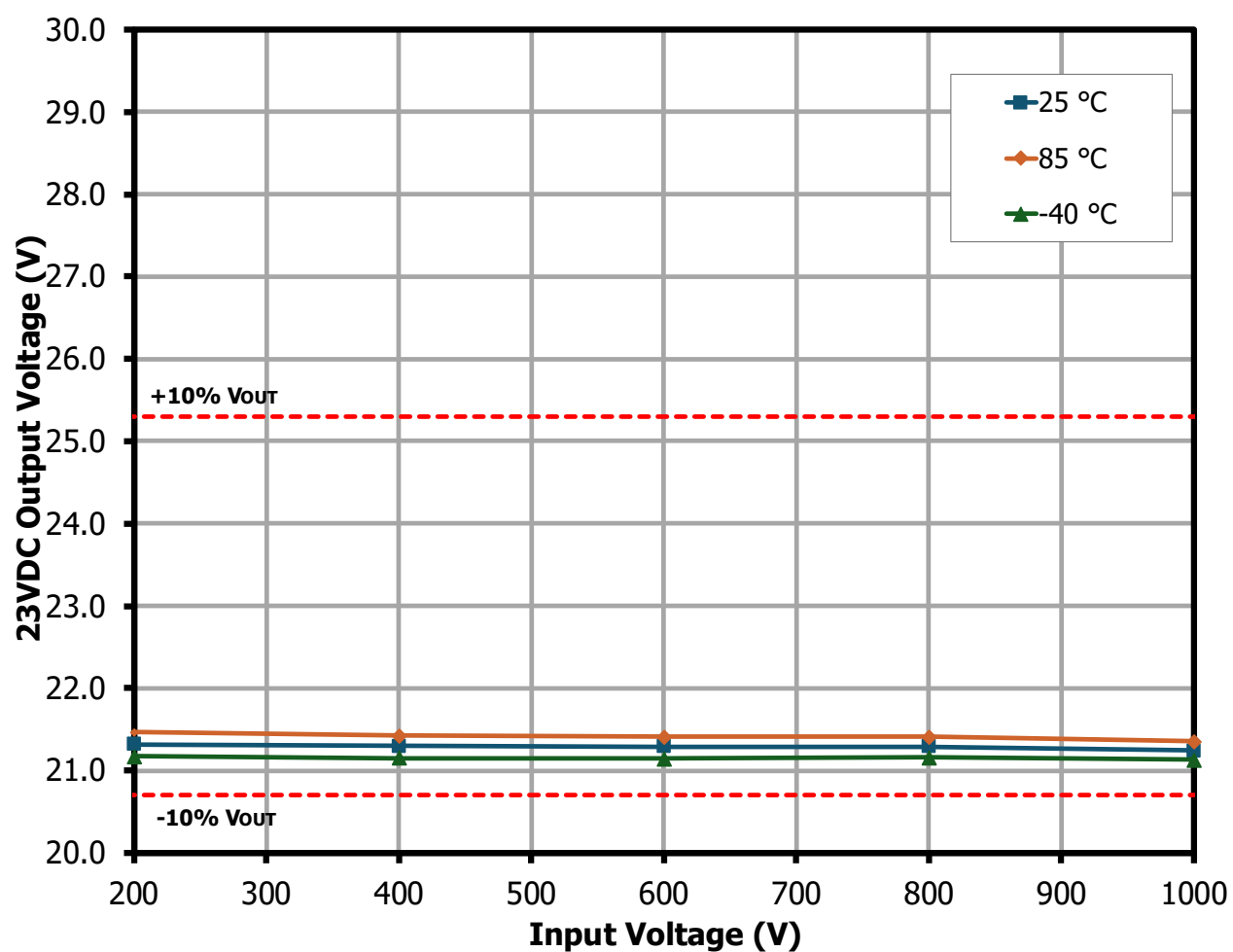


Figure 51 – 23 VDC Output Voltage vs Input Voltage at 14 VDC no load and 23 VDC maximum load.

10 Thermal Performance

10.1 Thermal Data at 85 °C Ambient

The unit was placed inside a thermal chamber and allowed to stabilize at 100% load for 90 minutes. Figure shows the test setup for thermal measurement.

Critical Components	Temperature (°C)		
	200 V _{DC}	800 V _{DC}	1000 V _{DC}
InnoSwitch3-AQ (IC200)	100	107	111
Primary Snubber Resistor (R202)	98.6	97.9	97.1
Transformer Winding (T200)	95.4	102	104
Transformer Core (T200)	95.7	103	105
Synchronous Rectifier MOSFET (Q100)	93.8	103	105
SR Snubber Resistor (R102)	93.2	106	109
Secondary Diode (D300)	92.2	102	103
Secondary Diode Snubber Resistor (R300)	91.6	103	106

Table 9 – Thermal Data of 16 W Multiple Output Flyback at 85 °C at Different Input Voltages.

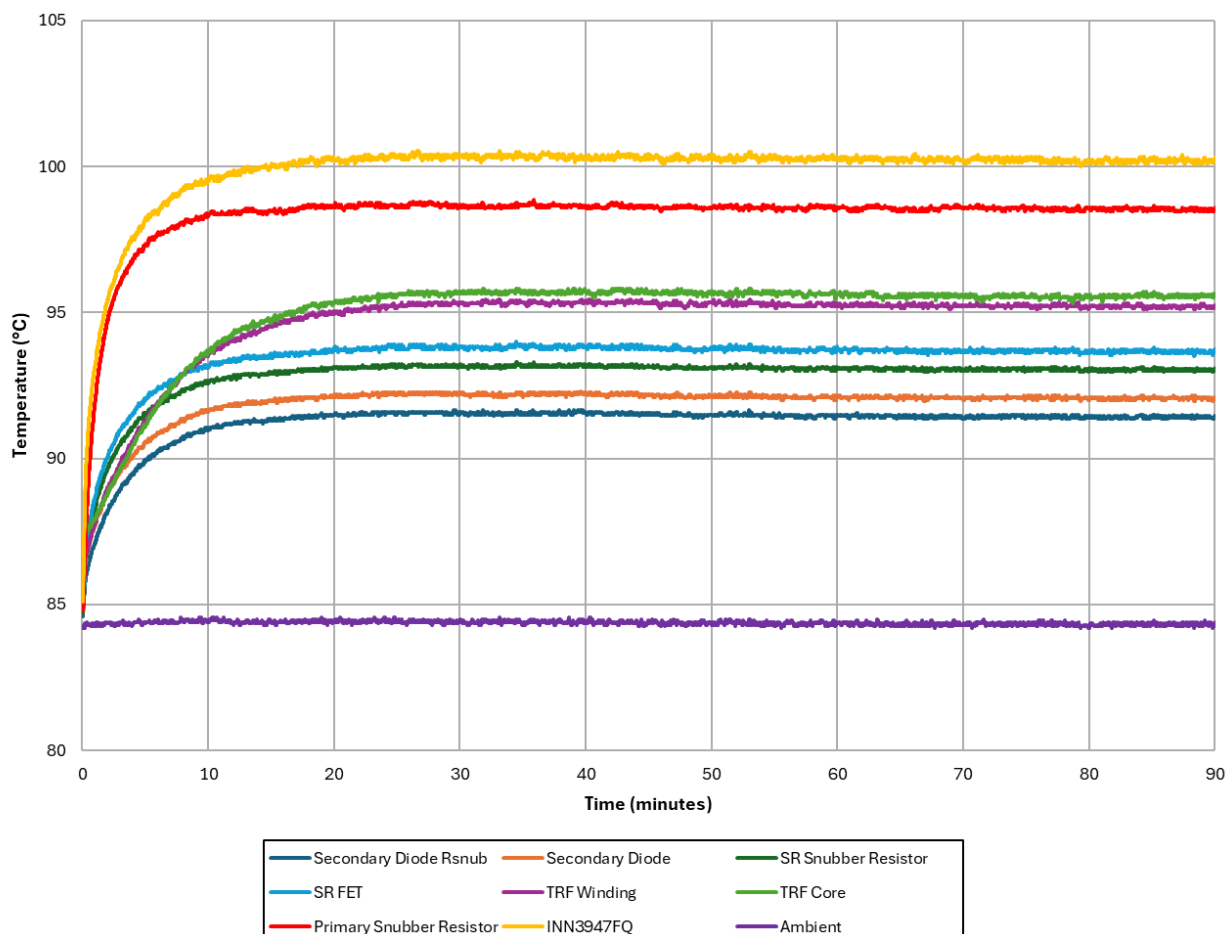


Figure 52 – Component Temperatures at 85 °C Ambient, 200 V Input, Full Load.

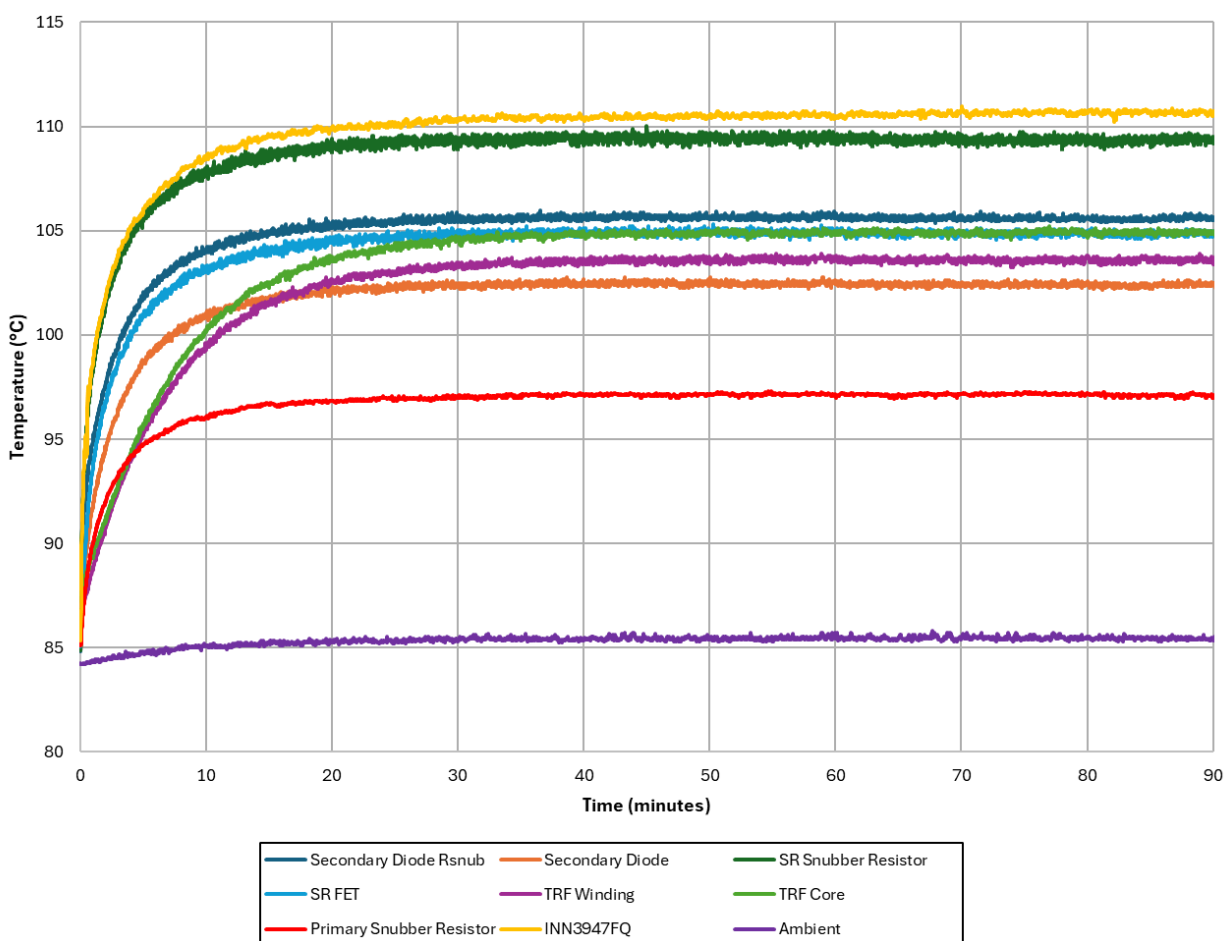


Figure 53 - Component Temperatures at 85 °C Ambient, 1000 V Input, Full Load.

10.2 Thermal Data at 25 °C Ambient

The following thermal scans were captured using a Fluke thermal imager after soaking the power supply in an enclosure to minimize the effect of airflow for 1 hour.

Critical Components	Temperature (°C)	
	200 V _{DC}	1000 V _{DC}
InnoSwitch3-AQ (IC200)	41.8	54.9
Primary Snubber Resistor (R202)	41.1	39.8
Transformer Winding (T200)	44.9	57.0
Transformer Core (T200)	44.2	56.2
Synchronous Rectifier MOSFET (Q100)	41.1	51.0
SR Snubber Resistor (R102)	37.0	58.2
Secondary Diode (D300)	36.3	49.6
Secondary Diode Snubber Resistor (R300)	36.7	58.6

Table 10 – Thermal Data at 25 °C at Different Input Voltages.

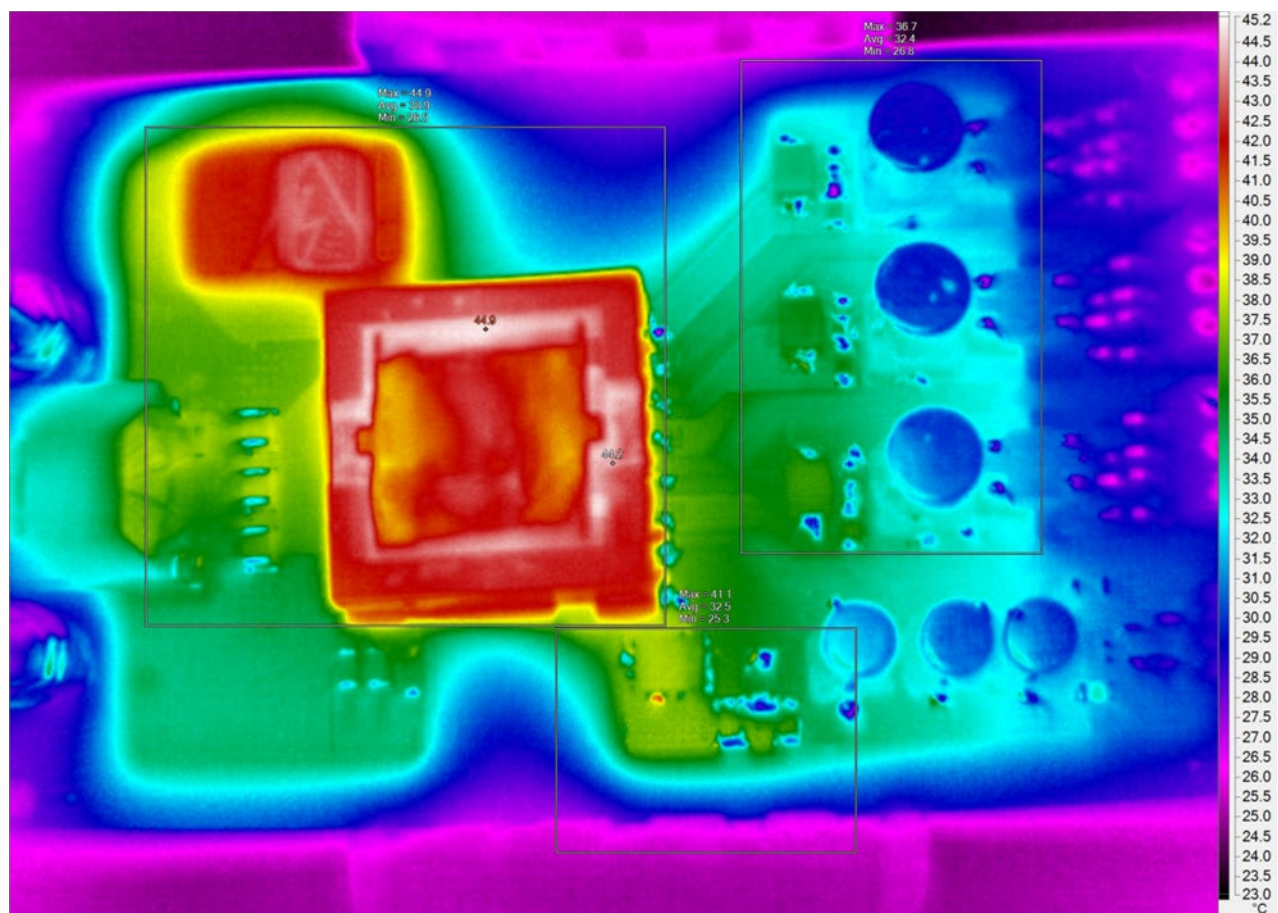


Figure 54 – PCB Top Thermal Scan at 200 V_{DC} Input, Full Load.

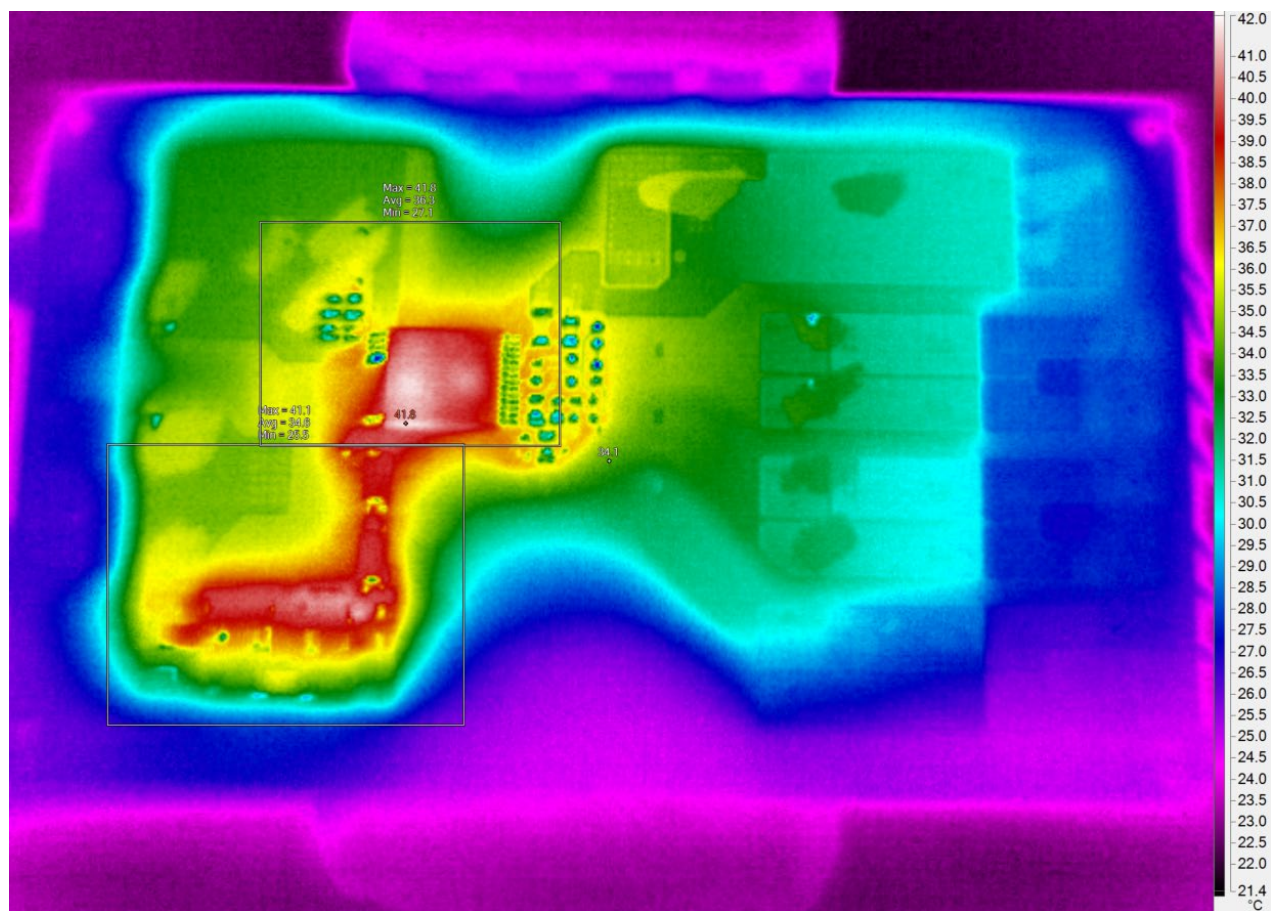


Figure 55 – PCB Bottom Thermal Scan at 200 V_{DC} Input, Full Load.

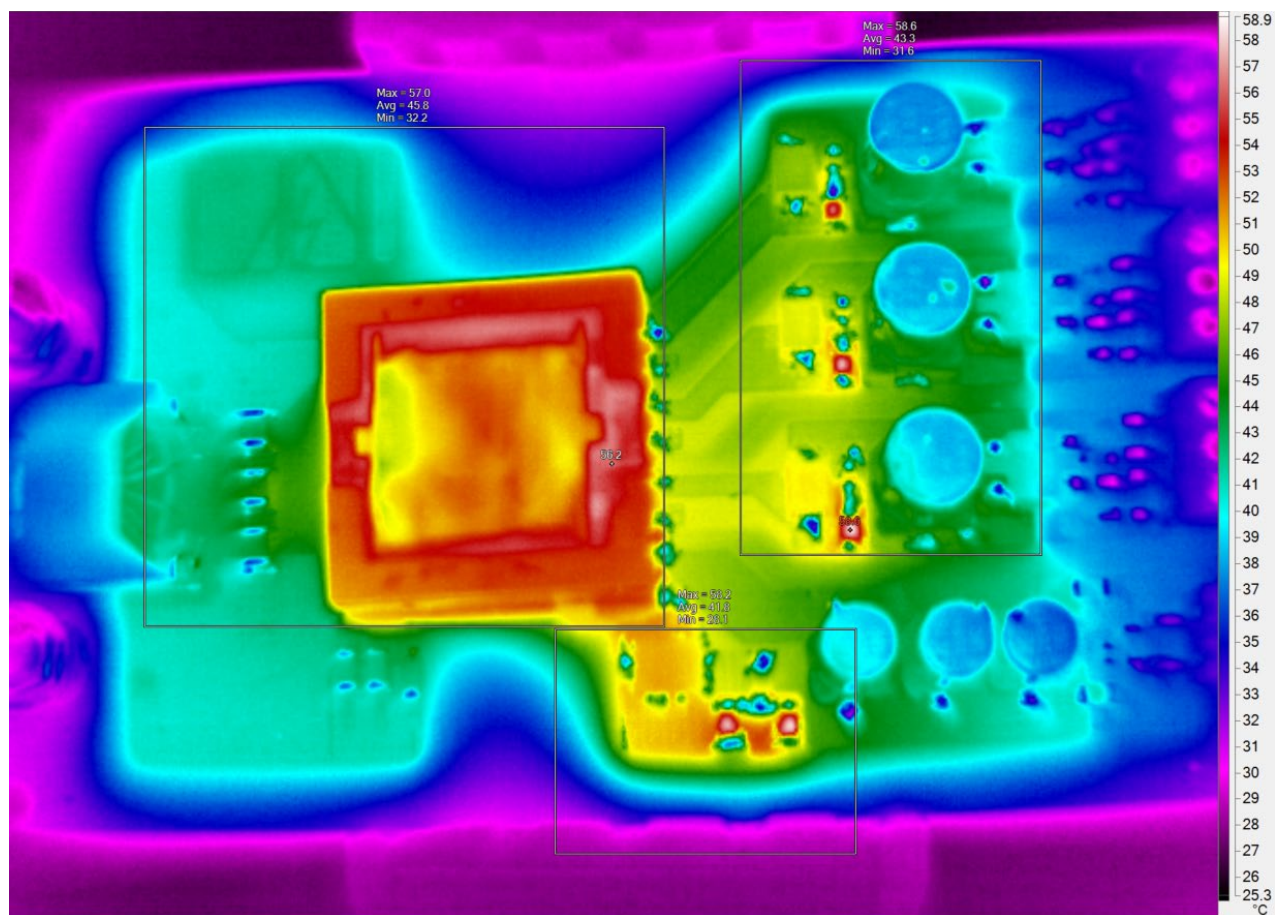


Figure 56 – PCB Top Thermal Scan at 1000 V_{DC} Input, Full Load.

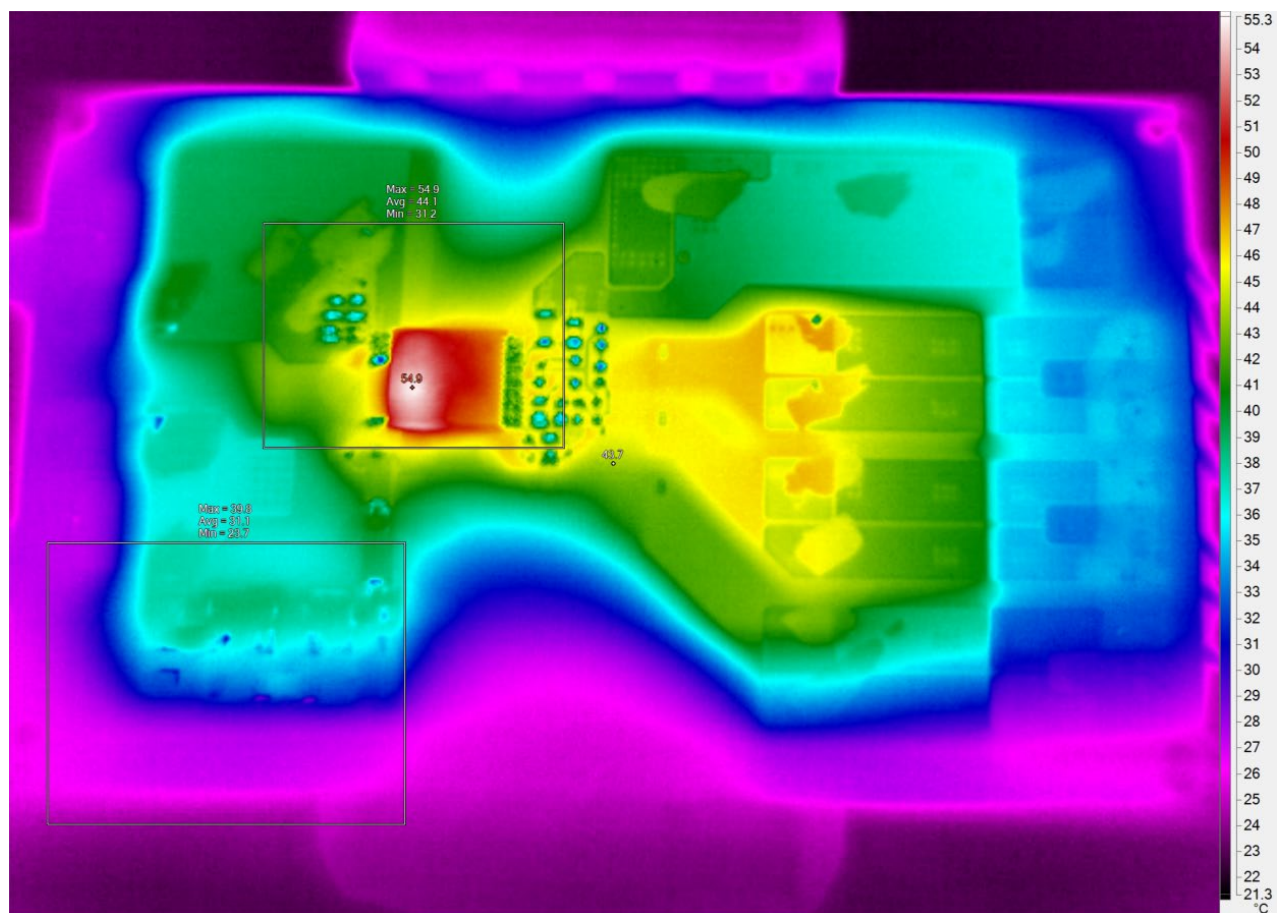


Figure 57 – PCB Top Thermal Scan at 1000 V_{DC} Input, Full Load.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by plugging the unit to a fully charged DC link capacitor⁹ at different input voltages. A constant resistive load configuration was used for all start up tests.

11.1.1 Output Voltage and Current at 85 °C Ambient^{10,11}

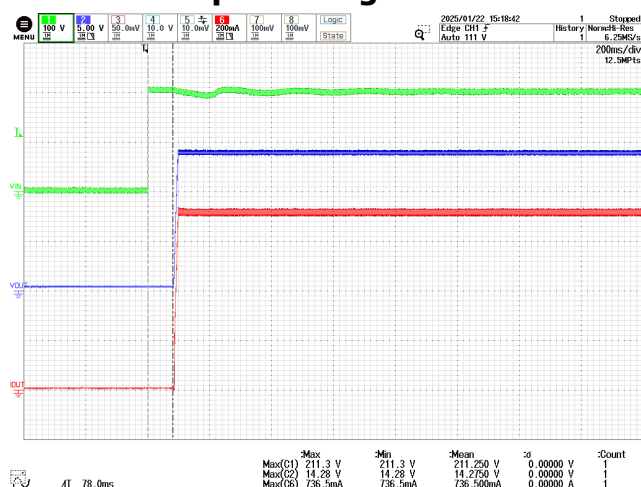


Figure 58 – 14 VOUT1 Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 200 mA / div.
Time: 200 ms / div.

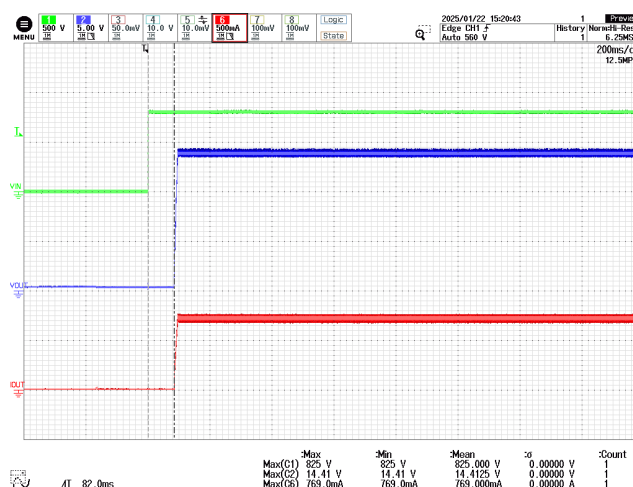


Figure 59 – 14 VOUT1 Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 200 mA / div.
Time: 200 ms / div.

⁹ Inrush current was limited by adding a 10 Ω series resistor between the DC-link capacitor and the unit under test.

¹⁰ The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load.

¹¹ Current waveforms were measured using a Yokogawa current probe. See Table 8 for list of equipment.

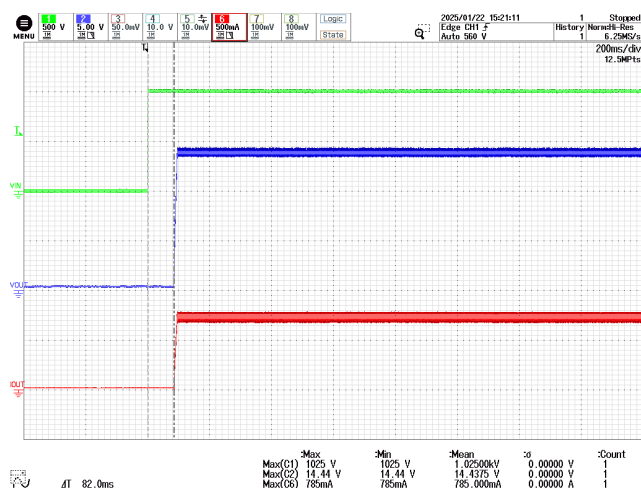


Figure 60 – 14 VOUT1 Output Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 200 mA / div.
Time: 200 ms / div.

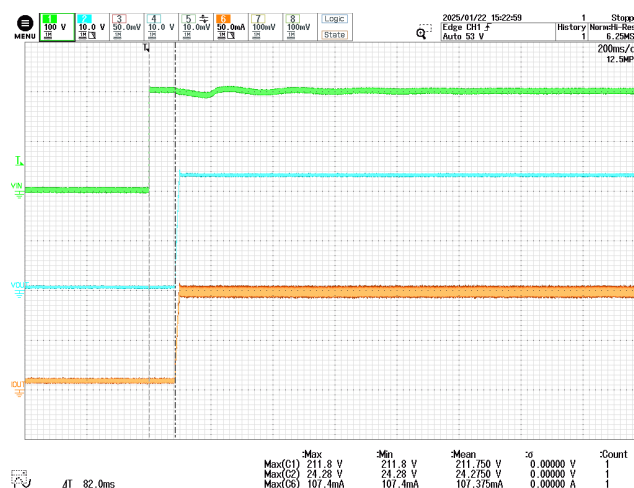


Figure 61 – 23 VOUT2 Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

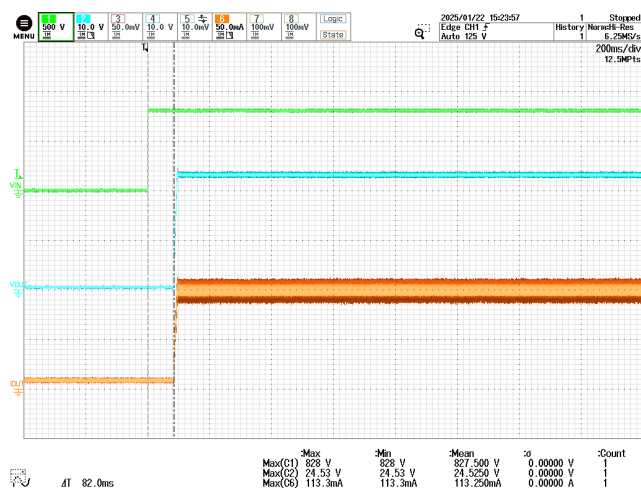


Figure 10 – 23 VOUT2 Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

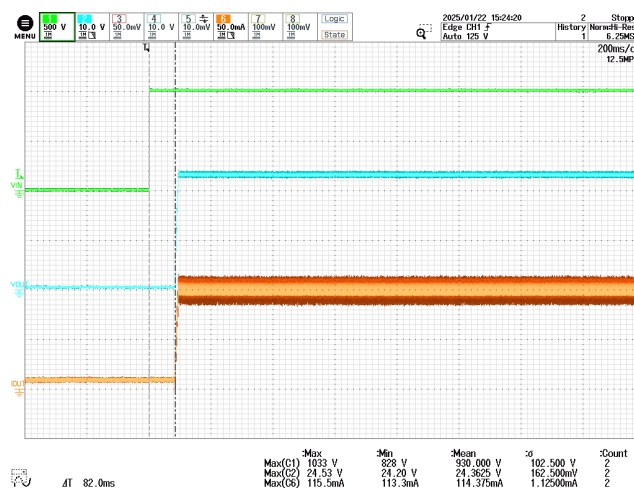


Figure 11 – 23 VOUT2 Output Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

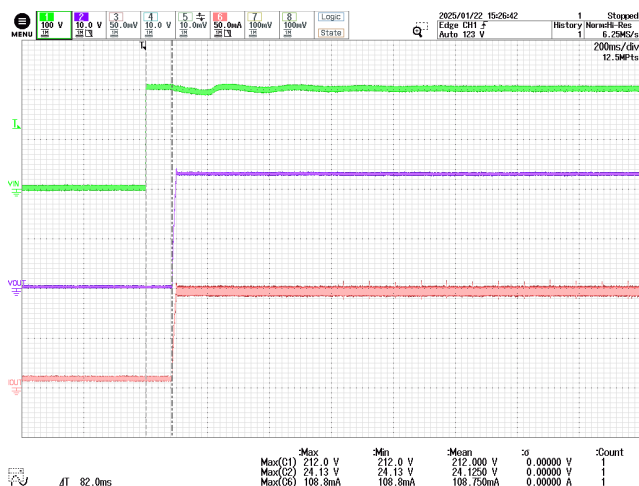


Figure 12 – 23 VOUT3 Output Voltage and Current.
200 V_{DC}, Full Load.

CH1: V_{IN}, 100 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

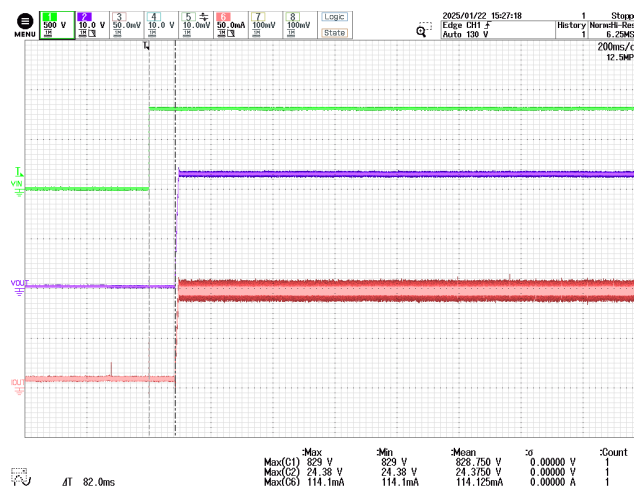


Figure 13 – 23 VOUT3 Output Voltage and Current.
800 V_{DC}, Full Load.

CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

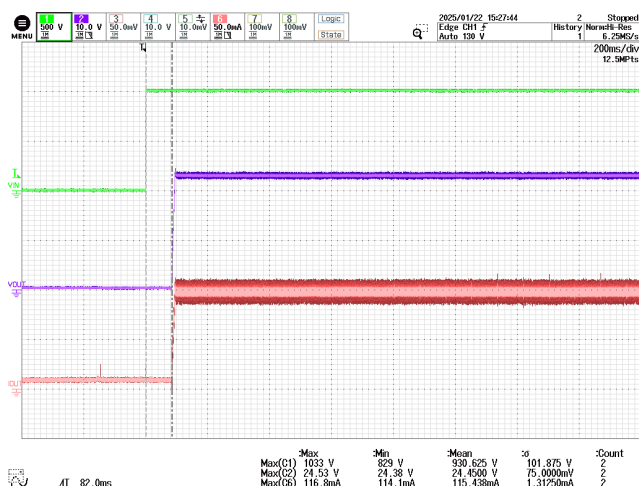


Figure 66 – 23 VOUT3 Output Voltage and Current.
1000 V_{DC}, Full Load.

CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

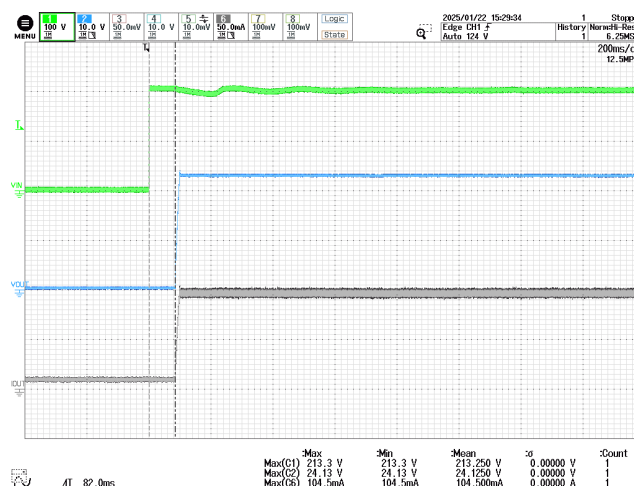


Figure 67 – 23 VOUT4 Output Voltage and Current.
200 V_{DC}, Full Load.

CH1: V_{IN}, 100 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

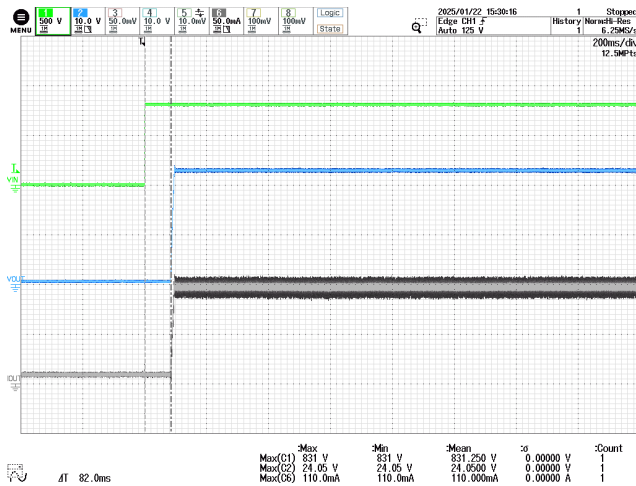


Figure 68 – 23VOUT4 Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

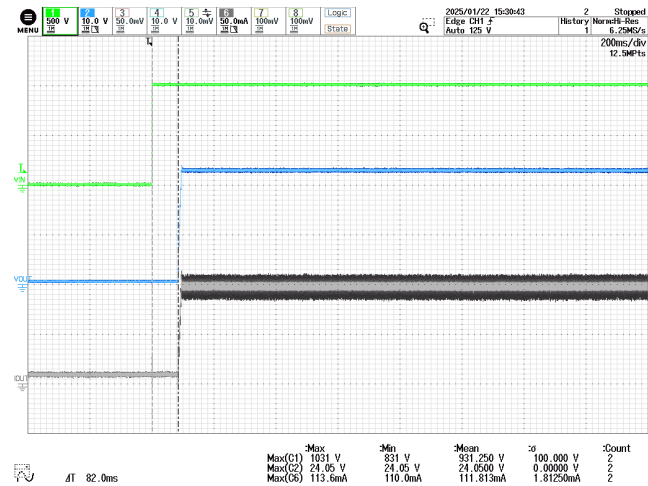


Figure 69 – 23VOUT4 Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85°C Ambient^{12,13}

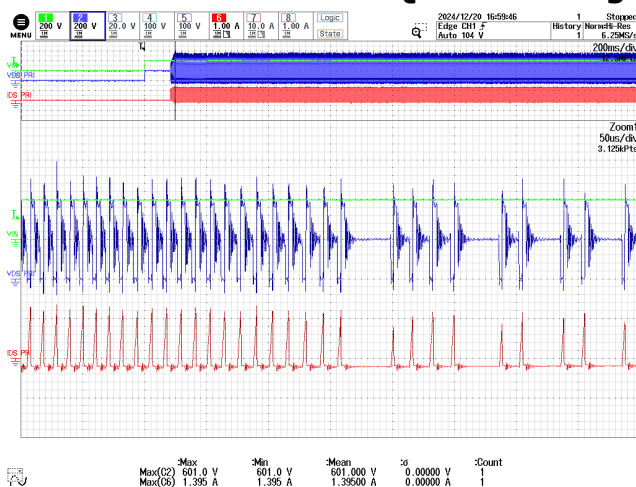


Figure 70 – INN3947FQ Drain Voltage and Current.
200 V_{DC}, Full Load.
CH2: V_{DS,INNO}, 200 V / div.
CH6: I_{D,INNO}, 1 A / div.
CH1: V_{IN}, 200 V / div.
Time: 200 ms / div.

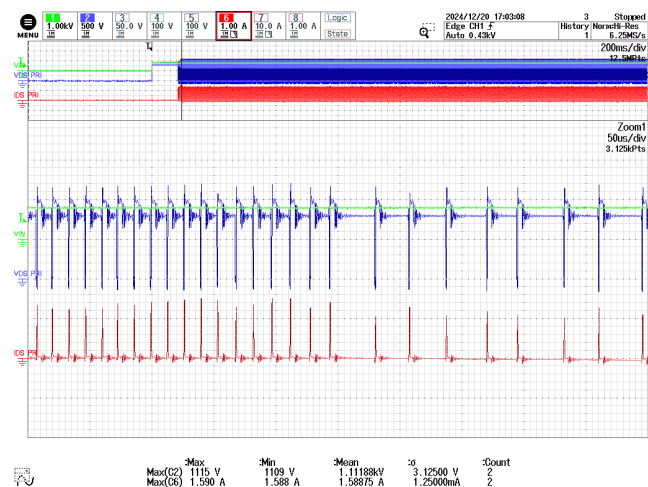


Figure 71 – INN3947FQ Drain Voltage and Current.
800 V_{DC}, Full Load.
CH2: V_{DS,INNO}, 500 V / div.
CH6: I_{D,INNO}, 1 A / div.
CH1: V_{IN}, 1000 V / div.
Time: 200 ms / div.

¹² The time between when V_{IN} turned on and the InnoSwitch3 starts switching is due to the “Wait and Listen” period of the InnoSwitch3.

¹³ Current waveforms were measured using a 30 A_{peak} Rogowski Coil, 5 MHz bandwidth-limited to reduce high frequency noise. See Table 8 for list of equipment.

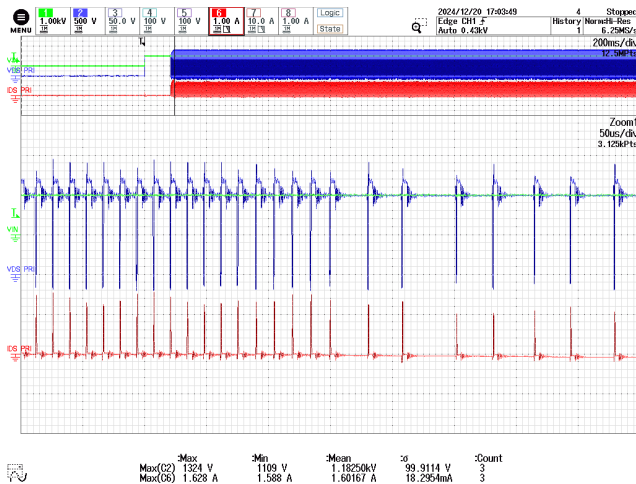


Figure 72 – INN3947FQ Drain Voltage and Current.
1000 V_{DC}, No Load.

CH1: V_{DS,INNO}, 500 V / div.

CH3: I_{D,INNO}, 1 A / div.

CH6: V_{IN}, 1000 V / div.

Time: 200 ms / div.

11.1.3 SR FET Drain Voltage and Current at 85 °C Ambient^{14,15}

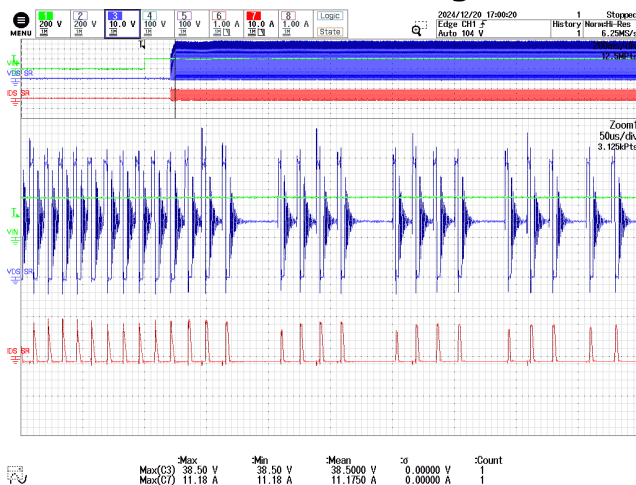


Figure 73 – SR FET Drain Voltage and Current.
200 V_{DC}, Full Load.

CH3: V_{DS,SR}, 10 V / div.

CH7: I_{D,SR}, 10 A / div.

CH1: V_{IN}, 200 V / div.

Time: 200 ms / div.

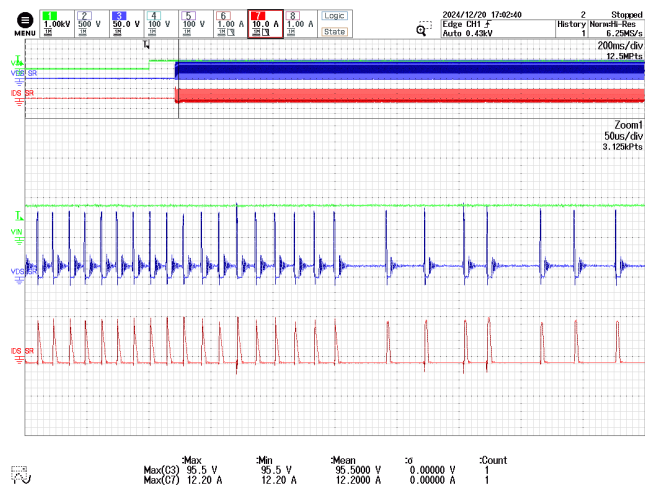


Figure 74 – SR FET Drain Voltage and Current.
800 V_{DC}, Full Load.

CH3: V_{DS,INNO}, 50 V / div.

CH7: I_{D,INNO}, 10 A / div.

CH1: V_{IN}, 1000 V / div.

Time: 200 ms / div.

¹⁴ The time between when V_{IN} turned on and the InnoSwitch3 starts switching is due to the “Wait and Listen” period of the InnoSwitch3.

¹⁵ Current waveforms were measured using a 120 A_{peak} Rogowski Coil, 5 MHz bandwidth-limited to reduce high frequency noise. See Table 8 for list of equipment.

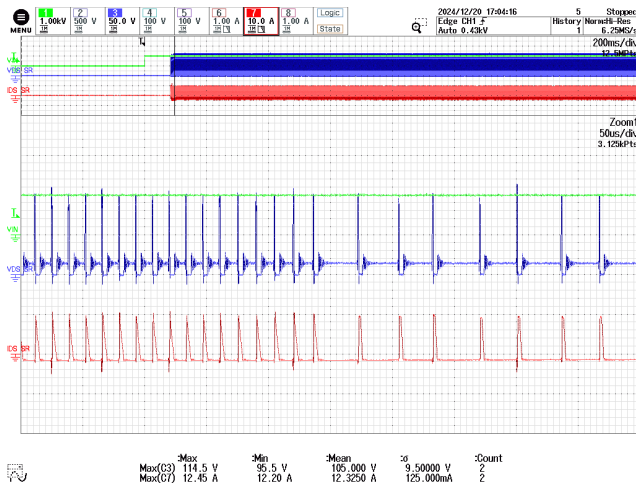


Figure 75 – SR FET Drain Voltage and Current.
1000 V_{DC}, Full Load.

CH2: V_{DS,INNO}, 50 V / div.

CH4: I_{D,INNO}, 10 A / div.

CH6: V_{IN}, 1000 V / div.

Time: 200 ms / div.

11.1.4 V_{DIODE} Drain Voltage and Current at 85 °C Ambient

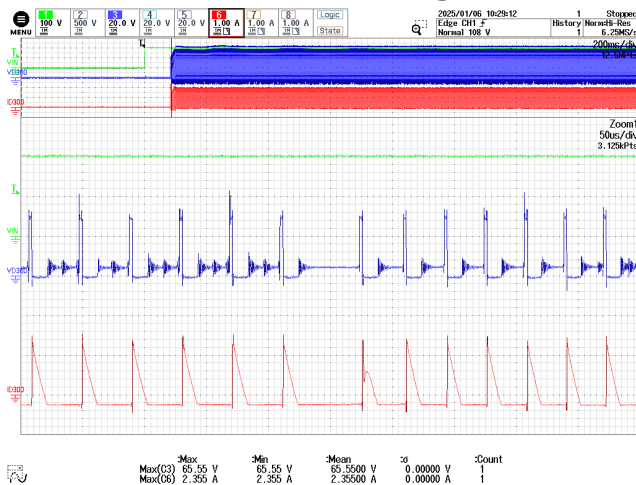


Figure 76 – V_{D300} Voltage and Current.
200 V_{DC}, Full Load.

CH1: V_{IN}, 100 V / div.

CH3: V_{D300}, 20 V / div.

CH6: I_{D300}, 1.00 A / div.

Time: 200 ms / div.

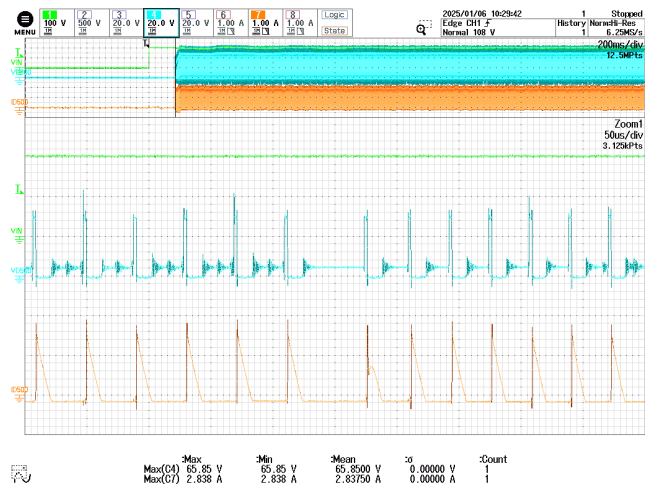


Figure 77 – V_{D500} Voltage and Current.
200 V_{DC}, Full Load.

CH1: V_{IN}, 100 V / div.

CH4: V_{D500}, 20 V / div.

CH7: I_{D500}, 1.00 A / div.

Time: 200 ms / div.

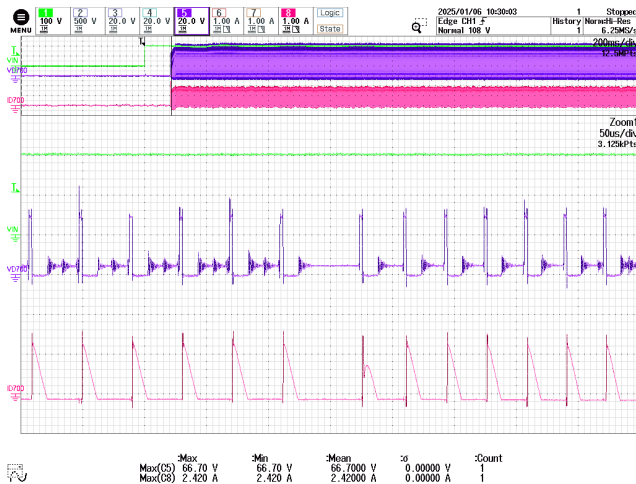


Figure 78 – V_{D700} Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH5: V_{OUT}, 20 V / div.
CH8: I_{OUT}, 1.00 A / div.
Time: 200 ms / div.

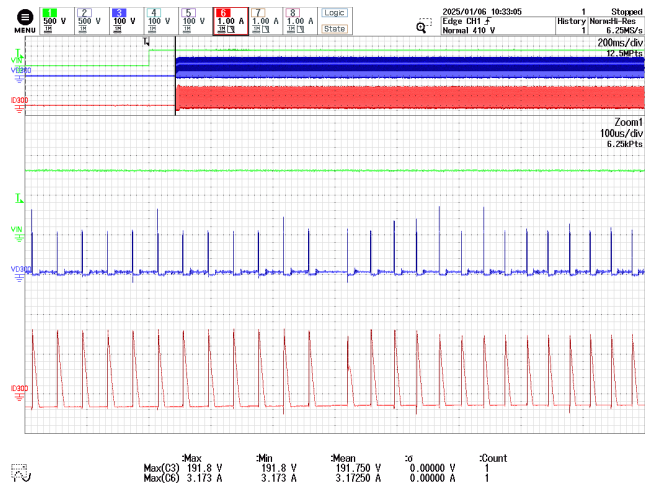


Figure 14 – V_{D300} Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH3: V_{D300}, 100 V / div.
CH6: I_{D300}, 1.00 A / div.
Time: 200 ms / div.

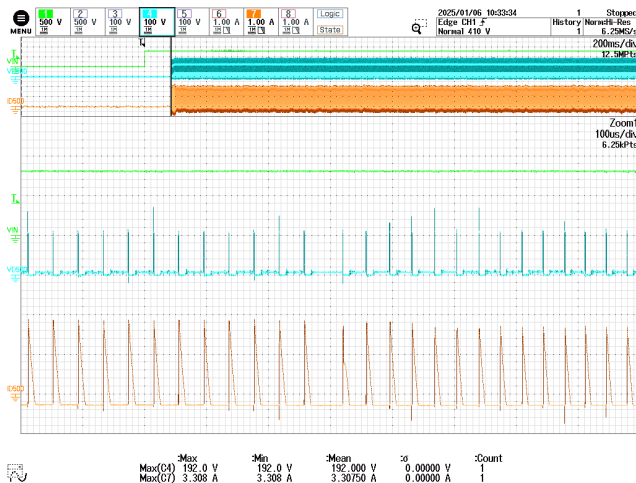


Figure 80 – V_{D500} Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH4: V_{D500}, 100 V / div.
CH7: I_{D500}, 1.00 A / div.
Time: 200 ms / div.

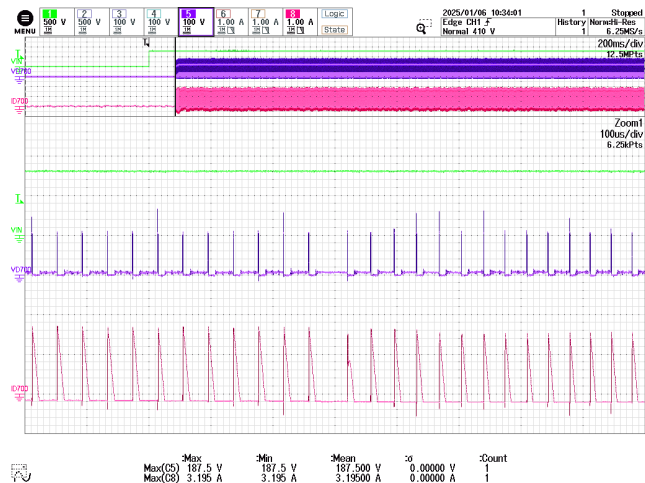


Figure 81 – Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH5: V_{OUT}, 100 V / div.
CH8: I_{OUT}, 1.00 A / div.
Time: 200 ms / div.

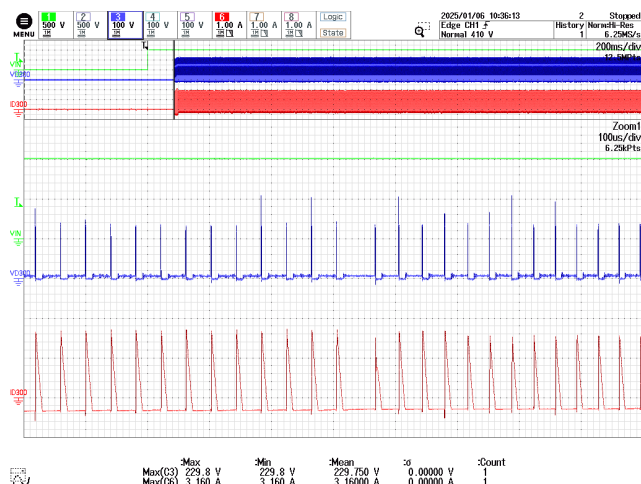


Figure 82 – V_{D300} Voltage and Current.
1000 V_{DC} , Full Load.

CH1: V_{IN} , 500 V / div.
CH3: V_{D300} , 100 V / div.
CH6: I_{D300} , 1.00 A / div.
Time: 200 ms / div.

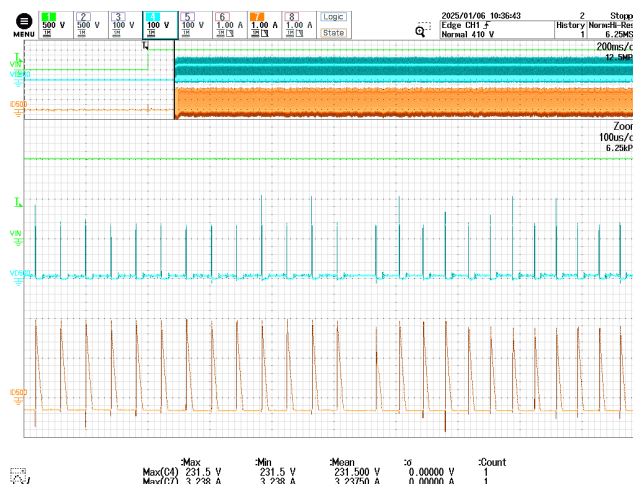


Figure 83 – V_{D500} Voltage and Current.
1000 V_{DC} , Full Load.

CH1: V_{IN} , 500 V / div.
CH4: V_{D500} , 100 V / div.
CH7: I_{D500} , 1.00 A / div.
Time: 200 ms / div.

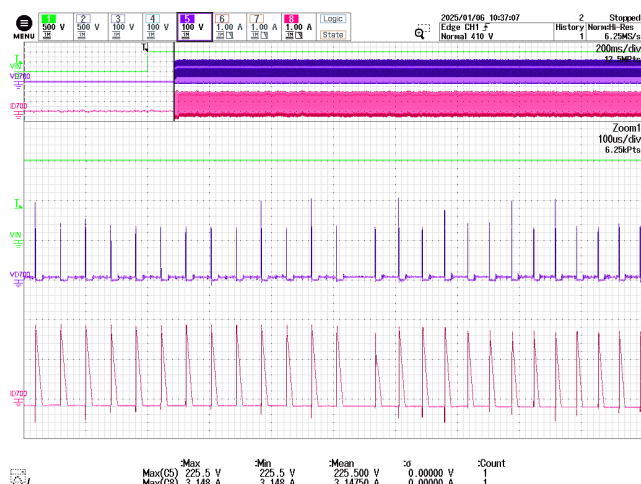


Figure 84 – Output Voltage and Current.
1000 V_{DC} , Full Load.

CH1: V_{IN} , 500 V / div.
CH5: V_{OUT} , 100 V / div.
CH8: I_{OUT} , 1.00 A / div.
Time: 200 ms / div.

11.1.5 Output Voltage and Current at -40 °C Ambient^{16,17}

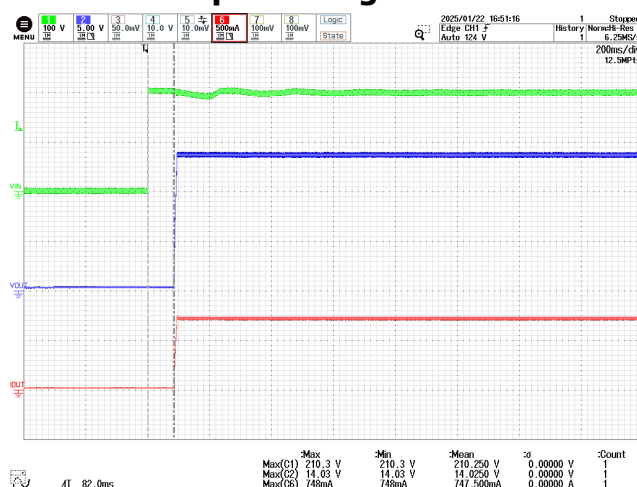


Figure 85 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 500 mA / div.
Time: 200 ms / div.

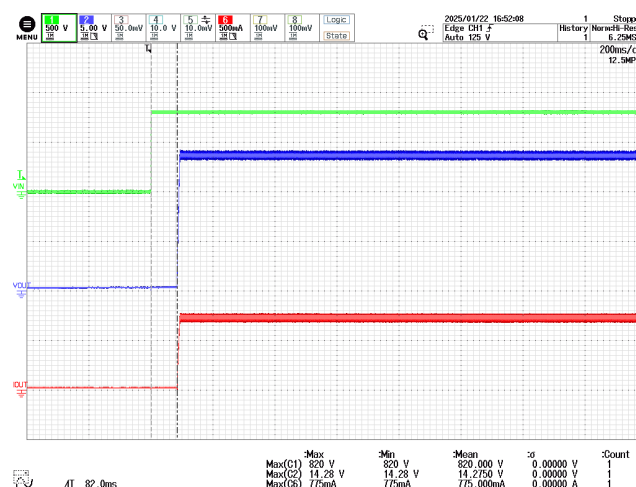


Figure 86 – Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 200 mA / div.
Time: 200 ms / div.

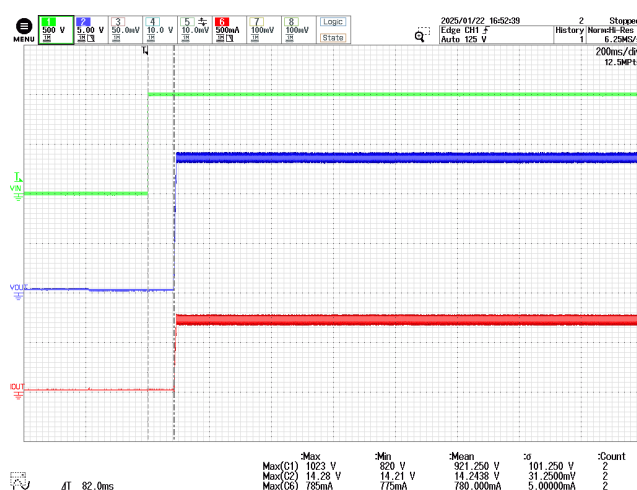


Figure 87 – Output Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT1}, 5 V / div.
CH6: I_{OUT1}, 200 mA / div.
Time: 200 ms / div.

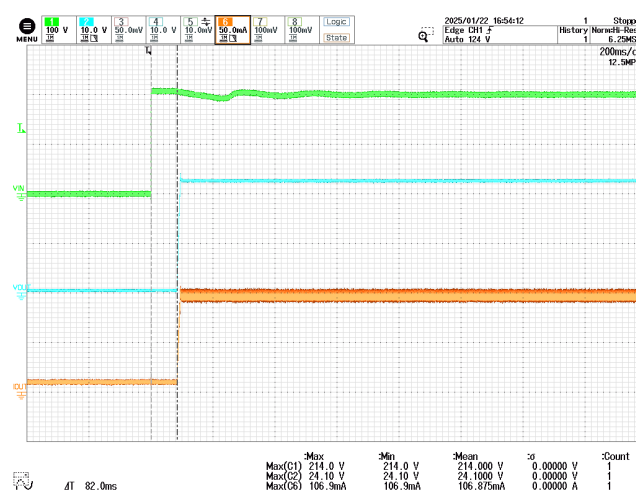


Figure 88 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

¹⁶ The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load.

¹⁷ Current waveforms were measured using a Yokogawa current probe. See Table 8 for list of equipment.

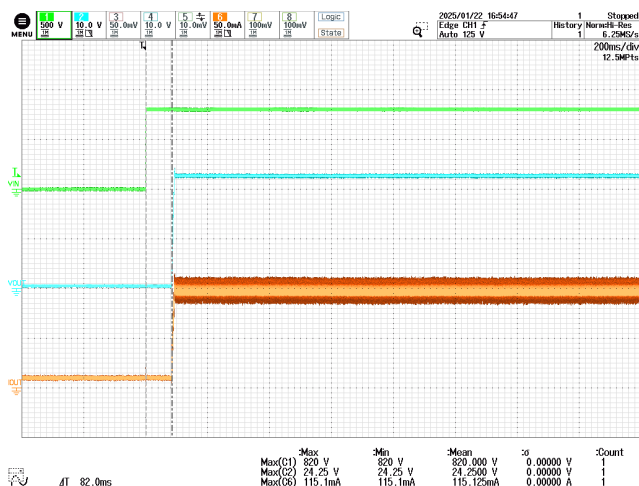


Figure 89 – Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

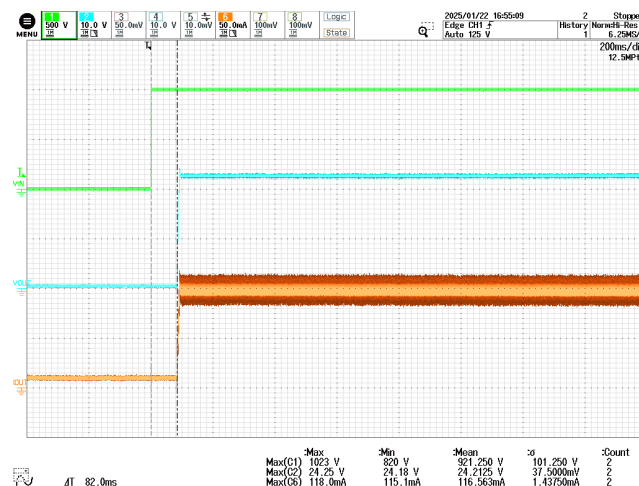


Figure 90 – Output Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT2}, 10 V / div.
CH6: I_{OUT2}, 50 mA / div.
Time: 200 ms / div.

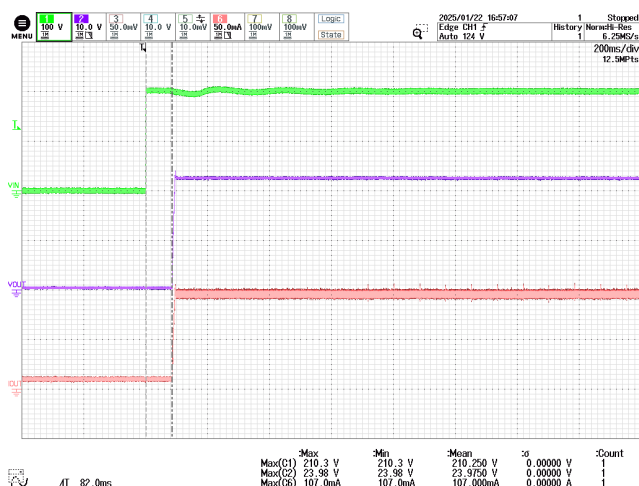


Figure 91 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

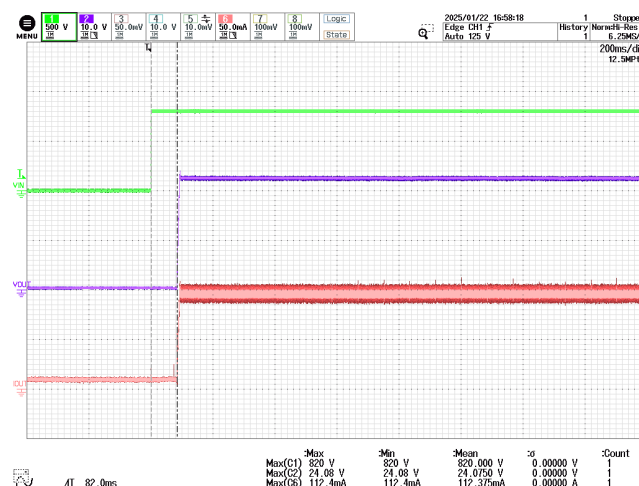


Figure 92 – Output Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

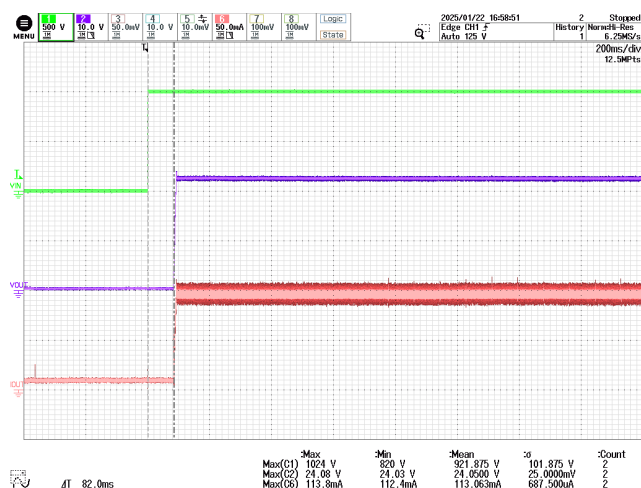


Figure 93 – Output Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

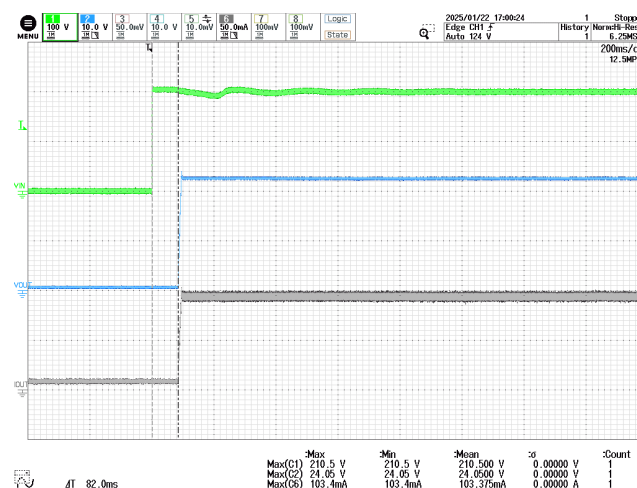


Figure 94 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

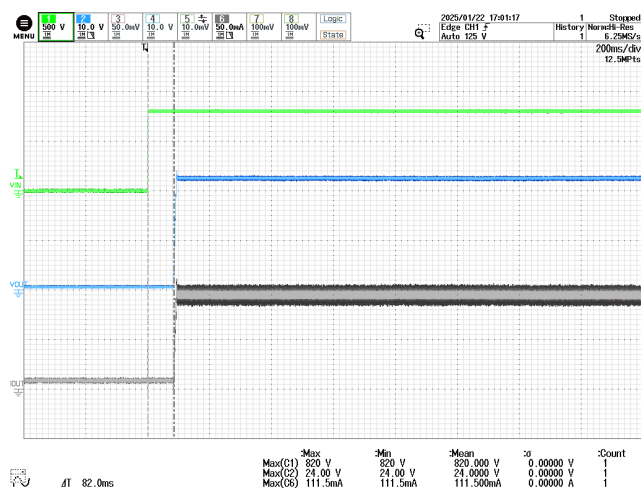


Figure 95 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

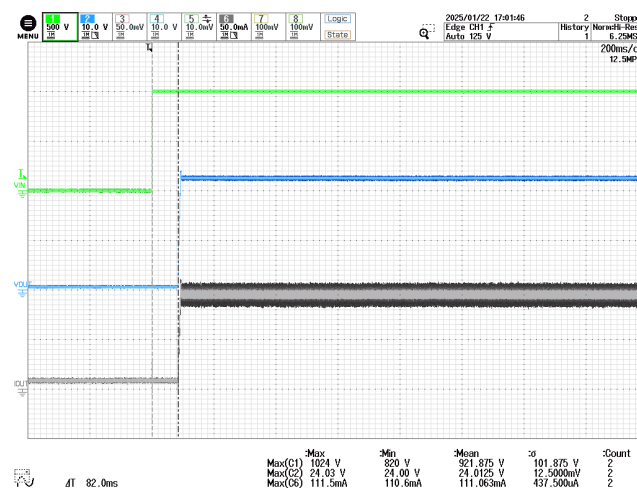


Figure 96 – Output Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT3}, 10 V / div.
CH6: I_{OUT3}, 50 mA / div.
Time: 200 ms / div.

11.1.6 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient^{18,19}

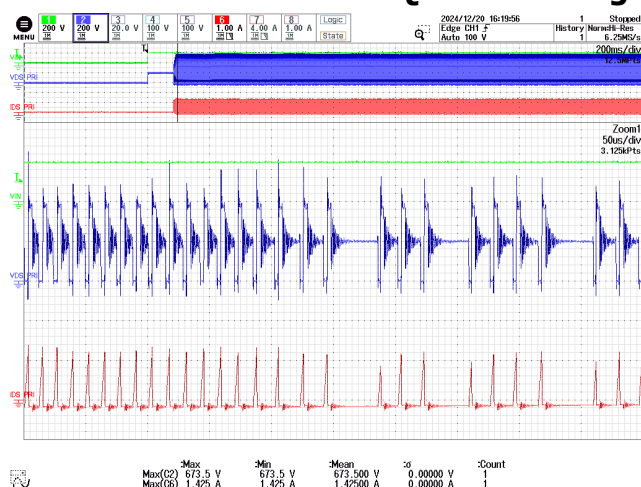


Figure 97 – INN3947FQ Drain Voltage and Current.
200 V_{DC}, Full Load.
CH2: V_{DS,INNO}, 200 V / div.
CH6: I_{D,INNO}, 1 A / div.
CH1: V_{IN}, 200 V / div.
Time: 200 ms / div.

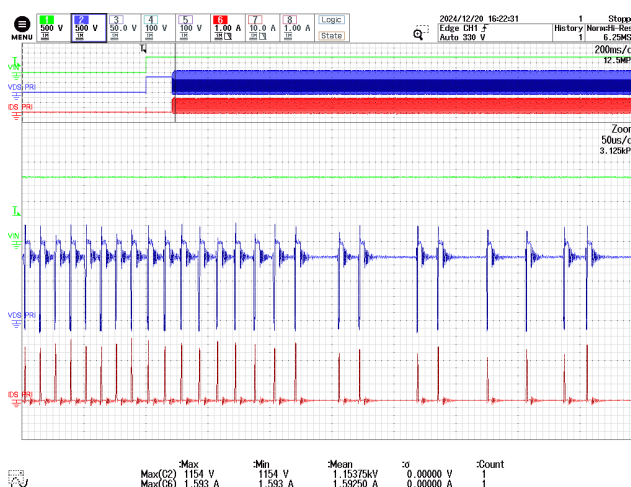


Figure 98 – INN3947FQ Drain Voltage and Current.
800 V_{DC}, Full Load.
CH3: V_{DS,INNO}, 500 V / div.
CH6: I_{D,INNO}, 1 A / div.
CH1: V_{IN}, 500 V / div.
Time: 200 ms / div.

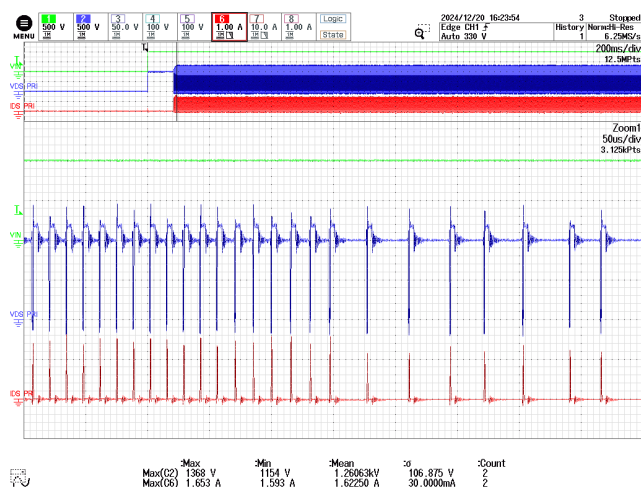


Figure 99 – INN3947FQ Drain Voltage and Current.
1000 V_{DC}, Full Load.
CH2: V_{DS,INNO}, 500 V / div.
CH6: I_{D,INNO}, 1 A / div.
CH1: V_{IN}, 500 V / div.
Time: 200 ms / div.

¹⁸ The time between when V_{IN} turned on and the InnoSwitch-3 IC starting to switch is due to the “Wait and Listen” period of the InnoSwitch3.

¹⁹ Current waveforms were measured using a 30 Apeak Rogowski Coil, 5 MHz bandwidth-limited to reduce high frequency noise. See Table 8 for list of equipment.

11.1.7 SR FET Drain Voltage and Current at -40 °C Ambient²⁰²¹

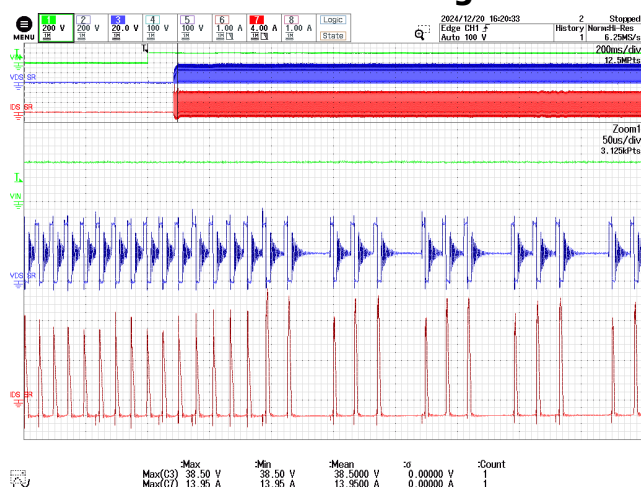


Figure 100 – SR FET Drain Voltage and Current.
200 V_{DC}, Full Load.
CH3: V_{DS,INNO}, 20 V / div.
CH7: I_{D,INNO}, 4 A / div.
CH1: V_{IN}, 200 V / div.
Time: 200 ms / div.

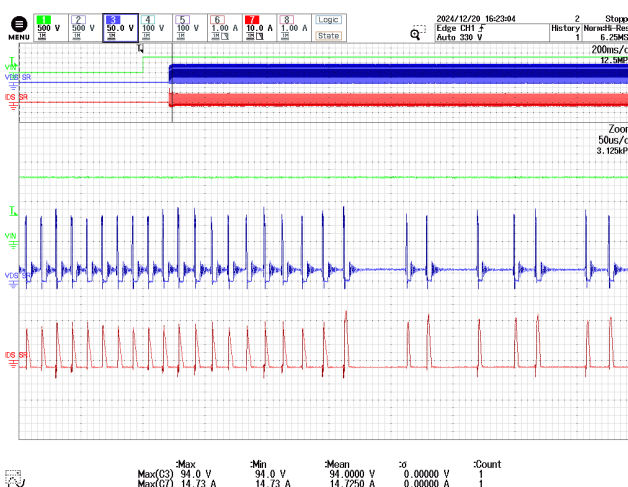


Figure 101 – SR FET Drain Voltage and Current.
800 V_{DC}, Full Load.
CH3: V_{DS,INNO}, 50 V / div.
CH7: I_{D,INNO}, 4 A / div.
CH1: V_{IN}, 500 V / div.
Time: 200 ms / div.

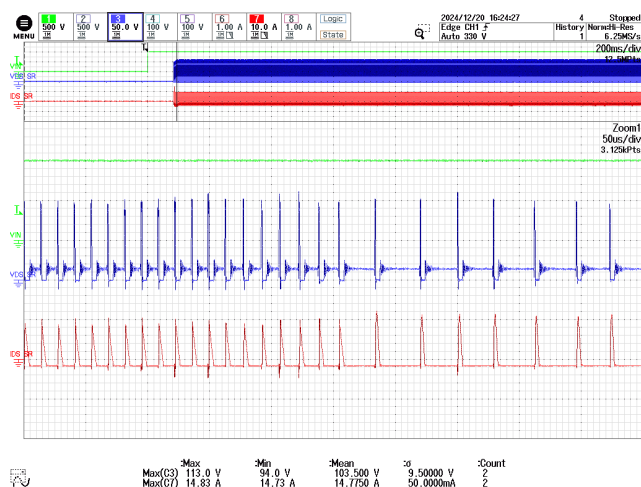


Figure 102 – SR FET Drain Voltage and Current.
1000 V_{DC}, Full Load.
CH3: V_{DS,INNO}, 50 V / div.
CH7: I_{D,INNO}, 4 A / div.
CH1: V_{IN}, 500 V / div.
Time: 200 ms / div.

²⁰ The time between when V_{IN} turned on and the InnoSwitch-3 IC starting to switch is due to the “Wait and Listen” period of the InnoSwitch-3.

²¹ Current waveforms were measured using a 300 A_{peak} Rogowski Coil, 5 MHz bandwidth-limited to reduce high frequency noise. See Table 8 for list of equipment.

11.1.8 V_{DIODE} Drain Voltage and Current at -40 °C Ambient

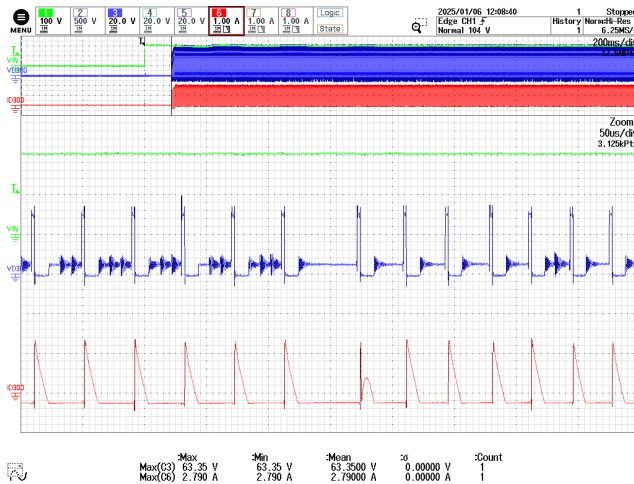


Figure 103 – V_{D300} Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH3: V_{D300}, 20 V / div.
CH6: I_{D300}, 1.00 A / div.
Time: 200 ms / div.

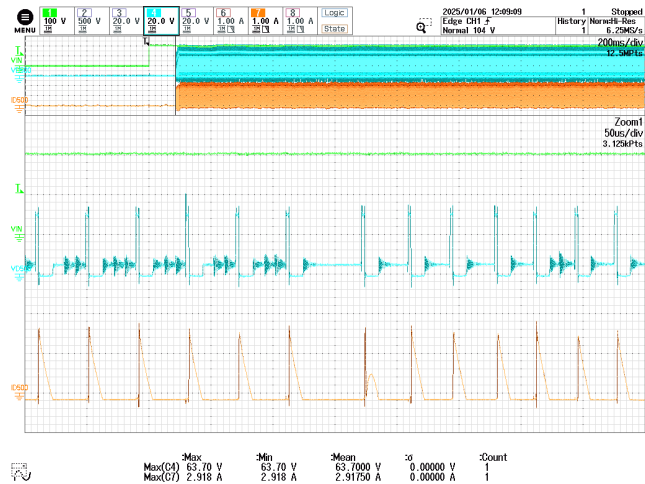


Figure 104 – V_{D500} Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH4: V_{D500}, 20 V / div.
CH7: I_{D500}, 1.00 A / div.
Time: 200 ms / div.

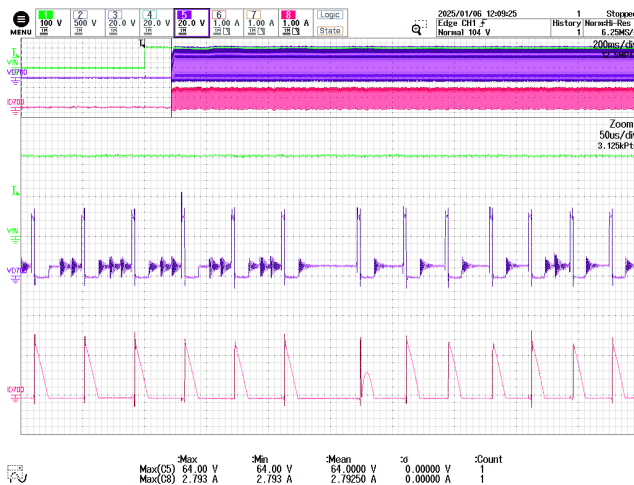


Figure 105 – V_{D700} Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{IN}, 100 V / div.
CH5: V_{OUT}, 20 V / div.
CH8: I_{OUT}, 1.00 A / div.
Time: 200 ms / div.

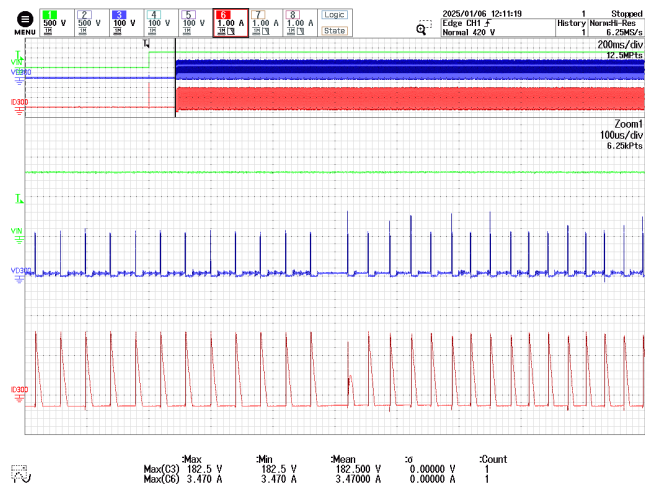


Figure 106 – V_{D300} Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{IN}, 500 V / div.
CH3: V_{D300}, 100 V / div.
CH6: I_{D300}, 1.00 A / div.
Time: 200 ms / div.

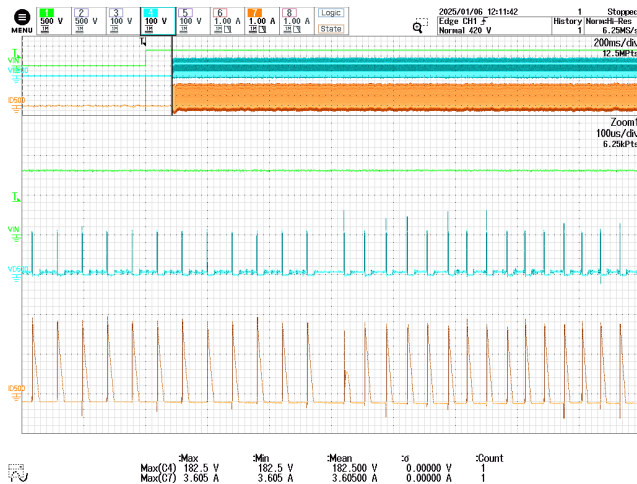


Figure 107 – V_{D500} Voltage and Current.
800 V_{DC} , Full Load.
CH1: V_{IN} , 500 V / div.
CH4: V_{D500} , 100 V / div.
CH7: I_{D500} , 1.00 A / div.
Time: 200 ms / div.

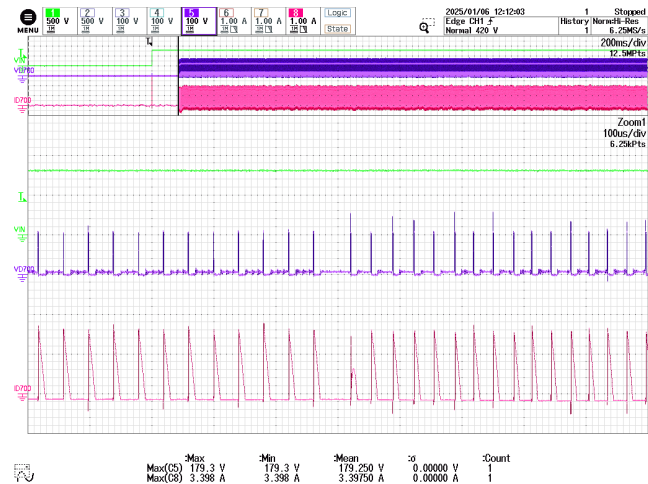


Figure 108 – Output Voltage and Current.
800 V_{DC} , Full Load.
CH1: V_{IN} , 500 V / div.
CH5: V_{OUT} , 100 V / div.
CH8: I_{OUT} , 1.00 A / div.
Time: 200 ms / div.

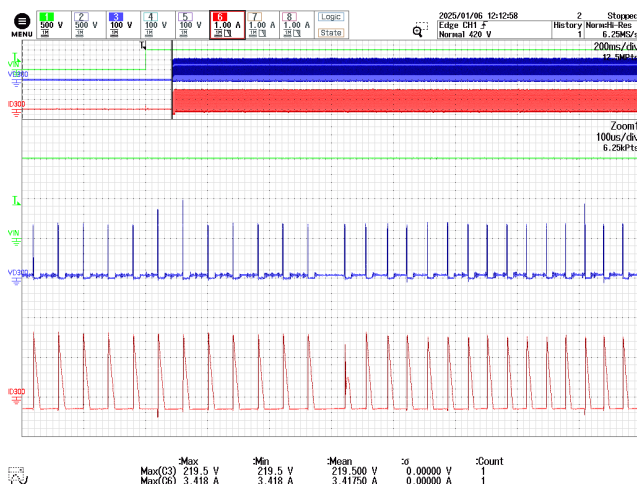


Figure 109 – V_{D300} Voltage and Current.
1000 V_{DC} , Full Load.
CH1: V_{IN} , 500 V / div.
CH3: V_{D300} , 100 V / div.
CH6: I_{D300} , 1.00 A / div.
Time: 200 ms / div.

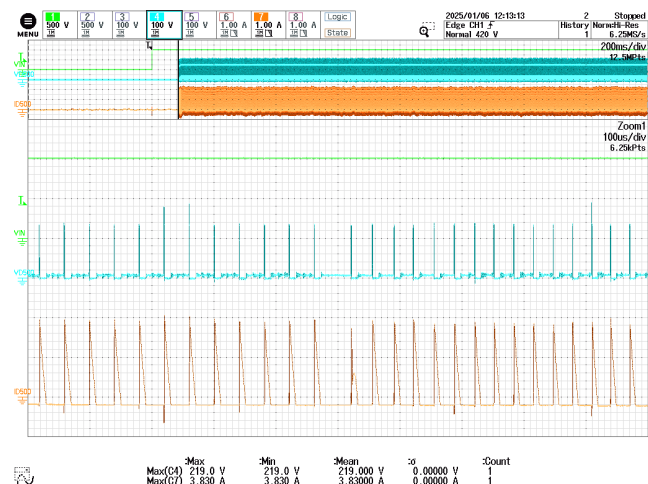


Figure 110 – V_{D500} Voltage and Current.
1000 V_{DC} , Full Load.
CH1: V_{IN} , 500 V / div.
CH4: V_{D500} , 100 V / div.
CH7: I_{D500} , 1.00 A / div.
Time: 200 ms / div.

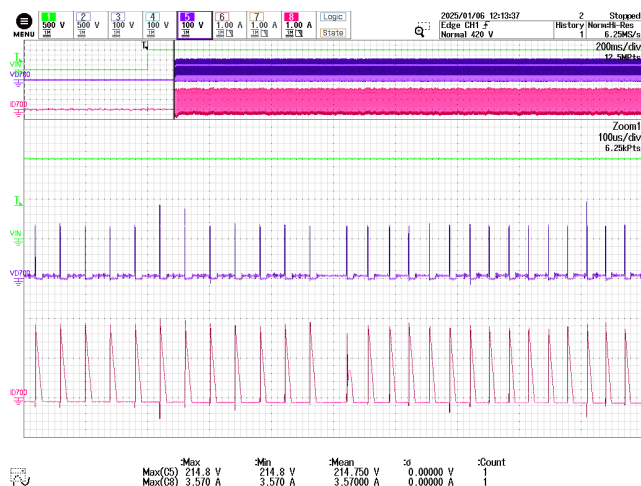


Figure 111 – Output Voltage and Current.

1000 V_{DC}, Full Load.

CH1: V_{IN}, 500 V / div.

CH5: V_{OUT}, 100 V / div.

CH8: I_{OUT}, 1.00 A / div.

Time: 200 ms / div.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C Ambient

11.2.1.1 Normal Operation Component Stress

Steady-State Switching Waveforms 85 °C Ambient								
Input	14 V Output	23 V Outputs*	INN3947FQ		14 V SR FET		23 V Freewheeling Diodes	
V _{IN} (V)	I _{OUT} (mA)	I _{OUT} (mA)	IC200 V _{DS} (V)	V _{STRESS} (%)	Q100 V _{DS} (V)	V _{STRESS} (%)	D300, D500, D700 (V _{KA})	V _{STRESS} (%)
200	714	87	560	32.9	38.8	25.9	72.8	18.2
	714	3	550	32.1	39.5	26.3	78.5	19.6
	0	87	510	30	39	26	69.8	17.5
800	714	87	1105	65	96	64	200	50
	714	3	1120	65.9	96.3	64.2	204	51
	0	87	1098	64.6	96	64	197	49.3
1000	714	87	1315	77.4	116	77	237	59.3
	714	3	1338	78.7	116	77.3	242	60.5
	0	87	1295	76.2	116	77.3	235	58.8

Table 11 – Summary of Voltage Stress on Critical Components at 85 °C Ambient.

11.2.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient

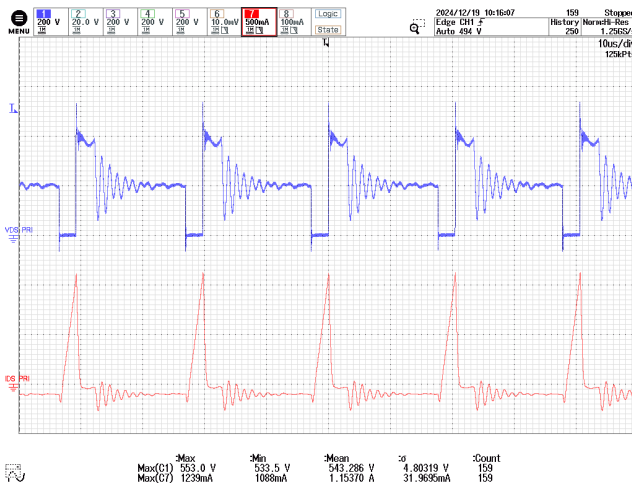


Figure 112 – INN3947FQ Drain Voltage and Current.
 200 V_{DC}, Full Load.
 CH1: V_{DS, INNO}, 200 V / div.
 CH7: I_{D, INNO}, 500 mA / div.
 Time: 10 μs / div.



Figure 113 – INN3947FQ Drain Voltage and Current.
 800 V_{DC}, Full Load.
 CH1: V_{DS, INNO}, 200 V / div.
 CH7: I_{D, INNO}, 500 mA / div.
 Time: 10 μs / div.

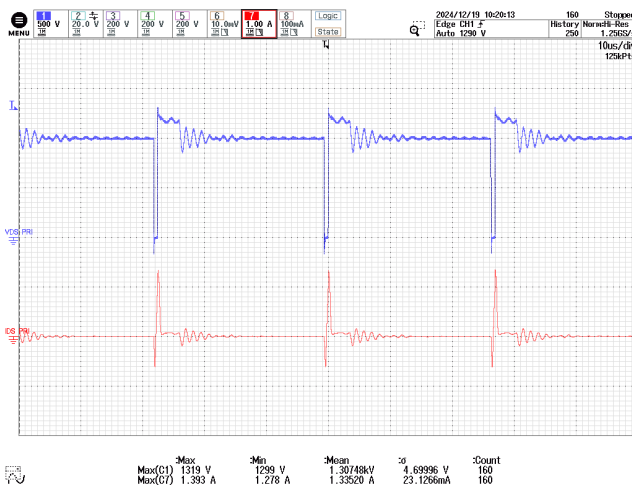


Figure 114 – INN3947FQ Drain Voltage and Current.
 1000 V_{DC}, Full Load.
 CH1: V_{DS, INNO}, 500 V / div.
 CH3: I_{D, INNO}, 1.00 A / div.
 Time: 10 μs / div.

11.2.1.3 SR FET Drain Voltage and Current at 85 °C Ambient

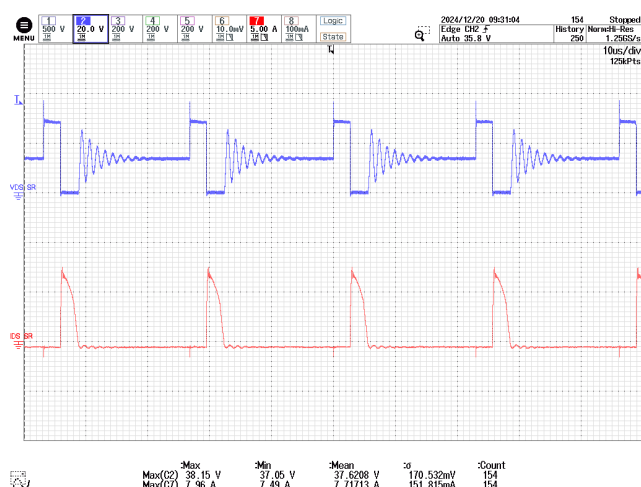


Figure 115 – SR FET Drain Voltage and Current.
200 V_{DC}, Full Load.
CH2: V_{DS,SR}, 20 V / div.
CH7: I_{D,SR}, 5 A / div.
Time: 10 μs / div.



Figure 116 – SR FET Drain Voltage and Current.
800 V_{DC}, Full Load.
CH2: V_{DS,SR}, 50 V / div.
CH7: I_{D,SR}, 5 A / div.
Time: 10 μs / div.

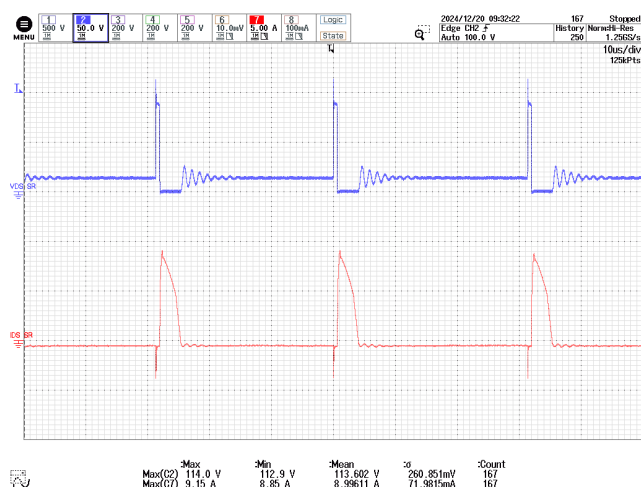


Figure 117 – SR FET Drain Voltage and Current.
1000 V_{DC}, Full Load.
CH2: V_{DS,SR}, 50 V / div.
CH7: I_{D,SR}, 5 A / div.
Time: 10 μs / div.

11.2.1.4 V_{DIODE} Voltage and Current at 85 °C Ambient

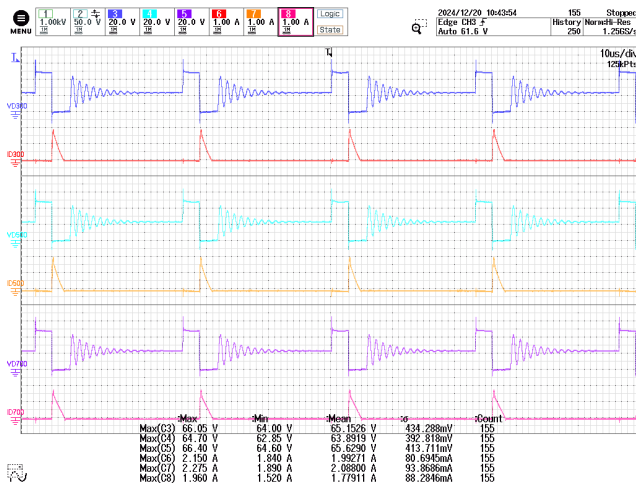


Figure 118 – V_{DIODE} Voltage and Current.

200 V_{DC}, Full Load.

CH3: V_{D300}, 20 V / div.

CH4: V_{D500}, 20 V / div.

CH5: V_{D700}, 20 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 µs / div.

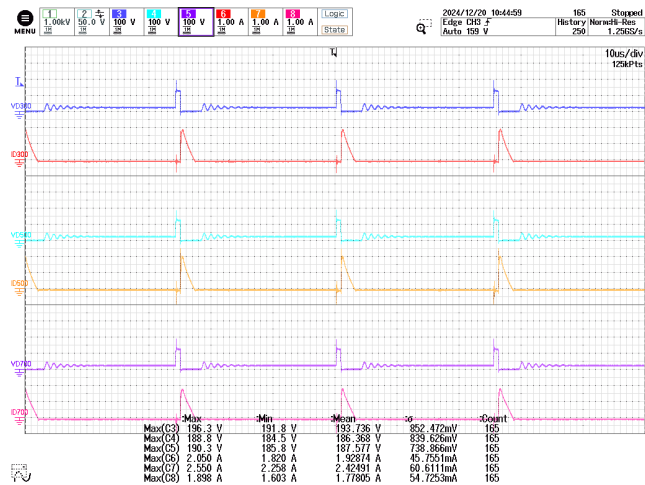


Figure 119 – V_{DIODE} Voltage and Current.

800 V_{DC}, Full Load.

CH3: V_{D300}, 100 V / div.

CH4: V_{D500}, 100 V / div.

CH5: V_{D700}, 100 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 µs / div.

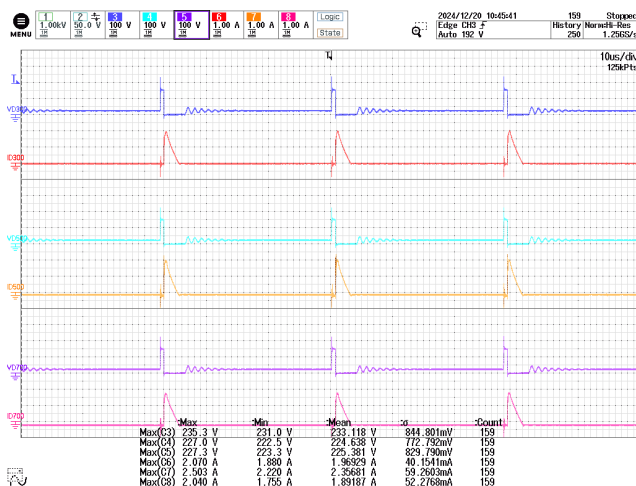


Figure 120 – V_{DIODE} Voltage and Current.

1000 V_{DC}, Full Load.

CH3: V_{D300}, 100 V / div.

CH4: V_{D500}, 100 V / div.

CH5: V_{D700}, 100 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 µs / div.

11.2.1.5 Short Circuit Response at 85 °C Ambient

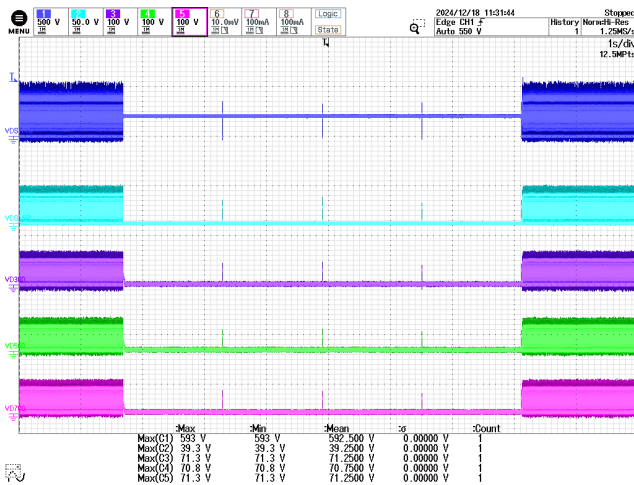


Figure 121 – INN3947FQ, SR FET, and V_{DIODE} Voltages. 200 V_{DC}, Full Load.

CH1: $V_{DS,INNO}$, 500 V / div.

CH2: $V_{DS,SR}$, 50 V / div.

CH3: V_{D300} , 100 V / div.

CH4: V_{D500} , 100 V / div.

CH5: V_{D700} , 100 V / div.

Time: 1 s / div.

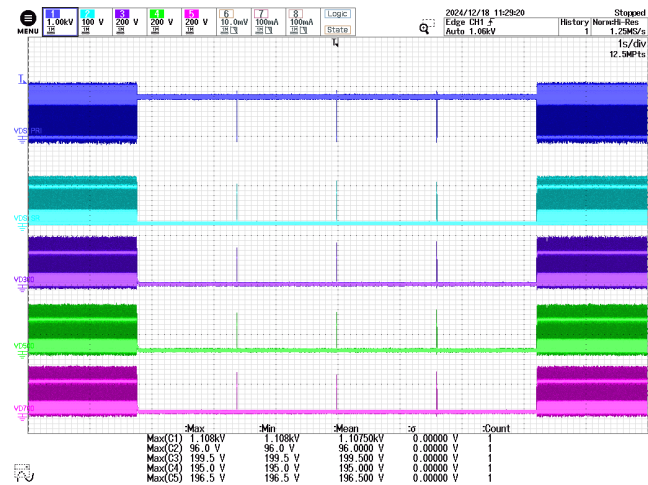


Figure 122 – V_{DIODE} Voltage and Current. 800 V_{DC}, Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

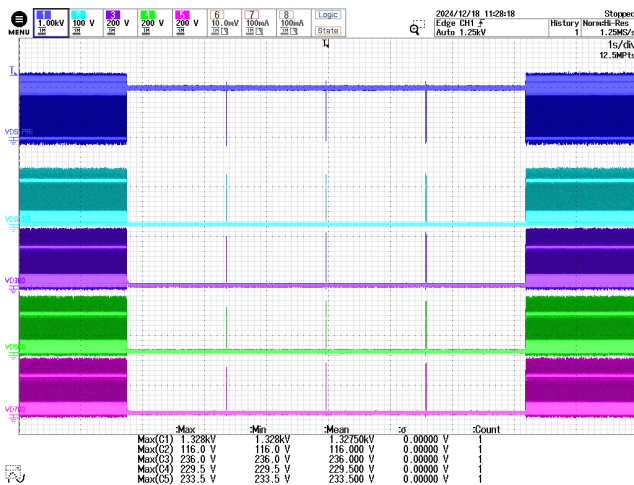


Figure 123 – V_{DIODE} Voltage and Current. 1000 V_{DC}, Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

11.2.2 Switching Waveforms at 25 °C Ambient

11.2.2.1 Normal Operation Component Stress

Steady-State Switching Waveforms 85 °C Ambient								
Input	14 V Output	23 V Outputs*	INN3947FQ		14 V SR FET		23 V Freewheeling Diodes	
V _{IN} (V)	I _{OUT} (mA)	I _{OUT} (mA)	IC200 V _{DS} (V)	V _{STRESS} (%)	Q100 V _{DS} (V)	V _{STRESS} (%)	D300, D500, D700 (V _{KA})	V _{STRESS} (%)
200	714	87	559	32.9	41	27.3	70.5	17.6
	714	3	546	32.1	40.3	26.9	75.8	19
	0	87	510	30	41	27.3	69.5	17.4
800	714	87	1098	64.6	104	69.5	189	47.3
	714	3	1100	64.7	103	68.7	195	48.8
	0	87	1075	63.2	104	69.5	189	47.6
1000	714	87	1295	76.2	123	81.9	226	56.5
	714	3	1315	77.4	123	82	230	57.5
	0	87	1293	76.1	123	82	226	56.9

Table 12 – Summary of Voltage Stress on Critical Components at 25 °C Ambient.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient



Figure 124 – INN3947FQ Drain Voltage and Current.
 200 V_{DC}, Full Load.
 CH1: V_{DS,INNO}, 200 V / div.
 CH7: I_{D,INNO}, 1 A / div.
 Time: 10 μs / div.



Figure 125 – INN3947FQ Drain Voltage and Current.
 800 V_{DC}, Full Load.
 CH1: V_{DS,INNO}, 500 V / div.
 CH7: I_{D,INNO}, 1 A / div.
 Time: 10 μs / div.



Figure 126 – INN3947FQ Drain Voltage and Current.
 1000 V_{DC}, Full Load.
 CH1: V_{DS,INNO}, 500 V / div.
 CH3: I_{D,INNO}, 1.00 A / div.
 Time: 10 μs / div.

11.2.2.3 SR FET Drain Voltage and Current at 25 °C Ambient

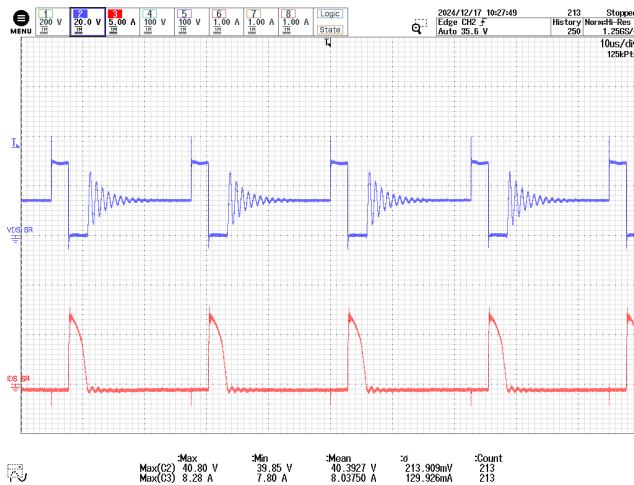


Figure 127 – SR FET Drain Voltage and Current.
200 V_{DC}, Full Load.
CH2: V_{DS,SR}, 20 V / div.
CH3: I_{D,SR}, 5 A / div.
Time: 10 μs / div.

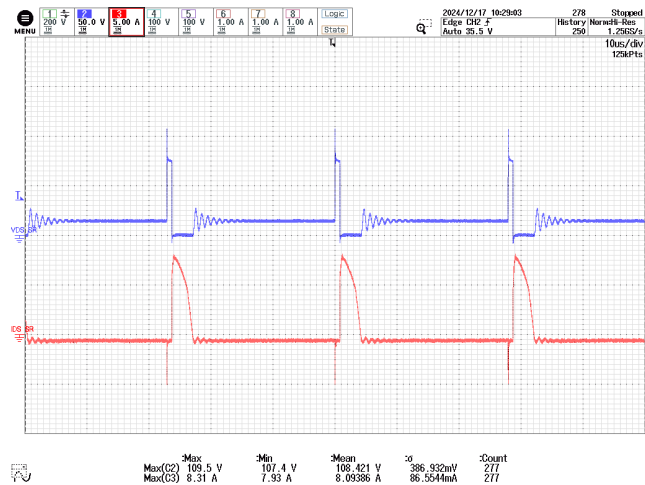


Figure 128 – SR FET Drain Voltage and Current.
800 V_{DC}, Full Load.
CH2: V_{DS,SR}, 50 V / div.
CH3: I_{D,SR}, 5 A / div.
Time: 10 μs / div.



Figure 129 – SR FET Drain Voltage and Current.
1000 V_{DC}, Full Load.
CH2: V_{DS,SR}, 50 V / div.
CH3: I_{D,SR}, 5 A / div.
Time: 10 μs / div.

11.2.2.4 V_{DIODE} Voltage and Current at 25 °C Ambient

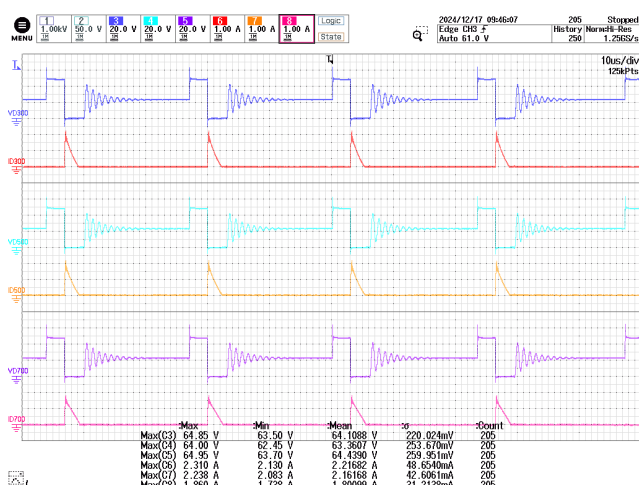


Figure 130 – V_{DIODE} Voltage and Current.

200 V_{DC}, Full Load.

CH3: V_{D300}, 20 V / div.

CH4: V_{D500}, 20 V / div.

CH5: V_{D700}, 20 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μs / div.

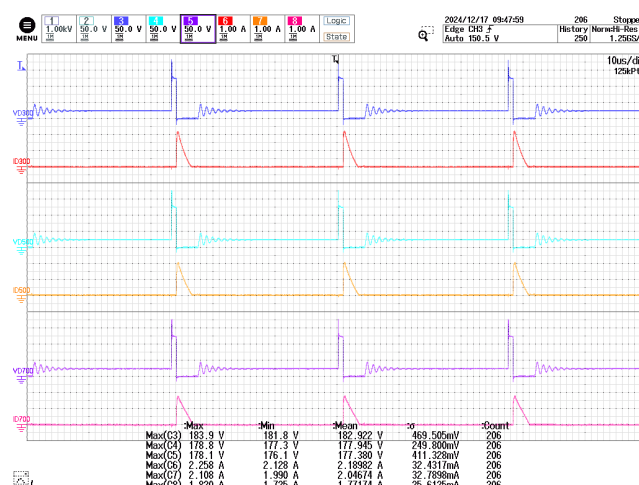


Figure 131 – V_{DIODE} Voltage and Current.

800 V_{DC}, Full Load.

CH3: V_{D300}, 50 V / div.

CH4: V_{D500}, 50 V / div.

CH5: V_{D700}, 50 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μs / div.

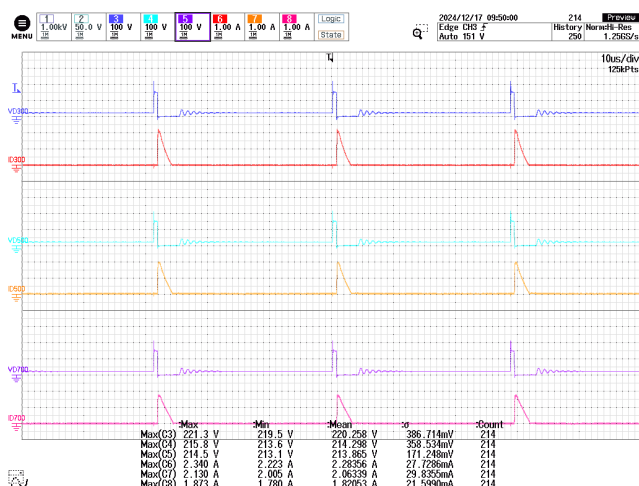


Figure 132 – V_{DIODE} Voltage and Current.

1000 V_{DC}, Full Load.

CH3: V_{D300}, 100 V / div.

CH4: V_{D500}, 100 V / div.

CH5: V_{D700}, 100 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μs / div.

11.2.2.5 Short Circuit Response at 25 °C Ambient

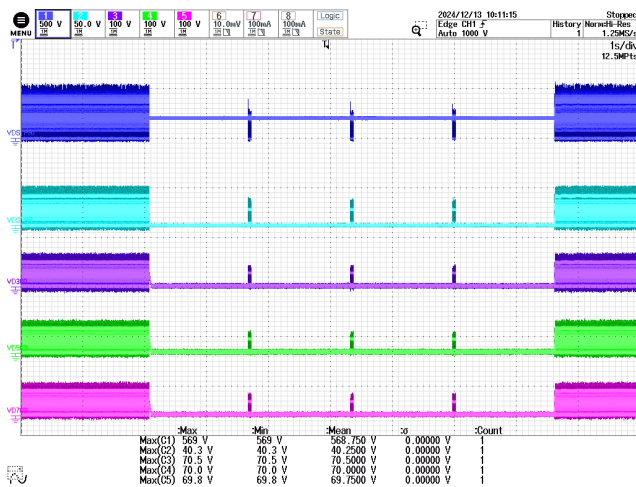


Figure 133 – INN3947FQ, SR FET, and V_{DIODE} Voltages. 200 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 500 V / div.

CH2: $V_{DS,SR}$, 50 V / div.

CH3: V_{D300} , 100 V / div.

CH4: V_{D500} , 100 V / div.

CH5: V_{D700} , 100 V / div.

Time: 1 s / div.

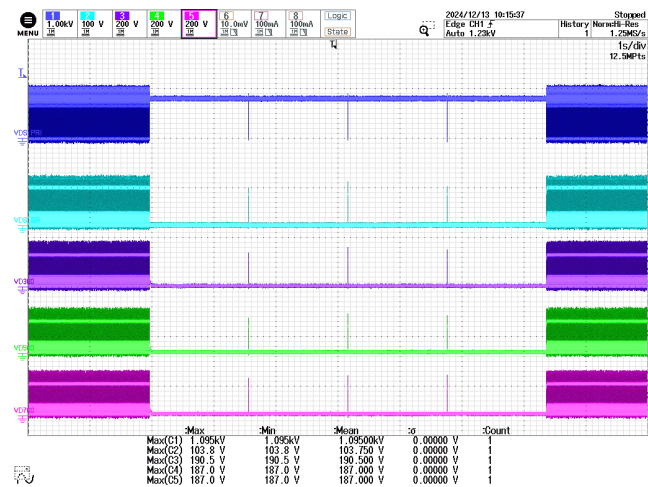


Figure 134 – V_{DIODE} Voltage and Current. 800 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

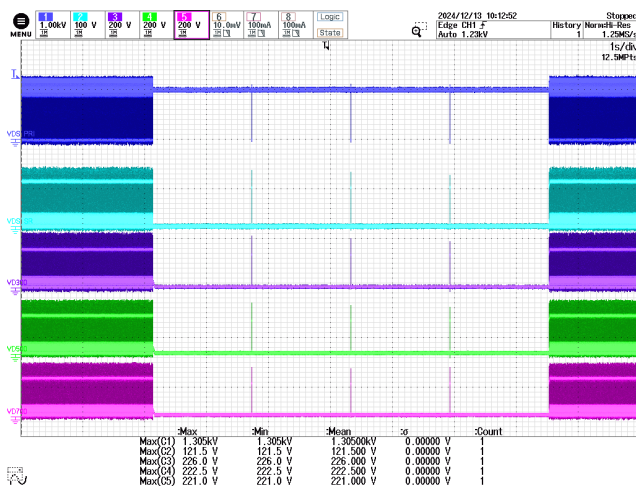


Figure 135 – V_{DIODE} Voltage and Current. 1000 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

11.2.3 Switching Waveforms at -40 °C Ambient

11.2.3.1 Normal Operation Component Stress

Steady-State Switching Waveforms 85 °C Ambient								
Input	14 V Output	23 V Outputs*	INN3947FQ		14 V SR FET		23 V Freewheeling Diodes	
V _{IN} (V)	I _{OUT} (mA)	I _{OUT} (mA)	IC200 V _{DS} (V)	V _{STRESS} (%)	Q100 V _{DS} (V)	V _{STRESS} (%)	D300, D500, D700 (V _{KA})	V _{STRESS} (%)
200	714	87	578	34.0	40.0	26.7	71.3	17.8
	714	3	560	32.9	39.9	26.6	77.5	19.4
	0	87	516	30.4	39.6	26.4	69.0	17.6
800	714	87	1123	66.1	96.0	64.0	191	47.8
	714	3	1135	66.8	96.0	64.0	199	49.6
	0	87	1110	65.3	96.0	64.0	189	47.3
1000	714	87	1340	78.8	116	77.0	230	57.5
	714	3	1355	79.7	116	77.3	231	57.6
	0	87	1305	76.8	115	76.3	224	56.0

Table 13 – Summary of Voltage Stress on Critical Components at -40 °C Ambient.

11.2.3.2 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient

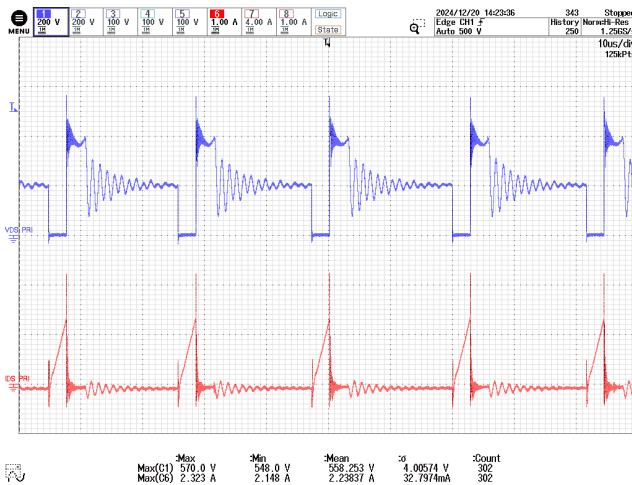


Figure 136 – INN3947FQ Drain Voltage and Current.
200 V_{DC}, Full Load.
CH1: V_{DS,INNO}, 200 V / div.
CH7: I_{D,INNO}, 1 A / div.
Time: 10 μs / div.

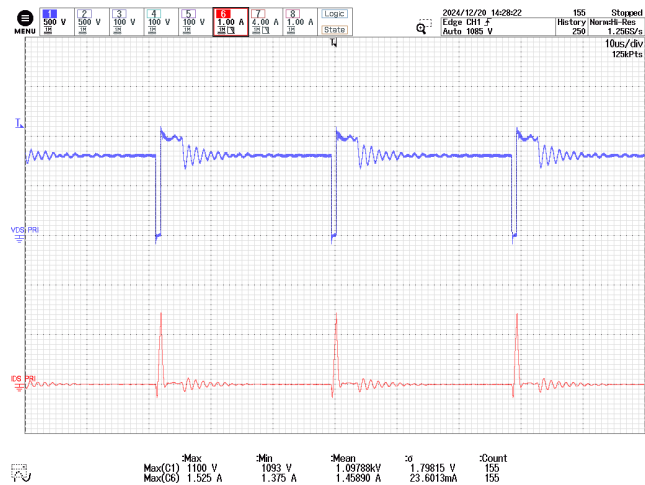


Figure 137 – INN3947FQ Drain Voltage and Current.
800 V_{DC}, Full Load.
CH1: V_{DS,INNO}, 500 V / div.
CH7: I_{D,INNO}, 1 A / div.
Time: 10 μs / div.

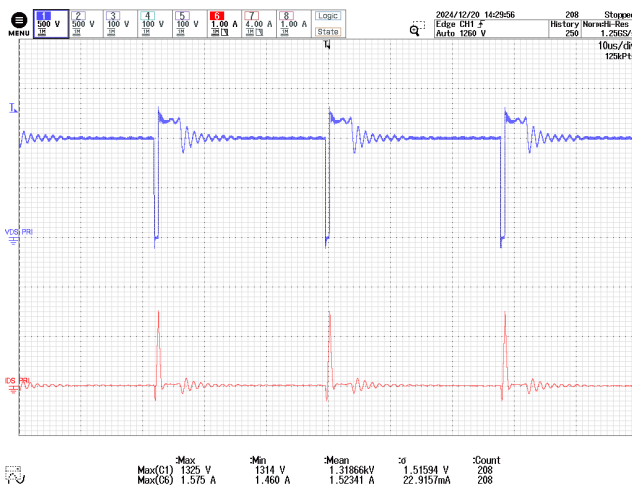


Figure 138 – INN3947FQ Drain Voltage and Current.
1000 V_{DC}, Full Load.
CH1: V_{DS,INNO}, 500 V / div.
CH3: I_{D,INNO}, 1.00 A / div.
Time: 10 μs / div.

11.2.3.3 SR FET Drain Voltage and Current at -40 °C Ambient

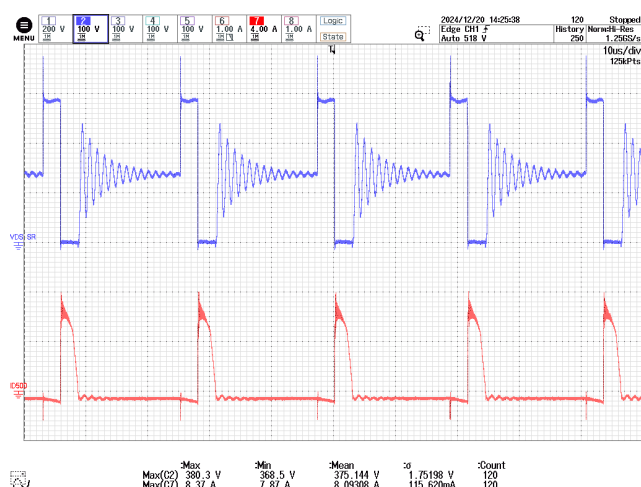


Figure 139 – SR FET Drain Voltage and Current.
200 VDC, Full Load.
CH2: VDS,SR, 10 V / div.
CH3: IDS,SR, 4 A / div.
Time: 10 μs / div.

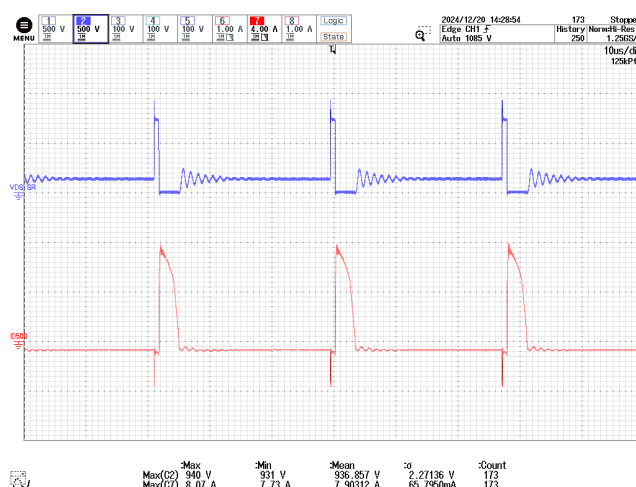


Figure 140 – SR FET Drain Voltage and Current.
800 VDC, Full Load.
CH2: VDS,SR, 50 V / div.
CH3: IDS,SR, 4 A / div.
Time: 10 μs / div.



Figure 141 – SR FET Drain Voltage and Current.
1000 VDC, Full Load.
CH2: VDS,SR, 50 V / div.
CH3: IDS,SR, 4 A / div.
Time: 10 μs / div.

11.2.3.4 V_{DIODE} Voltage and Current at -40 °C Ambient

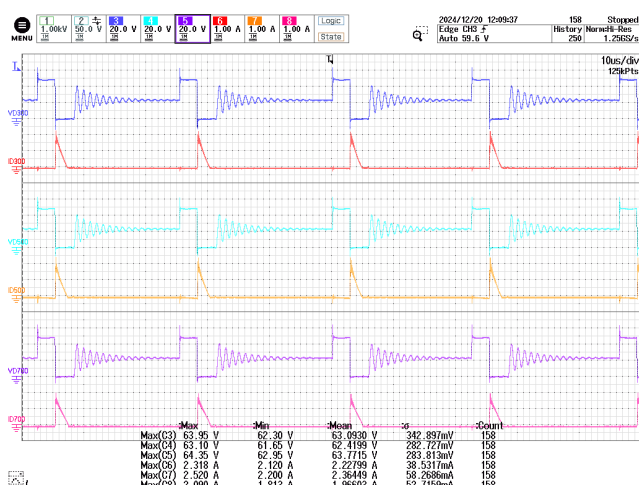


Figure 142 – V_{DIODE} Voltage and Current.

200 V_{DC}, Full Load.

CH3: V_{D300}, 20 V / div.

CH4: V_{D500}, 20 V / div.

CH5: V_{D700}, 20 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μ s / div.

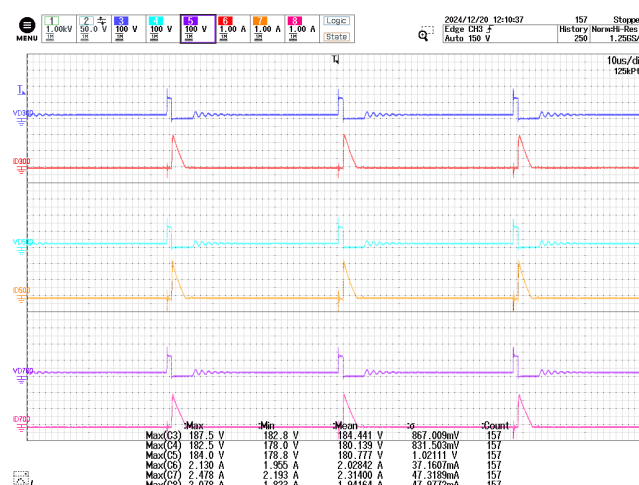


Figure 143 – V_{DIODE} Voltage and Current.

800 V_{DC}, Full Load.

CH3: V_{D300}, 100 V / div.

CH4: V_{D500}, 100 V / div.

CH5: V_{D700}, 100 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μ s / div.

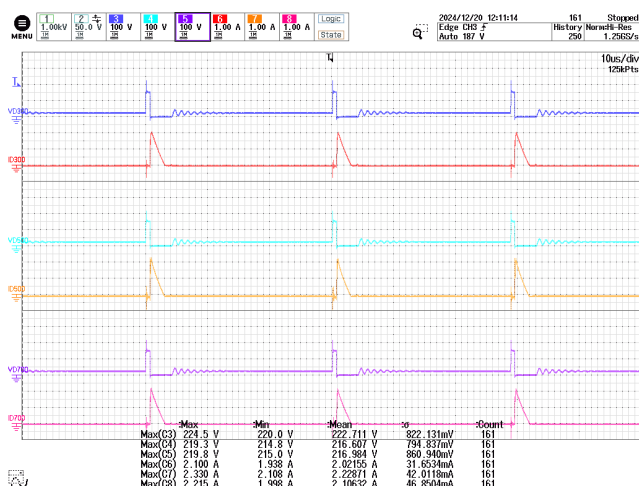


Figure 144 – V_{DIODE} Voltage and Current.

1000 V_{DC}, Full Load.

CH3: V_{D300}, 100 V / div.

CH4: V_{D500}, 100 V / div.

CH5: V_{D700}, 100 V / div.

CH6: I_{D300}, 1 A / div.

CH7: I_{D500}, 1 A / div.

CH8: I_{D700}, 1 A / div.

Time: 10 μ s / div.

11.2.3.5 Short Circuit Response at -40 °C Ambient

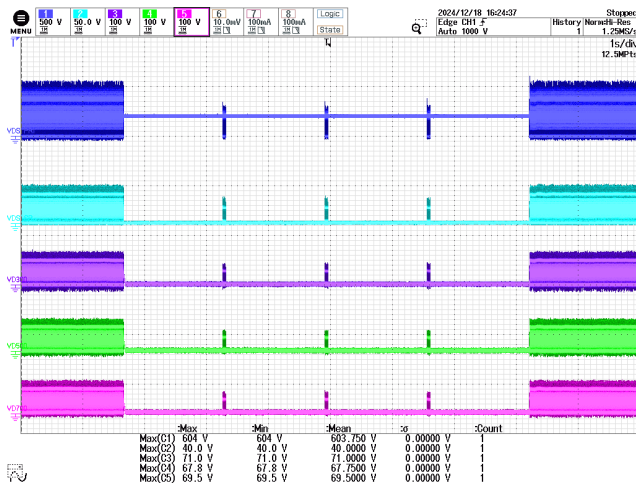


Figure 145 – INN3947FQ, SR FET, and V_{DIODE} Voltages. 200 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 500 V / div.

CH2: $V_{DS,SR}$, 50 V / div.

CH3: V_{D300} , 100 V / div.

CH4: V_{D500} , 100 V / div.

CH5: V_{D700} , 100 V / div.

Time: 1 s / div.

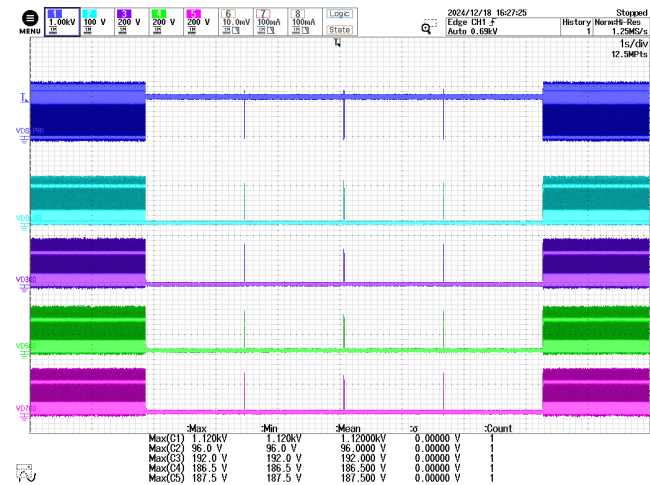


Figure 146 – V_{DIODE} Voltage and Current. 800 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

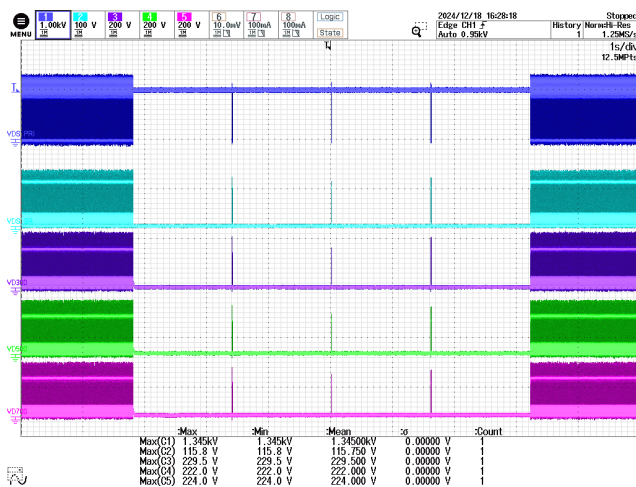


Figure 147 – V_{DIODE} Voltage and Current. 1000 V_{DC} , Full Load.

CH1: $V_{DS,INNO}$, 1000 V / div.

CH2: $V_{DS,SR}$, 100 V / div.

CH3: V_{D300} , 200 V / div.

CH4: V_{D500} , 200 V / div.

CH5: V_{D700} , 200 V / div.

Time: 1 s / div.

11.3 Load Transient Response

Load transient response describes the response characteristic of the power supply to sudden load changes. The output voltage waveforms on the unit were captured with switching load transient from 0% to 50%, 50% to 100%, and 10% to 90%. Duration for load state high is 100 ms and for low is 100 ms with a slew rate of 100 mA / μ s.

11.3.1 Load Transient Response at 85 °C Ambient

Test Conditions (0.1 A / μ s Slew Rate, 200 ms Period, Min.-Typ.-Min.)			Output Overshoot and Undershoot Results			
Input	14 V Output	23 V Output	14 V output		23 V Output	
V _{IN} (V)	I _{OUT} (mA)	I _{OUT} (mA)	14 V _{MAX} (mV)	14 V _{MIN} (mV)	23 V _{MAX} (mV)	23 V _{MIN} (mV)
200	0% to 50%	87	126	-181	805	-840
		3	106	-183	980	-1440
	50% to 100%	87	103	-106	273	-225
		3	138	-114	635	-670
	10% to 90%	87	120	-236	695	-650
		3	131	-266	1010	-1350
	714	0% to 50%	105	-38.5	1780	-1590
	0		46	-40.5	408	-383
	714	50% to 100%	78.5	-39.5	330	-313
	0		56	-33	370	-268
	714	10% to 90%	102	-38	1500	-1440
	0		47	-58	510	-478
800	0% to 50%	87	130	-230	875	-1315
		3	148	-119	950	-1380
	50% to 100%	87	9	-111	295	--245
		3	126	-161	605	-650
	10% to 90%	87	120	-255	720	-650
		3	154	-184	1000	-1300
	714	0% to 50%	104	-40	1650	-1460
	0		57.5	-39	290	-263
	714	50% to 100%	80.5	-39	360	-310
	0		59.5	-86.5	510	-955
	714	10% to 90%	94.5	-39.5	1430	-1400
	0		76.5	-122.5	523	-1285
1000	0% to 50%	87	129	-284	930	-1490
		3	148	-104	980	-1410
	50% to 100%	87	99	-114	300	-268
		3	125	-153	610	-625
	10% to 90%	87	135	-295	725	-665



		3	158	-185	1000	-1270
	714	0% to 50%	104	-43	1690	-1480
	0		63	-89.5	590	-910
	714	50% to 100%	84	-41	368	-315
	0		416	65.5	536	-438
	714	10% to 90%	95.5	-42.5	1440	-1430
	0		78.5	-95	558	-1363

Table 14 – Load Transient Response.

11.3.1.1 Output Voltage Ripple with 0% - 50% Transient Load at 85 °C Ambient

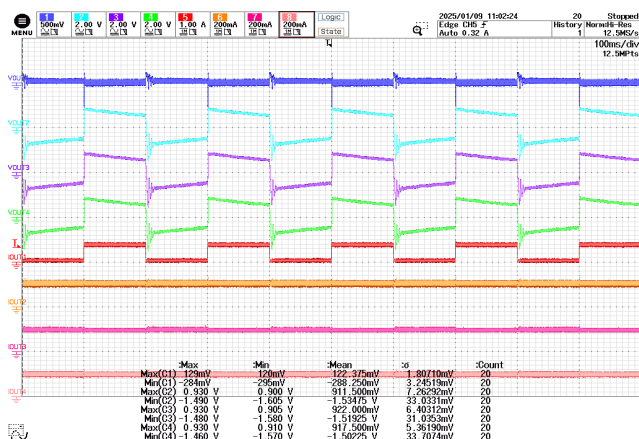


Figure 148 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Max Load.

CH1: V_{OUT1}, 500 mV / div.

CH2: V_{OUT2}, 2 V / div.

CH3: V_{OUT3}, 2 V / div.

CH4: V_{OUT4}, 2 V / div.

CH5: I_{OUT1}, 1 A / div.

CH6: I_{OUT2}, 200 mA / div.

CH7: I_{OUT3}, 200 mA / div.

CH8: I_{OUT4}, 200 mA / div.

Time: 100 ms / div.

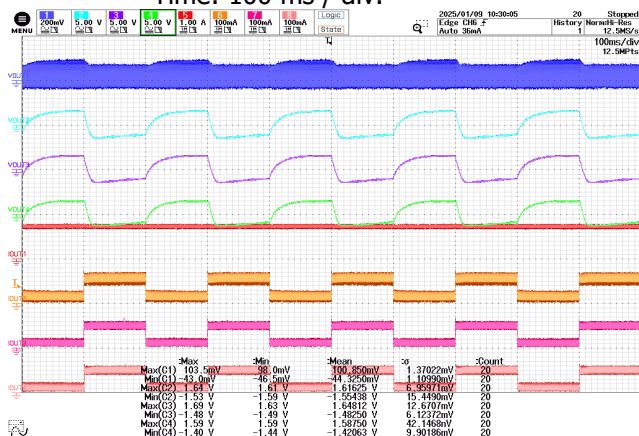


Figure 150 – Output Voltage and Current. 1000 V_{DC}, 14 V Max Load, 23 V Switching Load.

CH1: V_{OUT1}, 200 mV / div.

CH2: V_{OUT2}, 5 V / div.

CH3: V_{OUT3}, 5 V / div.

CH4: V_{OUT4}, 5 V / div.

CH5: I_{OUT1}, 1 A / div.

CH6: I_{OUT2}, 100 mA / div.

CH7: I_{OUT3}, 100 mA / div.

CH8: I_{OUT4}, 100 mA / div.

Time: 100 ms / div.

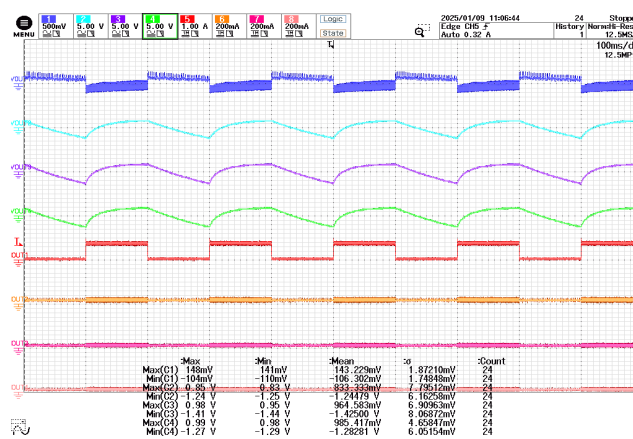


Figure 149 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Min Load.

CH1: V_{OUT1}, 500 mV / div.

CH2: V_{OUT2}, 5 V / div.

CH3: V_{OUT3}, 5 V / div.

CH4: V_{OUT4}, 5 V / div.

CH5: I_{OUT1}, 1 A / div.

CH6: I_{OUT2}, 200 mA / div.

CH7: I_{OUT3}, 200 mA / div.

CH8: I_{OUT4}, 200 mA / div.

Time: 100 ms / div.

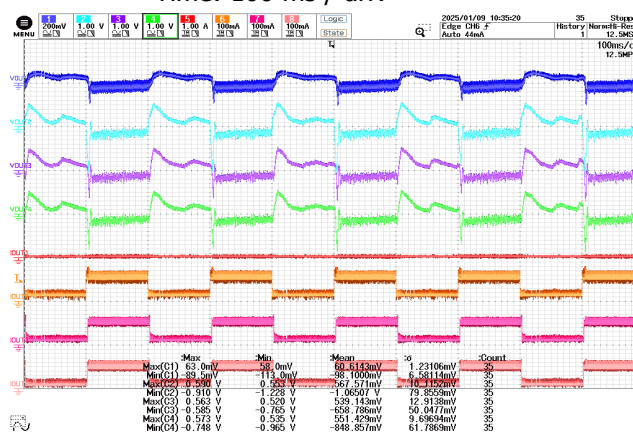


Figure 151 – Output Voltage and Current. 1000 V_{DC}, 14 V Min Load, 23 V Switching Load.

CH1: V_{OUT1}, 200 mV / div.

CH2: V_{OUT2}, 1 V / div.

CH3: V_{OUT3}, 1 V / div.

CH4: V_{OUT4}, 1 V / div.

CH5: I_{OUT1}, 1 A / div.

CH6: I_{OUT2}, 100 mA / div.

CH7: I_{OUT3}, 100 mA / div.

CH8: I_{OUT4}, 100 mA / div.

Time: 100 ms / div.

11.3.1.2 Output Voltage Ripple with 50% - 100% Transient Load at 85 °C Ambient

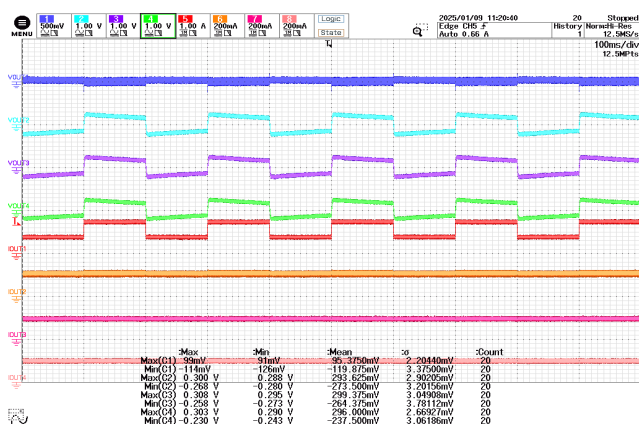


Figure 152 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Max Load.

CH1: V_{OUT1}, 500 mV / div.
 CH2: V_{OUT2}, 1 V / div.
 CH3: V_{OUT3}, 1 V / div.
 CH4: V_{OUT4}, 1 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 200 mA / div.
 CH7: I_{OUT3}, 200 mA / div.
 CH8: I_{OUT4}, 200 mA / div.
 Time: 100 ms / div.

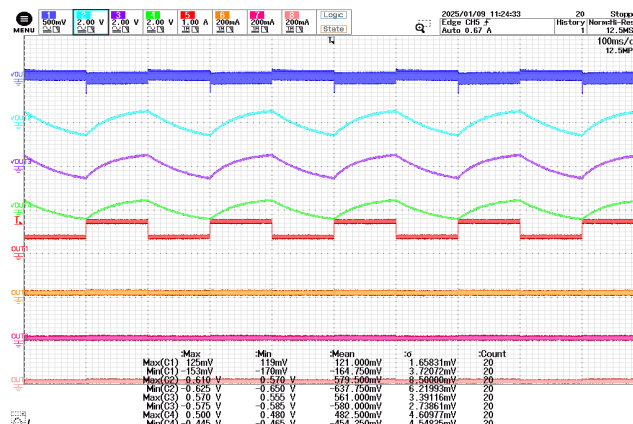


Figure 153 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Min Load.

CH1: V_{OUT1}, 500 mV / div.
 CH2: V_{OUT2}, 2 V / div.
 CH3: V_{OUT3}, 2 V / div.
 CH4: V_{OUT4}, 2 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 200 mA / div.
 CH7: I_{OUT3}, 200 mA / div.
 CH8: I_{OUT4}, 200 mA / div.
 Time: 100 ms / div.

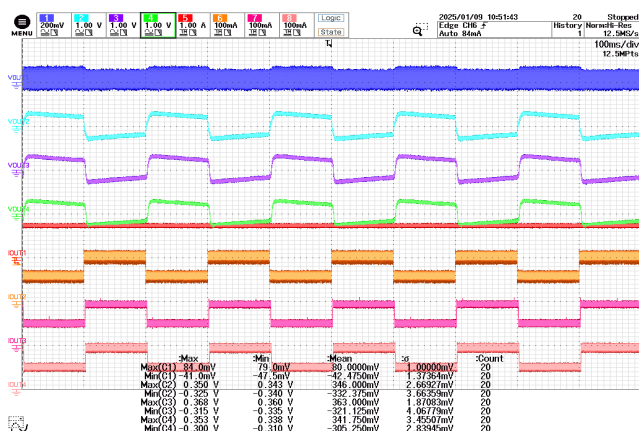


Figure 154 – Output Voltage and Current. 1000 V_{DC}, 14 V Max Load, 23 V Switching Load.

CH1: V_{OUT1}, 2.00 mV / div.
 CH2: V_{OUT2}, 1 V / div.
 CH3: V_{OUT3}, 1 V / div.
 CH4: V_{OUT4}, 1 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 100 mA / div.
 CH7: I_{OUT3}, 100 mA / div.
 CH8: I_{OUT4}, 100 mA / div.
 Time: 100 ms / div.

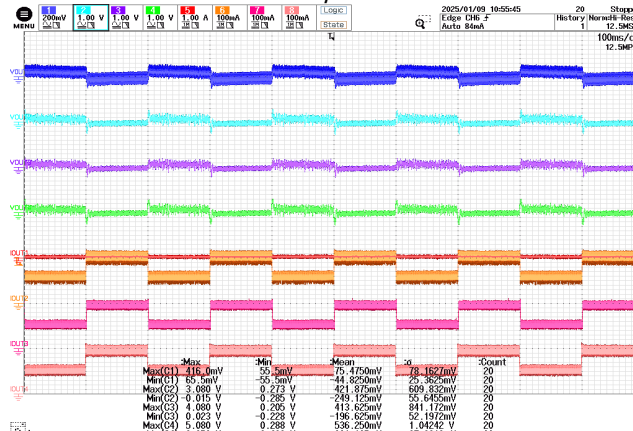


Figure 155 – Output Voltage and Current. 1000 V_{DC}, 14 V Min Load, 23 V Switching Load.

CH1: V_{OUT1}, 200 mV / div.
 CH2: V_{OUT2}, 1 V / div.
 CH3: V_{OUT3}, 1 V / div.
 CH4: V_{OUT4}, 1 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 100 mA / div.
 CH7: I_{OUT3}, 100 mA / div.
 CH8: I_{OUT4}, 100 mA / div.
 Time: 100 ms / div.

11.3.1.3 Output Voltage Ripple with 10% - 90% Transient Load at 85 °C Ambient

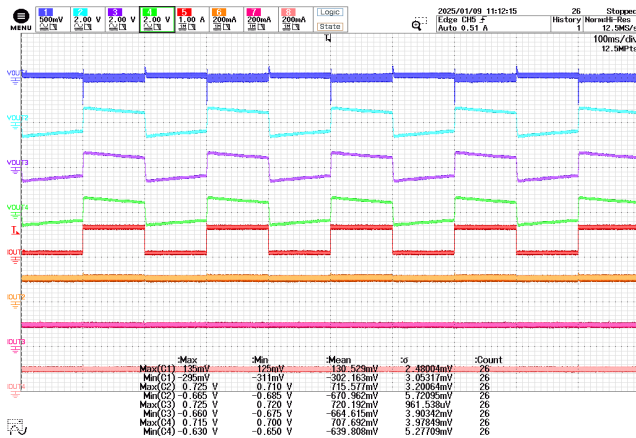


Figure 156 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Max Load.

CH1: V_{OUT1}, 500 mV / div.
 CH2: V_{OUT2}, 2 V / div.
 CH3: V_{OUT3}, 2 V / div.
 CH4: V_{OUT4}, 2 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 200 mA / div.
 CH7: I_{OUT3}, 200 mA / div.
 CH8: I_{OUT4}, 200 mA / div.
 Time: 100 ms / div.

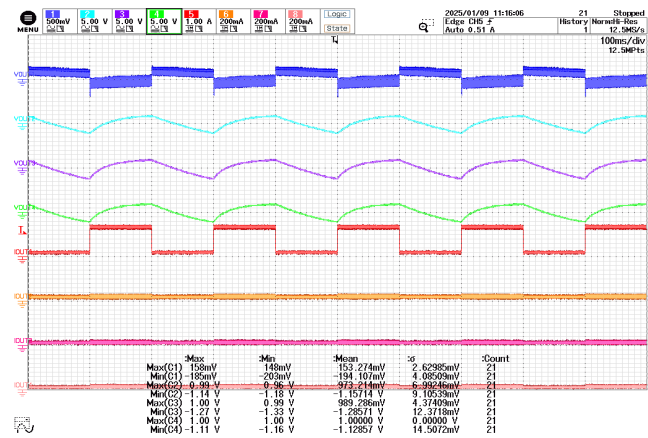


Figure 157 – Output Voltage and Current. 1000 V_{DC}, 14 V Switching Load, 23 V Min Load.

CH1: V_{OUT1}, 500 mV / div.
 CH2: V_{OUT2}, 5 V / div.
 CH3: V_{OUT3}, 5 V / div.
 CH4: V_{OUT4}, 5 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 200 mA / div.
 CH7: I_{OUT3}, 200 mA / div.
 CH8: I_{OUT4}, 200 mA / div.
 Time: 100 ms / div.

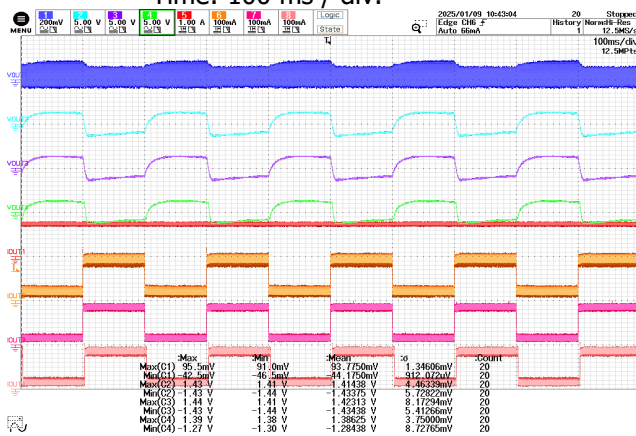


Figure 158 – Output Voltage and Current. 1000 V_{DC}, 14 V Max Load, 23 V Switching Load.

CH1: V_{OUT1}, 200 mV / div.
 CH2: V_{OUT2}, 5 V / div.
 CH3: V_{OUT3}, 5 V / div.
 CH4: V_{OUT4}, 5 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 100 mA / div.
 CH7: I_{OUT3}, 100 mA / div.
 CH8: I_{OUT4}, 100 mA / div.
 Time: 100 ms / div.

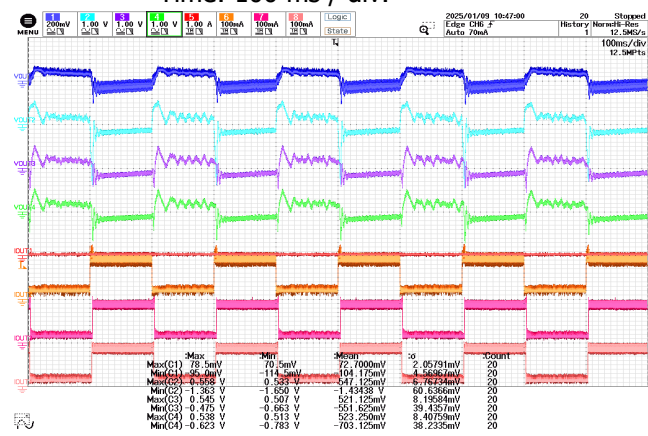


Figure 159 – Output Voltage and Current. 1000 V_{DC}, 14 V Min Load, 23 V Switching Load.

CH1: V_{OUT1}, 200 mV / div.
 CH2: V_{OUT2}, 1 V / div.
 CH3: V_{OUT3}, 1 V / div.
 CH4: V_{OUT4}, 1 V / div.
 CH5: I_{OUT1}, 1 A / div.
 CH6: I_{OUT2}, 100 mA / div.
 CH7: I_{OUT3}, 100 mA / div.
 CH8: I_{OUT4}, 100 mA / div.
 Time: 100 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to eliminate spurious signals due to pick-up. Details of the probe modification were Figure 160 and Figure 161 below.

A 1 μ F / 50 V ceramic capacitor was attached in parallel across the probe tip of a CT2708 probe adapter. A twisted pair of wires, kept as short as possible, were then soldered directly between the probe and the output terminals of the unit under test.

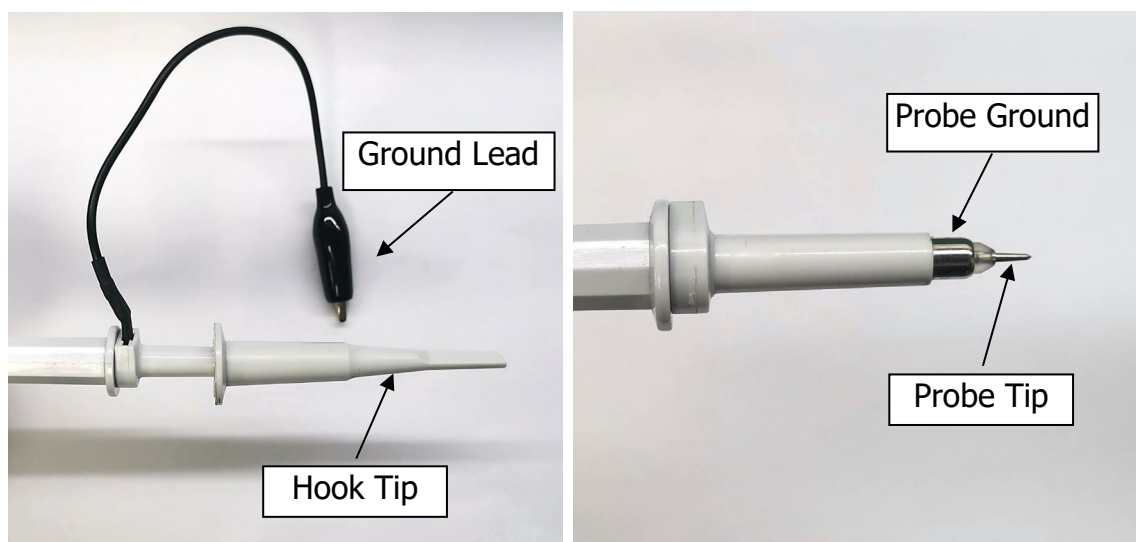


Figure 160 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

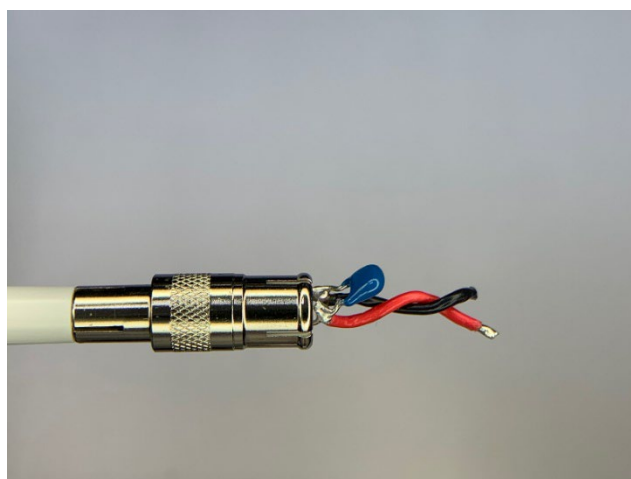


Figure 161 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

11.4.2.1 Output Voltage Ripple at 85 °C Ambient with Constant Full Load²²

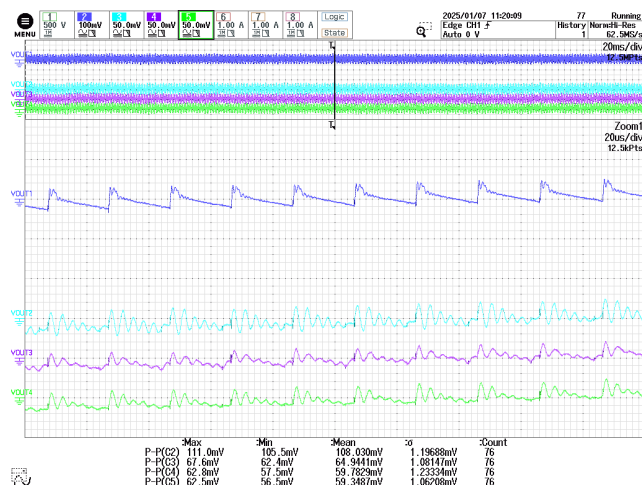


Figure 162 – Output Voltage Ripple.
200 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

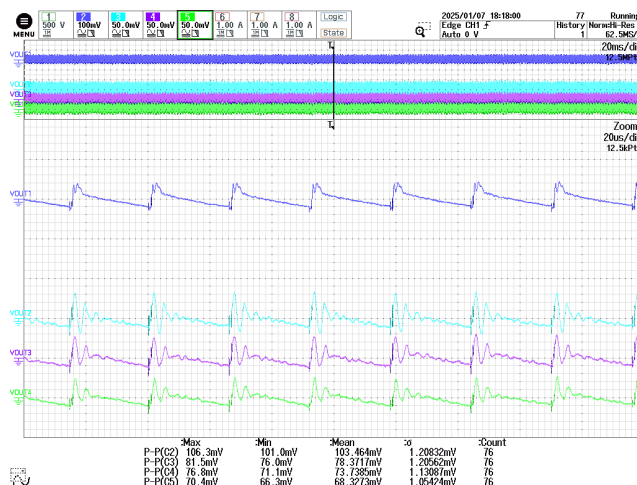


Figure 163 – Output Voltage Ripple.
800 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

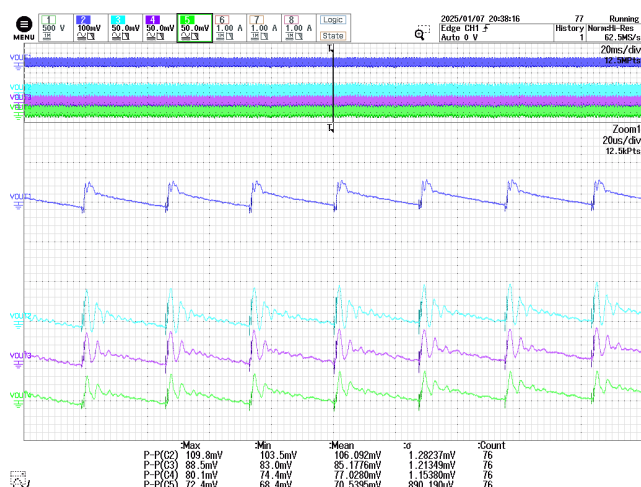


Figure 164 – Output Voltage Ripple.
1000 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

²² Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient with Constant Full Load²³

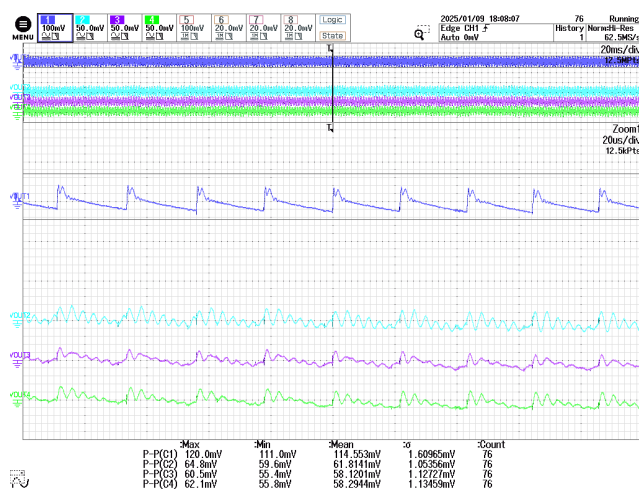


Figure 165 – Output Voltage Ripple.
200 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

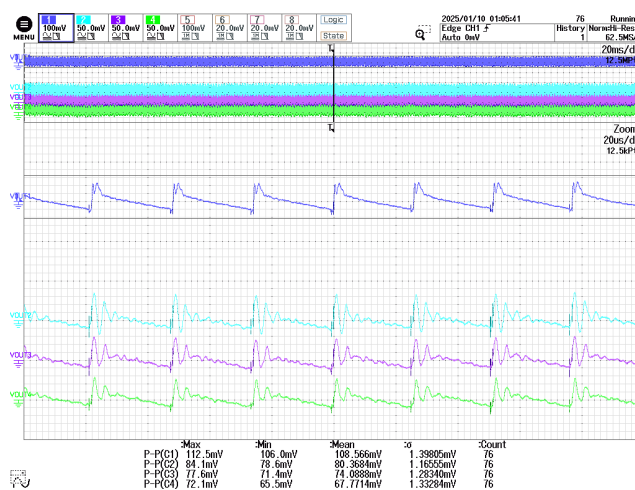


Figure 166 – Output Voltage Ripple.
800 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

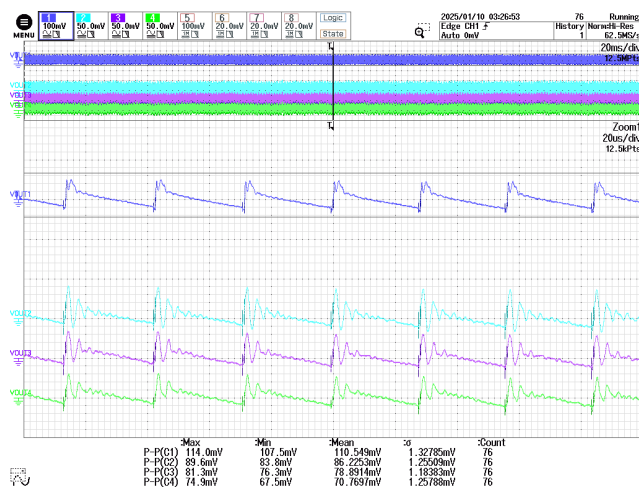


Figure 167 – Output Voltage Ripple.
1000 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

²³ Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient with Constant Full Load²⁴

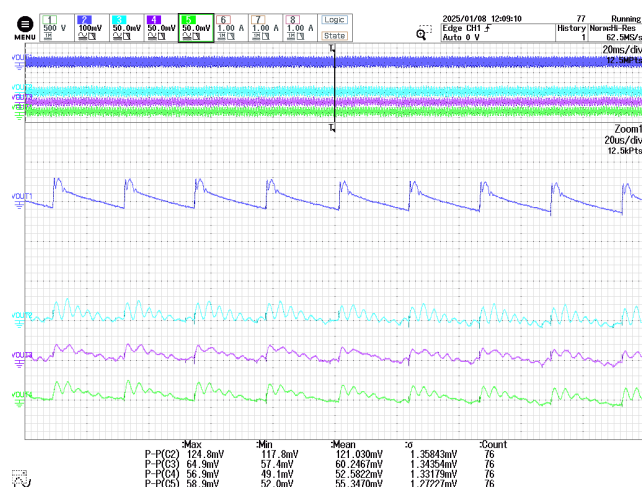


Figure 168 – Output Voltage Ripple.
200 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

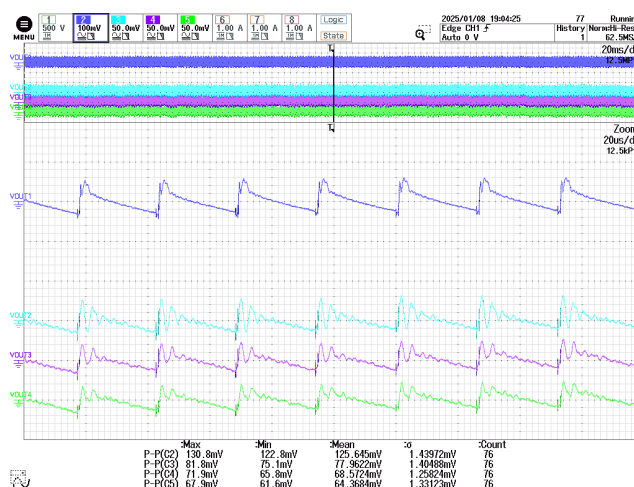


Figure 169 – Output Voltage Ripple.
800 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

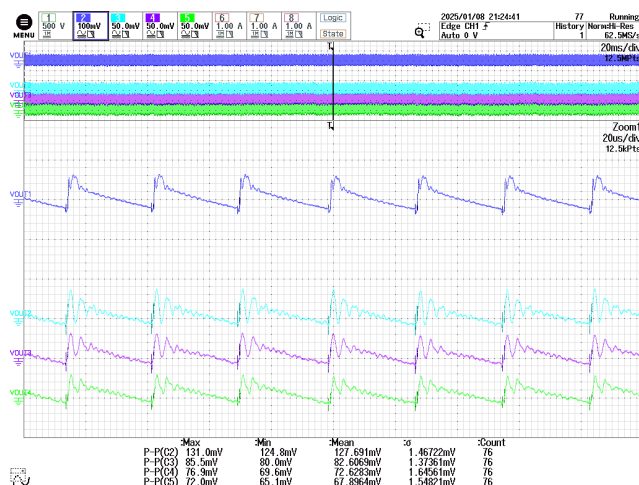


Figure 170 – Output Voltage Ripple.
1000 VDC, Full Load.
CH2: V_{OUT1} , 100 mV / div.
CH3: V_{OUT2} , 50 mV / div.
CH4: V_{OUT3} , 50 mV / div.
CH5: V_{OUT4} , 50 mV / div.
Time: 20 ms / div.

²⁴ Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

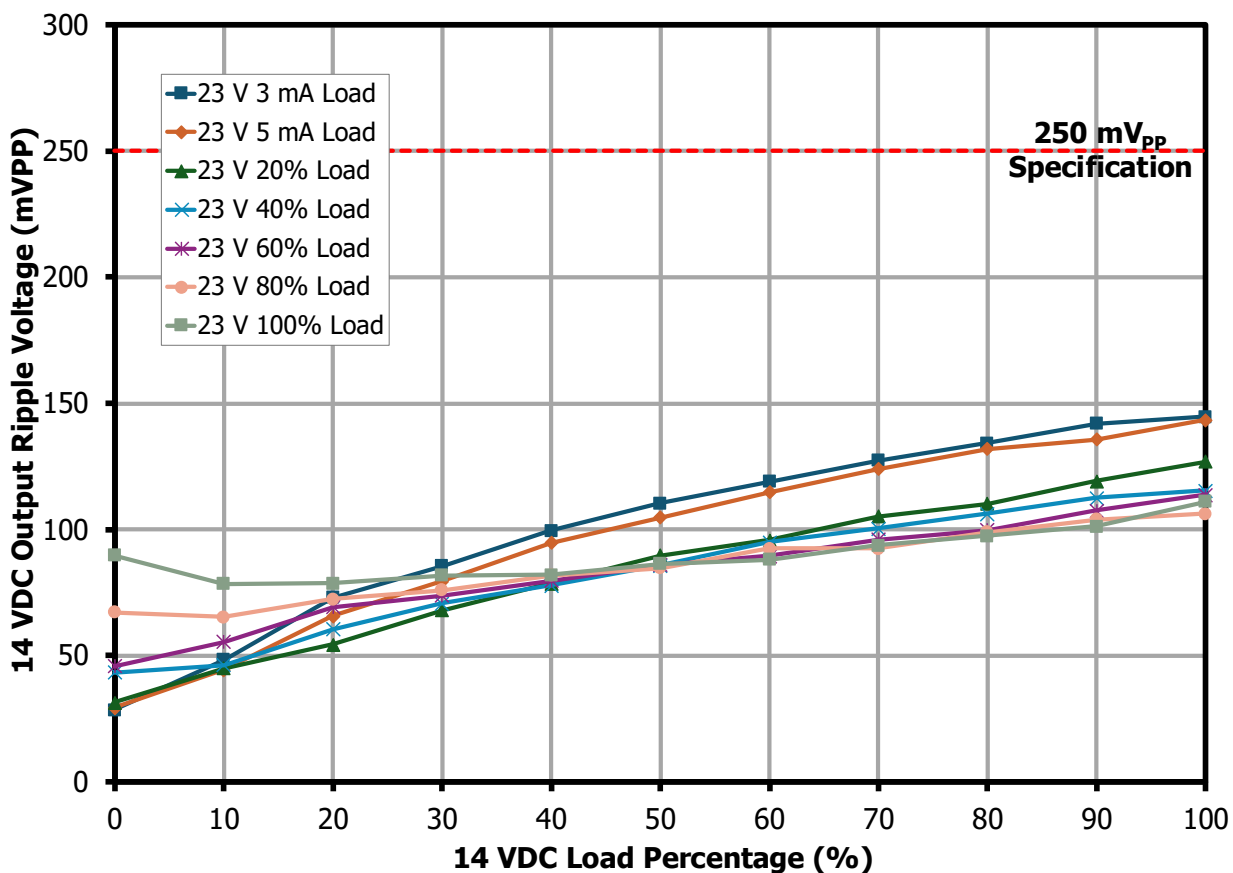


Figure 171 – 14 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (85 °C Ambient).

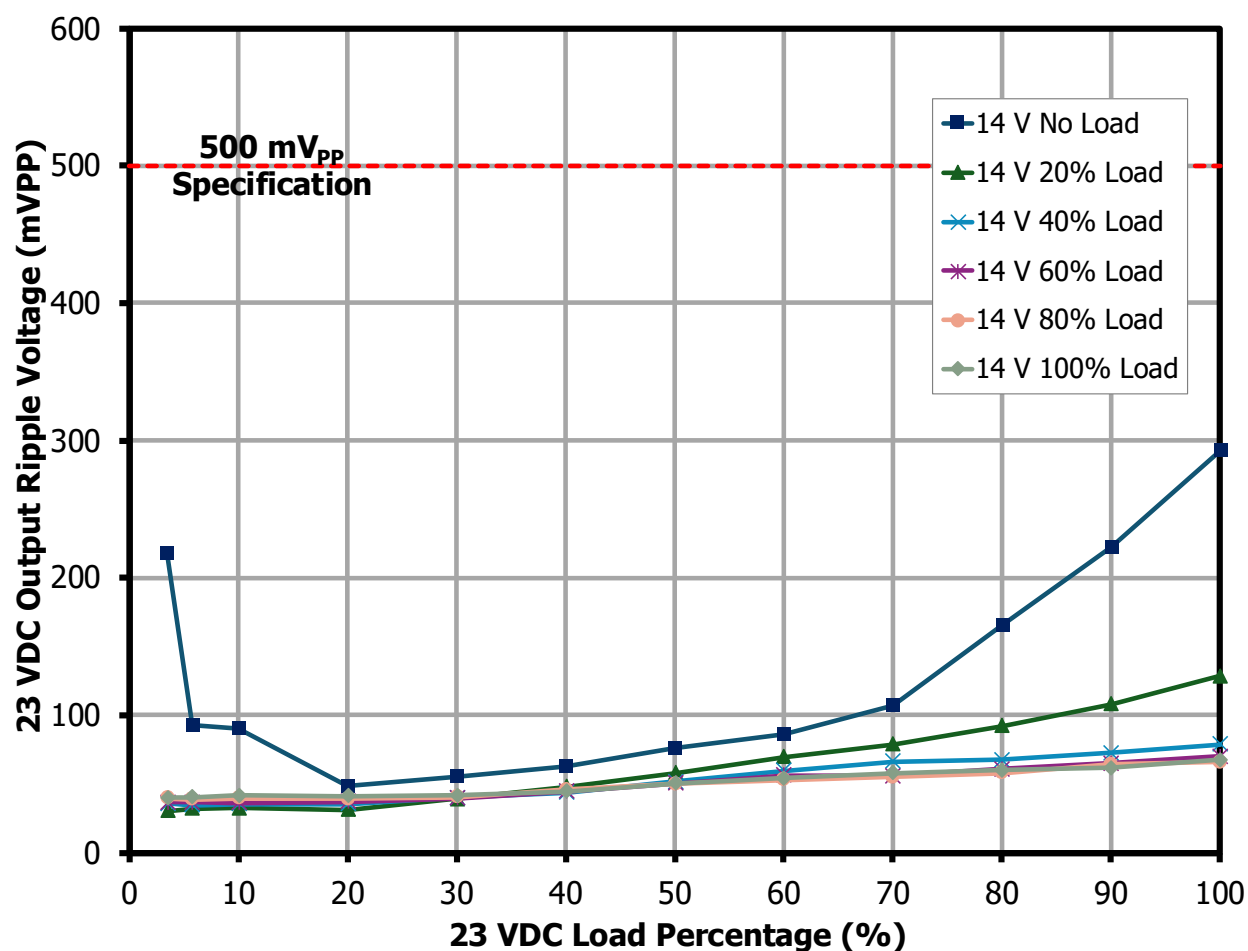


Figure 172 – 23 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (85 °C Ambient).

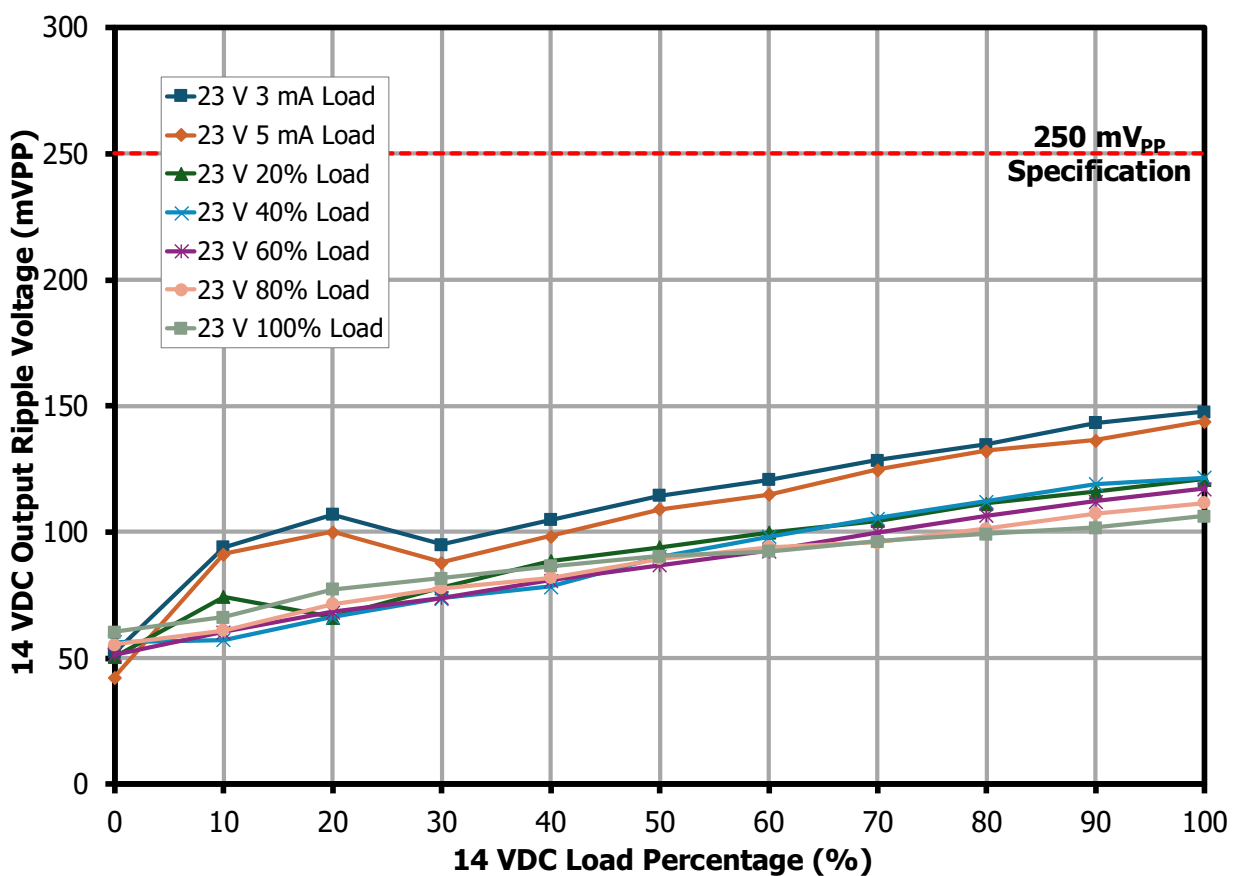


Figure 173 – 14 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (85 °C Ambient).

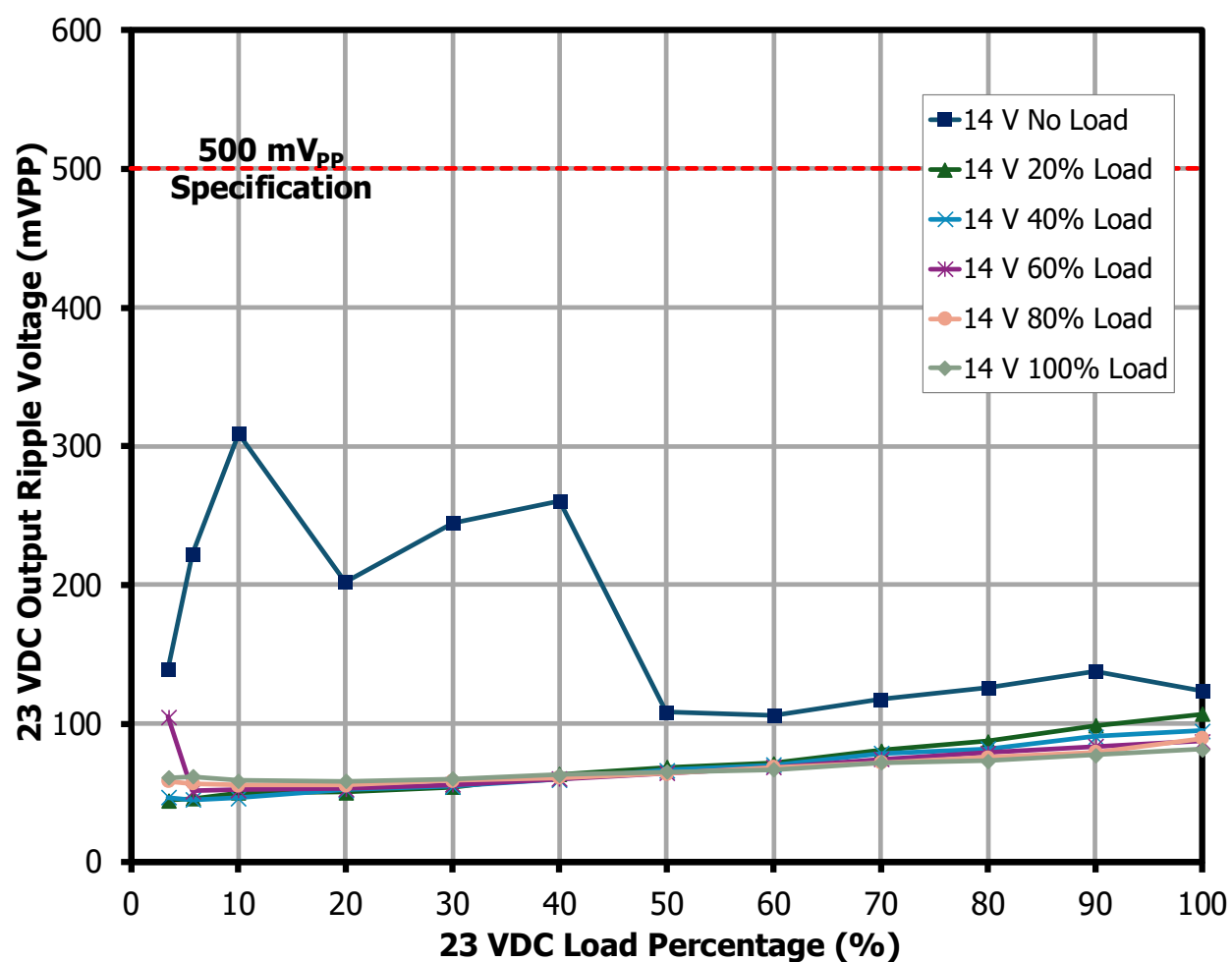


Figure 174 – 23 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (85 °C Ambient).

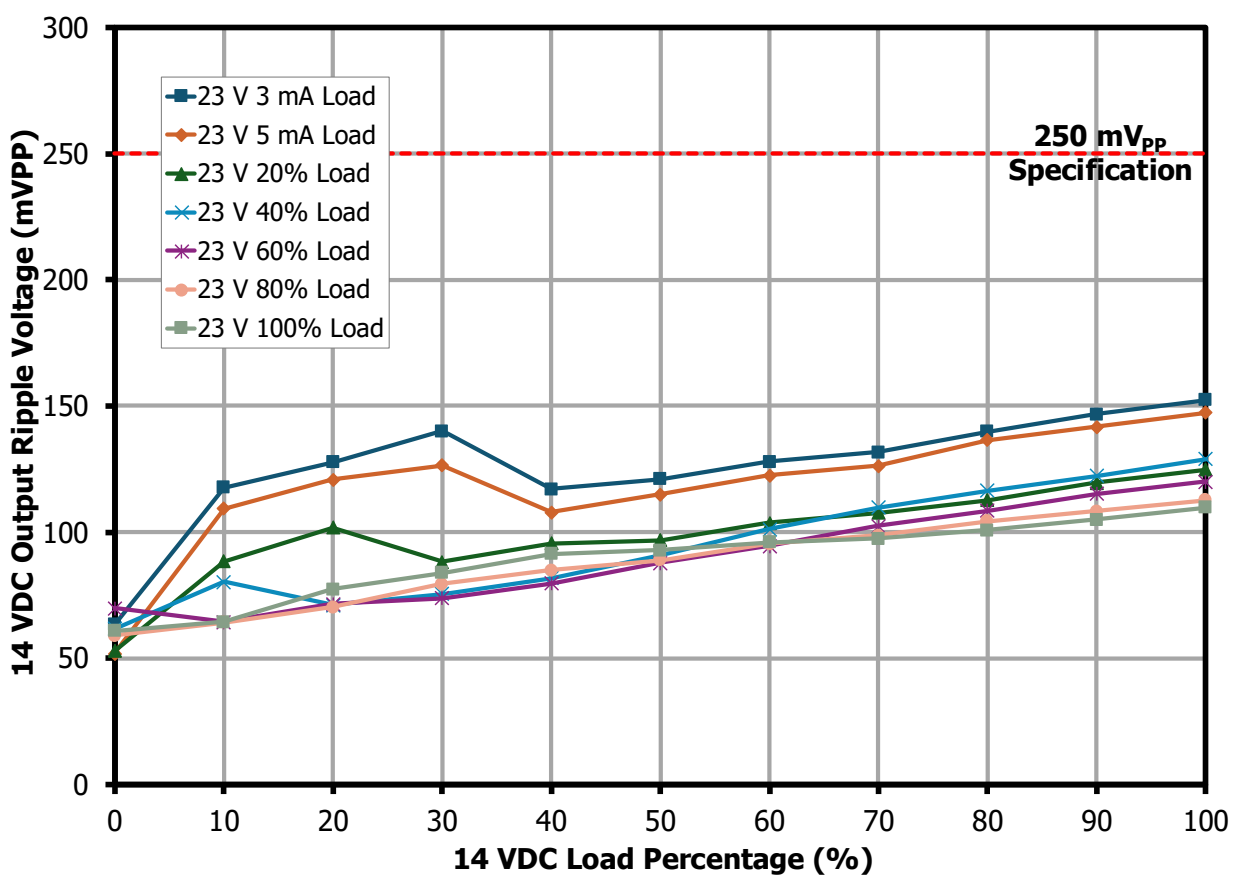


Figure 175 – 14 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (85 °C Ambient).

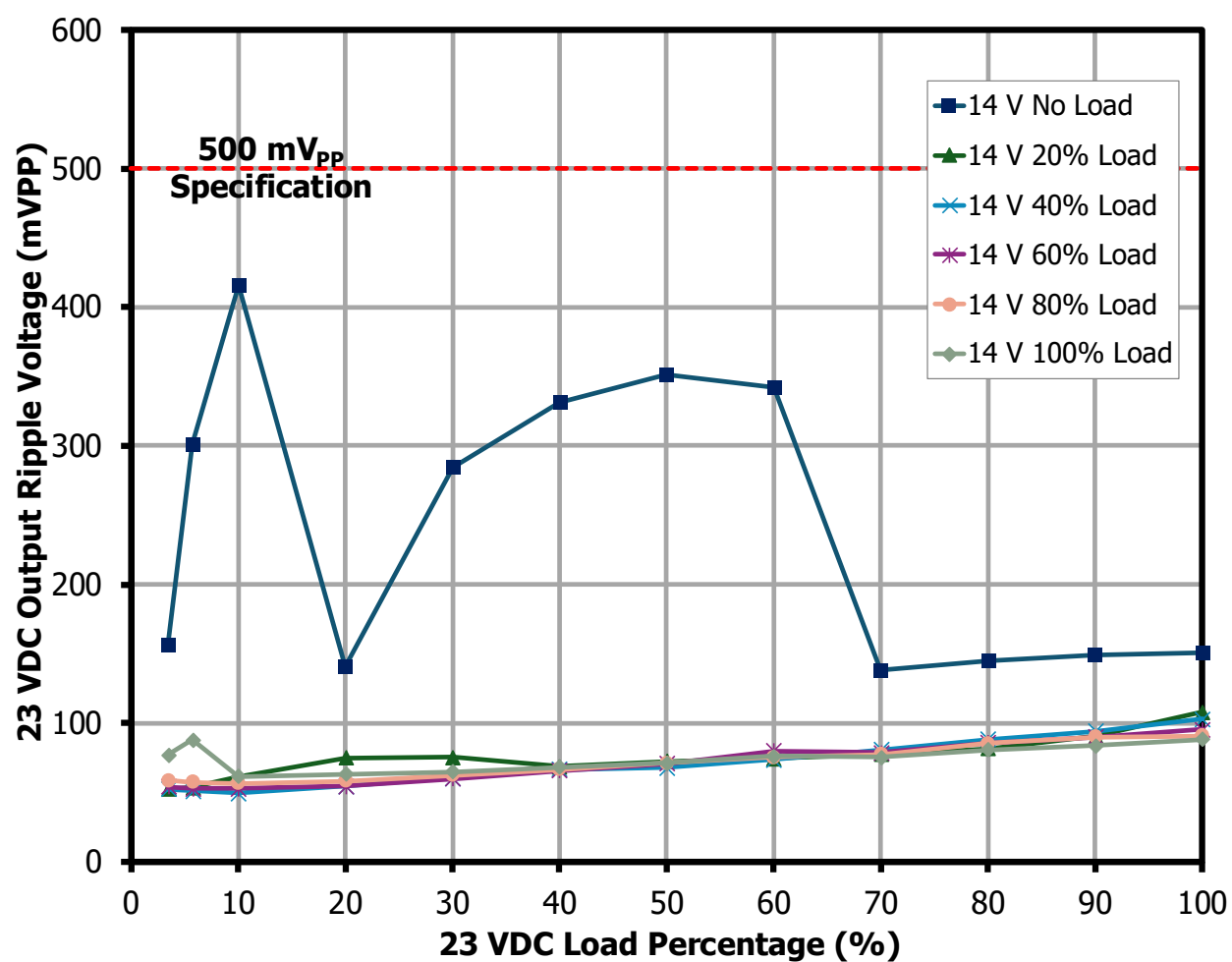


Figure 176 – 23 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

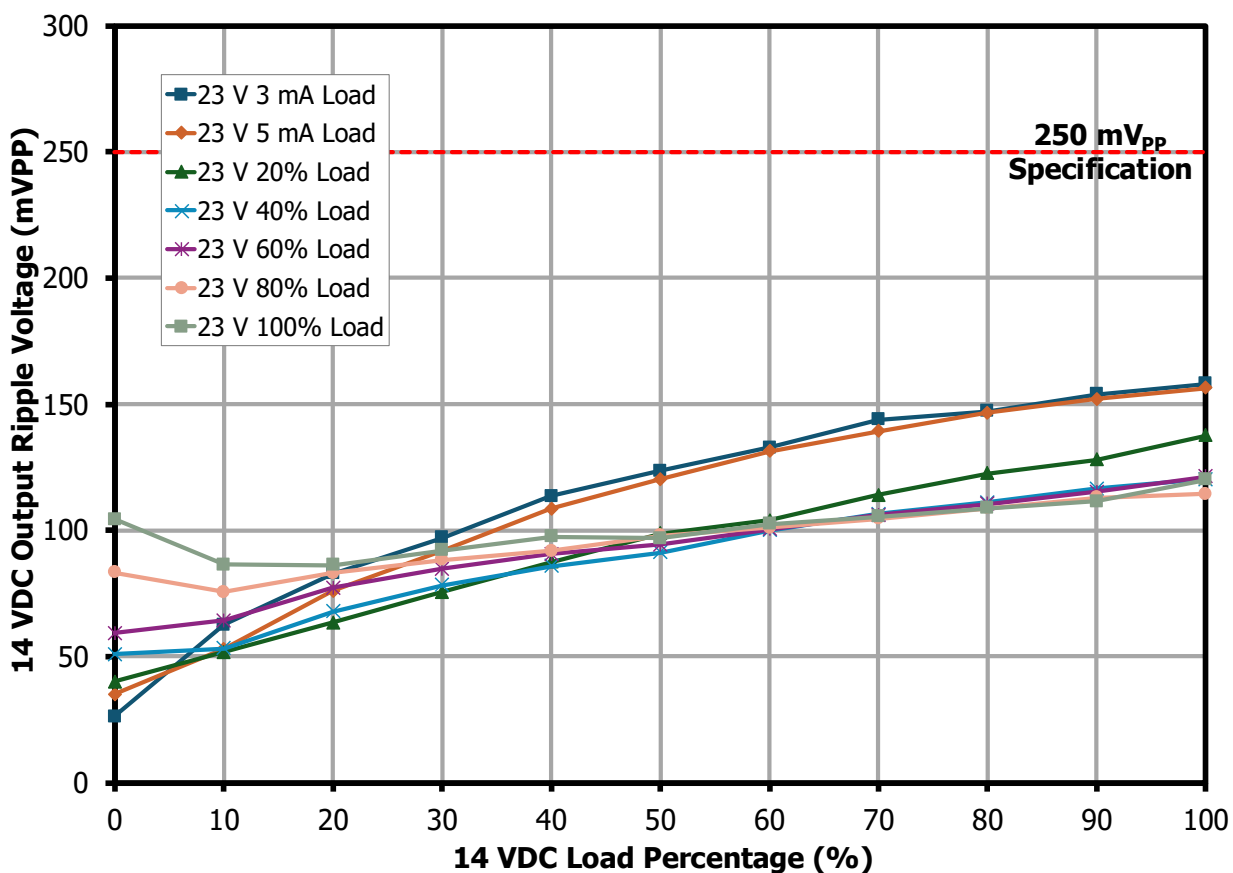


Figure 177 – 14 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (25 °C Ambient).

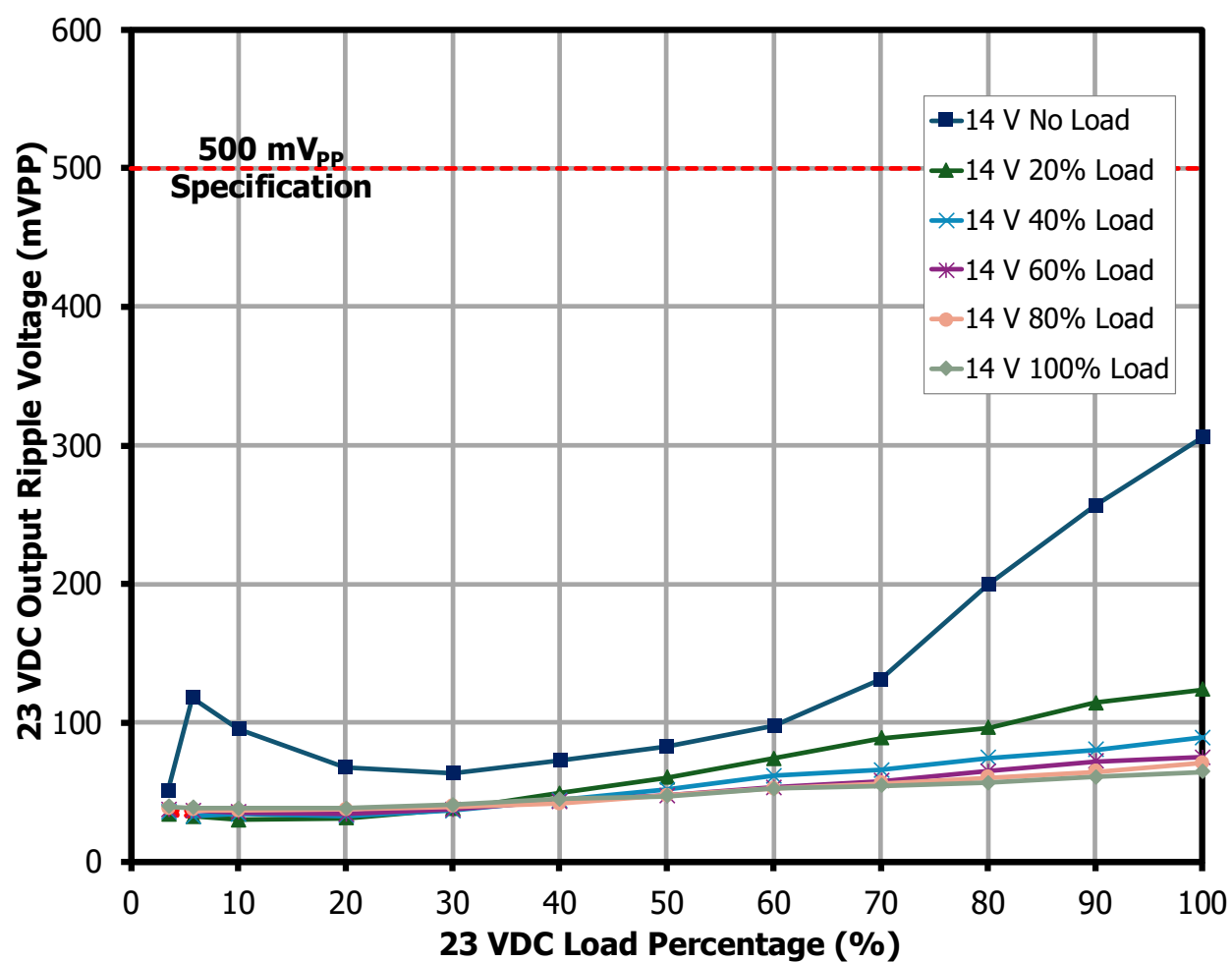


Figure 178 – 23 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (25 °C Ambient).

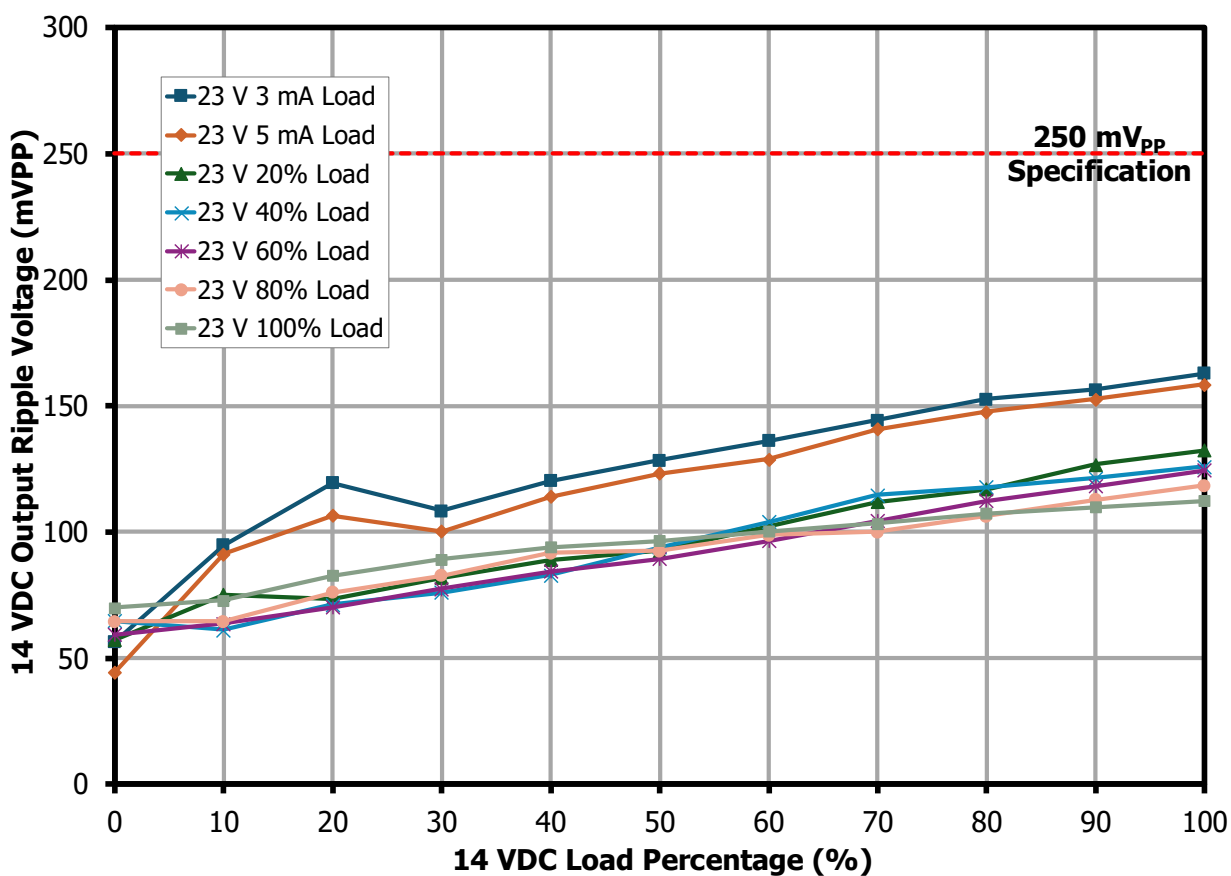


Figure 179 – 14 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (25 °C Ambient).

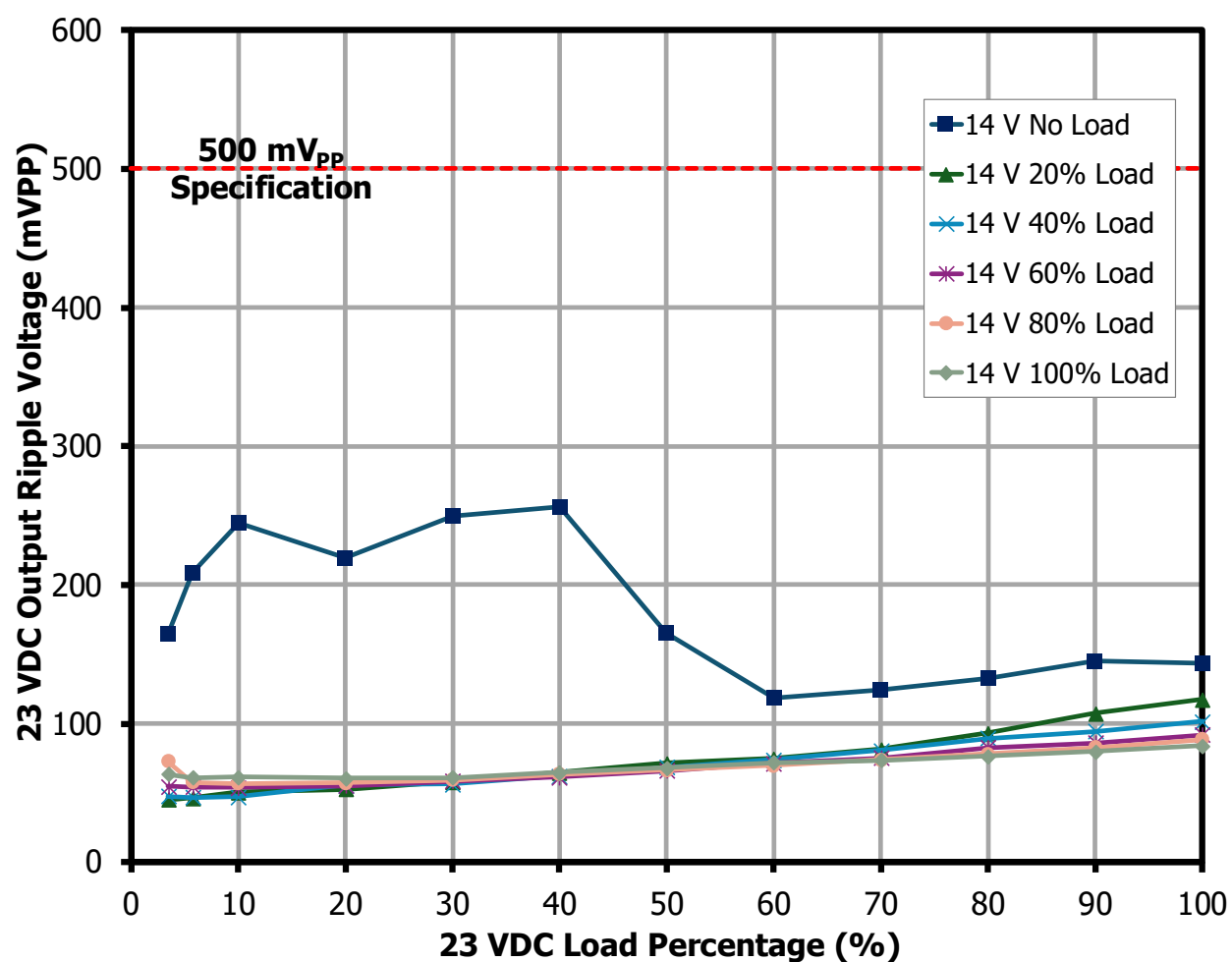


Figure 180 – 23 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (25 °C Ambient).

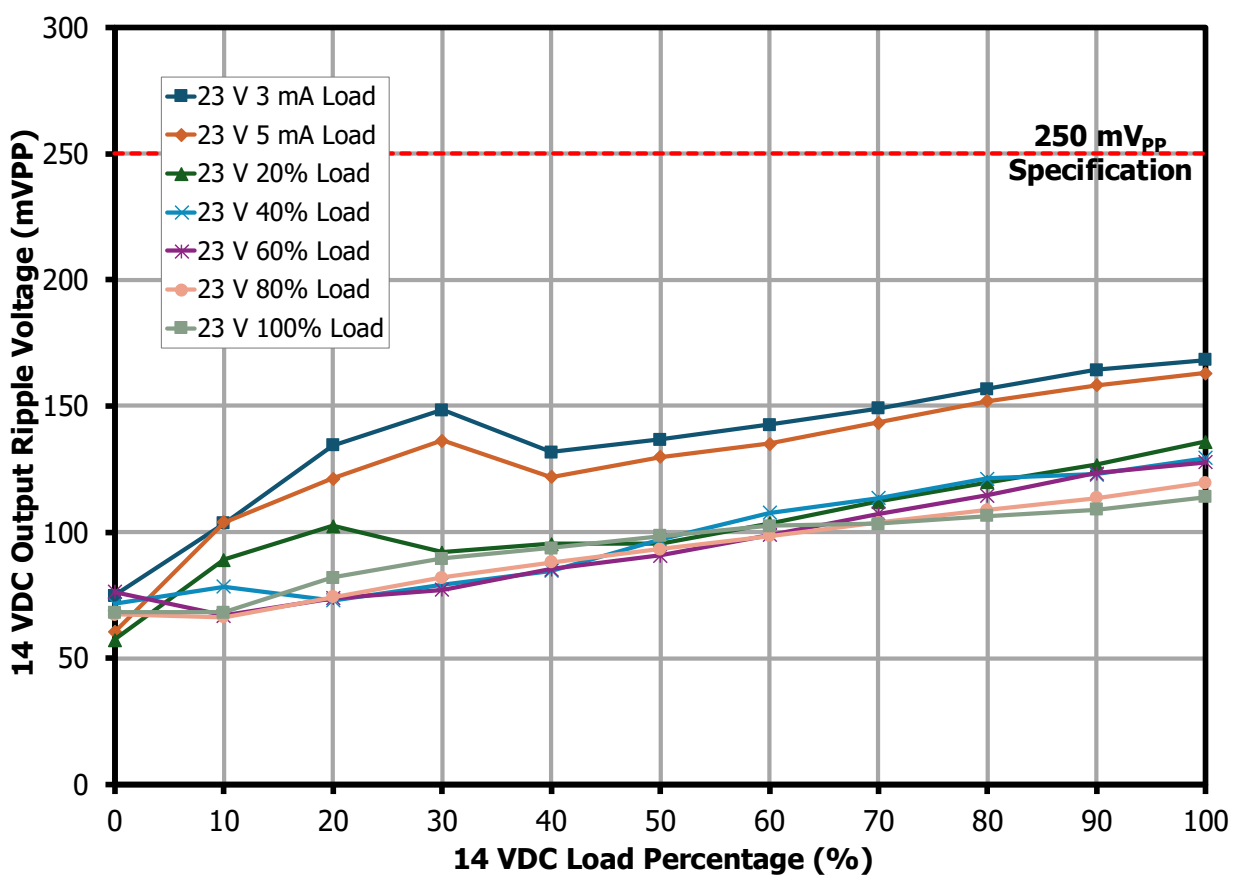


Figure 181 – 14 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (25 °C Ambient).

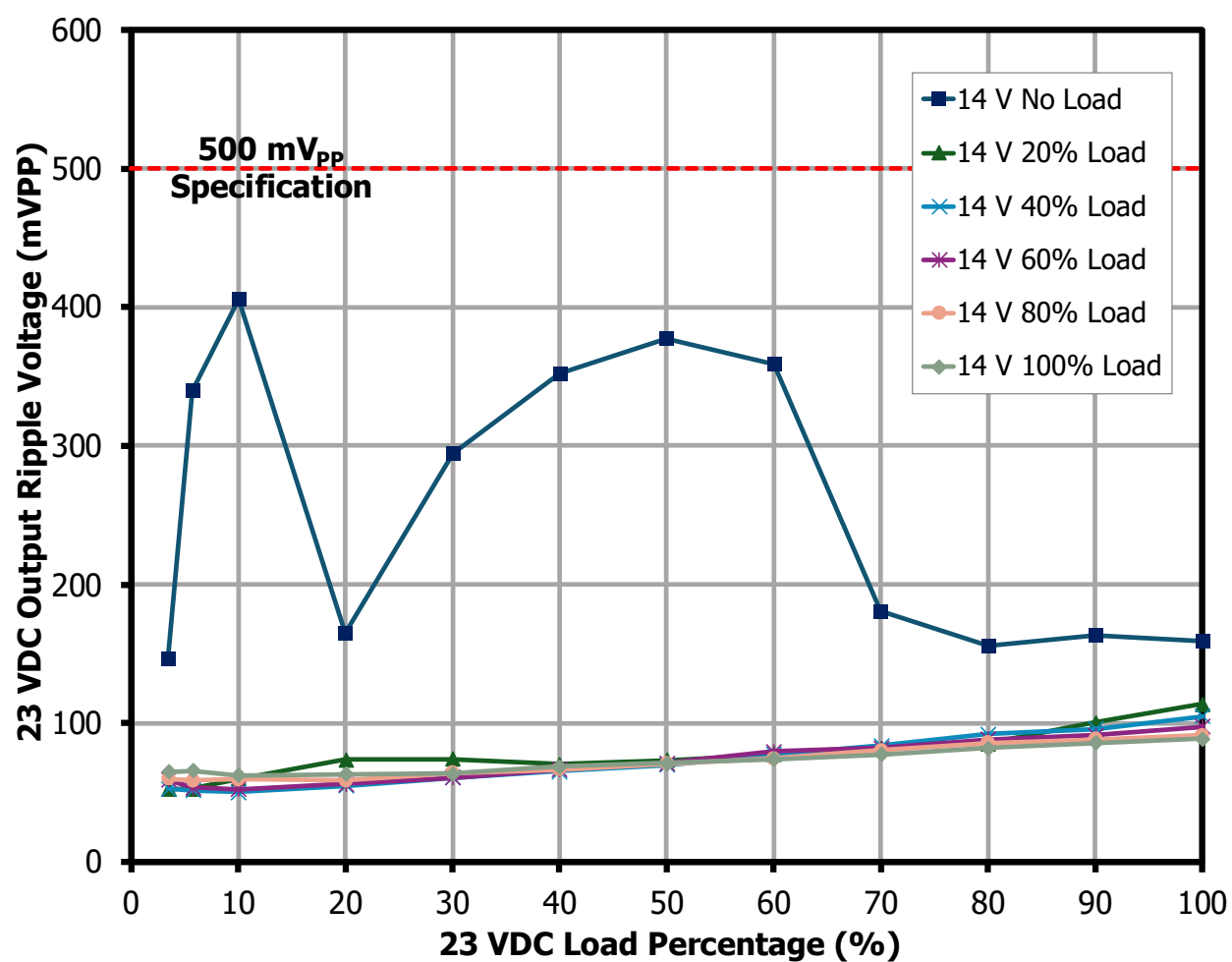


Figure 182 – 23 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

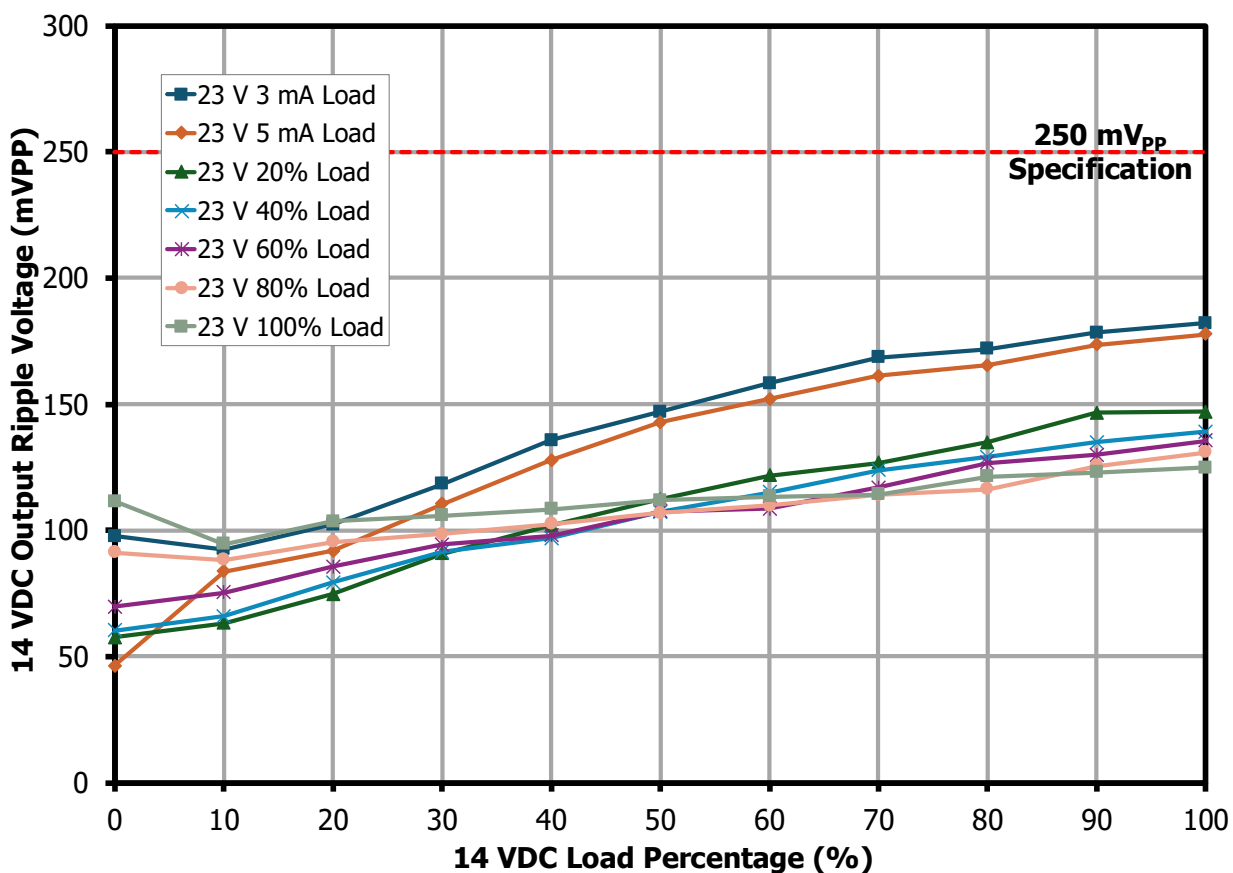


Figure 183 – 14 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

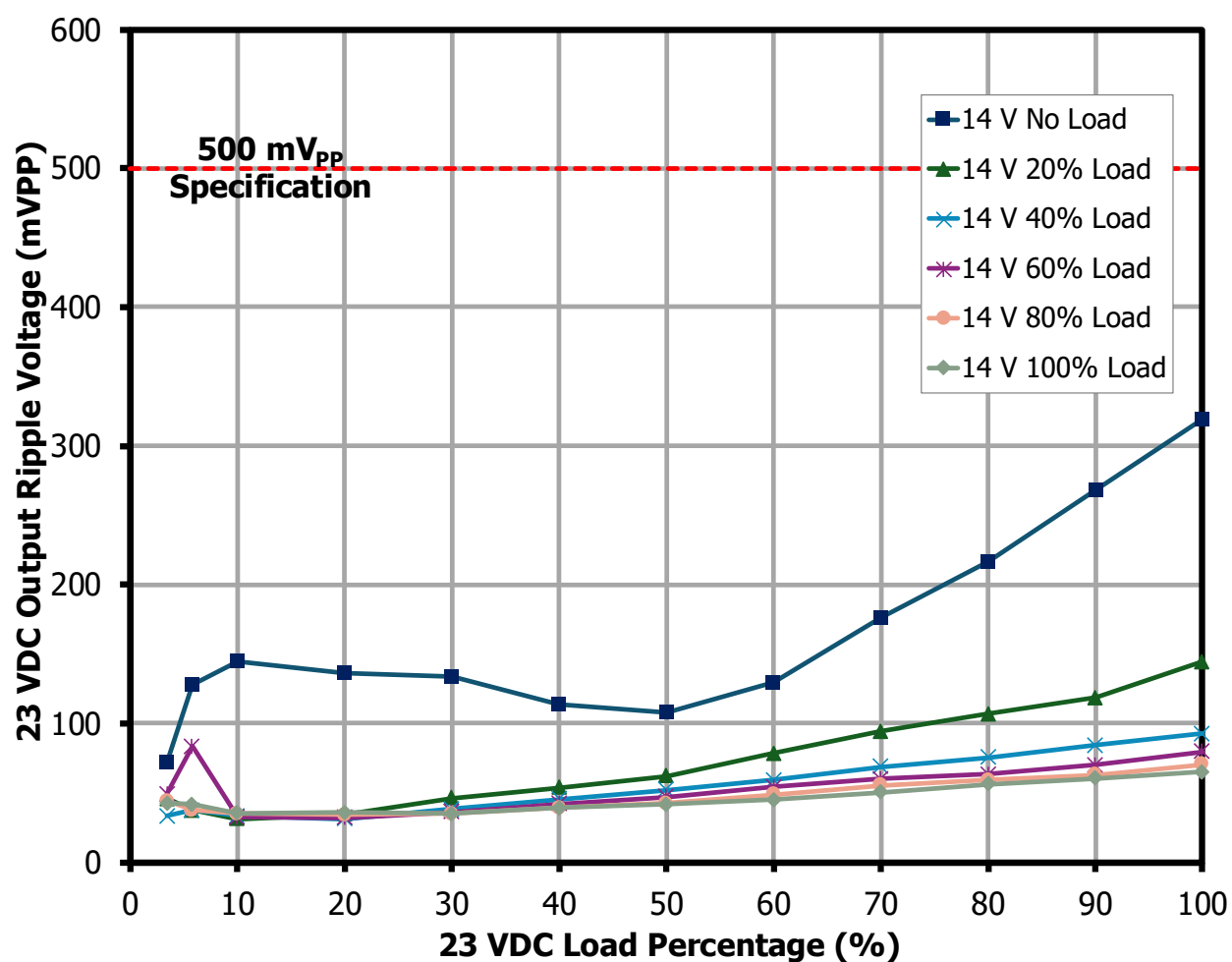


Figure 184 – 23 V Output Ripple Voltage at 200 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

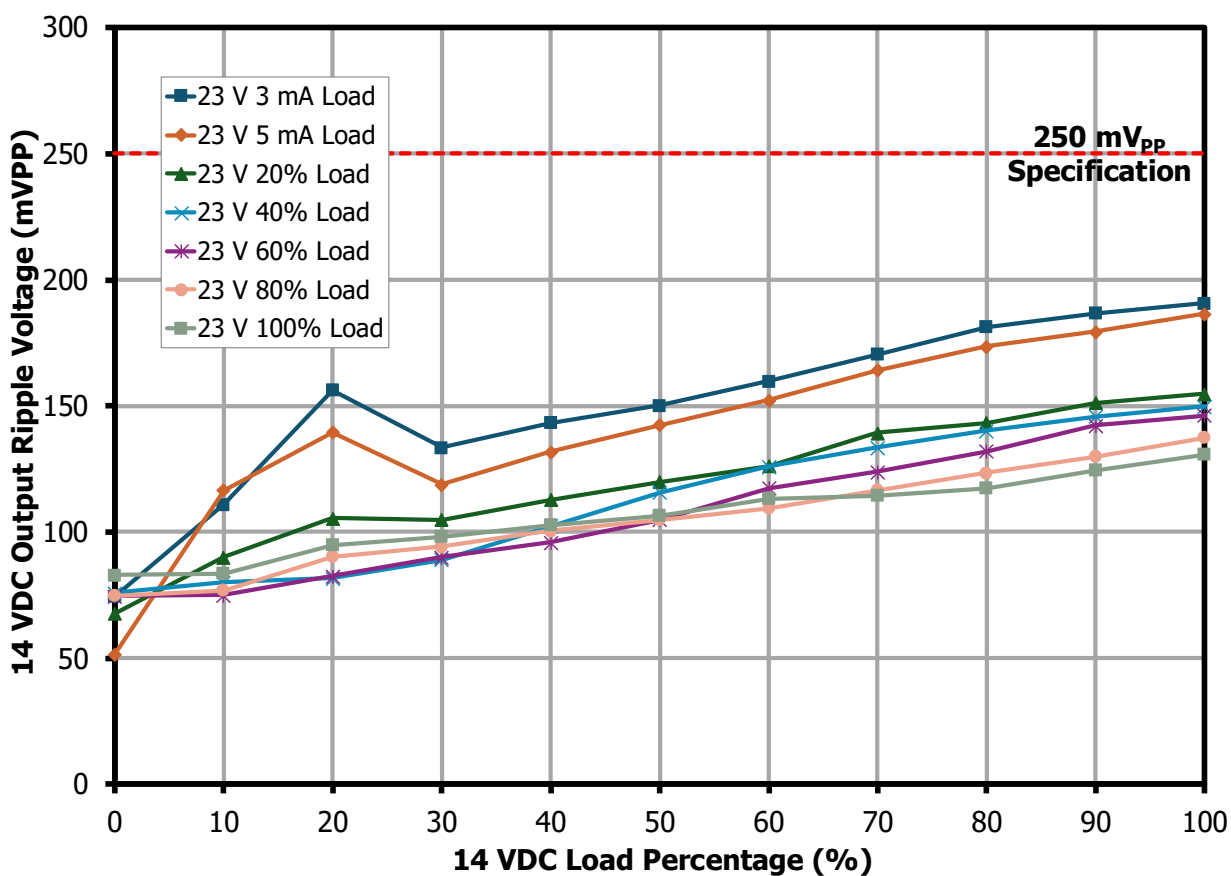


Figure 185 – 14 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

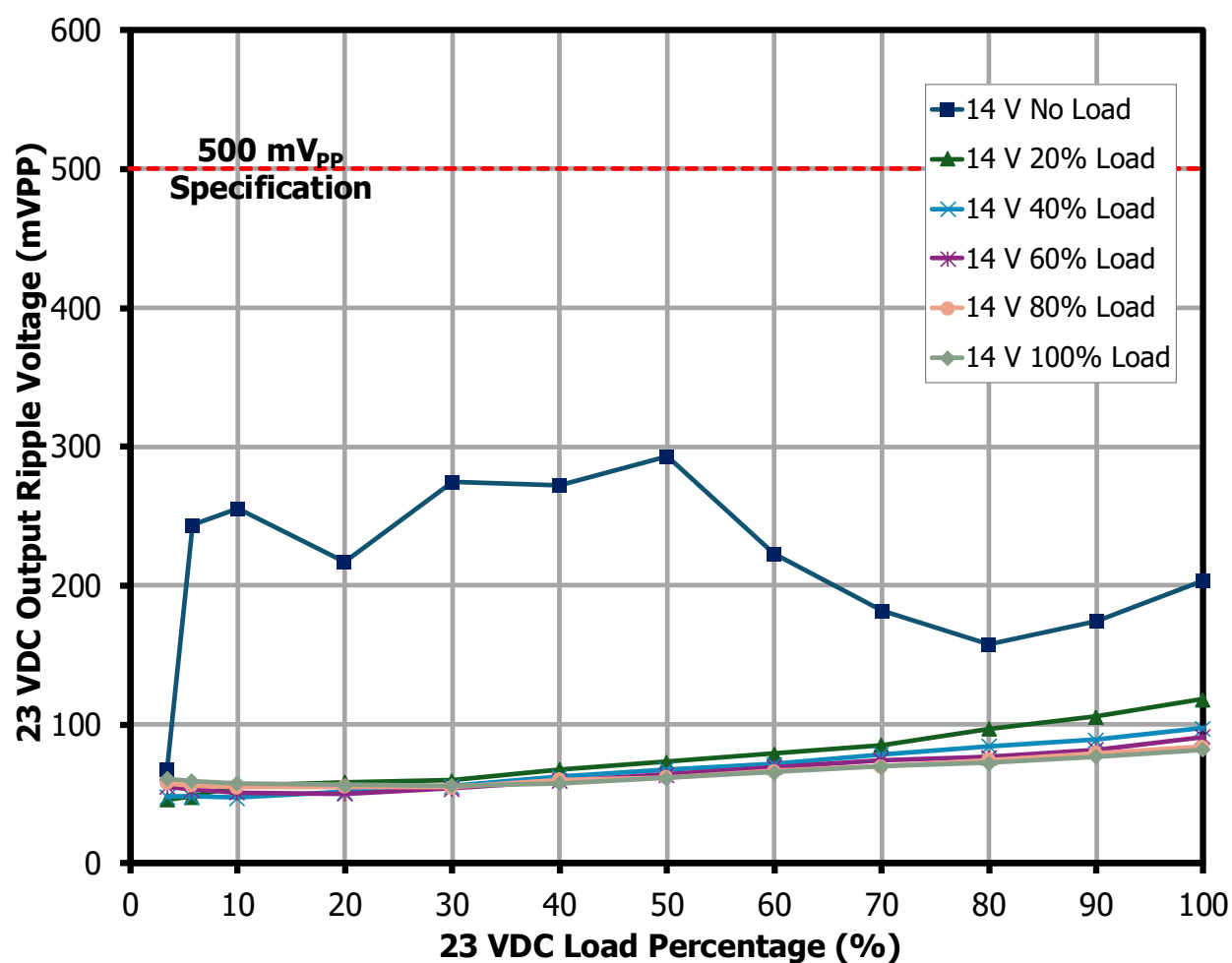


Figure 186 – 23 V Output Ripple Voltage at 800 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

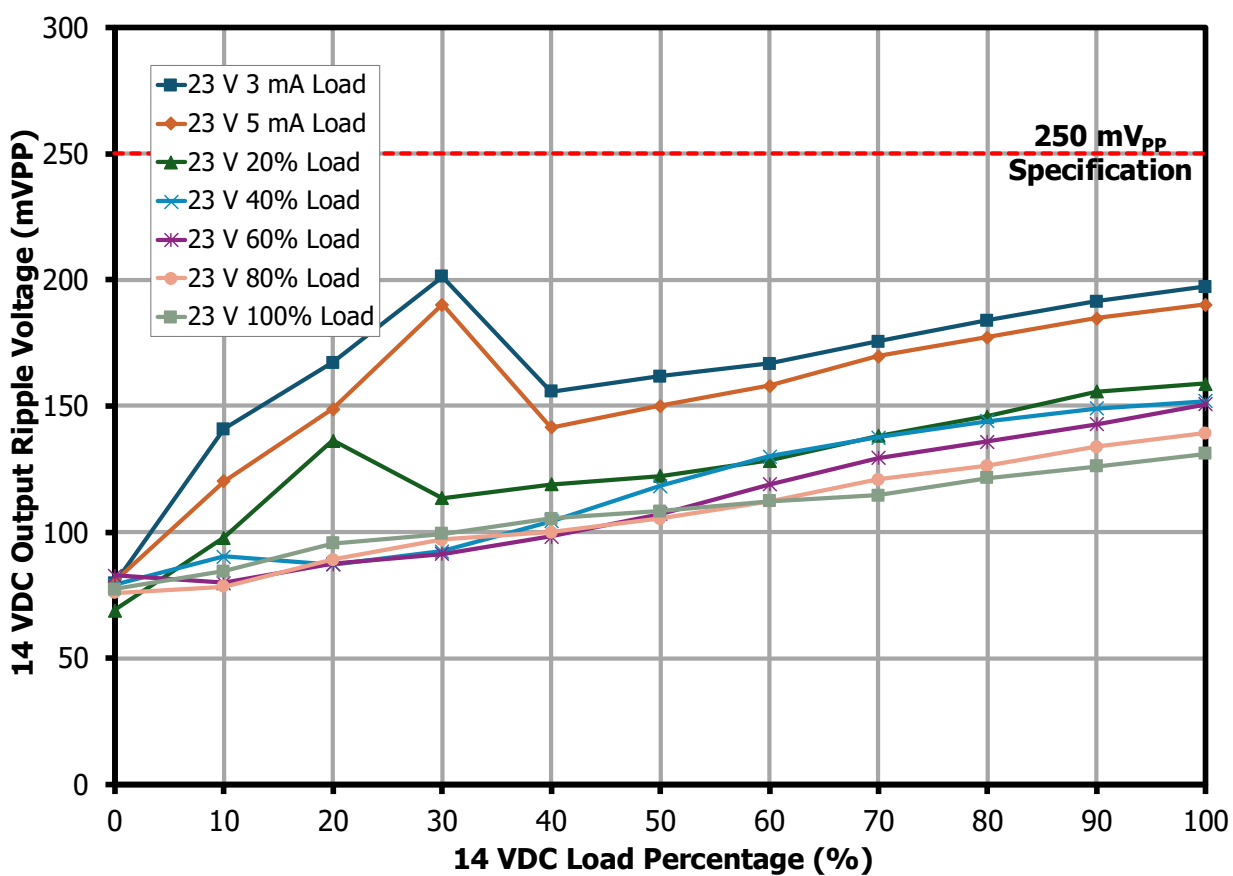


Figure 187 – 14 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

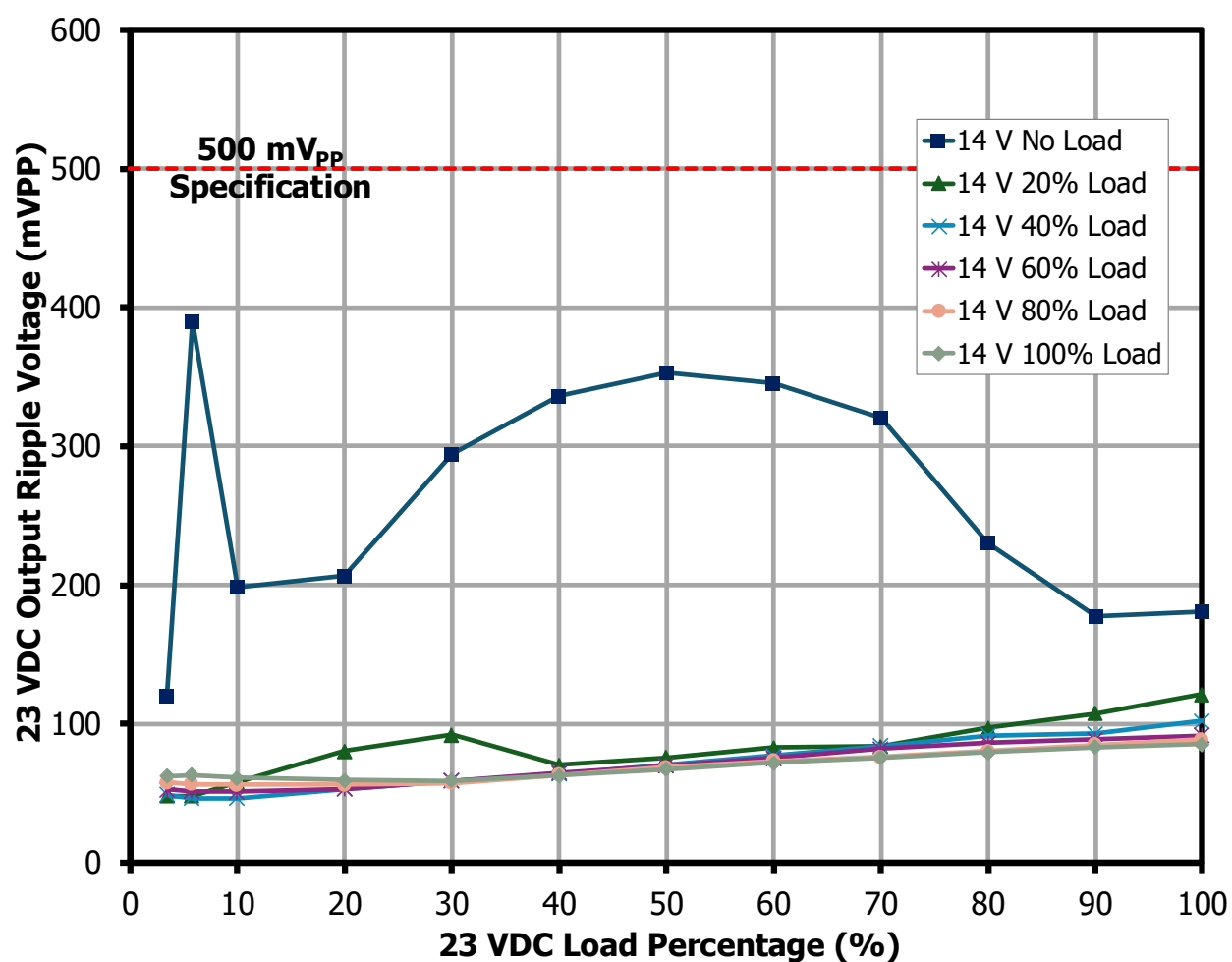


Figure 188 – 23 V Output Ripple Voltage at 1000 VDC Input Voltage Across Full Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. Output voltage and output current measurements were taken 60 seconds after every change in loading condition.

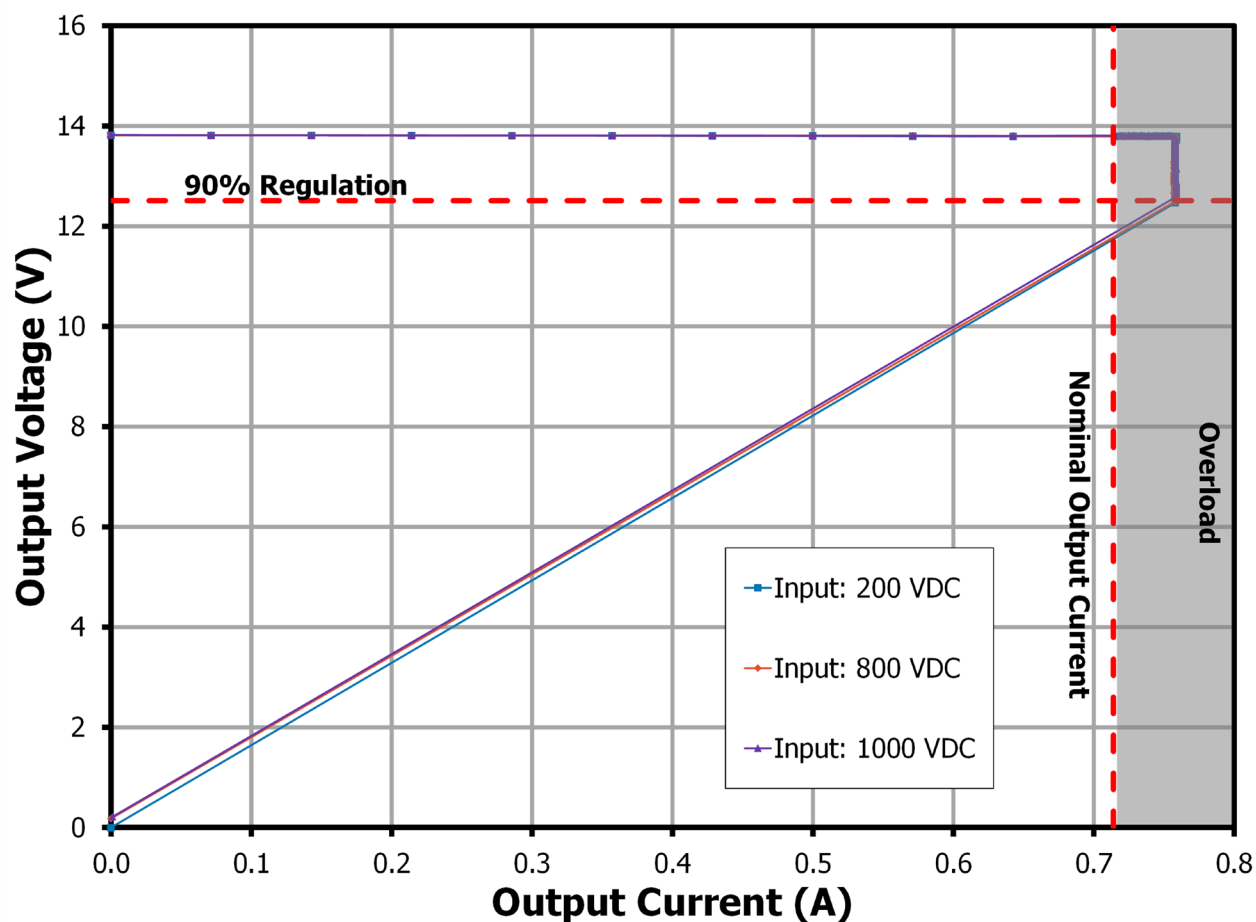


Figure 189 – Output Overload Curve at 85 °C Ambient.

13 Maximum Output Power

The unit under test was placed inside a thermal chamber with ambient temperature set to 85 °C. Maximum output power at each given input voltage was determined by finding the maximum loading condition at which the unit did not enter auto-restart (AR) or trigger any overtemperature protection. Case temperatures for critical components were also considered when determining the maximum output power capability for the power supply.

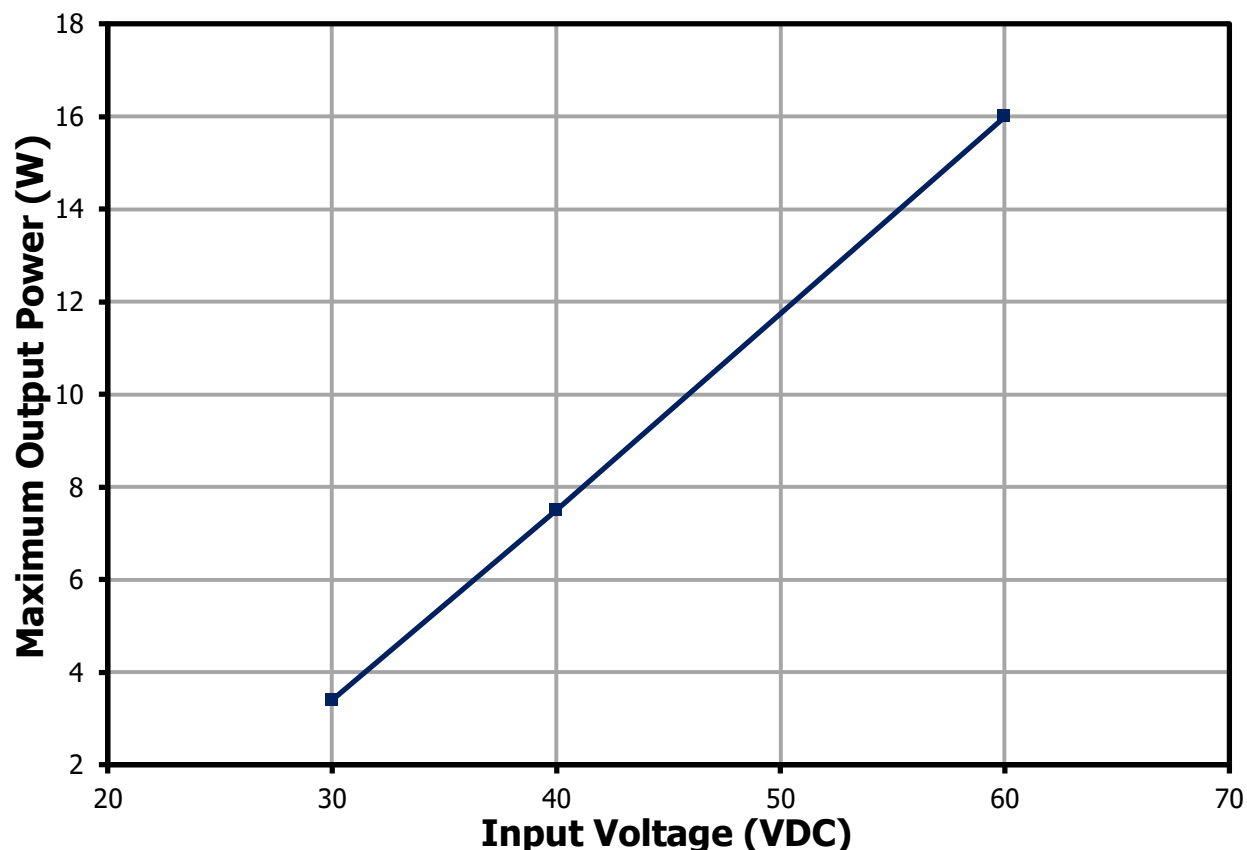


Figure 188 – Maximum Continuous Output Power Curve at 85 °C Ambient.

Input Voltage	Maximum Output Power	Limiting Factor
60 V _{DC} ²⁵	16 W	-
40 V _{DC}	7.5 W	Full Load Startup
30 V _{DC}	3.4 W	Full Load Startup

Table 15 – Limiting Factors on Maximum Output Power.

²⁵ The unit is able to full load start-up from 60 VDC to 200 VDC input supply.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
11-Mar-25	RP	A	Provisional Report Release.	Apps & Mktg
27-May-25	RP	B	Release Full Report. Updated Bill of Materials. Added Section 9.1 No-Load Input Power. Added Section 13 Maximum Output Power.	Apps & Mktg
07-Sep-26	RP	C	Convert DER to RDR. Update Schematic to include value for R108 and C106. Include R108 and C106 in BOM	Apps & Mktg



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