

Design Example Report

Title	70 W Automotive Power Supply for 400 V Systems Using InnoSwitch™3-AQ INN3949CQ
Specification	190 VDC – 450 VDC Input; 14 V / 5 A Output
Application	μDCDC / 12 V Battery Replacement
Author	Automotive Systems Engineering Department
Document Number	DER-1035Q
Date	December 17, 2024
Revision	B

Summary and Features

- Ultra-compact design for 400 VDC automotive BEV applications
- Low component count (only 66 electrical components)¹
- Full output power from 190 VDC to 450 VDC input²
- Transformer provides 450 V reinforced isolated (IEC-60664-1 and IEC-60664-4 compliant)
- ≥94% full load efficiency across the input voltage range
- ≤1% output voltage regulation across line and load
- Secondary-side control without optocouplers
- Ambient operating temperature range: -40 °C to 85 °C
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface mounted (SMD) components³
- Low profile, only 30 mm high

¹ Power conversion stage only, excluding input and output ports. See Figure 5

² Derated power below 190 VDC input. See Figure 86

³ AEC-Q200 transformer qualification and AEC-Q qualified SR MOSFET selection belong to final design.

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Disclaimer:

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1 Introduction

This engineering report describes a 70 W single-output automotive power supply intended for 400 V battery system electric vehicles. The design supports a wide input range of 190 VDC to 450 VDC. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides by observing the creepage and clearance requirements according to IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic, printed circuit board (PCB) layout, bill of materials (BOM), specification for the magnetics, and performance data.

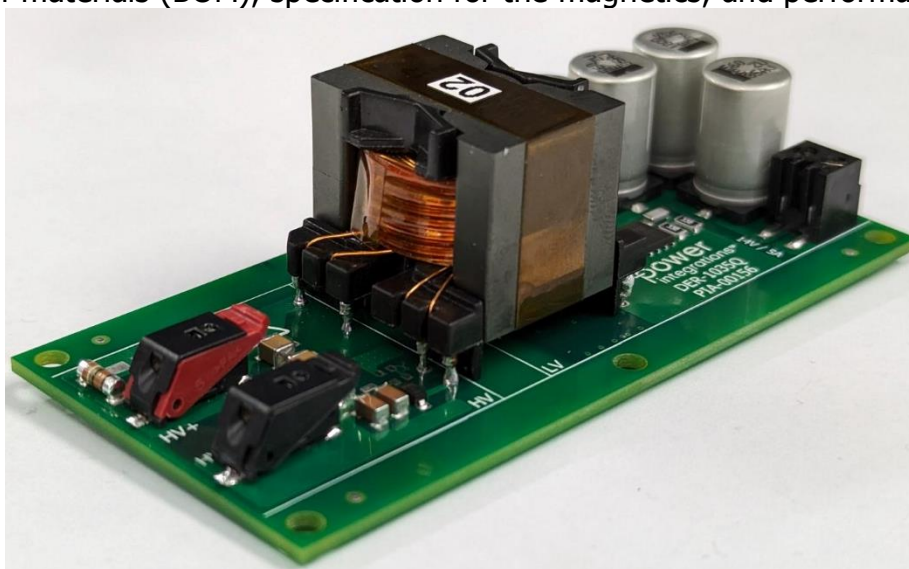


Figure 1 — Populated Circuit Board, Entire Assembly.

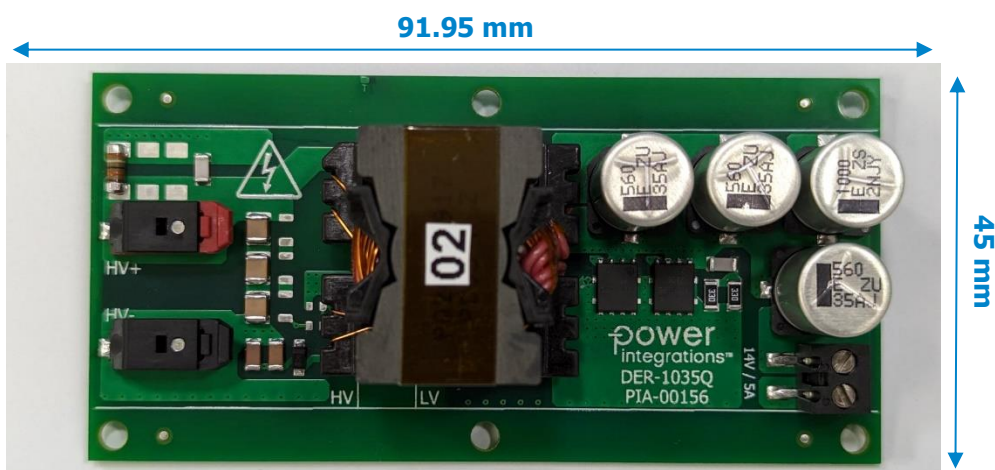


Figure 2 — Populated Circuit Board, Top.

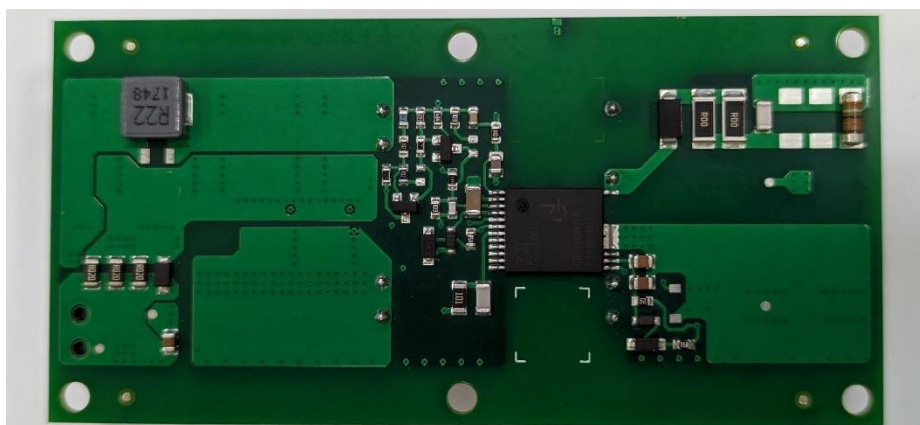


Figure 3 – Populated Circuit Board, Bottom.

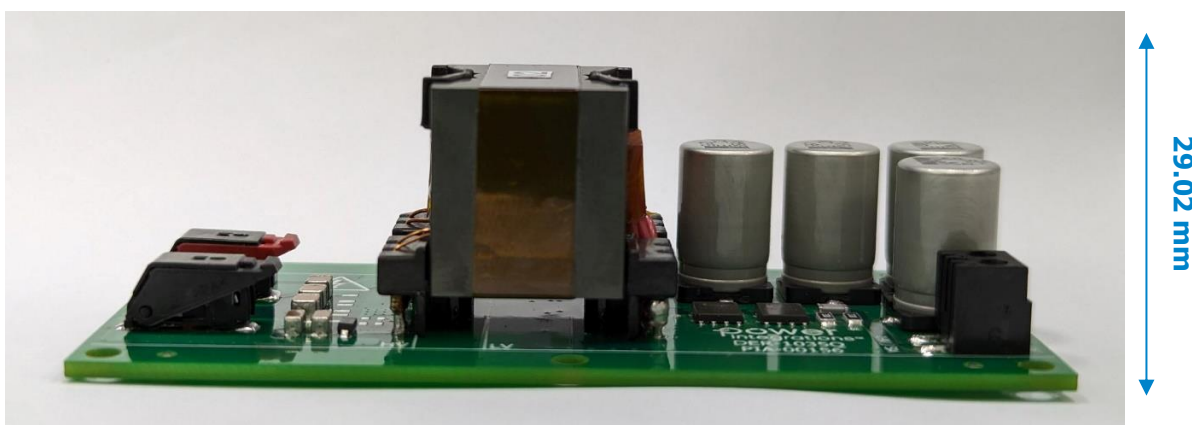


Figure 4 – Populated Circuit Board, Side.

The design can deliver 70 W output power continuously at 85 °C ambient from 190 VDC to 450 VDC input voltage range. The 14 V output configuration allows the design to replace a vehicle's auxiliary battery, helping reduce weight and maintenance requirements.

The InnoSwitch3-AQ IC provides accurate regulation by directly sensing the output voltage and providing fast feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also provides gate drive for synchronous rectification improving overall efficiency (compared to conventional diode rectifier), thus saving space by eliminating heatsinks.

2 Design Specification

The following tables represent the performance requirement for the design.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	HV	190 ⁴	300	450	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	13.8	14.0	14.2	VDC
Ripple Voltage Measured on Board	V_{RIPPLE}			150	mV
Output Current Parameters					
Output Current	I_{OUT}		5000		mA
Output Power Parameters					
Continuous Output Power at 190 VDC – 450 VDC Input	P_{OUT}		70.0 ⁵		W
Output Overshoot and Undershoot During Dynamic Load Condition	Δ V_{OUT}	-200		200	mV
Operating Parameters					
Operating Switching Frequency	f_{sw}	25		52	kHz

Table 1 – Electrical Specifications.

⁴ Operation with lower input voltage is possible with output power derating.

⁵ For maximum output power capability at VDC less than 190 V, see Section 12.



2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			720	V
Working Voltage	V_{WORKING}			450	V
Pollution Degree	PD			2	
CTI for FR4	CTI	175			
Rated Impulse Voltage	V_{IMPULSE}			2.50	kV
Altitude Correction Factor for h _a	Ch_a	1.59			
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	CLR_{REINFORCED}	4.8			mm
Basic Creepage Distance Requirement for PCB	CPG_{BASIC(PCB)}	3.6			mm
Reinforced Creepage Distance Requirement for PCB	CPG_{REINFORCED(PCB)}	7.2			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60 s	V_{ISO}	5000			V _{PK}
Partial Discharge Test Voltage	V_{PD_TEST}	1080			V _{PK}

Table 2 – Isolation Coordination⁶.

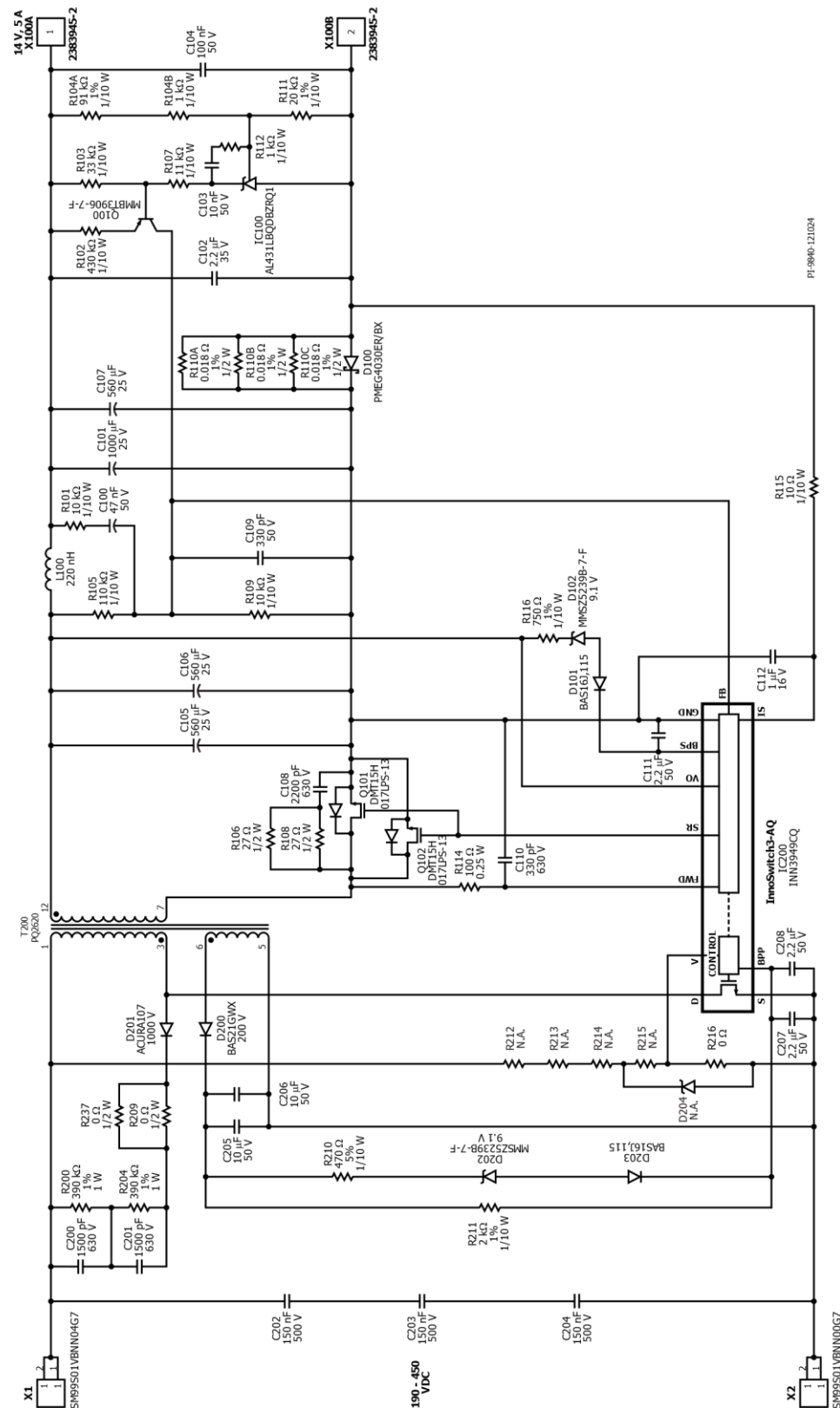
2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T _a	-40		85	°C
Altitude of Operation	h _a			5500	m

Table 3 – Environmental Specifications.

⁶ Clearance and creepage distances were derived from IEC 60664-1 and IEC 60664-4.

3 Schematic



4 Circuit Description

4.1 High-Voltage Circuit

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from a high-voltage input. The flyback transformer T200 primary winding is connected between the high-voltage DC input and the drain terminal of the 1700 V SiC power switch integrated into the InnoSwitch3-AQ IC (IC200).

An R2CD-type snubber circuit is placed across the primary winding to limit the drain-source voltage peaks during turn-off. A super-fast (or better) surface-mount, AEC-Q qualified diode should be used for the snubber. Diode D201 meets creepage and clearance requirements and ensures that the reverse voltage across the diode does not exceed 75% rating. Capacitors C200 and C201 store the energy from the leakage inductance of the transformer (T200). The capacitor values are selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation through the switching cycle. Resistors R200 and R204 dissipate the energy stored by the snubber capacitors. The resistor values are selected such that the snubber voltage will not exceed 80% of their voltage rating and to ensure that they will dissipate less than 50% of their rated power.

The transformer auxiliary winding provides power to the primary-side of the InnoSwitch3-AQ IC during normal operation. This minimizes the power derived from the internal high-voltage current source, improving overall efficiency, and reducing heating of InnoSwitch3-AQ IC. The auxiliary winding output is rectified and filtered by diode D200 and capacitors C205 and C206. The InnoSwitch3-AQ IC is self-starting, using an internal high-voltage current source to charge the BPP capacitors (C207 and C208). Current is fed to the BPP pin through resistor R211. Diodes D203, D202, and resistor R210 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) as long as the fault is present.

4.2 InnoSwitch3 Input Undervoltage Protection

The V pin of the InnoSwitch3-AQ IC is used to provide line undervoltage protection.

The InnoSwitch3-AQ IC is enabled when the current injected into the V pin is above the UV pin brown-in threshold ($I_{UV+} = 27 \mu\text{A}$), until this current is reached, the device is held off. The V pin is disabled by connecting the pin to the HV RTN by using jumper resistor R216. Additional provisions for setting the UV function are included. Resistors R212 to R214 must be sized such that the current injected into the V pin is above the brown-in threshold after D204 clamps the voltage between R214 and R215.

4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR



FETs Q101 and Q102 rectify the voltage across the secondary winding of the transformer (T200), which is then filtered by output capacitors C105 to C106. An RC-type snubber formed by resistors R106 and R108 and capacitor C108 damps high-frequency ringing across the SR FET.

The secondary-side controller inside InnoSwitch3-AQ IC controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed from the FWD pin via resistor R114. Capacitor C110 and resistor R114 form a low pass filter that reduces the voltage spike seen by the FWD pin during SR turn-off and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode, the SR gate signal is turned off before the secondary-side controller requests a new switching cycle from the primary. In discontinuous conduction mode, the SR FET is turned off when the voltage across it rises above $V_{SR(TH)}$ (~ 3.3 mV). Secondary-side control of the primary-side power MOSFET eliminates cross-conduction and ensures reliable operation.

The secondary-side of InnoSwitch3-AQ IC is powered by either the secondary winding forward voltage (thru R114 and the FWD pin) or the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C111 via an internal regulator.

Diodes D101, D102, and resistor R116 provide a secondary-side output overvoltage protection (secondary OVP). During output overvoltage events, current will be injected into the BPS pin of InnoSwitch3-AQ IC through these components and causes the IC to enter auto-restart (AR) mode. This network protect for faults on the secondary when the secondary controller is functional. When the secondary controller is not functional, the primary side BPP pin based output OV function is recommended.

The InnoSwitch3-AQ IC has an internal reference of 1.265 V which is presented on the FB pin. Resistors R105 and R109 form a voltage divider feedback network. For this design, the output voltage value set by R105 and R109 is 10-15% higher than the rated output voltage as a requirement for implementing the Precise Voltage Regulation circuit. Capacitor C109 provides decoupling from high-frequency. Capacitor C100 and resistor R101 form a feedforward network to speed up response time and lower output ripple.

Output current is sensed by monitoring the voltage drop across parallel resistors R110A to R110C. The resulting analog current is filtered using R115 and C112 and monitored by the IS pin reference to SECONDARY GROUND. An internal current sense threshold of approximately 35 mV is used to reduce losses. Once the threshold is met, InnoSwitch3-AQ IC will control the number of pulses and amplitude of primary switching cycles to maintain a fixed output current. The IC enters auto-restart (AR) operation when the output voltage falls below 90% of regulation and recovers when the load current is reduced below the CC limit. Diode D100 limits the voltage drop across R110A to R110C to protect the IS pin during overload or short-circuit conditions.

4.4 Precision Voltage Regulation (PVR) Circuit ⁷

The PVR circuit improves output voltage regulation by employing an external error amplifier with a high-precision reference voltage (ATL431) to bias the FB pin. The PVR injects a DC bias current into the FB pin of InnoSwitch3-AQ IC to reduce the DC error at the output. The ATL431 error amplifier network is placed after the output filter inductor L100 and current sense resistors R110A to R110C to compensate for voltage drops.

The ATL431LIBQDBZRQ1 voltage reference IC was selected for its high precision and stability across temperatures. The output voltage is sensed through voltage dividers R104A, R104B and R111. The resistor values are chosen such that at the rated output voltage, the voltage on the REF pin of IC100 equals the reference voltage of 2.5 V. IC100 sinks cathode current proportional to the difference between the scaled output voltage and its internal reference. The amount of cathode current controls the amount of current injected into the FB node. Capacitor C103 lowers the bandwidth of the PVR circuit so that it only corrects for DC error.

Resistors R103 and R107 provide the base current path for Q100 and bias current to IC100. Together with R102, the values of these resistors were chosen such that IC100 and Q102 are kept away from saturation and provide adequate margin for the base and cathode currents to swing during load transients. While operating in the forward active region, Q100 acts as a variable impedance in parallel to the upper feedback resistor R105.

⁷ Circuit implementation is only necessary if output voltage regulation needs to be within 1%.

5 PCB Layout

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

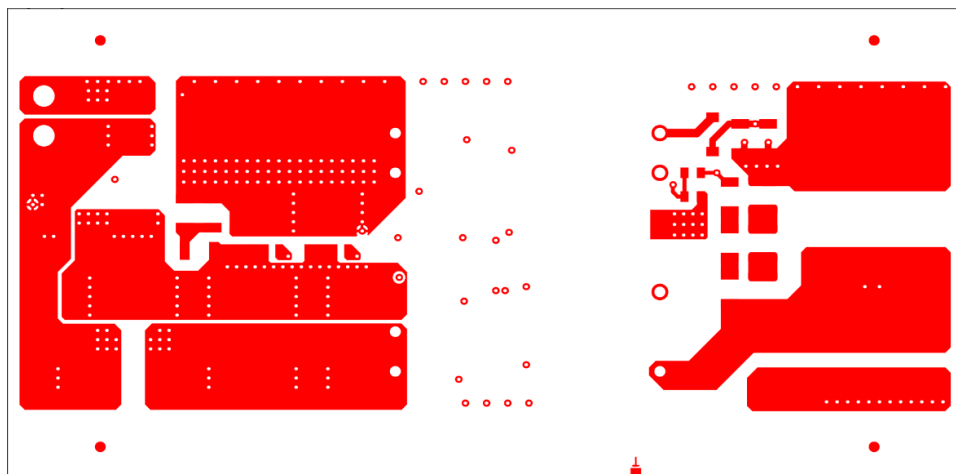


Figure 6 – DER-1035Q Top Layer PCB Layout.

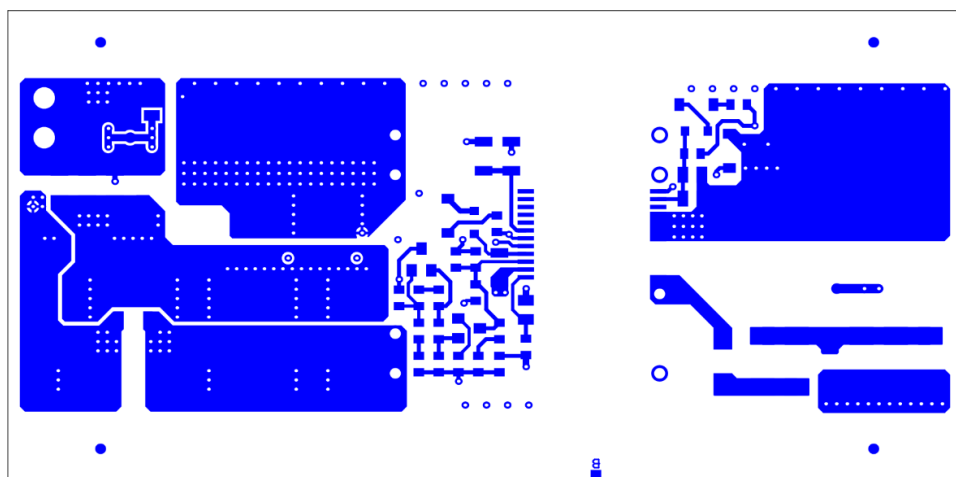


Figure 7 – DER-1035Q Bottom Layer PCB Layout.

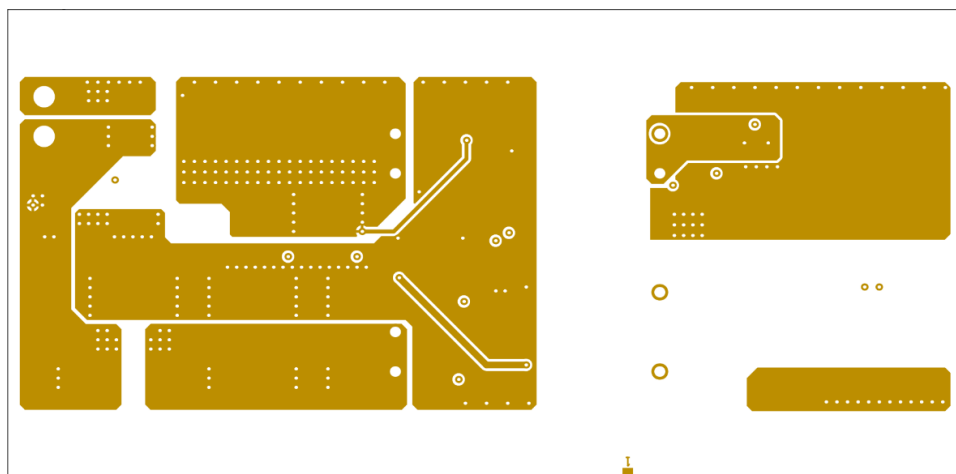


Figure 8 – DER-1035Q Mid-Layer 1 PCB Layout.

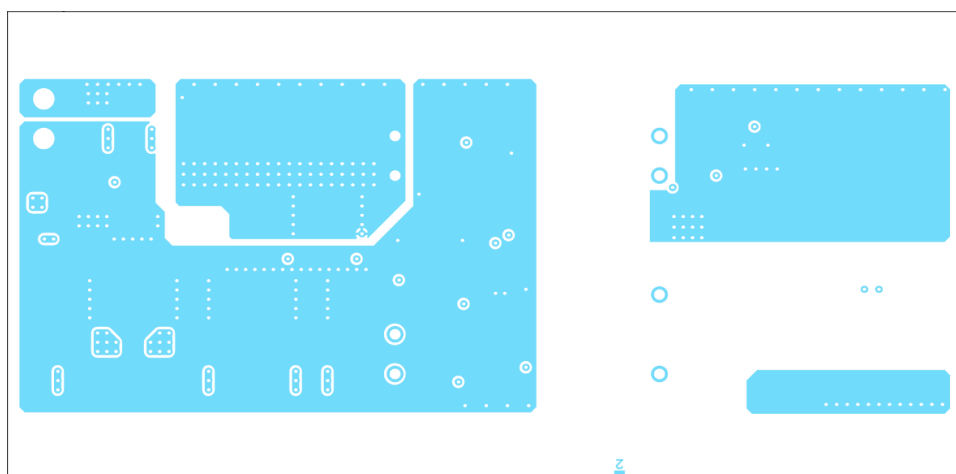


Figure 9 – DER-1035Q Mid-Layer 2 PCB Layout.

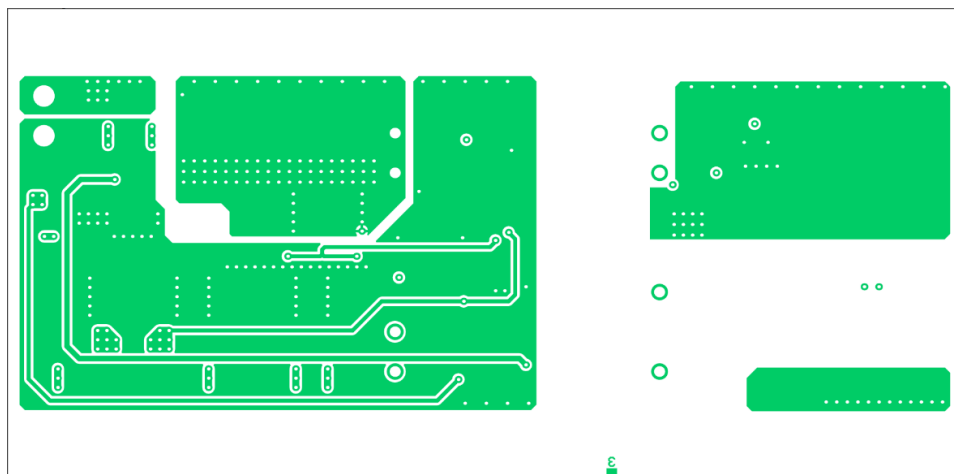


Figure 10 – DER-1035Q Mid-Layer 3 PCB Layout.

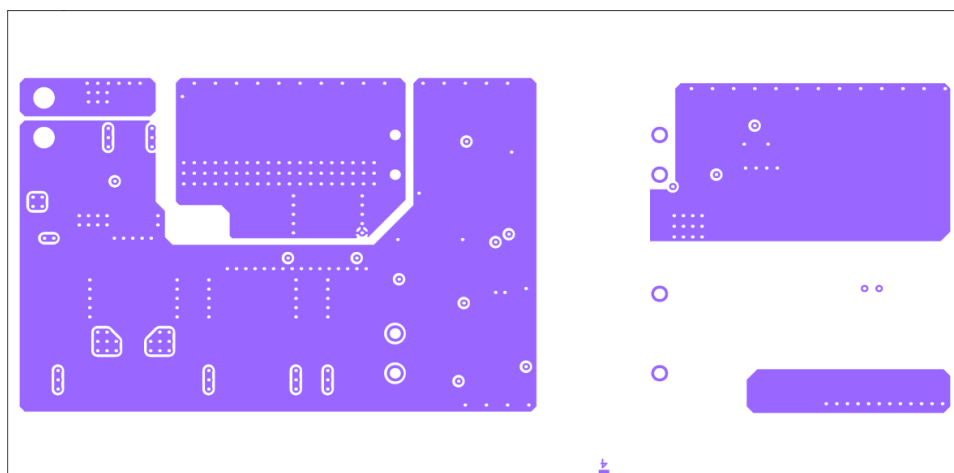
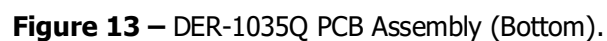
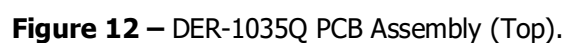


Figure 11 – DER-1035Q Mid-Layer 4 PCB Layout.



6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 47 nF X7R/50 V/10% 0603	C0603C103K5RACAUTO7411	KEMET
2	1	C101	Polymer Aluminium Capacitor 1000 µF AL/25 V/20% 10.3X10.3 mm	EEH-ZS1E102UP	Panasonic
3	1	C102	Ceramic Chip Capacitor 2.2 µF X7R/35 V/10% 0805	CGA4J1X7R1V225K125AC	TDK
4	1	C103	Ceramic Chip Capacitor 10 nF X7R/50 V/10% 0603	C0603C103M5RACAUTO	KEMET
5	1	C104	Ceramic Chip Capacitor 100 nF X7R/50 V/10% 0603	CGA3E2X7R1H104K080AA	TDK
6	3	C105, C106, C107	Polymer Aluminium Capacitor 560 µF AL/25 V/20% 10.3X10.3 mm	EEH-ZU1E561P	Panasonic
7	1	C108	Ceramic Chip Capacitor 2.2 nF C0G/630 V/5% 1206	GCM31B5C2J222JX01L	Murata
8	1	C109	Ceramic Chip Capacitor 330 pF C0G/50 V/5% 0603	GCM1885C1H331JA16D	Murata
9	1	C110	Ceramic Chip Capacitor 330 pF C0G/630 V/5% 1206	CGA5C4C0G2J331J060AA	TDK
10	1	C111	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 1206	GCM31CR71H225KA55K	Murata
11	1	C112	Ceramic Chip Capacitor 1 µF X7R/50 V/10% 0805	CGA4J3X7R1H105K125AB	TDK
12	2	C200, C201	Ceramic Chip Capacitor 1500 pF C0G/630 V/5% 1206	CGA5H4C0G2J152J115AA	TDK
13	3	C202, C203, C204	Ceramic Chip Capacitor 150 nF X7R/500 V/10% 1210	C1210X154KCRACAUTO	KEMET
14	2	C205, C206	Ceramic Chip Capacitor 10 µF X7R/50 V/10% 1206	CGA5L1X7R1H106K160AC	TDK
15	2	C207, C208	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 0805	CGA4J3X7R1H225K125AE	TDK
16	1	D100	Schottky Diode PMEG4030ER/8X 40 V/3 A SOD123W	PMEG4030ER/8X	Nexperia
17	2	D101, D203	Diode 100 V 250 mA Surface Mount SOD-323F	BAS16J,115	Nexperia
18	2	D102, D202	Zener Diode 9.1 V 500 mW ±5% SMT SOD-123 MMSZ5239B-7-F 9.1 V SOD-123	MMSZ5239B-7-F	Diodes, Inc.
19	1	D200	Diode Standard 200 V 225 mA (DC) SMT SOD-123 BAS21GWX 200 V / 225 mA SOD-123	BAS21GWX	Nexperia
20	1	D201	DIODE SCHOTTKY 1 kV 1 A ACURA107 1000 V / 1 A DO-214AC (SMA)	ACURA107-HF	Comchip
21	1	D204	not assembled Diode N.A. SOD123	N.A.	N.A.
22	1	IC100	Voltage References Automotive, high-bandwidth, low-IQ programmable shunt regulator ATL431LIBQDBZRQ1 2.5 V to 36 V SOT-23	ATL431LIBQDBZRQ1	Texas Instruments
23	1	IC200	InnoSwitch3-AQ 4.65 V to 5.15 V/V _{mos} =1700 V InSOP-24D	INN3949CQ	Power Integrations
24	1	L100	Shielded Power Inductor 220 nH 7.00 mm x 6.60 mm	SRP7028TA-R22Y	Bourns
25	1	Q100	40 V / 0.2 A PNP bipolar transistor MMBT3906-7-F PNP/40 V/0.2 A/300 mW SOT-23	MMBT3906-7-F	Diodes, Inc.
26	2	Q101, Q102	N-Channel MOSFET DMT15H017LPS-13 150 V 9.4 A (Ta), 58 A (Tc) 1.3 W (Ta) PowerDI5060-8	DMT15H017LPS-13	Diodes, Inc.
27	1	R100	Thick Film Chip Resistor N.A. 1%/0.25 W/200 V 1206	N.A.	N.A.
28	2	R101, R109	Thick Film Chip Resistor 10 kΩ 5%/0.1 W/75 V 0603	AC0603JR-0710KL	YAGEO
29	1	R102	Thick Film Chip Resistor 430 kΩ 5%/0.1 W/150 V 0603	ERJ-3GEYJ434V	Panasonic
30	1	R103	Thick Film Chip Resistor 33 kΩ 5%/0.1 W/150 V 0603	RMCF0603JT33K0	Stackpole
31	1	R104A	Thick Film Chip Resistor 91 kΩ 1%/0.1 W/150 V 0603	RK73H1JTTD9102F	KOA Speer
32	2	R104B, R112	Thick Film Chip Resistor 1 kΩ 5%/0.1 W/75 V 0603	CRGCQ0603J1K0	TE Connectivity
33	1	R105	Thick Film Chip Resistor 110 kΩ 5%/0.1 W/150 V 0603	RMCF0603JT110K	Stackpole
34	2	R106, R108	Thick Film Chip Resistor 27 Ω 5%/0.5 W/500 V 1206	SR1206FR-7W27RL	YAGEO
35	1	R107	Thick Film Chip Resistor 11 kΩ 5%/0.1 W/150 V 0603	RMCF0603JT11K0	Stackpole
36	2	R110A, R110B, R110C	Current Sense Resistor 0.018 kΩ 1%/ ½ W /200 V 1206	UCR18EVHFSR018	Rohm Semi
37	1	R111	Thick Film Chip Resistor 20 kΩ 1%/0.1 W/75 V 0603	ERJ-3EKF2002V	Panasonic
38	1	R114	Thick Film Chip Resistor 100 Ω 5%/0.25 W/200 V 1206	RMCF1206JT100R	Stackpole
39	1	R115	Thick Film Chip Resistor 10 Ω 5%/0.1 W/75 V 0603	CRGCQ0603J10R	TE Connectivity
40	1	R116	Thick Film Chip Resistor 750 Ω 1%/0.1 W/75 V 0603	CQ03WAF7500T5E	ROYALOHM
41	2	R200, R204	MELF Resistors 390 kΩ 1%/1 W/350 V MELF 0207	MMB02070C3903FB200	Vishay



42	6	R201, R202, R205, R206, R209, R237	MELF Resistors N.A. 1%/1 W/200 V MELF 0207	N.A.	N.A.
43	1	R210	Thick Film Chip Resistor 470 Ω 5%/0.1 W/75 V 0603	AC0603JR-13470RL	YAGEO
44	1	R211	Thick Film Chip Resistor 2 k Ω 1%/0.1 W/75 V 0603	RMCF0603FT2K00	Stackpole
45	3	R212, R213, R214	Thick Film Chip Resistor N.A. 1206	N.A.	N.A.
46	1	R215	Thick Film Chip Resistor N.A. 0603	N.A.	N.A.
47	1	R216	Thick Film Chip Resistor 0R 0603	RMCF0603ZT0R00	Stackpole
48	1	T200	PQ2620_THT PQ2620	PQ2620	Power Integrations
49	1	X1	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN04G7 RED	SM99S01VBNN04G7	METZ CONNECT
50	1	X100	TERMI-BLOK SMD MOUNT 180_2P_3.81 2383945-2 12 A 1x2Pin, Pitch 3.81 mm	2383945-2	TE
51	1	X2	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN00G7 BLACK	SM99S01VBNN00G7	METZ CONNECT
52	1	Z1	Printed Circuit Board PCB 1.55 mm PCB thickness 1.55 mm N		

Table 4 – DER-1035Q Bill of Materials⁸.

⁸ All components are AEC-Q qualified except the SR MOSFET, connectors, and transformer.



7 Transformer Specification (T200)

7.1 Electrical Diagram

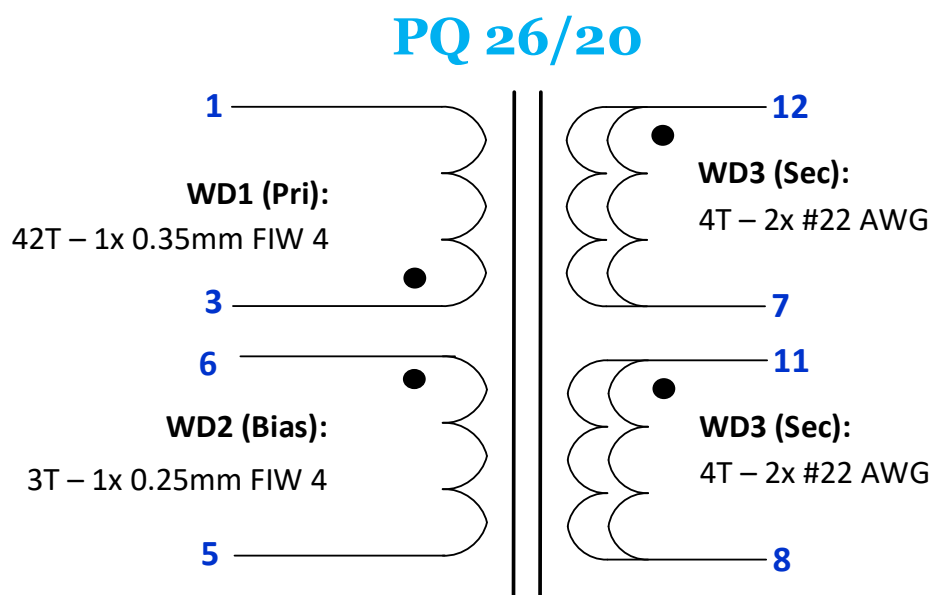


Figure 14 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			70.0	W
Input voltage VDC	Flyback topology	190	300	450	V
Switching frequency	Flyback topology			60	kHz
Duty cycle	Flyback topology	16.5		43.7	%
Np:Ns			11		
Rdc	Primary side		454		mΩ
Rdc	Secondary side		12.0		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V _{PK-PK} , 100 kHz frequency between pin 3 and pin 7, with pins 5-6 shorted, pins 1-3 shorted and pins 7-8-11-12 shorted at 25 °C		55.4		pF
Primary inductance	Measured at 1 V _{PK-PK} , 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		780		μH
Part to part tolerance	Tolerance of Primary Inductance		5.0		%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.		6.16		μH

Table 5 – Transformer (T1) Electrical Specifications.

7.3 Transformer Build Diagram

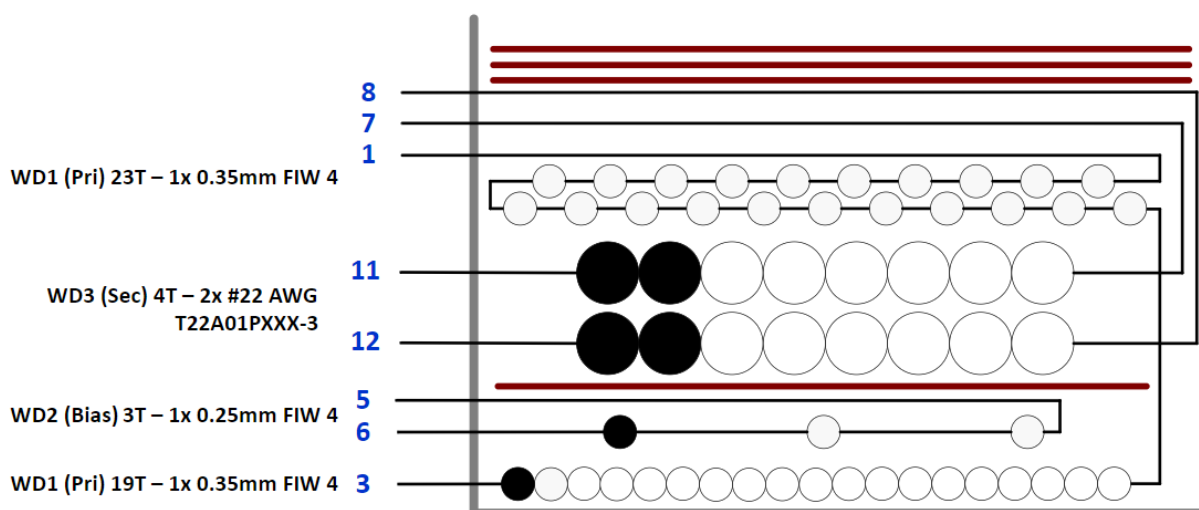


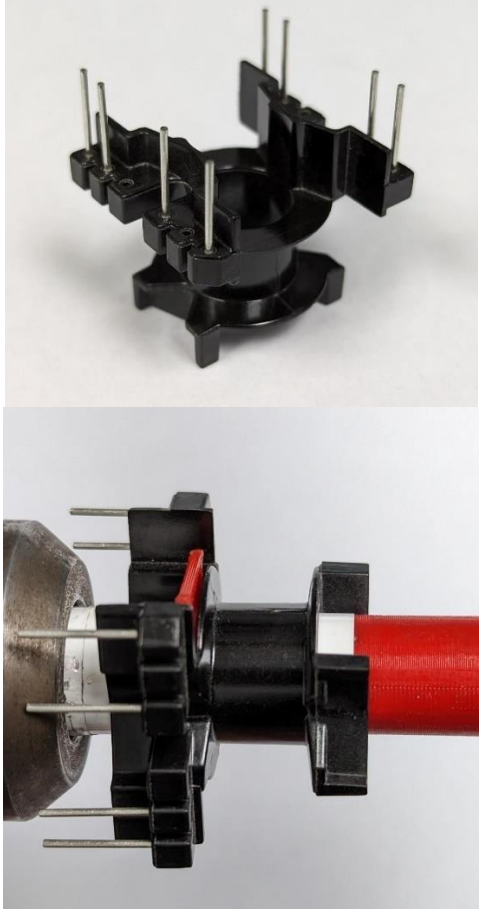
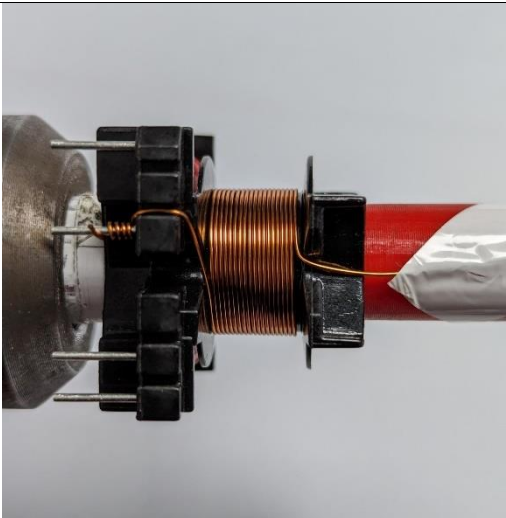
Figure 15 – Transformer Build Diagram.

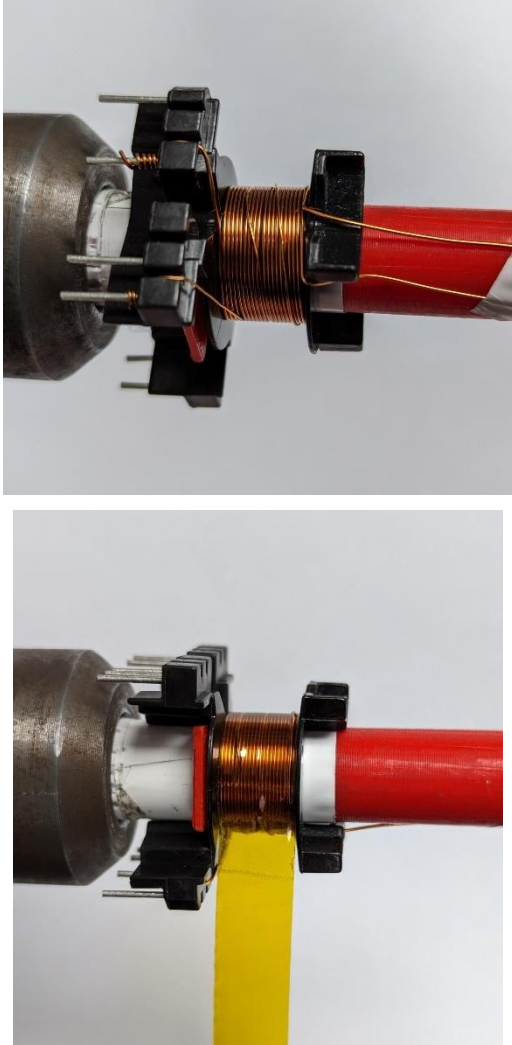
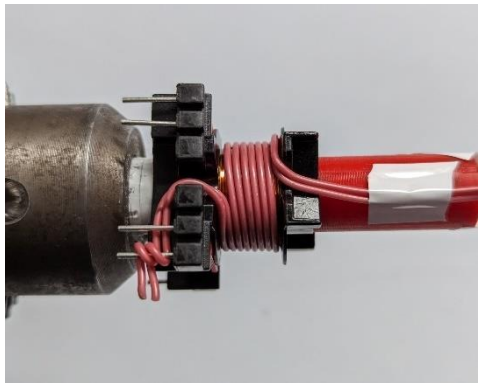
7.4 Material List


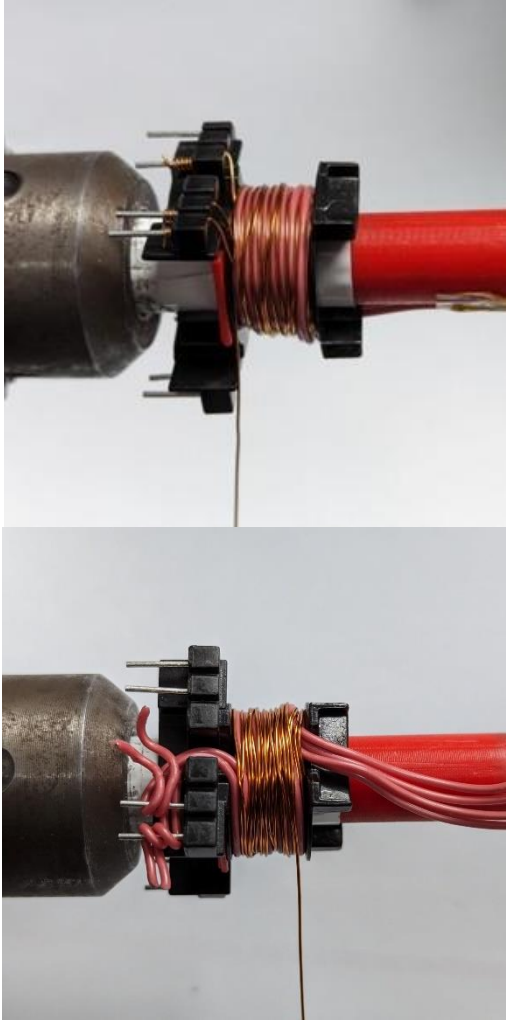
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: PQ26/20 – 2 (P6-S6)	1	PC	Phenolic	FerroxCube
[2]	Core: PQ26	2	PCS	PC95 (or equivalent)	TDK
[3]	WD1 (Pri): 0.35 mm FIW 4, Class F		mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.25 mm FIW 4, Class F		mm		Elektrisola
[5]	WD3 (Sec): AWG 22 PFA 0.003"		mm		Rubadue
[5]	3M Polyimide Film Tape 5413, width: 0.38 in (9.65 mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

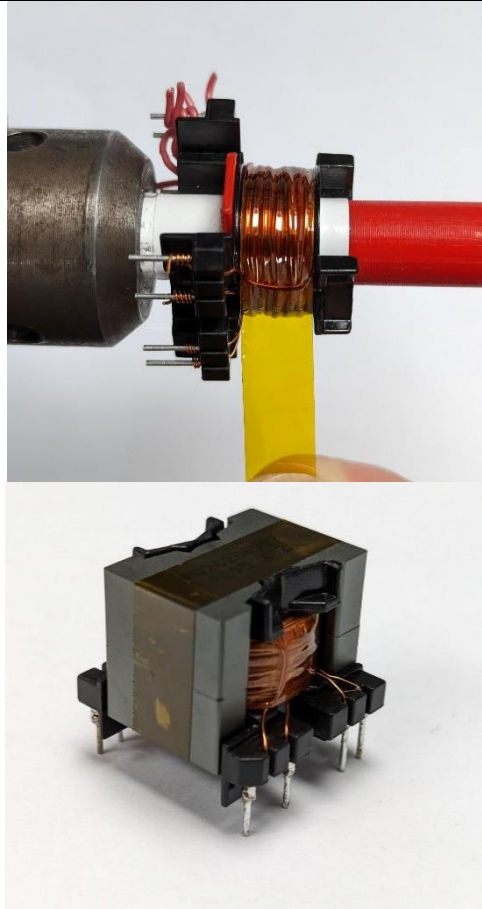
Table 6 – Transformer (T200) Material List.

7.5 Winding Instructions

Winding Preparation		<p>Start by removing the unused pins 2, 4, 5 and 10 of the bobbin.</p> <p>Position the bobbin on the mandrel such that the pins of the bobbin is on the left side. Winding direction is clockwise direction.</p>
WD1 (Primary)		<p>Use 0.35 mm FIW4 wire. Start on PIN 3.</p> <p>Wind the primary winding's first layer, 19 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p>

WD2 (Bias)		<p>Use 0.25 mm FIW4 wire. Start on PIN 6.</p> <p>Wind the bias winding, 3 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p> <p>Terminate bias winding at PIN 5.</p> <p>Secure using 1 Layer of tape.</p>
WD3 (Secondary)		<p>Use 2 x 22 AWG wire. Start on PIN 12.</p> <p>Wind the secondary winding's first layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p>

		<p>Use 2 x 22 AWG TIW wire. Start on PIN 11.</p> <p>Wind the secondary winding's second layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p>
WD1 (Primary)		<p>Continue winding the primary wire.</p> <p>Wind the primary winding's second layer, 12 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p> <p>Continue winding the primary wire.</p> <p>Wind the primary winding's third layer, 11 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.</p>

Finishing

Terminate primary winding at PIN 1.

Terminate secondary winding at PIN 7 and 8.

Secure using 3 Layers of tape.

Mount the gapped core using glue (a polyester film electrical tape can be used as alternative)

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3A Q_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VOUT	14.00		14.00	V	Output Voltage
4	OPERATING CONDITION 1					
5	VINDC1	190.00		190.00	V	Input DC voltage 1
6	IOUT1	5.00		5.000	A	Output current 1
7	POUT1			70.00	W	Output power 1
8	EFFICIENCY1	0.85		0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	OPERATING CONDITION 2					
12	VINDC2	450.00		450.00	V	Input DC voltage 2
13	IOUT2	5.00		5.00	A	Output current 2
14	POUT2			70.00	W	Output power 2
15	EFFICIENCY2	0.85		0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	PRIMARY CONTROLLER SELECTION					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSO _N _25DEG			0.62	Ω	Primary switch on-time resistance at 25 °C
76	RDSO _N _125DEG			1.10	Ω	Primary switch on-time resistance at 125 °C
77	ILIMIT_MIN			1.981	A	Primary switch minimum current limit
78	ILIMIT_TYP			2.130	A	Primary switch typical current limit
79	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.44	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			602	V	Peak drain voltage on the primary switch during turn-off
85	WORST CASE ELECTRICAL PARAMETERS					
86	FSWITCHING_MAX	60000		60000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	147.0		147.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			0.995		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			CCM		Mode of operation



90	DUTYCYCLE			0.437		Primary switch duty cycle
91	TIME_ON_MIN			3.22	μs	Minimum primary switch on-time
92	TIME_ON_MAX		Info	8.69	μs	Maximum primary switch on-time is greater than 11.75 μs: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			9.45	μs	Primary switch off-time
94	LPRIMARY_MIN			737.8	μH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			776.6	μH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			815.4	μH	Maximum primary magnetizing inductance
99 PRIMARY CURRENT						
100	IAVG_PRIMARY			0.402	A	Primary switch average current
101	IPEAK_PRIMARY			2.053	A	Primary switch peak current
102	IPEDestal_PRIMARY			0.009	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			2.053	A	Primary switch ripple current
104	IRMS_PRIMARY			0.742	A	Primary switch RMS current
108 TRANSFORMER CONSTRUCTION PARAMETERS						
109 CORE SELECTION						
110	CORE	PQ26		PQ26		Core selection
111	CORE NAME			PQ26/20-PC95		
112	AE			121.0	mm ²	Core cross sectional area
113	LE			45.0	mm	Core magnetic path length
114	AL			5530	nH	Ungapped core effective inductance per turns squared
115	VE			5470	mm ³	Core volume
116	BOBBIN NAME			PQ26/20 - 2 (P6-S6)		Bobbin name
117	AW			31.1	mm ²	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			9.00	mm	Bobbin width
119	BH			4.78	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122 PRIMARY WINDING						
123	NPRIMARY			42		Primary winding number of turns
124	BPEAK			3743	Gauss	Peak flux density
125	BMAX			3243	Gauss	Maximum flux density
126	BAC			1621	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			440	nH	Typical gapped core effective inductance per turns squared
128	LG			0.318	mm	Core gap length
130 SECONDARY WINDING						
131	NSECONDARY	4		4		Secondary winding number of turns
133 BIAS WINDING						
134	NBIAS			3		Bias winding number of turns

138	PRIMARY COMPONENTS SELECTION					
161	BIAS WINDING					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			39.36	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	μF	Bias winding rectification capacitor
166	CBPP			4.70	μF	BPP pin capacitor
170	SECONDARY COMPONENTS SELECTION					
171	FEEDBACK COMPONENTS					
172	RFB_UPPER ⁹			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			10.00	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	MULTIPLE OUTPUT PARAMETERS					
179	OUTPUT 1					
180	VOU1			14.00	V	Output 1 voltage
181	IOUT1			5.000	A	Output 1 current
182	POU1			70.00	W	Output 1 power
183	IRMS_SECONDARY1			8.843	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			7.293	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			4		Number of turns for output 1
186	VREVERSE_RECTIFIER1			54.48	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT15H017LPS-13		DMT15H017LPS-13		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25 degC and VGS = 4.4 V for output 1
218	PO_TOTAL			70.00	W	Total power of all outputs

Table 7 – DER-1035Q PIXIs Spreadsheet.

⁹ Actual value implemented on the unit is 110 kΩ as requirement for implementing the *Precision Voltage Regulator* circuit.

9 Performance data

Note: 1. Measurements were taken with the unit under test positioned inside a thermal chamber which was placed inside a high-voltage (HV) room.



Figure 16 – Set-up for High-Voltage Test.



Figure 17 – Set-up for Test Inside the High-Voltage Room.

2. The DER-1035Q board was placed inside a box within the thermal chamber to eliminate the effects of any airflows.



Figure 18 – Unit Under Test Placed Inside a Box to Eliminate the Effect of Airflow.

3. The DER board was allowed to settle for 5 minutes at full load at the start of every test sequence. The test board was allowed to stabilize for at least 1 minute at each load condition before measurements were taken.

4. List of Equipment Used for Testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	62024P-600-8	600 V / 8 A / 2400 W DC PSU	Chroma
Electronic Load	DL3021	150 V / 40 A / 200 W DC ELOAD	Rigol
Electronic Load	PEL-2020A	80 V / 20 A / 100 W DC ELOAD	GW Instek
Power Meter	66205	600 V / 30 A 10 kHz Digital Meter	Chroma
Power Meter	WT310E	600 V/20 A 100 kHz Digital Meter	Yokogawa
Current Meter	DMM-4050	Precision Multimeter	Tektronix
High Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Output Current Measurement	701928	100 MHz 30 A _{rms} Current Probe	Yokogawa
Component Current Measurement	CWTUM/015/B	30 MHz 30 A _{peak} Rogowski Coil	CWT
Component Current Measurement	CWTUM/06/R	30 MHz 120 A _{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20 channel Data Logger	Graphtec
Thermal Image	TiX580	1000 °C Thermal Imager Camera	Fluke
Oscilloscope	DLM5058	2.5GS/s 500 MHz Mixed Signal	Yokogawa
Power Supply	62024P-600-8	600 V / 8 A / 2400 W DC PSU	Chroma

Table 8 – List of Equipment Used for Testing.

9.1 No-Load Input Power

Figure 19 shows the schematic for no-load input power measurement. The voltmeter was placed before the ammeter; this was done to prevent the voltmeter bias current from affecting the input current measurement. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

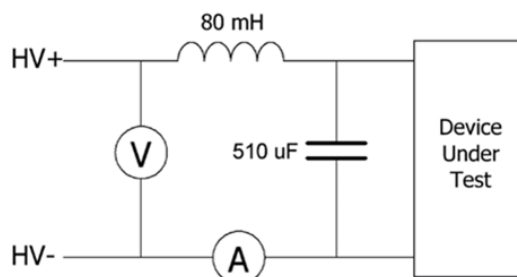


Figure 19 – No-Load Input Power Measurement Diagram.

The unit was allowed to stabilize for ten minutes for each test before measurements were started. The leakage current through the DC-Link capacitor was measured before testing and subtracted from the no-load input current measurement. The average voltage across the inductor was assumed to be negligible due to the inductor's very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible since the input current was DC.

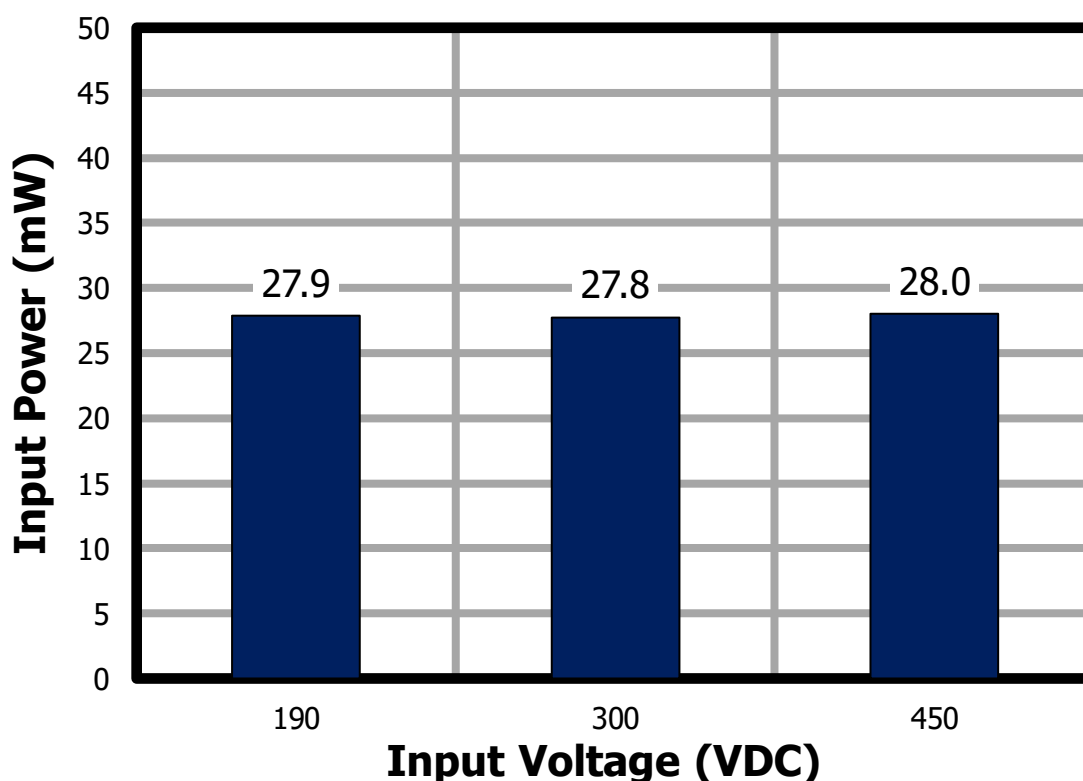


Figure 20 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Efficiency Across Line

Efficiency across line describes how the input voltage change affects the unit's overall efficiency. The points in the graph were taken at 100% load conditions.

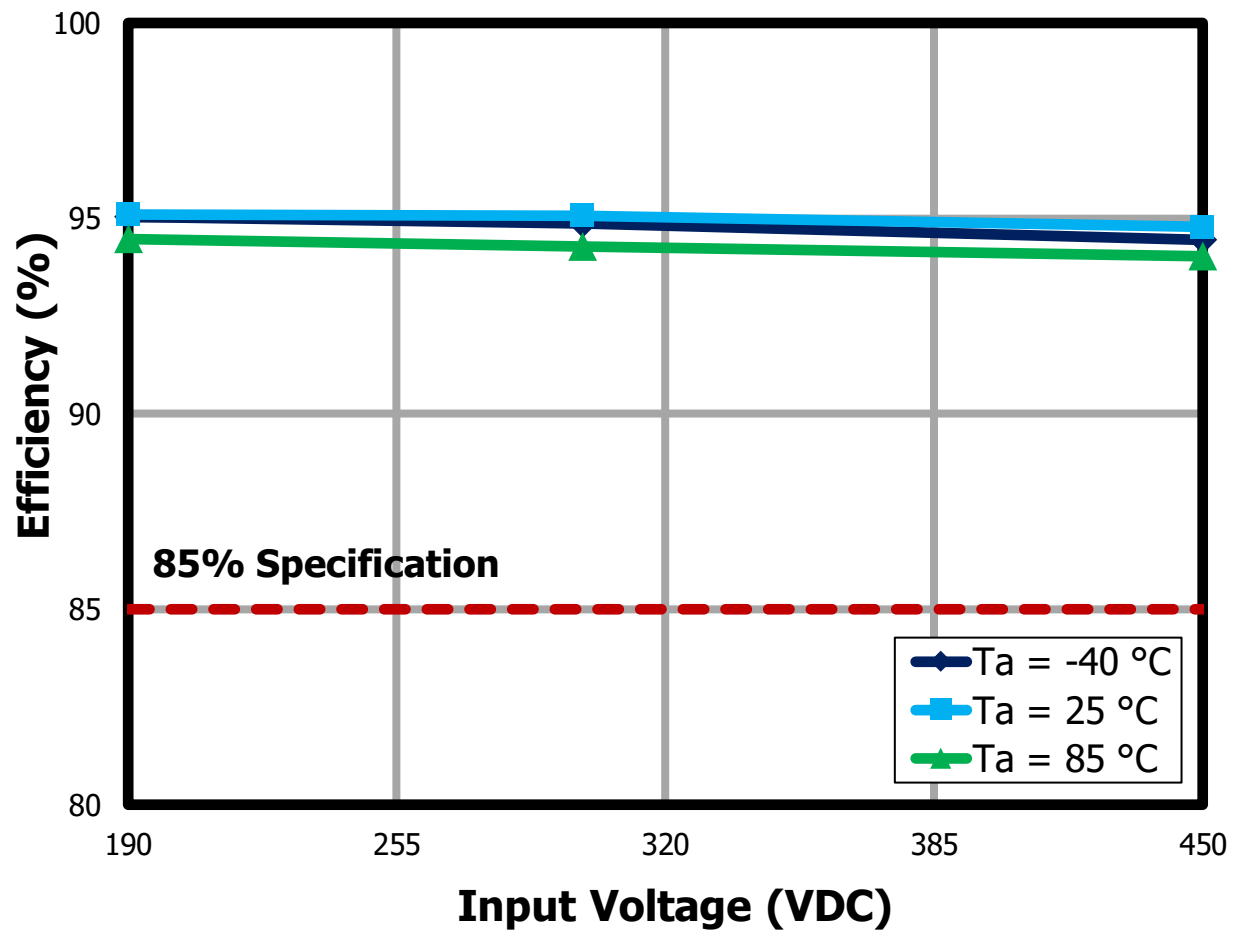


Figure 21 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Efficiency Across Load

This test describes how the change in output loading affects overall efficiency.

9.2.2.1 Efficiency Across Load at 85 °C

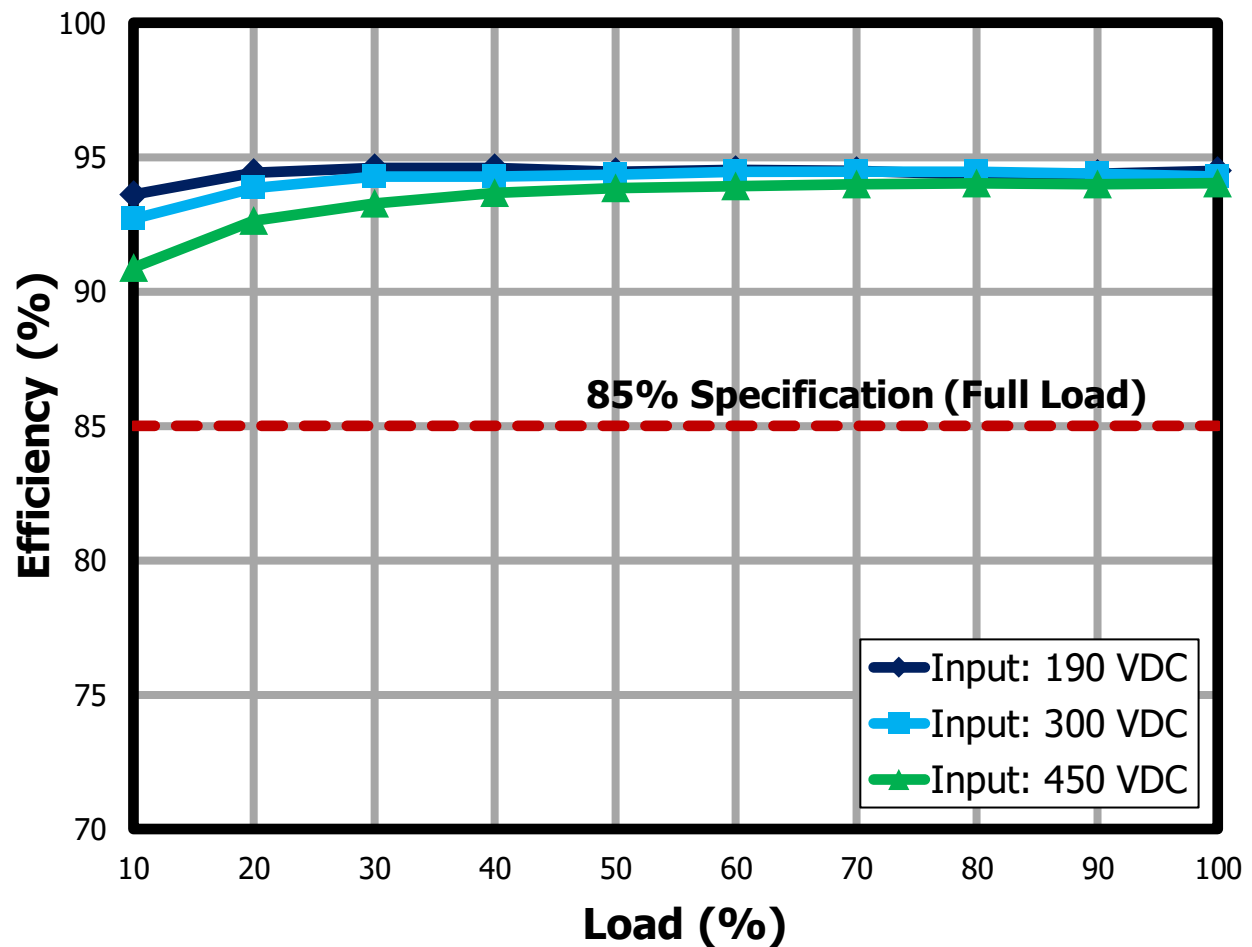


Figure 22 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

9.2.2.2 Efficiency Across Load at -40 °C

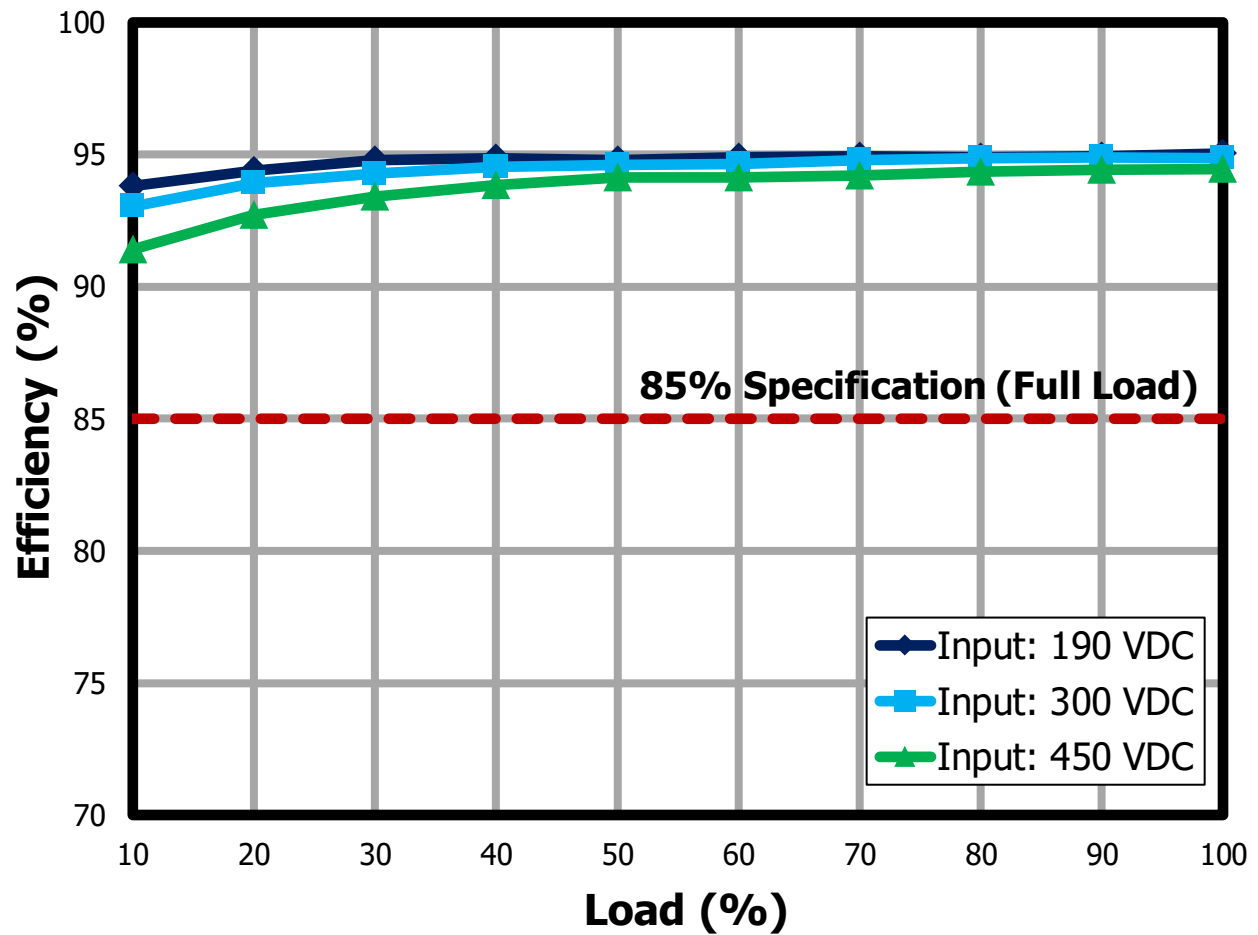


Figure 23 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.2.2.3 Efficiency Across Load at 25 °C

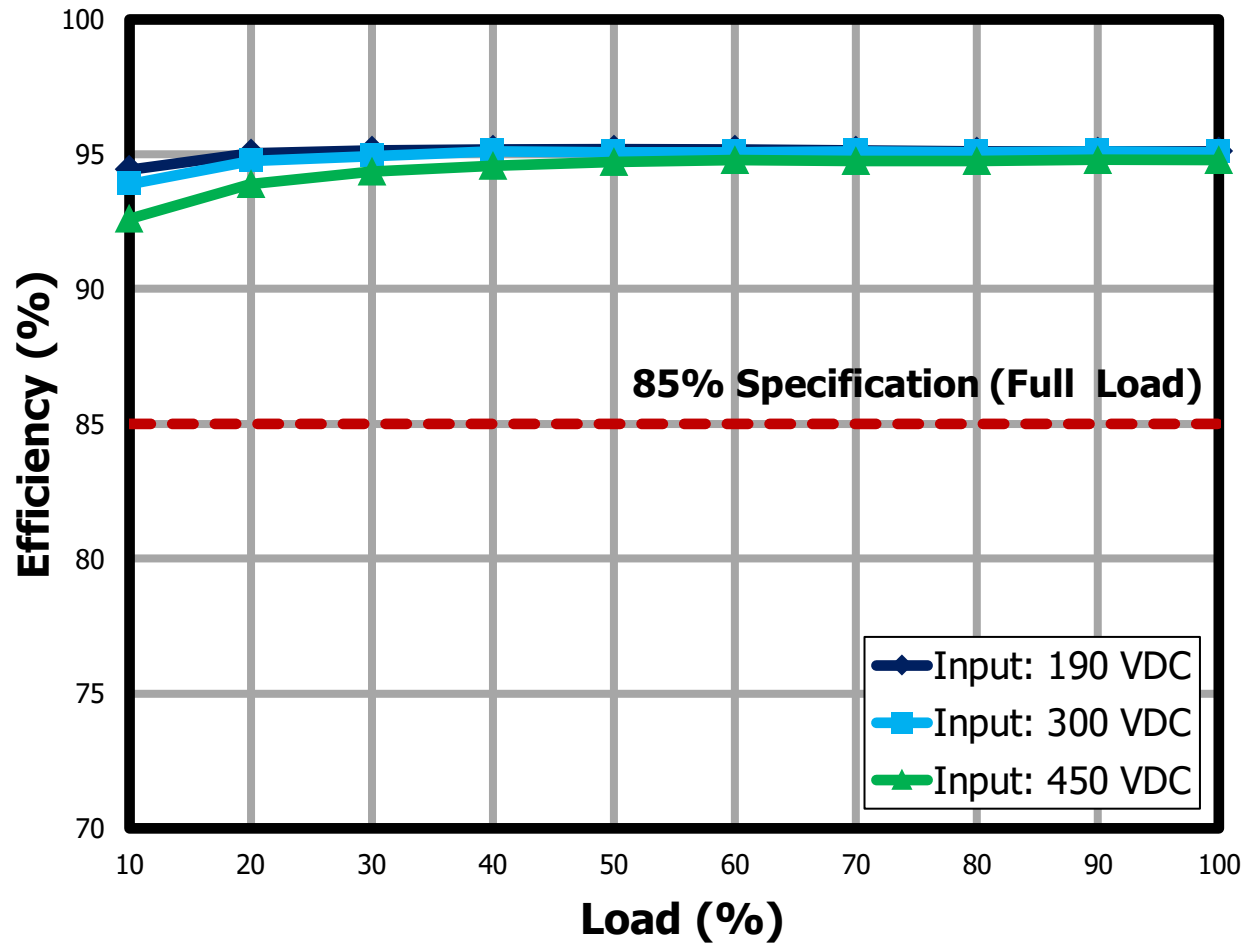


Figure 24 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.3 Line and Load Regulation

9.3.1 Load Regulation

Load regulation describes how the change in output load affects the output voltage of the unit.

9.3.1.1 Load Regulation at 85 °C

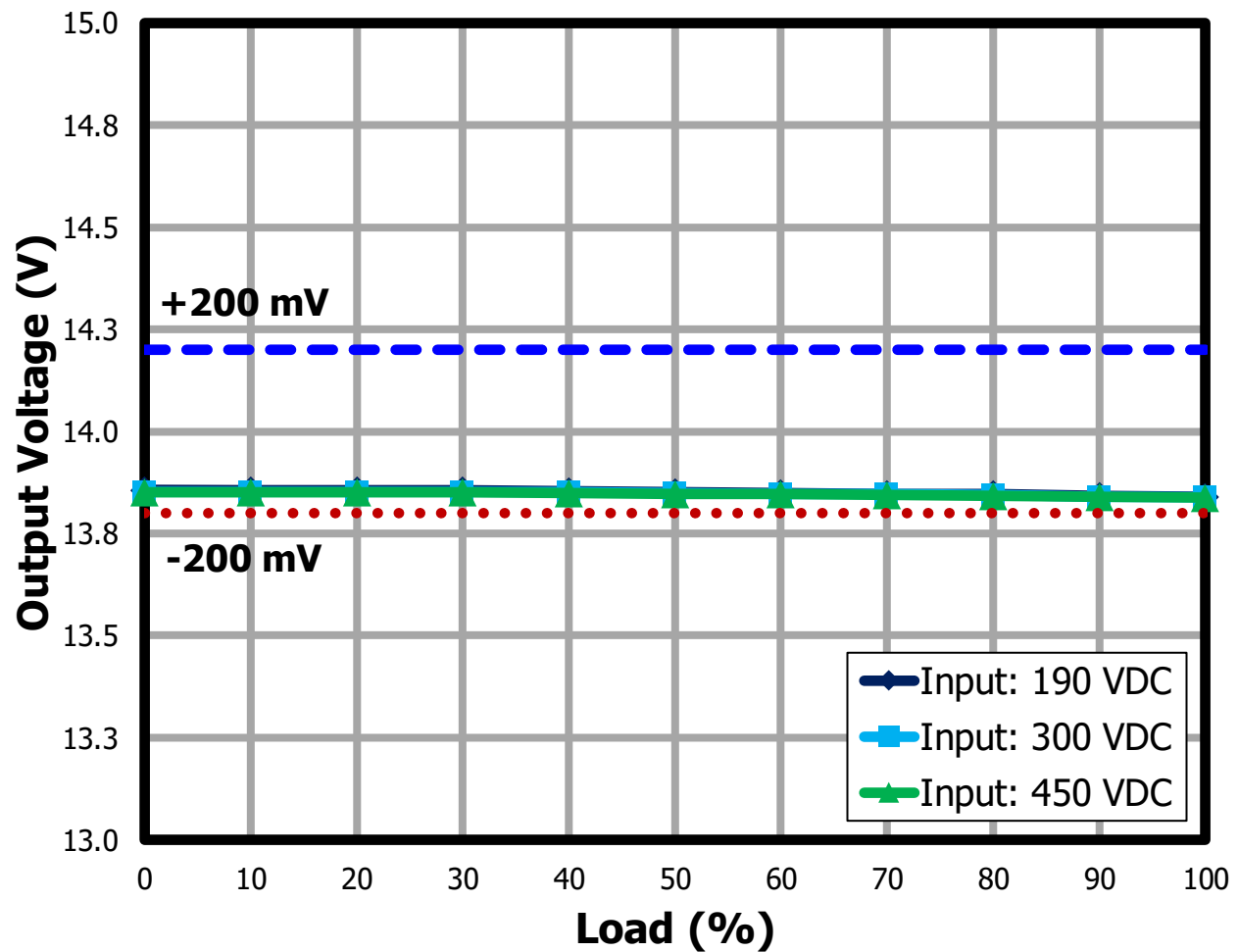
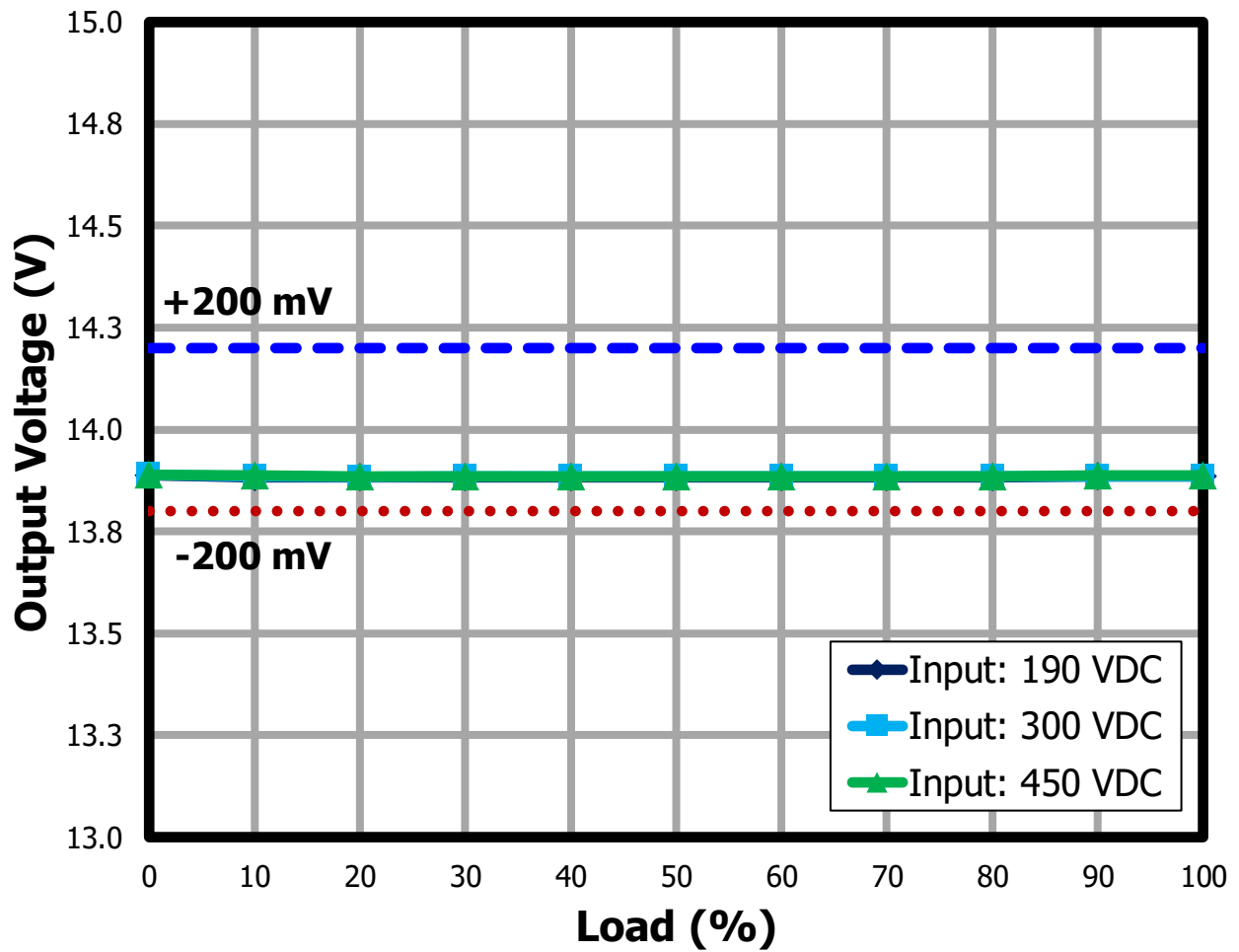


Figure 25 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at -40 °C**Figure 26** – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.1.3 Load Regulation at 25 °C

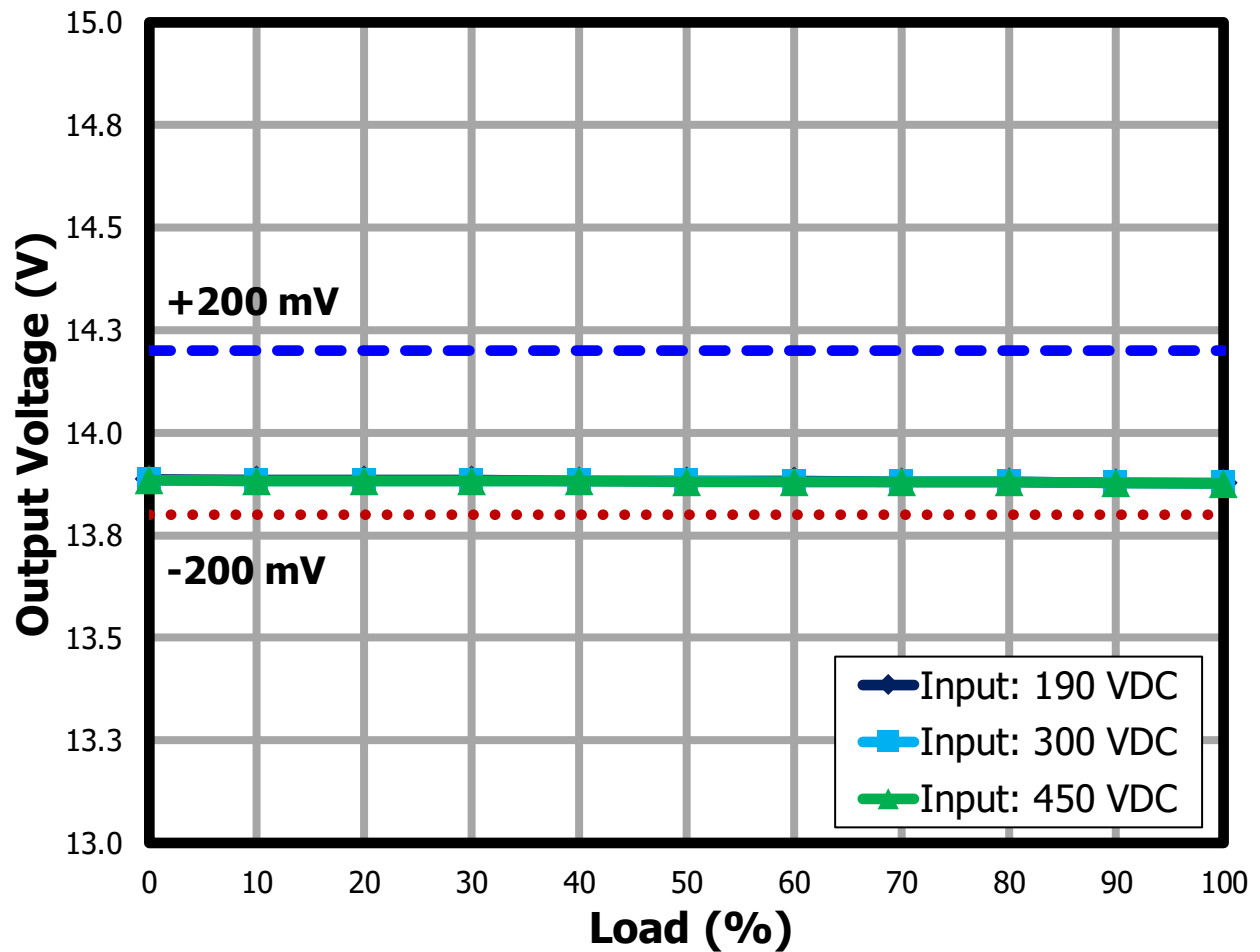


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.2 Line Regulation

Line regulation describes how the change in input voltage affects the average output voltage of the unit. The points in the following graph were taken at 100% load.

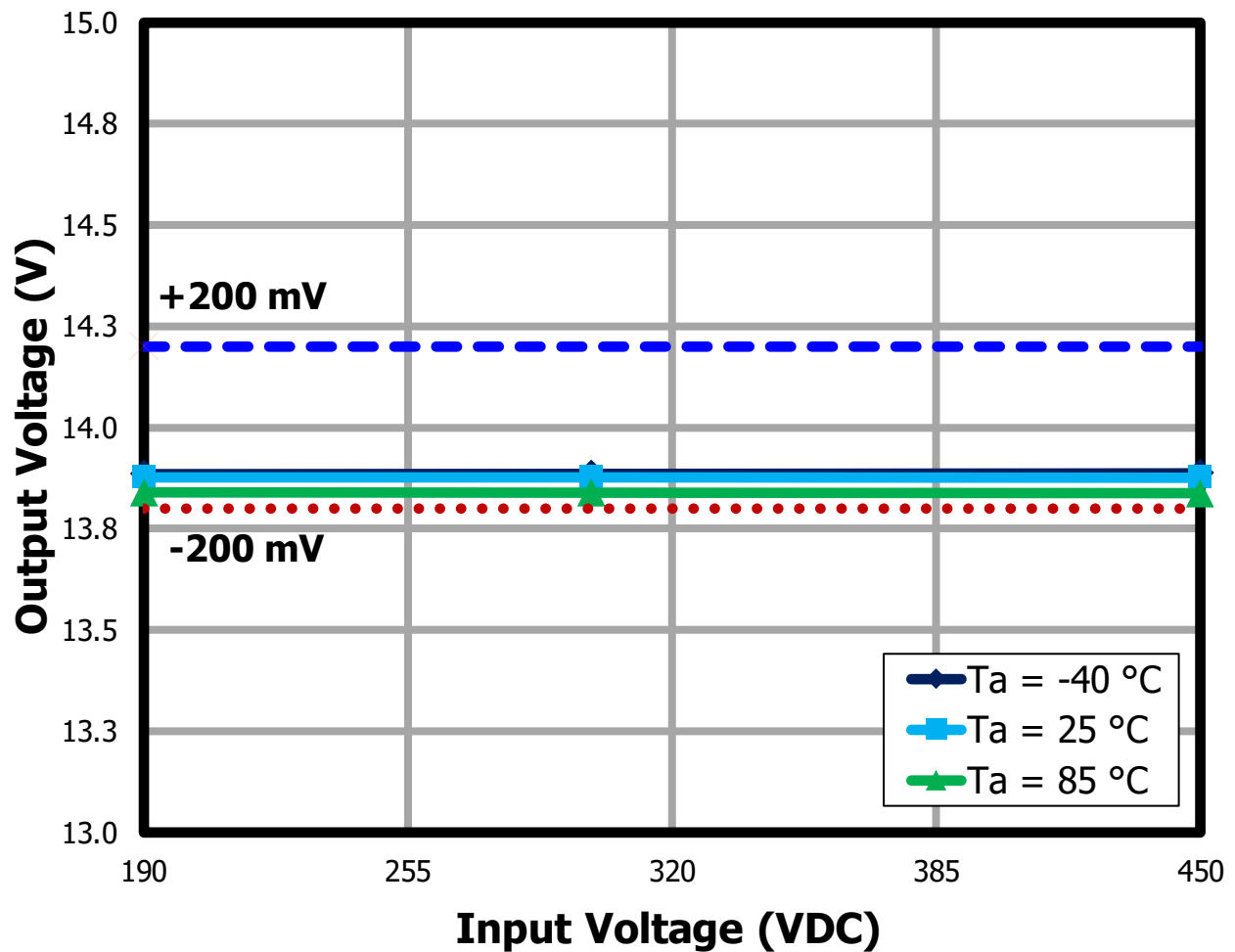


Figure 28 – Output Voltage vs Input Voltage at Full Load.

10 Thermal Performance

10.1 Thermal Data at 85 °C

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 18 shows the test set-up for thermal measurement.

Critical Components	Temperature (°C)		
	190 VDC	300 VDC	450 VDC
InnoSwitch3- AQ (IC200)	117	110	112
Primary Snubber Resistor (R204)	100	96.6	99.4
Primary Snubber Diode (D201)	103	100	102
Transformer Core	113	111	113
Transformer Winding	117	106	114
Output Capacitor (C106)	113	109	110
Synchronous Rectifier MOSFET (Q102)	124	118	120
Secondary Snubber Resistor (R106)	125	120	109
Output Current Sense Resistor (R110A)	112	106	109

Table 9 – Thermal Data at 85 °C at Different Input Voltages (VDC).

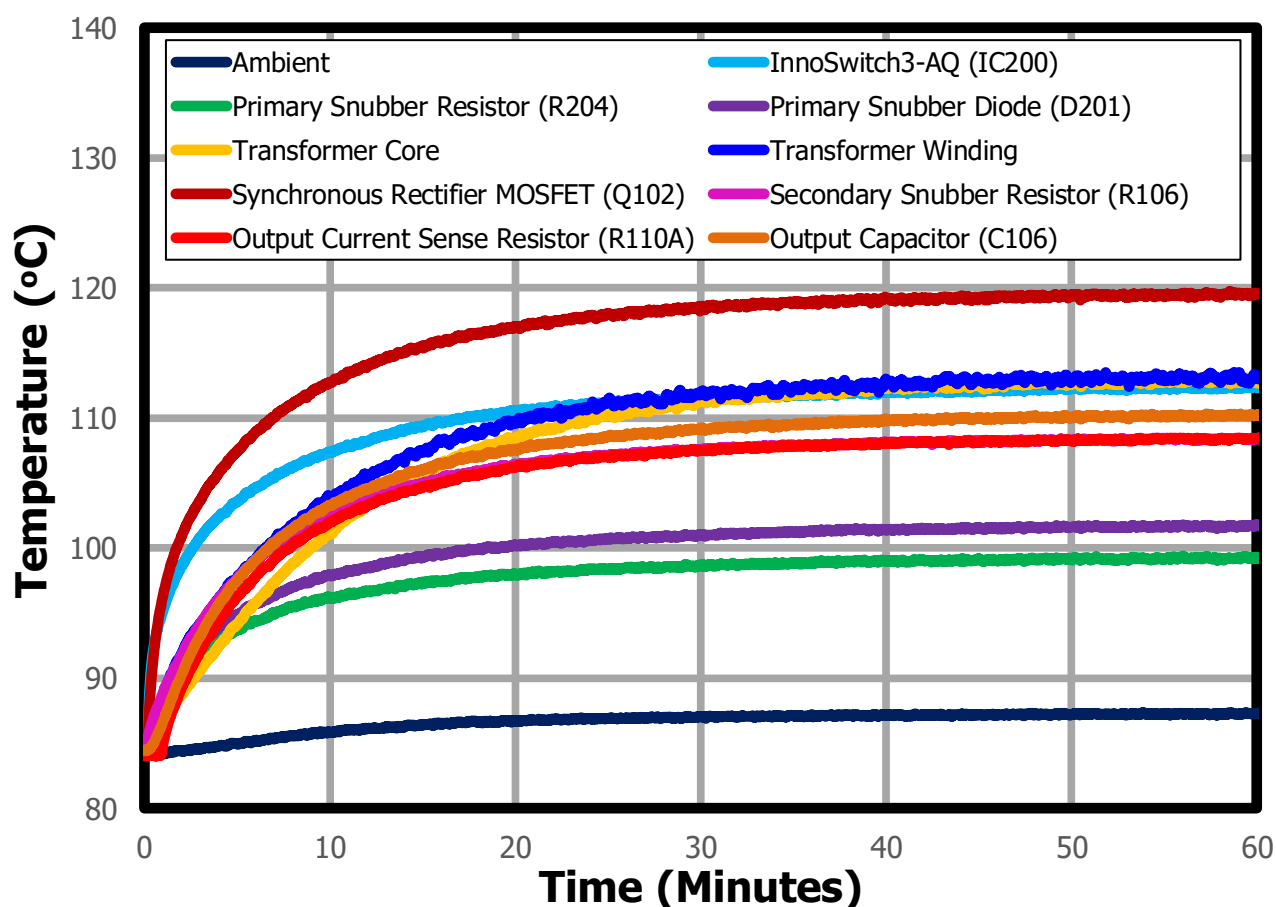


Figure 29 – Component Temperatures at 85 °C Ambient, 450 VDC Input.

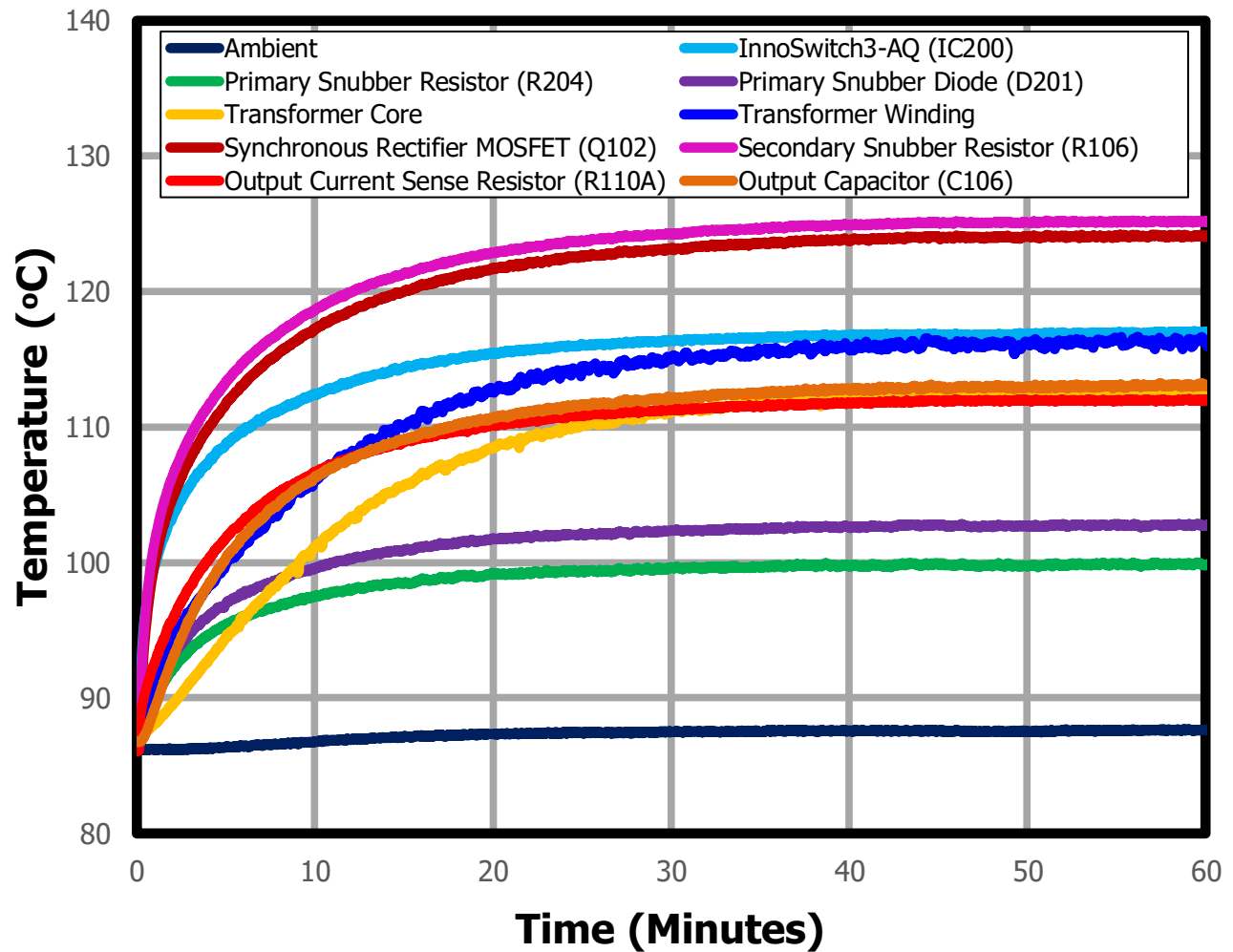


Figure 30 – Component Temperatures at 85 °C Ambient, 190 VDC Input.

10.2 Thermal Image Data at 25 °C

The following thermal scans were captured using a Fluke thermal imager after soaking for 1 hour. The set-up was placed inside an enclosure to minimize the effect of airflow.

Critical Components	Temperature (°C)		
	190 VDC	300 VDC	450 VDC
InnoSwitch3- AQ (IC200)	55.1	51.1	59.1
Primary Snubber Resistor (R204)	36.7	39.4	38.1
Primary Snubber Diode (D201)	41.0	40.8	42.4
Transformer Core	54.4	56.1	56.6
Transformer Winding	60.3	61.9	62.5
Output Capacitor (C106)	48.6	50.6	50.8
Synchronous Rectifier MOSFET (Q102)	54.5	57.4	58.5
Secondary Snubber Resistor (R106)	52.3	57.9	62.4
Output Current Sense Resistor (R110A)	49.6	51.0	49.9

Table 10 – Thermal Data at 25 °C at Different Input Voltages (VDC).

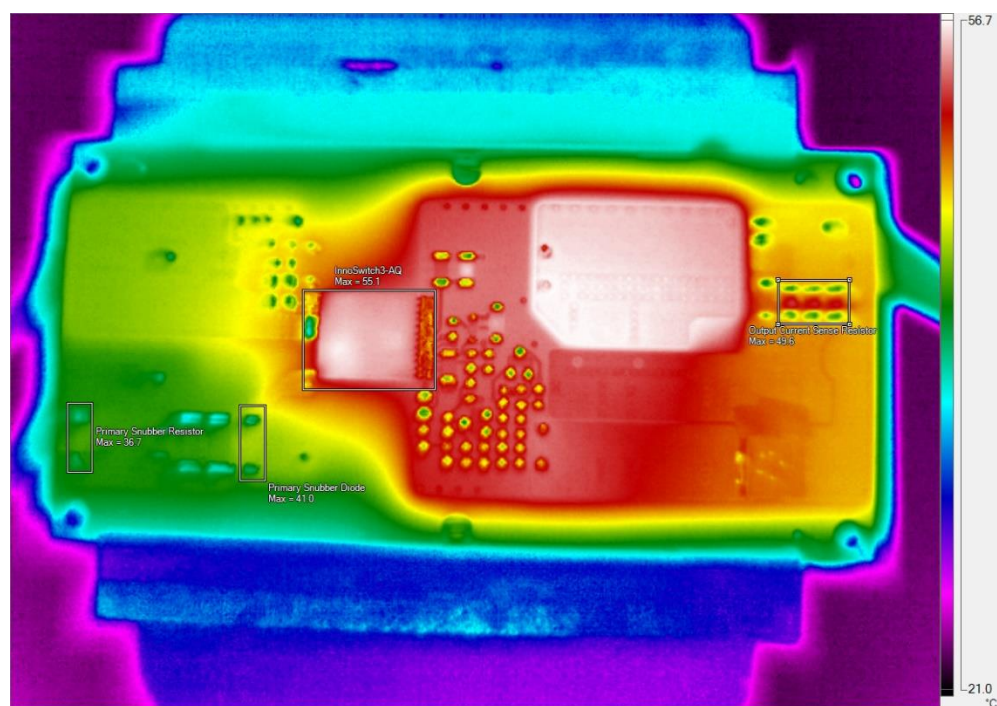


Figure 31 –Thermal Scan of the Bottom of the PCB at 190 VDC Input.

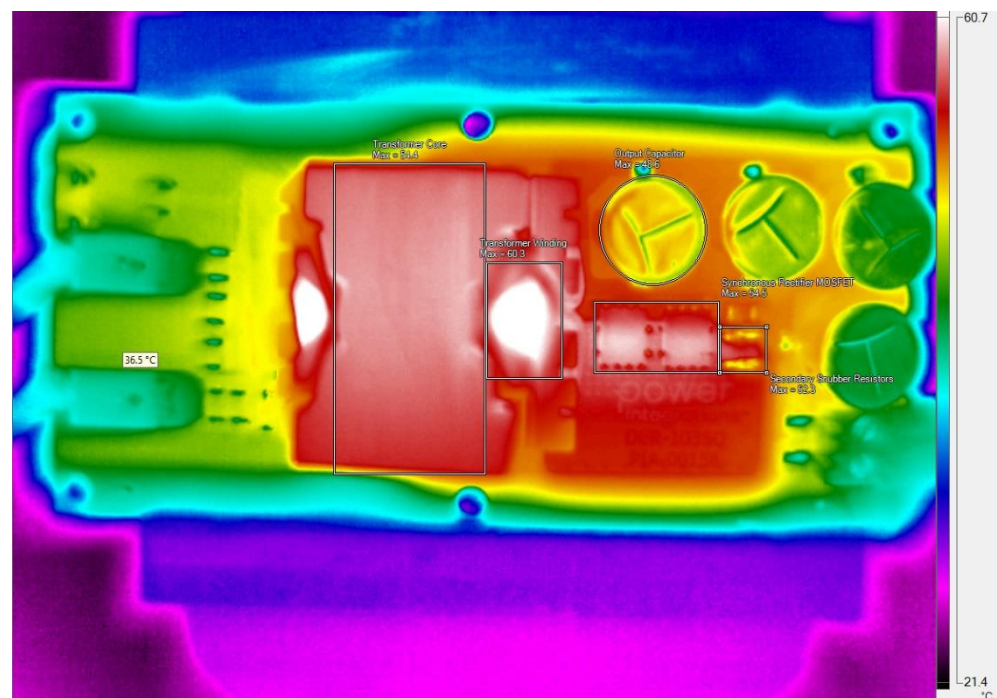


Figure 32 –Thermal Scan of the Top of the PCB at 190 VDC Input.

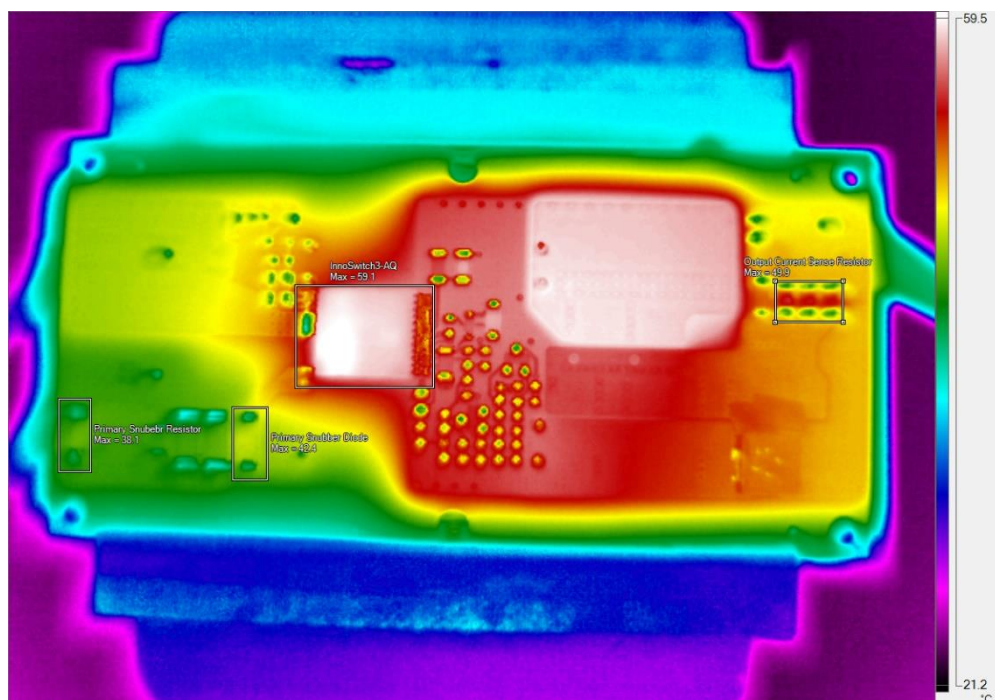


Figure 33 –Thermal Scan of the Bottom of the PCB at 450 VDC Input.

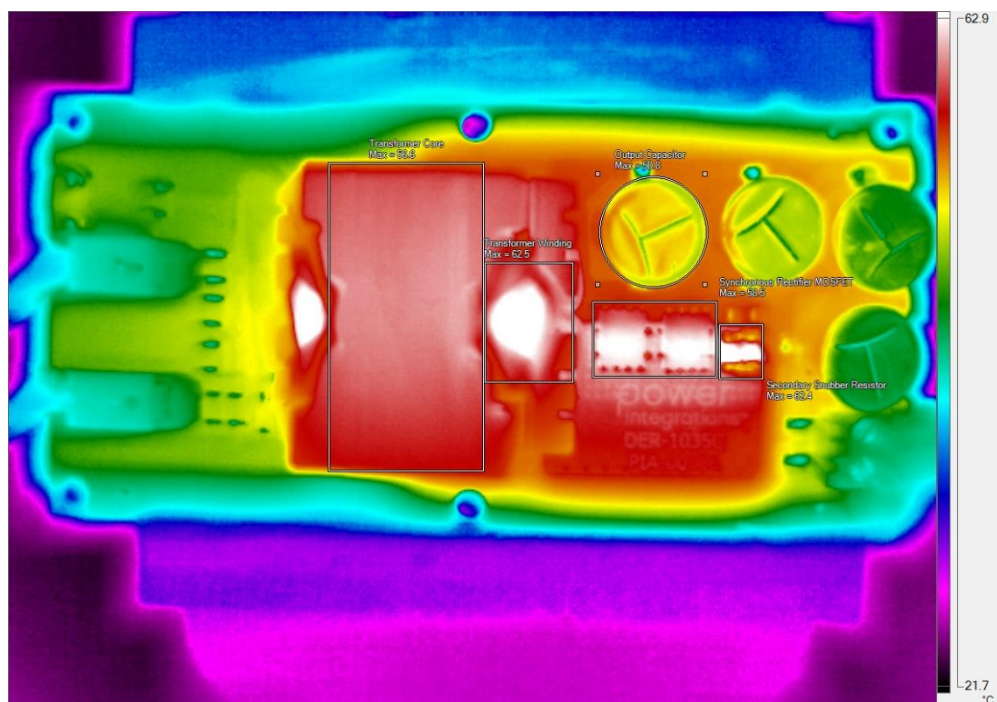


Figure 34 –Thermal Scan of the Top of the PCB at 450 VDC Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit under test to a fully charged DC link capacitor¹⁰ at different test input voltages. An electronic load configured for constant resistance was used for all start-up tests.

11.1.1 Output Voltage and Current at 85 °C^{11,12}

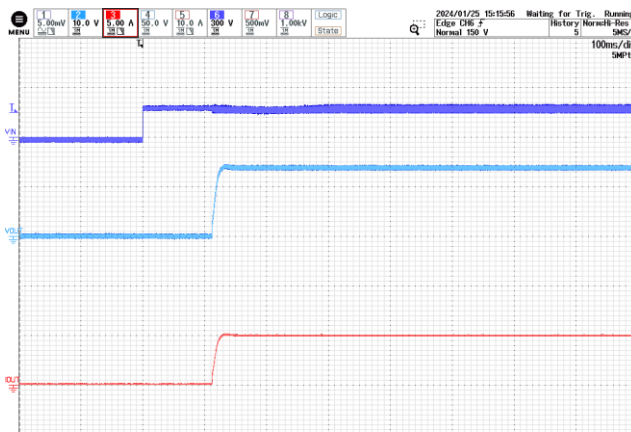


Figure 35 – Output Voltage and Current.
190 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

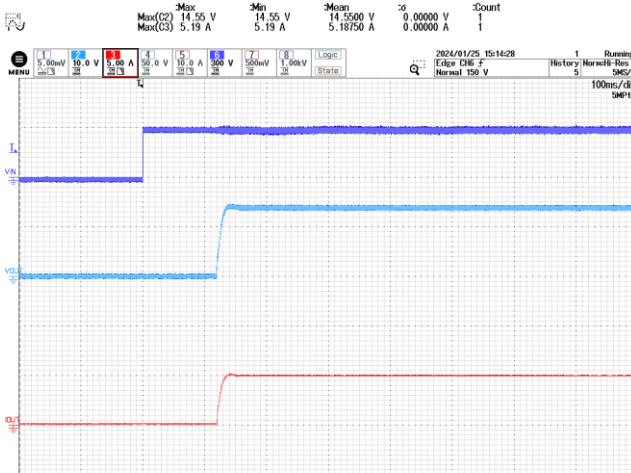


Figure 36 – Output Voltage and Current.
300 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

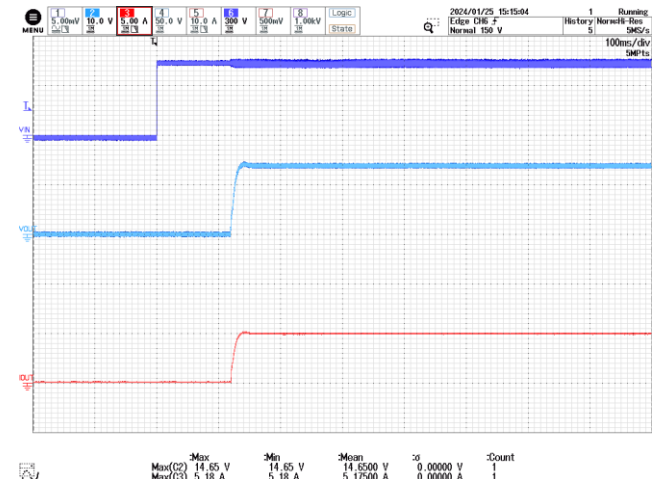


Figure 37 – Output Voltage and Current.
450 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

¹⁰ Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.

¹¹ Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

¹² Current waveforms were measured using a Yokogawa current probe

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C^{13,14}



Figure 38 – INN3949CQ Drain Voltage and Current.
190 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 500 V / div.
CH3: I_{OUT} , 2 A / div.
Time: 20 ms / div.

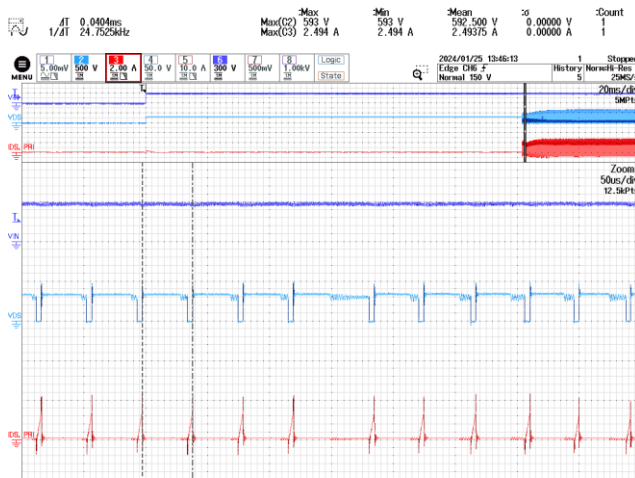


Figure 39 – INN3949CQ Drain Voltage and Current.
300 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 500 V / div.
CH3: I_{OUT} , 2 A / div.
Time: 20 ms / div.

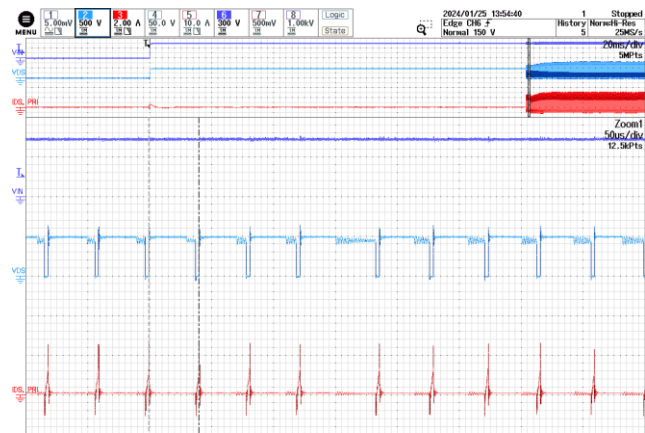


Figure 40 – INN3949CQ Drain Voltage and Current.
450 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 500 V / div.
CH3: I_{OUT} , 2 A / div.
Time: 20 ms / div.

¹³ The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the additional t_{AR} delay of InnoSwitch3.

¹⁴ Current waveforms were measured using a 30 A rogowski current probe.

11.1.3 SR FET Drain Voltage and Current at 85 °C^{15,16}

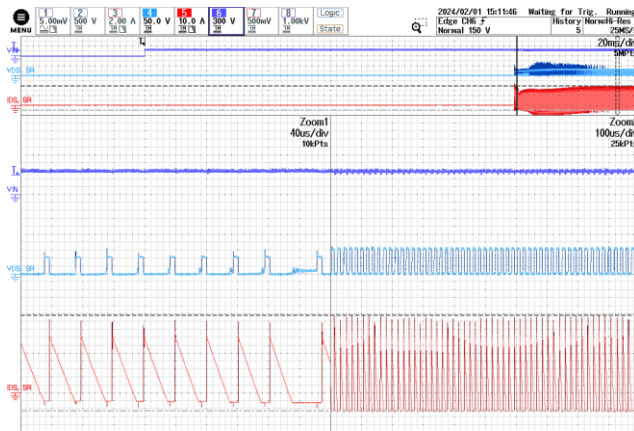


Figure 41 – SR FET Drain Voltage and Current.
190 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH4: V_{OUT} , 50 V / div.
CH5: I_{OUT} , 10 A / div.
Time: 20 ms / div.

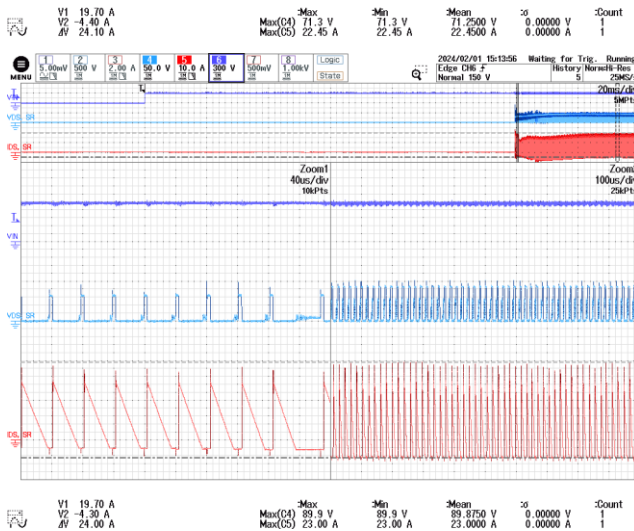


Figure 42 – SR FET Drain Voltage and Current.
300 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH4: V_{OUT} , 50 V / div.
CH5: I_{OUT} , 10 A / div.
Time: 20 ms / div.

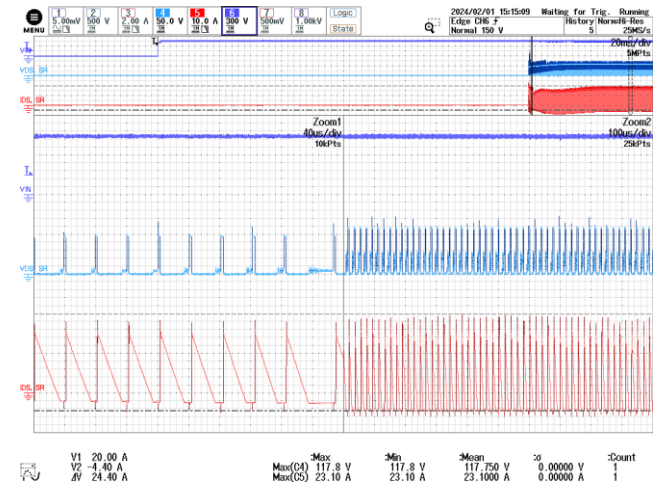


Figure 43 – SR FET Drain Voltage and Current.
450 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH4: V_{OUT} , 50 V / div.
CH5: I_{OUT} , 10 A / div.
Time: 20 ms / div.

¹⁵ The time between when V_{IN} turned on and the SR FET starts switching was due to the additional t_{AR} delay of InnoSwitch3.

¹⁶ Current waveforms were measured using a 120 A Rogowski current probe.

11.1.4 Output Voltage and Current at -40 °C^{17,18}

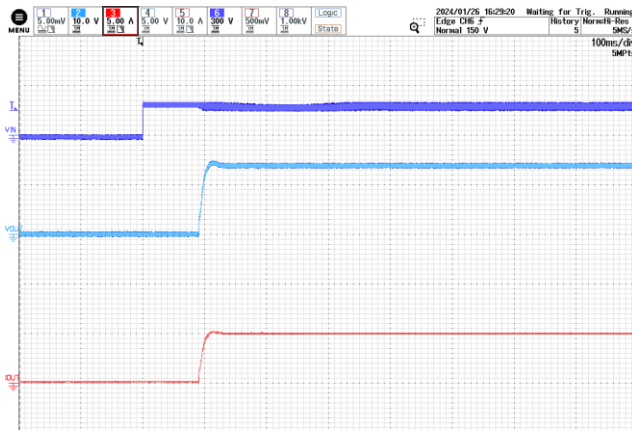


Figure 44 – Output Voltage and Current.

190 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

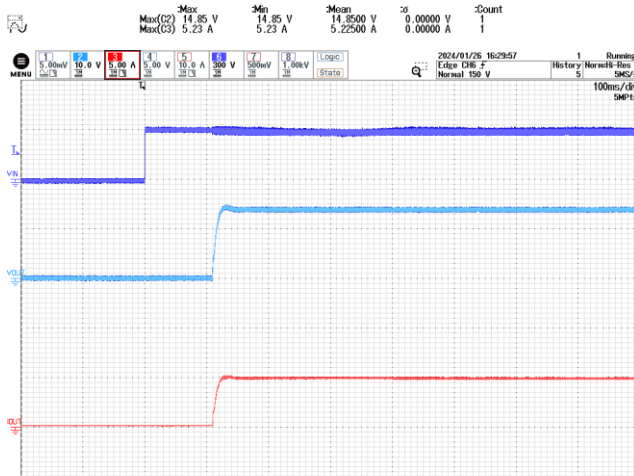


Figure 45 – Output Voltage and Current.

300 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

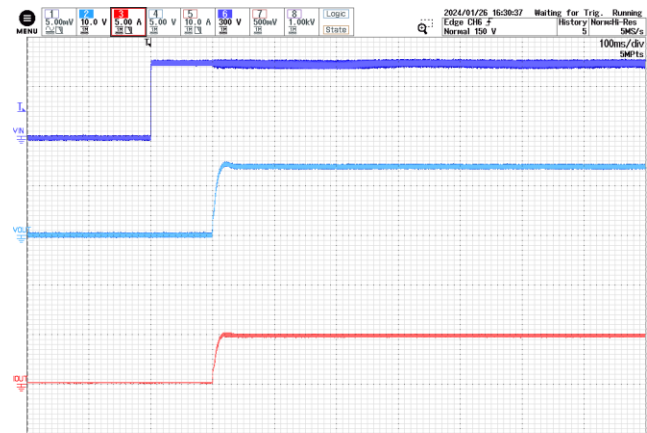


Figure 46 – Output Voltage and Current.

450 VDC, 2.8 Ω Load.

CH6: V_{IN} , 300 V / div.

CH2: V_{OUT} , 10 V / div.

CH3: I_{OUT} , 5 A / div.

Time: 100 ms / div.

¹⁷ Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

¹⁸ Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C^{19,20}

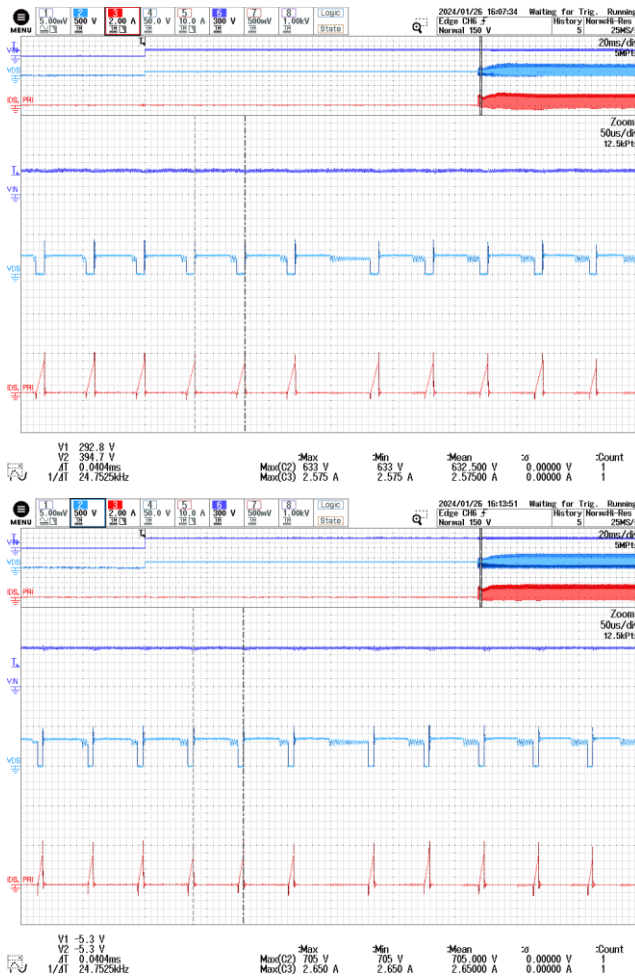


Figure 48 – INN3949CQ Drain Voltage and Current.
300 VDC, 2.8 Ω Load.
CH6: VIN, 300 V / div.
CH2: VOUT, 500 V / div.
CH3: IOUT, 2 A / div.
Time: 100 ms / div.

Figure 47 – INN3949CQ Drain Voltage and Current.
190 VDC, 2.8 Ω Load.
CH6: VIN, 300 V / div.
CH2: VOUT, 500 V / div.
CH3: IOUT, 2 A / div.
Time: 100 ms / div.

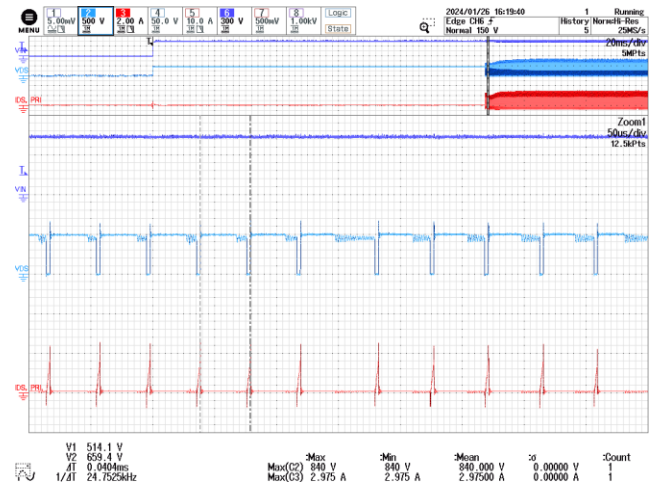


Figure 49 – INN3949CQ Drain Voltage and Current.
450 VDC, 2.8 Ω Load.
CH6: VIN, 300 V / div.
CH2: VOUT, 500 V / div.
CH3: IOUT, 2 A / div.
Time: 100 ms / div.

¹⁹ The time between when VIN turned on and the InnoSwitch3 starts switching was due to the additional t_{AR} delay of InnoSwitch3.

²⁰ Current waveforms were measured using a 30 A Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at -40 °C^{21,22}

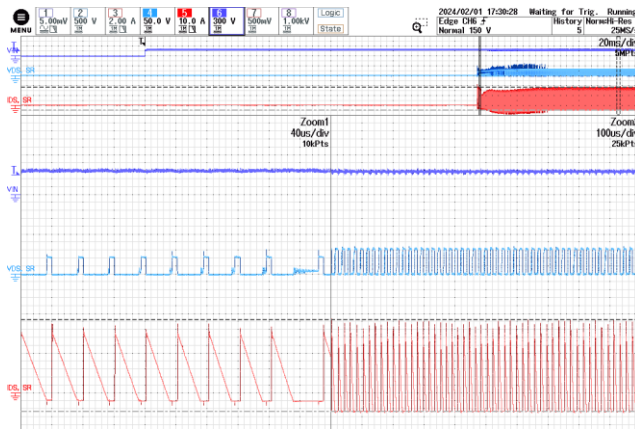


Figure 50 – SR FET Drain Voltage and Current.
190 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 50 V / div.
CH3: I_{OUT} , 10 A / div.
Time: 100 ms / div.

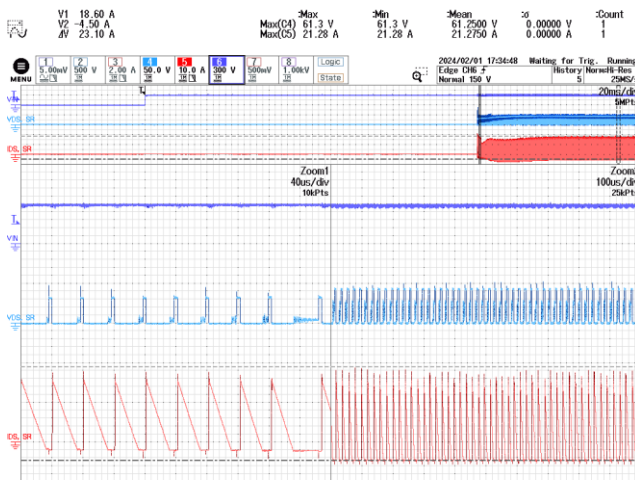


Figure 51 – SR FET Drain Voltage and Current.
300 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 50 V / div.
CH3: I_{OUT} , 10 A / div.
Time: 100 ms / div.

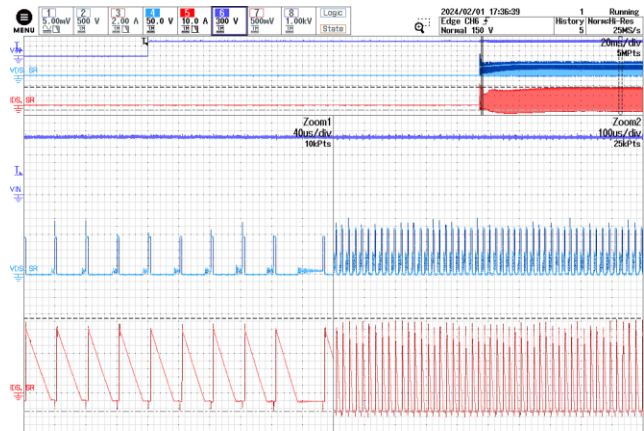


Figure 52 – SR FET Drain Voltage and Current.
450 VDC, 2.8 Ω Load.
CH6: V_{IN} , 300 V / div.
CH2: V_{OUT} , 50 V / div.
CH3: I_{OUT} , 10 A / div.
Time: 100 ms / div.

²¹ The time between when V_{IN} turned on and the SR FET starts switching was due to the additional t_{AR} delay of InnoSwitch3.

²² Current waveforms were measured using a 120 A Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C

11.2.1.1 Normal Operation Component Stress

Input	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
	INN3949CQ			SR FETs		
V_{IN} (VDC)	$I_D(A_{PK})$	$V_{DS}(V_{PK})$	V_{STRESS} (%)	$I_D(A_{PK})^{23}$	$V_{DS}(V_{PK})^{24}$	V_{STRESS} (%)
190	1.60	553	52.5	23.5	54.4	36.3
300	1.53	668	39.3	24.1	54.9	36.6
450	1.43	819	48.2	24.3	75.1	50.0

Table 11 – Summary of Critical Component Voltage Stresses at 85 °C Ambient.

²³ SR FET current is the sum of Q100 and Q101 currents.

²⁴ SR FET voltage was taken from Q101.

11.2.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C²⁵

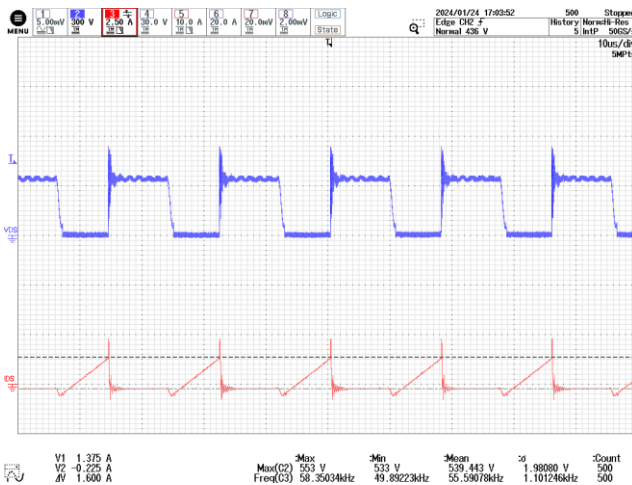


Figure 53 – INN3949CQ Drain Voltage and Current.
190 VDC, 5 A Load.
CH2: $V_{DS, INNO}$, 300 V / div.
CH3: $I_{DS, INNO}$, 2.5 A / div.
Time: 10 μ s / div.

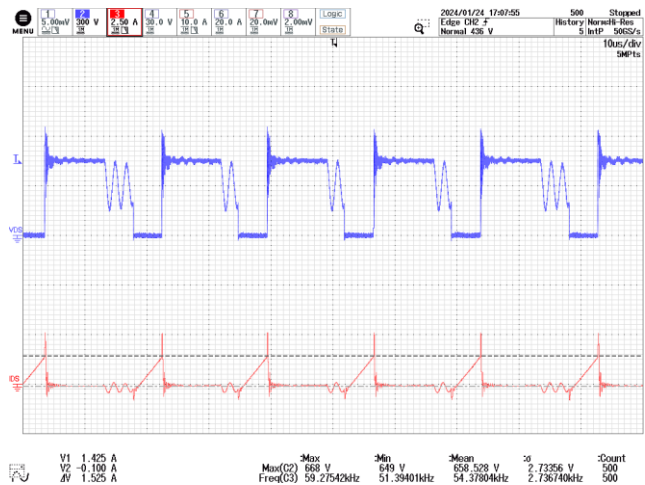


Figure 54 – INN3949CQ Drain Voltage and Current.
300 VDC, 5 A Load.
CH2: $V_{DS, INNO}$, 300 V / div.
CH3: $I_{DS, INNO}$, 2.5 A / div.
Time: 10 μ s / div.



Figure 55 – INN3949CQ Drain Voltage and Current.
450 VDC, 5 A Load.
CH2: $V_{DS, INNO}$, 300 V / div.
CH3: $I_{DS, INNO}$, 2.5 A / div.
Time: 10 μ s / div.

²⁵ Current was measured using a 30 A Rogowski probe

11.2.1.3 SR FET Drain Voltage and Current at 85 °C²⁶

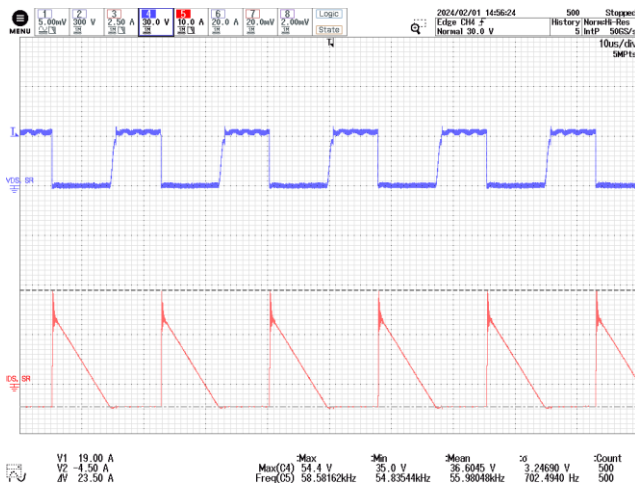


Figure 56 – SR FET Drain Voltage and Current.
190 VDC, 5 A Load.
CH4: $V_{DS, INNO}$, 50 V / div.
CH5: $I_{DS, INNO}$, 10 A / div.
Time: 10 μ s / div.

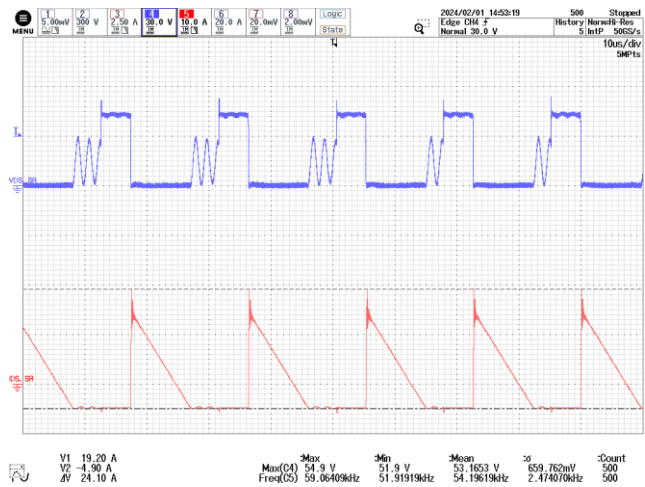


Figure 57 – SR FET Drain Voltage and Current.
300 VDC, 5 A Load.
CH4: $V_{DS, INNO}$, 50 V / div.
CH5: $I_{DS, INNO}$, 10 A / div.
Time: 10 μ s / div.

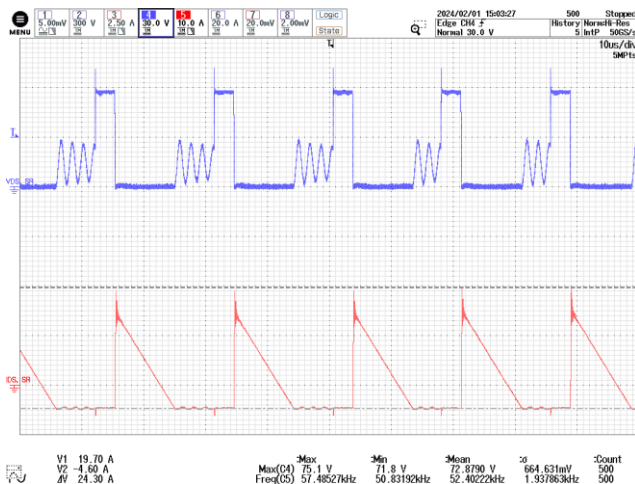


Figure 58 – SR FET Drain Voltage and Current.
450 VDC, 5 A Load.
CH4: $V_{DS, INNO}$, 50 V / div.
CH5: $I_{DS, INNO}$, 10 A / div.
Time: 10 μ s / div.

²⁶ Current was measured using a 120 A Rogowski probe

11.2.1.4 Short-Circuit Response at 85 °C

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to see if the unit could recover and operate normally. The expected response during short-circuit is for the unit to go to auto-restart (AR) mode and attempt recovery every 1.7 to 2.11 seconds. Full load setting was 2.8 Ω constant resistance.

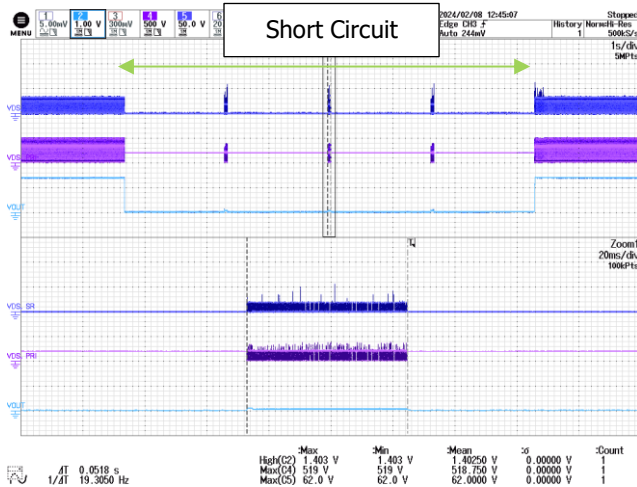


Figure 59 – INN3949CQ and SR FET Drain Voltage.
190 VDC, 2.8 Ω -Short-2.8 Ω .

CH2: V_{OUT}, 10 V / div.

CH4: V_{DS,PRI}, 500 V / div.

CH5: V_{DS,SR}, 50 V / div.

Time: 1 s / div.

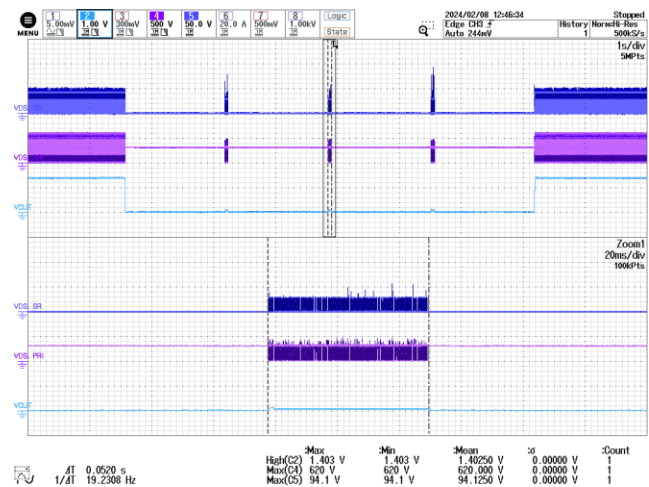


Figure 60 – INN3949CQ and SR FET Drain Voltage.
300 VDC, 2.8 Ω -Short-2.8 Ω .

CH2: V_{OUT}, 10 V / div.

CH4: V_{DS,PRI}, 500 V / div.

CH5: V_{DS,SR}, 50 V / div.

Time: 1 s / div.

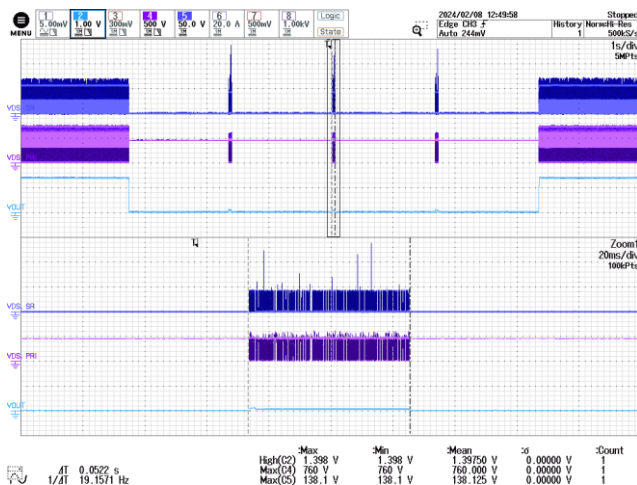


Figure 61 – INN3949CQ and SR FET Drain Voltage.
450 VDC, 2.8 Ω -Short-2.8 Ω .

CH2: V_{OUT}, 10 V / div.

CH4: V_{DS,PRI}, 500 V / div.

CH5: V_{DS,SR}, 50 V / div.

Time: 1 s / div.

11.2.2 Switching Waveforms at -40 °C

11.2.2.1 Normal Operation Component Stress

Input	Steady-State Switching Waveforms -40 °C Ambient, Full Load					
	INN3949CQ			SR FETs		
V_{IN} (VDC)	$I_D(A_{PK})$	$V_{DS}(V_{PK})$	V_{STRESS} (%)	$I_D(A_{PK})^{27}$	$V_{DS}(V_{PK})^{28}$	V_{STRESS} (%)
190	2.58	599	35.2	23.5	37.6	25.0
300	2.75	718	42.2	23.3	54.4	36.3
450	2.93	843	59.6	23.3	74.0	49.3

Table 12 – Summary of Critical Component Voltage Stresses at -40 °C Ambient.

²⁷ SR FET current is the sum of Q100 and Q101 currents.

²⁸ SR FET voltage was taken from Q101.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at -40 °C²⁹

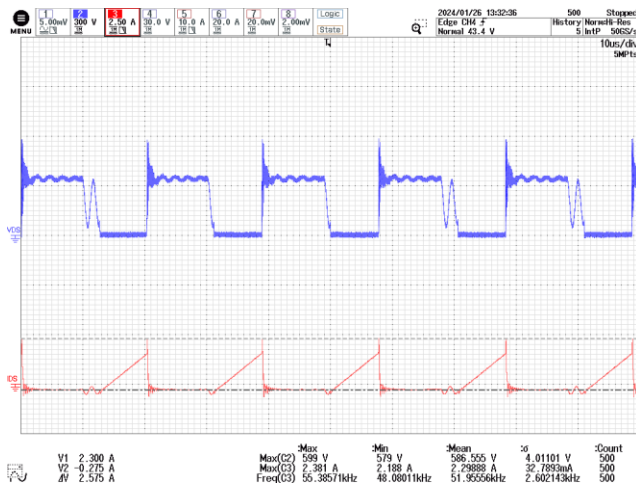


Figure 62 – INN3949CQ Drain Voltage and Current.
190 VDC, 5 A Load.

CH2: $V_{DS,INNO}$, 300 V / div.

CH3: $I_{DS,INNO}$, 2.5 A / div.

Time: 10 μs / div.

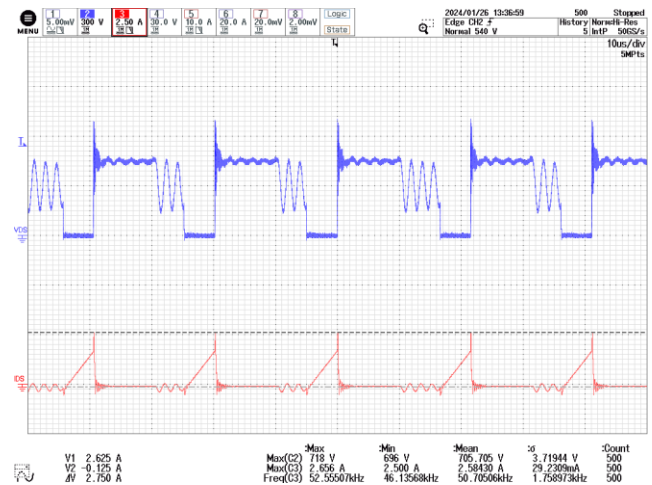


Figure 63 – INN3949CQ Drain Voltage and Current.
300 VDC, 5 A Load.

CH2: $V_{DS,INNO}$, 300 V / div.

CH3: $I_{DS,INNO}$, 2.5 A / div.

Time: 10 μs / div.

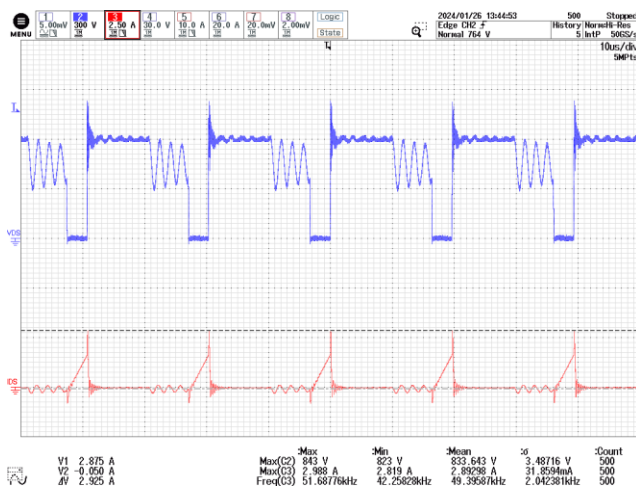


Figure 64 – INN3949CQ Drain Voltage and Current.
450 VDC, 5 A Load.

CH2: $V_{DS,INNO}$, 300 V / div.

CH3: $I_{DS,INNO}$, 2.5 A / div.

Time: 10 μs / div.

²⁹ Current was measured using a 30 A Rogowski probe

11.2.2.3 SR FET Drain Voltage and Current at -40 °C³⁰

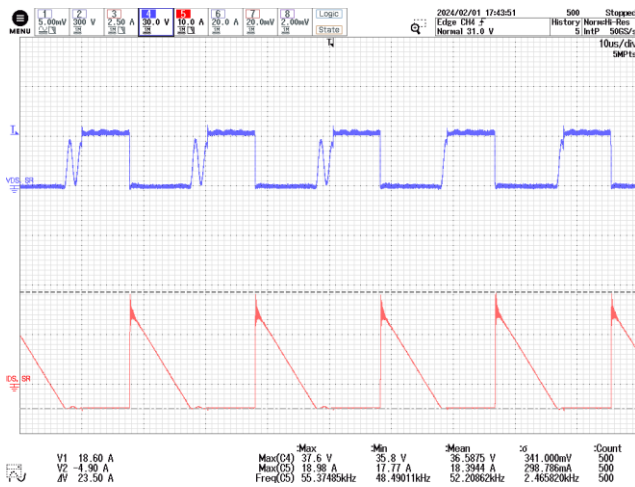


Figure 65 – SR FET Drain Voltage and Current.
190 VDC, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 μ s / div.

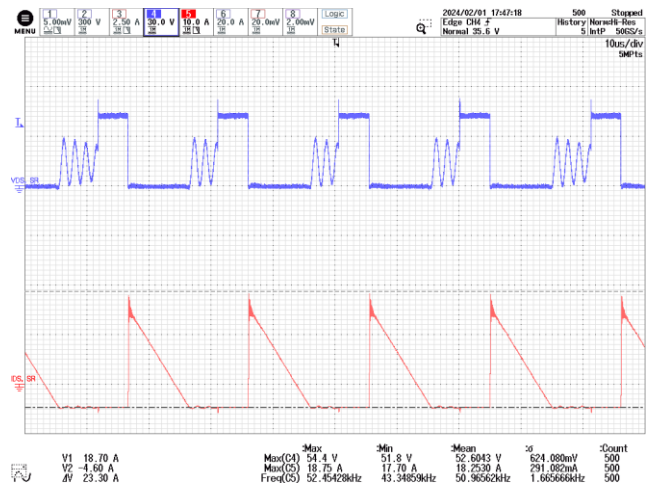


Figure 66 – SR FET Drain Voltage and Current.
300 VDC, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 μ s / div.

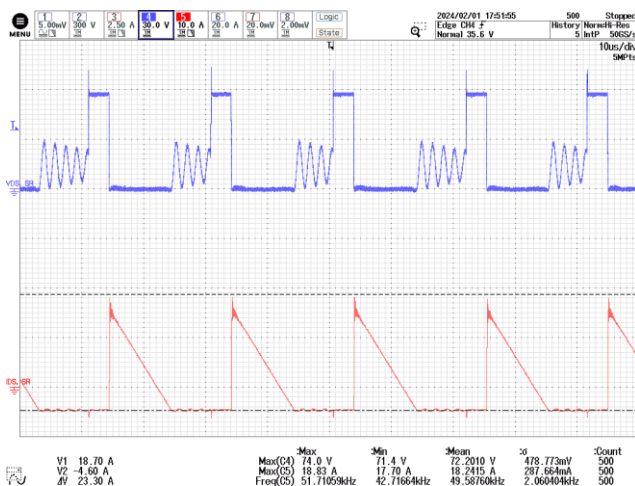


Figure 67 – SR FET Drain Voltage and Current.
450 VDC, 5 A Load.
CH2: $V_{DS,INNO}$, 30 V / div.
CH3: $I_{DS,INNO}$, 10 A / div.
Time: 10 μ s / div.

³⁰ Current was measured using a 120 A Rogowski probe

11.3 Load Transient Response

The output voltage waveform was captured during a dynamic load transient from 10% to 90% of full rated load. The duration for each load point was set to 500 ms with a load slew rate of 400 mA / μ s. The test was performed at 85 °C ambient with 10 samples taken per condition.

Dynamic Load Settings	V _{IN} (VDC)	ΔV_+ (V)	ΔV_- (V)
10% - 90% - 10%	190	0.113	-0.173
	300	0.102	-0.162
	450	0.098	-0.174

Table 13 – Load Transient Response.

11.3.1 Output Voltage Ripple with 10% - 90% - 10% Transient Load at 85 °C

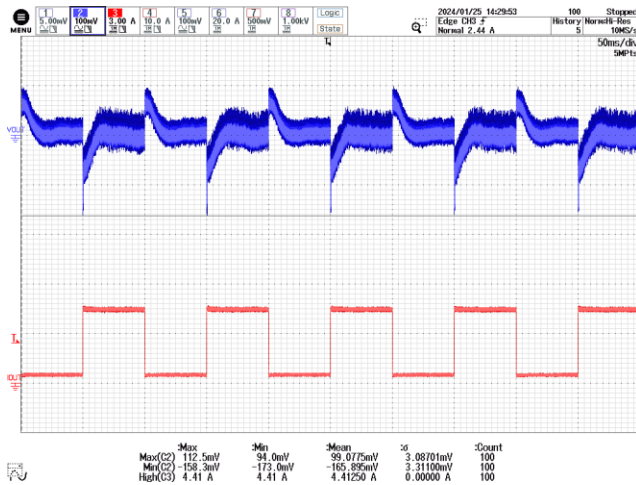


Figure 68 – Output Voltage and Current.
190 VDC, 0.5 A - 4.95 A - 0.5 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE} , 100 mV / div.
CH3: I_{OUT} , 3 A / div.
Time: 50 ms / div.

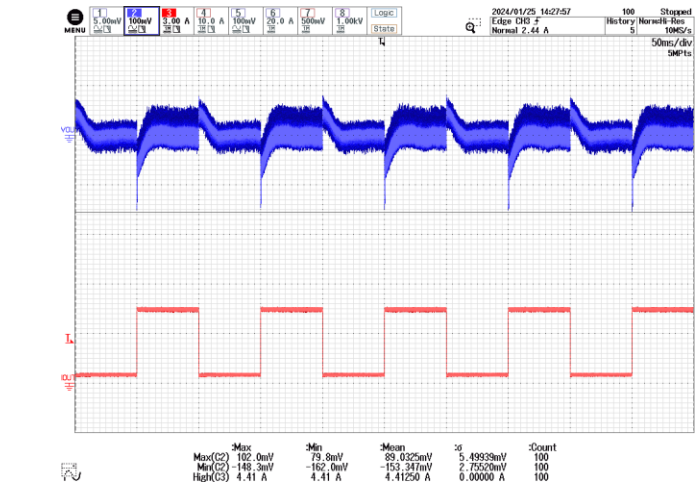
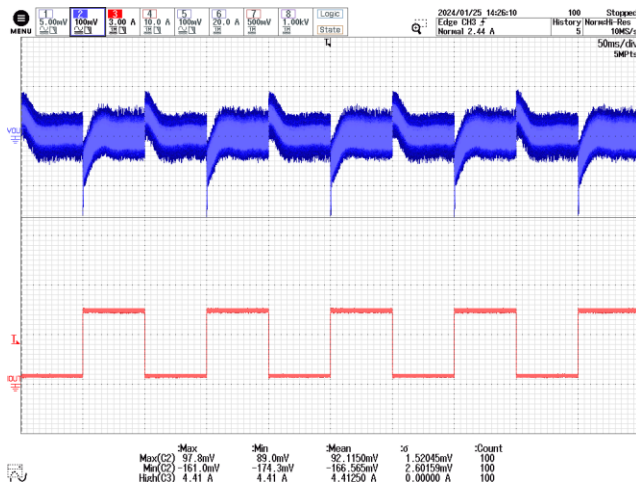


Figure 69 – Output Voltage and Current.
300 VDC, 0.5 A - 4.95 A - 0.5 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE} , 100 mV / div.
CH3: I_{OUT} , 3 A / div.
Time: 50 ms / div.

Figure 70 – Output Voltage and Current.
450 VDC, 0.5 A - 4.95 A - 0.5 A Transient Load,
85 °C Ambient.
CH2: V_{RIPPLE} , 100 mV / div.
CH3: I_{OUT} , 3 A / div.
Time: 50 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe must be utilized for DC output ripple measurements to reduce spurious signals due to noise pick-up. Details of the probe modification are provided in Figure 71 and Figure 72 below.

A CT2708 probe adapter was affixed with a 1 μ F / 50 V ceramic capacitor parallel to the probe tip and GND terminal. A twisted pair of wires, kept as short as possible, were soldered directly between the probe and the output terminals.

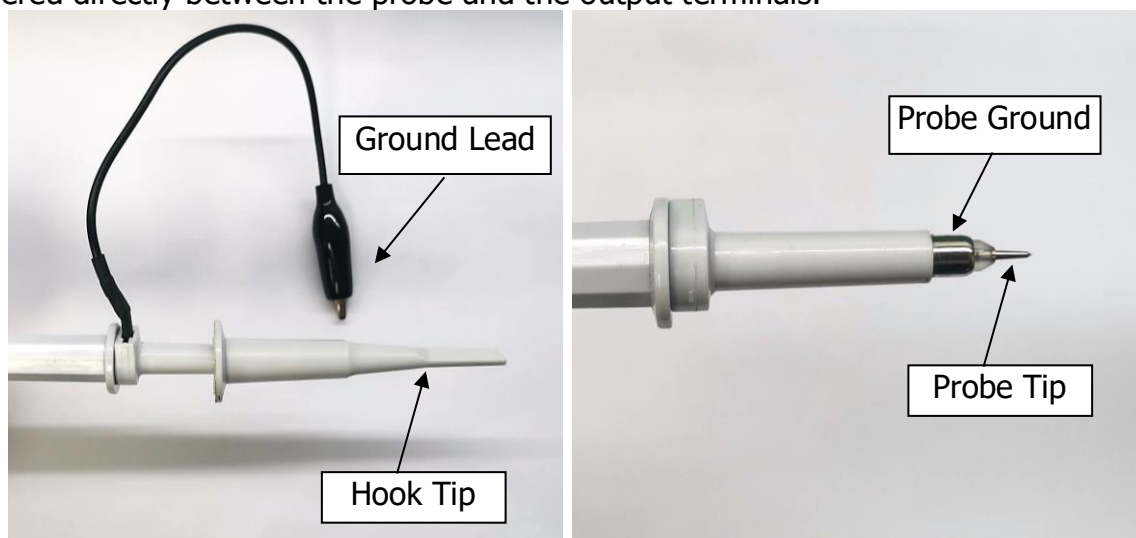


Figure 71 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

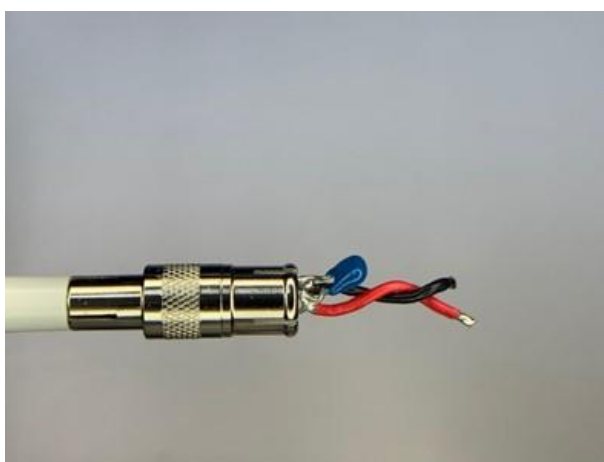


Figure 72 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurements, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform was captured at the output terminals using the ripple measurement probe with a decoupling capacitor. The waveforms shown were taken at the load setting where the highest ripple was observed and repeated for a range of input voltages.

11.4.2.1 Output Voltage Ripple at 85 °C with Constant Full Load³¹

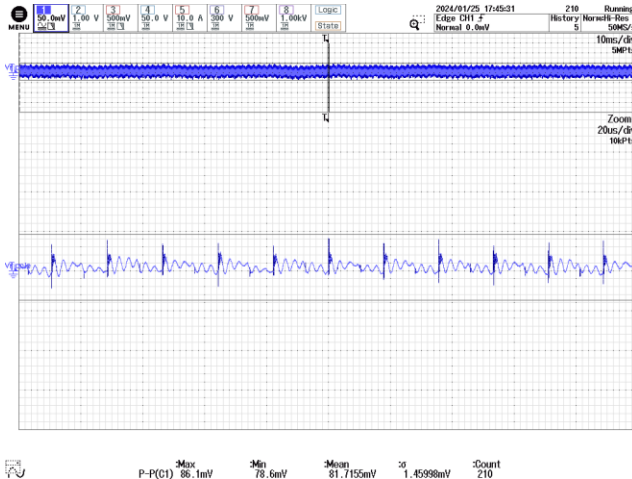


Figure 73 – Output Voltage Ripple.
190 VDC, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 10 ms / div.
 $V_{\text{RIPPLE}} = 86.1 \text{ mV}$.

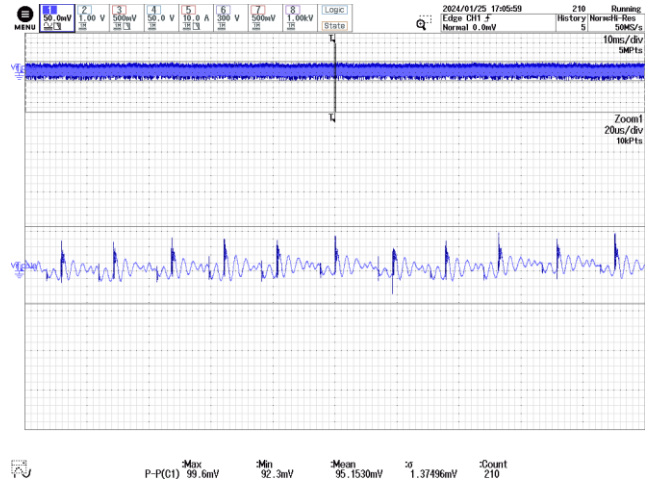
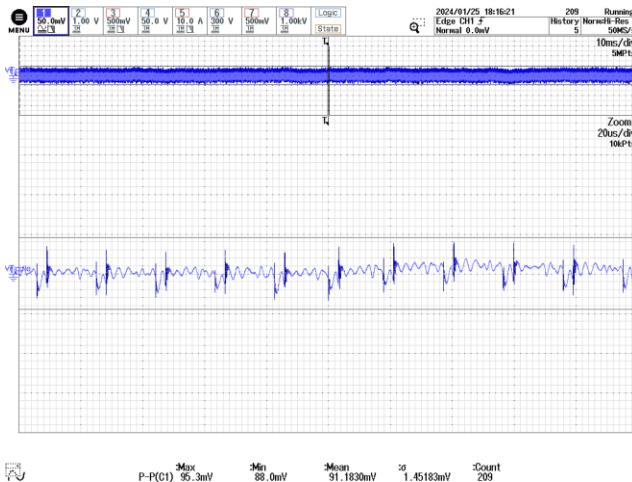


Figure 74 – Output Voltage Ripple.
300 VDC, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 10 ms / div.
 $V_{\text{RIPPLE}} = 99.6 \text{ mV}$.

Figure 75 – Output Voltage Ripple.
450 VDC, 5 A Load, 85 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 10 ms / div.
 $V_{\text{RIPPLE}} = 95.3 \text{ mV}$.

³¹ Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at -40 °C with Constant Full Load³²

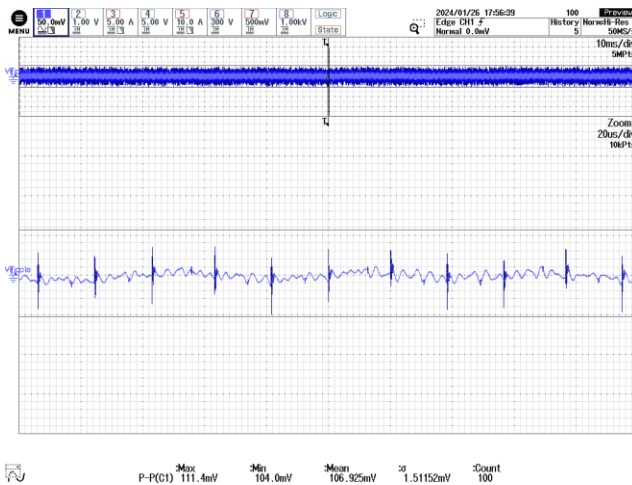


Figure 76 – Output Voltage Ripple.
190 VDC, 5 A Load, -40 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 1 ms / div.
 $V_{RIPPLE} = 150$ mV.

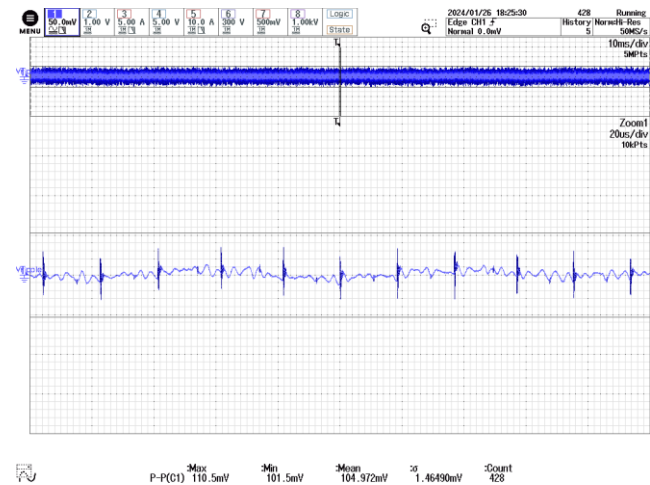
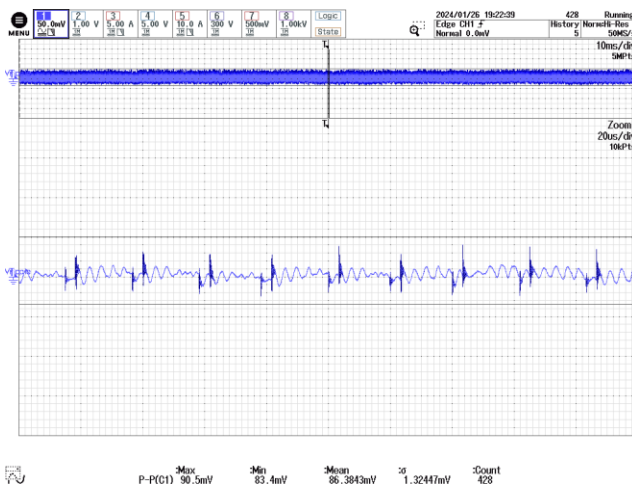


Figure 77 – Output Voltage Ripple.
300 VDC, 5 A Load, -40 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 1 ms / div.
 $V_{RIPPLE} = 141$ mV.

Figure 78 – Output Voltage Ripple.
450 VDC, 5 A Load, -40 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.
Time: 1 ms / div.
 $V_{RIPPLE} = 103$ mV.

³² Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at 25 °C with Constant Full Load³³

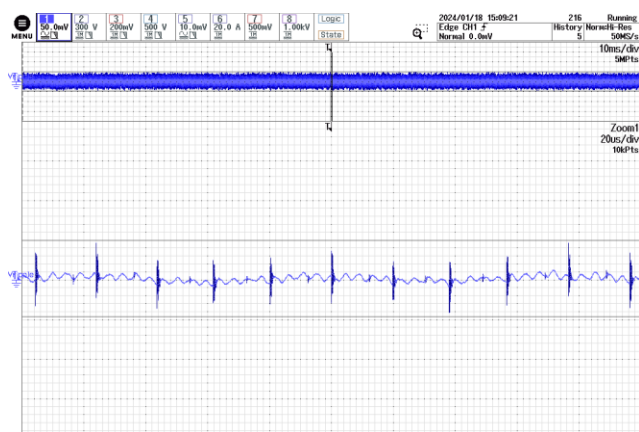


Figure 79 – Output Voltage Ripple.

190 VDC, 5 A Load, 25 °C Ambient.
CH1: V_{RIPPLE} , 50 mV / div.

Time: 10 ms / div.
 $V_{RIPPLE} = 103$ mV

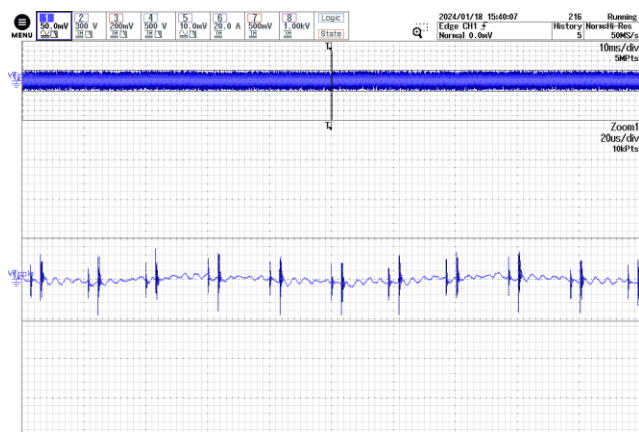


Figure 79 – Output Voltage Ripple.

190 VDC, 5 A Load, 25 °C Ambient.

CH1: V_{RIPPLE} , 50 mV / div.

Time: 10 ms / div.

$V_{RIPPLE} = 103$ mV

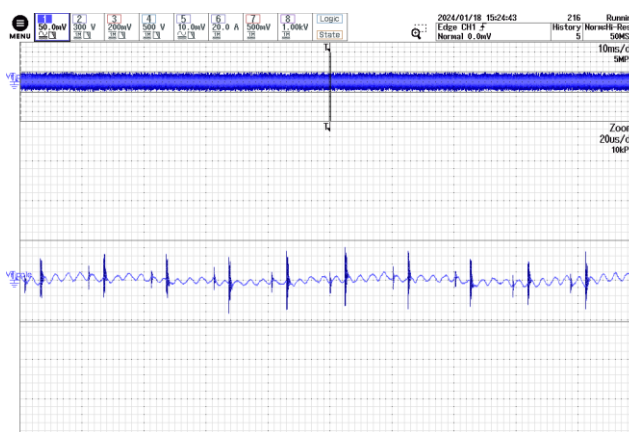


Figure 80 – Output Voltage Ripple.

300 VDC, 5 A Load, 25 °C Ambient.

CH1: V_{RIPPLE} , 50 mV / div.

Time: 10 ms / div.

$V_{RIPPLE} = 107$ mV.

Figure 81 – Output Voltage Ripple.

450 VDC, 5 A Load, 25 °C Ambient.

CH1: V_{RIPPLE} , 50 mV / div.

Time: 10 ms / div.

$V_{RIPPLE} = 110$ mV.

³³ Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C

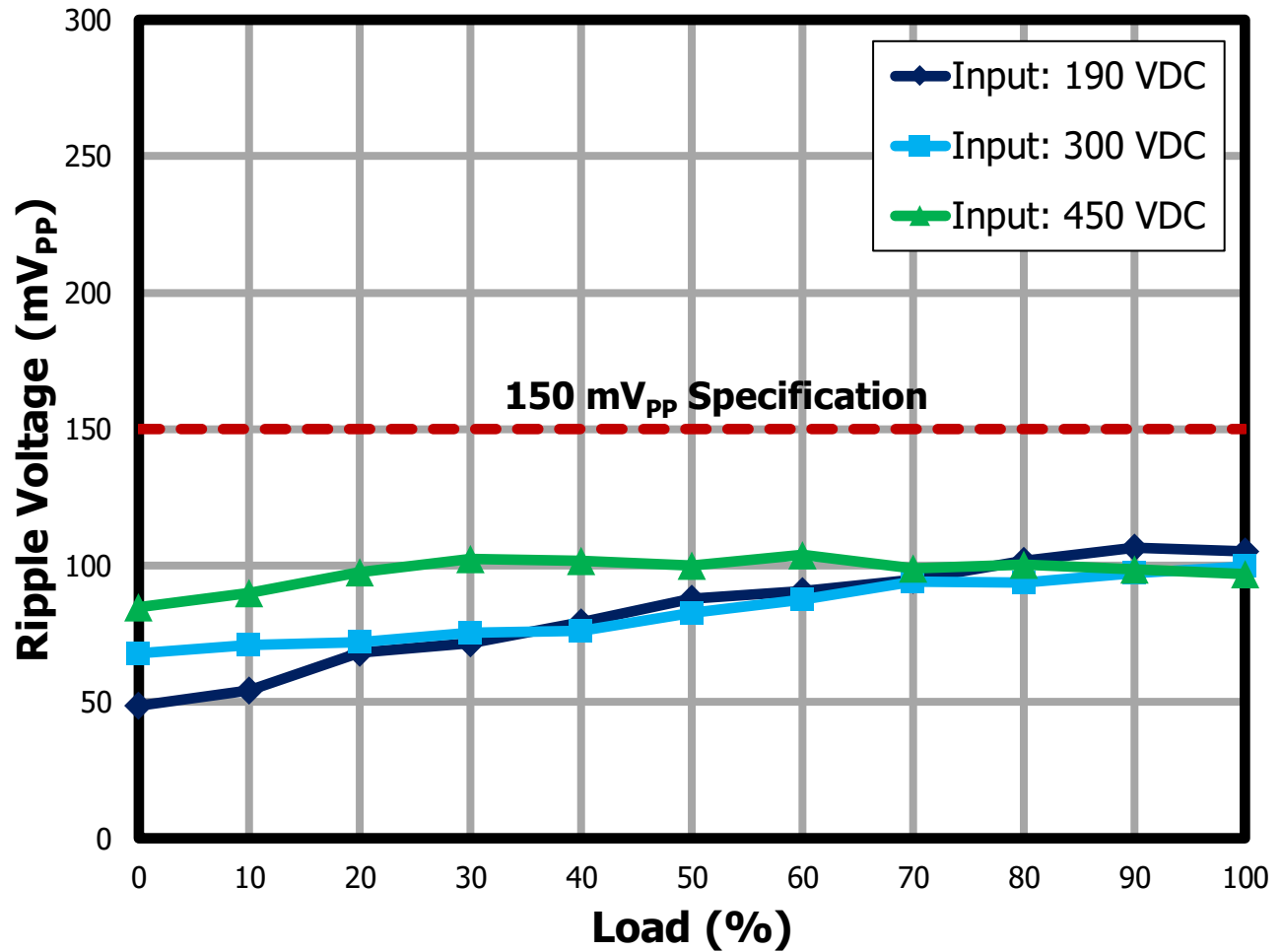


Figure 82 – Output Ripple Voltage Across Whole Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C

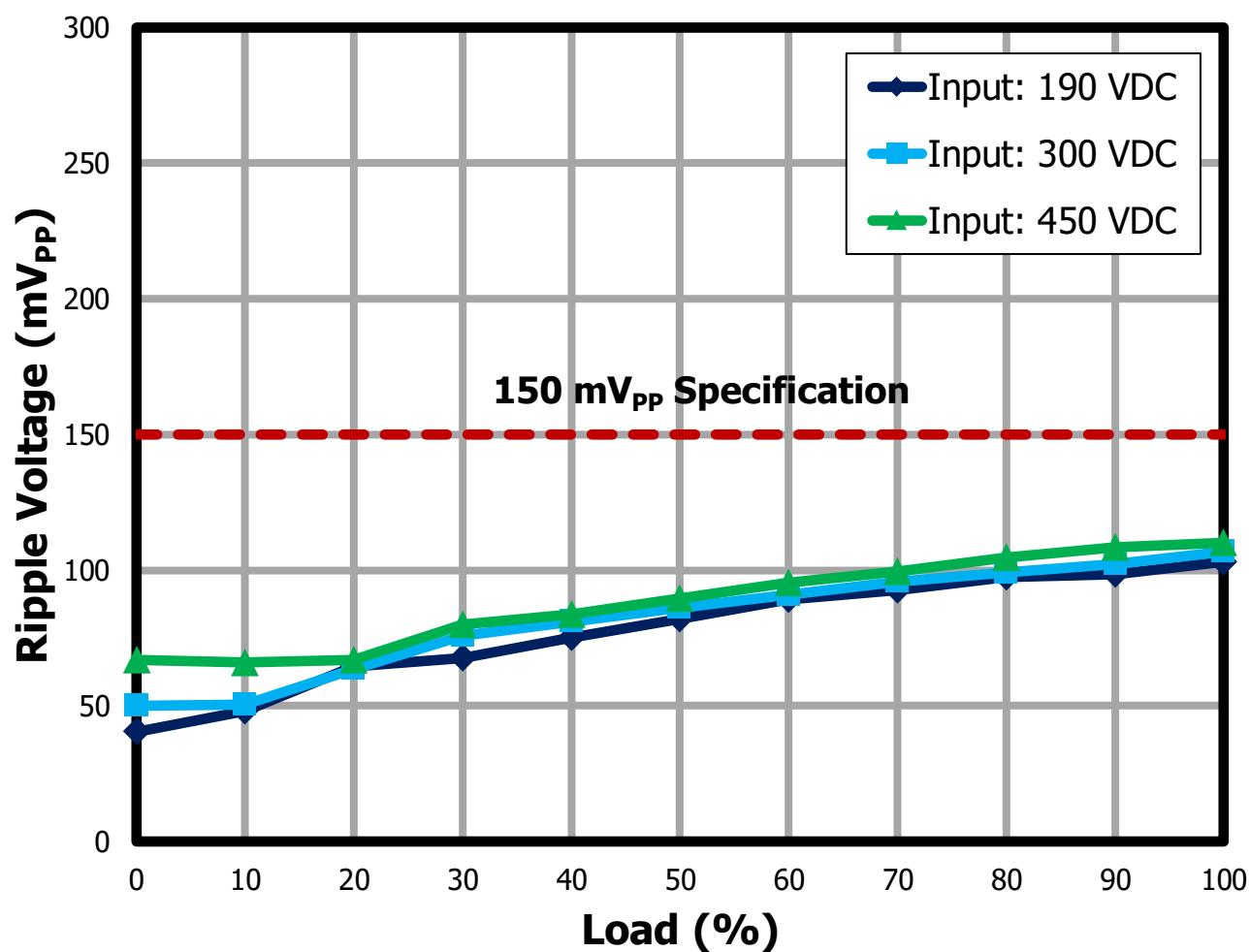


Figure 83 – Output Ripple Voltage Across Whole Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C

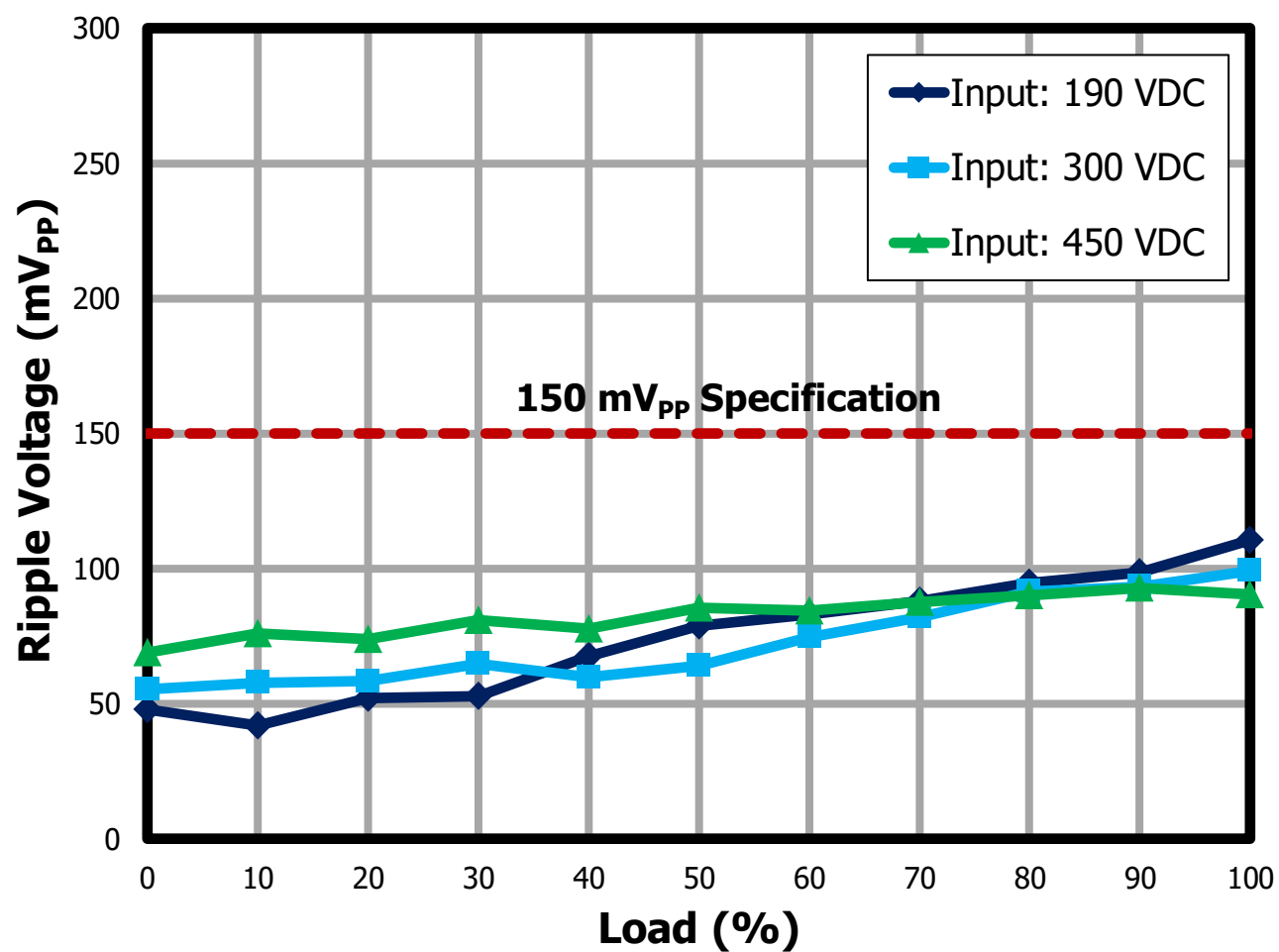


Figure 84 – Output Ripple Voltage Across Whole Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to desired ambient temperature and allowed to stabilize for 30 minutes before turning on the unit under test. For every loading condition, unit under test was allowed to stabilize for 60 seconds before output voltage and current measurements were taken.

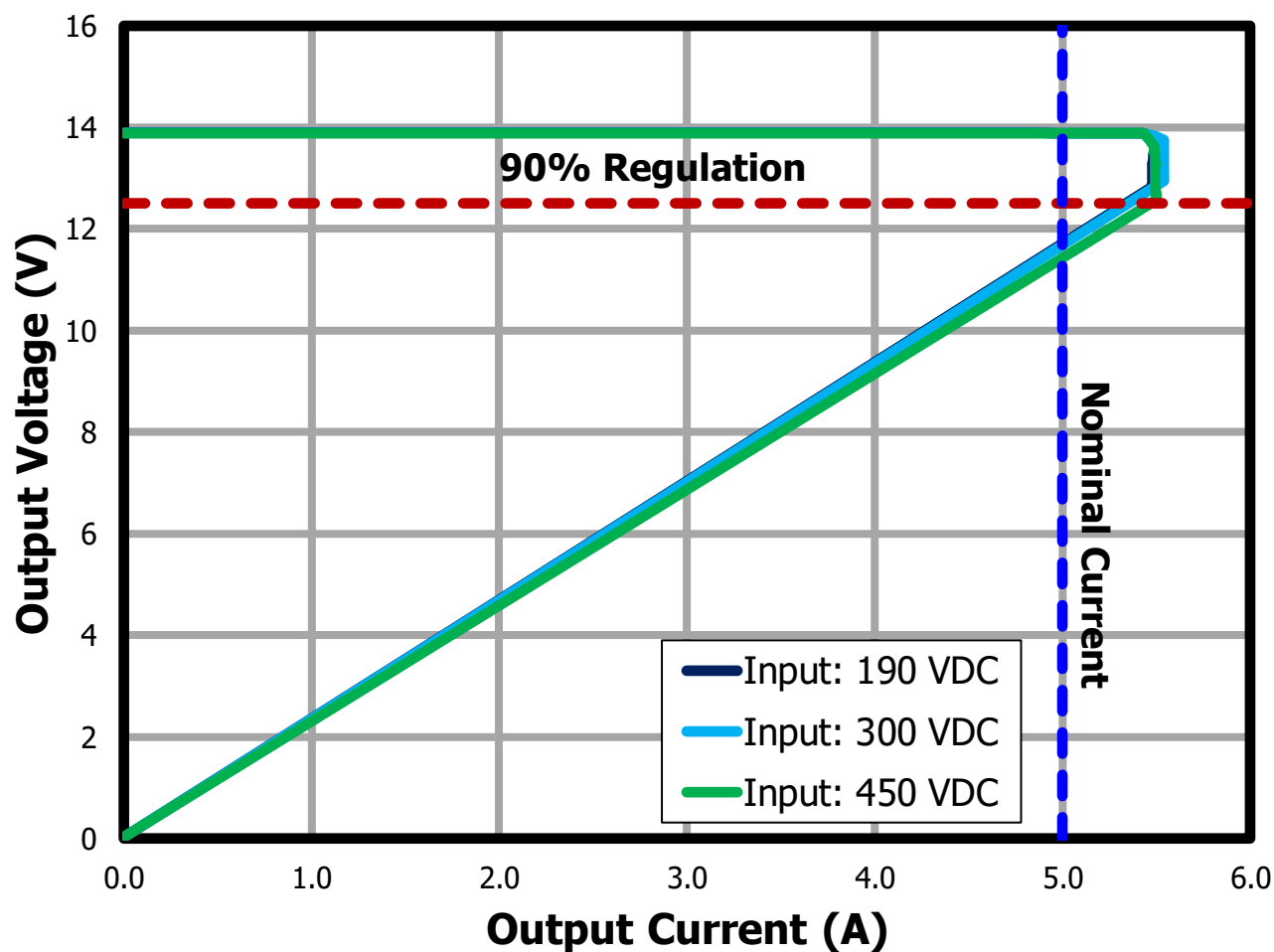


Figure 85 – 14 V Output Overload Curve at 85 °C Ambient.

13 Maximum Output Power

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. The unit was allowed to settle for 30 minutes at the start of each test sequence.

Maximum output power at a given input voltage was determined by finding the maximum loading condition in which the unit did not enter auto-restart (AR) mode operation or trigger any overtemperature protection. Component case temperature ratings for the critical components were also considered in determining the maximum output power capability.

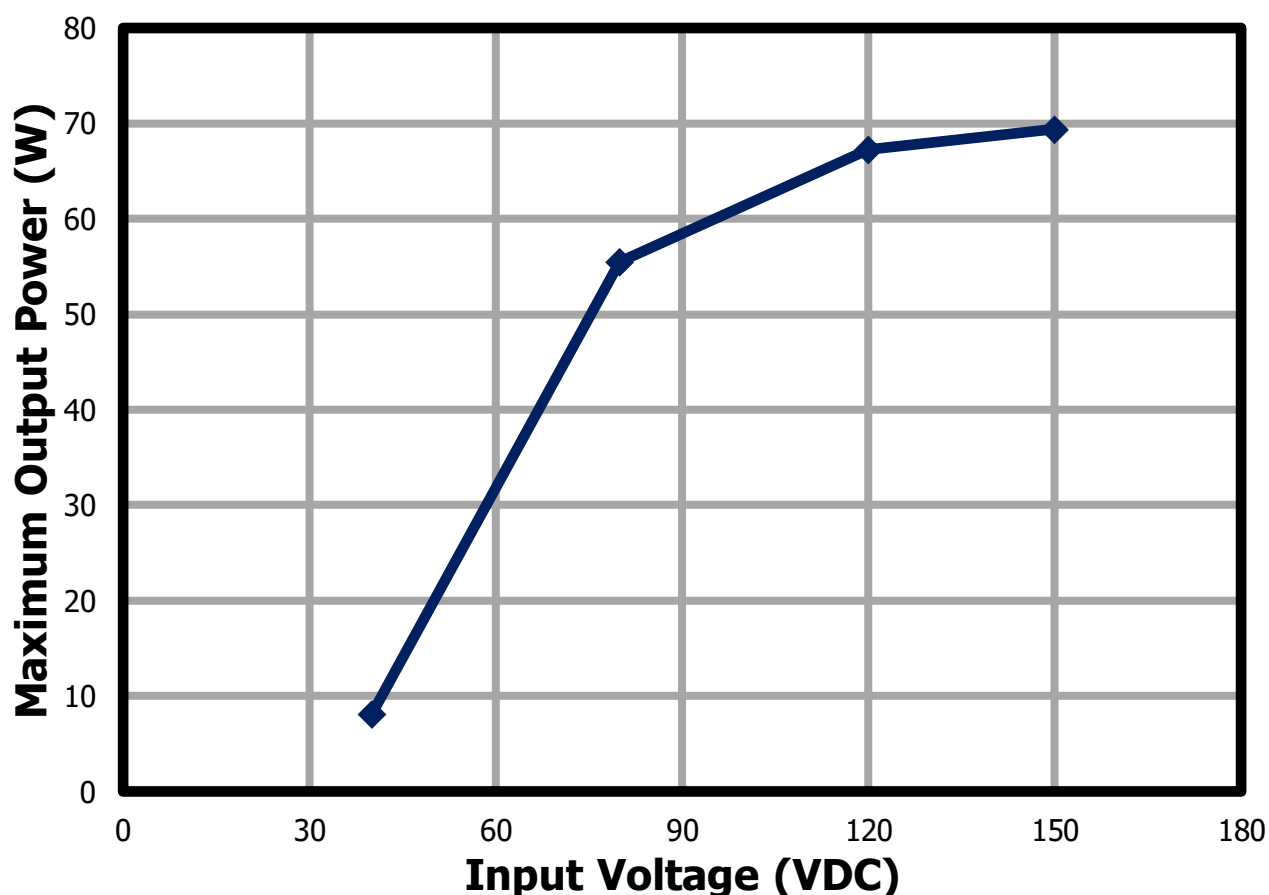


Figure 86 – Maximum Output Power Curve at 85 °C Ambient.

Input Voltage (VDC)	Maximum Power (W)	Limiting Factor	Value (°C)
150	69.4	SR Snubber Temperature	125
120	67.3	SR Snubber Temperature	125
80	55.5	InnoSwitch3-AQ OverTemperature Protection	128
40	8.07	InnoSwitch3-AQ Minimum Off-time	-

Table 14 – Maximum Output Power Capability Limiting Factor.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Feb-24	RS	A	Initial Release.	CC/JRLC
17-Dec-24	NU	B	Text Changes. Updated Schematic and No-Load Figure. Updated Bill of Materials.	Apps & Mktg



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