Design Example Report

Title	**60 W Isolated Flyback Power Supply Using INN3629C – An InnoSwitch3-EP IC with a 1250 V PowiGaN Switch**
Specification	90 VAC – 480 VAC Input; 12 V / 5 A Output
Application	Auxiliary Power Supply for High Voltage Industrial Applications
Author	Applications Engineering Department
Document Number	DER-1025
Date	May 31, 2026
Revision	A

Summary and Features

- Off-line CV/CC QR flyback integrated switcher IC with 1250 V PowiGaN™ switch and synchronous rectification for higher efficiency
- < 140 mW no-load input power across voltage range
    - < 50 mW at 230 VAC
- Very high full-load efficiency
    - >93% at 230 VAC
- High average efficiency
    - >92% at 115 VAC and 230 VAC
    - >90% from 90 VAC up to 480 VAC
- FluxLink™ barrier crossing technology means that no optocoupler is required - increases reliability and reduces part-count
- Meets EN550022 and CISPR-22 Class B conducted EMI with ≥ 6db margin
- Very low component count: 67 components

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a 12 V / 5 A power supply using the InnoSwitch™3-EP IC (INN3629C) with an integrated 1250 V PowiGaN switch. This design demonstrates the high-power density and efficiency that can be achieved due to the high level of integration of the InnoSwitch3 IC and excellent switching efficiency provided by the control algorithm, synchronous rectification and the PowiGaN switch.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board, Top View

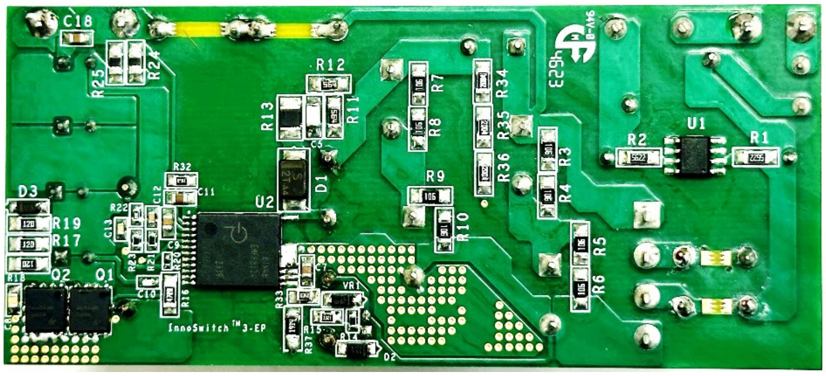


Figure 2 – Populated Circuit Board, Bottom View

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min.	Nom.	Max.	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	480	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				<140	mW	Vin: 90 VAC – 480 VAC
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth, at 25 °C Ambient
Output Current	I_{OUT}		5		A	
Total Output Power						
Continuous Output Power	P_{OUT}		60		W	
Efficiency	η		91			Average @ 90 VAC
			92			Average @ 115 VAC
			93			Average @ 230 VAC
			93			Average @ 265 VAC
			90			Average @ 480 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				6	kV	1.2/50 µs Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
Combination Wave Surge Test				6	kV	
EFT				4	kV	IEC 61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Table 1 – Power Supply Specifications

3 Schematic

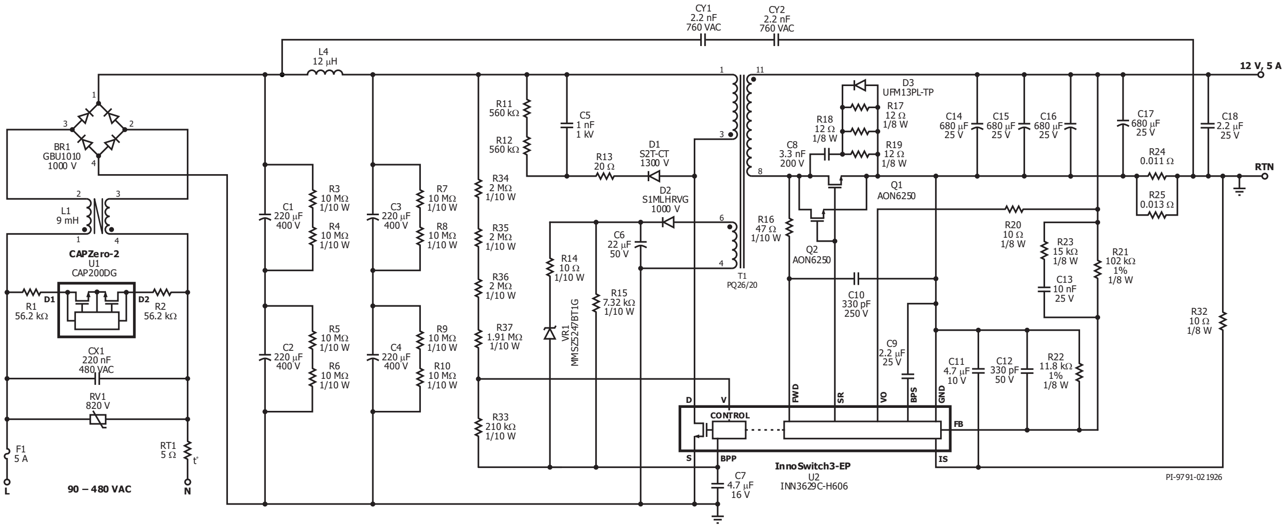


Figure 3 – Power Supply Schematic

4 Circuit Description

The InnoSwitch3-EP IC combines primary, secondary, isolation and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates a 1250 V PowiGaN primary switch, primary-side controller, secondary-side controller for synchronous rectification and safety-rated FluxLink™ barrier crossing technology which eliminates the optocoupler typically required for secondary-side feedback in conventional SSR power supplies. The InnoSwitch3-EP IC also employs quasi-resonant switching to achieve high efficiency. This feature is particularly beneficial for high line voltage applications where switching losses become significant.

4.1 EMI Filtering and AC Rectifier Stage

Fuse F1 isolates the circuit and provides protection in the event of component failure. Resistor RT1 reduces inrush current. Varistor RV1 clamps any input voltage spike generated by abnormal surge events. X-capacitor CX1 and common mode choke L1 attenuate common mode noise. To meet safety requirements, the voltage across CX1 is discharged by the CAPZero™-2 IC (U1) in series with R1 and R2 when AC is disconnected. During normal operation the CAPZero IC is open circuit – reducing no-load consumption. Bridge rectifier BR1 rectifies the AC line voltage and provides a full-wave rectified DC across the input filter capacitors C1, C2, C3 and C4. Inductor L4 is connected between input filter capacitors to form a π-filter. The filter attenuates both common and differential mode noise. Capacitors CY1 and CY2 reduce common mode electromagnetic interference (EMI). Resistors R3, R4, R5, R6, R7, R8, R9 and R10 are used to balance the voltage across the input filter capacitors.

4.2 InnoSwitch3-EP IC Primary

One end of the transformer (T1) primary winding is connected to the rectified DC bus; the other end is connected to the drain terminal of the power switch inside the InnoSwitch3-EP IC (U2). Resistors R33, R34, R45, R36 and R37 provide input voltage information to the InnoSwitch3-EP IC via the V pin. This information is used by U1 to provide the overvoltage and undervoltage protection.

A simple RCD clamp formed by diode D1, resistors R11, R12, R13 and capacitor C5 limits the peak drain voltage appearing across U2 at turn-off by dissipating the energy stored in the leakage inductance of transformer T1.

U2 is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C7) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R15 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U2).

Zener diode VR1 in series with resistor R14 offers primary sensed output overvoltage protection (OVP). In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage on the output of the converter, the auxiliary winding voltage increases and causes Zener diode VR1 to breakdown. This causes a current to flow into the BPP pin of U2. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-EP device enters auto restart, protecting the circuit.

4.3 The InnoSwitch3-EP IC also controls the Output Stage

The secondary side of the InnoSwitch3-EP IC (U2) provides output voltage and output current sensing and provides drive to the Synchronous Rectification Field-Effect Transistors (SR FETs). The output from the secondary winding of the transformer is rectified by the SR FETs Q1, Q2 and filtered by output capacitors C14, C15, C16, C17 and C18. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced by an RCD snubber comprised of resistors R17, R18, R19, C8 and diode D3 which minimizes power dissipation in the resistors.

The gates of Q1 and Q2 are turned on by the secondary-side (Master) controller inside U2, based on the winding voltage sensed via resistor R16 and fed into the FWD pin of the IC. Capacitor C10 prevents high voltage spikes from appearing on the FWD pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (via the FWD pin) or the output voltage. Capacitor C9 which connected to the BPS pin of InnoSwitch3-EP IC (U2) provides energy storage and decoupling for the internal circuitry.

Output current is sensed between the IS and GND pins by monitoring the voltage drop across resistors R24 and R25. The voltage drop is limited to approximately 36 mV to reduce losses. Capacitor C11 and resistor R32 provide filtering for the IS pin of U1 to protect it from external noise.

The InnoSwitch3-EP IC operates in constant voltage mode before reaching the current limit. During normal operation, output voltage regulation is achieved through sensing the output voltage via a voltage divider made up of resistors R21 and R22. The voltage across resistor R22 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is adjusted such that the output of the potential divider matches this voltage. Capacitor C12 provides decoupling from high frequency noise while capacitor C13 and resistor R23 form a feed-forward circuit to speed up response time and reduce output ripple. Resistor R20 in series with the VO pin acts as protection from common mode surges and electrostatic discharge (ESD).

5 PCB Layout

PCB copper thickness is 2.0 oz.
PCB Material Thickness is 0.062 inches.
PCB Material is FR4.

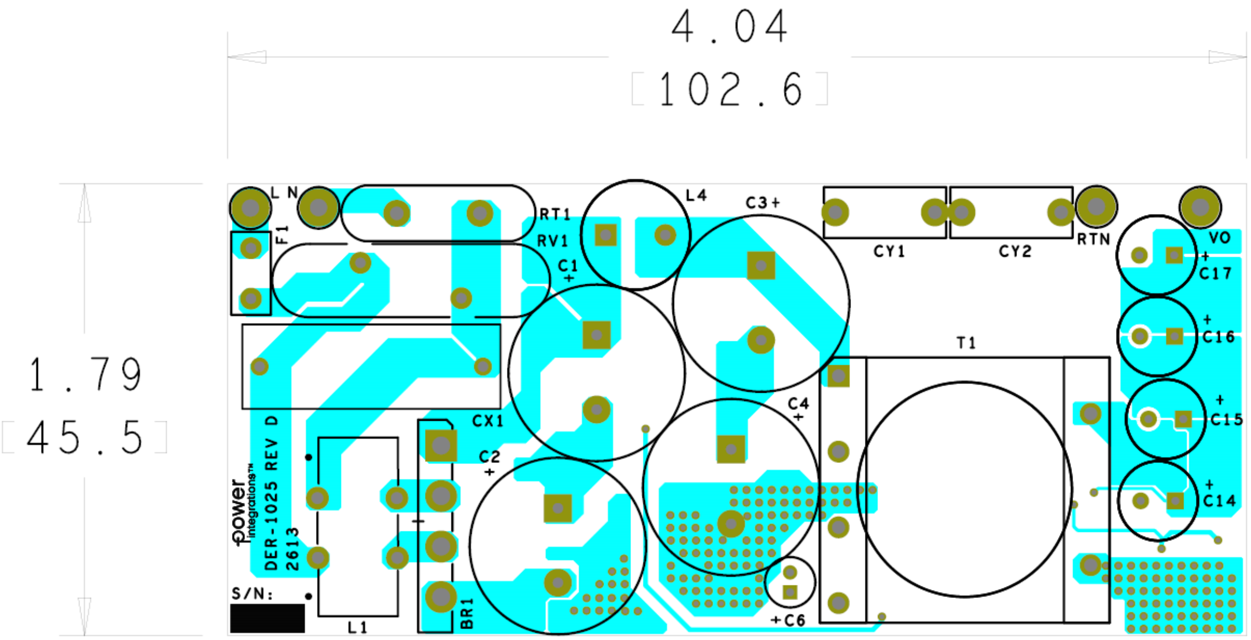


Figure 4 – Printed Circuit Board, Top

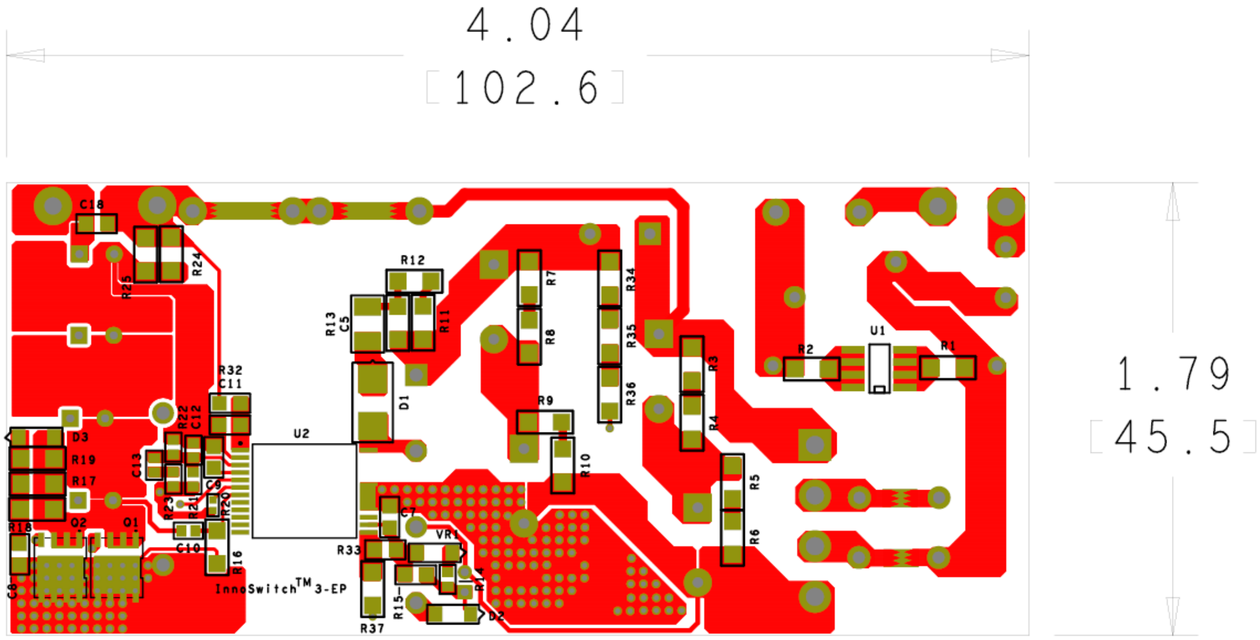


Figure 5 – Printed Circuit Board, Bottom

6 Bill of Materials

6.1 Bill of Material: Electrical Components

Item	Qty.	Ref Des	Description	Manufacturer Part Number	Manufacturer
1	1	BR1	Bridge Rectifier, Single Phase, Standard, 1 kV, Through Hole GBU	GBU1010	SMC Diode Solutions
2	4	C1 C2 C3 C4	220 μF, 400 V, Aluminum Electrolytic Capacitors, Radial, Can, 2000 Hrs @ 105 °C, (18 x 45 mm)	EPAG401ELL221MM45S	United Chemi-Con
3	1	C5	1000 pF, ±10%, 1000 V (1 kV), Ceramic Capacitor, C0G, NP0 1206 (3216 Metric)	C1206C102KDGACAUTO	Kemet
4	1	C6	22 μF, 50 V, Aluminum Electrolytic Capacitors, Radial, Can 2000 Hrs @ 85 °C, (5 x 11), LS 2 mm	EEU-FM1H220H	Panasonic Electronic Components
5	1	C7	4.7 μF, 16 V, Ceramic, X7R, 0805 (2012 Metric)	CL21B475KOFNNNE	Samsung Electro-Mechanics
6	1	C8	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX Corp
7	1	C9	2.2 μF, ±10%, 25 V, Ceramic Capacitor X7R, 0805 (2012 Metric)	CL21B225KAFNFNE	Samsung Electro-Mechanics
8	1	C10	330 pF ±5% 250 V Ceramic Capacitor C0G, NP0 0603 (1608 Metric)	CGA3E3C0G2E331J080AA	TDK Corp
9	1	C11	4.7 μF ±10% 10 V Ceramic Capacitor X7R 0805 (2012 Metric)	LMK212B7475KGHT	Taiyo Yuden
10	1	C12	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
11	1	C13	10 nF, 0.01 μF, ±10%, 25 V, Ceramic Capacitor, X7R, General Purpose, -55 °C ~ 125 °C, 0603 (1608 Metric)	CL10B103KA8NFNC	Samsung Electro-Mechanics
12	4	C14 C15 C16 C17	680 μF, ±20%, 25 V, Aluminum - Polymer Capacitors Radial, Can 16 mOhm 2000 Hrs @ 105 °C (8 mm x 16 mm)	A750KW687M1EAAE016	KEMET
13	1	C18	2.2 μF, ±10%, 25 V, X7R, r, -55 °C ~ 125 °C, 0805 (2012 Metric)	CL21B225KAFVPNE	Samsung Electro-Mechanics America, Inc.
14	1	CX1	0.22 μF, ±20%, Film Capacitor 480 V 1000 V (1 kV) Polypropylene (PP), Metallized Radial, 26 mmL x 8.5 mmW x 18 mmH x 22.5 mmLS	F339X142248MIP2T0	Vishay Beyschlag/Draloric/BC Components
15	2	CY1 CY2	CAP, 2200 pF, ±20%, 760 VAC, Ceramic Capacitor Y5U (E) Radial, Disc	AY1222M47Y5UC63L0	Vishay/ BC Components
16	1	D1	Diode, Standard, 1300 V, 2 A, Surface Mount SMB, (DO-214AA)	S2T-CT	Diotec Semiconductor
17	1	D2	Diode, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
18	1	D3	DIODE, GEN PURP, 200 V, 1 A, SOD-123F, SOD123FL	UFM13PL-TP	Micro Commercial Co.
19	1	F1	5 A, 250 V, Slow, Long Time Lag, RST	RST 5	Belfuse
20	1	L1	9 mH, Toroidal Common Mode Input Choke, L1, custom, DER-1025, wound on 32-00331-00 core	32-00457-00	Power Integrations
21	1	L4	Fixed Inductor, 12 μH @100 KHz, ± 10%, 5.1 A, 0.03 5 ohm, AEC-Q200, Unshielded, Ferrite, Radial, -40 °C ~ 85 °C, 11 x 11.5 mm	RFB1010-120L	Coilcraft
22	2	Q1 Q2	MOSFET, N-CH, 150 V, 52 A, 8DFN	AON6250	Alpha & Omega Semiconductor Inc
23	2	R1 R2	RES, 56.2 k, 1%, 1/4 W, Thick Film, 1206	RC1206FR-0756K2L	YAGEO
24	8	R3 R4 R5 R6 R7 R8 R9 R10	RES, 10 M, 5%, 1/4 W, Thick Film, 1206	RC1206FR-0710ML	YAGEO

25	2	R11 R12	RES, 560 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J564V	Panasonic
26	1	R13	RES, 20 Ohm, ±5%, 0.5 W, 1/2 W, 1210 (3225 Metric), Thick Film	CRCW121020R0JNEA	Vishay Dale
27	1	R14	RES, 10 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
28	1	R15	RES, 7.32 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7321V	Panasonic
29	1	R16	RES, 47.0 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF47R0V	Panasonic
30	3	R17 R18 R19	RES, 12 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J120V	Panasonic
31	1	R20	RES, 10 R, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
32	1	R21	RES, 102 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1023V	Panasonic
33	1	R22	RES, 11.8 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1182V	Panasonic
34	1	R23	RES, 15 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1502V	Panasonic
35	1	R24	0.011 Ohm, ±1%, ±75 ppm/°C, 1W, 1206 (3216 Metric), Automotive AEC-Q200, Current Sense, -55 °C ~ 155 °C	ERJ-8CWFR011V	Panasonic Electronic Components America, Inc.
36	1	R25	RES, 13 mOhms ±1% 1 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Current Sense Thick Film	ERJ-8BWFR013V	Panasonic Electronic Components
37	1	R32	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
38	1	R33	RES, 210 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2103V	Panasonic
39	3	R34 R35 R36	RES, 2.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
40	1	R37	RES, 1.91 M, 1%, 1/4 W, Thick Film, 1206	RMCF1206FT1M91	Stackpole
41	1	RT1	NTC Thermistor, 2.5 Ohms, 8 A	CL-30	Thermometrics
42	1	RV1	510 VAC, 10 kA, 365 J, disc 20 mm, RADIAL	V20E510P	Littlefuse
43	1	T1	Bobbin, PQ26/20, Vertical, 12 pins	B65878E0012D001	EPCOS (TDK)
44	1	U1	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
45	1	U2	INN3629C-H606, INNO3 Switch Integrated Circuit, InnoSwitch-3EP_1250V, InSOP24D	INN3629C-H606	Power Integrations
46	1	VR1	DIODE, ZENER, 17V, ±5%, 500mW, SOD123, SOD-123	MMSZ5247BT1G	ON Semi

Table 2 – Bill of Materials, Electrical parts

6.2 Bill of Material: Mechanical Components

Item	Qty.	Ref Des	Description	Manufacturer Part Number	Manufacturer
1	1	L	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	2	N RTN	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

Table 3 – Bill of Materials, Mechanical parts

7 Transformer (T1) Specification

7.1 Electrical Diagram

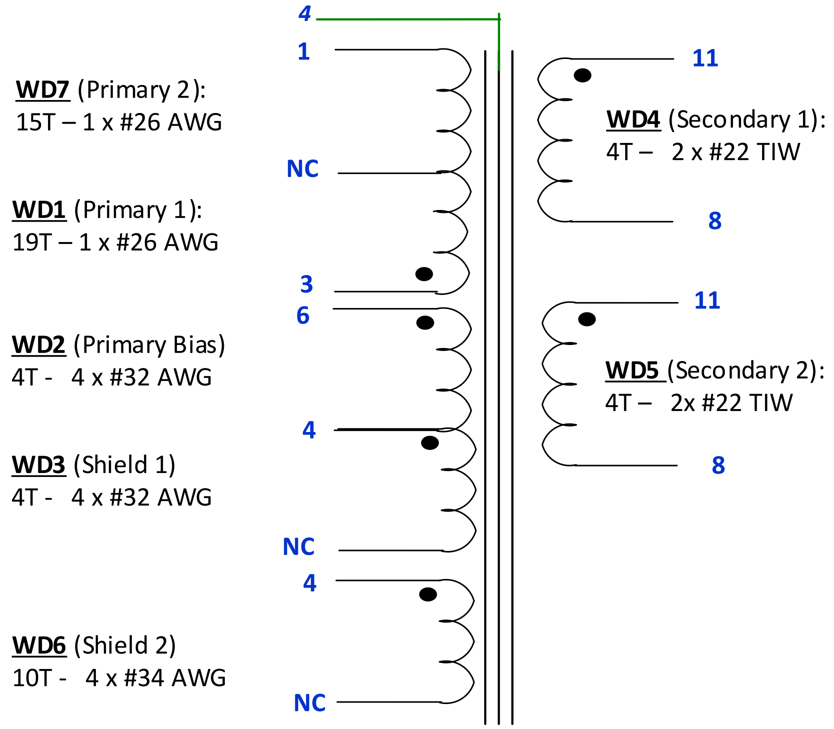


Figure 6 – Transformer Electrical Diagram

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 3 to pin 1, with all other Windings open.	622 µH ±5.0%
Electrical Strength	60 Hz 1 second, from pins 1, 3, 4, 6 to pins 8, 11	3000 VAC
Primary Leakage Inductance	Measured between pin 3 to pin 1, with all other windings shorted.	6 µH (Max.)

Table 4 – Transformer Electrical Specifications

7.3 List of Materials

Item	Description
[1]	Core: PQ2620, TDK-PC95.
[2]	Bobbin: PQ26/20-Vert-12pins (6/6); PI#: 25-01140-00.
[3]	Magnet wire: #26 AWG, double coated.
[4]	Magnet wire: #32 AWG, double coated.
[5]	Magnet wire: #34 AWG, double coated.
[6]	Magnet wire: #22 AWG, Triple Insulated Wire.
[7]	Bus wire: #28 AWG, Alpha wire, tinned copper.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 9.3 mm width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 19.0 mm width.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 25.0 mm width.
[11]	Varnish: Dolph BC-359.

Table 5 – Transformer Materials List

7.4 Transformer Build Diagram

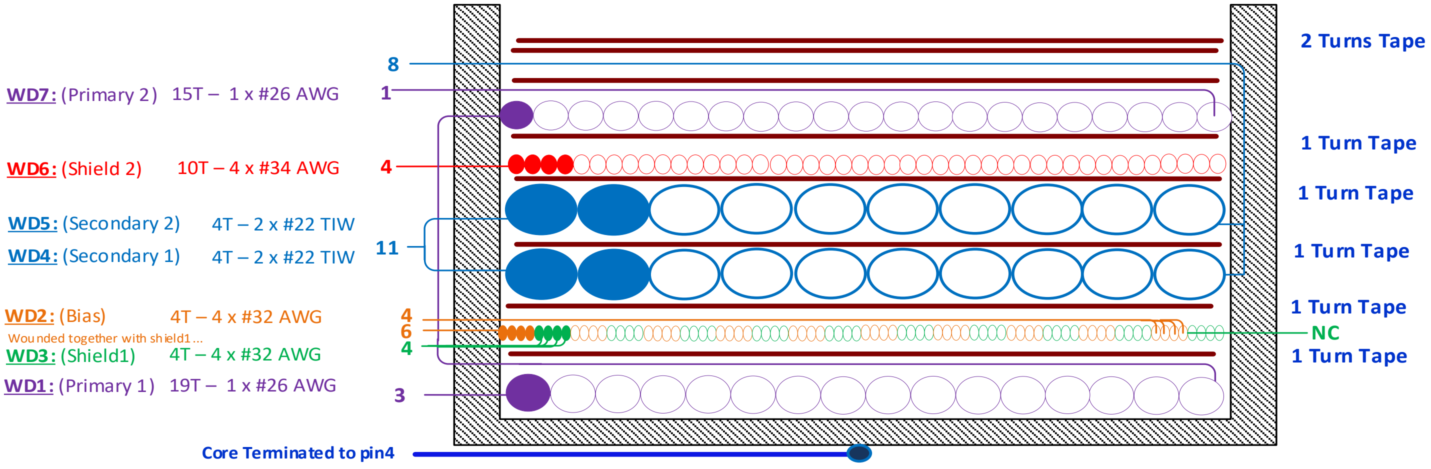


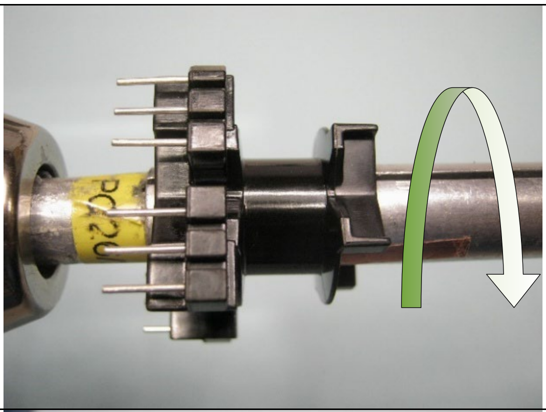
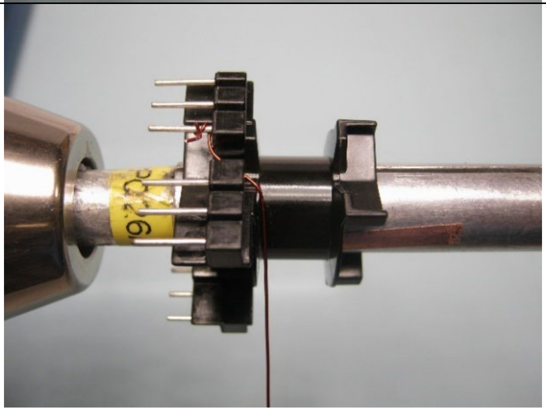
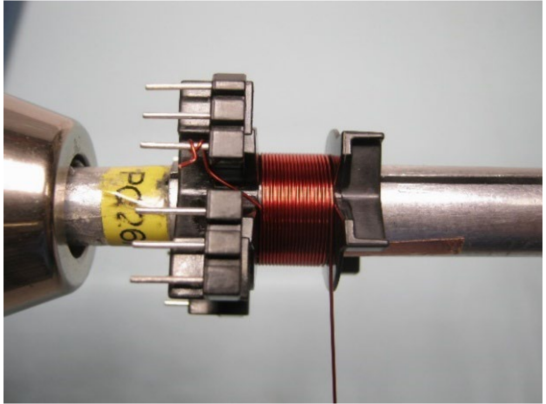
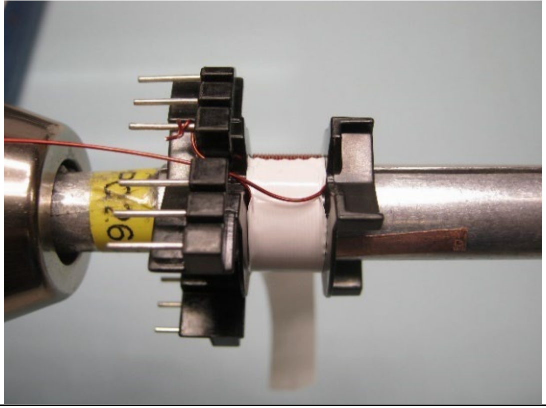
Figure 7 – Transformer Build Diagram

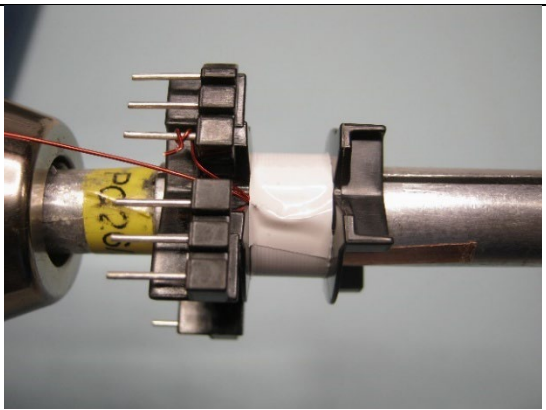
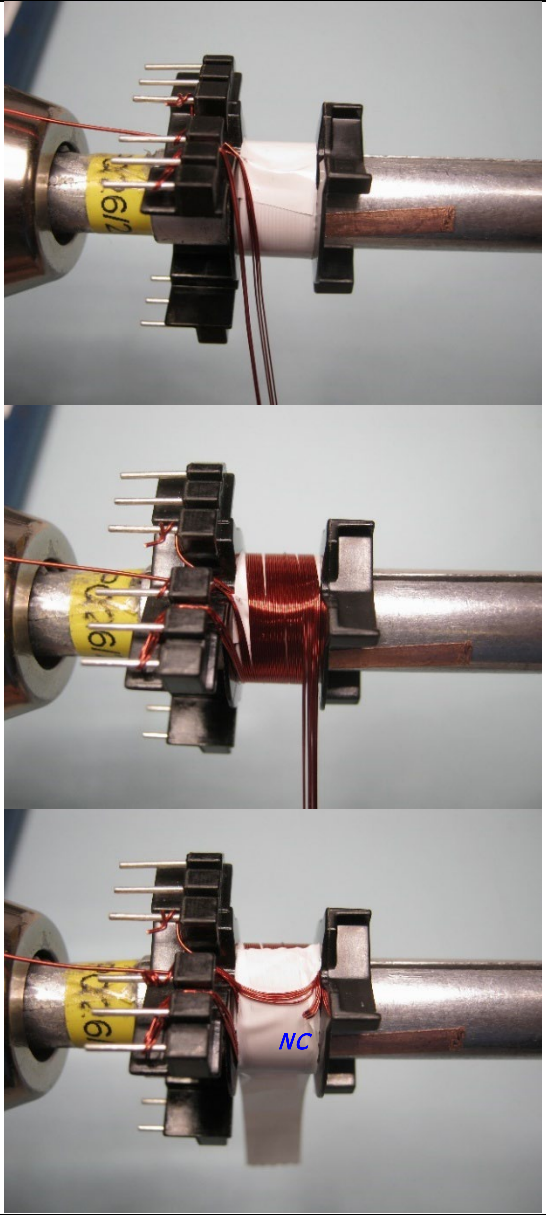
7.5 Transformer Instructions

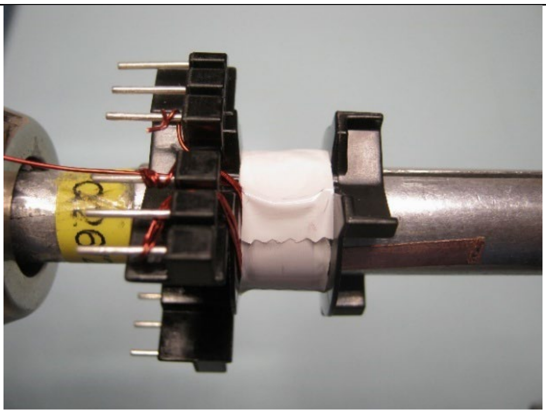
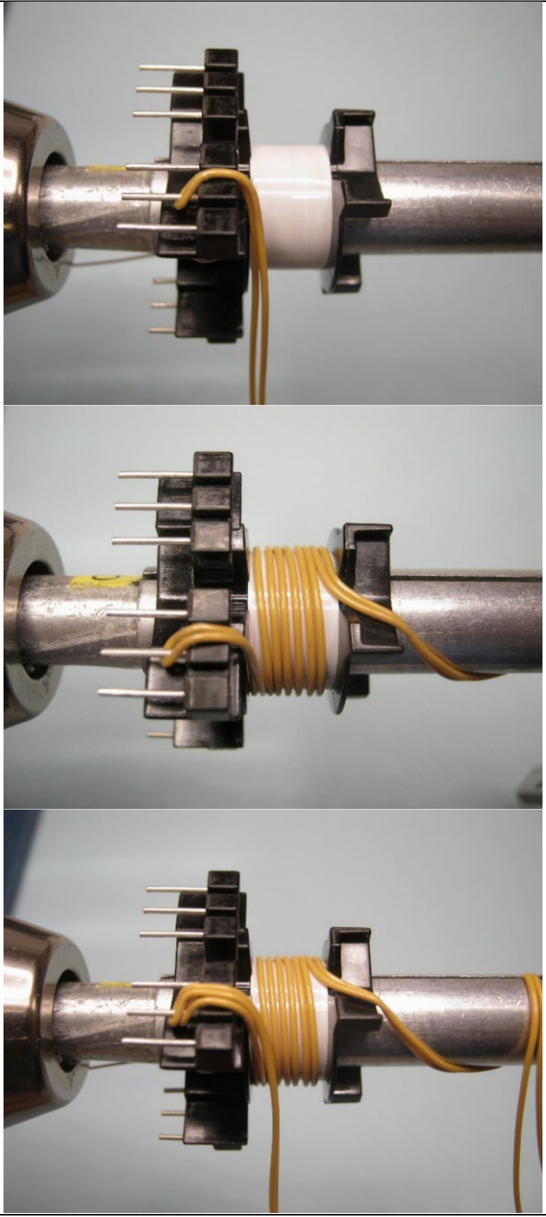
Winding preparation	Position the bobbin, Item [2], on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise (CW) for forward direction.
WD1 1st Primary Winding	Use wire of Item [3]. Starting at pin 3, wind 19 turns (1 layer), with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire floating for WD7-2nd Primary Winding.
1st Primary Insulation Layer	Add 1 layer of tape, Item [8], above WD1-1st Primary Winding.
WD2: Bias & WD3: Shield1 Winding	Use 4 wires of Item [4]. Starting at pin 6 for WD2-Bias Winding. Also use 4 wires of same Item [4] starting at pin 4 for WD3-Shield1 Winding. Wind all 8 wires in parallel, at the 4th turn: - bring 4 wires for WD2-Bias Winding to the left then terminate at pin 4, - cut short 4 wires for WD3-Shield1 Winding as No-Connect.
Bias & Shield1 Insulation Layer	Add 1 layer of tape, Item [8], above WD2-Bias and WD3-Shield1 Winding.
WD4 & WD5 Secondary1 & Secondary2 Winding	Use wire of Item [6]. Starting at pin 11, wind 4 bi-filar turns from left to right. At the last turn exit at right slot and leave ~ 25mm of wires floating for WD4-Secondary1 Winding. Repeat winding same as above for WD5-Secondary2 Winding.
Secondary1 & Secondary2 Insulation Layer	Add 1 layer of tape, Item [8], above WD4-Secondary1 and WD5-Secondary2 Winding.
WD6 Shield2 Winding	Use wire of Item [5]. Starting at pin 4, wind 10 quad-filar turns from left to right. At the last turn, cut short to leave as No-Connect.
Shield2 Insulation Layer	Add 1 layer of tape, Item [8], above Shield2 Winding.
WD7 2nd Primary Winding	Use the floating wire from WD1-1st Primary Winding. Wind 15 turns from left to right. At the last turn, bring the wire back to left and finish at pin 1.
2nd Primary Insulation Layer	Add 1 layer of tape, Item [8], above WD7-2nd Primary Winding.
Finish	Bring the 4 wires floating from WD4-Secondary1 Winding and WD5-Secondary2 Winding to left and terminate at pin 8. Gap core halves to get 620 μH. Use tape, Item [9], to cover one side of core as shown in the picture below, only for bottom secondary side. Solder pin 4 with bus-wire, Item [7] then lean along core halves and secure with tape. Use 2 layers of tape, Item [9], horizontally to secure the cores. Varnish with Item [11]. Use a wide tape, Item [10], to envelop bottom and secondary side part of the bobbin.

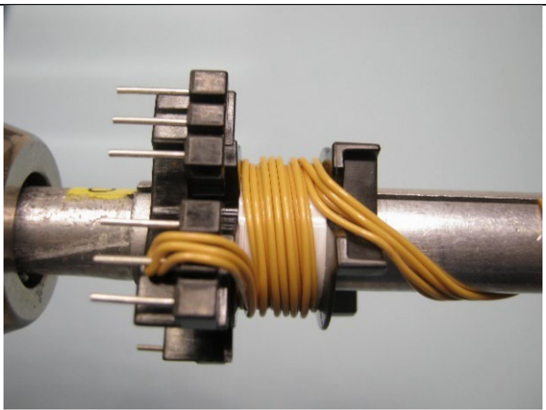
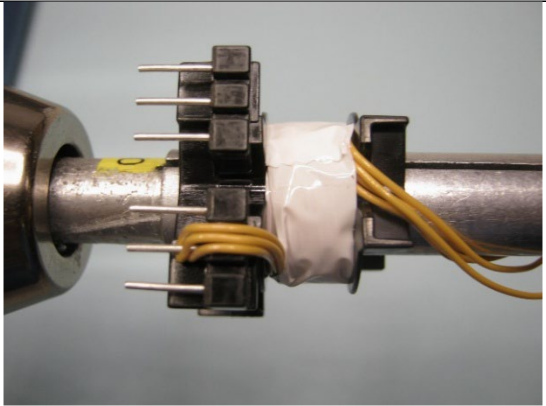
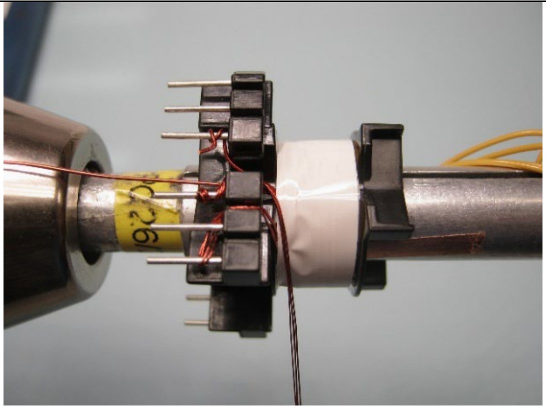
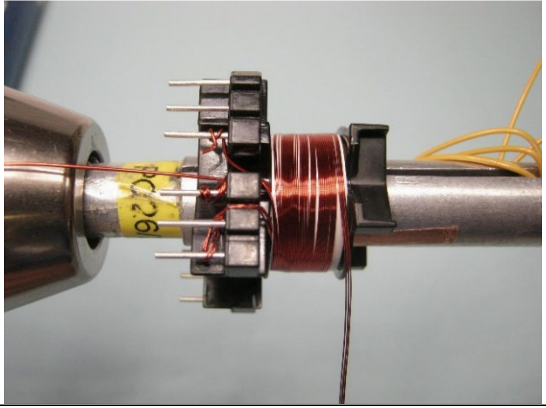
Table 6 – Transformer Instructions

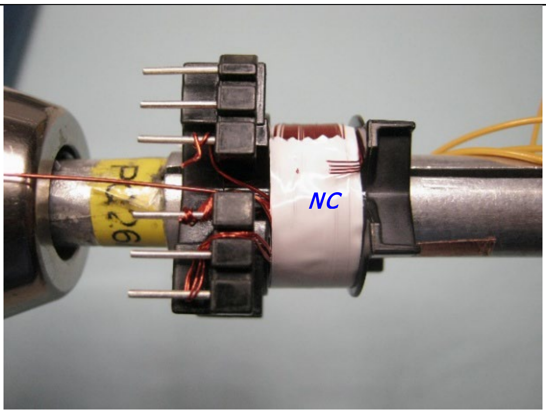
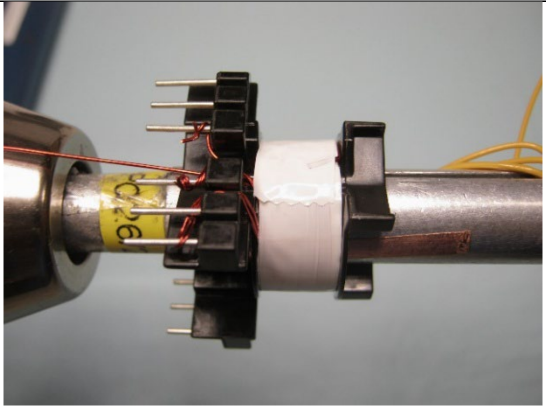
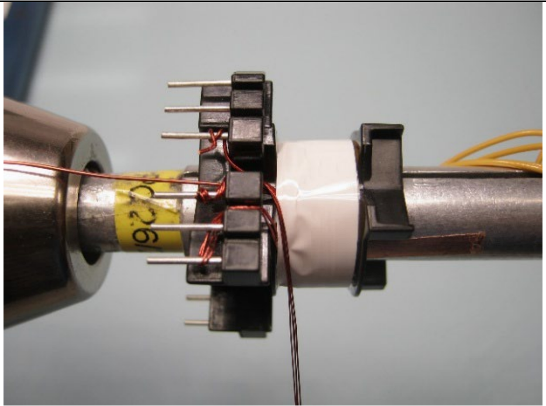
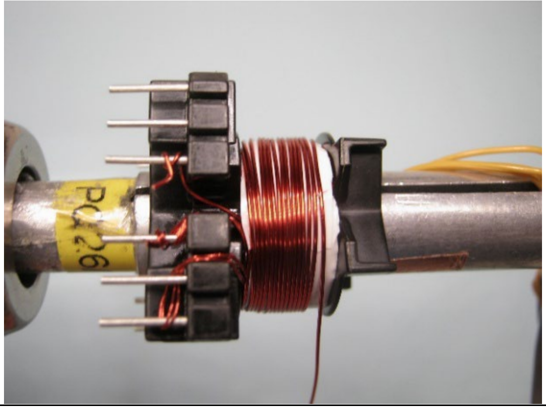
7.6 Winding Illustrations

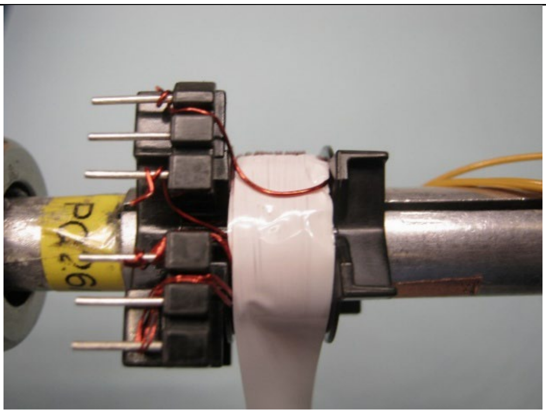
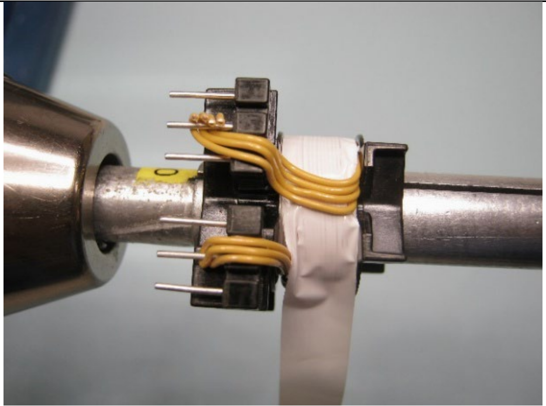
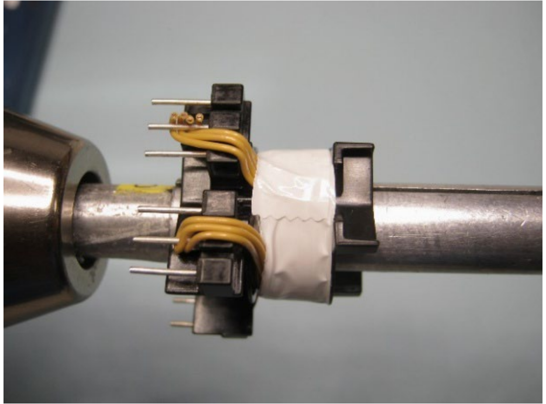
Winding preparation		Position the bobbin, Item [2], on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise (CW) for forward direction.
WD1 **1st Primary Winding**	  	Use wire of Item [3]. Starting at pin 3, wind 19 turns (1 layer), with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire floating for WD7-2nd Primary Winding.

1st Primary Insulation Layer		Add 1 layer of tape, Item [8], above WD1-1st Primary Winding.
WD2: Bias & WD3: Shield1 Winding		Use 4 wires of Item [4]. Starting at pin 6 for WD2-Bias Winding. Also use 4 wires of same Item [4], starting at pin 4 for WD3-Shield1 Winding. Wind all 8 wires in parallel, at the 4th turn: - bring 4 wires for WD2-Bias Winding to the left then terminate at pin 4, - cut short 4 wires for WD3-Shield1 Winding as No-Connect.

Bias and Shield1 Insulation Layer		Add 1 layer of tape, Item [8], above WD2-Bias and WD3-Shield1 Winding.
WD4 & WD5 Secondary1 & Secondary2 Winding		Use wire of Item [6]. Starting at pin 11, wind 4 bi-filar turns from left to right. At the last turn exit at right slot and leave ~ 25mm of wires floating for WD4 -Secondary1 Winding. Repeat winding same as above for WD5-Secondary2 Winding.

		
Secondary 1 and Secondary 2 Insulation Layer		Add 1 layer of tape, Item [8], above WD4-Secondary1 and WD5-Secondary2 Winding.
WD6 Shield2 Winding	 	Use wire, Item [5]. Starting at pin 4, wind 10 quad-filar turns from left to right. At the last turn, cut short to leave as No-Connect.

		
Shield 2 Insulation Layer		Add 1 layer of tape, Item [8], above Shield2 Winding.
WD7 **2nd Primary Winding**	 	Use the floating wire from WD1-1st Primary Winding. Wind 15 turns from left to right. At the last turn, bring the wire back to left and finish at pin 1.

		
Finish	  	Add 1 layer of tape, Item [8], above WD7-2nd Primary Winding. Bring the 4 wires floating from WD4-Secondary1 Winding and WD5-Secondary2 Winding to left and terminate at pin 8. Gap core halves to get 620μH. Use tape, Item [9], to cover one side of core as shown in the picture beside, only for bottom secondary side. Solder pin 4 with bus-wire, Item [7] then lean along core halves and secure with tape. Use 2 layers of tape, Item [9], horizontally to secure the cores. Varnish with Item [11]. Use a wide tape, Item [10] to envelop bottom and secondary side part of the bobbin.

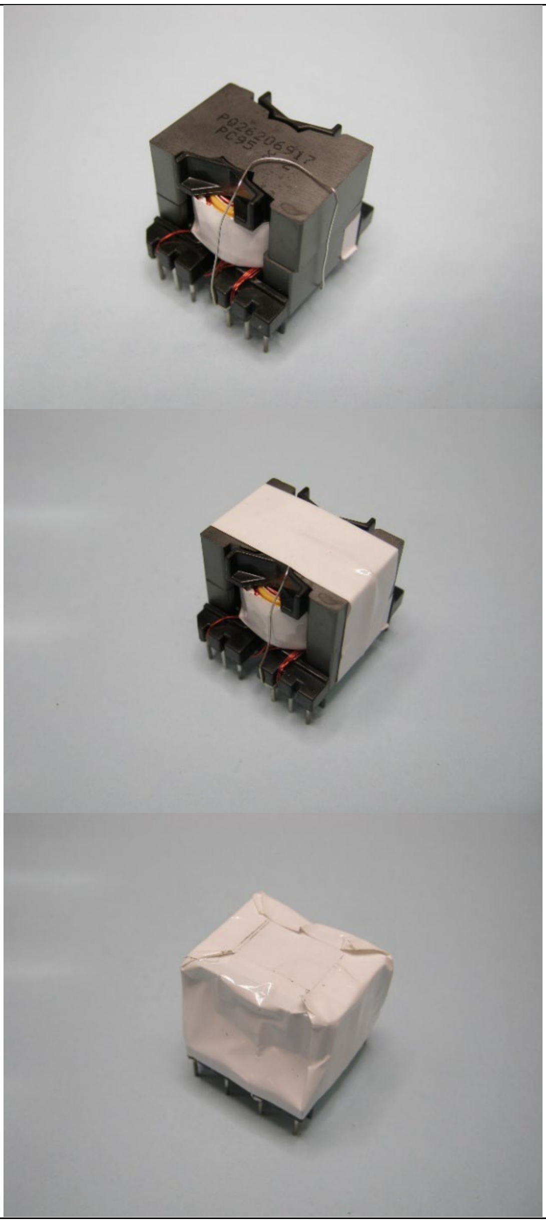
		

Table 7 – Transformer Winding Instructions

8 Transformer Design Spreadsheet

1	**ACDC_InnoSwitch3-EP1250V_Flyback_011224; Rev.1.0; Copyright Power Integrations 2024**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch3-EP 1250 V Flyback Design Spreadsheet**
2	Application Variables					**Design Title**
3	VIN_MIN	90		90	V	Minimum AC input voltage
4	VIN_MAX	480		480	V	Maximum AC input voltage
5	VIN_RANGE			WIDE RANGE UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	220.0		220.0	mF	Input capacitor
8	VOUT			12.00	V	Output voltage at the board
9	PERCENT_CDC			0		Cable drop compensation desired at full load
10	IOUT	5.000		5.000	A	Output current
11	POUT			60.00	W	Output power
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE			OPEN FRAME		Power supply enclosure
15	Primary Controller Selection					
16	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
17	DEVICE_GENERIC	AUTO		INN36X9C		Generic device code
18	DEVICE_CODE			INN3629C		Actual device code
19	POUT_MAX			75	W	Power capability of the device based on thermal performance
20	RDSON_100DEG			0.58	Ω	Primary switch on time drain resistance at 100 °C
21	ILIMIT_MIN			1.980	A	Minimum current limit of the primary switch
22	ILIMIT_TYP			2.130	A	Typical current limit of the primary switch
23	ILIMIT_MAX			2.279	A	Maximum current limit of the primary switch
24	VDRAIN_BREAKDOWN			1250	V	Device breakdown voltage
25	VDRAIN_ON_PRSW			0.34	V	Primary switch on time drain voltage
26	VDRAIN_OFF_PRSW			802.4	V	Peak drain voltage on the primary switch during turn-off
27	Worst Case Electrical Parameters					
28	FSWITCHING_MAX	66500		66500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
29	VOR	100.0		100.0	V	Secondary voltage reflected to the primary when the primary switch turns off

30	VMIN			109.36	V	Valley of the minimum input AC voltage at full load
31	KP			0.69		Measure of continuous/discontinuous mode of operation
32	MODE_OPERATION			CCM		Mode of operation
33	DUTYCYCLE			0.478		Primary switch duty cycle
34	TIME_ON			11.46	ms	Primary switch on-time
35	TIME_OFF			7.84	ms	Primary switch off-time
36	LPRIMARY_MIN			590.8	mH	Minimum primary inductance
37	LPRIMARY_TYP			621.9	mH	Typical primary inductance
38	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
39	LPRIMARY_MAX			653.0	mH	Maximum primary inductance
40	PRIMARY CURRENT					
41	IPEAK_PRIMARY			2.076	A	Primary switch peak current
42	IPEDESTAL_PRIMARY			0.578	A	Primary switch current pedestal
43	IAVG_PRIMARY			0.584	A	Primary switch average current
44	IRIPPLE_PRIMARY			1.709	A	Primary switch ripple current
45	IRMS_PRIMARY			0.911	A	Primary switch RMS current
46	SECONDARY CURRENT					
47	IPEAK_SECONDARY			17.644	A	Secondary winding peak current
48	IPEDESTAL_SECONDARY			4.913	A	Secondary winding current pedestal
49	IRMS_SECONDARY			8.086	A	Secondary winding RMS current
50	Transformer Construction Parameters					
51	CORE SELECTION					
52	CORE	PQ26		PQ26		Core selection
53	CORE CODE			PQ26/20-3C95		Core code
54	AE			121.00	mm^2	Core cross sectional area
55	LE			45.00	mm	Core magnetic path length
56	AL			7020	nH/turns^2	Ungapped core effective inductance
57	VE			5470.0	mm^3	Core volume
58	BOBBIN			PQ26/20 - 2 (P6-S6)		Bobbin
59	AW			31.10	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
60	BW			9.00	mm	Bobbin width
61	BH			4.78	mm	Bobbin height
62	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
63	Primary Winding					
64	NPRIMARY			34		Primary turns
65	BPEAK			3702	Gauss	Peak flux density
66	BMAX			3249	Gauss	Maximum flux density
67	BAC			1310	Gauss	AC flux density (0.5 x Peak to Peak)
68	ALG			538	nH/turns^2	Typical gapped core effective inductance

69	LG			0.261	mm	Core gap length
70	LAYERS_PRIMARY			2		Number of primary layers
71	AWG_PRIMARY			25	AWG	Primary winding wire AWG
72	OD_PRIMARY_INSULATED			0.518	mm	Primary winding wire outer diameter with insulation
73	OD_PRIMARY_BARE			0.455	mm	Primary winding wire outer diameter without insulation
74	CMA_PRIMARY			352	Cmil/A	Primary winding wire CMA
75	Secondary Winding					
76	NSECONDARY	4		4		Secondary turns
77	AWG_SECONDARY			18	AWG	Secondary winding wire AWG
78	OD_SECONDARY_INSULATED			1.328	mm	Secondary winding wire outer diameter with insulation
79	OD_SECONDARY_BARE			1.024	mm	Secondary winding wire outer diameter without insulation
80	CMA_SECONDARY			201	Cmil/A	Secondary winding wire CMA
81	Bias Winding					
82	NBIAS			4		Bias turns
83	Primary Components Selection					
84	Line Undervoltage					
85	BROWN-IN REQURED			81.0	V	Required AC RMS line voltage brown-in threshold
86	RLS			7.48	MΩ	Connect two 3.74 MOhm resistors to the V-pin for the required UV/OV threshold
87	BROWN-IN ACTUAL			45.0 - 80.0	V	Actual AC RMS brown-in range
88	BROWN-OUT ACTUAL			29.8 - 65.5	V	Actual AC RMS brown-out range
89	Line Overvoltage					
90	OV_TARGET			482.4	V	AC RMS line voltage at which overvoltage will trigger. For High Line designs, brown-in threshold might need to be lowered to get the required overvoltage
91	RV_BIAS_ENABLED	AUTO		YES		Resistor between BPP and V pins to increase Line OV threshold without increasing Line UV
92	RV_BIAS			280	kΩ	Biasing resistor between BPP and V pins of the device
93	OVERVOLTAGE_LINE			488 - 573	V	Actual AC RMS line over-voltage range
94	Bias Diode					
95	VBIAS	9.0	Info	9.0	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 10V
96	VF_BIAS			0.70	V	Bias winding diode forward drop
97	VREVERSE_BIASDIODE			88.70	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
98	CBIAS			22	mF	Bias winding rectification capacitor
99	CBPP			4.70	mF	BPP pin capacitor
100	Secondary Components					

101	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
102	RFB_LOWER			11.80	kΩ	Lower feedback resistor
103	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
104	Multiple Output Parameters					
105	OUTPUT 1					
106	VOUT1			12.00	V	Output 1 voltage
107	IOUT1			5.00	A	Output 1 current
108	POUT1			60.00	W	Output 1 power
109	IRMS_SECONDARY1			8.086	A	Root mean squared value of the secondary current for output 1
110	IRIPPLE_CAP_OUTPUT1			6.355	A	Current ripple on the secondary waveform for output 1
111	NSECONDARY1			4		Number of turns for output 1
112	VREVERSE_RECTIFIER1			91.70	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
113	SRFET1	AUTO		AON7254		Secondary rectifier (Logic MOSFET) for output 1
114	VF_SRFET1			0.330	V	SR FET on-time drain voltage for output 1
115	VBREAKDOWN_SRFET1			150	V	SR FET breakdown voltage for output 1
116	RDSON_SRFET1			66.0	mΩ	SR FET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1

Table 8 – Transformer Design Spreadsheet

9 Performance Data

All performance data was measured on the board unless otherwise noted.

9.1 Full-load Efficiency vs. Line

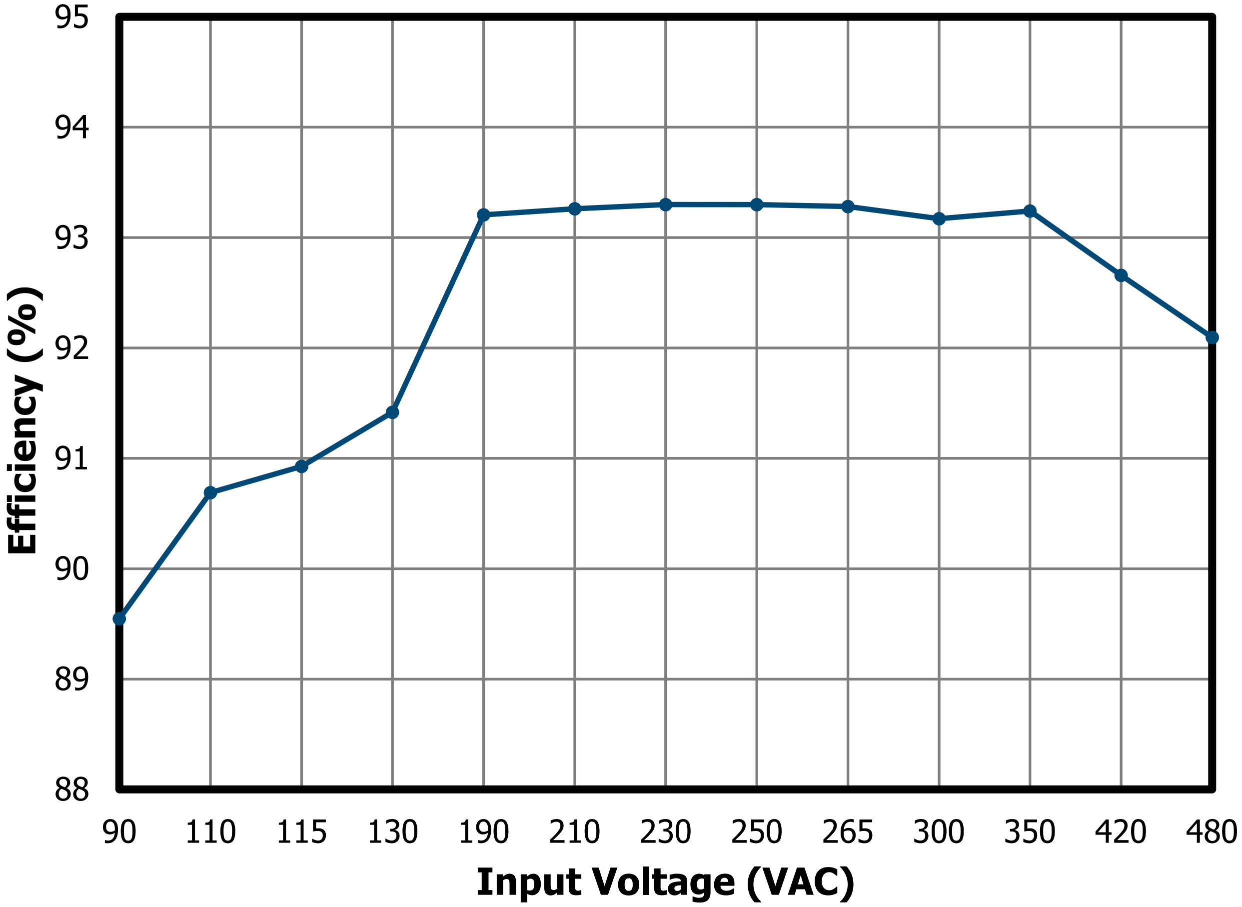


Figure 8 – Full-load Efficiency vs. Line, Room Temperature

9.2 Efficiency vs. Load

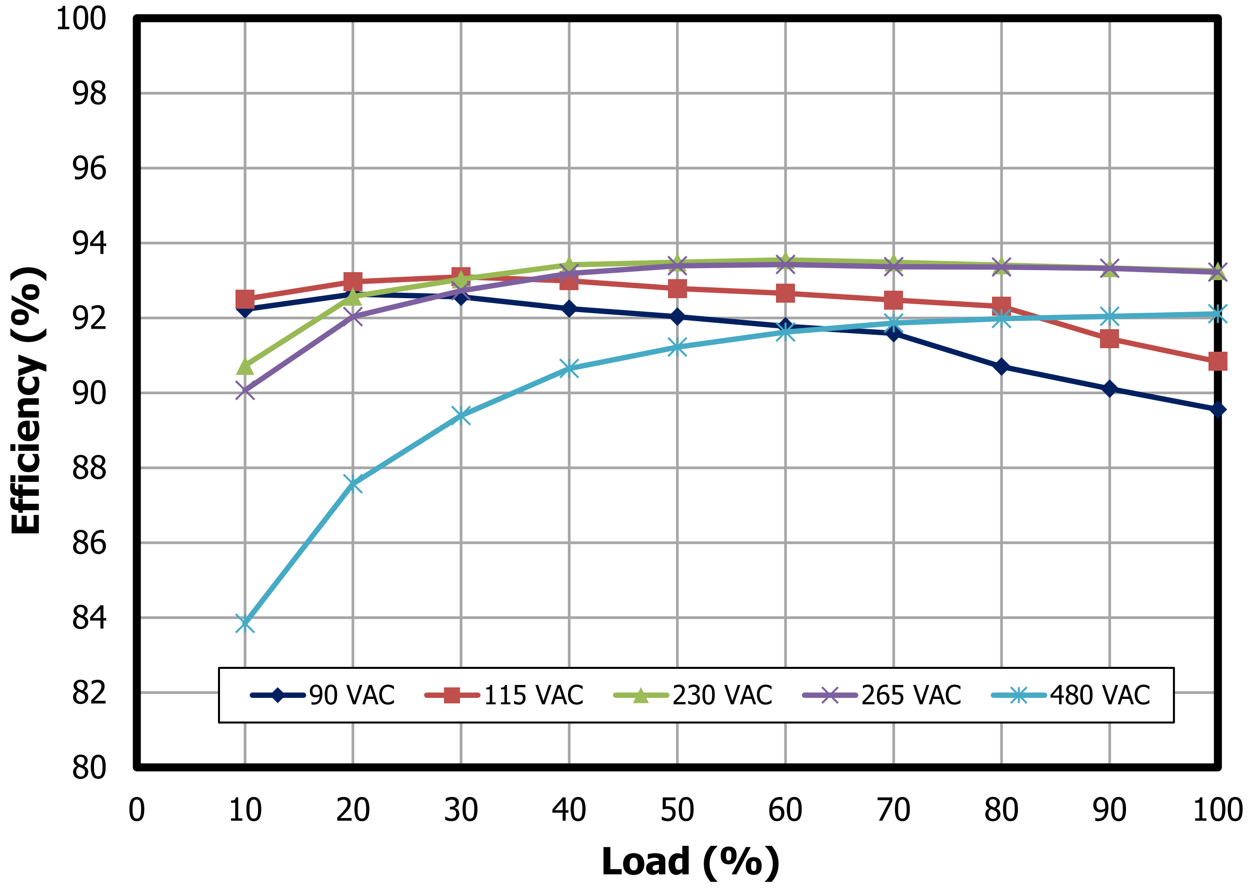


Figure 9 – Efficiency vs. Load, Room Temperature

9.3 Average Efficiency

Output Voltage (V)	Test Power [W]	Average DOE6 Limit (%)	Average CoC v5 Tier 2 (%)	10% Load CoC v5 Tier 2 (%)
12	60	88.0	89.0	79.0

Table 9 - Average Efficiency - International Standards

9.3.1 Average and 10% Efficiency at 90 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	66.6	59.7	89.6	91.4
75	49.4	45.1	91.3	
50	32.7	30.1	92.1	
25	16.3	15.1	92.6	
10	6.55	6.04	92.3	

Table 10 – Average and 10% Efficiency at 90 VAC

9.3.2 Average and 10% Efficiency at 115 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	65.9	59.9	90.9	92.3
75	48.8	45.1	92.4	
50	32.5	30.2	92.8	
25	16.3	15.1	93.1	
10	6.54	6.04	92.4	

Table 11 – Average and 10% Efficiency at 115 VAC

9.3.3 Average and 10% Efficiency at 230 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	64.4	60.0	93.2	92.2
75	48.5	45.3	93.4	
50	32.3	30.2	93.5	
25	16.3	15.2	92.8	
10	6.66	6.03	90.6	

Table 12 – Average and 10% Efficiency at 230 VAC

9.3.4 Average and 10% Efficiency at 265 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	64.7	60.3	93.2	93.1
75	48.6	45.4	93.3	
50	32.4	30.2	93.4	
25	16.4	15.1	92.5	
10	6.72	6.03	89.8	

Table 13 – Average and 10% Efficiency at 230 VAC

9.3.5 Average and 10% Efficiency at 480 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	65.1	60.1	92.4	91.2
75	49.3	45.4	92.1	
50	33.1	30.3	91.4	
25	17.1	15.2	88.8	
10	7.19	6.06	84.3	

Table 14 – Average and 10% Efficiency at 480 VAC

9.4 No-Load Input Power

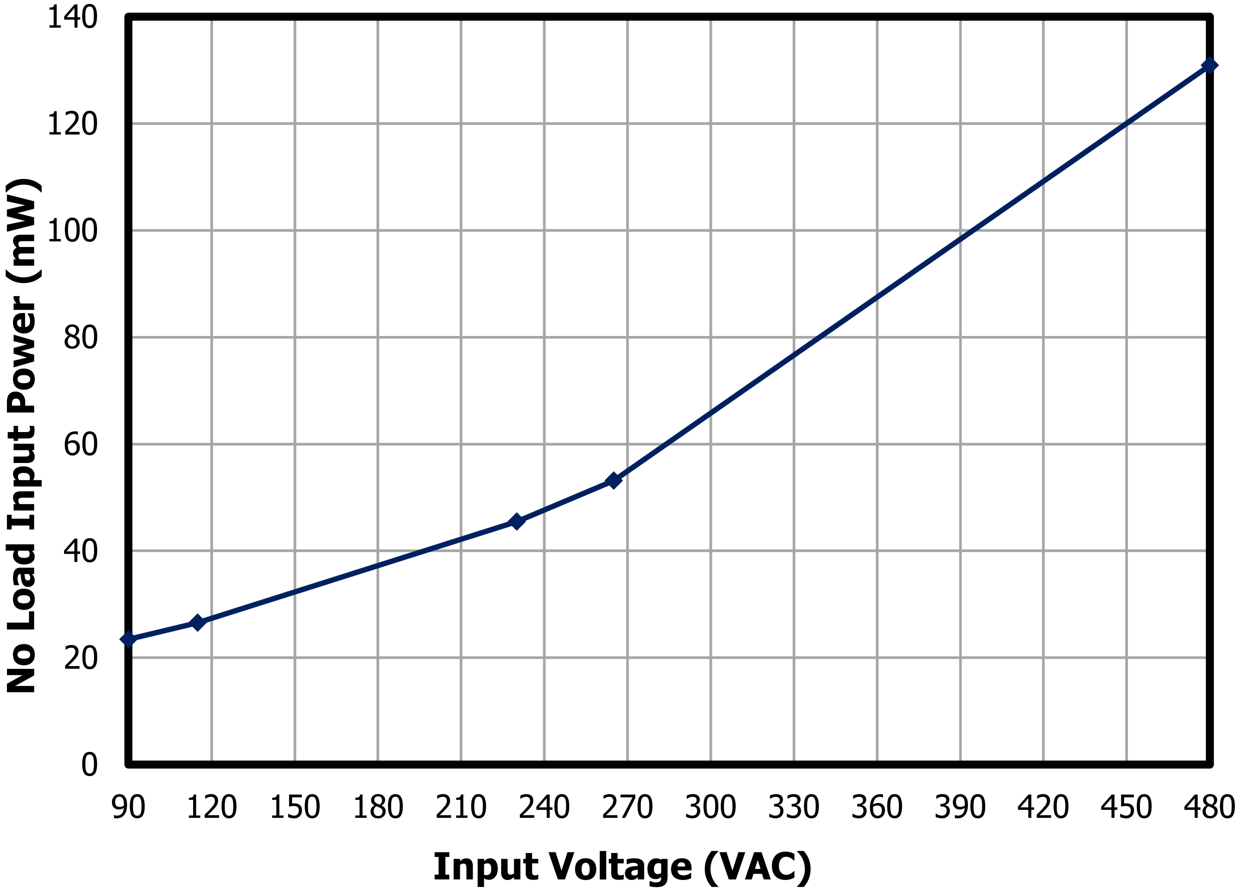


Figure 10 – No-Load Input Power vs. Input Line Voltage, Room Temperature

9.5 Line Regulation (Full Load)

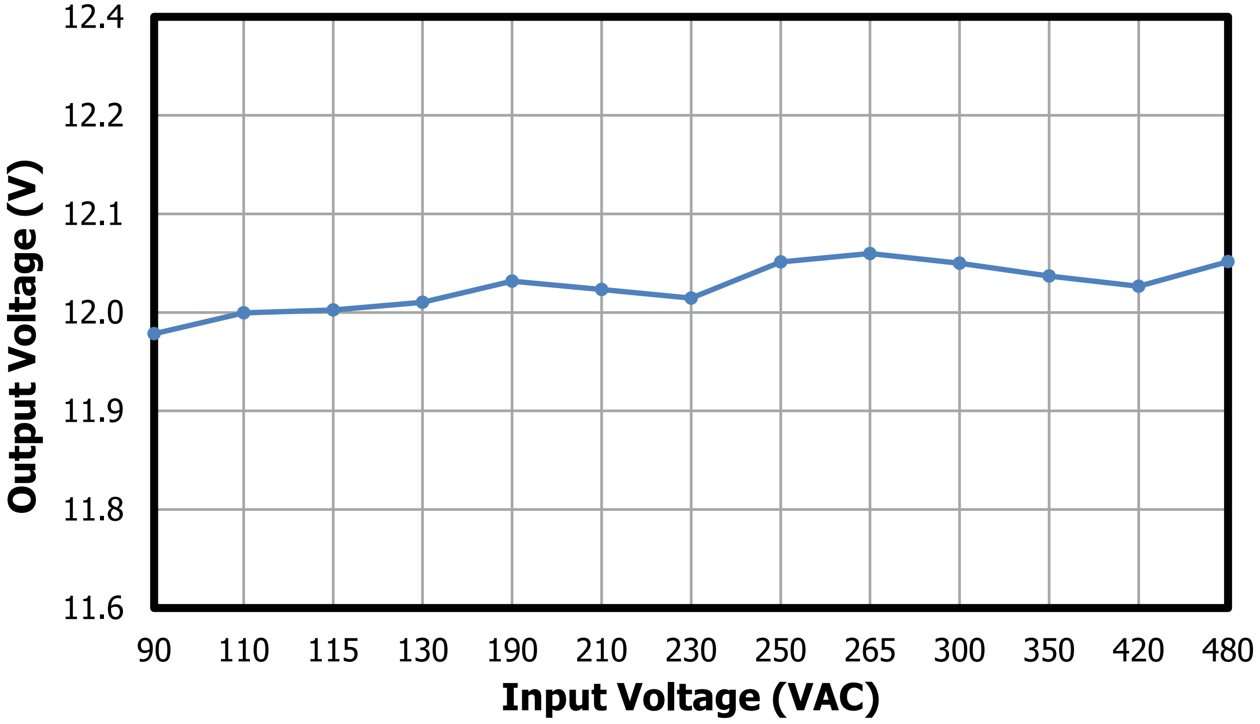


Figure 11 – Line Regulation - Full Load

9.6 Load Regulation

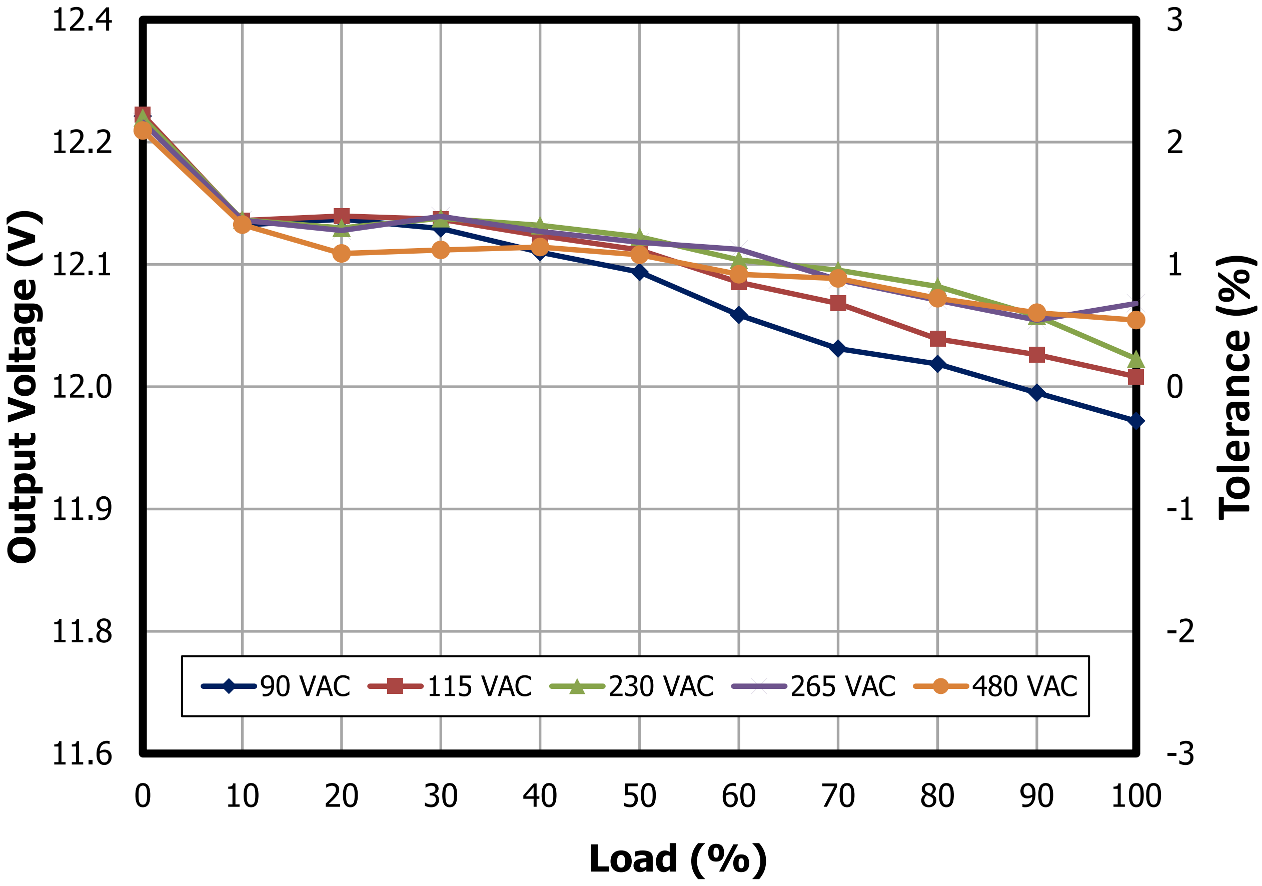


Figure 12 – Load Regulation

9.7 Standby Output Power

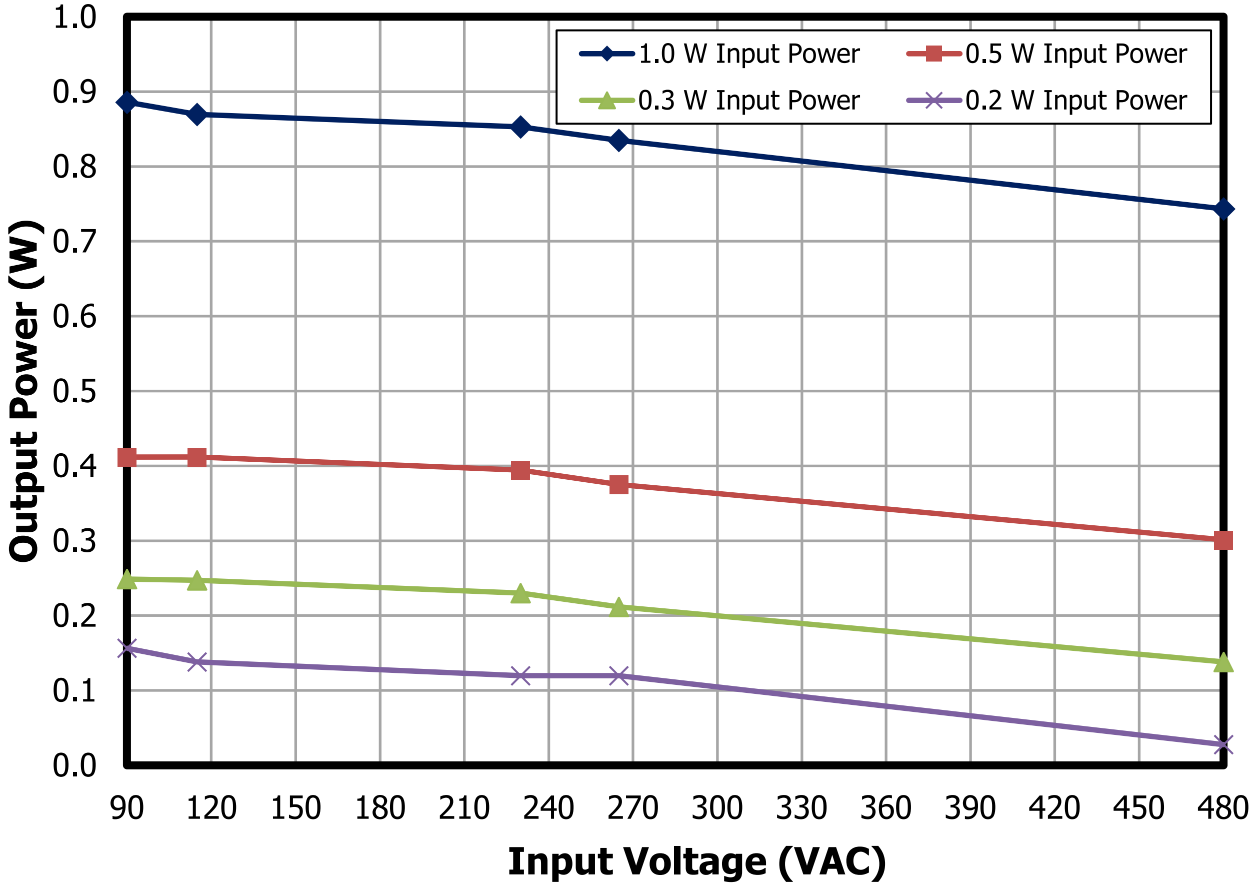
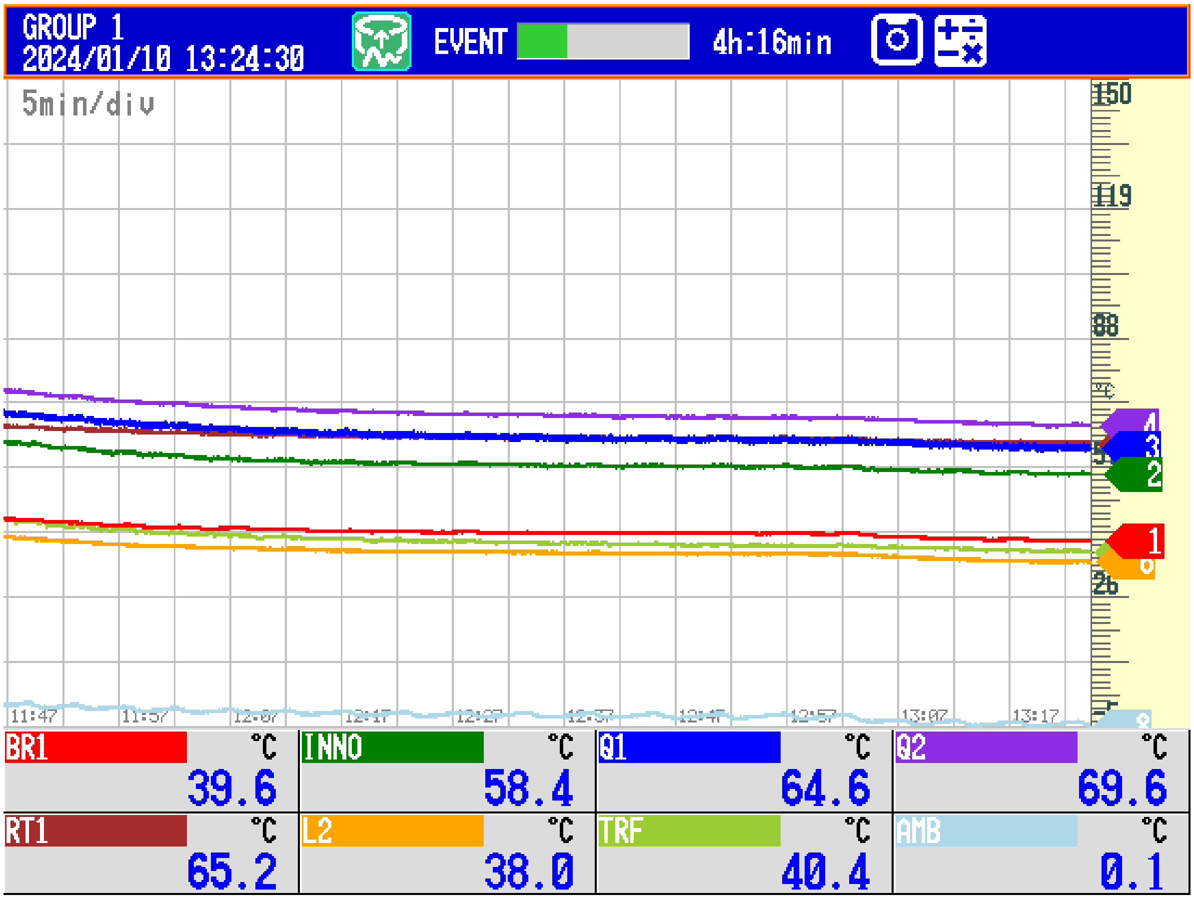


Figure 13 – Load Regulation

10 Thermal Performance

The Temperature of key components was measured with the power supply positioned inside a thermal chamber at ambient temperatures of 0 °C, 25 °C and 40 °C. Temperatures were recorded over time using a data logger. The test was continued until thermal equilibrium was achieved.

10.1 90 VAC, 60 W at 0 °C Ambient



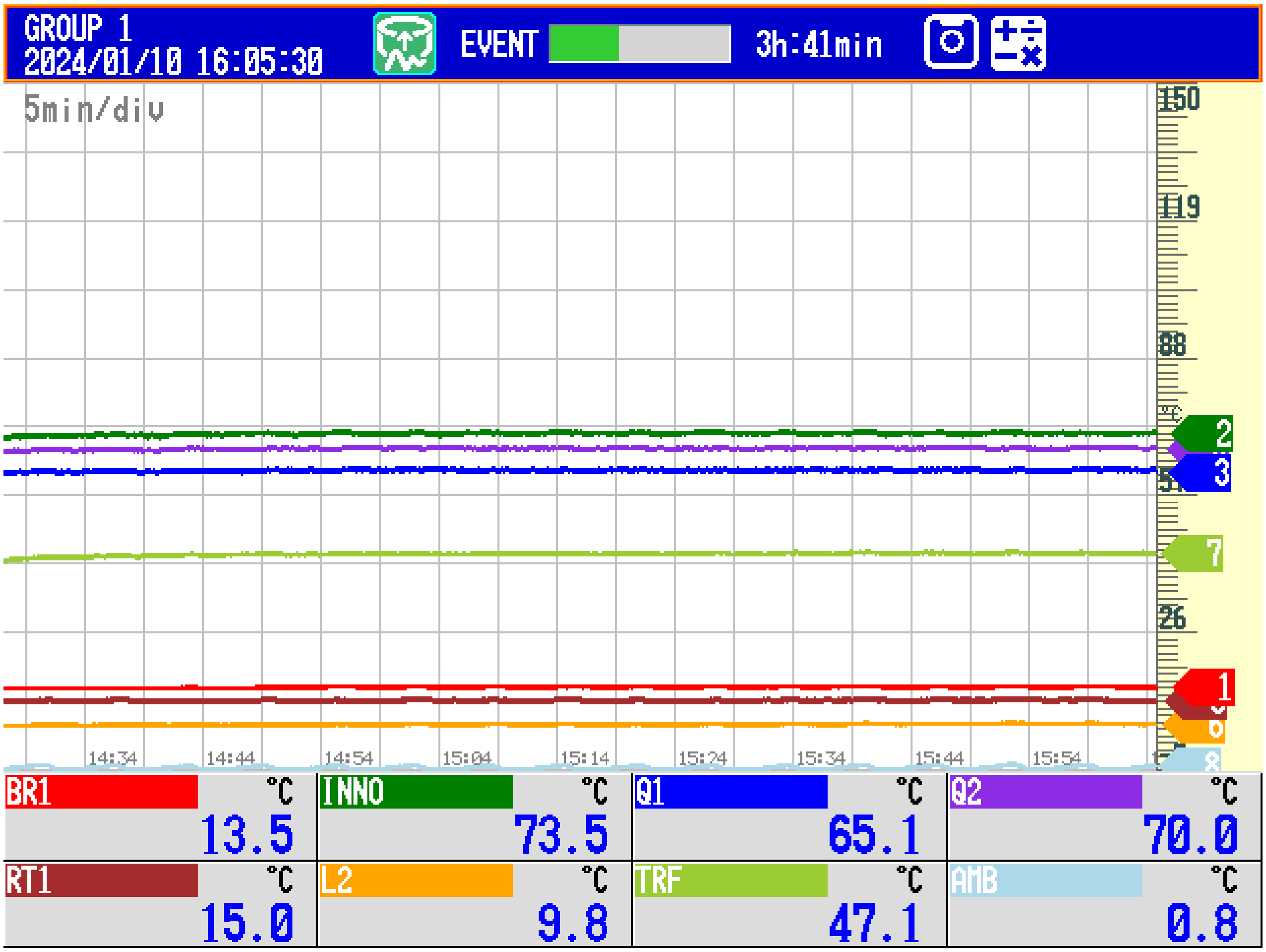
BR1 °C	INNO °C	Q1 °C	Q2 °C
39.6	58.4	64.6	69.6
RT1 °C	**L2 °C**	**TRF °C**	**AMB °C**
65.2	38.0	40.4	0.1

Figure 14 – Thermal Performance at 90 VAC Input

Component	Temperature (°C)
Bridge Diode (BR1)	39.6
InnoSwitch (U2)	58.4
SR FET (Q1)	64.6
SR FET (Q2)	69.6
Thermistor (RT1)	65.2
CMC (L1)	38.0
Transformer Core (T1)	40.4
Ambient	0.1

Table 15 – Temperature Measurement of Critical Components at 0 ºC

10.2 480 VAC, 60 W at 0 °C Ambient



BR1 °C 13.5	INNO °C 73.5	Q1 °C 65.1	Q2 °C 70.0
RT1 °C 15.0	L2 °C 9.8	TRF °C 47.1	AMB °C 0.8

Figure 15 – Thermal Performance at 480 VAC Input

Component	Max. Temperature (°C)
Bridge Diode (BR1)	13.5
InnoSwitch (U2)	73.5
SR FET (Q1)	65.1
SR FET (Q2)	70.0
Thermistor (RT1)	15.0
CMC (L1)	9.8
Transformer Core (T1)	47.1
Ambient	0.8

Table 16 – Temperature Measurement of Critical Components at 0 °C

10.3 90 VAC, 60 W at 25 °C Ambient

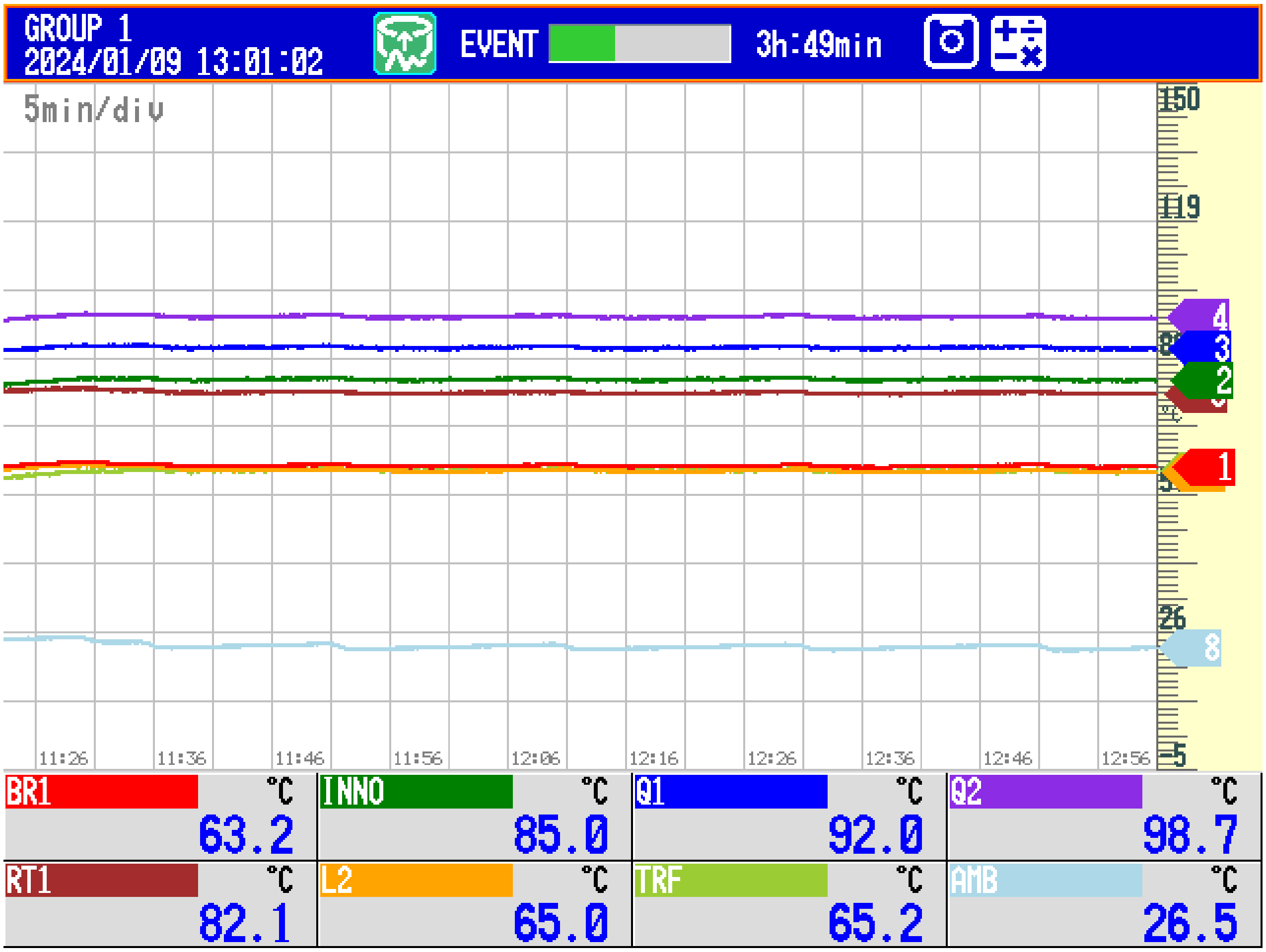
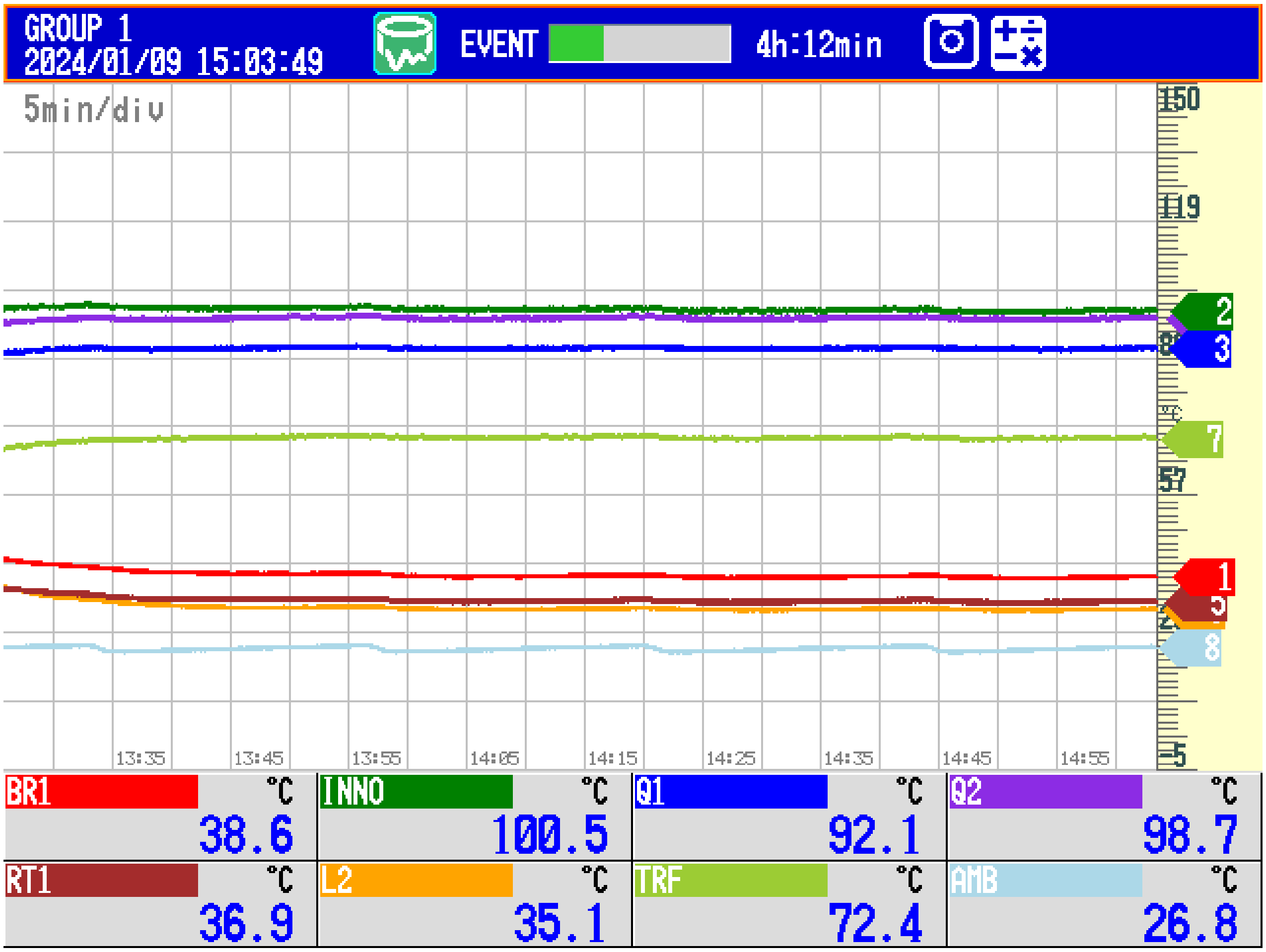


Figure 16 – Thermal Performance at 90 VAC Input

Component	Max. Temperature (°C)
Bridge Diode (BR1)	63.2
InnoSwitch (U2)	85.0
SR FET (Q1)	92.0
SR FET (Q2)	98.7
Thermistor (RT1)	82.1
CMC (L1)	65.0
Transformer Core (T1)	65.2
Ambient	26.5

Table 17 – Temperature Measurement of Critical Components at 25 °C

10.4 480 VAC Input, 60 W at 25 °C Ambient



GROUP 1
2024/01/09 15:03:49

EVENT

4h:12min

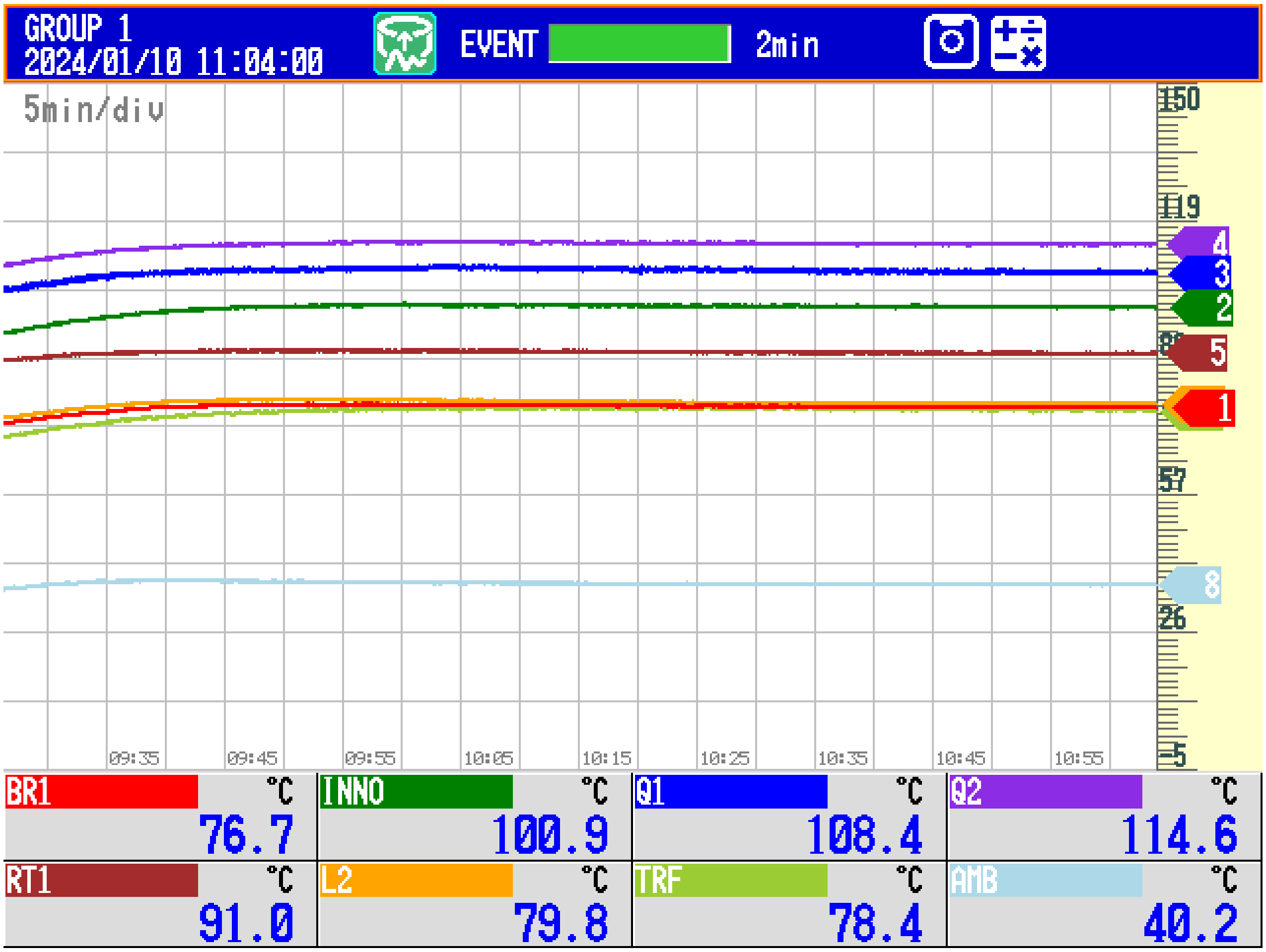
BR1 °C 38.6
INNO °C 100.5
Q1 °C 92.1
Q2 °C 98.7
RT1 °C 36.9
L2 °C 35.1
TRF °C 72.4
AMB °C 26.8

Figure 17 – Thermal Performance at 480 VAC Input

Component	Max. Temperature (°C)
Bridge Diode (BR1)	38.6
InnoSwitch (U2)	101
SR FET (Q1)	92.1
SR FET (Q2)	98.7
Thermistor (RT1)	36.9
CMC (L1)	35.1
Transformer Core (T1)	72.4
Ambient	26.8

Table 18 – Temperature Measurement of Critical Components at 25 °C

10.5 90 VAC Input, 60 W at 40 °C Ambient



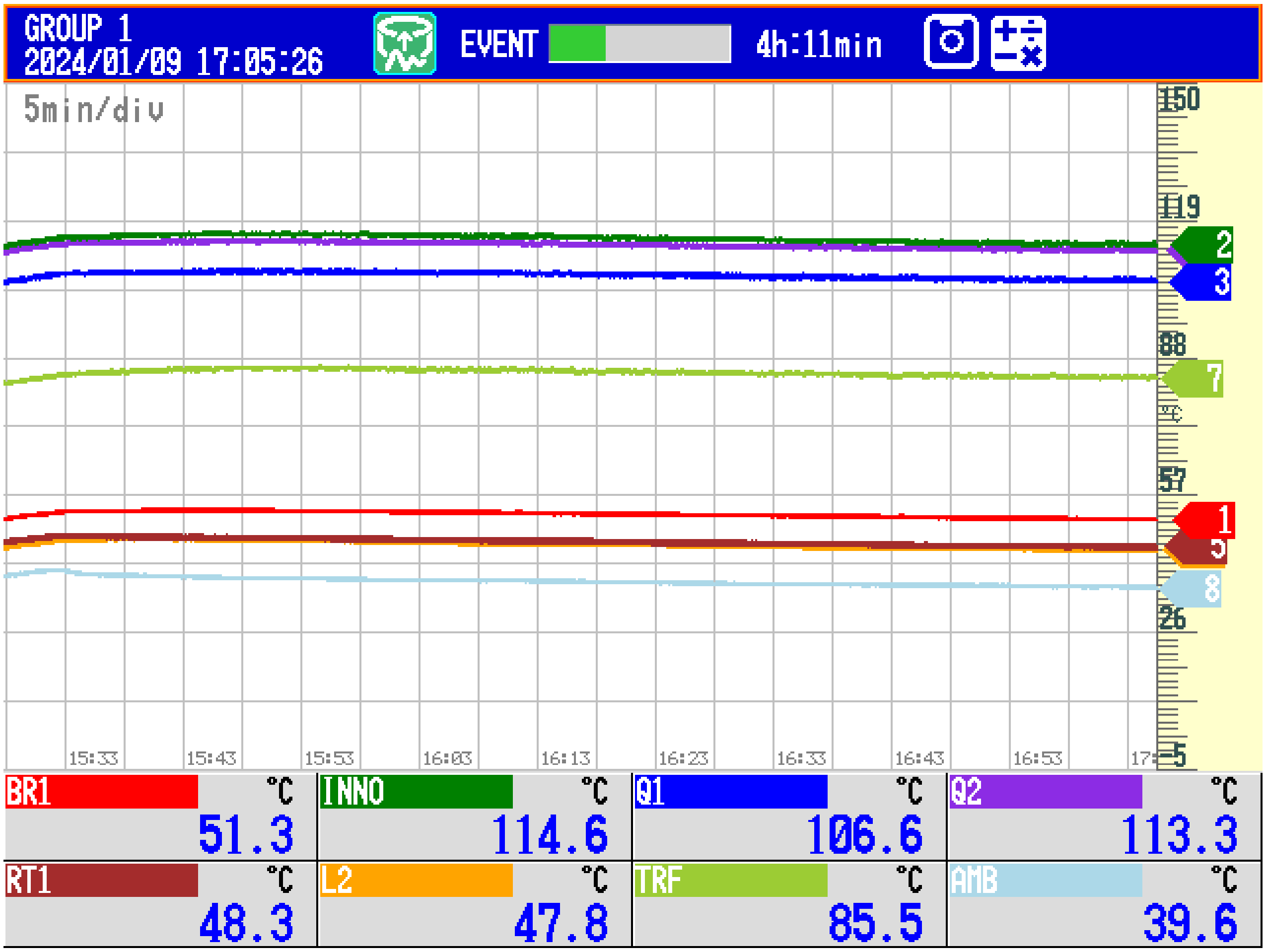
BR1 °C 76.7
INNO °C 100.9
Q1 °C 108.4
Q2 °C 114.6
RT1 °C 91.0
L2 °C 79.8
TRF °C 78.4
AMB °C 40.2

Figure 18 – Thermal Performance at 90 VAC Input

Component	Max. Temperature (°C)
Bridge Diode (BR1)	76.7
InnoSwitch (U2)	101
SR FET (Q1)	108
SR FET (Q2)	115
Thermistor (RT1)	91.0
CMC (L2)	79.8
Transformer Core (T1)	78.4
Ambient	40.2

Table 19 – Temperature Measurement of Critical Components at 40 °C

10.6 480 VAC Input, 60 W at 40 °C Ambient



BR1 °C 51.3

INNO °C 114.6

Q1 °C 106.6

Q2 °C 113.3

RT1 °C 48.3

L2 °C 47.8

TRF °C 85.5

AMB °C 39.6

Figure 19 – Thermal Performance at 480 VAC Input

Component	Max. Temperature (°C)
Bridge Diode (BR1)	51.3
InnoSwitch (U2)	115
SR FET (Q1)	107
SR FET (Q2)	113
Thermistor (RT1)	48.3
CMC (L2)	47.8
Transformer Core (T1)	85.5
Ambient	39.6

Table 20 – Temperature Measurement of Critical Components at 40 °C

11 Waveforms

11.1 Output Voltage Start-up Waveforms at Room Temperature

11.1.1 CC Load

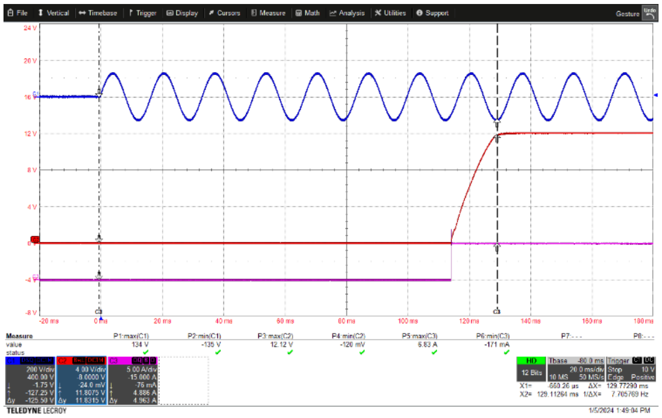


Figure 20 – 90 VAC 60 Hz, I$_O$ = 5 A
CH1: Input Voltage: 200 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.1 V
Output Voltage, Rise Time = 15.1 ms
Start-up Time = 130 ms

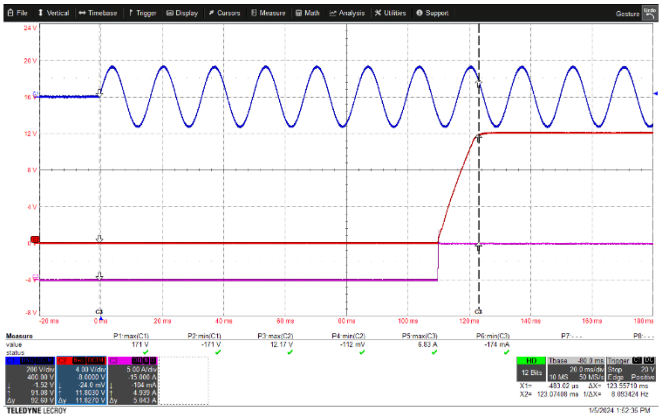


Figure 21 – 115 VAC 60 Hz, I$_O$ = 5 A
CH1: Input Voltage: 200 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.2 V
Output Voltage, Rise Time = 13.5 ms
Start-up Time = 124 ms

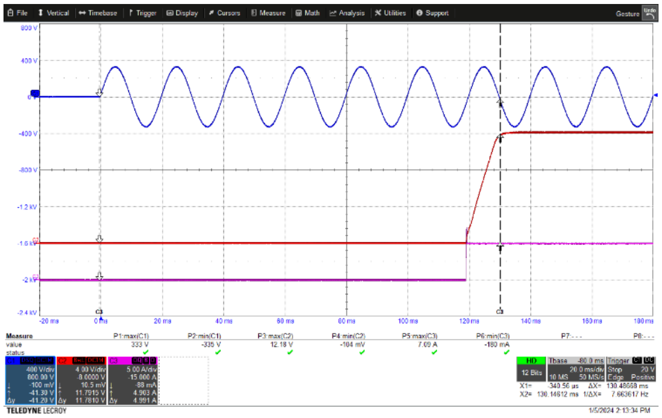


Figure 22 – 230 VAC 60 Hz, I$_O$ = 5 A
CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.2 V
Output Voltage, Rise Time = 11.3 ms
Start-up Time = 130 ms

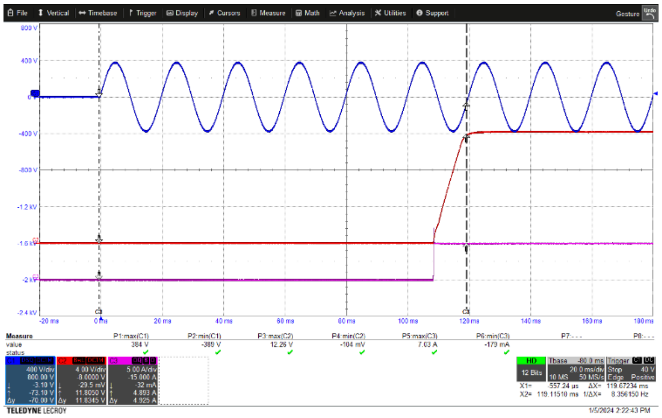


Figure 23 – 265 VAC 60 Hz, I$_O$ = 5 A
CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Zoom: 5 ms / div
Output Voltage, Max. = 12.3 V
Output Voltage, Rise Time = 11 ms
Start-up Time = 120 ms

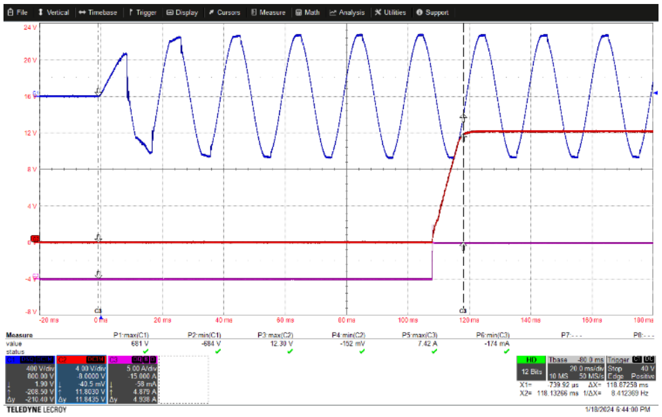


Figure 24 – 480 VAC 60 Hz, I_O = 5 A

CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.2 V
Output Voltage, Rise Time = 10.3 ms
Start-up Time = 119 ms

11.1.2 CR Load

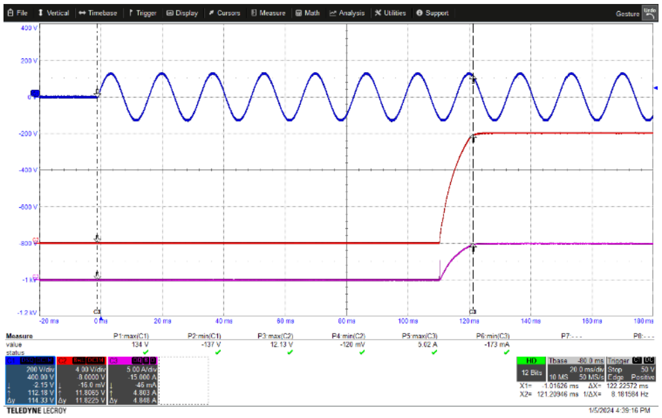


Figure 25 – 90 VAC 60 Hz, R_O= 2.4 Ω (Full-Load, CR).

CH1: Input Voltage: 200 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.1 V
Output Voltage, Rise Time = 11.2 ms
Start-up Time = 122 ms

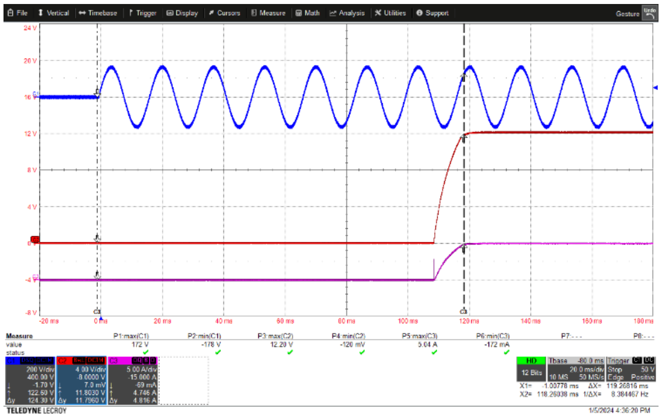


Figure 26 – 115 VAC 60 Hz, R_O= 2.4 Ω (Full-Load, CR).

CH1: Input Voltage: 200 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max = 12.2 V
Output Voltage, Rise Time = 10.1 ms
Start-up Time = 119 ms

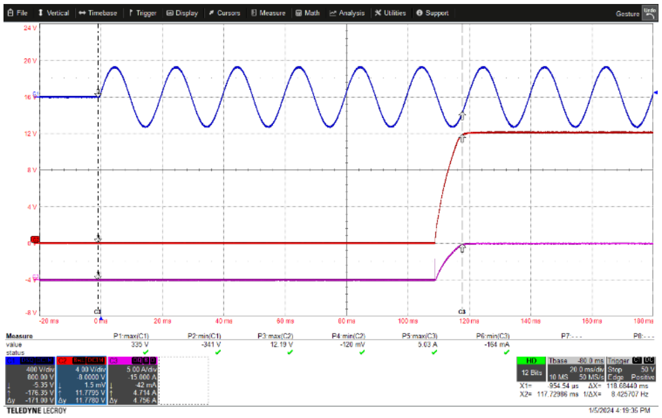


Figure 27 – 230 VAC 60 Hz, R_O = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.2 V
Output Voltage, Rise Time = 9.20 ms
Start-up Time = 119 ms

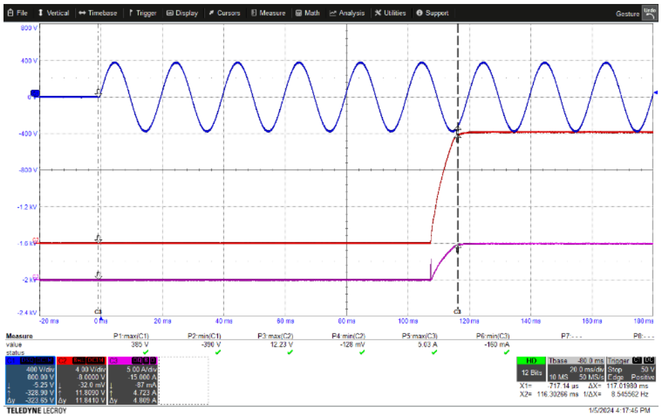


Figure 28 – 265 VAC 60 Hz, R_O = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.2 V
Output Voltage, Rise Time = 8.86 ms
Start-up Time = 117 ms

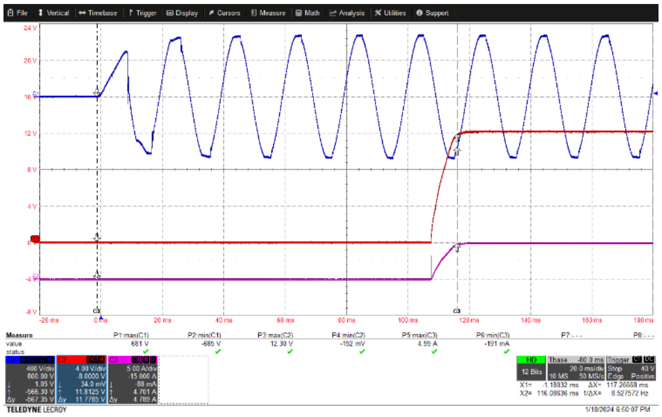


Figure 29 – 480 VAC 60 Hz, R_O = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div
CH2: Output Voltage: 4 V / div., 20 ms / div
CH3: Output Current: 5 A / div., 20 ms / div
Output Voltage, Max. = 12.3 V
Output Voltage, Rise Time = 8.67 ms
Start-up Time = 117 ms

11.2 Load Transient Response

11.2.1 0 – 100 % Load Step

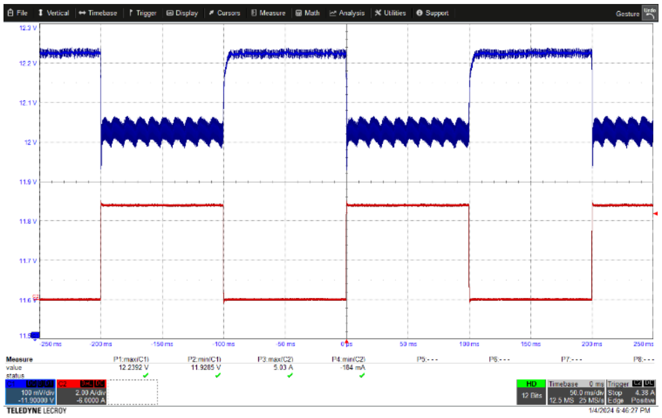


Figure 30 – 90 VAC; I_O = 0 A – 5 A (0-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 11.9 V

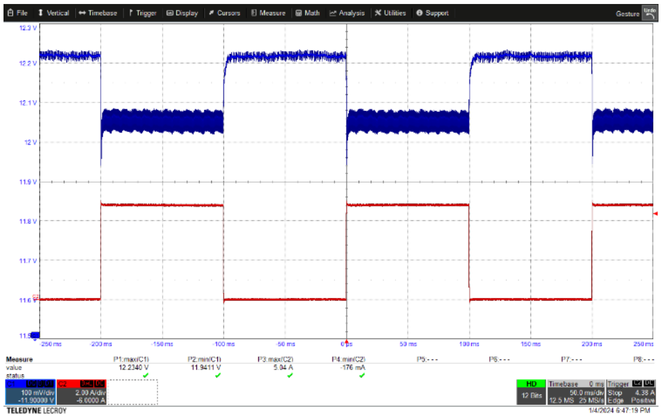


Figure 31 – 115 VAC; I_O = 0 A – 5 A (0-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 11.9 V

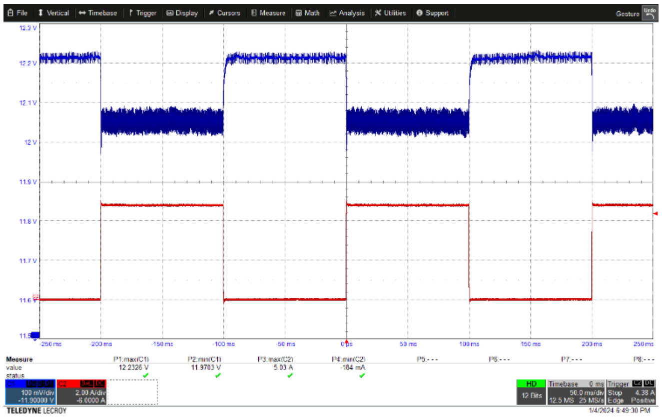


Figure 32 – 230 VAC; I_O = 0 A – 5 A (0-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 12 V

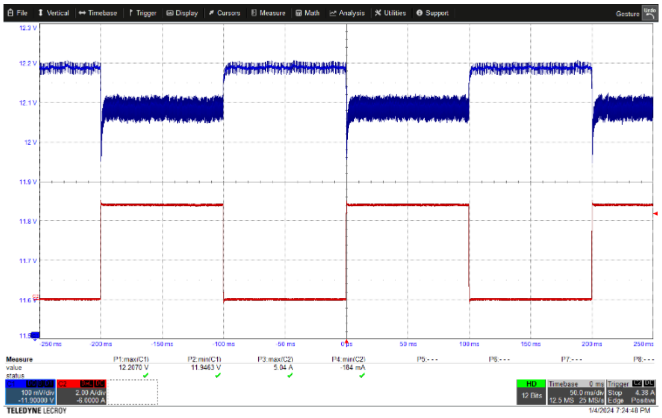
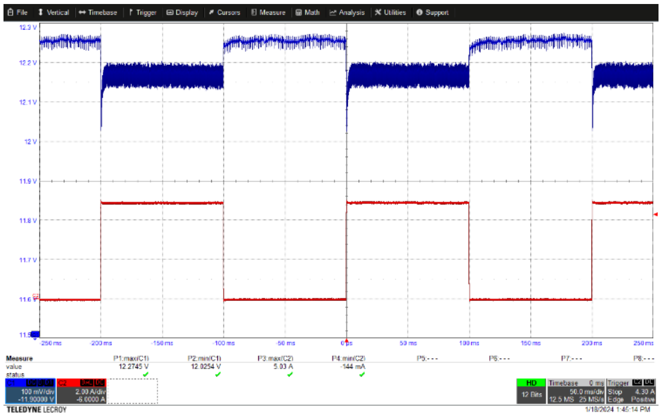


Figure 33 – 265 VAC; I_O = 0 A – 5 A (0-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 12 V



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.2745 V	12.0254 V	5.03 A	-144 mA				
status	✓	✓	✓	✓				

Figure 34 – 480 VAC; I$_O$ = 0 A – 5 A (0-100%) Load Step

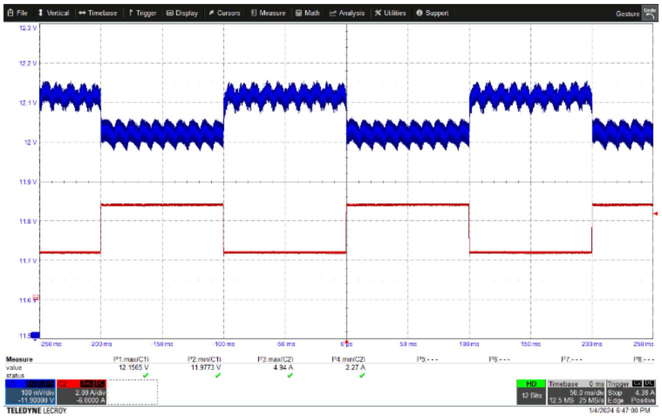
CH1: Output Voltage: 100 mV / div, 50 ms / div

CH2: Output Current: 2 A / div, 50 ms / div

V$_{MAX}$: 12.3 V

V$_{MIN}$: 12.03 V

11.2.2 50 % – 100 % Load Step



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.1565 V	11.9773 V	4.94 A	2.27 A				
status	✓	✓	✓	✓				

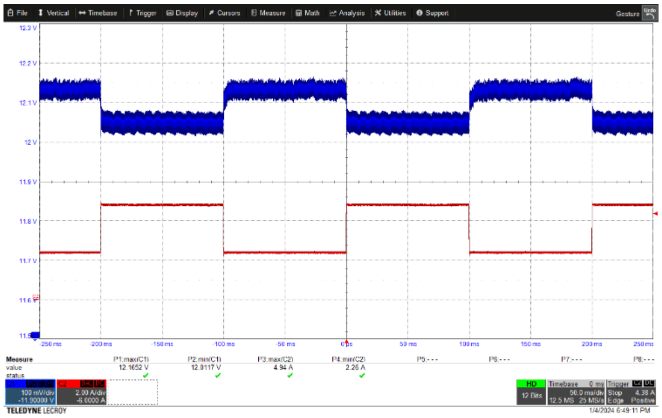
Figure 35 – 90 VAC; I$_O$ = 2.5 A – 5 A (50-100%) Load Step

CH1: Output Voltage: 100 mV / div, 50 ms / div

CH2: Output Current: 2 A / div, 50 ms / div

V$_{MAX}$: 12.2 V

V$_{MIN}$: 12.0 V



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.1652 V	12.0117 V	4.94 A	2.26 A				
status	✓	✓	✓	✓				

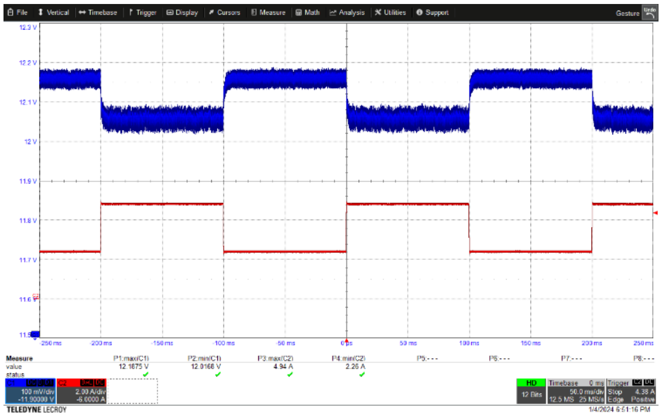
Figure 36 – 115 VAC; I$_O$ = 2.5 A – 5 A (50-100%) Load Step

CH1: Output Voltage: 100 mV / div, 50 ms / div

CH2: Output Current: 2 A / div, 50 ms / div

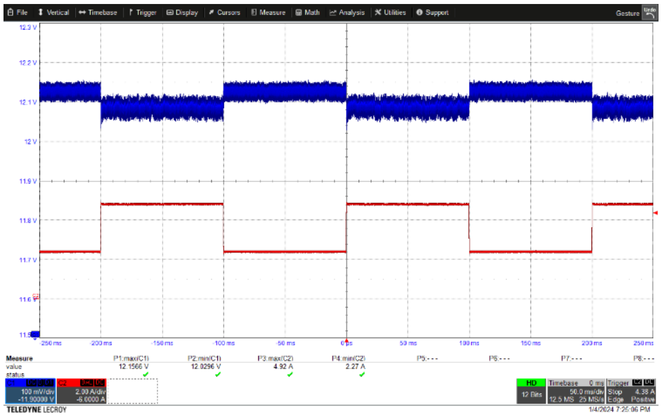
V$_{MAX}$: 12.2 V

V$_{MIN}$: 12.01 V



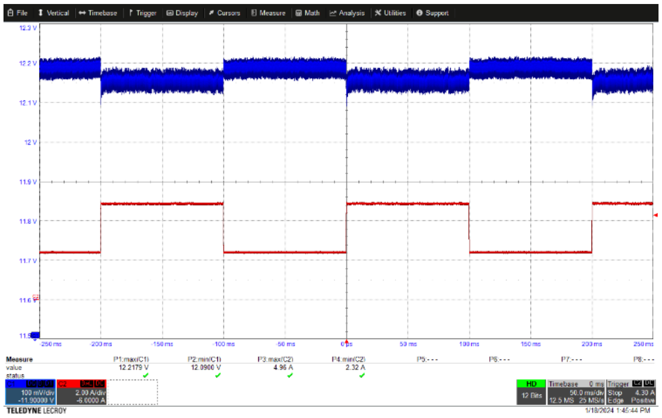
Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.1875 V	12.0168 V	4.94 A	2.26 A				
status	✓	✓	✓	✓				

Figure 37 – 230 VAC; I_O = 2.5 A – 5 A (50-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 12.0 V



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.1566 V	12.0296 V	4.92 A	2.27 A				
status	✓	✓	✓	✓				

Figure 38 – 265 VAC; I_O = 2.5 A – 5 A (50-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 12.0 V



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	12.2179 V	12.0900 V	4.96 A	2.32 A				
status	✓	✓	✓	✓				

Figure 39 – 480 VAC; I_O = 2.5 A – 5 A (50-100%) Load Step
CH1: Output Voltage: 100 mV / div, 50 ms / div
CH2: Output Current: 2 A / div, 50 ms / div
V_{MAX}: 12.2 V
V_{MIN}: 12.1 V

11.3 InnoSwitch Switching Waveforms

11.3.1 Drain Voltage and Current at Start-up

Figure 40 – 90 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 20 ms / div
CH 2: Drain Current: 2 A / div, 20 ms / div
Drain voltage, Max. = 301 V
Drain current, Max. = 3.25 A

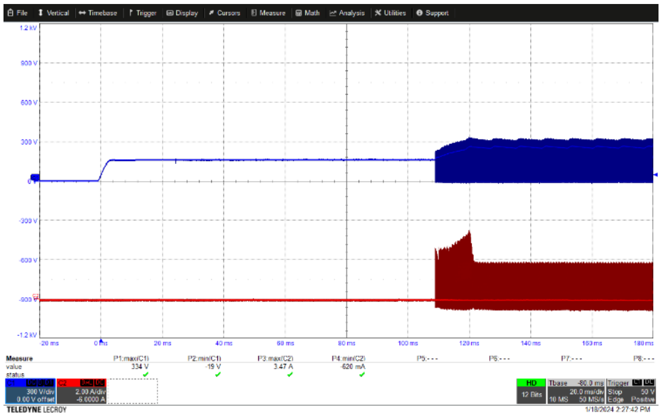


Figure 41 – 115 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 20 ms / div
CH 2: Drain Current: 2 A / div, 20 ms / div
Drain voltage, Max. = 334 V
Drain current, Max. = 3.47 A

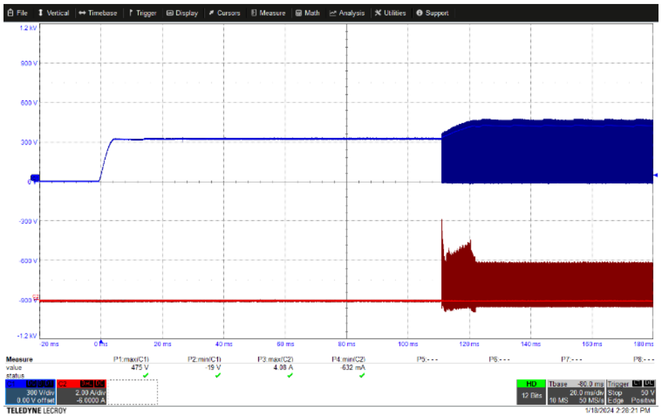


Figure 42 – 230 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 20 ms / div
CH 2: Drain Current: 2 A / div, 20 ms / div
Drain voltage, Max. = 475 V
Drain current, Max. = 4.08 A

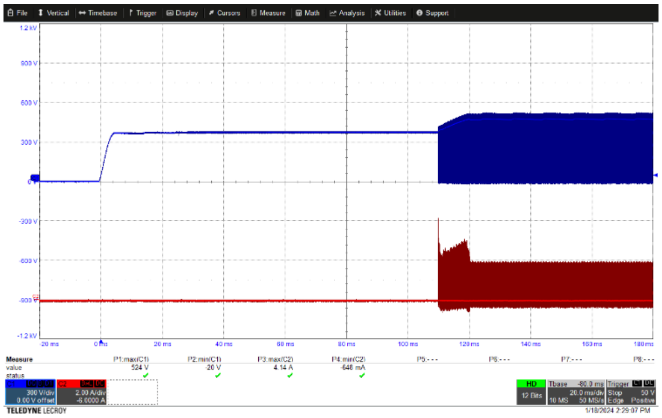
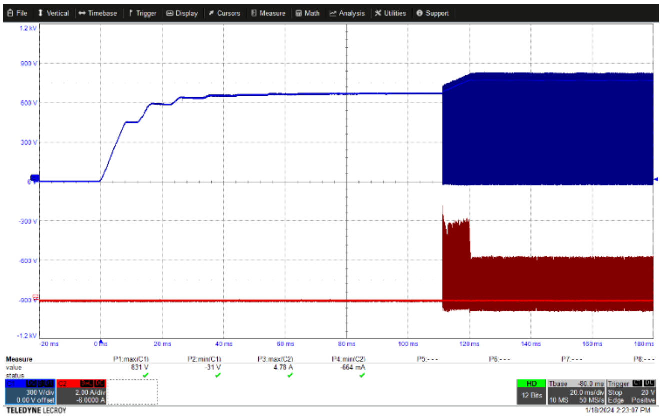


Figure 43 – 265 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 20 ms / div
CH 2: Drain Current: 2 A / div, 20 ms / div
Drain voltage, Max. = 524 V
Drain current, Max. = 4.14 A



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	831 V	-31 V	4.78 A	-664 mA				
status	✓	✓	✓	✓				

Figure 44 – 480 VAC, I_O = 5 A (Full-Load)

CH 1: Drain Voltage: 200 V / div, 20 ms / div

CH 2: Drain Current: 2 A / div, 20 ms / div

Drain voltage, Max. = 831 V

Drain current, Max. = 4.78 A

11.3.2 Drain Voltage and Current at Normal Operation

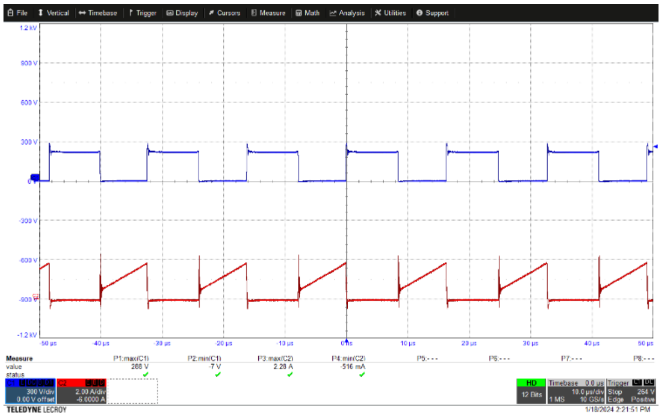


Figure 45 – 90 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 2 A / div, 10 µs / div
Drain voltage, Max. = 288 V
Drain current, Max. = 2.28 A

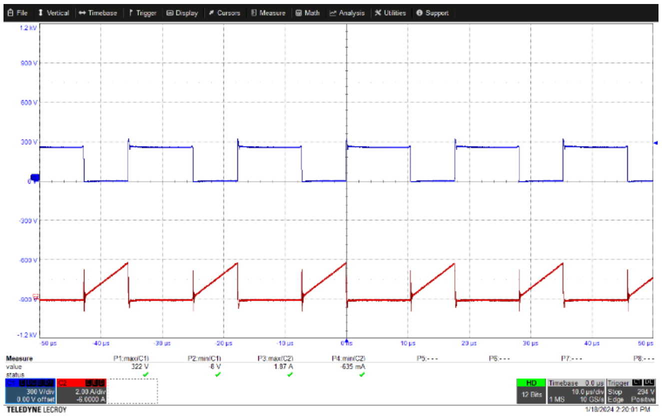


Figure 46 – 115 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 2 A / div, 10 µs / div
Drain voltage, Max. = 322 V
Drain current, Max. = 1.87 A

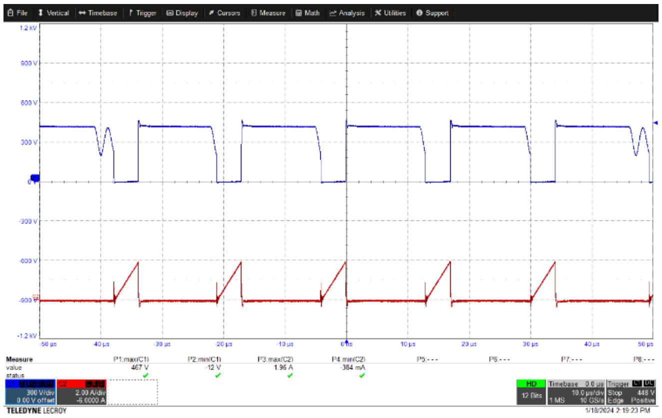


Figure 47 – 230 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 2 A / div, 10 µs / div
Drain voltage, Max. = 467 V
Drain current, Max. = 1.96 A

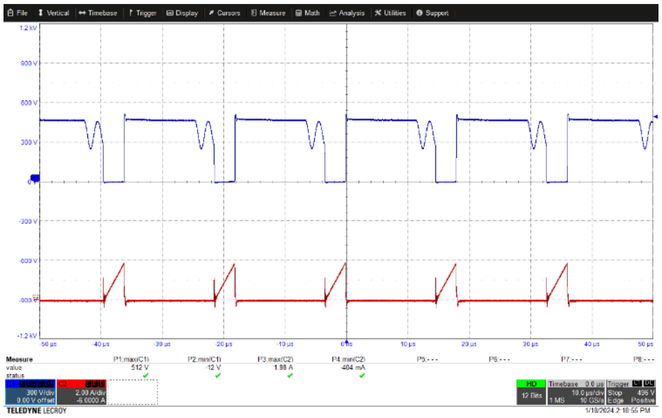
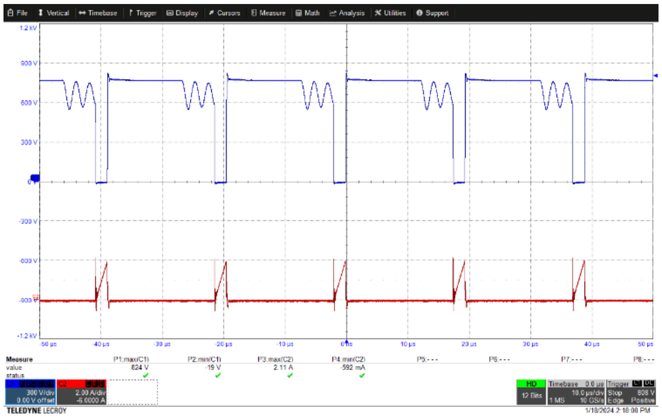


Figure 48 – 265 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 2 A / div, 10 µs / div
Drain voltage, Max. = 512 V
Drain current, Max. = 1.88 A



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	824 V	-19 V	2.11 A	-592 mA				
status	✓	✓	✓	✓				

Figure 49 – 480 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 200 V / div, 10 µs / div
CH 2: Drain Current: 2 A / div, 10 µs / div
Drain voltage, Max. = 824 V
Drain current, Max. = 2.11 A

11.3.3 Drain Voltage and Current with Output Short

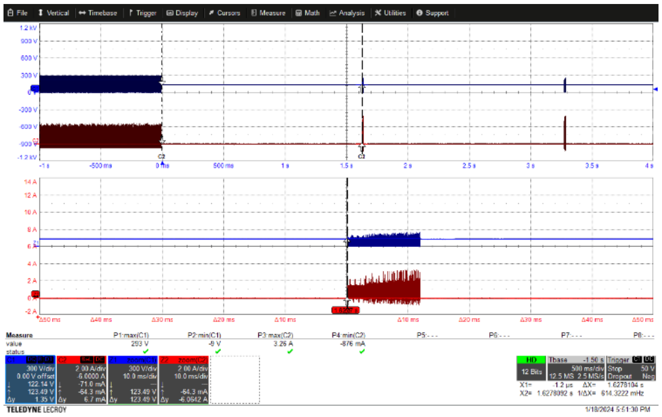


Figure 50 – 90 VAC
CH1: Drain Voltage: 200 V / div, 500 ms/div
CH2: Drain Current: 2 A / div, 500 ms/div
Zoom: 10 ms / div
Drain voltage, Max. = 293 V
Drain current, Max. = 3.26 A

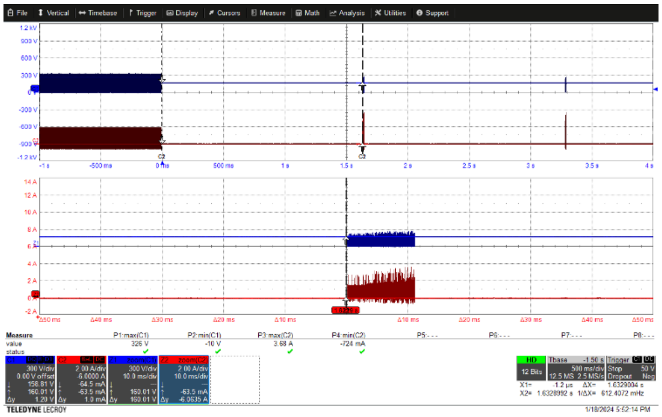


Figure 51 – 115 VAC
CH1: Drain Voltage: 200 V / div, 500 ms/div
CH2: Drain Current: 2 A / div, 500 ms/div
Zoom: 10 ms / div
Drain voltage, Max. = 326 V
Drain current, Max. = 3.68 A

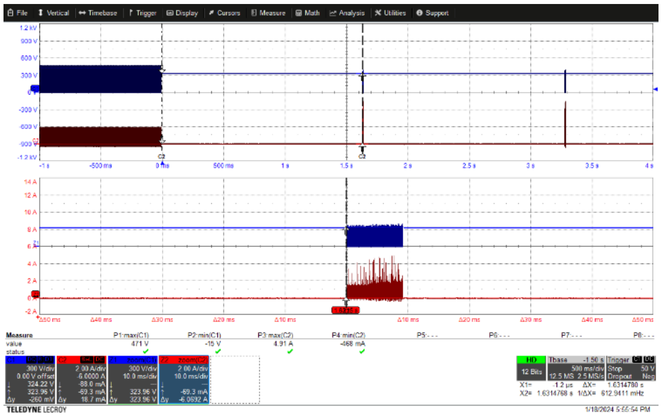


Figure 52 – 230 VAC
CH1: Drain Voltage: 200 V / div, 500 ms /div
CH2: Drain Current: 2 A / div, 500 ms/div
Zoom: 10 ms / div
Drain voltage, Max. = 471 V
Drain current, Max. = 4.91 A

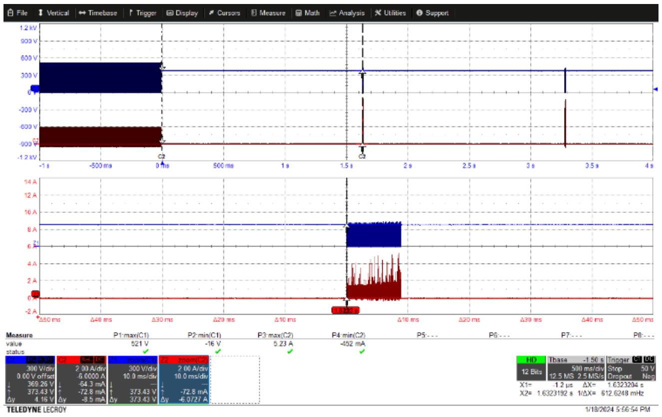
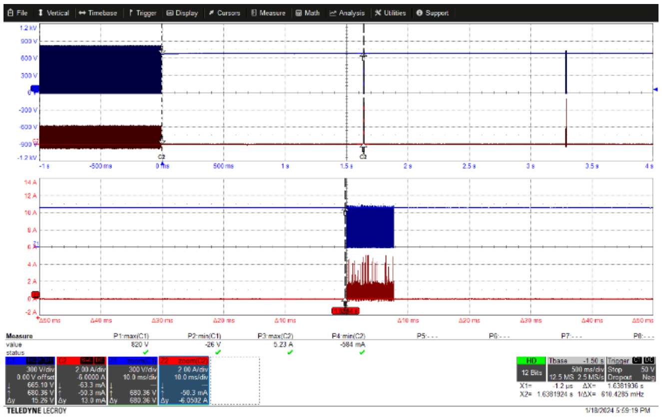


Figure 53 – 265 VAC
CH1: Drain Voltage: 200 V / div, 500 ms/div
CH2: Drain Current: 2 A / div, 500 ms/div
Zoom: 10 ms / div
Drain voltage, Max. = 521 V
Drain current, Max. = 5.23 A



Measure	P1:max(C1)	P2:min(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	820 V	-26 V	5.23 A	-584 mA				
status	✓	✓	✓	✓				

C1	C2	Z1 zoom(C1)	Z2 zoom(C2)
300 V/div	2.00 A/div	300 V/div	2.00 A/div
0.00 V offset	-6.0000 A	10.0 ms/div	10.0 ms/div
↓ 665.10 V	↓ -63.3 mA	↓ ---	↓ ---
↑ 680.36 V	↑ -50.3 mA	↑ 680.36 V	↑ -50.3 mA
Δy 15.26 V	Δy 13.0 mA	Δy 680.36 V	Δy -6.0502 A

HD 12 Bits
Tbase -1.50 s 500 ms/div 12.5 MS 2.5 MS/s
Trigger Stop 50 V Dropout Neg
X1= -1.2 µs ΔX= 1.6381936 s
X2= 1.6381924 s 1/ΔX= 610.4285 mHz

Figure 54 – 480 VAC

CH 1: Drain Voltage: 200 V / div, 500 ms / div
CH 2: Drain Current: 2 A / div, 500 ms / div
Zoom: 10 ms / div
Drain voltage, Max. = 820 V
Drain current, Max. = 5.23 A

11.4 SR FET Switching Waveforms

11.4.1 SR FET Voltage and Current at Start-up

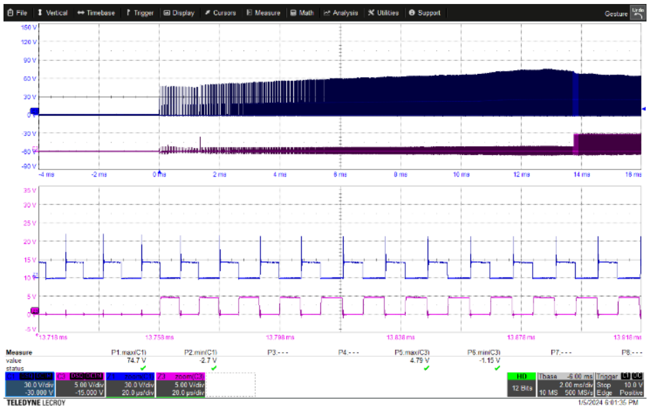


Figure 55 – 90 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Voltage, Max. = 74.7 V

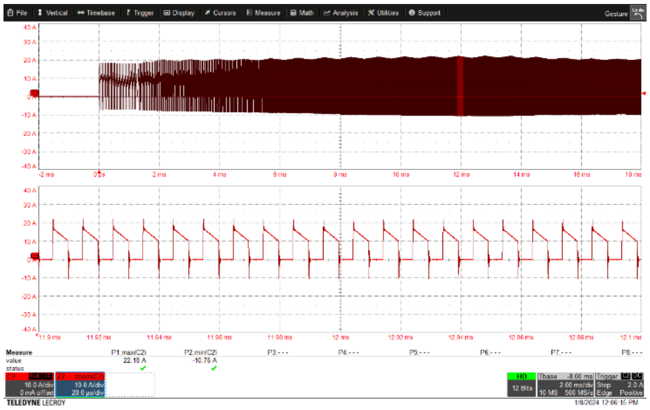


Figure 56 – 90 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Current, Max. = 22.2 A

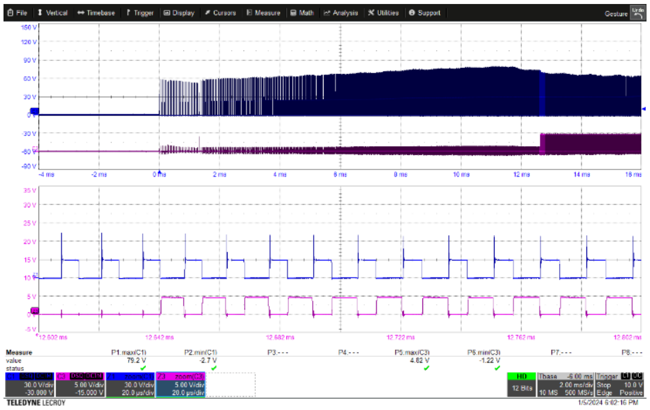


Figure 57 – 115 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Voltage, Max. = 79.2 V

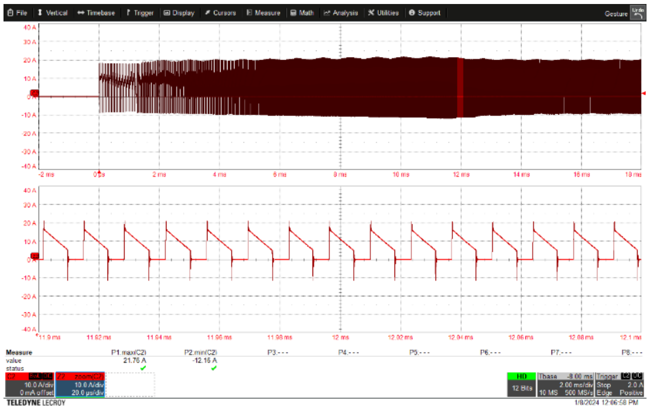


Figure 58 – 115 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Current, Max. = 21.8 A

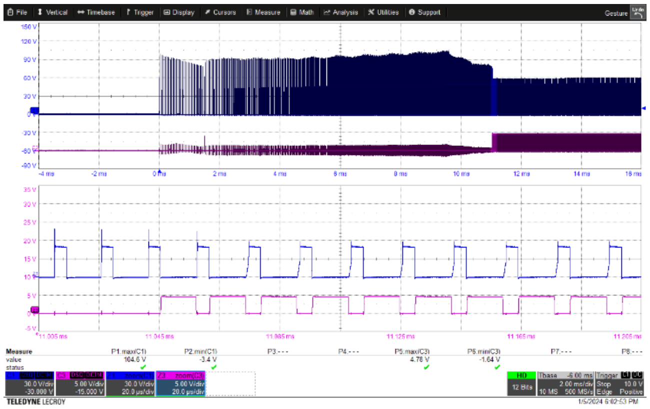


Figure 59 – 230 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 μs
SR FET Drain Voltage, Max. = 105 V

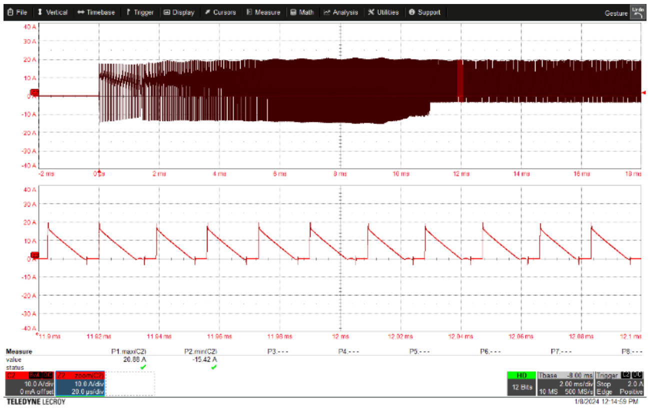


Figure 60 – 230 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 2 ms / div
Zoom: 20 μs
SR FET Drain Current, Max. = 20.9 A

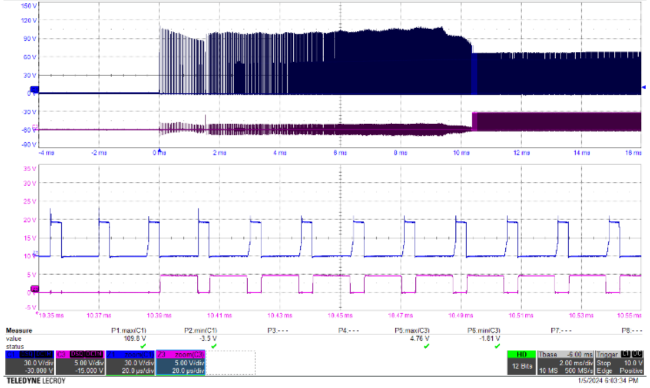


Figure 61 – 265 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 μs
SR FET Drain Voltage, Max. = 110 V

Figure 62 – 265 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 2 ms / div
Zoom: 20 μs
SR FET Drain Current, Max. = 20.6 A

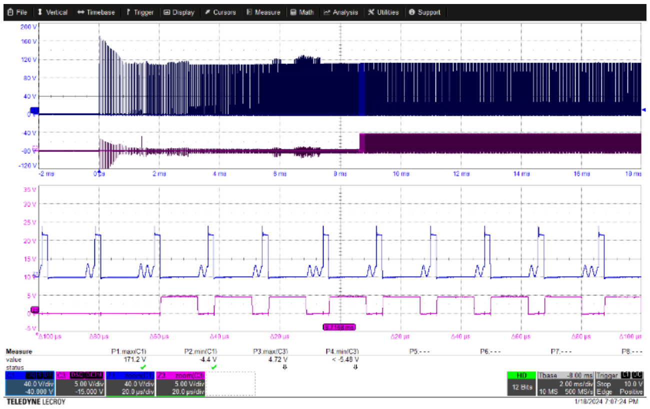


Figure 63 – 480 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 40 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Voltage, Max. = 171 V
*Voltage spike can be clamp with TVS diode if needed to retain 150 V rated SR FET

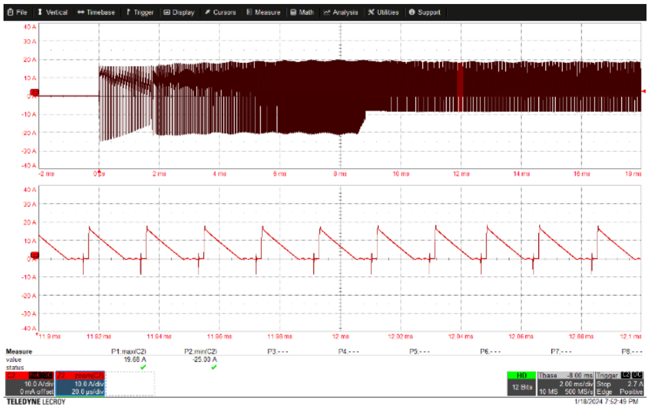


Figure 64 – 480 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Current, Max. = 19.7 A

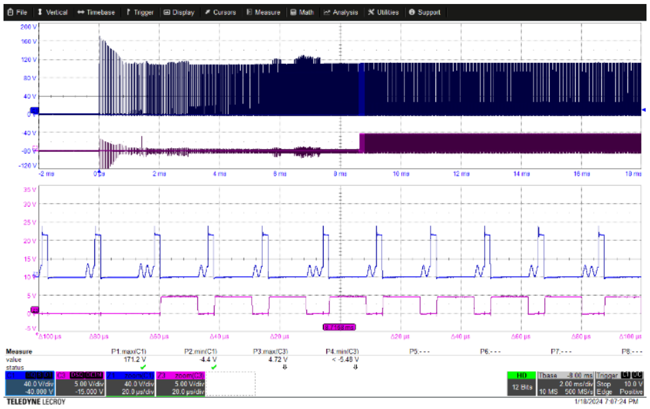


Figure 65 – 480 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 40 V / div, 2 ms / div
CH 3: Gate Voltage: 5 V / div, 2 ms / div
Zoom: 20 µs
SR FET Drain Voltage, Max. = 171 V
(with TVS SMAJ90A in parallel with SR FET)

11.4.2 SR FET Voltage and Current at Normal Operations

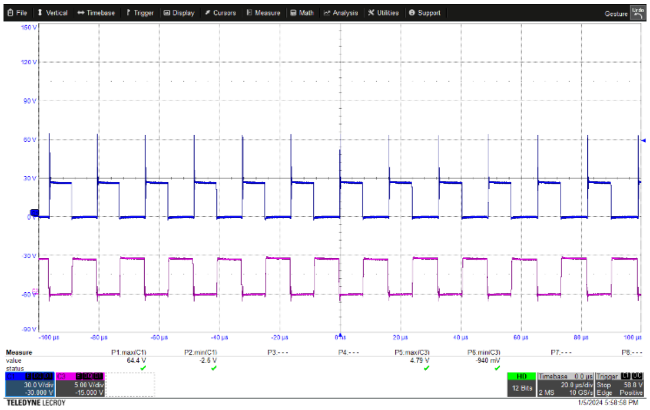


Figure 66 – 90 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 20 µs / div
CH 3: Gate Voltage: 5 V / div, 20 µs / div
SR FET Drain Voltage, Max. = 64.4 V

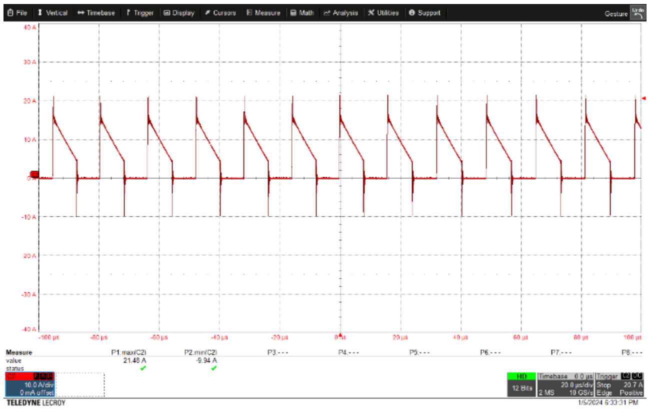


Figure 67 – 90 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 20 µs / div
SR FET Drain Current, Max. = 21.5 A

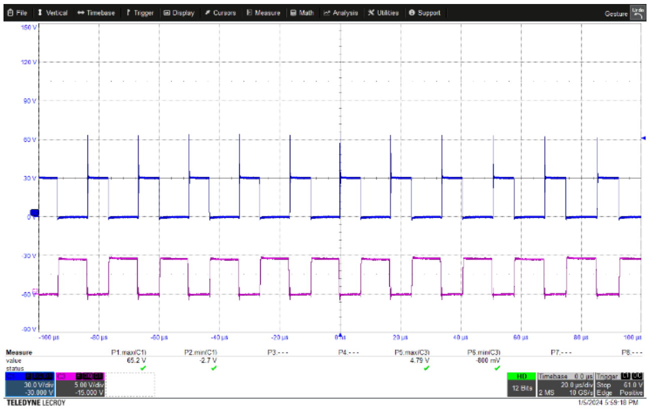


Figure 68 – 115 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 20 µs / div
CH 3: Gate Voltage: 5 V / div, 20 µs / div
SR FET Drain Voltage, Max. = 65.2 V

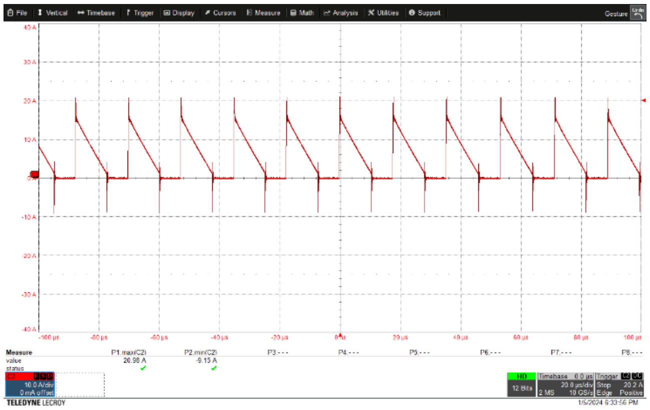


Figure 69 – 115 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 20 µs / div
SR FET Drain Current, Max. = 21 A

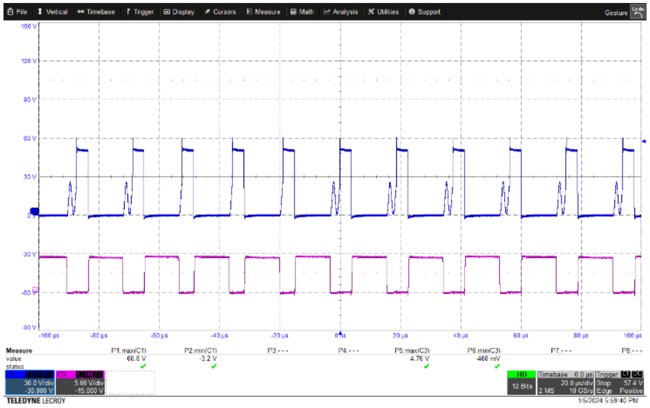


Figure 70 – 230 VAC, I_O = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 20 µs / div
CH 3: Gate Voltage: 5 V / div, 20 µs / div
SR FET Drain Voltage, Max. = 60.6 V

e

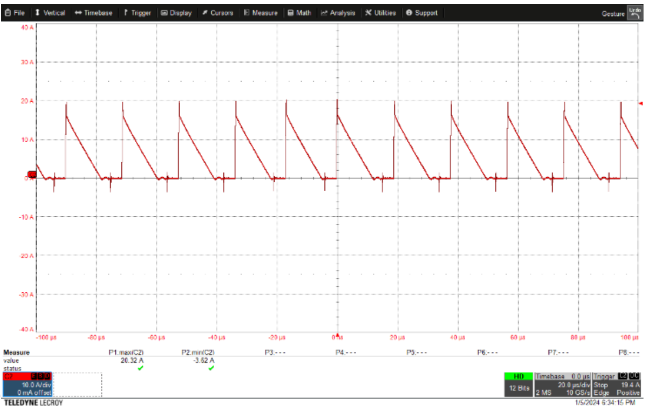


Figure 71 – 230 VAC, I_O = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 20 µs / div
SR FET Drain Current, Max. = 20.3 A

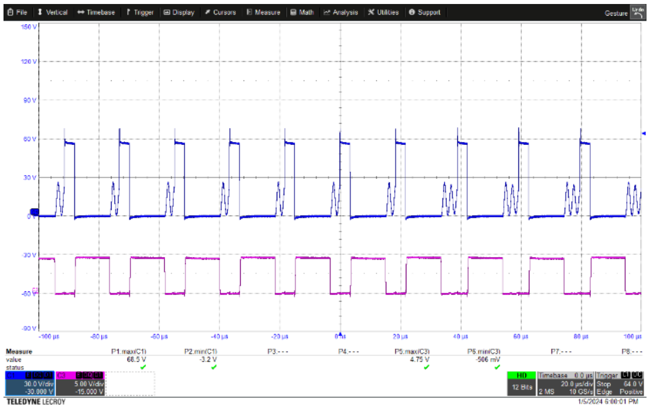


Figure 72 – 265 VAC, IO = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 20 µs / div
CH 3: Gate Voltage: 5 V / div, 20 µs / div
SR FET Drain Voltage, Max. = 68.5 V

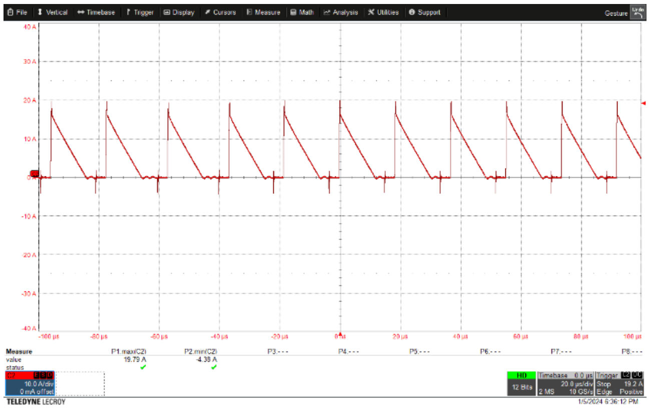


Figure 73 – 265 VAC, IO = 5 A (Full-Load
CH 2: Drain Current: 10 A / div, 20 µs / div
SR FET Drain Current, Max. = 19.8

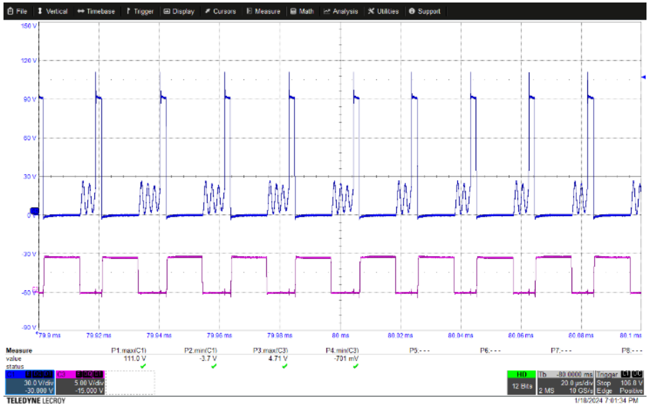


Figure 74 – 480 VAC, IO = 5 A (Full-Load)
CH 1: Drain Voltage: 30 V / div, 20 µs / div
CH 3: Gate Voltage: 5 V / div, 20 µs / div
SR FET Drain Voltage, Max. = 111.0 V

e

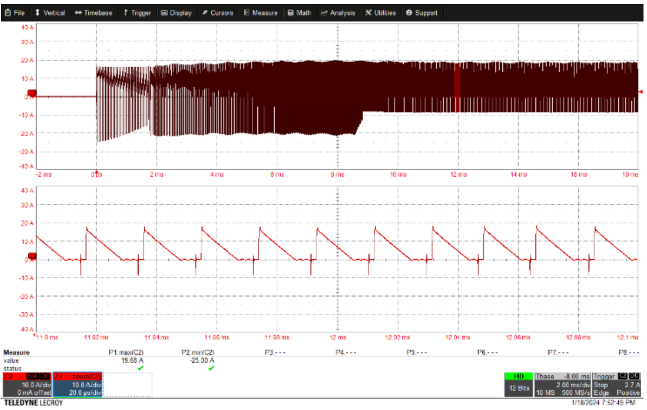


Figure 75 – 480 VAC, IO = 5 A (Full-Load)
CH 2: Drain Current: 10 A / div, 20 µs / div
SR FET Drain Current, Max. = 19.0 A

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figures 76 and 77.

The PP026 probe adapter is modified by having two capacitors tied in parallel across the probe tip. The capacitors are one 0.1 μF/50 V ceramic and one 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

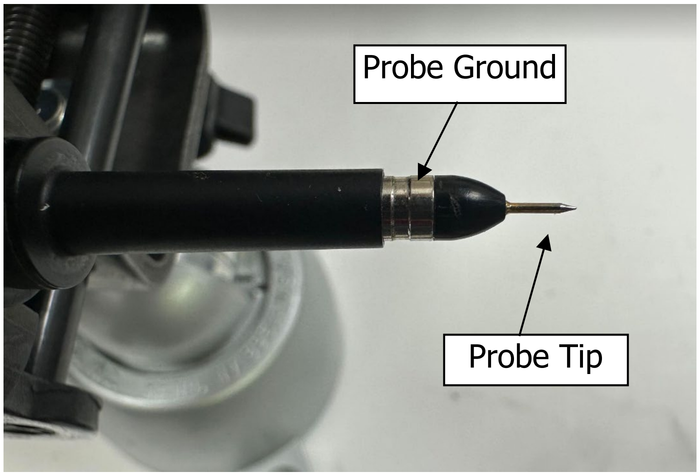


Figure 76 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

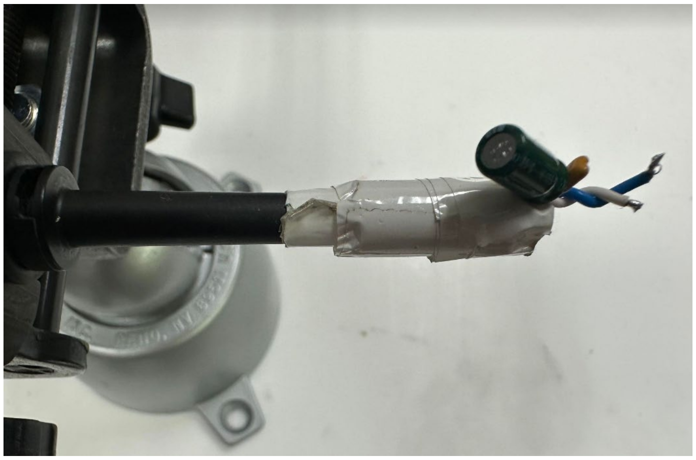


Figure 77 – Oscilloscope Probe with BNC Adapter

(https://www.teledynelecroy.com/probes/passive-probes/pp026-1)

11.5.2 Ripple Waveforms (Measured on Board)

11.5.2.1 100% Load

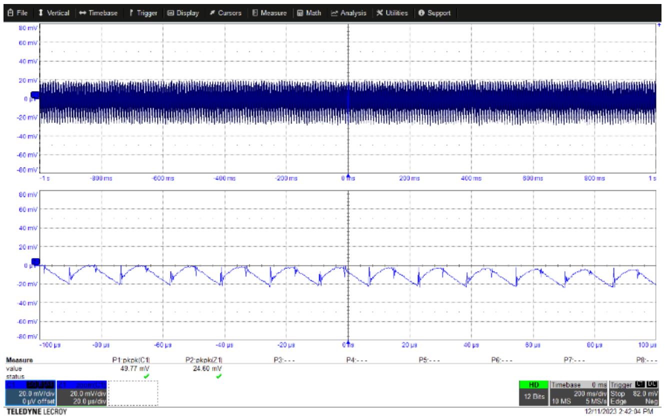


Figure 78 – 90 VAC Input, 100% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 49.8 mVpp

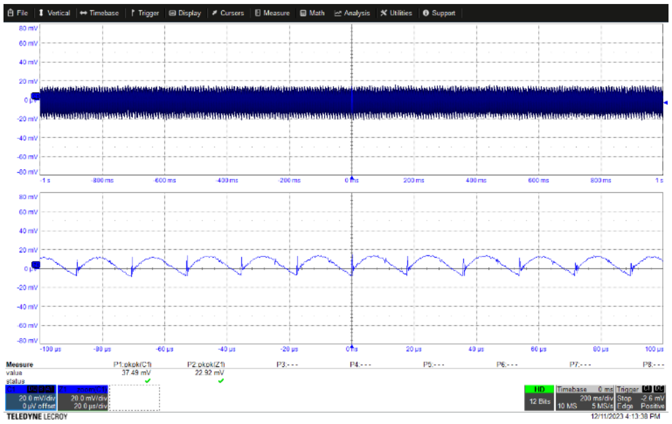


Figure 79 – 115 VAC Input, 100% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 37.5 mVpp

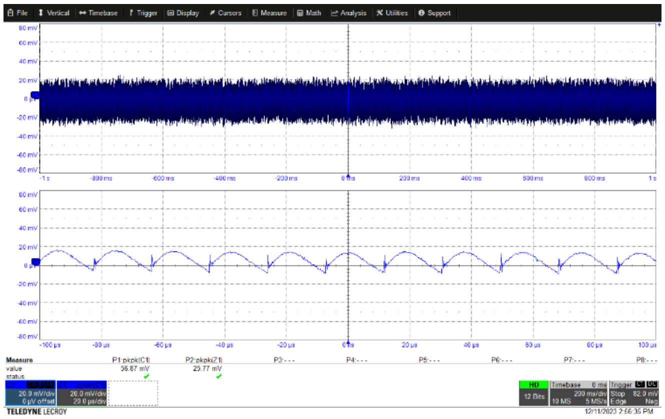


Figure 80 – 230 VAC Input, 100% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 56.9 mVpp

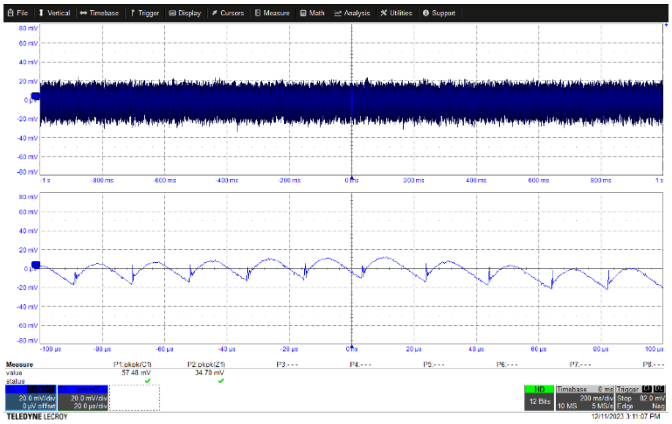


Figure 81 – 265 VAC Input, 100% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 57.5 mVpp

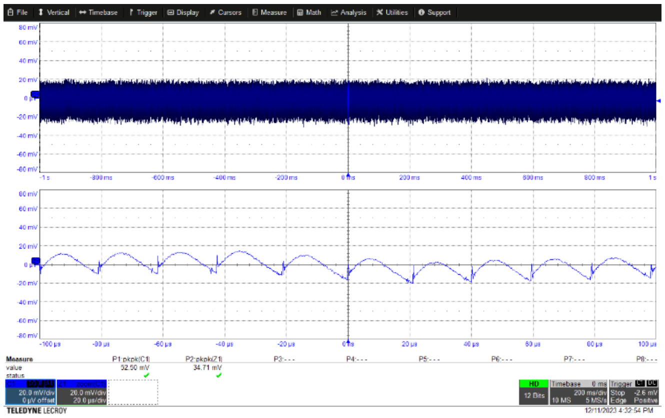


Figure 82 – 480 VAC Input, 100% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 52.5 mVpp

11.5.2.2 50% Load

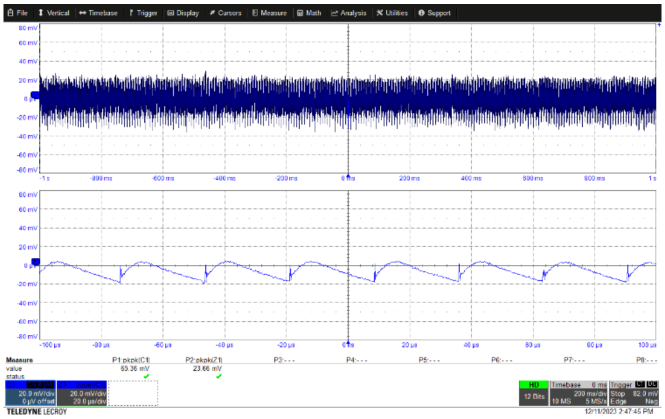


Figure 83 –90 VAC Input, 50% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 65.4 mVpp

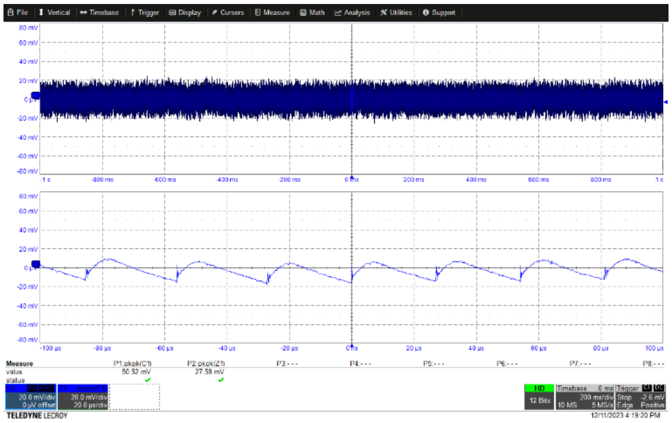


Figure 84 – 115 VAC Input, 50% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 50.5 mVpp

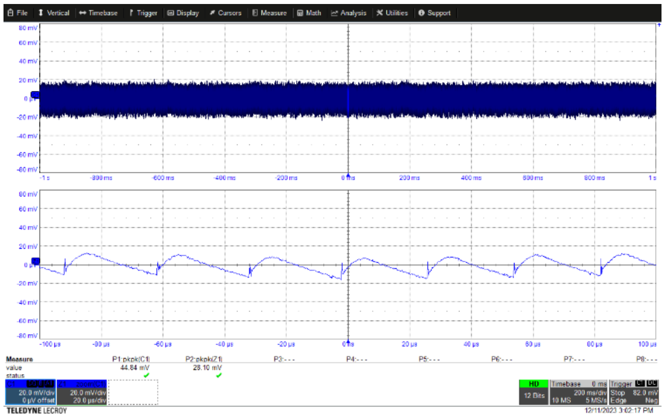


Figure 85 – 230 VAC Input, 50% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 μs
Voltage Ripple: 44.8 mVpp

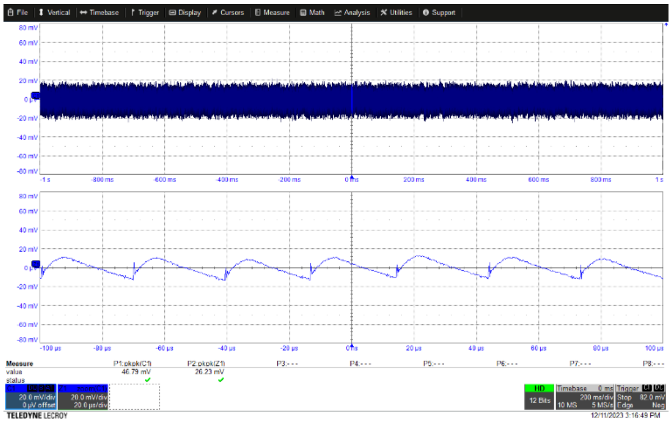


Figure 86 – 265 VAC Input, 50% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 μs
Voltage Ripple: 46.8 mVpp

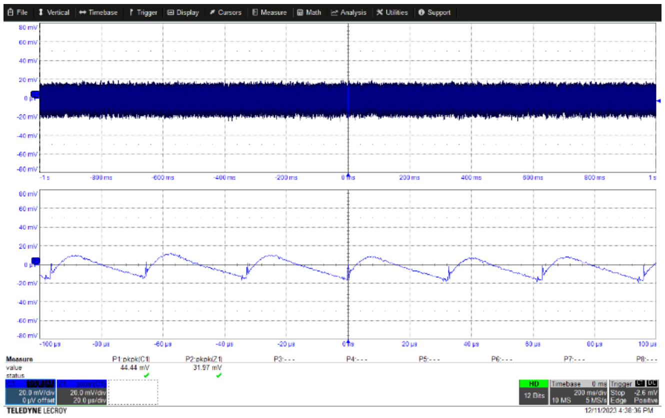


Figure 87 – 480 VAC Input, 50% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 μs
Voltage Ripple: 44.4 mVpp

11.5.2.3 10% Load

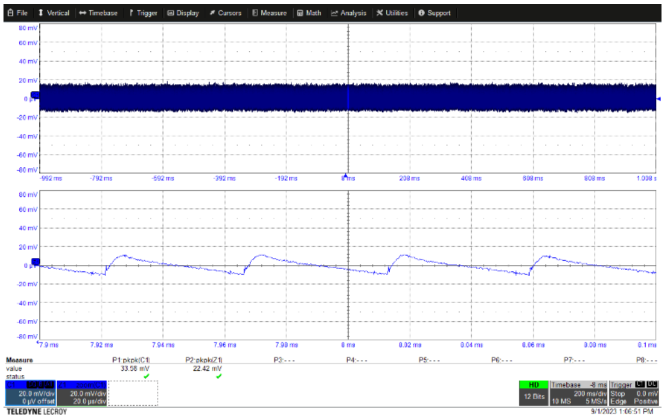


Figure 88 –90 VAC Input, 10% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 33.6 mVpp

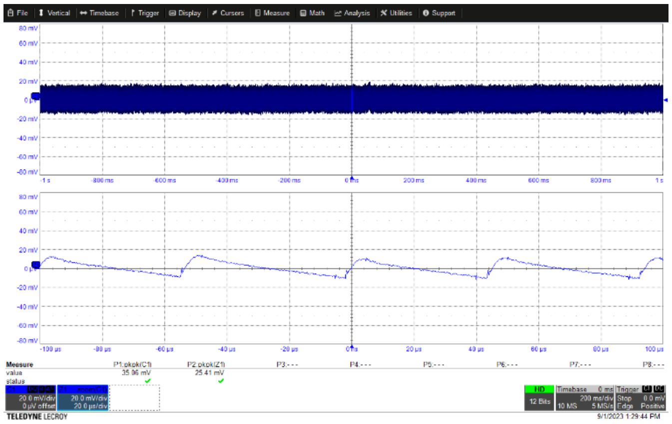


Figure 89 – 115 VAC Input, 10% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 35.1 mVpp

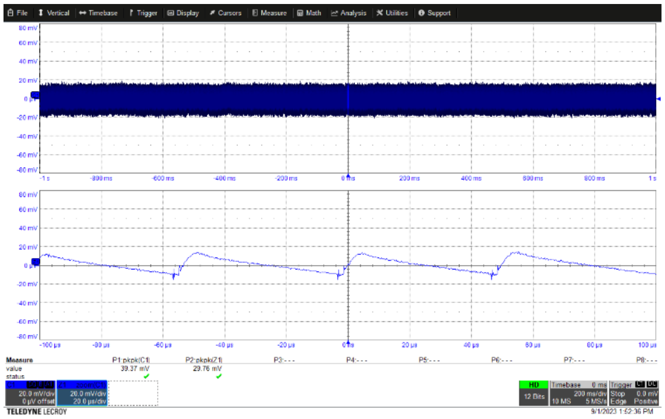


Figure 90 – 230 VAC Input, 10% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 39.4 mVpp

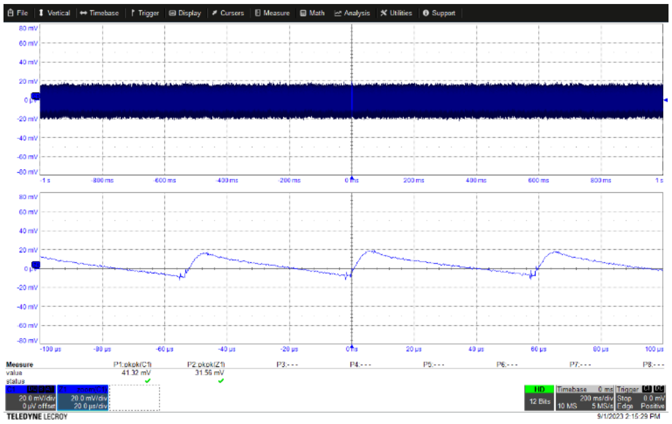
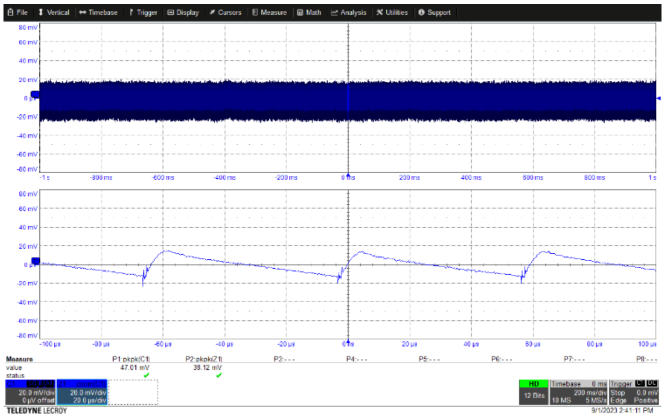


Figure 91 – 265 VAC Input, 10% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 41.3 mVpp



Measure	P1:pkpk(C1)	P2:pkpk(Z1)	P3:- - -	P4:- - -	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	47.01 mV	38.12 mV						
status	✓	✓						

Figure 92 – 420 VAC Input, 10% Load
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs
Voltage Ripple: 47.0 mVpp

11.5.3 Output Voltage Ripple

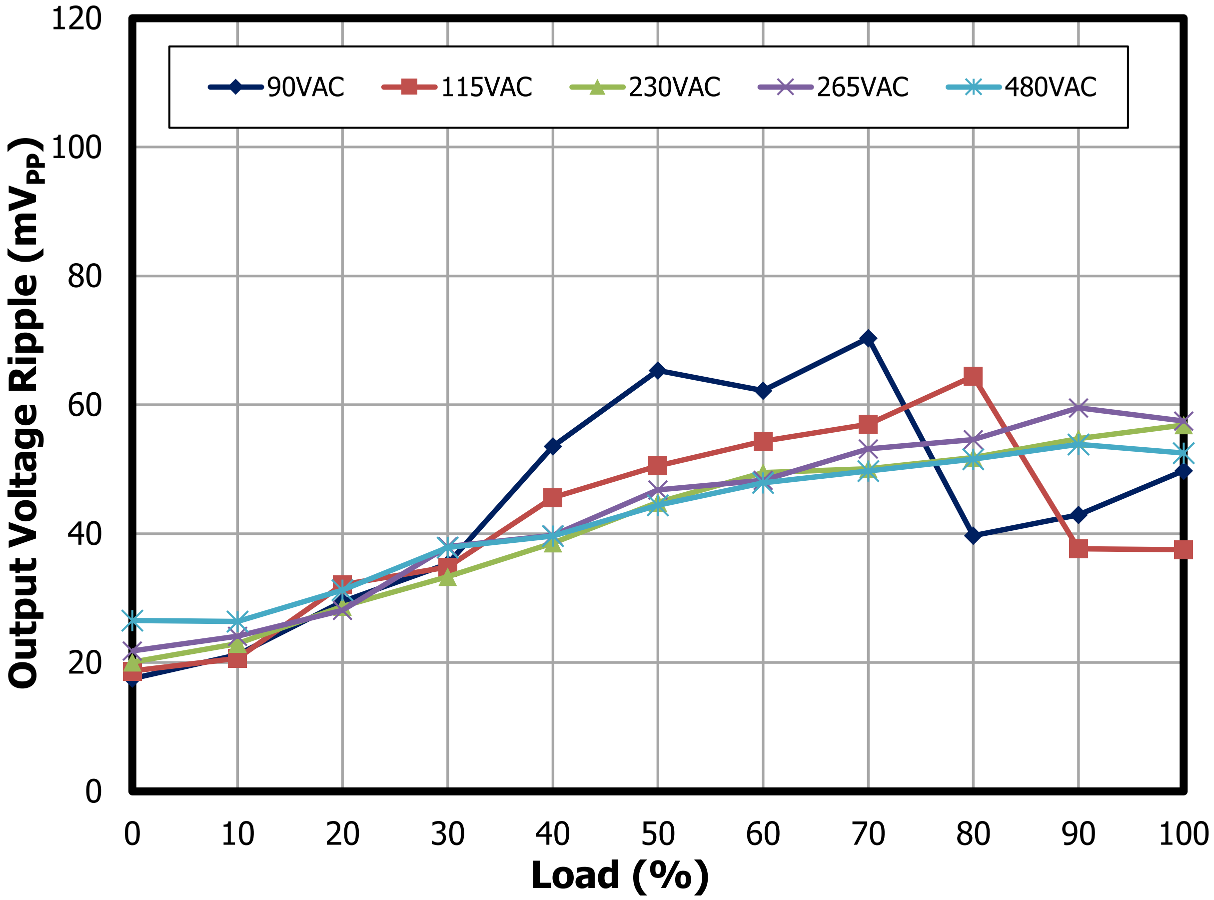
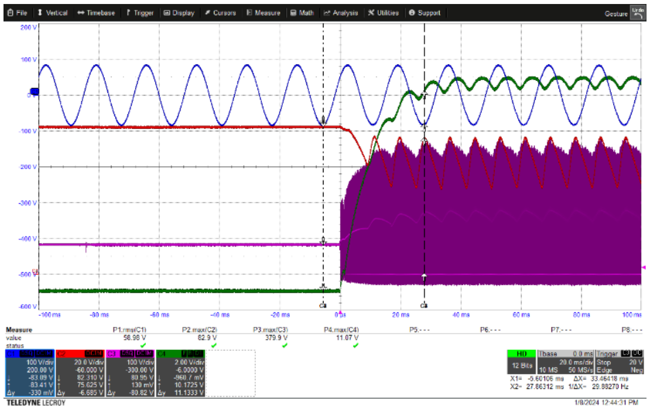


Figure 93 – Output Voltage Ripple

11.6 Input Undervoltage Detection



Measure	P1:rms(C1)	P2:max(C2)	P3:max(C3)	P4:max(C4)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	58.98 V	82.9 V	379.9 V	11.07 V				
status	✓	✓	✓	✓				

Figure 94 – UV+, I_o = 5 A (Full-Load)

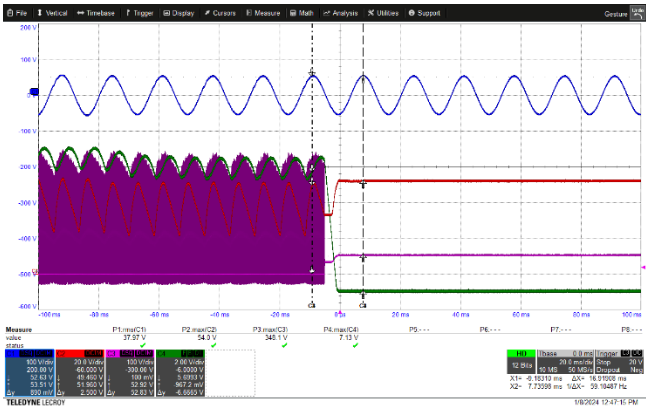
CH 1: Input Voltage: 100 V / div, 20 ms / div

CH 2: Bulk Voltage: 20 V / div, 20 ms / div

CH 3: V_{DS} (InnoSwitch): 100 V / div, 20 ms / div

CH 4: Output Voltage: 2 V / div, 20 ms / div

UV+ = 59 VAC



Measure	P1:rms(C1)	P2:max(C2)	P3:max(C3)	P4:max(C4)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	37.97 V	54.0 V	348.1 V	7.13 V				
status	✓	✓	✓	✓				

Figure 95 – UV-, I_o = 5 A (Full-Load)

CH 1: Input Voltage: 100 V / div, 20 ms / div

CH 2: Bulk Voltage: 20 V / div, 20 ms / div

CH 3: V_{DS} (InnoSwitch): 100 V / div, 20 ms / div

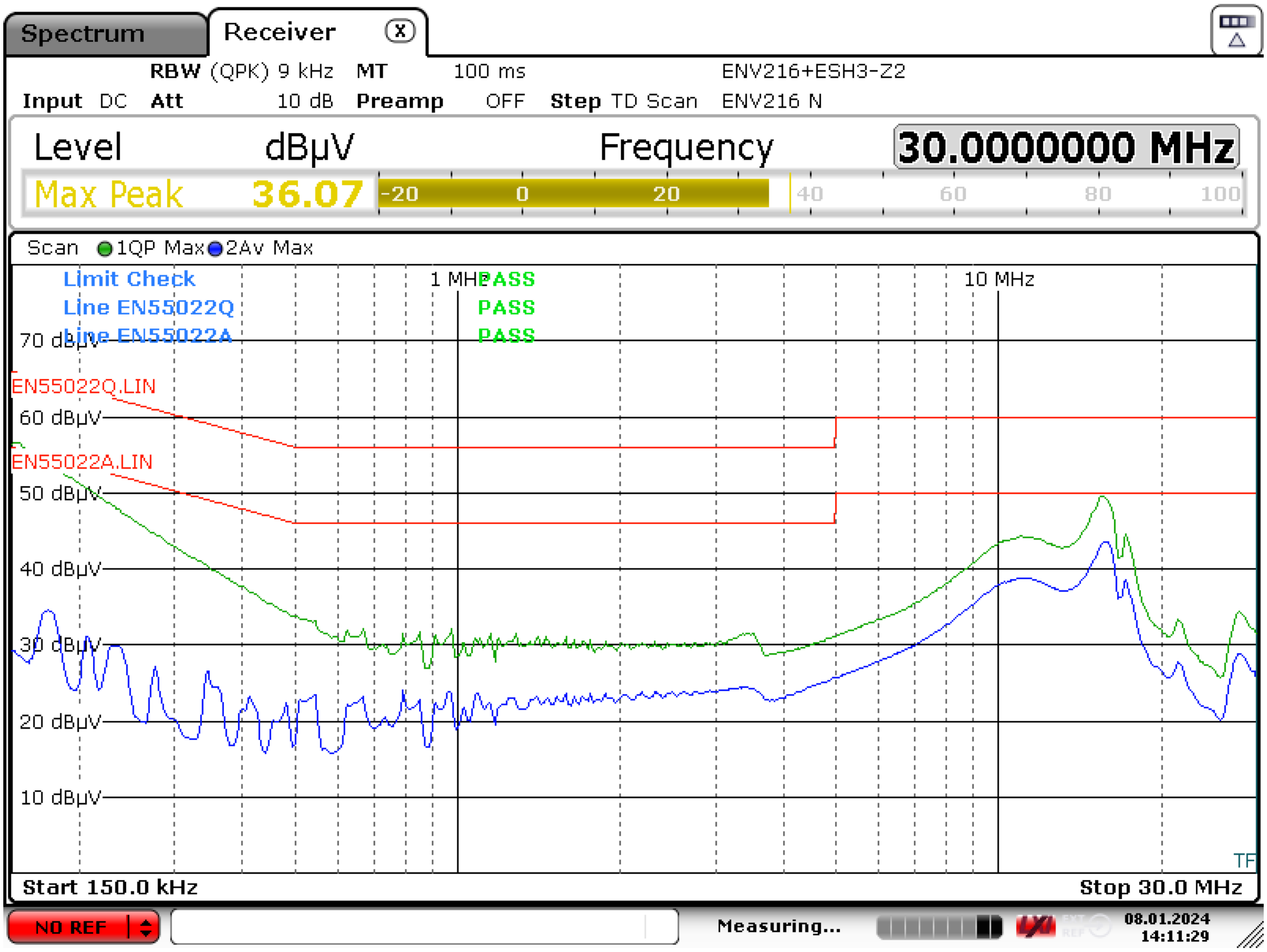
CH 4: Output Voltage: 2 V / div, 20 ms / div

UV- = 38.0 VAC

12 Conducted EMI

12.1 Grounded Output

12.1.1 VIN: 115 VAC



RBW (QPK) 9 kHz MT 100 ms ENV216+ESH3-Z2
Input DC Att 10 dB Preamp OFF Step TD Scan ENV216 N

Level dBµV Frequency 30.0000000 MHz
Max Peak 36.07

Limit Check PASS
Line EN55022Q PASS
Line EN55022A PASS

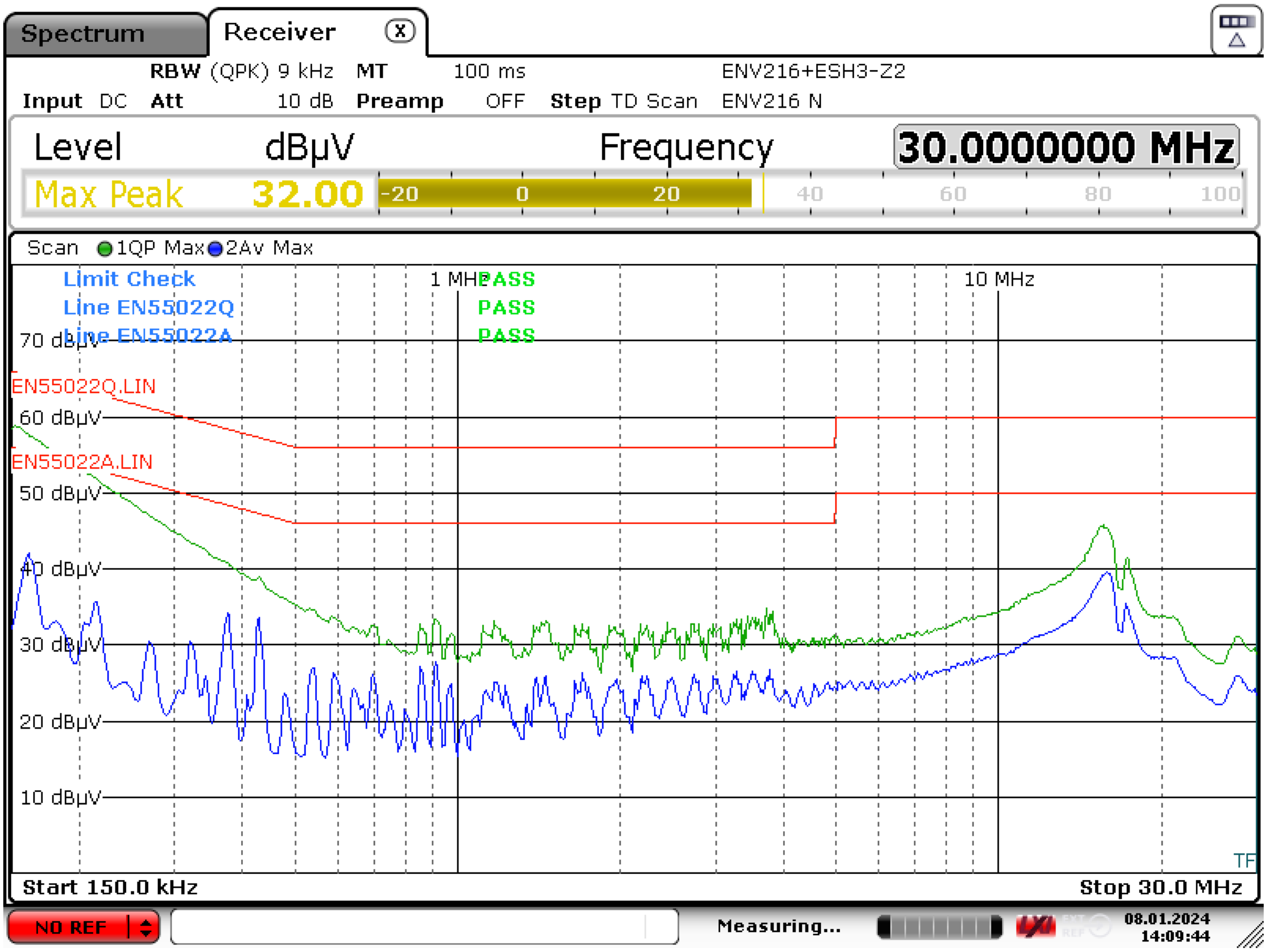
Start 150.0 kHz Stop 30.0 MHz

Measuring... 08.01.2024 14:11:29

Date: 8.JAN.2024 14:11:29

Figure 96 – Grounded Output EMI, Line, 12 V / 100% Load

12.1.2 VIN: 230 VAC



RBW (QPK) 9 kHz MT 100 ms ENV216+ESH3-Z2
Input DC Att 10 dB Preamp OFF Step TD Scan ENV216 N

Level dBµV Frequency 30.0000000 MHz
Max Peak 32.00

Scan ●1QP Max ●2Av Max

Limit Check PASS
Line EN55022Q PASS
Line EN55022A PASS

Start 150.0 kHz Stop 30.0 MHz

Measuring... 08.01.2024 14:09:44

Date: 8.JAN.2024 14:09:44

Figure 97 – Grounded Output EMI, Line, 12 V / 100% Load

13 Line Surge

13.1 Differential Mode Test

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	L, N	2	10	Pass
–6000	90	L, N	2	10	Pass
+6000	180	L, N	2	10	Pass
–6000	180	L, N	2	10	Pass
+6000	270	L, N	2	10	Pass
–6000	270	L, N	2	10	Pass

Table 21 – Test Data at 6 kV Differential Surge

13.2 Ring Wave Surge

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	L, N → PE	12	10	Pass
–6000	90	L, N → PE	12	10	Pass
+6000	180	L, N → PE	12	10	Pass
–6000	180	L, N → PE	12	10	Pass
+6000	270	L, N → PE	12	10	Pass
–6000	270	L, N → PE	12	10	Pass

Table 22 – Test Data at 6 kV Ring Wave Surge

14 EFT

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	90	L, N - PE	5	15 ms	300	120	Pass
–4000	90	L, N - PE	5	15 ms	300	120	Pass
+4000	180	L, N - PE	5	15 ms	300	120	Pass
–4000	180	L, N - PE	5	15 ms	300	120	Pass
+4000	270	L, N - PE	5	15 ms	300	120	Pass
–4000	270	L, N - PE	5	15 ms	300	120	Pass
+4000	90	L, N - PE	100	750 µs	300	120	Pass
–4000	90	L, N - PE	100	750 µs	300	120	Pass
+4000	180	L, N - PE	100	750 µs	300	120	Pass
–4000	180	L, N - PE	100	750 µs	300	120	Pass
+4000	270	L, N - PE	100	750 µs	300	120	Pass
–4000	270	L, N - PE	100	750 µs	300	120	Pass

Table 23 – Test Data at 4 kV EFT

15 Electrostatic Discharge (ESD)

The power supply passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under full load condition for both 115 VAC and 230 VAC.

15.1 Contact Discharge at 115 VAC and 230 VAC

Contact Discharge(kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 2	V_{OUT} (+)	10	0/10	PASS
- 2		10	0/10	PASS
+ 2	V_{OUT} (-)	10	0/10	PASS
- 2		10	0/10	PASS
+ 4	V_{OUT} (+)	10	0/10	PASS
- 4		10	0/10	PASS
+ 4	V_{OUT} (-)	10	0/10	PASS
- 4		10	0/10	PASS
+ 6	V_{OUT} (+)	10	0/10	PASS
- 6		10	0/10	PASS
+ 6	V_{OUT} (-)	10	0/10	PASS
- 6		10	0/10	PASS
+ 8	V_{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V_{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8.8	V_{OUT} (+)	10	0/10	PASS
- 8.8		10	0/10	PASS
+ 8.8	V_{OUT} (-)	10	0/10	PASS
- 8.8		10	0/10	PASS

Table 24 – Test Data at 115 VAC and 230 VAC

15.2 Air Discharge at 115 VAC and 230 VAC

Air Discharge (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 8	V_{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V_{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 10	V_{OUT} (+)	10	0/10	PASS
- 10		10	0/10	PASS
+ 10	V_{OUT} (-)	10	0/10	PASS
- 10		10	0/10	PASS
+ 12	V_{OUT} (+)	10	0/10	PASS
- 12		10	0/10	PASS
+ 12	V_{OUT} (-)	10	0/10	PASS
- 12		10	0/10	PASS
+ 14	V_{OUT} (+)	10	0/10	PASS
- 14		10	0/10	PASS
+ 14	V_{OUT} (-)	10	0/10	PASS
- 14		10	0/10	PASS
+ 15	V_{OUT} (+)	10	0/10	PASS
- 15		10	0/10	PASS
+ 15	V_{OUT} (-)	10	0/10	PASS
- 15		10	0/10	PASS
+ 16.5	V_{OUT} (+)	10	0/10	PASS
- 16.5		10	0/10	PASS
+ 16.5	V_{OUT} (-)	10	0/10	PASS
- 16.5		10	0/10	PASS

Table 25 – Test Data at 115 and 230 VAC

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
31-May-2026	JMR	A	First Release	Apps & Mktg

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