Circuit Idea
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Drive Scheme for Reduced Conduction Loss in Dual-Output Converter

Summary of the Idea

In a power converter with two regulated outputs, each output can be provided with a separate MOSFET-based selection switch to allow output conduction when the switch is ON, and to block reverse conduction when the switch is OFF. The selection switches (a PFET and an NFET) are driven in complementary fashion, using a shared control signal as input to level-shifting capacitors that form the gate voltages of the selection switches. The blocking functionality is provided by the body diodes of the selection switches, which have less conduction loss compared to a discrete blocking diode.

Description

Dual-output power converters can provide a pair of constant-voltage (CV) or constant-current (CC) outputs. One output is usually regulated to a higher voltage than the other output. A blocking diode is typically required on the higher-voltage rail to prevent reverse current from the higher-voltage output/output capacitor to the lower-voltage output/output capacitor. This blocking diode introduces significant conduction loss during forward conduction.

To reduce conduction loss, the blocking diode can be replaced with a MOSFET-based selection switch so that each output is selected using a respective selection switch. The selection switches operate to conduct forward current but block reverse current and have much lower conduction loss compared to a discrete diode.

The drive scheme for the selection switches is relatively simple when the selection switch for the higher-voltage output is a p-channel MOSFET (PFET) and the selection switch for the lower-voltage output is an n-channel MOSFET (NFET). The PFET and NFET are driven in complementary fashion, so only one selection switch is turned ON at any given time. This can be accomplished using a shared control signal and level-shifting circuitry to generate the gate voltages of the selection switches.

Figure 1 illustrates a power converter with a controller that generates a shared control signal CDR for the selection switches based on secondary-side feedback. The feedback signal(s) may include a signal FB1 representative of output V_{OUT1}, a signal FB2 representative of output V_{OUT2}, and/or a signal FWD representative of a voltage at a secondary winding. The controller also generates a drive signal for a primary-side power switch and a drive signal SRD for a synchronous rectifier coupled between the secondary winding and secondary-side ground. C1 and C2 are output capacitors.

PFET P1 and NFET M1 are the respective selection switches for V_{OUT1} and V_{OUT2}. Capacitor C3 is charged/discharged to generate the gate voltage for P1. Capacitor C4 is charged/discharged to generate the gate voltage for M1. C3 and C4 are level-shifting capacitors that are respectively pre-charged to $\approx V_{OUT1}$ and $\approx V_{OUT2}$. When CDR is set low, Zener diode Z1 reverse conducts to make the voltage at C3 (P1 gate) equal to V_{OUT1} minus the reverse voltage across Z1, turning P1 ON. When CDR is set high, Z1 forward conducts to make the voltage at C3 equal to V_{OUT1} plus the forward voltage across Z1, turning P1 OFF.

Capacitor C4 and diode D1 operate to turn NFET M1 on/off in a similar manner. When CDR is set low, diode D1 conducts to make the voltage at C4 (M1 gate) equal to V_{OUT2} minus the forward voltage across D1, turning M1 OFF. When CDR is set high, diode D1 is reverse-biased and the voltage at C4 increases by 5V to equal V_{OUT2} + 5V minus D1's forward voltage, turning M1 ON.

Table 1 lists the states of the selection switches P1, M1 and control signal CDR during the following operating phases:

i) Delivery of current to output capacitor C1 (V_{OUT1} selected),
ii) Delivery of current to output capacitor C2 (V_{OUT2} selected), and
iii) Primary conduction (power switch ON).

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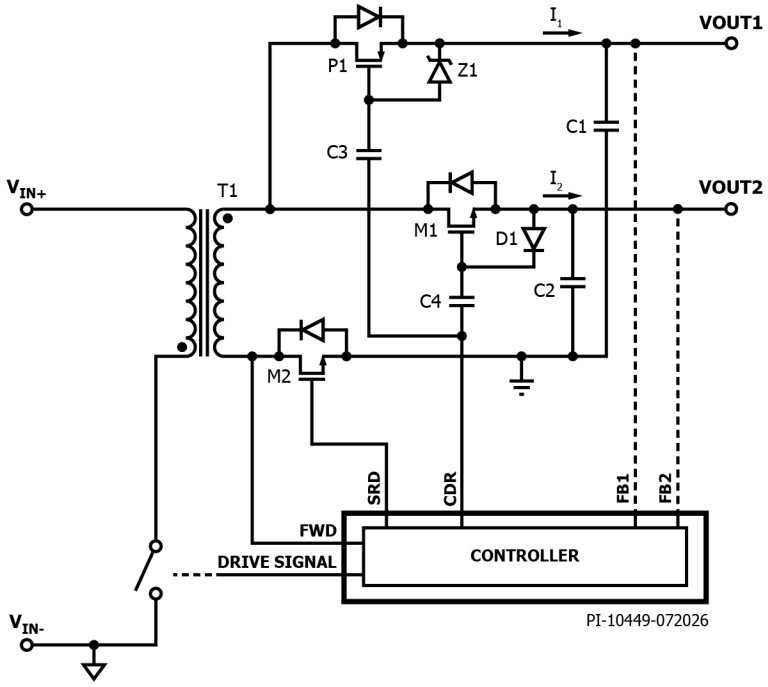

Figure 1. Example dual-output power converter with selection switches and circuitry to drive the selection switches.

Selection Switch	Switch Type	Body Diode Current-Blocking Function	V_{OUT1} Selected	V_{OUT2} Selected	Primary Conduction
P1	PMOS	Reverse Blocking (V_{OUT1} to V_{OUT2})	ON	OFF	ON
M1	NMOS	Reverse Blocking (V_{OUT2} to V_{OUT1})	OFF	ON	OFF
Signal CDR			LOW	HIGH	LOW

Table 1. Selection switch states for delivering current to a selected output.

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