

CAP400DG CAPZero-4

Zero Loss Automatic X-Capacitor Rapid Discharge IC

Product Highlights

- Blocks current through X capacitor discharge resistors when AC voltage is connected
- Automatically discharges X capacitors through discharge resistors when AC is disconnected
- Meets IEC 60335 X capacitor discharge to below 34 V in less than 1 second
- Supports X capacitor values up to 6 μF
- Simplifies EMI filter design – larger X capacitor allows smaller inductive components
- Meets safety standards for use before or after system input fuse
- >4 mm creepage on package and Printed Circuit Board (PCB)
- Self supplied – no external bias required
- High common mode surge immunity – no external ground connection
- High differential surge withstand – 900 V internal MOSFETs
- EN/IEC 62368-1 (NEMKO), UL 62368-1 (UL), and GB 4943.1 (CQC) certification

EcoSmart– Energy Efficient

- <0.75 mW consumption at 230 VAC for any capacitor value

Applications

- All AC-DC converters with X capacitors between 100 nF and 6 μF
- Appliances requiring ErP Lot 6 compliance
- Adapters requiring ultra low no-load consumption
- All converters requiring very low standby power

Description

When AC voltage is applied, the CAP400DG IC blocks current flow through the X capacitor safety discharge resistors, reducing the power loss to less than 0.75 mW at 230 VAC. When AC voltage is disconnected, the CAP400DG IC automatically discharges the X capacitors by connecting the series discharge resistors. This operation allows flexibility in the choice of the X capacitor to optimize differential mode EMI filtering and reduce inductor cost.

Designing with CAP400DG IC is simply a matter of selecting the appropriate external resistor values to meet the necessary X-capacitor discharge time.

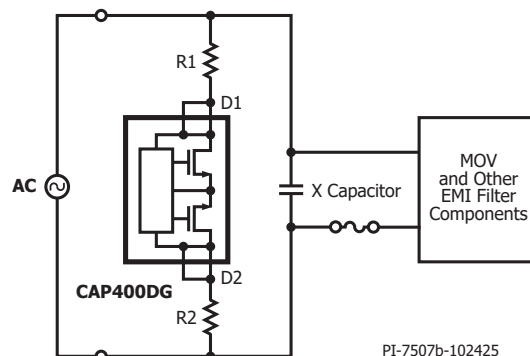


Figure 1. Typical Application.

Component Table

Product ²	BV _{DSS}	Total X Capacitance	Total Series Resistance ¹ (R1 + R2)
CAP400DG	900 V	100 nF to 6 μF	50 k Ω Minimum 100 k Ω Maximum

Table 1. Component Table.

Notes:

1. Nominal Values.
2. Package: D: SO-8.

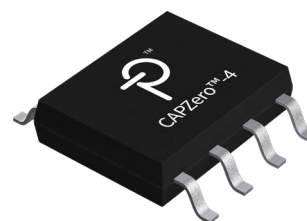


Figure 2. SO-8 D Package.

Pin Functional Description

The pin configuration shown in Figure 3 ensures that the width of the SO-8 package is used to provide a creepage and clearance distance of greater than 4 mm.

Although electrical connections are only made to pins 2, 3, 6 and 7, it is recommended that pins 1-4 and pins 5-8 are connected together on the PCB in two groups – see Key Applications section.

Key Application Considerations

Breakdown Voltage Selection

The CAP400DG device has a breakdown voltage of 900 V. In any instance the voltage on CAP400DG should not exceed 900 V. MOV should be added to provide adequate protection against differential surge. Recommend to add MOV after the fuse (Figure 4). This will clamp the differential surge voltage upon entry to the circuit.

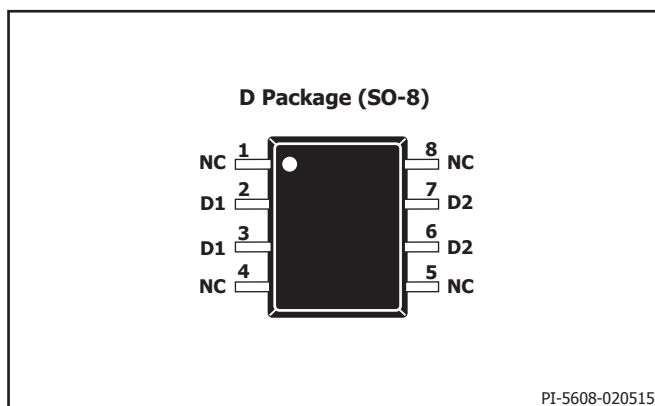


Figure 3. Pin Configuration.

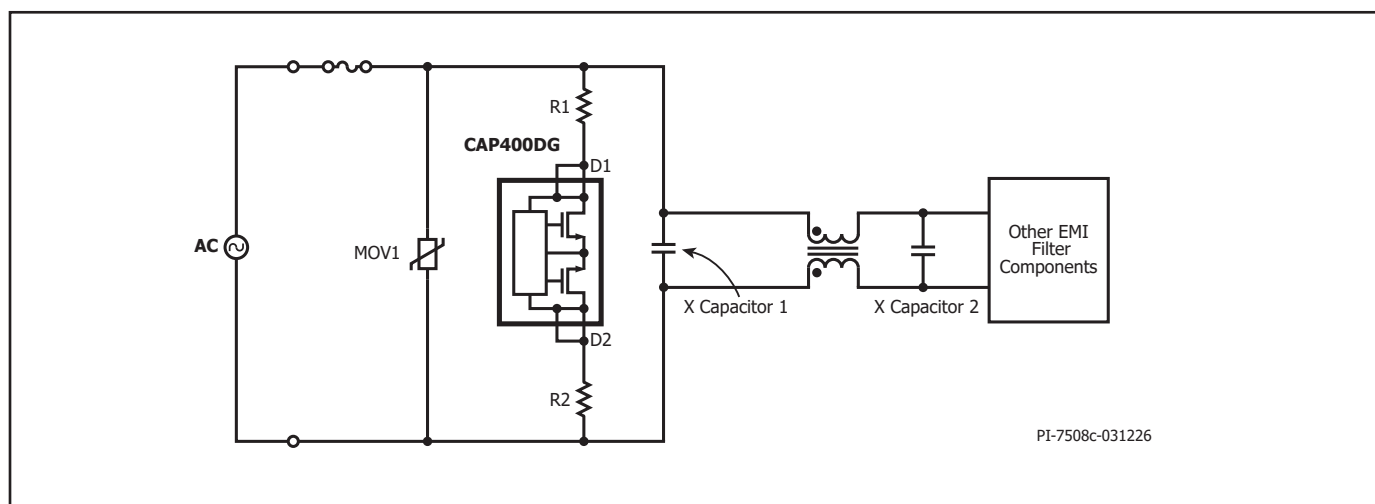


Figure 4. Placement of MOV, CAP400DG, and X capacitor.

PCB Layout and External Resistor Selection

Figure 5 shows a typical layout to use with a CAP400DG IC. The discharge resistance is provided by R1 and R2 which share the discharge energy, distributing losses during fault conditions (such as a short between D1 and D2). Resistors R1 and R2 are each rated for 50% of the system input voltage to ensure safe operation during single fault testing. If lower dissipation or lower voltage across each resistor is required during fault tests, the total external resistance can be divided between additional resistors.

Safety

The CAPZero™-4 IC meets safety requirements even if placed before the system input fuse. If a short-circuit occurs between D1 and D2, the system behaves in the same way as conventional passive discharge circuits.

It is not possible to create an open circuit fault condition through a single pin fault (such as created during the lifted-pin test) since two pins are connected to D1 and two to D2. If multiple disconnected pins create an open circuit, the condition is identical to an open circuit X capacitor discharge resistor in existing systems where CAP400DG is not used. If redundancy against open circuit faults is required, two CAP400DG ICs and R1 / R2 circuits can be placed in parallel.

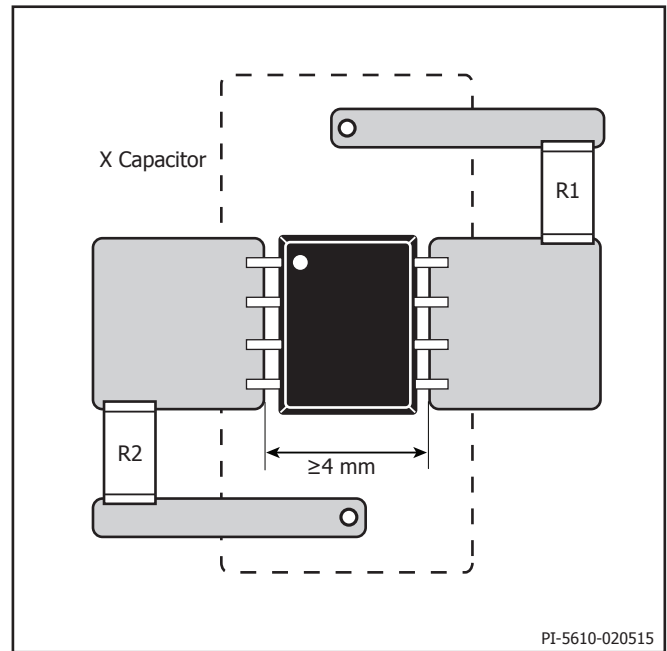


Figure 5. Typical PCB Layout.

Absolute Maximum Ratings⁽⁴⁾

DRAIN Pin Voltage ⁽¹⁾	900 V
DRAIN Peak Current ⁽²⁾	10.2 mA
Storage Temperature	-65 °C to 150 °C
Lead Temperature ⁽³⁾	260 °C
Operating Ambient Temperature.....	-40 °C to 125 °C
Maximum Junction Temperature.....	-40 °C to 125 °C

Notes:

1. Voltage of D1 pin relative to D2 pin in either polarity.
2. The peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
3. 1/16 in. from case for 5 seconds.
4. The Absolute Maximum Ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal ResistanceThermal Resistance: D Package⁽¹⁾:

(θ_{JA}).....	160 °C/W (Single layer JEDEC PCB)
(θ_{JC}).....	40 °C/W (Bottom)
(θ_{JC}).....	75 °C/W (Top)

Notes:

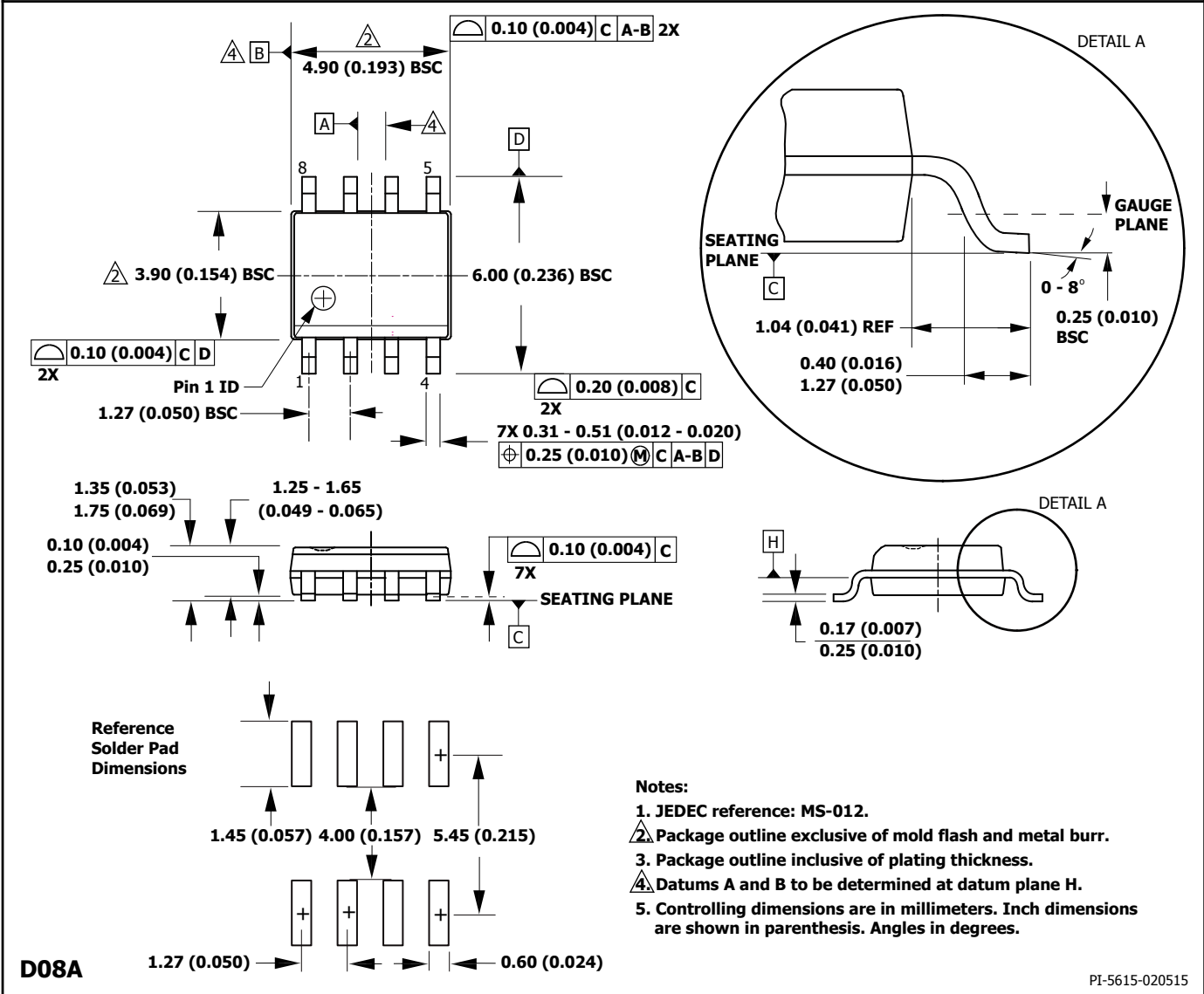
1. Reference thermal resistance test conditions: JEDEC JESD51-3, SEMI Test Method #G43-87, and MIL-STD-883 Method 10121.1.

Parameter	Symbol	Conditions $T_A = -40$ to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
AC Removal Detection Time	t_{DETECT}	Line Cycle Frequency 47 - 63 Hz	20	22	36	ms
Drain Saturation Current^{A,B}	I_{DSAT}	CAP400DG	5			mA
Supply Current	I_{SUPPLY}	$T_A = 25$ °C		2.5	3.4	μA
Power Consumption	Pin	$T_A = 25$ °C		600		μW

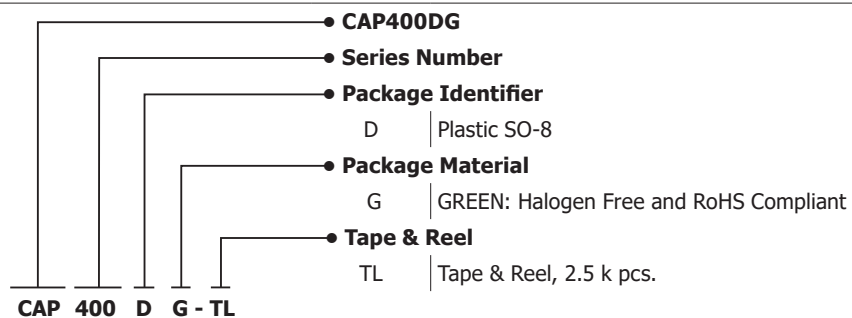
NOTES:

- A. Saturation current specification ensures a RC discharge characteristic at all voltages up to 265 VAC with the external resistor values specified in Table 1.
- B. Specifications are guaranteed by characterization and design.

SO-8 (D Package)



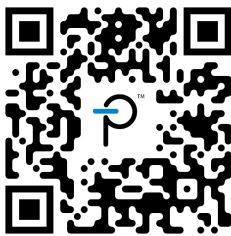
Part Ordering Information



Revision	Notes	Date
A	Initial release.	06/26

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