# An Enhanced PWM Control Technique Optimized for High Conversion Efficiency Across Input Line and Load

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# Abstract

This paper discusses an enhanced pulse width modulation (PWM) control technique that delivers very high efficiency across a wide range of input line and load conditions. This approach provides a method for increasing available power during standby, achieving high efficiency below 1 W input. Additional features improve transient response and avoid the problems caused by the bandwidth limitations encountered when using conventional barrier crossing techniques in the feedback loop. The simplicity and flexibility of the design allows for seamless integration into power systems from 15 W to over 190 W. This paper details the innovative aspects of this new approach and demonstrates its potential to better optimize the efficiency of power supply designs.

## 1. Practical Implementation

For offline converter, primary-side controlled flyback is the most common topology. A TL431 plus optocoupler circuit is the conventional method for providing isolated feedback. The IC-based flyback topology, shown in Fig. 1, offers a novel PWM control technique for reducing standby power consumption and improving transient response.

The IC combines a high-voltage power switch, along with primary-side controller in one device. TL431 converts output information to a feedback current, which is transmitted to the control input (C pin) by an optocoupler. The controller uses the feedback current information to modulate frequency and current limit. The control approach operates in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The controller also provides other power conversion functions and includes a frequency jitter oscillator, a current limit controller, an internal regulator, protection circuity for overvoltage and short-circuit detection, an input line sensing circuit, current limit selection circuitry, over-temperature protection, leading-edge blanking, and a silicon MOSFET power switch.

### 1.1 System Bandwidth

The majority of consumer facing power supplies employ a TL431 precision reference placed on the low-voltage secondary side of the converter to generate an error signal that is transmitted to the primary side of the isolation barrier via an optocoupler. The controller receives the phototransistor's feedback current via the control pin and uses it to perform output regulation. The impedance of control pin and the AC characteristic of optocoupler have significant impact to the closed control loop system, especially when designing for higher switching frequency or pushing the crossover frequency.

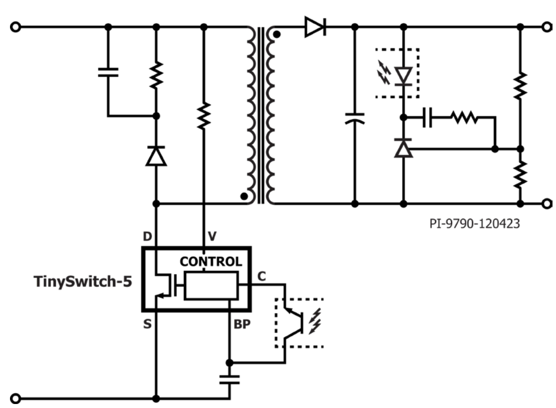


**Fig. 1 Typical flyback application**

Figure 2 shows the bandwidth of the optocoupler at different control pin impedances. The highest frequency that an optocoupler can transmit with the control pin impedance at 100 Ω is 200 kHz.

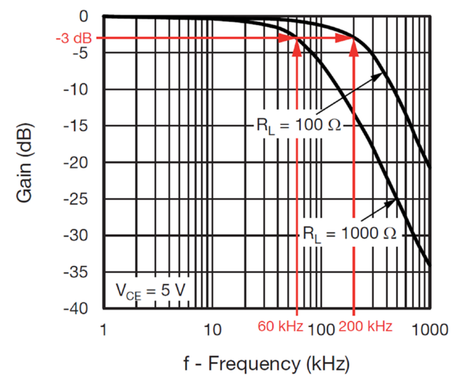


**Fig. 2 Gain vs. frequency of optocoupler**

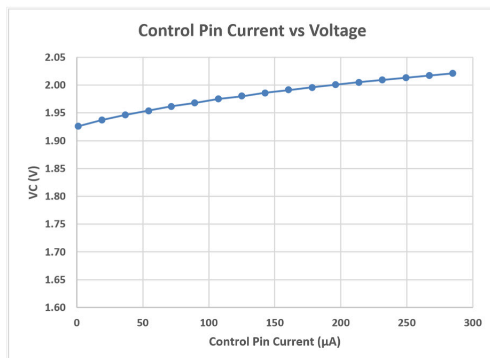


**Fig. 3 Constant control pin voltage**

The bandwidth of the optocoupler drops to 60 kHz when the control pin impedance increases to 1000 Ω. Figure 4 illustrates how the phase shifts as a function of frequency at different control input impedances. Therefore, to avoid the limitations of optocoupler bandwidth affecting transient response, control impedance needs to be low.

The typical approach to reduce the impedance of the control pin is to increase the size of active circuitry devices and reduce the value of the resistors. The downside is that electrostatic discharge (ESD) performance becomes worse. Also, it may be impractical and costly to keep increasing the size of the interface circuitry. Finally, reducing resistance means increasing overall power consumption.

To avoid the bandwidth limitation problem caused by the optocoupler pole, the control pin CPIN impedance is kept at ~200 Ω. A unique design technique is implemented to not only have a low impedance pin, but to also pass ESD and minimize IC consumption.

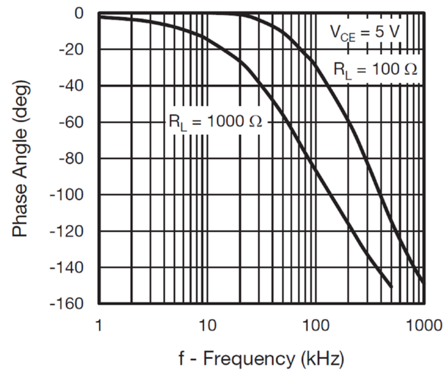


**Fig. 4 Phase vs. frequency of optocoupler**

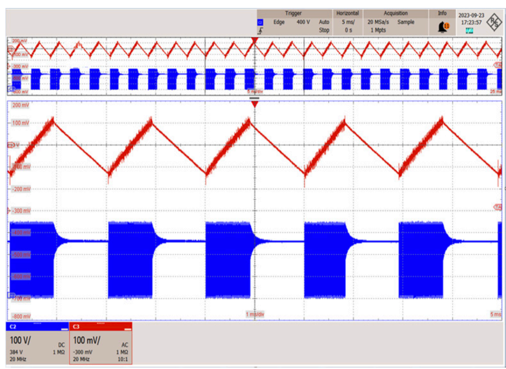

**Fig. 5 Output voltage ripple in burst mode**

In this approach, the optocoupler is driven by a BP pin, which is a constant voltage source, shown in Fig. 1. The collector of the phototransistor is connected to the control pin CPIN which is constantly regulated at 2 V, shown in Fig. 3. This implementation minimizes the Miller Effect which further reduces the impact of the optocoupler pole.

## 1.2 Standby Load Consumption

Under the latest European Union (EU) regulations (Regulation 2023/826), most electronic devices in standby or off-mode must not exceed 0.5 W power consumption. Devices with display information while in standby mode can consume up to 0.8 W.  Additional reductions are planned for 2027 to further decrease standby power consumption.

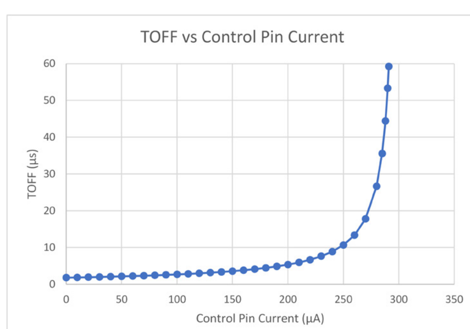


**Fig. 6 Control pin current vs. off-time**

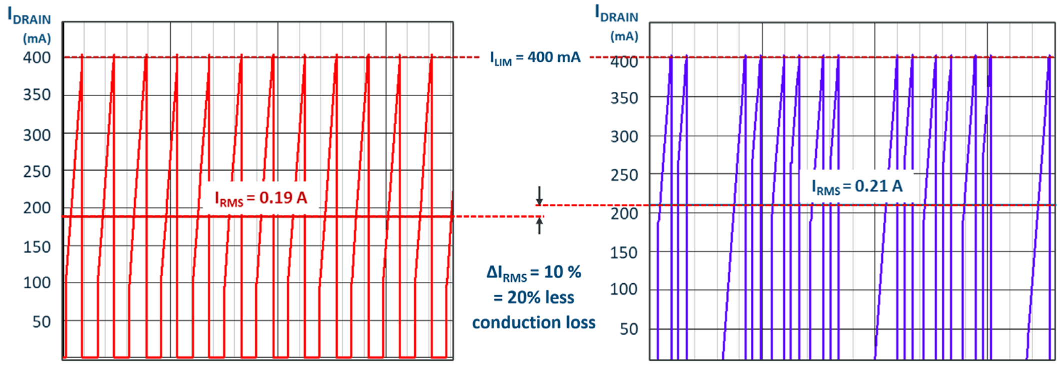


**Fig. 7 Uniform switching vs. burst mode switching pattern**

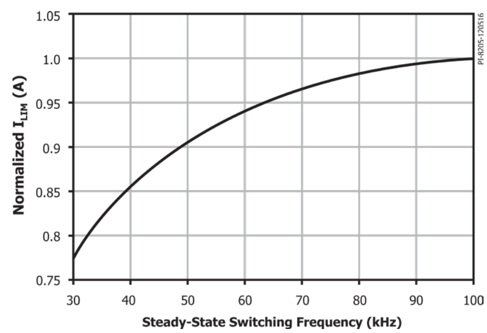


**Fig. 8 Normalized current limit vs. frequency**

To minimize no-load and standby load consumption, the traditional method is to use a burst mode function. When operating in burst mode, the controller enables a group of switching pulses for tburst_on then stops switching for tburst_off. This control approach has disadvantages, such as bad output voltage regulation or increased output ripple, and adds complexity to the design. New control eliminates the implementation complexity to achieve low no-load and standby load consumption.

## 2. Principle of Operation

The controller employs variable off-time and variable current limit control. The key element is an off-time modulator that converts the analog feedback current (sampled via the optocoupler) to the duration of the off-time, which is made proportional to that feedback current. This algorithm produces longer off-time as the output load reduces.

The controller integrates the feedback current and converts it to off-time information. At the end of the off-time cycle, the off-time modulator initiates an on-cycle request to turn on the integrated power switch. The power MOSFET is turned off when the drain current reaches the current limit threshold.

As shown in Fig. 6, the controller typically operates with a control pin current below 300 μA. Once the control pin current reaches 300 μA, the off-time tends towards infinity. The control pin current for the no-load condition then approaches 300 μA.

The primary switch current limit is set according to the duration of the off-time between switching cycles. The current limit threshold decreases as off-time increases. This characteristic produces a current limit that increases as the switching frequency (and output load) increases. Switching cycles have a maximum peak current approaching 100 percent current limit at 100 kHz switching frequency. Shown in Fig. 8, when switching frequency increases from 30 kHz to 100 kHz, the maximum primary switch current increases from 75 percent to 100 percent of the current limit. The increase in peak current results in flat efficiency across line and load.

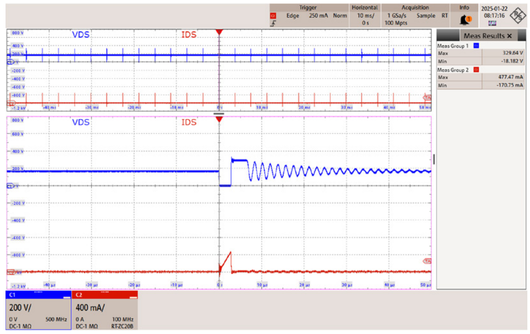


Fig. 9 No-load switching waveform


Fig. 10  0 percent to 100 percent load transient response

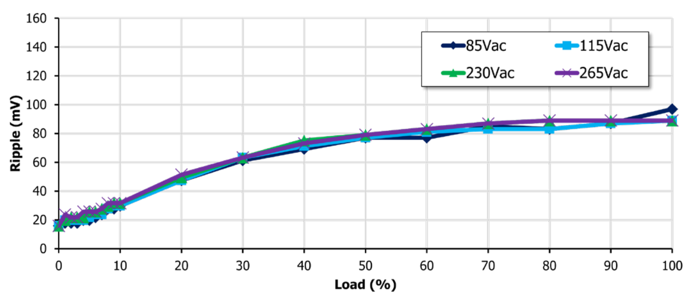


Fig. 11 Output voltage ripple

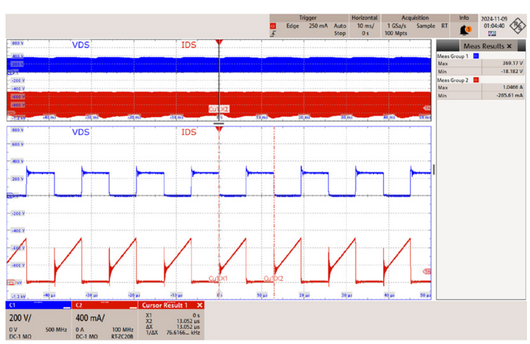


Fig. 12 Full-load switching waveform

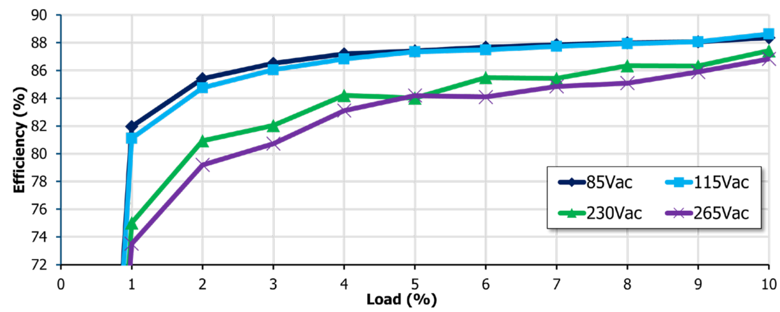


**Fig. 13 Light-load efficiency**

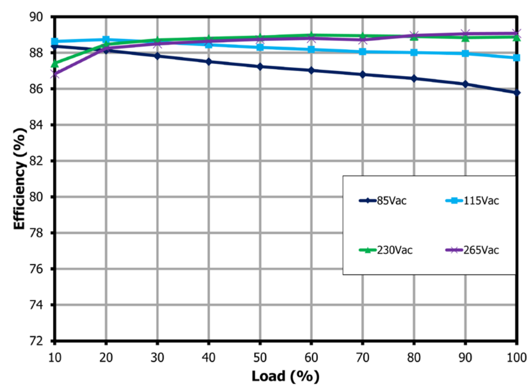


**Fig. 14 Output voltage regulation**

The maximum switch current gradually reduces to 30 percent of the full current limit as the load decreases. The time between switching cycles will also continue to increase (switching frequency will reduce). This characteristic produces the seamless transition between normal load and standby (light-load) conditions. Switching pulses are uniformly spread out. The illustration in Fig. 7, shows that with the same peak current, the uniform switching pattern produces 10 percent lower RMS current compared to the burst mode switching pattern.

At the end of the off-time cycle, the off-time modulator initiates an on-cycle request to turn on the integrated power switch. Drain current of power MOSFET rises with the slope determined by input voltage and primary inductance. Once drain current reaches the current limit reference, controller turns off the power MOSFET and start the off-time cycle.

## 3 Experimental Results

### 3.1 Light-Load Consumption

Figure 13 shows the excellent light-load (1 percent to 10 percent load) efficiency performance of this approach. The 100 percent output load is 36 W. At 1 percent load, the efficiency is 75 percent at 230 VAC input. That means that to meet the latest EU regulations for 500 mW input power, this new PWM control approach delivers 360 mW to the output.

### 3.2 Output Voltage Regulation

Figures 11 and 14 show outstanding output voltage regulation. Across line input voltage and output load conditions, the regulation is less than ±1 percent. Additionally, output voltage ripple maintains less than 100 mV which is 1 percent of output voltage across the combinations of line input voltage and output loads. The output voltage ripple is below 40 mV when output load is less than 10 percent. This reflects the benefits of the new PWM control technique when bursting is not required.

Figures 9 and 12 show the switching waveforms at no load and full load conditions. At full load conditions, peak current is 1000 mA and switching frequency is 80 kHz. When output load reduces to zero, the controller reduces the switching frequency to 300 Hz and peak current to 400 mA. Switching is stable even at no load which ensures high light-load efficiency and better output voltage regulation.

### 3.3 Load Transient Response

Figure 10 illustrates the load transient response of the controller at 115 VAC. The load step is from no load to 100 percent load. The fast loop response indicates the advantage of the control engine in improving transient response. During transient, the output voltage excursion is less than ±1 percent, with <100 mV output undershoot and overshoot.

## 4. Conclusion

The innovative PWM control described in this article represents a significant step forward in power management. By utilizing a modulator that translates feedback current provided by the optocoupler to off-time, this controller achieves high efficiency, especially under light-load conditions.

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