Achieving High Efficiency Across Load in a Compact 2-Stage 140 W Flyback USB PD 3.1 Notebook Adapter

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Abstract

Flyback converters are widely used for their simplicity and cost effectiveness. However, when output power exceeds 100 W, meeting regulatory efficiency requirements for light- to full-load can be difficult. The primary sources of efficiency losses are switching losses in the primary power switch and conduction losses, particularly due to hard switching.

This paper explores methods to reduce switching and conduction losses through component selection and how transformer leakage inductance can improve efficiency. Also, optimizing zero voltage switching (ZVS) at different load points and the use of external circuits to minimize power dissipation at light-loads will be explored.

1. Introduction

The front end of a conventional 140 W USB PD 3.1 notebook adapter consists of a boost PFC stage, followed by a flyback converter that delivers up to 5 A across various output voltages: 28 V, 20 V, 15 V, 12 V, 9 V, and 5 V. Efficiency requirements for external power supplies, such as notebook adapters, are becoming increasingly stringent as government and regulatory bodies continue to raise standards to reduce energy consumption and lower carbon footprints.

In addition to regulatory demands, OEMs require high efficiency at full-load and under low input voltage conditions. This is driven by the increasing need for compact and lightweight power supplies that are easier to carry and fit into tight spaces. High-efficiency adapters also generate less heat, which is critical for designing smaller, thermally optimized power supplies.

The following methodology outlines key strategies for achieving high efficiency across different load conditions.

2. Methodology

2.1 Input Rectifier and EMI Filter

At 140 W output power, conduction loss in the input common-mode choke (CMC), differential choke, and bridge rectifier becomes significant, especially at extremely low input voltage (90 VAC). The input current flowing through these components is approximately 1.7 A, resulting in high VI and I^2R losses. The first step in reducing EMI filter conduction loss is to minimize differential and common-mode noise by employing shield windings in the flyback transformer, implementing a proper PCB layout with EMI considerations, and selecting appropriately sized input X-capacitors and Y-capacitors. Figure 1 shows the shield windings technique implemented between primary and secondary windings to sufficiently reduce common mode noise minimizing the size and DC resistance of input common mode choke [1].

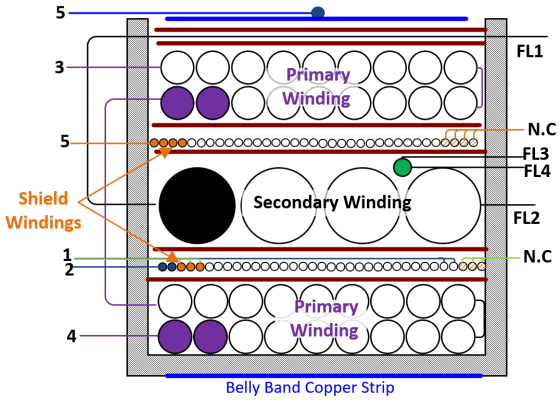

Fig. 1 Shield windings in flyback transformer

Using a full-wave active bridge rectifier instead of a conventional diode bridge can significantly improve efficiency, reducing power loss by approximately 0.8 W at low-line input voltage (90 V). However, this comes at a higher cost due to the use of four high-voltage power MOSFETs with low $R_{DS(ON)}$ in addition to the active bridge controller IC.

For a cost-effective alternative, selecting bridge diodes with a low forward voltage drop (Vf) can also improve efficiency. Higher current-rated diodes typically exhibit lower Vf at high currents compared to lower-rated diodes. In this case, upgrading from a 1 kV, 4 A bridge rectifier to a 1 kV, 8 A version resulted in an efficiency gain of approximately 0.07 percent.

Figure 2 illustrates the optimizations made to reduce conduction losses in the input rectifier and EMI filter, along with the corresponding power loss reduction and efficiency improvements achieved.

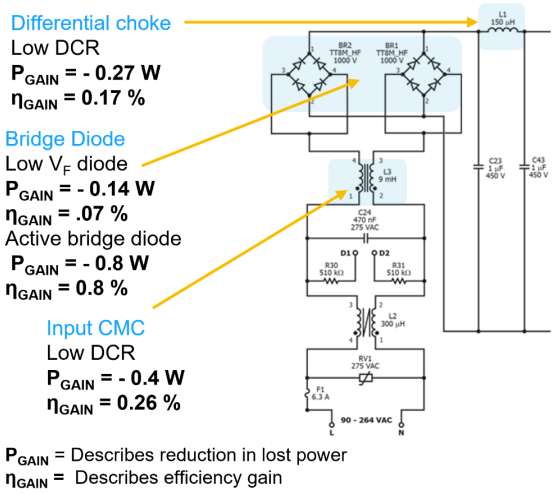

Fig. 2 Input rectifier and EMI filter optimization [2]

2.2 Boost Power Factor Corrector

The boost power factor corrector (PFC) utilizes the HiperPFS™-5 controller IC, which incorporates a GaN MOSFET, making it ideal for high efficiency and compact form factor solutions. In addition, it incorporates an automatic X-capacitor discharge circuit to reduce standby power, further enhancing light-load efficiency [3].

Key PFC components to consider when designing for high efficiency include the boost inductor, boost diode, and bulk capacitor. The boost inductor experiences higher losses at extremely low-line conditions due to DCM operation, and higher switching frequencies increase its AC resistance. Using Litz wire helps reduce AC resistance caused by skin and proximity effects. For the boost diode, an ultrafast diode with a low forward voltage drop should be used to minimize conduction losses. The bulk capacitor should have low ESR to reduce power dissipation. Figure 3 illustrates the reduction in power loss and the efficiency gain achieved after optimizing key components in the boost PFC [1].

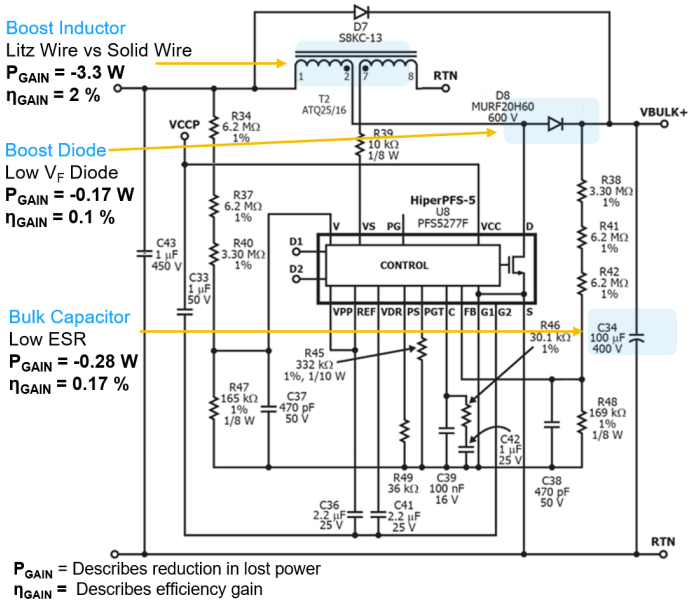

Fig. 3 Boost PFC efficiency improvements [2]

2.3 Low PFC Output Voltage at Low Line Reduces Flyback Switching Loss

At extreme low input line (90 VAC), the 140 W 2-stage notebook adapter experiences its lowest full-load efficiency due to high conduction losses in the PFC circuit and input EMI filter. One way to improve efficiency under low-line conditions is by reducing the PFC output voltage (bulk voltage) while maintaining a high-power factor. Lowering the PFC output voltage at lower input voltages reduces the drain-to-source voltage (VDS) across both the flyback primary MOSFET and the synchronous rectifier (SR) FET, leading to lower switching losses during turn-on and turn-off transitions.

The PFC control IC (HiperPFS-5) incorporates a boost follower feature that dynamically adjusts the PFC output voltage based on the input peak voltage. When the input voltage is detected as low-line, the target output voltage is reduced; when the input voltage is sensed as high-line, the PG pin in Fig. 4 is shorted to ground by an internal switch increasing the target output voltage. The low-line and high-line hysteresis thresholds are set at 140 VAC and 170 VAC, respectively [3].

The following equations define the PFC output voltage based on the schematic in Fig. 4. Equation (1) describes the PFC output voltage at high-line input, where the feedback sense resistors RBF and RDWN are connected in parallel by the internal switch to increase the PFC output voltage [3].

$$V_O = V_{FB}\, x \left(\frac{R_{UPP} + R_{BF}//R_{DWN}}{R_{BF}//R_{DWN}}\right) \qquad (1)$$

At low-line input, the feedback resistor RBF is disconnected from ground by the internal switch, causing the target PFC output voltage to decrease. Equation (2) defines the PFC output voltage under low-line conditions [3].

$$V_O = V_{FB}\, x \left(\frac{R_{UPP} + R_{DWN}}{R_{DWN}}\right) \qquad (2)$$

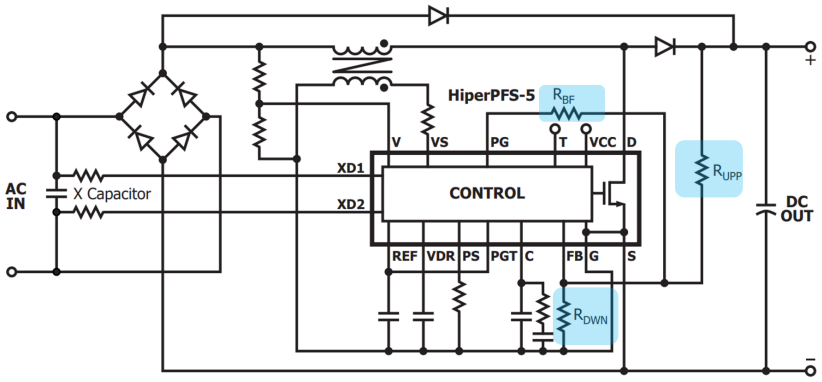

Fig. 4 PFC with line dependent VOUT [3]

The efficiency curve comparison in Fig. 5 shows an approximate 0.22 percent improvement at low-line operation with a reduced PFC bulk voltage.

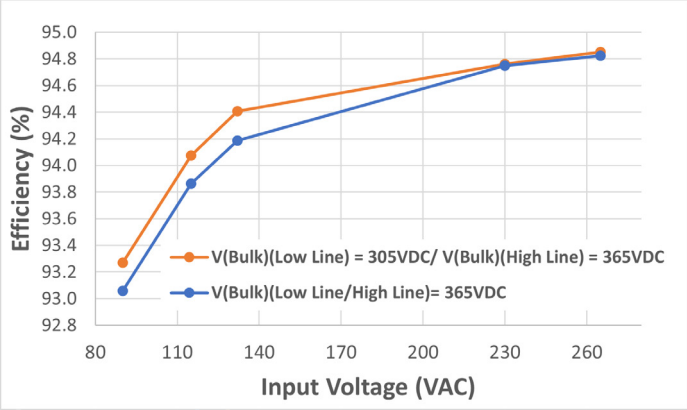

Fig. 5 Efficiency with a boost follower PFC

2.4 Flyback Component Optimization

The flyback controller IC used in this design is the InnoSwitch™5-Pro, which incorporates primary and secondary side control along with a GaN MOSFET, making it highly suitable for compact form factor solutions. Due to hard switching, the flyback peak current in the primary and secondary windings is high, generating significant copper loss. Litz wire should be used for both the primary and secondary windings to reduce AC resistance caused by proximity and skin effects, while the winding structure should be carefully designed to minimize leakage inductance. High leakage inductance increases switching losses in both the primary MOSFET and the synchronous rectifier (SR) FET.

Leakage inductance in a flyback transformer is primarily caused by poor coupling between the primary and secondary windings, which occurs due to physical separation between them. The greater the distance between the primary and secondary windings, the weaker the magnetic coupling, leading to higher leakage inductance [1].

Figure 6 illustrates how an evenly split primary winding and a reduced number of secondary winding layers significantly reduce leakage inductance by improving magnetic coupling, thereby enhancing efficiency.

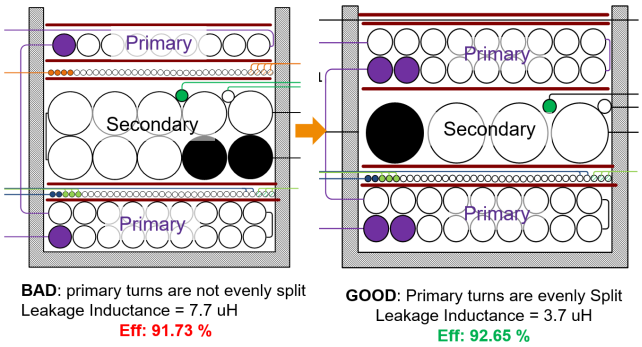

Fig. 6 Low leakage flyback transformer

The primary bias supply for the flyback controller IC must be optimized to prevent both under-supply and over-supply conditions. Under-supply causes the high voltage drain to internally power the primary side of the IC, which is inefficient, particularly at high input line voltages. Conversely, over-supply increases power dissipation in the IC's internal shunt regulator. Additionally, power loss reduction can be achieved in the primary snubber by leveraging the primary MOSFET's 725 V VDS rating during transient operation. Figure 7 illustrates the efficiency improvement and power loss reduction achieved after optimizing the flyback primary components.

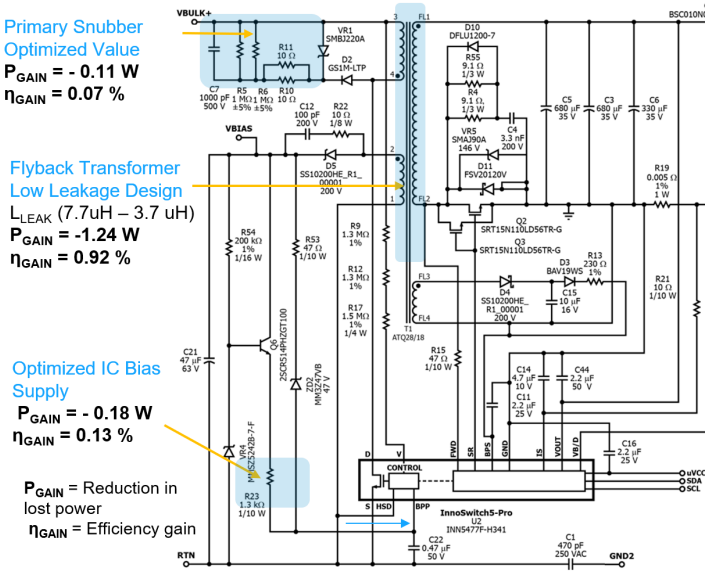

Fig. 7 Flyback primary-side optimization [2]

On the secondary side, adding a rectifier diode (D10) across the resistor of the synchronous rectifier (SR) FET RC snubber significantly reduces power dissipation in the snubber resistor. As shown in the schematic in Fig. 8, the rectifier diode (D10) bypasses the discharging current from the snubber capacitor during the SR FET turn-on phase, thereby reducing power dissipation in the snubber resistor. Additionally, adding a secondary bias to the 28 V output minimizes headroom loss on the 4.5 V linear regulator within the secondary side of the flyback control IC. Two SR FETs are required for a 5 A output current load to reduce conduction losses caused by SR FET RDSON. Figure 8 illustrates the efficiency gain and power loss reduction achieved after implementing these improvements in the secondary side.

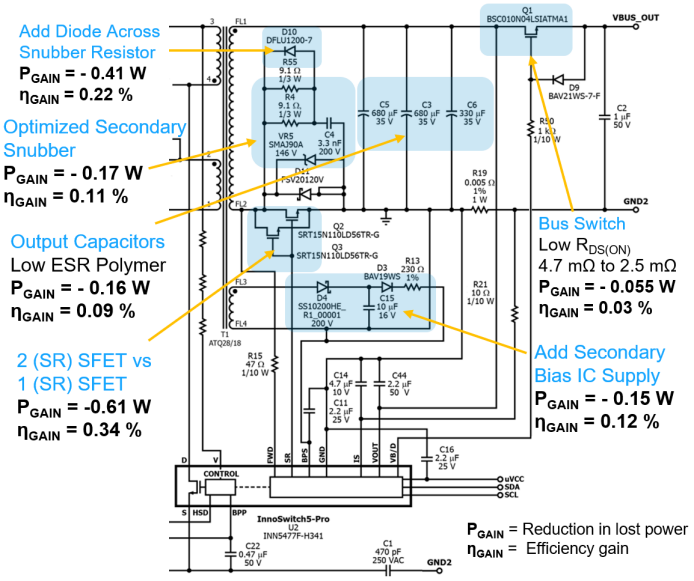

Fig. 8 Flyback secondary-side optimization [2]

2.5 Optimizing the Flyback Zero Voltage Switching Operation

To minimize flyback switching losses in DCM mode, the InnoSwitch5-Pro controller IC employs SR-based zero voltage switching (ZVS). This is achieved by momentarily turning on the (SR) FET on the secondary side to drive the magnetizing inductance into negative polarity. A delay is then introduced, allowing the magnetizing inductance current to pull the drain voltage down to zero before the primary switch turns on. Waveforms on Fig. 11 describes the flyback SR-ZVS operation.

The SR-ZVS on-time and delay time are adjustable via I^2C in ~85 ns increments, depending on output voltage and load current, to optimize efficiency across varying load conditions. Once these parameters are finetuned for different output voltages (5 V to 28 V), they are programmed into the USB PD control IC as on count and delay count values, which dynamically adjusts the SR-ZVS on-time and delay-time in response to output voltage changes. Equations (3) and (4) define the SR-ZVS on-time and SR-ZVS delay-time, respectively [2].

$$On\ Time \approx\ 170ns\ + 85ns(on\ count) \quad (3)$$

$$Delay\ Time \approx\ 85ns\ + 85ns(delay\ count) \quad (4)$$

The schematic in Fig. 9 and the waveforms in Fig. 11 illustrate the current direction during a controlled SR-ZVS on-time, where the (SR) FET momentarily biases the magnetizing inductance [2].

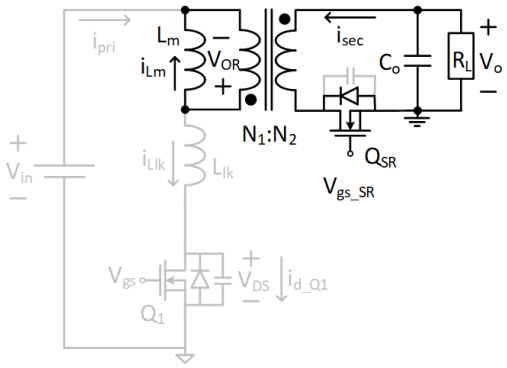

Fig. 9 $t_0 - t_1$ (t_{ON_SR})

The waveforms in Fig. 11 illustrate that a controlled SR-ZVS delay time allows the magnetizing current to naturally pull the drain voltage to zero before the primary switch turns on. This ZVS operation is exclusive to DCM and is automatically disabled by the controller IC (Innoswitch5-Pro) in continuous conduction mode (CCM). The schematic in Fig. 10 shows how the voltage polarity across the primary winding reverses as the SR FET turns off, enabling the VDS voltage stored in COSS to discharge before the primary switch turns on [2].

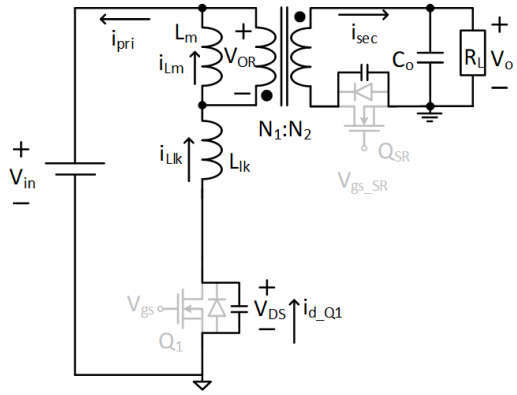

Fig. 10 $t_1 - t_2$ (t_{OFF_SR})

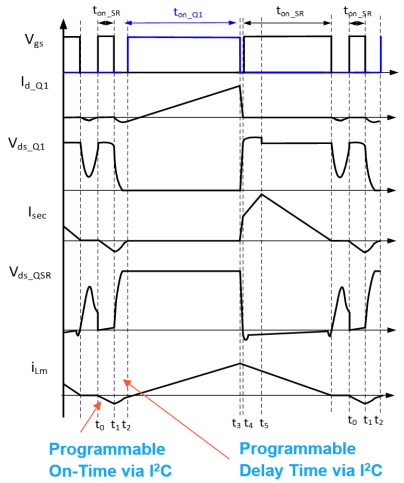

Fig. 11 SR-ZVS waveforms

Figure 12 shows the waveform when ZVS is disabled. The primary drain voltage is high at the moment of switch turn-on, resulting in increased switching losses.

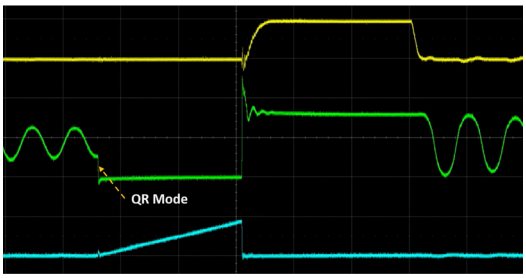

Fig. 12 ZVS disabled (QR mode)

Figure 13 shows the flyback switching waveform with insufficient SR on-time, which results in a small negative magnetizing current that may be inadequate to pull down the drain voltage. Similarly, an insufficient delay time will not allow enough time to reduce the drain voltage before the primary switch turns on, leading to switching losses.

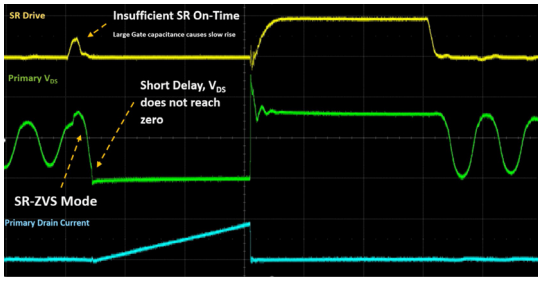

Fig. 13 Insufficient SR on-time

Figure 14 shows long SR on-time can cause excessive negative magnetizing current, leading to potential efficiency losses. This can result in the primary switch turning on when voltage across it is already rising leading to increased switching losses.

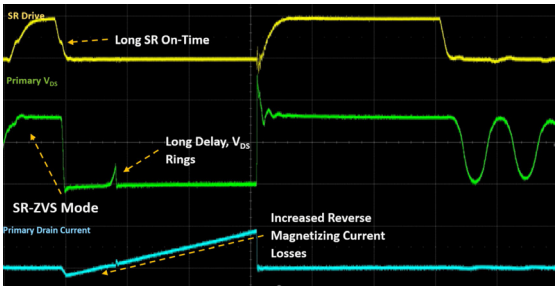

Fig. 14 Long SR on-time

Figure 15 shows the waveform of the optimized SR-ZVS on-time and delay-time, achieving ideal zero voltage switching (ZVS) and significantly reducing switching loss.

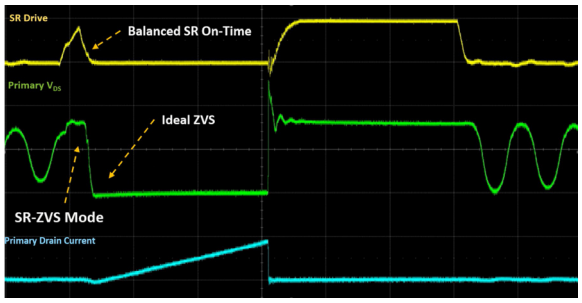

Fig. 15 Optimized SR on-time and delay-time

Figure 16 shows the efficiency curves comparing different SR-ZVS on-time and delay-time settings, illustrating how optimized efficiency across the load is achieved at a 28 V, 5 A output with a 115 V input. This optimization has been applied across output voltages ranging from 5 V to 28 V.

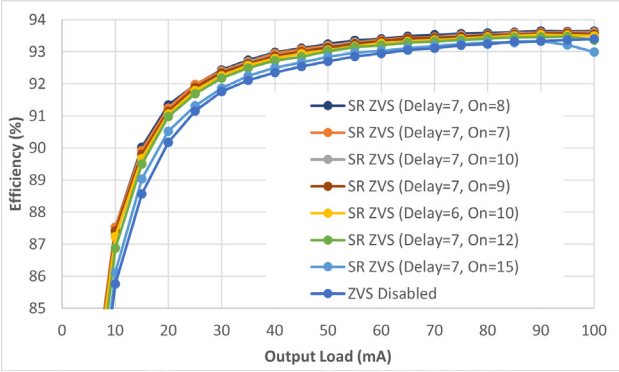

Fig. 16 Efficiency curves at 28 V, 5 A

2.6 PFC Turn-Off With Flyback Control IC Adaptive Bias Supply

In a design for USB PD 3.1 notebook adapter using a flyback topology, we normally use a regulated primary bias supply to the flyback controller IC where the linear regulator provides a regulated bias current across the load. The problem is that, at light-load condition or standby mode, the unwanted bias supply is dissipated in the shunt regulator internal to the controller IC significantly reducing the light-load efficiency. The measured power dissipation by supplying too much bias current to the flyback control IC at light-load condition is around 50 mW.

A PFC turn-off circuit is implemented to improve efficiency at light-load and no-load conditions where power factor correction is not required. This is achieved by disabling the VCC bias supply of the PFC control IC (HiperPFS-5) using an optocoupler connected to the base-collector of the PFC linear regulator transistor (Q6). The optocoupler is controlled by the USB PD control IC on the secondary side, based on a programmable threshold set in the firmware.

In this design, the PFC remains off when the output voltage is 5 V or 9 V. For output voltages between 12 V and 28 V, the PFC turns off at approximately 35 W and stays off down to no load. It turns back on when the output power reaches 40 W, maintaining operation up to full.

The PFC linear regulator is also used to dynamically provide an adaptive bias supply to the flyback control IC from light-load to full-load, reducing power dissipation by 45 mW. This is crucial for meeting EU eco-design directives for Energy-related Products (ErP) Lot 6 standards.

Figure 17 shows the PFC turn-off circuit, which is controlled by the USB PD control IC on the secondary side and provides a dynamic bias supply to the primary side of the flyback controller IC (InnoSwitch5-Pro) by connecting D12 and R56. From 40 W to full load, the bias current is IBIAS = IBIAS1 + IBIAS2, supplying approximately 5 mA to the IC. When the output load is around 35 W, the bias current is IBIAS = IBIAS2, providing approximately 600 µA primary bias current to the flyback control IC.

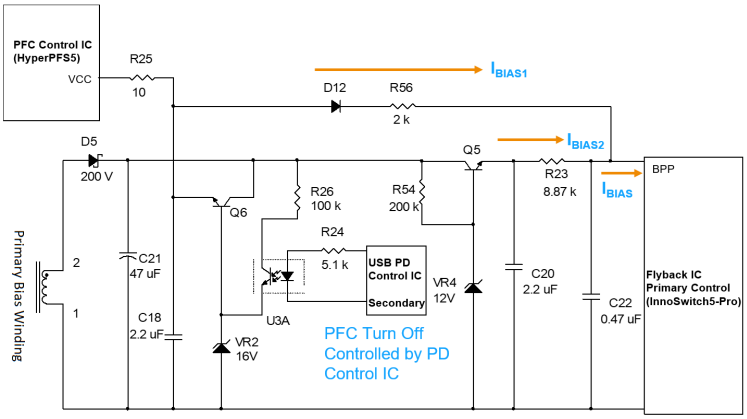

Fig. 17 PFC turn-off with adaptive IC bias circuit

Figure 18 illustrates a significant 11 percent improvement in light-load efficiency with the adaptive primary bias.

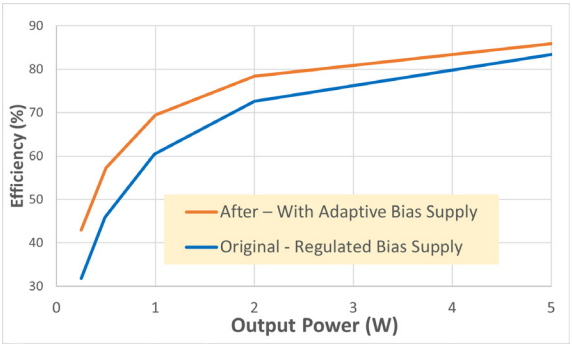

Fig. 18 Efficiency with adaptive primary bias

2.7 Low Voltage USB PD Control IC Bias Supply

Conventionally, the external bias supply of the USB PD control IC is connected directly to VBUS, which is the flyback output voltage ranging from 28 V to 5 V. This setup results in high power dissipation at higher output voltages due to headroom loss in the 3.3 V linear regulator internal to the PD control IC. To minimize headroom loss, the external bias supply voltage must be lowered.

The circuit diagram in Fig. 19 illustrates an implementation that provides a low-voltage bias supply for output voltages ranging from 28 V to 12 V, derived from the secondary bias supply. The secondary bias winding consists of just two turns, ensuring a low secondary bias voltage at high output voltages. However, at output voltages of 9 V and 5 V, the secondary bias voltage becomes insufficient. To compensate, a 4.5 V MOSFET regulator (Q23) is activated, supplying a stable 4.5 V bias to the PD control IC at these voltages. This setup significantly reduces power dissipation in the PD control IC, particularly during high output voltage conditions with light loads.

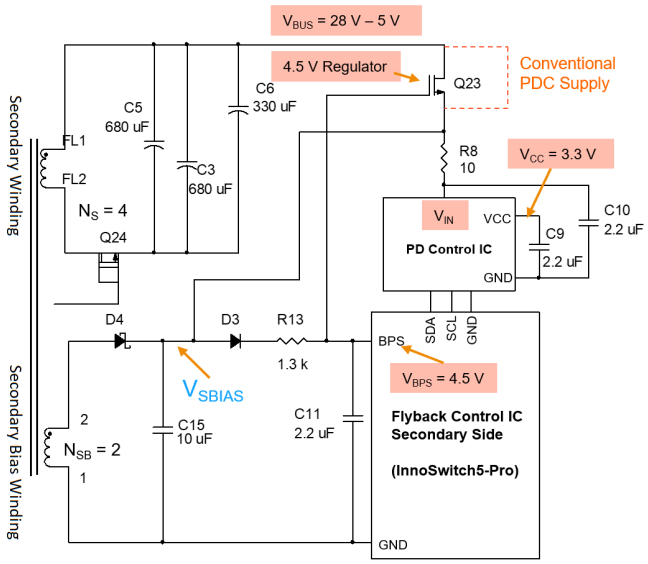

Fig. 19 Low voltage PD control IC bias supply

Figure 20 illustrates a significant 7 percent improvement in light-load efficiency when using an external bias supply for the low-voltage USB PD control IC, compared to direct connection to the VBUS.

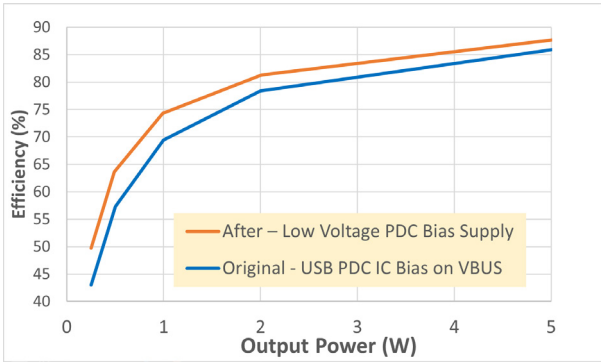

Fig. 20 Efficiency with low-voltage PDC IC bias

3. Results

The following test results demonstrate that the consolidated improvements have achieved high efficiency while meeting various efficiency regulatory requirements. The unit also passed the thermal test with the use of proper thermal management implementations.

Figure 21 illustrates the 140 W USB PD 3.1 notebook adapter, highlighting key components that have been optimized to achieve high efficiency.

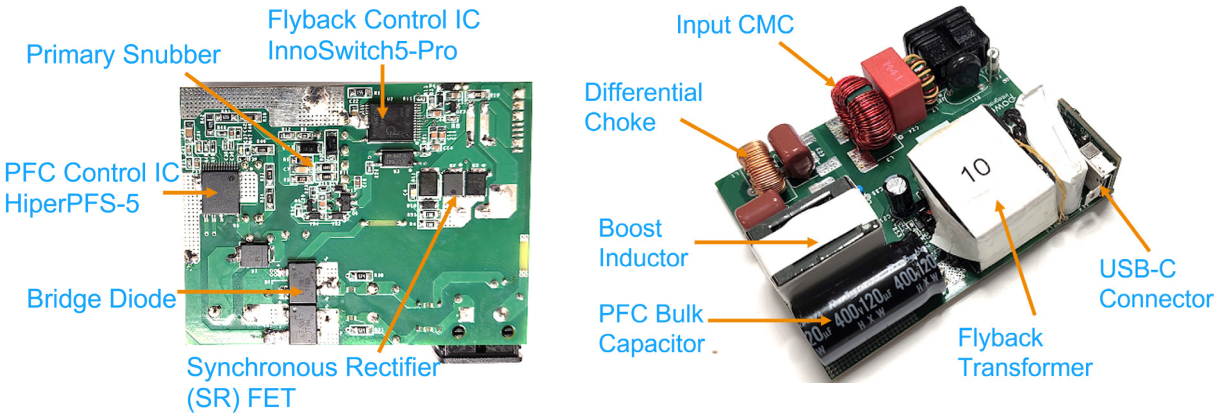

Fig. 21 140 W USB PD 3.1 notebook adapter

Figure 22 shows the efficiency across the load at 28 V output at an input voltage of 230 VAC 50 Hz is almost flat across the output load range.

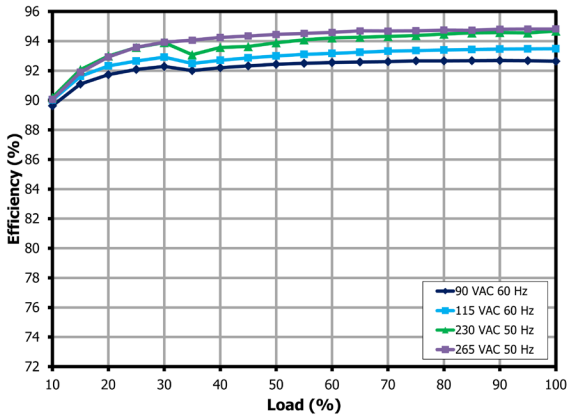

Fig. 22 Efficiency performance at 28 V / 5 A

The average efficiency at different output loads, as shown in Figs. 23 and 24, meets the DoE VI and CoC Tier 2 requirements.

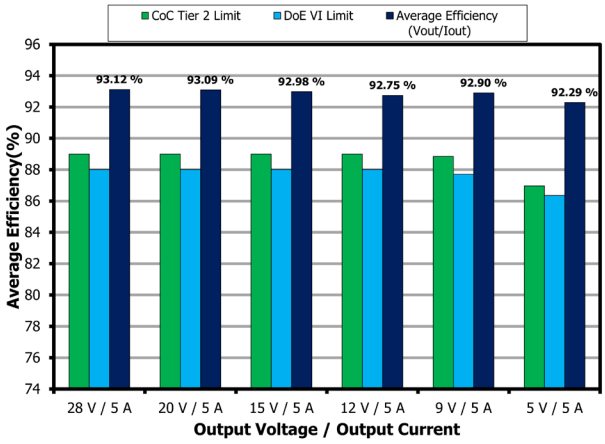

Fig. 23 Average efficiency at 115 VAC 60 Hz

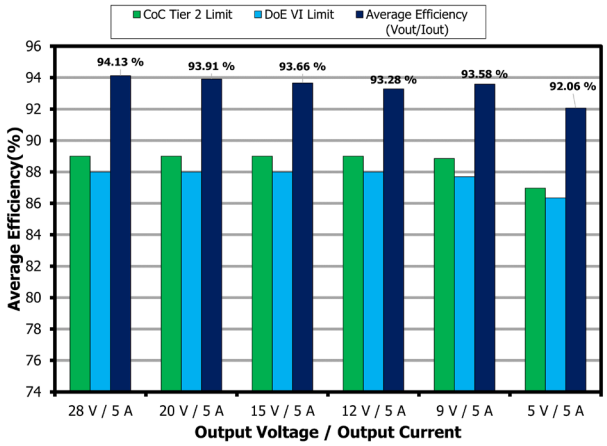

Fig. 24 Average efficiency at 230 VAC 60 Hz

The light-load efficiency performance data at a 20 V output, as shown in Fig. 25, demonstrates that the unit meets the < 500 mW input power ErP Lot 6 Tier 2 requirements at a 250 mW output standby load [4].

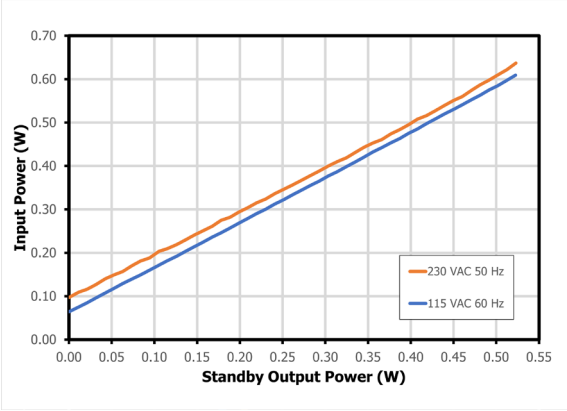

Fig. 25 Light-load efficiency at 20 V output

References

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