

# Application Note AN-300

## Qspeed™ Family



### HTRB Reliability Testing

#### Abstract

High Temperature Reverse Bias (HTRB) testing is often used to verify the reliability of power semiconductor diodes. This application note describes the requirements of a valid HTRB test for power semiconductor diodes. It also proposes an effective strategy for performing an HTRB test that requires minimal supervision while assuring that no parts are inadvertently destroyed by unintentional overheating.

#### Introduction

HTRB testing is an accelerated life-test for power semiconductor diodes that is often used to verify the robustness of the devices themselves and the reliability of their assembly and packaging. It artificially ages the devices under test (DUTs) by making them block a voltage that is close to their maximum rated reverse breakdown voltage ( $V_{RRM}$ ) while close to their maximum rated junction temperature ( $T_{JMAX}$ ). As the maximum junction temperature of any power semiconductor is approached, adequate removal of heat from the device package is critically important to prevent thermal runaway from occurring and driving the devices into self-destruction. This is particularly true when there is very little difference between the ambient temperature ( $T_A$ ) and the junction temperature ( $T_J$ ) of the device. The most significant factor of any HTRB test strategy involves affixing a heatsink to each device that is put on test. Heatsinking the DUTs achieves three objectives. 1) For a properly designed test, it eliminates the need to measure DUT case temperatures to ensure that an acceptable junction temperature is being maintained throughout the duration of the test. 2) It ensures a fairly consistent junction temperature for all of the DUTs in the test environment. 3) It minimizes the likelihood of accidental device

destruction due to thermal runaway driven overheating. The appendix suggests a potential heatsink vendor and the part number of a heatsink that should be adequate for the HTRB testing of diodes mounted in TO-220 packages.

#### Valid HTRB Test Conditions

JEDEC specification JESD22-A108C, section 4.2.1 [1] addresses HTRB testing of power devices and defines the acceptable test condition as one where the ambient temperature keeps the junction temperatures of the DUTs at or above 125 °C. A108C also declares that the  $T_J$  of the DUTs should not exceed the  $T_{JMAX}$  specified in the manufacturer's data sheet (typically 150 °C, for Silicon devices).

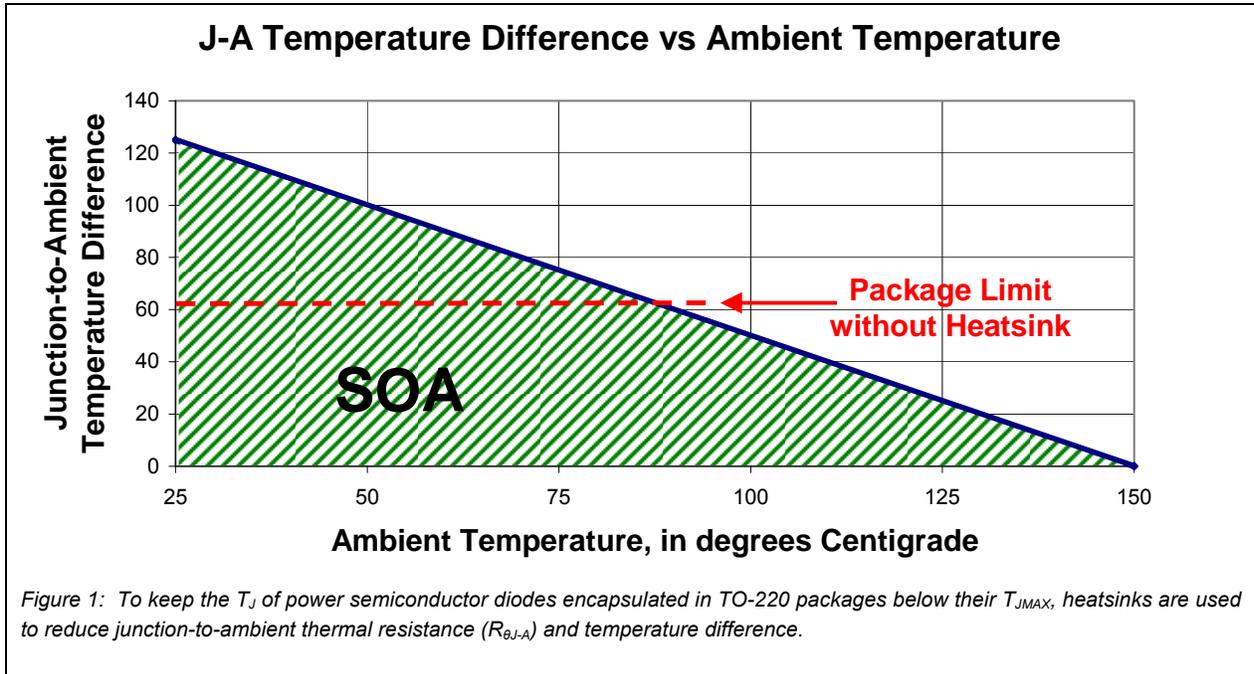
The closer the  $T_A$  of a power semiconductor is to the  $T_{JMAX}$  of the device, the more difficult it becomes to effectively remove heat from the die, and less internally dissipated heat is required to maintain an elevated  $T_J$ . That is why reverse bias (leakage) current ( $I_R$ ) is used to accelerate the aging of power diodes. The small amount of internally dissipated heat that results when  $I_R$  flows at a high reverse voltage can very effectively keep the  $T_J$  of the device close to its maximum rated value when the  $T_A$  is held at or slightly above 125 °C. Reliability Engineering is typically responsible for ensuring that the  $T_J$  of the DUTs stay within the proscribed 125 to 150 °C window. Any combination of heatsinks and  $T_A$  set points that result in device case temperatures between 125 and 140 °C should qualify as an acceptable HTRB test setup.

#### Why Thermal Runaway during HTRB Testing is Probable and Problematic

The  $I_R$  of power diodes has a positive temperature coefficient, and therefore, an increase in  $T_J$  causes  $I_R$  to increase, which

further increases the  $T_J$ . This makes thermal runaway inevitable, if the dissipated heat is not adequately conducted away from the die. When

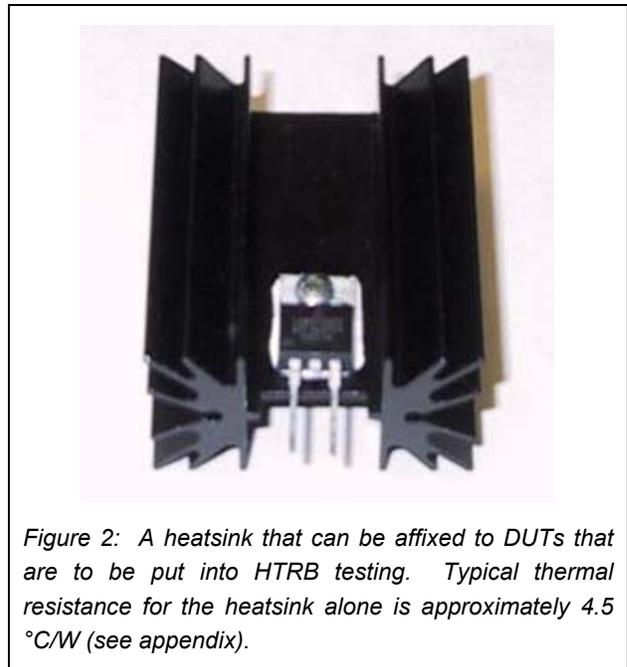
the case-to-ambient thermal resistance ( $R_{\theta C-A}$ ) with a heatsink. The heatsink significantly lowers  $R_{\theta C-A}$ , which helps to maintain tight



the ambient temperature is high ( $\geq 85^\circ\text{C}$ ) and the difference between the  $T_J$  and the  $T_A$  of a device is small, a heatsink is the only practical way to remove enough heat from the device package to prevent the junction from overheating and the device from being driven into thermal runaway. Figure 1 is a graph of the junction-to-ambient temperature difference that must not be exceeded, for power diodes encapsulated in TO-220 packages.

Due to the relatively high junction-to-ambient thermal resistance ( $R_{\theta J-A}$ ) of a typical TO-220 package—especially when the die is isolated from the lead frame ( $\approx 62^\circ\text{C/W}$ )—small fluctuations in device power dissipation can cause large swings in  $T_J$ . As can be seen from the graph, the difference between  $T_J$  and  $T_A$  must be linearly reduced as the ambient temperature increases, and especially as it approaches the maximum junction temperature of the DUTs. This is accomplished by reducing

control of DUT junction temperatures. With the heatsink shown in Figure 2 (specified in the Appendix),  $R_{\theta J-A}$  for the DUT is reduced to about  $7^\circ\text{C/W}$ .



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## Summary

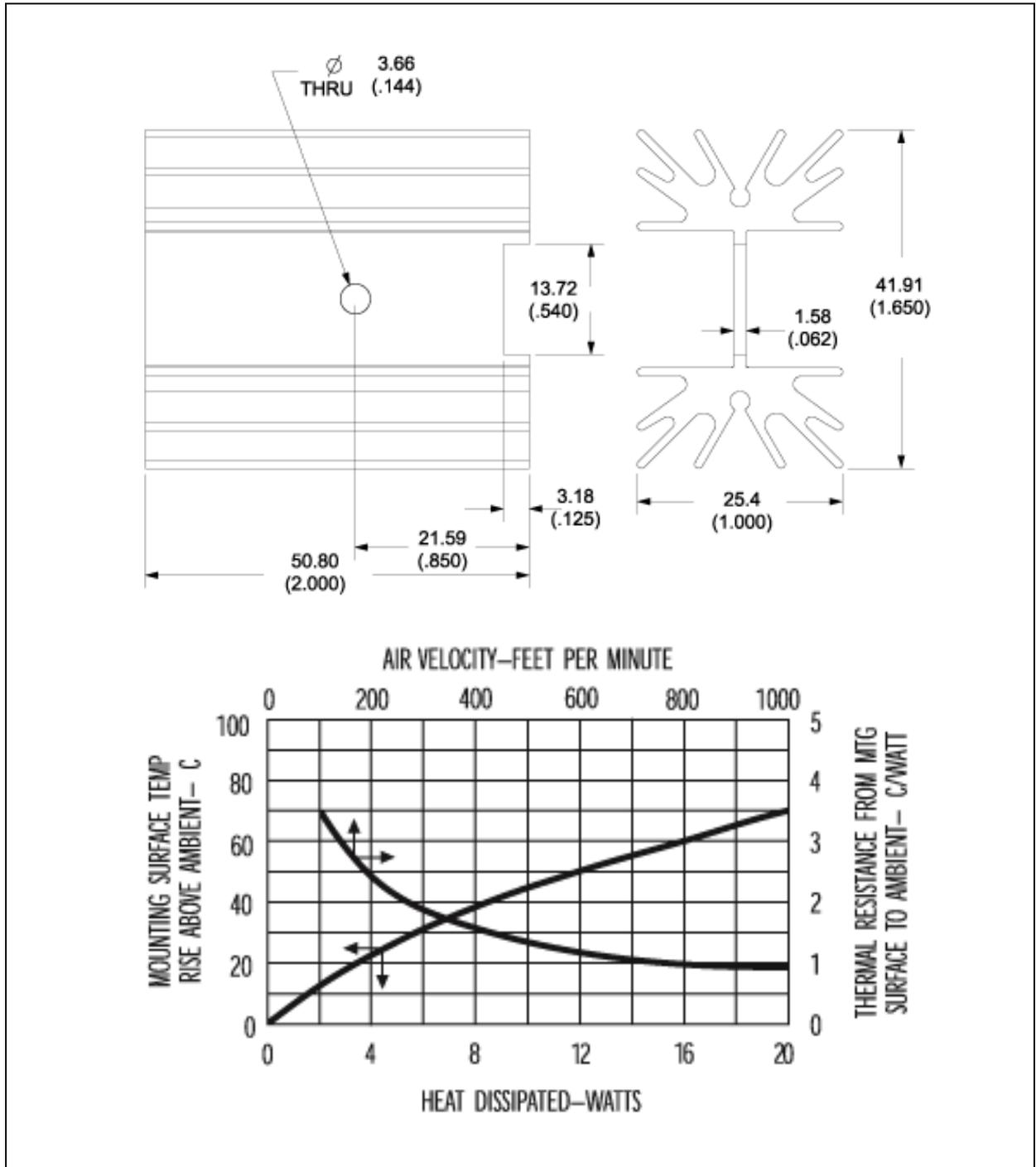
In order to avoid accidentally destroying DUTs during HTRB reliability testing, a heatsink should be affixed to each device to be tested. In a properly designed test, an adequate heatsink eliminates the need to measure DUT case temperatures to ensure that an acceptable  $T_J$  is being maintained throughout the test period, ensures a fairly consistent  $T_J$  for all DUTs in the test environment, and minimizes the likelihood of driving them into thermal runaway. The appendix suggests a potential heatsink vendor and the part number of a heatsink that should be adequate for the HTRB testing of diodes mounted in TO-220 packages.

## References

- 1] JEDEC specification JESD22-A108C  
<http://www.jedec.org/download/search/22a108c.pdf>

**Appendix**

Specifications of a heatsink for power semiconductor diodes in TO-220 packages. Aavid p/n 529902B00000 mechanical drawing and thermal characteristics:



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<b>Revision</b>	<b>Notes</b>	<b>Date</b>
1.4	Released by Qspeed	01/08
1.5	Converted to Power Integrations Document	01/11

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#### **WORLD HEADQUARTERS**

5245 Hellyer Avenue  
San Jose, CA 95138, USA.  
Main: +1-408-414-9200  
Customer Service:  
Phone: +1-408-414-9665  
Fax: +1-408-414-9765  
*e-mail:*  
[usasales@powerint.com](mailto:usasales@powerint.com)

#### **GERMANY**

Rueckertstrasse 3  
D-80336, Munich  
Germany  
Phone: +49-89-5527-3911  
Fax: +49-89-5527-3920  
*e-mail:*  
[eurosales@powerint.com](mailto:eurosales@powerint.com)

#### **JAPAN**

Kosei Dai-3 Building  
2-12-11, Shin-Yokohama,  
Kohoku-ku, Yokohama-shi,  
Kanagawa 222-0033  
Japan  
Phone: +81-45-471-1021  
Fax: +81-45-471-3717  
*e-mail:* [japansales@powerint.com](mailto:japansales@powerint.com)

#### **TAIWAN**

5F, No. 318, Nei Hu Rd., Sec. 1  
Nei Hu District  
Taipei 114, Taiwan R.O.C.  
Phone: +886-2-2659-4570  
Fax: +886-2-2659-4550  
*e-mail:*  
[taiwansales@powerint.com](mailto:taiwansales@powerint.com)

#### **CHINA (SHANGHAI)**

Rm 1601/1610, Tower 1  
Kerry Everbright City  
No. 218 Tianmu Road West  
Shanghai, P.R.C. 200070  
Phone: +86-021-6354-6323  
Fax: +86-021-6354-6325  
*e-mail:*  
[chinasales@powerint.com](mailto:chinasales@powerint.com)

#### **INDIA**

#1, 14<sup>th</sup> Main Road  
Vasanthanagar  
Bangalore-560052  
India  
Phone: +91-80-4113-8020  
Fax: +91-80-4113-8023  
*e-mail:*  
[indiasales@powerint.com](mailto:indiasales@powerint.com)

#### **KOREA**

RM 602, 6FL  
Korea City Air Terminal B/D, 159-6  
Samsung-Dong, Kangnam-Gu,  
Seoul, 135-728  
Korea  
Phone: +82-2-2016-6610  
Fax: +82-2-2016-6630  
*e-mail:* [koreasales@powerint.com](mailto:koreasales@powerint.com)

#### **EUROPE HQ**

1st Floor, St. James's House  
East Street, Farnham  
Surrey GU9 7TJ  
United Kingdom  
Phone: +44 (0) 1252-730-141  
Fax: +44 (0) 1252-727-689  
*e-mail:*  
[eurosales@powerint.com](mailto:eurosales@powerint.com)

#### **CHINA (SHENZHEN)**

Rm A, B & C 4<sup>th</sup> Floor, Block C,  
Electronics Science and  
Technology Building  
2070 Shennan Zhong Road  
Shenzhen, Guangdong,  
P.R.C. 518031  
Phone: +86-755-8379-3243  
Fax: +86-755-8379-5828  
*e-mail:*  
[chinasales@powerint.com](mailto:chinasales@powerint.com)

#### **ITALY**

Via De Amicis 2  
20091 Bresso MI  
Italy  
Phone: +39-028-928-6000  
Fax: +39-028-928-6009  
*e-mail:*  
[eurosales@powerint.com](mailto:eurosales@powerint.com)

#### **SINGAPORE**

51 Newton Road,  
#19-01/05 Goldhill Plaza  
Singapore, 308900  
Phone: +65-6358-2160  
Fax: +65-6358-2015  
*e-mail:*  
[singaporesales@powerint.com](mailto:singaporesales@powerint.com)

#### **APPLICATIONS HOTLINE**

World Wide +1-408-414-9660

#### **APPLICATIONS FAX**

World Wide +1-408-414-9760