Application Guidelines

The following guidelines are meant to optimize the overall system performance when using 2SP0430T gate drivers in various applications.

Power Supply

The gate driver has to be supplied by a fixed voltage of typically 15V at VDC and VCC. It is mandatory that one supply is used for both terminals.

DC-Link Design

The mechanical and electrical design of the DC-link of the target application determines during turn-off events of the driven power semiconductor the over voltages ΔV_{CE} according to equation (1). Here, L_σ describes the overall DC-link stray inductance (i.e. sum stray inductance of DC-capacitors, DC-link bus bar and power module) and di_C/dt the collector current change.

$$\Delta V = L_\sigma \cdot \frac{di_C}{dt} \qquad (1)$$

If the over voltage ΔV_{CE} plus the applied DC-link voltage V_{DC} exceed the breakdown voltage of the driven power module (refer to the reverse bias safe operating area RBSOA), the power module may be damaged. In case of excessive turn-off over voltages, one or more of the following application parameters have to be decreased:

- DC-link voltage V_{DC}
- Stray inductance L_σ
- Collector current i_C

Therefore, during the installation and testing of the target application the actual over voltages ΔV_{CE} at different conditions have to be measured.

Note: 2SP0430T gate driver will actively limit any over voltage during turn-off events under normal and over current conditions to safe levels using the implemented Dynamic Advanced Active Clamping scheme. However, it is not recommened that the clamping feature is active during normal switching conditions. It may lead to an over load of the implemented clamping devices. Furthermore, it might lead to an under voltage lock-out (UVLO) condition on the secondary-side power supply of the gate driver.

Paralleling of Power Modules

Paralleling of PrimePACK™ 3+ power modules with 2SP0430T gate driver is in principle possible if the following basic rules are obeyed to ensure minimum load current imbalances and general proper system operation.

The load current sharing between paralleled power modules depends on several factors:

- Deviation of the power modules parameters like IGBT saturation voltage V_{CEsat}, diode forward voltage V_F, rise and fall times t_r and t_f, turn-on and turn-off delay times $t_{d(on)}$ and $t_{d(off)}$. They are influencing the current sharing in the conducting (static) and switching (dynamic) phase.
- Deviation in the cooling of the power modules. The before mentioned parameters are mostly temperature dependent. Inhomogeneous cooling of paralleled power modules influences therefore the static and dynamic current sharing.
- Deviation of the gate loop impedance. It leads to static and dynamic current imbalances.
- Deviation of the apparent DC-link stray inductance and resistance per paralleled power module. It leads to static and dynamic current imbalances.

Power module parameter deviations can be addressed by screening of power modules as offered by some manufacturers. The deviation in cooling can be compensated to a fair degree by the inherent positive temperature coefficient of the power modules. In case one power module takes over more current than the other power modules, it will heat-up more than the others. As a result the saturation voltage is increased, which leads to a reduction of the current in the power module. The system is self-regulated to a certain extent.

Deviations of the gate loop impedances are minimized by design, process and assembly control of 2SP0430T. Part of the gate loop impedance is also the terminal screw connection of the gate driver towards the power module. Here the recommended (i.e. maximum) mounting torque must be obeyed to minimize its influence.

Deviation of the apparent DC-link stray inductance and resistance between paralleled power modules refers to the mechanical arrangement of the power modules and DC-link.

Depending on the actual application conditions is might be required to add inductors in the AC output phases of each paralleled power module to symmetrize load current imbalance.

Note: Do not operate paralleled power modules without connected gate driver. This may lead to half-bridge short-circuits within the power modules and will eventually destroy them.

Multilevel Topologies

2SP0430T gate driver are designed for 2-level and 3-level topologies. For 3-level topologies:

- Cascaded multilevel topologies on system level like for instance Modular Multilevel Converter (MMC) operating with 2-level topologies within one cell are supported without any restriction (implying that required isolation requirements are fulfilled).
- For 3-level systems the turn-off sequence has to be obeyed by the system controller to avoid overvoltage events, which might lead to an RBSOA (reverse biased safe operating area) violation of the power module. However, 2SP0430T gate driver have Power Integrations' Dynamic Advanced Active Clamping (DA²C) implemented, which enables the gate driver to protect the power modules against over voltage conditions arising by wrong turn-off sequences. The suitability of DA²C has to be checked within the target application.

  Note: During short-circuit and/or under voltage events, the gate driver will immediately switch-off the respective power module. No control on the turn-off

sequence is given. Therefore, the suitability of 2SP0430T has to be checked on application level for this kind of topology.

Conformal Coating

The electronic components of the 2SP0430T gate driver are protected with a layer of acrylic conformal coating using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments. Nevertheless, standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the 2SP0430T gate driver.

Product Dimensions

2SP0430T2A0C all versions

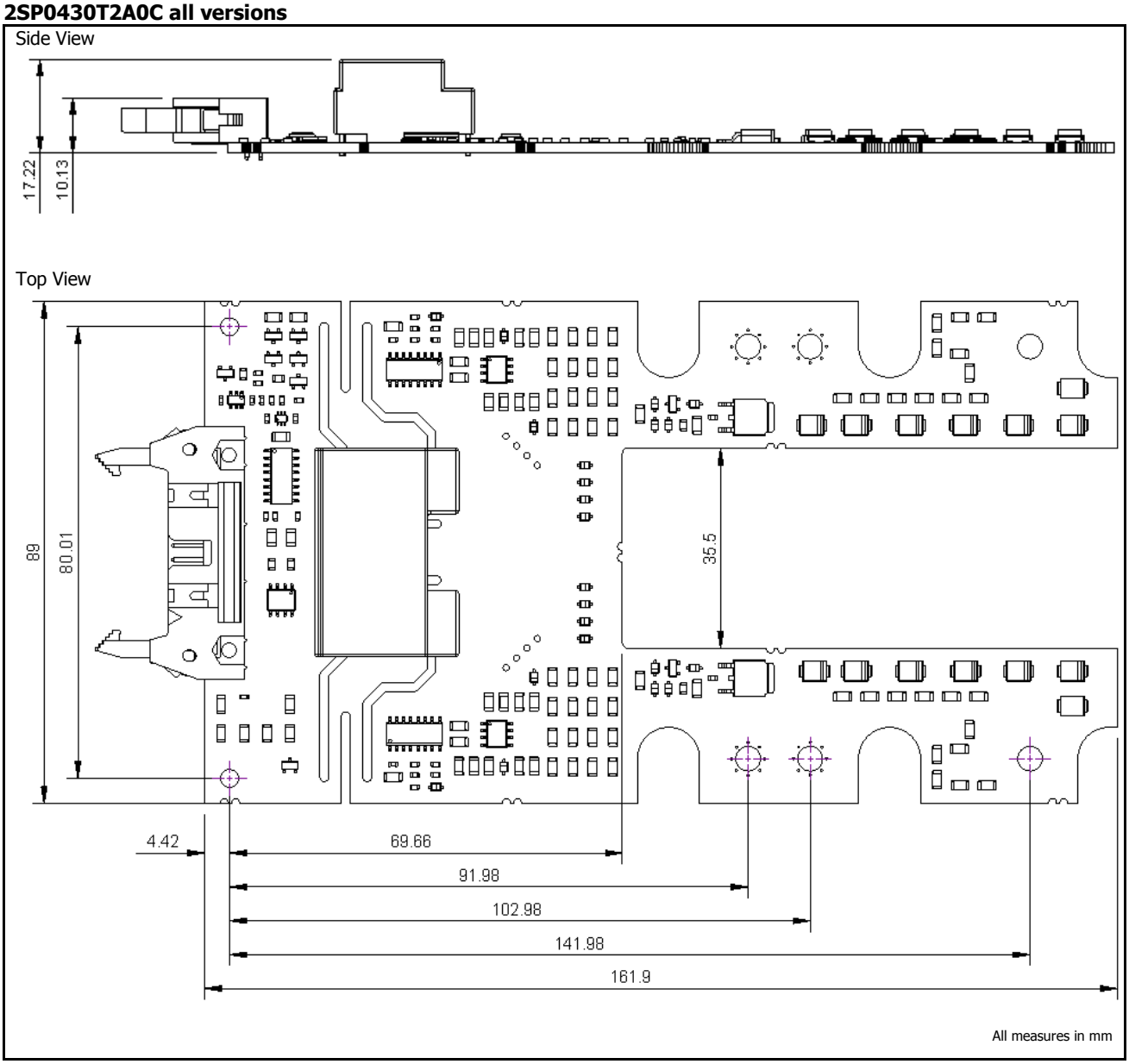


Figure 9. Dimensions.

2SP0430T2B0C all versions

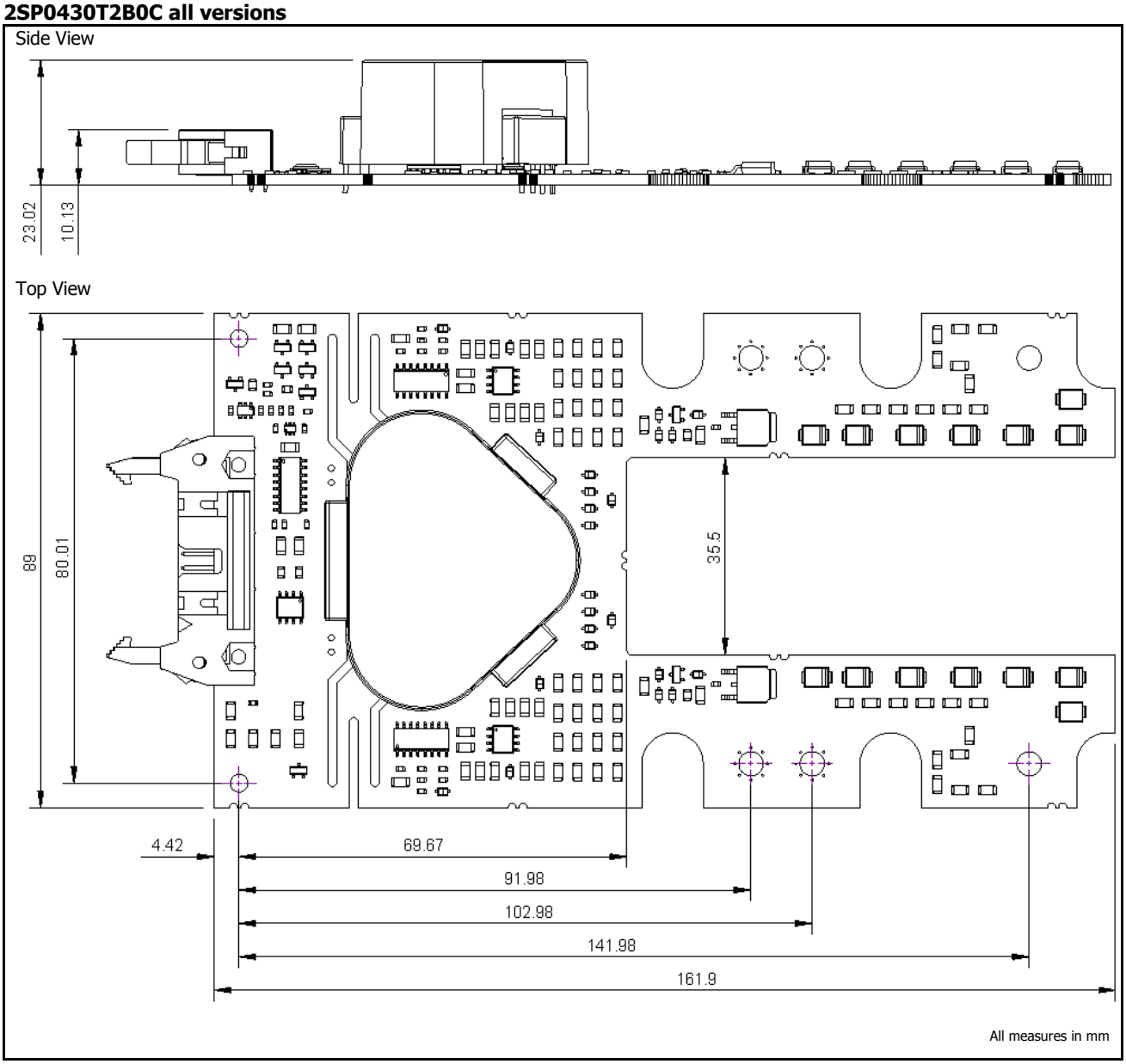


Figure 10. Dimensions.

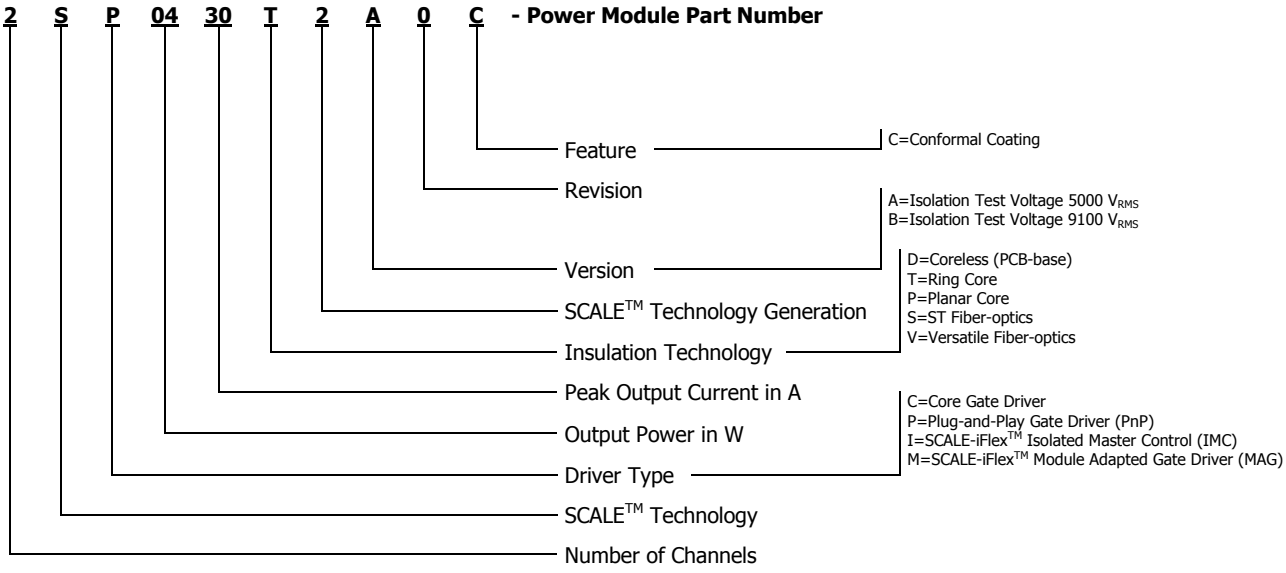
Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

On the basis of Annexes II and III of European Directive 2011/65/EC of 008 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), we hereby state that the products described in this datasheet do not contain lead (Pb), mercury (Hg), hexavalent chromium (Cr VI), cadmium (Cd), polibrometo of bipenyl (PBB) or polibrometo diphenyl ether (PBDE) in concentrations exceeding the restrictions set forth in Annex II of 2011/65/EC with due consideration of the applicable exemptions as listed in Annex III of 2011/65/EC.

Part Ordering Information



Revision	Notes	Date
A	Target Datasheet, initial version	10/18

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