1SP0635V2A0D
SCALE-2 Family

Gate Driver for IGBT Modules up to 3300 V
Versatile Fiber-Optic Interface

PRELIMINARY

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for power modules up to 3300 V blocking voltage
- Single-channel gate driver
- 35 A peak output gate current
- 3 W output power at maximum operating temperature
- Supports parallel connection of up to four power modules
- -40 °C to +85 °C operating ambient temperature range
- Optical status indicator

Protection / Safety Features

- Short-circuit protection
- Dynamic Advanced Active Clamping (DA^2C)
- Undervoltage lock-out (UVLO) protection
- NTC temperature sensing
- DC-link voltage measurement at 75 kHz
- Gate monitoring
- Double-sided conformally coated (ELPEGUARD SL 1307 FLZ/4 from Lackwerke Peters)
- RoHS compliant

Applications

- Railway inverter
- Industrial drives
- Other industrial applications

Description

The Plug-and-Play 1SP0635V2A0D gate driver is a compact single-channel intelligent gate driver designed to support a range of IGBT modules. It features a versatile fiber-optic interface.

The 1SP0635V2A0D is designed to work with an isolated DC-DC converter ISO6125R-33, which needs to be purchased separately as it is not integrated into the driver.

Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range to support the IGBT off-state for up to 60 seconds. This is ideal for railway and regenerating applications.

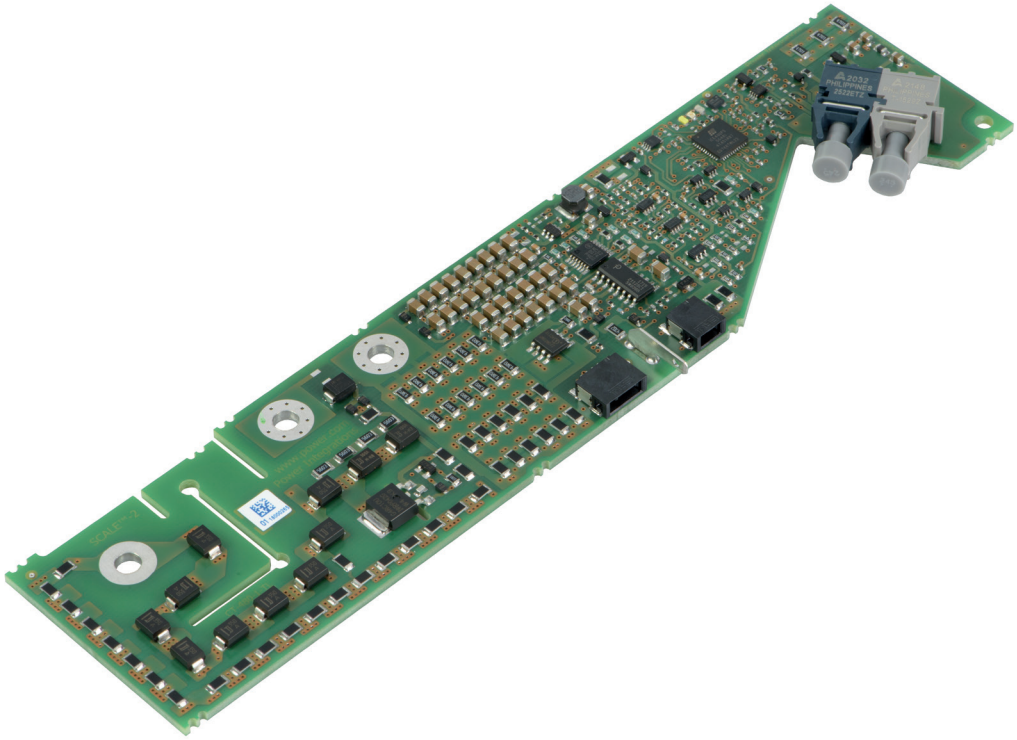

Figure 1. Product Photo of 1SP0635V2A0D.

Pin Functional Description

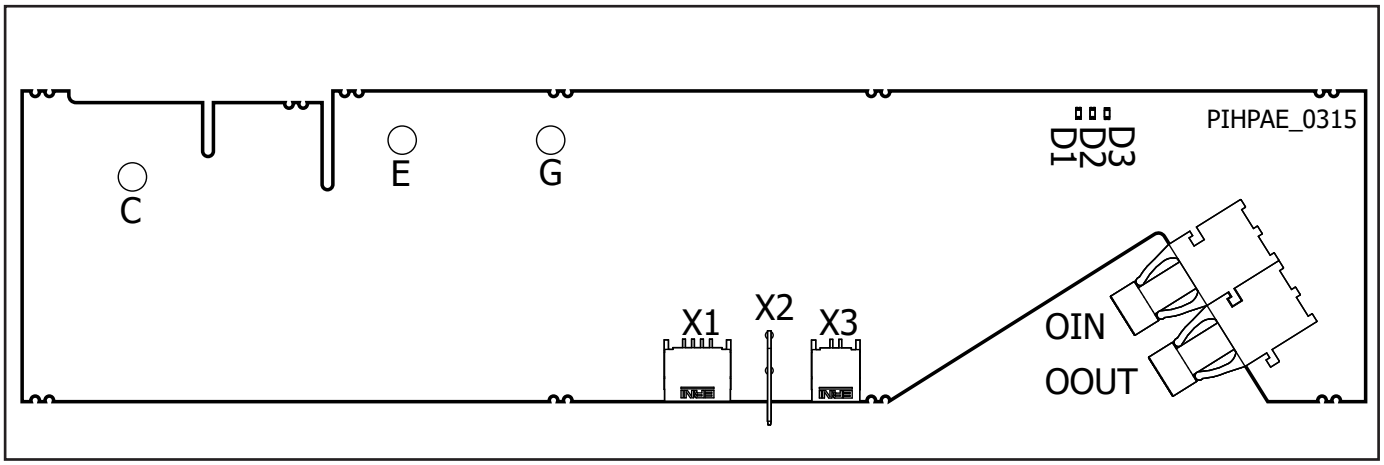

Figure 2. 1SP0635V2A0D Interfaces.

Connector X1

ERNI interface to connect main driver external DC-DC converter.
Part number: ERNI 504255-E, 4 pin, right angle.

COM (Pins 1, 4)
This pins are the connection to secondary-side ground potential.

VISO (Pins 2, 3)
This pins are the connection to secondary-side supply voltage.

Connector X2

Quick FIT terminal to DC-link measuring input
Part number: Ettinger 019.25.131.

Connector X3

ERNI interface for NTC measurement.
Part number: ERNI 504235-E, 2 pin, right angle.

NTC (Pin 1)
This pin is the first NTC terminal.

COM (Pin 2)
This pin is the second NTC terminal.

Connection to Semiconductor

Terminal G
Gate contact of IGBT.

Terminal E
Auxiliary emitter contact of IGBT.

Terminal C
Auxiliary collector contact of IGBT.

Fiber-Optic Interface

Main driver to external controller (fiber optic receiver and transmitter).

OIN (Receiver)
This fiber optic receiver is the command input.
Part number: Broadcom HFBR-2522ETZ

OOUT (Transmitter)
This fiber optic transmitter is the status output.
Part number: Broadcom AFBR-1529Z

Optical Indicators

For easy verification of the operation of the gate driver.

D1
White LED for monitoring the power supply. The indicator is turned on when the driver is supplied with voltage.

D2
Green LED for monitoring the status of optic input. The indicator is turned on when the driver receives a turn-on command.

D3
Red LED for monitoring the fault status.
The LED is turned ON and keeps to light ON upon a Fault detected by the driver (i.e. VCE-short-circuit detection (SC_VCE), undervoltage monitoring high (UVLO_POS) or low (UVLO_NEG).

The LED is turned OFF at the next turn-on command under the condition that all Fault conditions are cleared.

Functional Description

The basic topology of the 1SP0635V2A0D driver is shown in Figure 3. This driver is a single-channel intelligent gate driver. The driver is equipped with the following features:

- Dynamic V_{CE} monitoring (short-circuit protection)
- Dynamic Advanced Active Clamping DA²C (overvoltage protection at turn-off)
- Gate monitoring
- NTC temperature sensing
- DC-link voltage measurement at 75 kHz
- Gate clamping to the positive rail
- Power supply monitoring

The driver 1SP0635V2A0D is not equipped with a DC-DC converter. The signals are isolated with versatile fiber optics links. The power supply (isolated DC-DC converter ISO6125R-33) has not been integrated in the driver. It is a separate unit. The signals are isolated with versatile fiber optics links.

Plug-and-play capability means that the drivers are ready to operate immediately after mounting. The user does not need to invest any effort in designing or adjusting the driver to match a specific application.

Description of X1, X2 and X3
The main driver is equipped with a 4-pin interface connector X1. It is recommended to connect both COM and VISO pins.

The X2 connector is the input for measuring the DC-link voltage through an external resistor connected to the DC-link. It is referred to the emitter voltage. This feature is only available for low-side drivers (in two-level applications). For the HS driver, the signal must be left unconnected. The X3 connector provides an interface from the External NTC thermistor to the driver measuring input.

Screw Terminals
The main driver is mounted on top of the power module and fixed by screws.

Connection Cables for X1
For recommended cables, please refer to data sheets RLC-PSI-641-050-0.

Power Supplies and Electrical Isolation
The power supply shall be an isolated DC/DC converter such as Power Integration ISO6125R-33.

Fiber Optic Receiver OIN
The input signal OIN is received by a fiber optic receiver. OIN has a positive logic (light on implies turn-on) and is edge-triggered. The gate driver signal is transferred from the OIN receiver to the gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for turn-off commands as illustrated in Figure 5. Filtering is implemented to ensure that any positive or negative command pulses below $t_{FILTER(ON\_PULSE)}$ and respectively $t_{FILTER(OFF\_PULSE)}$ are not transmitted to the Gate.

Fiber Optic Transmitter OOUT
The status output signal OOUT is transmitted by a fiber optic transmitter to external control. OOUT provides a data stream according to a UART protocol described in the section "Data Protocol".

Short-Circuit Detection
Figure 6 shows the response of the driver in the event of a short-circuit fault. Upon the short circuit detection, a delay of $t_{P(HL),FAULT}$ is applied before the IGBT is turned off. The status bit SC_VCE of the status register is set to binary '1' and it is transferred to the status output OOUT feedback terminal with a delay of response time $t_{SC\_VCE(LH)}$.

The IGBT can be turned on again by applying a positive edge to the fiber-optic input after the fault status has disappeared and a successive period of t_{BLK} has elapsed. The fault status LED is also enabled upon fault detection.

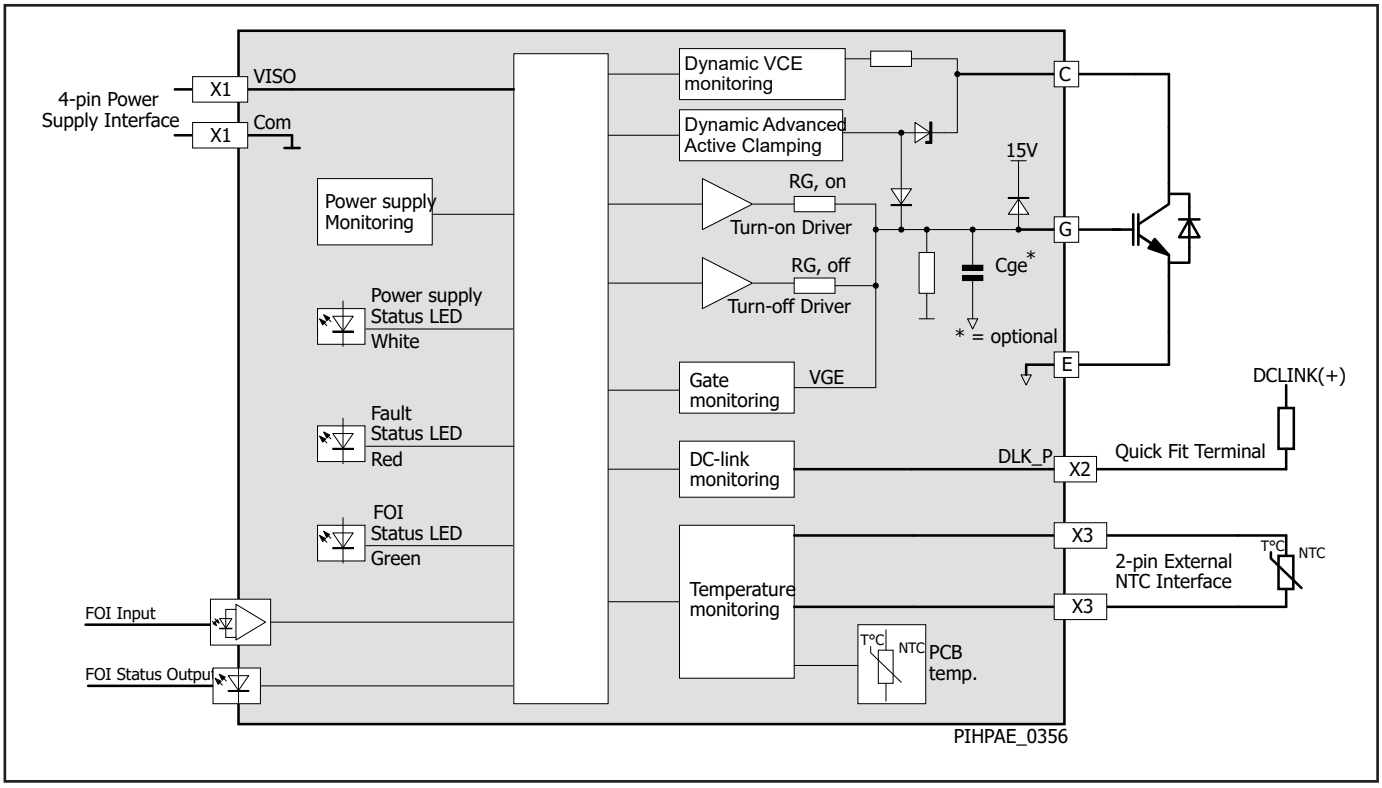

Figure 3. Functional Block Diagram.

Undervoltage Detection
In the event of an undervoltage fault being detected on either the VISO-VEE or VEE-COM supply voltages, the fault status remains active and the driver is locked for as long as the undervoltage remains. In case the VISO-VEE or the VEE-COM goes in undervoltage, the status bit UVLO_POS respectively UVLO_NEG of the status register is set to binary '1' after a delay time response of $t_{UVLO(LH)}$.

The status bits are cleared after the fault status has disappeared and the IGBT can be turned on again by applying a positive edge to the fiber-optic input after a successive blocking time t_{BLK} is elapsed. The fault status LED is also enabled upon fault detection.

Gate Monitoring Warning Detection
When the Gate-Emitter voltage goes below the threshold $V_{GE\_mon(ON)}$ or $V_{GE\_mon(OFF)}$, after a delay time $t_{GE\_mon(FILTER)}$ following the VGE switching, the warning status bit VGE_STAT_HI respectively VGE_STAT_HI of the status register is set to binary '1' and transferred to the fiber optic transmitter with a delay of the response time $t_{GMON(LH)}$. Figure 7 illustrates the Gate monitoring timing.

DC-Link Voltage Monitoring
The driver comprises an input to measure the DC-link voltage referred to the Emitter voltage. This feature is only available for the low-side driver of a 2 Level System Converter. The X2 connector has to be connected to a high voltage-rated external resistance to the DC-Link source.

The DC-link measured value is transferred to the optical transmitter OOUT through the DLK[11.0] data bit fields at a rate of S_{DLK}. The response time to reach 95% of the measured value is given by t_{DLK}. Both measuring range V_{DLK_RANGE} and measuring output resolution V_{DLK_RES} are specified according to a specific value of external resistance (refer to characteristics section).

Please note the following:
- Precautions shall be considered when connecting the external resistance to the X2 input to minimize the connecting loop and any undesired coupling that may affect the measurement accuracy.
- For the high-side driver, the X2 input must be either left unconnected or connected to the driver emitter, and the data bit fields DLK[11.0] returned by the optical transmitted ignored.

PCB NTC Temperature Monitoring
The driver is assembled with a thermistor measuring the driver's PCB temperature. The measured temperature value is transferred to the optical transmitter OOUT through the DAT[11.0] data bit fields at a rate of S_{NTC1} (for the data format, refer to the sub-section "NTC Temperature" of the "Protocol section)". The response time to reach 95% of the measured value is t_{NTC1}. The measuring range is defined by the parameter V_{NTC1_RANGE} and measuring output resolution is defined by the parameter V_{NTC1_RES}.

External NTC Temperature Monitoring
The driver comprises a connector (X3) available for connecting an external NTC thermistor for measuring for instance heatsink temperature. The measured external temperature value is transferred to the optical transmitter OOUT through the DAT[11.0] data bit field at a rate of S_{NTC2} (for the data format, refer to sub-section "NTC Temperature" of the "Protocol section)". The response time to reach 95% of the measured value is given by t_{NTC2}. The measuring range is defined by the parameter V_{NTC2_RANGE} and measuring output resolution is defined by the parameter V_{NTC2_RES}.
The NTC shall be electrically isolated according to the system isolation requirements. Both external NTC terminals shall not be connected to any external potential such as the emitter or the collector.

In case the external NTC is unused, the connector X3 shall be left unconnected. A Missing or unconnected NTC thermistor will generate a constant negative full-scale value in the DAT[11..0] data bit field.

Dynamic Advanced Active Clamping (DA²C)
Active clamping acts to partially turn on the IGBT if the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate. The gate driver in 1SP0635V2A0D contains Power Integrations' Dynamic Advanced Active Clamping (DA²C) that operates as follows:

When active clamping is activated, the turn-off MOSFET for the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature is called as Advanced Active Clamping (AAC). The principle of AAC is illustrated in Figure 4.

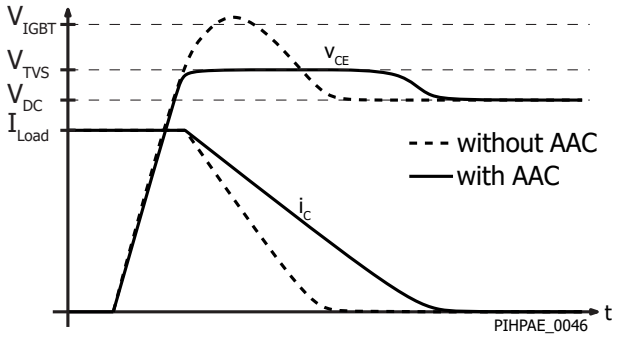

Figure 4. Advanced Active Clamping.

Additional TVS diodes are added in series with the TVS diodes required to withstand the maximum DC-link voltage during switching. These TVS diodes are short-circuited during the IGBT on-state for about 15 to 20 µs after the turn-off command is received to ensure efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). Note that the time that the voltage can be applied above the value for switching operation should be limited to short periods (< 60s).

Blocking Time
After a short circuit detection or an undervoltage detection, the gate signal is turned off for a period of t_{BLK} and the status bit G_BLOCKING of the status register is maintained to binary '1' during the whole period and goes to binary '0' afterward.

Self-Test
A driver internal self-test is implemented to check driver functionalities. The warning status bit "ST" of the status register is set to binary '1' in case the self-test detects parameters outside the expected range. Otherwise, the "ST" status bit is set to binary '0'.

Dynamic Behavior of IGBT
Due to the different behavior of the included IGBT and diode chips, the dynamic behavior of the IGBT module depends on their type and manufacturer. Module construction and the distribution of the internal gate resistances and inductances also play a role in determining dynamic response. Note that different module types from the same manufacturer may also require a specific gate-driver adaptation.
Power Integrations, therefore, supplies specific versions of SCALE™-2 plug-and-play drivers adapted to each type of IGBT module. These drivers must not be used with IGBT modules other than those for which they were specified.

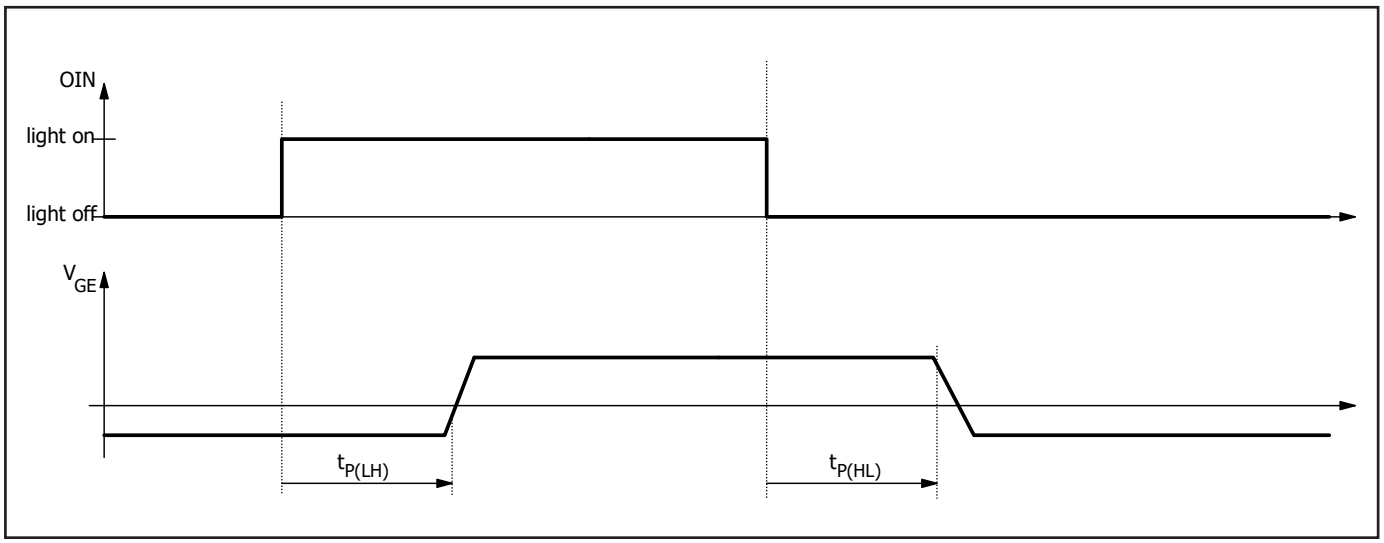

Figure 5. Driver Gate Signal in Normal Operation Mode.

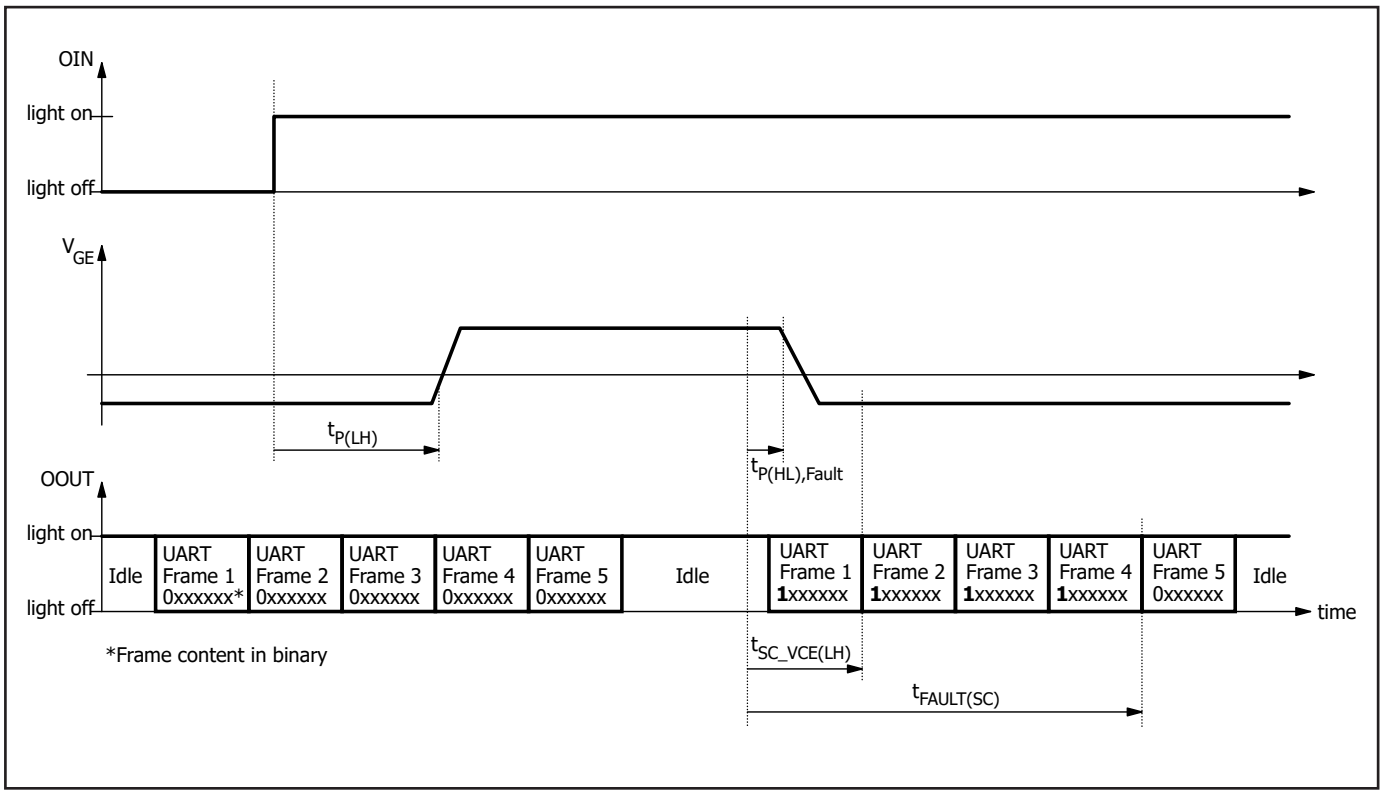

Figure 6. Fiber Optic Feedback from the Driver in Short-Circuit Fault Mode.

Turn-On of the IGBT / Commutation of Diode Current

When a driver input goes high (light on), the gate driver turns on the corresponding IGBT. The driver includes the gate resistors, matched to the appropriate IGBT module.

The driver is optimized to achieve minimum switching losses when paired with relatively low inductances within the power stack. It is therefore recommended to check the commutation behavior of the system assembly.

Turn-Off of the IGBT

The IGBT is turned off when the corresponding input turns low (light off). The gate resistance is already optimized and should not be altered.

Fast turn-off of the IGBT may cause overvoltage, which increases with DC-link voltage or load current. The turn-off overvoltage is approximately:

$$V_{TR} = L_S \times di_C/dt$$

where V_{TR} is the turn-off overvoltage, i_C is the collector current and L_S is the stray inductance.

Limiting overvoltage at turn-off is essential for high-power or high-voltage IGBTs. To ensure this, SCALE-2 plug-and-play drivers provide a Dynamic Advanced Active Clamping function DA^{2}C.

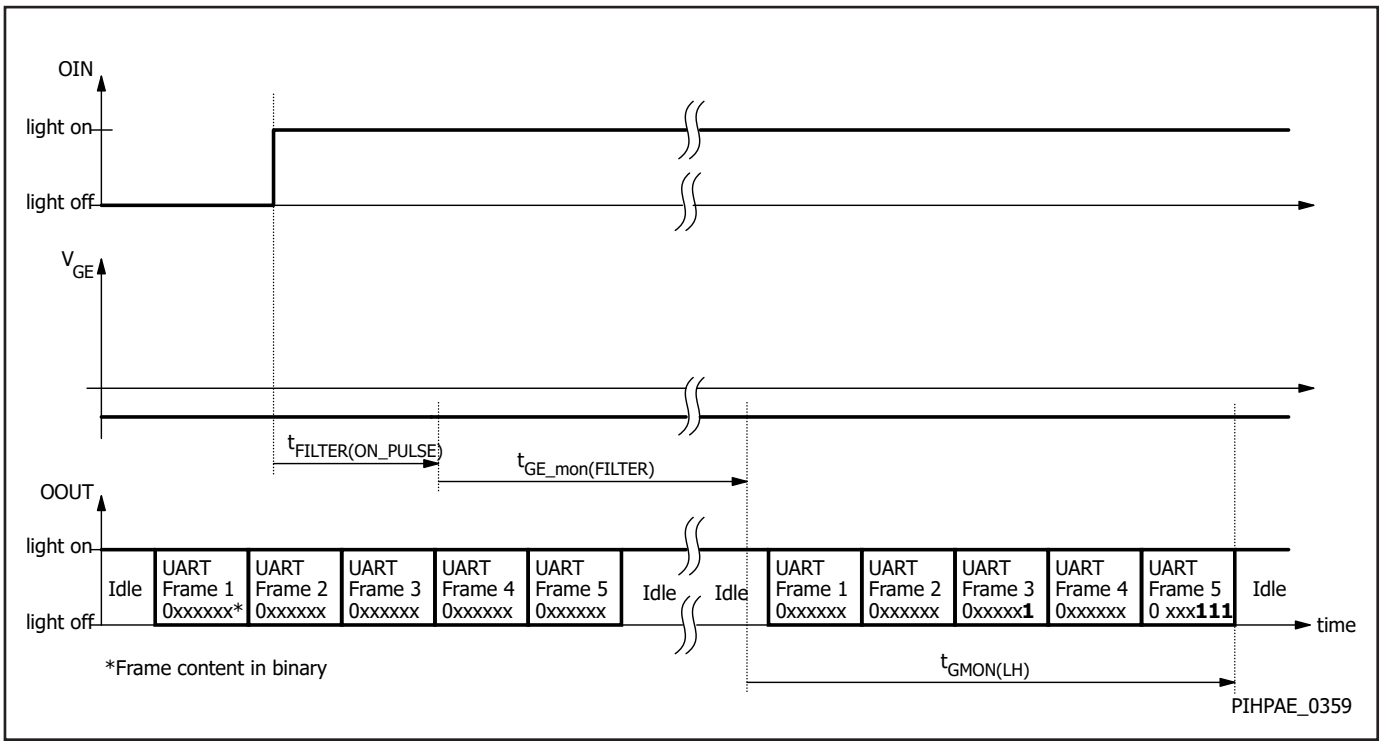

Figure 7. Fiber Optic Feedback of the Driver in Normal Operation Mode.

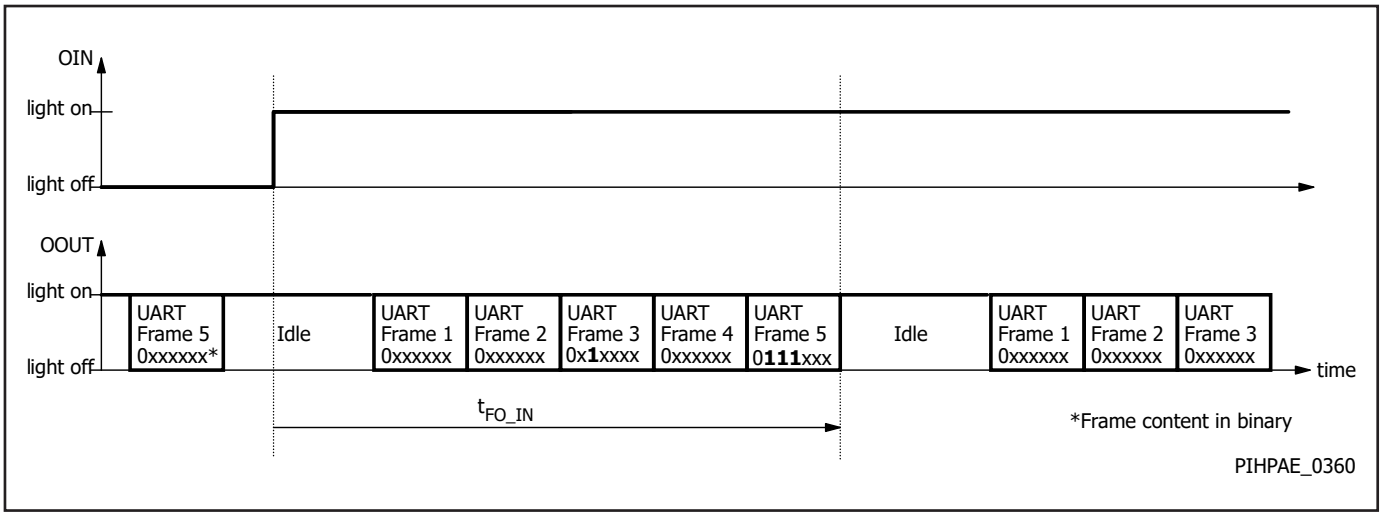

Figure 8. Fiber Optic Status Register Bit in Normal Operation Mode.

Data Protocol

The fiber optical output provides a signal according to Power Integrations' proprietary protocol. It is based on the UART protocol.

UART Frame

Figure 9 shows the timing of the UART frame and the polarity of the optical transmitter. Each UART frame of the protocol comprises 1 start bit, 6 data bits (DATA BIT 0 … 5), 1 VCE_SC (short-circuit) data bit, 1 parity bit (even), and 1 stop bit. The length of an UART frame is defined by t_{UART} and the bit rate by BR_{UART}. Both start bit and stop bit have a length of 1 bit. The least significant bit (LSB) of the data is sent first. This means that after sending the start bit, the DATA BIT 0 is sent and before sending the STOP BIT, the parity bit is sent.

The parity bit is defined as the even parity calculation of the following bit fields: DATA BIT 0 to DATA BIT 5 and the SC_VCE bit. The status bit SC_VCE bit indicates a short-circuit detection. The polarity of the bit related to the optical transmitter is defined as follows:

- the start bit is a transition from light ON to light OFF
- the stop bit is a transition from light OFF to light ON
- a logical low data (including VCE_SC) is defined as a light ON
- a logical high data (including VCE_SC) is defined as a light OFF
- the idle state is defined as a light ON

Data Packet

The protocol is defined in such a way a data packet of five consecutive UART frames (as in Figure 9) is sent periodically at a rate of f_{DATA} (refer to Figure 10). The data packet length is defined as t_{PACKET} and between two packets there is an idle time of t_{IDLE} where no data are transmitted.

Short Circuit Detection and Idle Time

As the protocol is asynchronous to any VCE short-circuit detection, depending on the time of the VCE shorct circuit detection, the idle time might be reduced to inform the host controller about the event. Both Figure 11 and Figure 12 show examples where the idle time t_{IDLE} and data frequency f_{DATA} are impacted.

Data Packet Format

Each data packet meets the format illustrated below:

	MSB					LSB
	SC_VCE bit	Data bit5	Data bit4	Data bit3	Data bit2	Data bit1	Data bit0
UART FRAME1	SC_VCE	DLK[5]	DLK[4]	DLK[3]	DLK[2]	DLK[1]	DLK[0]
UART FRAME2	SC_VCE	DLK[11]	DLK[10]	DLK[9]	DLK[8]	DLK[7]	DLK[6]
UART FRAME3	SC_VCE	DAT[5]	DAT[4]	DAT[3]	DAT[2]	DAT[1]	DAT[0]
UART FRAME4	SC_VCE	DAT[11]	DAT[10]	DAT[9]	DAT[8]	DAT[7]	DAT[6]
UART FRAME5	SC_VCE	ADR[2]	ADR[1]	ADR[0]	CRC[2]	CRC[1]	CRC[0]

PIHPAE_0365

Data Bit Fields Description

SC-VCE

This is a status bit that indicates when a VCE short-circuit is detected. It is set to binary '1' when a VCE short-circuit is detected or else to binary '0'. When a VCE short-circuit is detected, the SC-VCE bit is updated at the host side with a delay of $t_{SC\_VCE(LH)}$.

DLK[11]..DLK[0]

These 12 bits are used for the DC-link measurement value. The format is an unsigned integer, and the resolution is 1V. The DC-link data is refreshed with a S_{DLK} rate.
Example of data DLK[11..0] value and its corresponding DC-link value: 1001 1100 0100 = 2500V

ADR[2]..ADR[0]

These three bits are address bits. They are used to define the content of the data value returned in *DAT[11..0]*.

ADR[2]	ADR[1]	ADR[0]	DAT[11..0]
1	1	1	Status register
1	0	1	External NTC temperature
1	1	0	PCB NTC temperature
Other combination			Reserved for other use

DAT[11]..DAT[0]

The data of 12 data bits is defined by the address ADR[2..0]. It is refreshed with a rate defined by f_{DATA}. In normal operation (no VCE short-circuit detected), the Data Register is updated as the following sequence:

- The Status Register is copied and transferred to DAT[11..0] at the rate f_{DATA} during 31 consecutive cycles.
- One value of the PCB NTC temperature is transferred to DAT[11..0] during one cycle.
- The Status Register is copied and transferred to DAT[11..0] at the rate f_{DATA} during 31 consecutive cycles.
- One value of the External NTC temperature is transferred to DAT[11..0] during one cycle.

Both PCB NTC temperature and External NTC temperature are refreshed with S_{NTC1} and S_{NTC2} rates respectively. In the case of a VCE short-circuit detection, the above sequence is restarted.

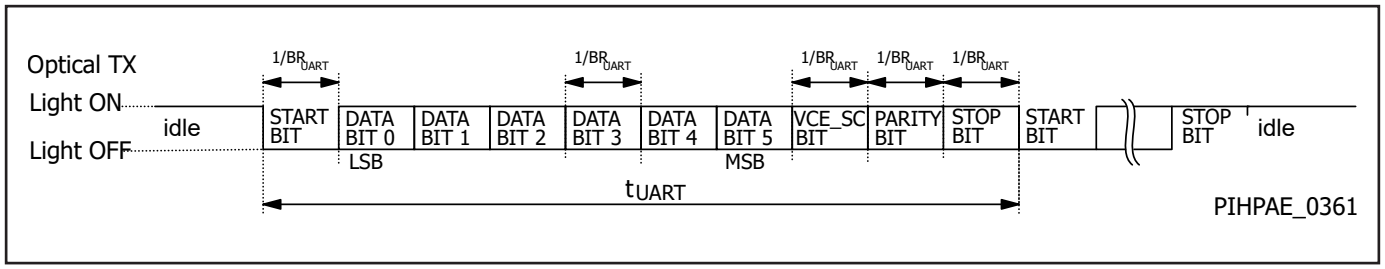

Figure 9. UART Frame Timing and Optical Transmitter Polarity.

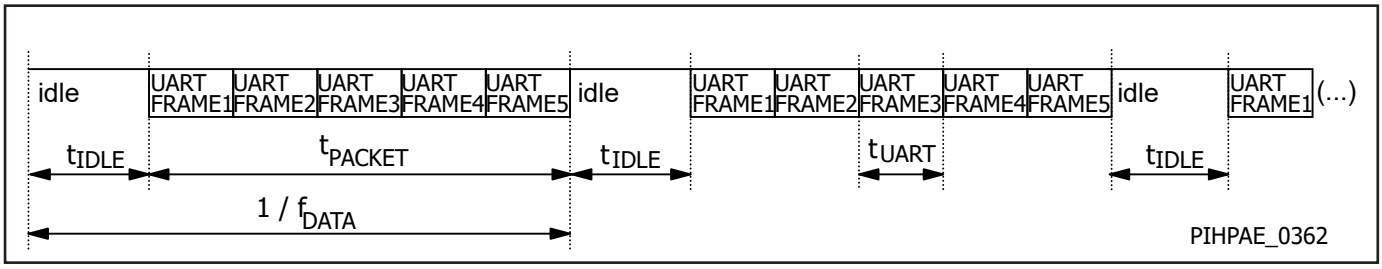

Figure 10. Data Packet Timing in Normal Operating Condition.

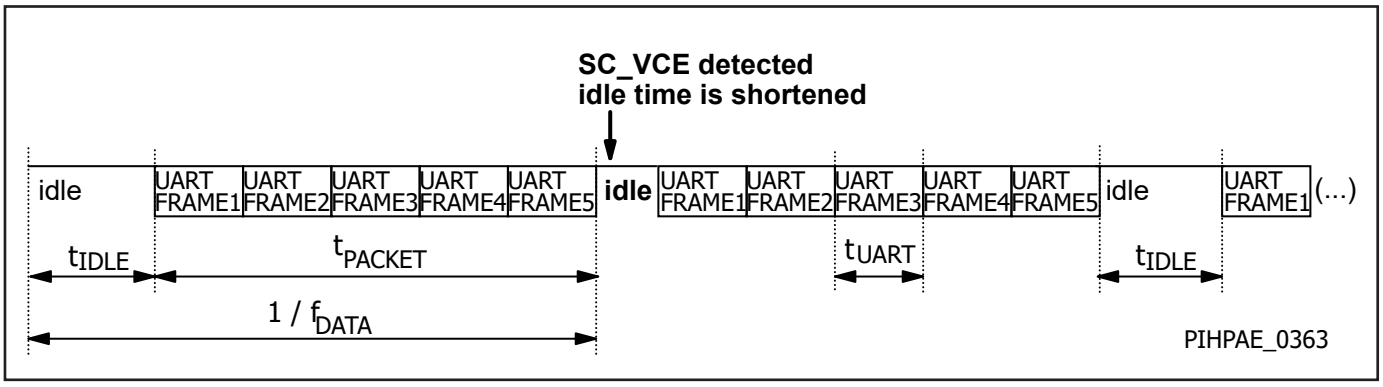

Figure 11. Data Packet Timing for a Short Circuit Condition Detected During Idle.

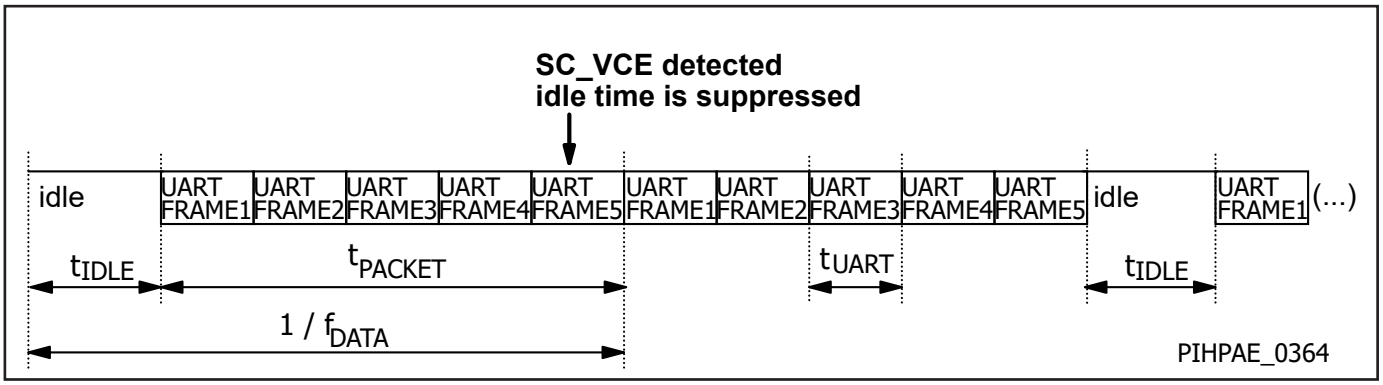

Figure 12. Data Packet Timing for a Short Circuit Condition Detected at the End of Data Packet.

Status Register
The status register contains 12 bits, to indicate the driver status.

Status Register	Bit Name	Description
SR[11] (MSB)		Unused
SR[10]		Unused
SR[9]		Unused
SR[8]		Unused
SR[7]	G_BLOCKING	Gate blocking status bit. Set to binary 1 when the gate output is blocked or else to binary '0'
SR[6]	SUM_FAILURE	Sum failure status bit. Set to binary '1' when at least one Failure bit is set and set to binary '0' when all failure bits are cleared. The sum includes the status of VCE_SC fault and both unvervoltage monitoring faults VGE_STAT_HI and VGE_ STAT_LO
SR[5]	ST	Driver self-test warning status bit. Set to binary '1' when an internal Failure is detected or else to binary '0'
SR[4]	IN_STAT	Optical fiber receiver status bit. Set to binary '1' when a turn-on command is sent or else set to binary '0'
SR[3]	UVLO_POS	Undervoltage fault status bit of VISO-VEE. Set to binary '1' when a failure is detected or else to binary '0'
SR[2]	UVLO_NEG	Undervoltage fault status bit of VEE-COM. Set to binary '1' when a failure is detected or else to binary '0'
SR[1]	VGE_STAT_HI	Gate monitoring of Gate-Emitter during ON-state, warning status bit. Set to binary '1' when a warning is detected or else to binary '0'
SR[0] (LSB)	VGE_STAT_LO	Gate monitoring of Gate-Emitter during OFF-state, warning status bit. Set to binary '1' when a warning is detected or else to binary '0'

NTC Temperature
Both external NTC temperature and PCB NTC temperature are provided to the host through the data DAT[11..0] when the address ADR[2..0] is selected accordingly. The NTC measurement is provided through 12 bits unsigned, the resolution is 0.5K and the data is offset by 40K. The driver PCB NTC temperature data is refreshed with a rate defined by S_{NTC1}. The external NTC temperature data is refreshed with a rate defined by S_{NTC2}.

Examle of data values DAT[11..0]	Temperature (°C)
0000 0000 0000	-40 °C (minimum)
0000 0000 0001	-39.5 °C
0000 0100 1111	-0.5 °C
0000 0101 0000	0 °C
0000 0101 0001	0.5 °C
0001 0001 1000	100 °C
0001 0101 0100	130 °C (maximum)

Note that unconnected NTC will generate a -40°C temperature value.

CRC[2..0]
These are a 3 bit Cyclic Redundancy Checks (CRC) covering the following bit fields respectively: DLK[5..0], DLK[11..6], DAT[5..0], DAT[11..6], ADR[2..0]. The CRC parameters calculation is as folllows:

CRC polynomial coefficient	x^3 + x + 1
CRC width	3 bits
CRC shift direction	right (little-endian)
CRC initial value	0

Absolute Maximum Ratings

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Units
Absolute Maximum Ratings[1]					
Supply Voltage	$V_{VISO-COM}$	VISO to COM		28	V
Average Supply Current	I_{DC}	Average supply current		TBD	mA
Gate Output Power[2]	P_G			3	W
Switching Frequency	f_{SW}	Continuous		3	kHz
DC-Link Voltage	$V_{DC-LINK}$	Switching operation (continuous)		2200	V
		Switching operation[3] (short-term)		2500	
		Off State[4]		3000	
Operating Voltage	V_{CE}	Collector-emitter voltage		3300	V_{PEAK}
Storage Temperature[5]	T_{ST}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Component Surface Temperature[6]	T_{SURF}			125	°C
Relative Humidity	H_R	No condensation		95	%
Altitude of Operation[7]	A_{OP}			4000	m
Voltage on X2 (DLK_P)		Referenced to emitter voltage	-10	50	V

Recommended Operating Condition

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Units
Power Supply						
Supply Voltage	$V_{VISO-COM}$	VISO to COM	23.5	25	26.5	V

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Actually achievable maximum power depends on several parameters and may be lower than the given value. It has to be validated in the final system. It is mainly limited by the maximum allowed surface temperature.
3. This limit is only valid in on-state condition (switching) and must be limited to short periods of time (≤ 60 s). Note that this parameters may be limited to lower values for specific IGBT modules.
4. This limit is only valid in off-state condition (not switching) and must be limited to short periods of time (≤ 60 s).
5. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85 °C.
6. The component surface temperature, which may strongly vary depending on the operating condition, must be limited to the given value to ensure long-term reliability of the product.
7. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Characteristics

Parameter	Symbol	Conditions $V_{VISO-COM}$ = 25 V, T_A = 25 °C		Min	Typ	Max	Units
Power Supply							
Supply Current	$I_{VISO-COM}$	Without load			44		mA
		P_G = 2.5 W, f_{SW} = 3 kHz, 50% duty cycle			149		
Power Supply Monitoring Threshold	$UVLO_{VISO}$	Referenced to E	Clear fault (resume operation)		13.0		V
			Set fault (suspend operation)		13.5		
			Hysteresis		0.5		
	$UVLO_{COM}$		Clear fault (resume operation)		-5.2		V
			Set fault (suspend operation)		-5.4		
			Hysteresis		0.2		
Power Supply Monitoring Filter Time	t_{UVLO}				4.0		µs
Timing Characteristics							
Gate Turn-On Delay	$t_{P(LH)}$	OIN-Light ON to 10% of $V_{GE(ON)}$, no load attached, 1m FO cable to external control, pulse suppression time $t_{PULSE(ON)}$ included			3.5		µs
Gate Turn-Off Delay	$t_{P(HL)}$	OIN-Light OFF to 90% of $V_{GE(OFF)}$, no load attached, 1m FO cable to external control, pulse suppression time $t_{FILTER(ON)}$ included			3.6		µs
Minimal Gate Turn-On Pulse Suppression Time	$t_{FILTER(ON\_PULSE)}$				3.2		µs
Minimal Gate Turn-Off Pulse Suppression Time	$t_{FILTER(OFF\_PULSE)}$				3.2		µs
Propagation Delay of Fault Short Circuit to UART at the Optical Transmitter[13]	$t_{SC\_VCE(LH)}$	Complete UART frame. Parity and stop bits included.			1.9 to 4.2		µs
Propagation Delay of Fault Undevoltage to UART at the Optical Transmitter[13]	$t_{UVLO(LH)}$	Complete data packet, inclusing status register, CRC and UART stop bits are included.			TBD		µs
Propagation Delay of Warning Gate Monitoring to UART at the Optical Transmitter[8]	$t_{GMON(LH)}$				TBD		µs
Propagation Delay of OIN Status to UART at the Optical Transmitter[8]	t_{OIN}				TBD		µs
Duration of Fault State Short-Circuit Condition[8]	$t_{FAULT(SC)}$			3 to 5 UART frame			
Blocking Time	t_{BLK}	After fault detection			20		ms

Characteristics (Cont.)

Parameter	Symbol	Conditions $V_{VISO-COM}$ = 25 V, T_A = 25 °C		Min	Typ	Max	Units
Short-Circuit Protection							
Static V_{CE}-Monitoring Threshold	$V_{CE(SAT)}$				143		V
Response Time	t_{RES}	10% to 90% of V_{GE}	DC-link voltage = 2400 V		7.5		µs
			DC-link voltage = 1800 V		7.7		
			DC-link voltage = 1200 V		8.0		
Turn-Off Delay after Short-circuit Detection	$t_{P(HL)FAULT}$				0.2		µs
Gate monitoring[9]							
Turn-On Threshold	$V_{GE(ON)MAX}$	G to E, set fault			12.9		V
Turn-Off Threshold	$V_{GE(OFF)MIN}$	G to E, set fault			-7.8		V
Filter Delay	$t_{D(FILTER)}$	Turn-on			30		µs
		Turn-off			30		
DC-Link Voltage Measurement							
DC-Link measuring range[10]	V_{DLK_RANGE}			0		3200	V
DC-Link measuring output resolution[10]	V_{DLK_RES}				1		V
DC-Link measuring tolerances[11]	tol_{DLK}	DC-Link voltage between 500V and 3200V			±2		%
DC-Link filter frequency	f_{DLK}	Cut-off frequency at -3dB			10		kHz
DC-Link response time[11]	t_{DLK}	Time to reach 95% of measured value			100		µs
DC-Link data refresh rate	S_{DLK}				75		kHz
Driver PCB Temperature (NTC_1) Measurement [12]							
NTC_1 measuring range	V_{NTC1_RANGE}			-40		130	°C
NTC_1 measuring output resolution	V_{NTC1_RES}				0.5		K
NTC_1 measuring tolerances	tol_{NTC1}	At temperature of 85 °C			±3		K
NTC_1 filter frequency	f_{NTC1}	Cut-off frequency at -3 dB			50		Hz
NTC_1 response time	t_{NTC1}	Time to reach 95% of measured value			TBD		ms
NTC_1 data refresh rate	S_{NTC1}				1.2		kHz

Characteristics (Cont.)

Parameter	Symbol	Conditions $V_{VISO-COM}$ = 25 V, T_A = 25 °C	Min	Typ	Max	Units
External Temperature (NTC_2) Measurement[13]						
NTC_2 measuring range	V_{NTC2_RANGE}		-40		130	°C
NTC_2 measuring output resolution	V_{NTC2_RES}			0.5		K
NTC_2 measuring tolerances	tol_{NTC2}	Temperature from -20 °C to 130 °C, excluding external NTC tolerance		±2		K
NTC_2 filter frequency	f_{NTC2}	Cut-off frequency at -3 dB		50		Hz
NTC_2 response time	t_{NTC2}	Time to reach 95% of measured value		TBD		ms
NTC_2 data refresh rate	S_{NTC2}			1.2		kHz
UART Protocol Characteristics						
UART Baud Rate	BR_{UART}			5		MBd
UART Baud Rate tolerance	BR_{UART_TOL}			1		%
UART frame duration	t_{UART}	Start bit, data bits, parity bit and and Stop bits included		2		µs
Data packet duration	t_{PACKET}	No short circuit detected		10		µs
Inter-data-packet delay	t_{IDLE}	No short circuit detected		3.3		µs
Data packet rate	f_{DATA}	No short circuit detected		75		kHz
Mounting[14]						
Mounting Holes	D_{HOLE}	Diameter of screw hole S1		4		mm
Mounting Torque	M	Screw M4, as per IGBT data sheet				Nm
Bending	I_{BEND}	According to IPC			0.75	%
Gate Output						
Turn-On Gate Output Voltage	$V_{GE(ON)}$	Steady-state		15		V
Turn-Off Gate Output Voltage	$V_{GE(OFF)}$	Steady-state		-10		V

NOTES:

8. The specified delay shows a variation that depends on the asynchronous nature of the protocol.
9. The Gate-Emitter voltage value is filtered and compared to the given values at turn-on and turn-off. If the specified values are exceeded ($V_{GE} < V_{GE\_mon(ON)}$ at turn-on respectively $V_{GE} > V_{GE\_mon(OFF)}$ at turn-off) after the given filter delay $t_{GE\_mon(FILTER)}$, the driver sets a warning status bit in the status register.
10. With an external resistance value of 4.32MΩ.
11. Assessed with an exernal chain resistors of 16 series resistors of 270kΩ, 0.1% tolerances (i.e. 4.32MΩ). Valid from DC-link measuring point to optical transmitter.
12. This is the tempeature measured on the driver PCB, which is typically higher than the ambient temperature by an amount of 10K to 20K.
13. The external temperature measurement is specified with a NTC with the following characteristics: R_{25} = 10 kΩ, $B_{25/85}$ = 3435 K.

Product Dimensions

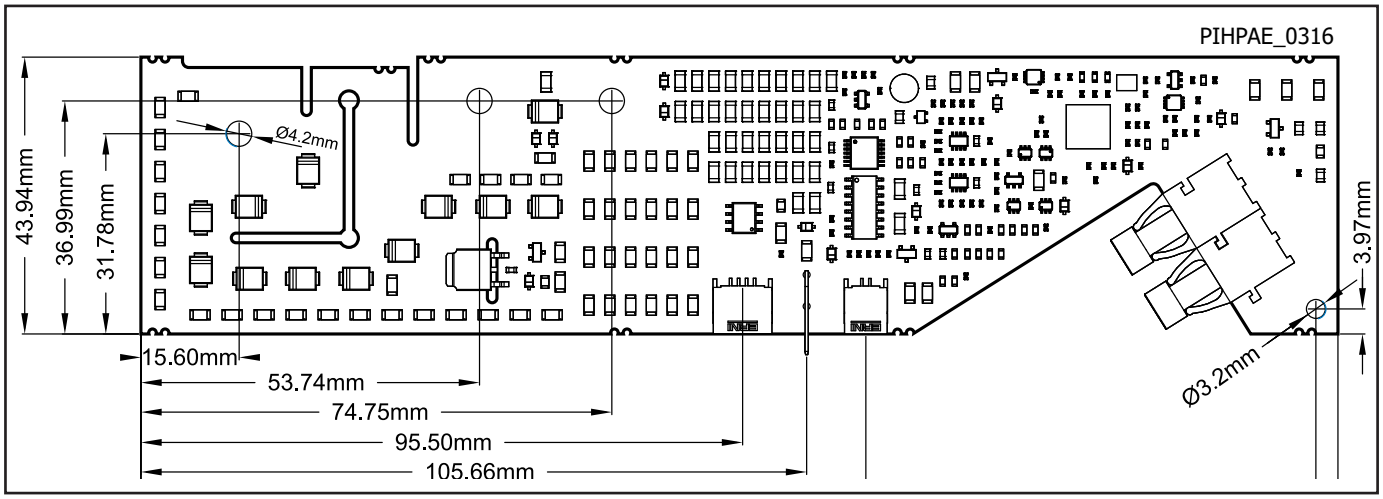

Figure 13. Top View.

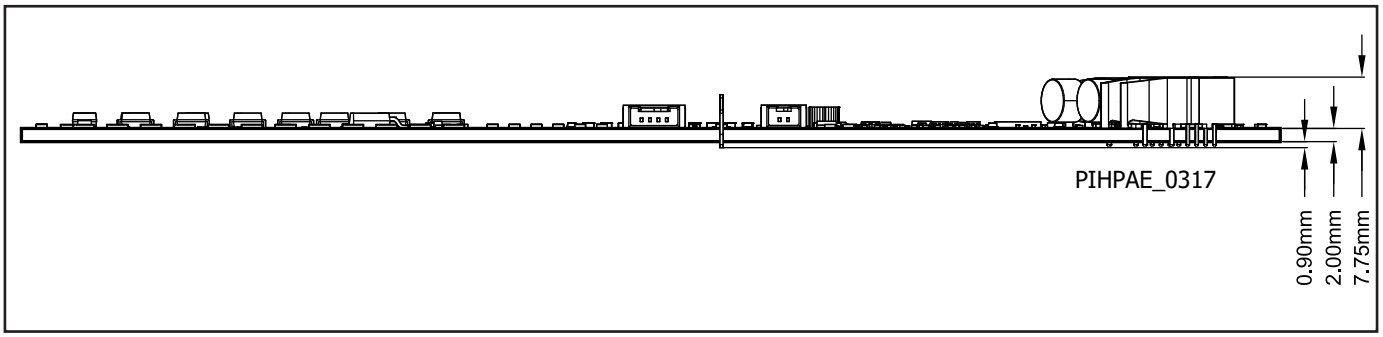

Figure 14. Side View.

Conformal Coating

The electronic components in the gate driver are protected by a layer of acrylic conformal coating on both sides of the PCB with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/4 from Lackwerke Peters. This coating layer increases product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer must be prevented. This water will diffuse through the layer over time. If allowed to remain, it will eventually form a thin film between the PCB surface and coating layer, which will cause leakage currents to increase. Such currents will interfere with the performance of the gate driver.

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according to Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Product Details

Part Number	Power Module	Voltage Class	Current Class	Package	IGBT Supplier	$R_{G(ON)}$	$R_{G(OFF)}$	C_{GE}
1SP0635V2A0D-FZ2400R33HE4	FZ2400R33HE4	3300 V	2400 A	IHV	Infineon	0.52 Ω	3.58 Ω	Not Assembled

Revision	Notes	Date
A	Preliminary Datasheet.	04/23

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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