Absolute Maximum Ratings – 1SP0351V2A0C-5SNA2000K452300

Parameters	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Unit
Absolute Maximum Ratings[1]					
Primary-side supply voltage	V_{V15}	V15 to GND	0	16	V
Primary-side supply current	I_{V15}	Steady-state condition		360	mA
Switching Frequency	f_{SW}	Continuous operation		2	kHz
Gate output power	P_G	T_A = 85 °C		1.8	W
Gate output current	I_G			50	A
Test voltage primary-side to secondary-side	$V_{iso,ps}$	50 Hz, 60 s		10200	V_{RMS}
Operating voltage primary-side to secondary-side	V_{op}	Transient only		4500	V_{pk}
		Permanently applied		3400	V_{DC}
DC-link voltage	V_{DLK}	Switching operation		3400	V
		Off-state, limited to 60 s		4000	V
Storage temperature[2]	T_{stg}		-40	50	°C
Operating ambient temperature	T_A		-40	85	°C
Surface temperature[3]	T_{sf}			125	°C
Relative humidity	H_r	No condensation		93	%
Altitude of operation[4]	A_{op}			2000	m

Notes:

1. ⚠ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
3. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
4. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Recommended Operating Conditions – 1SP0351V2A0C-5SNA2000K452300

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Unit
Power Supply						
Primary-Side Supply Voltage	V_{V15}	V15 to GND	14.5	15	15.5	V

Characteristics – 1SP0351V2A0C-5SNA2000K452300

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Power Supply							
Supply current	I_{V15}	V_{V15} = 15 V, without load			150		mA
		V_{V15} = 15 V, P_G = $P_{G,max}$			280		mA
Power supply monitoring threshold (secondary-side)	$UVLO_{VISO}$	Referenced to terminal E	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
	$UVLO_{COM}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		V
			Hysteresis		0.3		V
Output voltage (secondary-side)	V_{VISO}	Referenced to V_{COM}	V_{V15} = 15 V, without load		24.4		V
			V_{V15} = 15 V, P_G = $P_{G,max}$		24.1		V
Coupling capacitance	C_{io}	Primary-side to secondary-side			8		pF
Timing Characteristics							
Turn-on delay[5]	$t_{P(LH)}$	OIN to 50% of $V_{GE(on)}$, no load attached (optical cable length 1 m)			100		ns
Turn-off delay[5]	$t_{P(HL)}$	OIN to 50% of $V_{GE(off)}$, no load attached (optical cable length 1 m)			125		ns
Transmission delay of fault state[6]	t_{OOUT}	Optical cable length 1 m			100		ns

Notes:

5. Measured from the transition of the turn-on or turn-off command at the optical transmitter of the external controller to the direct output of the gate drive unit (excluding the delay of the gate resitors).
6. Measured from the driver secondary-side (ASIC output) to the optical receiver on the external controller.

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Timing Characteristics (cont.)						
Delay to clear fault state[8]	t_{blk}	Measured on the external controller side (optical cable length 1 m)		8		µs
Acknowledge delay time[9]	$t_{d(ack)}$	Optical cable length 1 m		190		ns
Acknowledge pulse width	t_{ack}	Measured on the external controller side (optical cable length 1 m)	400	600	1050	ns
Gate Output						
Gate turn-on voltage	$V_{GE(on)}$	V_{V15} = 15 V, without load, referenced to terminal E		15		V
		V_{V15} = 15 V, P_G = $P_{G,max}$ referenced to terminal E		15		V
Gate turn-off voltage	$V_{GE(off)}$	V_{V15} = 15 V, without load, referenced to terminal E		-9.4		V
		V_{V15} = 15 V, P_G = $P_{G,max}$ referenced to terminal E		-9.1		V
Short-Circuit Protection						
Static VCE-monitoring threshold	$V_{CE(stat)}$			680		V
Response time	t_{res}	DC-link voltage = 3400 V		8		µs
		DC-link voltage = 2800 V		8		µs
		DC-link voltage = 1500 V		8		µs
Delay to power semiconductor turn-off after short-circuit detection	$t_{pd,SC}$			0.2		µs

Notes:

8. The fault status is stretched by the given value after the fault condition has been turned-off.
9. Measured from the transition of the turn-on or turn-off command at the optical transmitter of the external controller to the transition of the acknowledge signal at the optical receiver of the external controller.

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Electrical Isolation						
Test voltage[10]	$V_{iso,ps}$	Primary-side to secondary-side	10.2			kV_{RMS}
Partial discharge extinction voltage[11]	$P_{D,ps}$	Primary-side to secondary-side	5400			V_{pk}
Creepage distance	$CPG_{P-S,PCB}$	On the PCB (Material group IIIa), Primary-side to secondary-side	45			mm
	$CPG_{P-S,Trf}$	On the transformer (Material group I), Primary-side to secondary-side	36			mm
Clearance distance	CLR_{P-S}	Primary-side to secondary-side	25			mm
Mounting						
Terminal connection torque	M_{M4}	Screw M4	1.8		2.1	Nm
Bending[12]	l_{bend}	According to IPC			0.75	%
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			1.875		Ω
Turn-off gate resistor	$R_{G(off)}$			8.5		Ω
Auxiliary gate capacitor	C_{GE}			330		nF

Notes:

10. The transformer of every production sample has undergone 100% testing at the given value for 1s.
11. Partial discharge measurement is performed on each transformer. The measurements are performed in accordance with IEC 60270 and IEC 60664-1 for basic insulation requirements.
12. Refer to section Mounting Instruction for absolute values of allowed bending distances.

Mounting Instruction

The gate driver has to be mounted on top of a suitable surface using the provided non-plated fixation holes S1 to S8 as shown in Figure 7. To avoid corona effects non-conducting M4 screws have to be used.

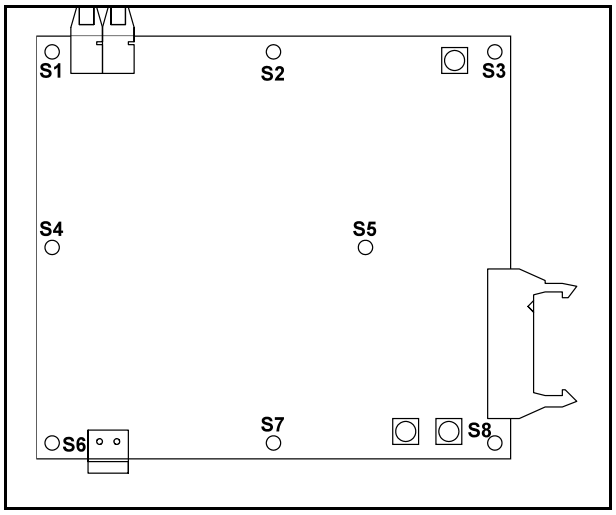


Figure 7. Fixation Points

To avoid mechanical stress of the gate driver during and after the mounting process any bending or warping force imposed to the gate driver must not lead to a vaulting or twisting of the PCB of 0.75 % per axis according to Figure 8:

- Axis 1 and 3: max. 1.4 mm bending
- Axis 2: max. 1.0 mm bending
- Axis 4: max. 1.1 mm bending

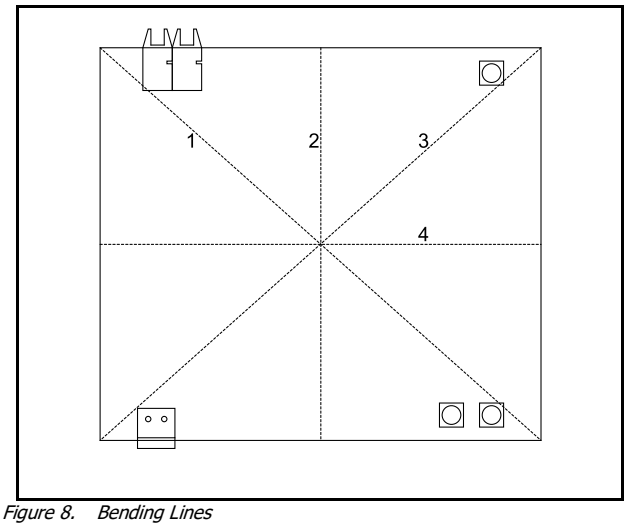


Figure 8. Bending Lines

The maximum mounting force for the terminal C is given with M_{M4}.

As the 1SP0351V2A0C-5SNA2000K452300 is designed for high voltage applications care has to be taken concerning the surrounding area of the gate driver. The gate driver itself possesses a basic isolation with clearance and creepage distances of CLR_{P-S} and $CPG_{P-S,PCB}$. To maintain this isolation the following distances according to Figure 9 must be kept:

d_1: It defines the distance between the surrounding area and any primary-side potential of the gate driver. If the surrounding area is connected to the primary-side GND potential, d_1 can be set to 0 mm. Otherwise d_1 has to be set according to the nearest potential and relevant standard for isolation coordination of the application.

d_2: It defines the distance between the surrounding area and the top of the DC/DC transformer. This distance must not be smaller than 20 mm.

d_3: It defines the distance between the bottom side of the gate driver PCB and the mounting plate. In case the mounting plate is made of metal and/or is electrically conducting the isolated stand-offs must have a distance as defined in the isolation coordination of the application. In case the mounting plate is non-conducting any surrounding conducting area has to be kept away from the bottom side of the gate driver with a distance of not smaller than 20 mm, i.e. $d_3 = d_2$.

d_4: If defines the distance between the top side of the gate driver PCB and the surrounding area. The distance must be chosen according to the isolation coordination of the application plus 4 mm (to respect the height of mounted components on top of the gate driver PCB).

d_5: It defines the distance between the surrounding area and any secondary-side potential of the gate driver. The distance must be chosen according to the isolation coordination of the application.

d_6: It defines the distance between the collector, emitter and/or gate cables to the surrounding area. The minimum distance is defined according to the nearest potential and relevant standard for isolation coordination of the application. However, the distance must not be smaller than 20 mm.

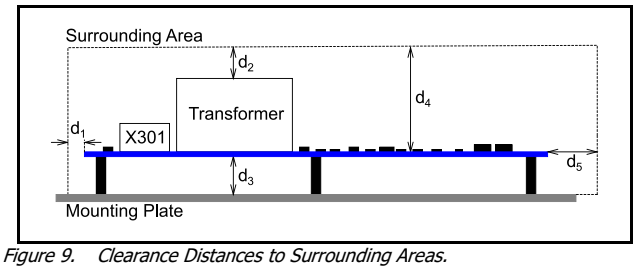


Figure 9. Clearance Distances to Surrounding Areas.

Cables

The cable from gate driver connector X301 to the power supply is not part of the 1SP0351V2A0C-5SNA2000K452300 gate driver. It is recommended to route the cable with minimum parasitic coupling from the controller to the gate driver. Parasitic coupling in particular to any potential of the secondary-side of the gate driver (i.e. high voltage side) and the AC and/or DC bus bar has to be avoided. Otherwise, increased common-mode currents may circulate, which may cause interferences with command and/or status feedback signals.

Application Guidelines

The following guidelines are meant to optimize the overall system performance when using 1SP0351V2A0C-5SNA2000K452300 gate drivers in various applications.

Power Supply

The gate driver has to be supplied by a fixed voltage of typically 15V at V15.

Gate Output Power Calculation

The gate driver can provide up to 1.8 W of gate output power. This value must not be exceeded to prevent any electrical and/or thermal overload of the 1SP0351V2A0C-5SNA2000K452300 gate driver.

The gate output power is related to the power semiconductor's gate charge Q_G as stated in the correspondig datasheet, actual switching frequency f_{SW}, and gate turn-on $V_{GE(on)}$ and turn-off $V_{GE(off)}$ voltage and can be estimated according to equation (1).

$$P_g = Q_G \cdot \frac{\left(V_{GE(on)} - V_{GE(off)}\right)^2}{V_{GE(on)*} - V_{GE(off)*}} \cdot f_{SW} \qquad (1)$$

The voltages $V_{GE(on)*}$ and $V_{GE(off)*}$ refer to the referenced gate turn-on and turn-off gate voltages of the respective driven power semiconductor datasheet at which the gate charge Q_G is given.

DC-Link Design

The mechanical and electrical design of the DC-link of the target application determines during turn-off or diode reverse recovery events of the driven power semiconductor the over voltages ΔV_{CE} according to equation (2). Here, L_σ describes the overall DC-link stray inductance (i.e. sum stray inductance of DC-capacitors, DC-link bus bar and power semiconductor) and relevant di_C/dt the collector current change.

$$\Delta V = L_\sigma \cdot \frac{di_C}{dt} \qquad (2)$$

If the over voltage ΔV_{CE} plus the applied DC-link voltage V_{DC} exceed the breakdown voltage of the driven power semiconductor (refer to the reverse bias safe operating area RBSOA resp. to the reverse recovery safe operating area RRSOA), the device may be damaged. In case of excessive turn-off or reverse recovery over voltages, one or more of the following application parameters have to be decreased:

- DC-link voltage V_{DC}
- Stray inductance L_σ
- Collector current i_C (only for turn-off even)

Therefore, during the installation and testing of the target application the actual over voltages ΔV_{CE} at different conditions have to be measured.

Note: 1SP0351V2A0C-5SNA2000K452300 gate driver will actively limit any over voltage during turn-off events under normal and over current conditions to safe levels using the implemented Dynamic Advanced Active Clamping scheme. However, it is not recommened that the clamping feature is active during normal switching conditions. It may lead to an over load of the implemented clamping devices. Furthermore, it might lead to an under voltage lock-out (UVLO) condition on the secondary-side power supply of the gate driver and an increase of the turn-off switching losses.

Multilevel Topologies

1SP0351V2A0C-5SNA2000K452300 gate driver are designed for 2-level topologies. Operation within 3-level or multilevel designs is, however, also possible:

- Cascaded multilevel topologies on system level like for instance Modular Multilevel Converter (MMC) operating with 2-level topologies within one cell are supported without any restriction (implying that required isolation requirements are fulfilled).
- For 3-level systems the turn-off sequence has to be obeyed by the system controller to avoid overvoltage events, which might lead to an RBSOA (reverse biased safe operating area) violation of the power semiconductor. However, 1SP0351V2A0C-5SNA2000K452300 gate driver have Power Integrations' Dynamic Advanced Active Clamping (DA²C) implemented, which enables the gate driver to protect the power semiconductor against over voltage conditions arising by wrong turn-off sequences. The suitability of DA²C has to be checked within the target application.

  Note: During short-circuit and/or under voltage events, the gate driver will immediately switch-off the respective power semiconductor. No control on the turn-off sequence is given. Therefore, the suitability of 1SP0351V2A0C-5SNA2000K452300 has to be checked on application level for this kind of topology.

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50µm using *ELPEGUARD SL 1307 FLZ/2* from *Lackwerke Peters* on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

⚠ Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

Reliability Test Items

Test Item	Test Methods and Conditions
Environmental Tests[13]	
Mechanical vibrations (sinusoidal)	IEC 60068-2-6, frequency range 10 - 150 Hz (7.5 mm displacement, 20 m/s², 30 min), 3 axis, 20 sweep cycles
Damp heat	IEC 60068-2-78, 65 °C (95 % RH, 24 h) → 25 °C (1 h, DUT operated), 10 cycles
Damp heat cyclic	IEC 60068-2-30, 25 °C / 60 % RH → within 1 h up to 95 % RH → within 3 h up to 60 °C → stable 93 % RH for 12 h → within 3 h down to 25 C → end at 24 h, 6 cycles
Dry heat	IEC 60068-2-2, 85 °C (48 h, 2 h recovery, operated after 0.5 h)
Cold	IEC 60068-2-1, -40 °C (48 h, 2 h recovery, operated after 0.5 h)
Salt spray	IEC 60068-2-11, 5 % concentration, 35 °C, 48 h → 25 °C, 1 h recovery → DUT operated
Change of temperature	IEC 60068-2-14, -40 °C and 85 °C, holding time 3 h, 10 cycles (read-out after 5th cycle, DUT operated at -10 °C and 70 °C)
Endurance Tests	
High temperature, high load test	V_{V15} = 15 V, P_G = $P_{G,max}$ (capacitive load), 85 °C, test duration 1000 h
Thermal cycling	IEC 60068-2-14, -40 °C → 125 °C (5K/min, 500 cycles, DUT unpowered)

EMC Test Items

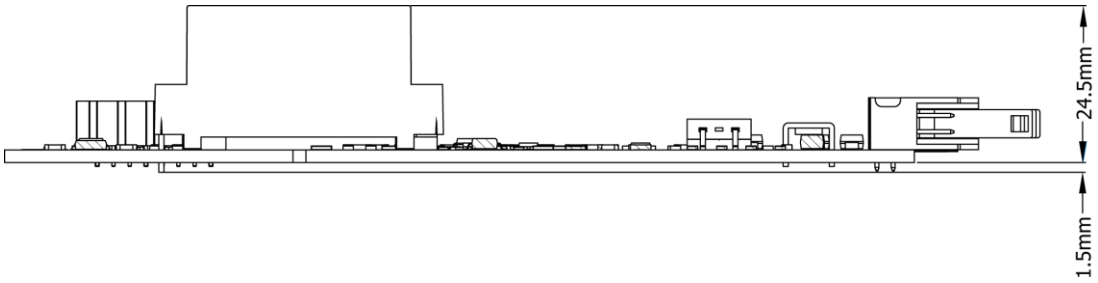
Test Item	Test Methods and Conditions
EMC Tests	
Electrostatic discharge immunity	IEC 61000-4-2, contact discharge 8 kV, air discharge 15 kV, terminal test points C, E, G and GND
Radiated noise immunity	IEC 61000-4-3, frequency range 80 – 3000 MHz, sine wave 80% AM modulated (1 kHz), 30 V/m
	IEC 61000-4-3, frequency points 80 / 160 / 380 / 450 / 900 MHz, sine wave 80% AM modulated (1 kHz), 30 V/m, test duration 15 s per frequency point
Fast transient burst immunity	IEC 61000-4-4, capacitive clamp with 50 Ω termination, ±5 kV, 5 kHz (15 ms) and 100 kHz (0.75 ms), test points V15 and GND / C and E with attached power semiconductor, test duration 200 s
Conducted noise immunity	IEC 61000-4-6, frequency range 0.15 – 80 MHz, sine wave 80% AM modulated (1 kHz), 20 V_{RMS}, test points V15 and GND
Magnetic field immunity	IEC 61000-4-8, 100 m/A (30 s), 1000 A/m (1 – 3 s), 3 axis
	IEC 61000-4-9, 1000 A/m, 5 cycles, 3 axis
	IEC 61000-4-10, 100 A/m, 100 kHz and 1 MHz, 3 axis, test duration 2s
Ring wave immunity	IEC 61000-4-12, line-to-line 2 kV, line-to-ground 4 kV, test points V15 and GND
Damped oscillatory wave immunity	IEC 61000-4-18, common mode 2 kV, differential mode 1 kV, 100 kHz and 1 MHz, test points V15 and GND
Radiated Noise	EN 55032:2015 (CISPR32:2015)

Notes:

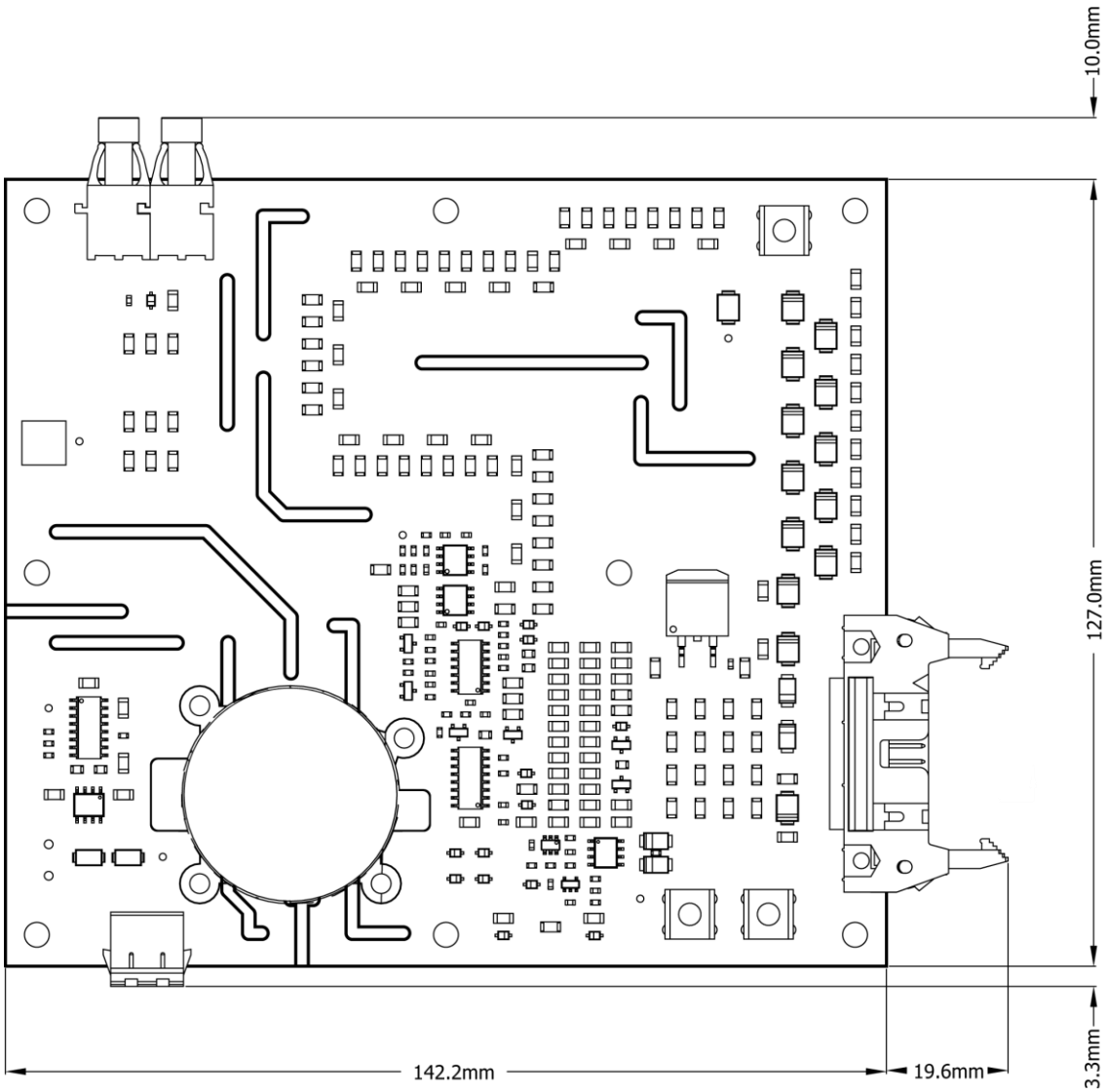
1. All environmental tests are conducted on the same sample in the given order of tests.

Product Dimensions - 1SP0351V2A0C-5SNA2000K452300

Side Views



Top View



all measures in mm

Figure 10. Dimensions.

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Revision	Notes	Date
A	Final Datasheet	08/20

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