1250 V / 1700 V PowiGaN™ for 800 VDC AI Data Center Architecture

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Introduction

GaN-based power semiconductor devices are ideally suited for high-efficiency power converters due to their superior material properties. GaN HEMTs have been adopted into many commercial power supply designs covering a broad range of applications taking advantage of the technology's fast-switching capability with low losses.

Commercially available devices from various manufacturers typically offer voltage ratings below 200 V and in the 600 V-650 V range. Beyond 650 V, only a few manufacturers have released GaN HEMTs with a rated voltage of 900 V. Commercially available GaN HEMT technologies built using a silicon substrate are very difficult to scale to voltages beyond 900 V due to the need for very thick buffer layers, which adds significant processing challenges.

Because of this, applications needing wide-bandgap power devices with 1200 V rating and beyond have been constrained to using SiC switches. However, GaN enables much higher switching frequency compared to SiC and can provide a pathway to meeting the increasing power density required by applications, such as artificial intelligence (AI) data centers, while maintaining high efficiency. GaN HEMTs built by Power Integrations with its proprietary PowiGaN™ technology offer a unique advantage of being capable of achieving a very high voltage rating (up to 1700 V) in a practical device, making it a readily available and compelling alternative to 1200 V SiC and beyond.

To take advantage of the benefits of GaN in 800 VDC bus applications, 650 V GaN devices have been used in a two-in-series stacked half-bridge configuration with a total of four 650 V GaN devices. While this stacked topology can operate at the high frequencies that GaN is capable of, it introduces several challenges including increased control complexity, reliability risk due to input voltage imbalance, increased footprint, and increased conduction loss resulting in lower efficiency and higher cost. In contrast, using a 1250 V rated PowiGaN switch in this application would simplify the power converter topology significantly while taking full advantage of the properties of GaN that make it an ideal high-frequency power switch.

With the 1250 V PowiGaN cascode switch, power supply designers can reliably specify an operating peak V_{DS} of 1000 V, while allowing for industry-standard 80% de-rating. For applications exceeding an operating peak V_{DS} of 1000 V and up to 1360 V, using the 1700 V PowiGaN cascode switch allows the user to design similarly high-efficiency power supplies, but now at an even higher voltage. In this paper, we describe the reliability and robustness of industry-first GaN power switches with rated voltages beyond 1200 V and illustrate their suitability to meet the power density and >98% efficiency requirements of the NVIDIA 800 VDC AI data center architecture.

1250 V / 1700 V GaN HEMT Cascode Switch from Power Integrations

The 1250 V / 1700 V GaN HEMT is a normally-on, depletion mode device built using Power Integrations' proprietary PowiGaN technology. It is connected in series with a low-voltage silicon MOSFET in a cascode configuration to achieve effective normally-off operation, which is essential for safe operation of power electronic systems. The depletion-mode GaN devices are regarded as highly reliable since they do not require a p-type GaN gate layer. As a result, they avoid threshold voltage drift and related instability concerns, ensuring long-term stability. The circuit schematic for the cascode switch with the high-voltage GaN HEMT and a low-voltage silicon MOSFET is shown in Fig. 1. A micro-photograph of a 60 mOhm (Max @ 25 °C), 1250 V GaN cascode switch with the low-voltage silicon MOSFET stacked on top of the GaN HEMT is shown in Fig. 2.

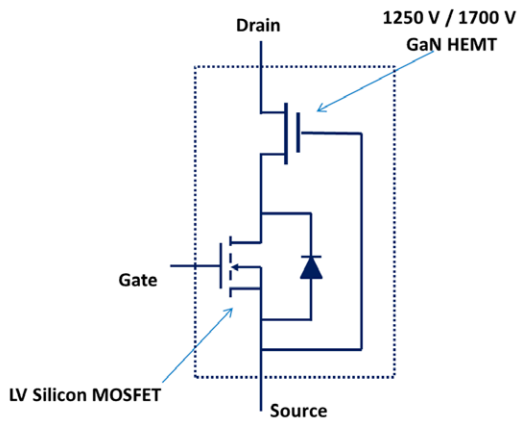

Fig. 1. Schematic of the high-voltage PowiGaN cascode switch

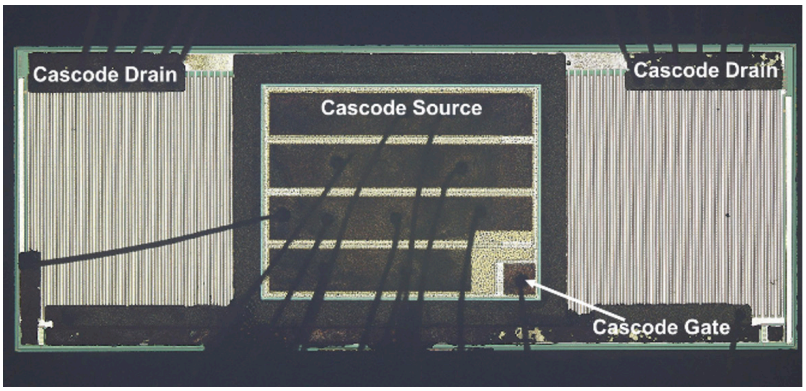

Fig. 2 Micro-photograph of a 60 mOhm, 1250 V PowiGaN cascode switch

Off-state characteristics of a typical 1250 V and 1700 V PowiGaN cascode switch are shown in Figs. 3 and 4, illustrating stable leakage behavior well beyond their voltage rating ensuring excellent transient overvoltage capability. This demonstrates significant safety margin compared with similarly rated silicon or SiC devices.

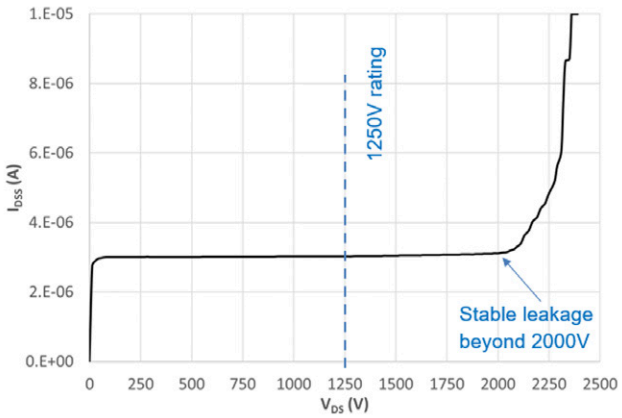

Fig. 3 Typical off-state characteristics of the 1250 V PowiGaN cascode switch

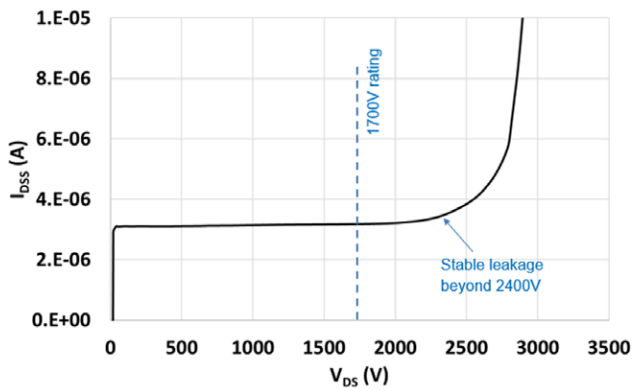

Fig. 4 Typical off-state characteristics of the 1700 V PowiGaN cascode switch

Ensuring Field Reliability

While having good electrical characteristics is important, the power device must also be able to meet and exceed industry-standard reliability qualification requirements to ensure reliable operation in the field. In this section, we share results from critical high-voltage reliability stress evaluations covering both static and dynamic conditions that were performed as part of the qualification of the 1250 V GaN HEMT for power conversion applications.

A. High Temperature Reverse Bias (HTRB)

High Temperature Reverse Bias (HTRB) is an off-state reliability stress test that evaluates the long-term stability of the power device under high drain-to-source bias and is intended to accelerate thermally activated failure mechanisms under high E-fields over an extended period. HTRB stress test of the 1250 V GaN cascode switch was performed in a 150 °C ambient environment and stressed with an off-state V_{DS} of 1000 V (80% of 1250 V rating) for 1000 hours with passing results in accordance with the specifications laid out in the JEDEC HTRB guideline, JEP198. Excellent device leakage stability was observed as shown in Fig. 5, validating its suitability for high-reliability applications at high voltage.

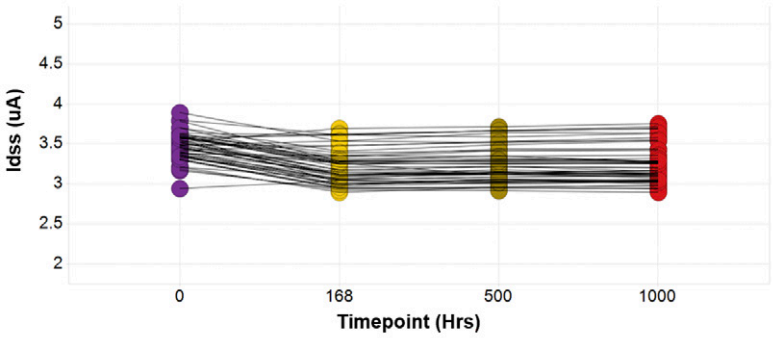

Fig. 5 Stable off-state drain leakage through 1000 hours of HTRB stress at 1000 V / 150 °C

Voltage/Temperature	80 °C	100 °C	120 °C
2100 V		✓	
2150 V	✓	✓	✓
2200 V		✓	

Table 1 Accelerated evaluation conditions in the off-state

In addition to the HTRB qualification test described above, intrinsic off-state failure rates were extracted by running tests on a large number of units under accelerated V_{DS} conditions (2100 V to 2200 V) across multiple temperatures (80 °C to 120 °C) as shown in Table 1.

Based on the time-to-failure Weibull distribution obtained from this set of experiments, a voltage acceleration factor was extracted using an exponential model while the temperature acceleration factor was extracted via an Arrhenius model. The extracted model predicts a cumulative failure rate of 1 ppm in >15 thousand years of operation at 1000 V/100 °C, indicating a significant built-in reliability margin for the 1250 V GaN cascode power switch (Fig. 6).

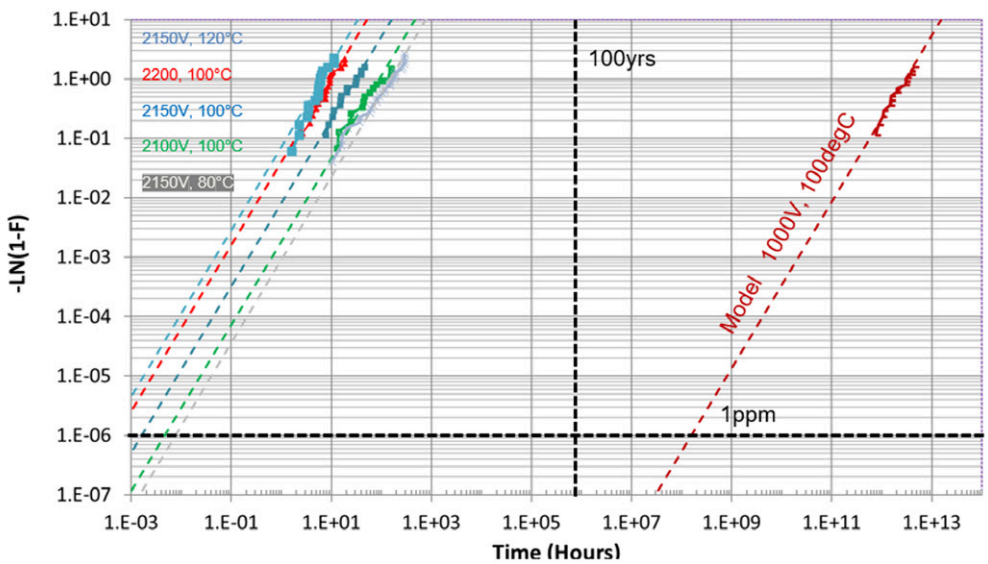

Fig. 6 Weibull distributions indicating time-to-failure under multiple accelerated stress conditions and the projected distribution at 1000 V / 100 °C

B. High-Voltage High-Humidity High-Temperature Reverse Bias (HV-H3TRB)

For many high-reliability deployments, passing HTRB-based off-state reliability qualification stress alone is not sufficient. The product may often be exposed to harsh external environmental conditions, operating continually or for extended periods of time in extreme mission-critical applications. For such applications, it is important to pass the HV-H3TRB test, where a controlled high humidity environment is used as an additional stressor to the original HTRB test. This stress test incorporates additional failure modes due to moisture penetration and is a test for all aspects of the device including passivation layer, active and termination design as well as the underlying structures.

HV-H3TRB stress test of the 1250 V GaN cascode switch was performed in an 85 °C ambient environment with relative humidity (RH) of 85% and stressed with an off-state V_{DS} of 1000 V for 1000 hours, following the JEDEC standard JESD22-A101. Clean passing results were obtained for this stress test with identical off-state leakage stability as during HTRB, shown in Fig. 5.

C. Dynamic High-Temperature Operating Life (DHTOL)

One of the main concerns which initially delayed the commercial introduction of GaN HEMTs was its reliability when switching in high-voltage applications, where the on-resistance of the device was found to increase immediately after turn-on compared to the DC condition. This phenomenon, known as dynamic $R_{DS(ON)}$, is attributed to charge trapping effects within the device under high electric field-strengths. Various techniques have been employed to address this issue including epitaxial structure engineering and carefully optimized processing techniques.

Switching reliability of PI's 1250 V GaN cascode switch was evaluated in a custom testbed in compliance with JEDEC DHTOL guideline JEP180, with the capability to evaluate multiple units in parallel at 125 °C. The most stringent operating conditions possible were chosen — hard-switched turn-on and turn-off at 1000 V–based on the switching locus described in the guideline. For GaN devices, dynamic $R_{DS(ON)}$ during high-voltage switching is of particular interest. An improperly designed GaN HEMT device will likely exhibit a significant increase in $R_{DS(ON)}$ during high-voltage switching transitions due to additional electron trapping, which can have a detrimental effect on the converter efficiency or, even worse, result in hard failures.

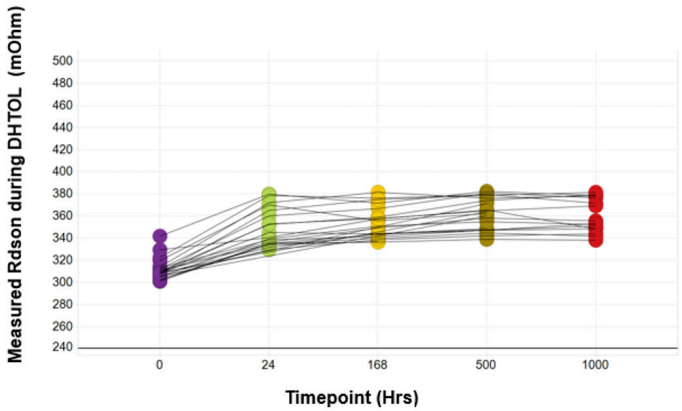

Fig. 7 Stable $R_{DS(ON)}$ observed during 1000 hours DHTOL with minimal shift (<20%)

$R_{DS(ON)}$ of the 1250 V GaN cascode monitored over the course of 1000 hours of DHTOL stress at 1000 V/125 °C shows stable performance (Fig. 7) from the earliest timepoint with a minimal shift of <20% and is on par with state-of-the-art 650 V GaN HEMTs tested under similar hard-switching conditions. This result demonstrates that GaN HEMTs can be scaled to >1200 V without any compromise in performance, including the critical hard-switching capability, and demonstrates their robustness to meet all potential high-reliability applications.

Use Case in NVIDIA 800 VDC AI Data Center Architecture

A. HVDC AI Data Center Architecture Background

It is becoming increasingly clear that high-voltage DC (HVDC) distribution will replace the conventional 54 V DC bus architecture in AI data centers. One of the leading proposals comes from the Open Compute Project (OCP)—initiated by Google, Meta, and Microsoft—which defines a 800 VDC power system. This new architecture transforms power delivery, scaling from the traditional sub-100 kW per rack to 1 MW per rack, while enabling more efficient power conversion and greater power density.

NVIDIA is also proposing an 800 VDC architecture for next-generation AI data centers. By adopting a direct 800 VDC input, compute racks can receive power more efficiently without relying on conventional integrated AC-DC PSU stages. Instead, racks accept two-conductor 800 VDC feeds and use high-voltage isolated DC-DC converters within the rack to supply the xPU subsystems. This approach eliminates rack-level AC-DC conversion blocks, freeing up space for additional compute resources and improving thermal management. Compared to traditional AC-DC architectures, direct 800 VDC input simplifies rack design while simultaneously boosting performance.

At the device level, 1250 V and 1700 V PowiGaN technology can play a critical role in enabling this transformation. Its combination of simplified topology, fast switching speed, and robust voltage capability makes it ideal for high-efficiency, high-density HVDC conversion in the emerging 800 VDC AI data center architecture. This section will explain the value propositions of 1250 V / 1700 V PowiGaN compared with 1) stacked, 650 V e-mode GaN; and 2) a 1200 V SiC MOS.

B. 1250 V PowiGaN vs. 650 V e-mode GaN

Fig. 8 illustrates an 800 VDC input and 12.5 V output fixed-ratio LLC topology comparison between 650 V e-mode GaN and 1250 V PowiGaN. Because of fast-switching GaN devices, both solutions can operate at high frequencies above 500 kHz with 800 VDC input. For 650 V e-mode GaN, a stacked LLC converter is required to withstand the 800 VDC input. On the primary side, this architecture uses two-in-series stacked half-bridges (a total of four 650 V e-mode GaN switches). On the secondary side, the outputs are connected in parallel so that each half-bridge supports half of the total output power. However, this stacked topology introduces several challenges:

- **Input voltage imbalance:** Input voltage imbalance during normal operation must be carefully managed. If imbalance occurs between the half-bridges, the stress voltage across the GaN devices can exceed the expected ~400 V. Under this higher voltage stress, dynamic $R_{DS(ON)}$ degradation becomes more pronounced due to current trapping effects within the HEMT's 2DEG channel. These limitations highlight the reliability and efficiency risks of using 650 V e-mode GaN in stacked configurations for 800 VDC input systems.
- **Complex drive design:** The stacked topology also introduces additional design complexity, particularly in the gate-driver circuitry. Each half-bridge requires a dedicated high-side driver along with an isolated bias supply, further increasing system cost, space, and design overhead.
- **Less efficient and higher cost:** With the same $R_{DS(ON)}$ GaN devices, the stacked topology incurs higher conduction loss compared to a 1250 V PowiGaN single half-bridge topology. This means that a 1250 V PowiGaN design can use devices with 2x higher $R_{DS(ON)}$ while still achieving the same overall efficiency and loss profile.

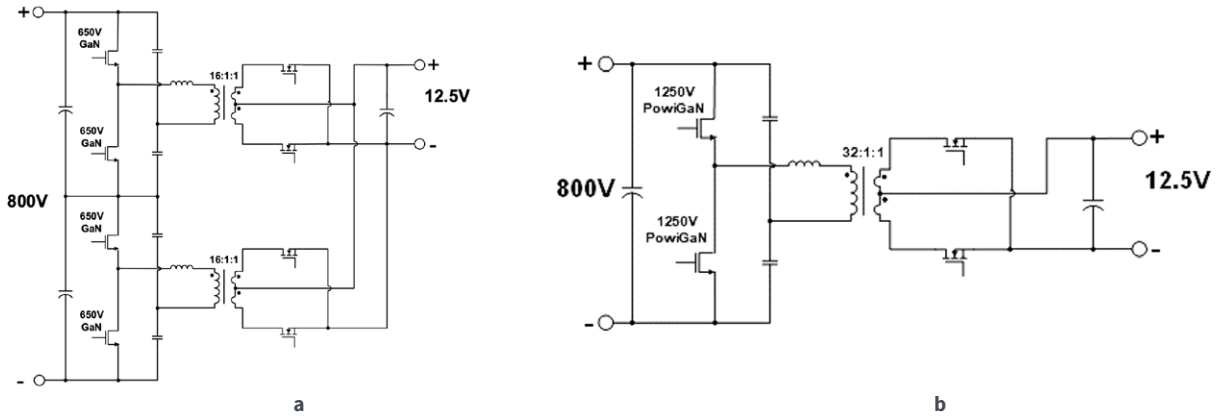

Fig. 8 (a) 650 V e-mode GaN-based stacked half bridge LLC; (b) 1250 V PowiGaN-based single half bridge LLC

Differences between 650 V e-mode GaN and 1250 V PowiGaN in a half-bridge LLC application are summarized in Table 2, illustrating the clear advantages of the single half-bridge approach with 1250 V PowiGaN for high-density 800 VDC power architecture.

	Stacked half-bridge LLC with 650 V e-mode GaN	**Single half-bridge LLC with 1250 V PowiGaN**
Input capacitance imbalance	Yes	No
Gate drivers	4 pcs drivers with 3 pcs isolated drivers	2 pcs drivers with 1 pcs isolated driver
Isolated bias supply for driver	3 pcs	1 pcs
Conduction losses with same GaN $R_{DS(ON)}$	x2 higher losses	—
Required GaN $R_{DS(ON)}$ with same efficiency and loss	—	x2 higher $R_{DS(ON)}$

Table 2 Half-bridge LLC comparison between 650 V e-mode GaN and 1250 V PowiGaN

C. 1250 V PowiGaN vs. 1200 V SiC MOSFET for 1 MHz LLC operation

To achieve high power density, operating the LLC converter at high frequency is crucial and the maximum operating frequency is determined by a few key parameters. Figure 9 shows the LLC equivalent circuit during dead time transition and waveforms. To achieve the ZVS for turn-on, the parasitic output capacitance of the transistor should be fully discharged/charged by using this peak magnetizing current I_{lm_pk} during each dead time. However, the magnetizing current will contribute an additional circulating loss on the primary during the dead time. Minimizing magnetizing current I_{lm_pk} is thus a goal for improving an LLC converter frequency and efficiency.

To achieve higher frequency, the power switch should have a small value of $C_{o(tr)}$ (time-related effective output capacitance), or called Q_{oss} (output charge), which is obtained as the product of $C_{o(tr)} \cdot V_{dc}$. The minimum dead time $t_{deadmin}$ for a half-bridge LLC's ZVS achieving condition can be obtained from equation (1).

$$(1) \quad t_{deadmin} = 8 \cdot C_{o(tr)} \cdot L_m \cdot f_s$$

Here, L_m is the magnetizing inductance of the main transformer and f_s is the switching frequency.

From equation (1), the device parameter $C_{o(tr)}$, which describes the output capacitance needed to transition the drain to source voltage passively, is a key parameter for high-efficiency and high-density LLC converter. For a given L_m and t_{dead}, the lower value of effective $C_{o(tr)}$, the higher switching frequency f_s can be used with ZVS condition to make a higher density.

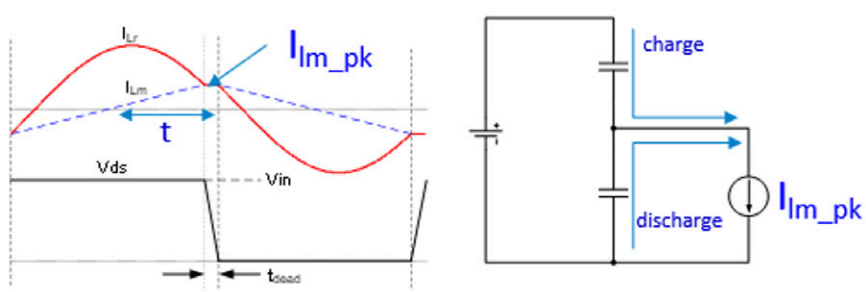

Fig. 9 Primary current and voltage waveform for the half-bridge LLC equivalent circuit during dead time transition

Other key device parameters which influence the switching frequency are the total gate charge Q_g and turn-off delay time $T_{d(off)}$. In short, the lower the values of Q_{oss}, Q_g, and $T_{d(off)}$, the better the performance of the LLC converter designed for efficiency and power density. Table 3 shows the comparison between 1250 V PowiGaN vs. 1200 V SiC MOS. The conclusion is clear that 1250 V PowiGaN can enable a higher-frequency LLC compared to a 1200 V SiC MOS with a similar $R_{DS(ON)}$.

	SiC MOS	PowiGaN	PowiGaN Value Proposition
Voltage Rating (V)	1200	1250	Higher BV
$R_{DS(ON)}$ mΩ 25 °C	60	60	Same $R_{DS(ON)}$
Q_{oss} @ 800 V; nC	180	140	High Frequency
LLC iQ_g; nC	106	45	Low drive loss
$T_{d(off)}$; ns	48	15	Low turn-off loss

Table 3 Parameter comparison between 1200 V SiC MOS and 1250 V PowiGaN

Validating the maximum switching frequency of the 1250 V, 60 mΩ PowiGaN device, Fig. 10 presents the 800 VDC input, 1 MHz half-bridge LC resonant waveforms, compared against a best-in-class 1200 V, 60 mΩ SiC MOS. The results demonstrate that 1250 V PowiGaN technology achieves 1 MHz ZVS operation with a transition dead time of less than 100 ns. In contrast, the 1200 V SiC MOS fails to achieve ZVS at 1 MHz with hard-switching commutation, exhibiting pronounced ringing with higher temperature. Fig. 11 provides zoomed-in V_{GS} and V_{DS} waveforms for turn-off with the same R_{GOFF}=2 Ω: SiC MOS displays a substantially longer Vgs falling time (~3x longer falling time than PowiGaN), effectively capping its practical operating frequency below 500 kHz.

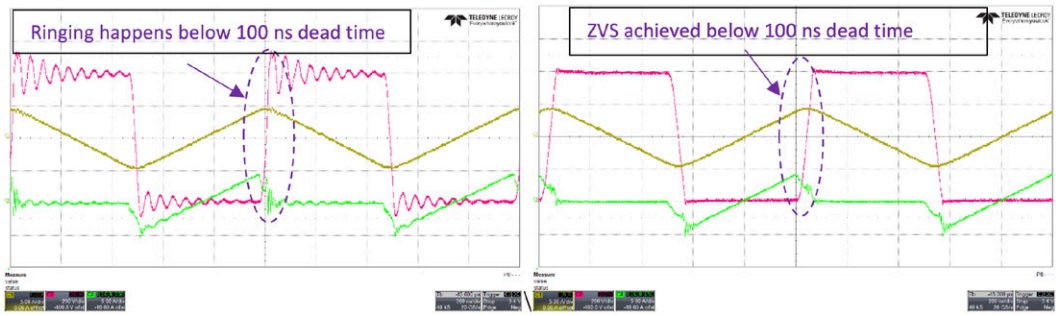

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Fig. 10 (a) 1200 V 60 mΩ SiC MOS 1 MHz resonant waveform; (b) 1250 V 60 mΩ PowiGaN 1 MHz resonant waveform (200ns/div)

(Green: low-side I_D current 5 A/div; Red: half-bridge switching node V_{DS} voltage 200 V/div; Yellow: magnetizing current 5A/div)

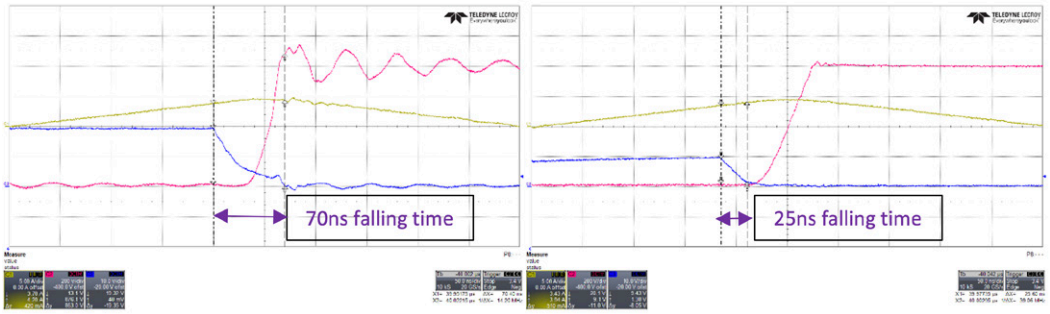

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Fig. 11 Zoomed-in V_{GS} and V_{DS} waveforms for turn-off period (a) 1200 V 60 mΩ SiC MOS 1 MHz resonant waveform; (b) 1250 V 60 mΩ PowiGaN 1 MHz resonant waveform (50ns/div)

(Blue: Gate to source V_{GS} voltage 10 V/div; Red: half bridge switching node V_{DS} voltage 200 V/div; Yellow: magnetizing current 5A/div)

D. 1700 V PowiGaN for HVDC AI data center

In 2024, Power Integrations released an industry-first 1700 V PowiGaN-based product—IMX2353F (520 mΩ at 25 °C)—that easily supports 1000 VDC nominal input voltage while perfectly matching auxiliary power requirements for HVDC AI data center applications. As shown in Fig. 12, IMX2353F belongs to the family of InnoMux™2-EP, which incorporates both primary and secondary-side controllers, with protection, sense elements and a safety-rated feedback mechanism (FluxLink™) into a single IC with 1700 V PowiGaN. By independently regulating and protecting each output, it eliminates multiple downstream conversion stages.

IMX2353F provides the flexibility of having from one to three regulated output voltages and exclusively operates in DCM SR-ZVS mode featuring ZVS in the primary switch. This feature is of great benefit for high-voltage applications in the 800 VDC to 1000 VDC input range to reduce parasitic capacitive discharge losses during turn-on and overall thermals.

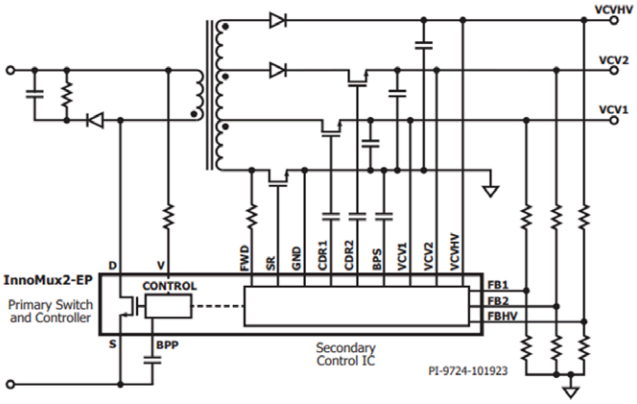

Fig. 12 Typical application of IMX2353F

Fig. 13 shows waveforms and thermal with a 60 W reference design using IMX2353F with 1000 V input. Because of 1700 V PowiGaN and unique SR-ZVS control, the temperature rise is only 22.3 °C at 1000 V input and full power. It helps to achieve a small size and low-temperature auxiliary power supply for an HVDC AI data center; this device is especially ideal for a trending 48 V fan implementation in the 800 VDC PSU while 12 V system output is also needed.

Fig. 13 60 W reference design with IMX2353F and 1000 V input

Conclusions

With Power Integrations' proprietary PowiGaN technology, high-reliability GaN HEMTs with voltage ratings beyond 1200 V can be achieved. These industry-first 1250 V GaN switches can enable designers to build high-density, high-efficiency power supplies for the NVIDIA 800 VDC AI data center architecture, with significant improvement in performance compared to solutions using 1200 V SiC or a stacked topology using 650 V GaN.

Going forward, the trend in HVDC systems is moving toward voltages beyond 800 VDC, driven by the increasing power demand per rack in modern data centers. This shift opens new opportunities for high-reliability 1700 V PowiGaN devices in the main power stage, where its lower on-state resistance can deliver higher efficiency and power density. The future is arriving faster than ever.

Further Reading List

K. Varadarajan et al. " Reliability Qualification of 1250 V Lateral GaN HEMTs for High Reliability Industrial Applications," IEEE International Reliability Physics Symposium proceeding, 3A2.1-3A2.6 (2025)

K. Varadarajan et al. "Reaching Beyond 1200 V: Lateral GaN HEMTs for High-Reliability EV and Industrial Applications" PCIM Europe proceeding, 1593-1598 (2024)

K. Murukesan et al. "State of the Art 1.7kV Lateral GaN HEMTs, an Alternative to SiC", IEEE Applied Power Electronics Conference proceeding, 180-184 (2025)

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