Prime(PACK) Time for SCALE-2

New Plug & Play driver for PrimePACK modules plus a look into planar transformer gate drivers.

Two distinctively different gate driver solutions are presented that both have one mission: to make power designer's life a little less complicated. Each driver relies on the highly integrated SCALE-2 chipset for fast and dependable signal transmission. The PrimePACK driver family offers easy to use control for today's power electronics systems – whereas planar transformer technology might break new ground in the near future.

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Power system designers are more and more under pressure to deliver highly optimized solutions in short design cycles. This situation can be considerably eased by dedicated gate drivers which are already fully customized to the IGBT module in question. CONCEPT's Plug & Play driver series is successfully serving this steadily growing demand since 1999.

Part I: PrimePACK Gate Driver

Now, the Plug & Play series is extended to the rapidly growing 1200V / 1700V PrimePACK family of IGBT half bridge modules. Based on the recently introduced SCALE-2 chip technology [1] the drivers benefit from high integration level, very low delay times of 100ns, and practically instantaneous error feedback in less than 1µs. Figure 1 shows a picture of a 2SD421 PrimePACK driver variant. The schematic of the driver is shown in Figure 2.

All PrimePACK drivers feature up to 4W output power per channel, 20A maximum gate drive current, 3.3V to 15V compatible interface logic, and unlimited duty cycle range from 0% to 100%. The IGBT is turned on with regulated +15V supply. An unregulated -10V rail is employed in the turn-off path. Advanced active clamping aids performance optimization of the IGBT module. Both direct mode and a module-specific half bridge mode with automatic cross current interlock are supported – and last but surely not least, great emphasis has been placed on highly reproducible signal transmission with a measured delay time jitter of less than +/-2ns.

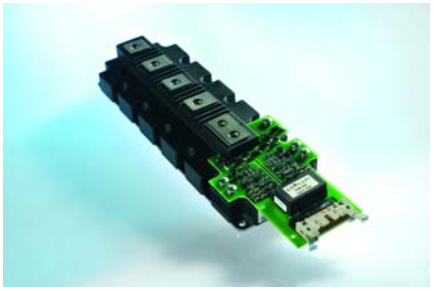

Figure 1 2SD421 PrimePACK Plug & Play driver mounted onto the module (Number and type of the gate resistors are being adjusted to output power and peak current.)

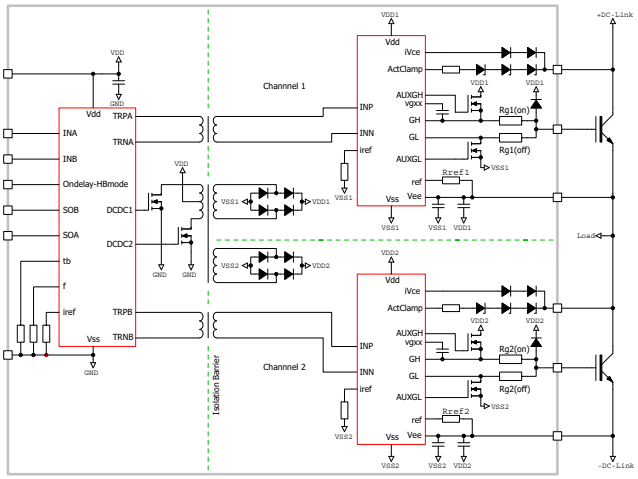

Figure 2 Schematic of the 2SD421 half bridge driver for PrimePACK modules

Custom-Specific Design Options

A great variety of design options can be implemented for future modules and special customer requests. Fiber optic interfaces serve physically large systems. The placement of the transformer block at the rear side of the PCB allows for the power terminals to be tapped across the driver PCB. Secondary side error input and dv/dt control make the SCALE-2 driver even more flexible with respect to innovative system design.

Part II: Planar Integration

There is tremendous potential for increased power density and manufacturing automation when planar transformers are adopted. Here the transformer windings are merged into the driver PCB (printed circuit board) as shown in Figure 3. The planar concept has already demonstrated its superiority in low voltage designs such as POL (point of load) regulators and other non-isolated switching converters.

However, great care needs to be taken to ensure safety and long time reliability of the HV insulation inside the PCB. Especially the behaviour of the board material under applied HV bias and environmental stress has to be considered. In the following section, we discuss the current development status of a 1.7kV SCALE-2 gate driver using planar transformers.

HV Board Reliability

FR4 board substrate is a composite material that quite naturally lends itself to HV insulation. It consists of woven glass fiber strands embedded in an epoxy resin matrix. Freshly cured FR4 sustains as high as 40kV/mm dielectric stress. So one could wonder why it isn't widely used for HV insulation. But like so many times, the devil is in the details – to be more precise: in the aging behavior of the

insulation characteristics.

There are mainly two effects which threaten the HV planar concept. The first one is the degradation of dielectric strength due to temperature cycles, corrosive agents and mechanical fatigue. This situation is common to all solid insulation materials. It can be controlled by applying generous derating of the maximum sustainable dielectric stress. We used derating margins well above a factor of ten. Under these conditions the planar HV transformer shows slower degradation than a conventional wire-wound ring core transformer. Our test criterion is the shift of the partial discharge extinction voltage versus temperature cycles for a group of planar transformers and a reference group of conventional resin-molded ring core transformers. This method allows repeated non-destructive testing and is considered the gold standard for insulation testing. Figure 4 shows the test results. The stability of the planar FR4 insulation is even more notable as the reference group consisted of series production components with a proven application life time of more than 15 years.

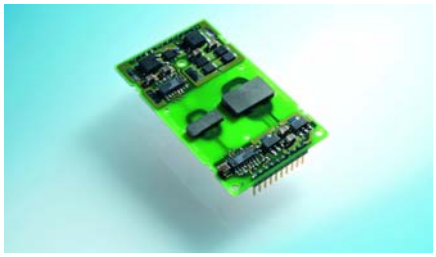

Figure 3 Planar transformer 1.7kV gate driver delivering 22W output power at 44 x 74 mm², delay time 100ns, switching frequency DC to 250kHz (all data valid for unforced convection)

Conductive Anodic Filaments

The other degradation mechanism is specific to fiber reinforced insulation materials such as FR4. It leads to the growth of conductive anodic filaments (CAF) between HV traces. CAF is a known phenomenon since its first detailed analysis in the mid 1970's, yet the exact growth mechanism and its kinetics are still not fully clear today.

A conductive filament progresses along glass fibers where the bond between glass and epoxy resin has been weakened. This can happen because of thermal cycling stress, mechanical stress such as hole drilling and board flexing, and it is strongly advanced by high levels of humidity. Below a certain relative humidity threshold ranging from 50% to 75% [2] [3], there is no CAF growth at all. Above this threshold, hydrolysis of the glass fiber surface creates a path

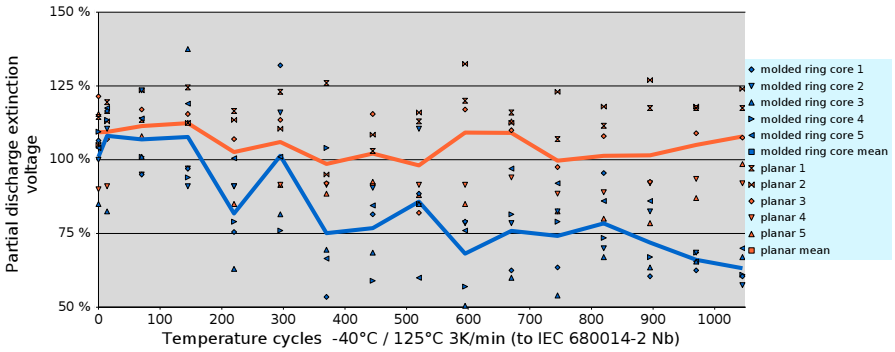

Figure 4 Accelerated ageing behavior of planar and wire-wound transformers

for the electrochemical reaction that forms CAF. Copper is dissolved at the anode and transported towards the cathode in the form of an aqueous solution of copper salts. These copper salts are deposited along the glass fiber in a complex equilibrium reaction involving the electric field, capillary and diffusion forces, pH value, and reactants from the PCB material [4] [5] [6]. Fig. 5 shows an illustration of CAF growth between two HV traces.

Until now, CAF has mostly been studied with emphasis on highly integrated PCBs for telecommunication installations or server backplanes. For HV insulation, however, the focus needs to be shifted from small to wide insulation barriers and form voltages in the tens of volts to more than one kilovolt.

We have therefore conducted CAF testing under 1500V DC bias in highly accelerating climate of 85°C and 85% relative humidity (rH). In the first design-of-experiment test, we used standard FR4 and standard layer buildup to ascertain the CAF severity for conventional PCBs. Fig. 6 shows examples of lateral CAF in the xy direction on the PCB. The filaments grew to more than 7mm in the test and eventually they short-circuited the supply traces. Consequently the test had to be stopped after 730h. Vertical CAF between stacked power planes has also been observed. A standard layer buildup failed after as short as 80h. Its improved counterpart using several insulation layers withstand the whole test and did not fail until the final 730h. The improvement factor between standard layer buildup and improved HV buildup is thus 9 times or larger.

For the second test step, we used halogen free, low CTE (coefficient of thermal expansion) FR4 material to determine the improvement factor between standard FR4 and up-to-date high performance FR4. The results are shown in Figure 7 in the form of a Weibull net. Two groups of eight samples each were tested in parallel. One group (A)

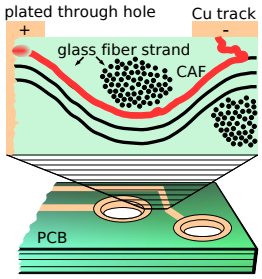

Figure 5 Formation of conductive filaments in FR4 material (schematic)

has been processed with a minimum thermal budget (optimization, no rework) and the other group (B) has undergone two additional SMD reflow cycles. It can be seen that both the characteristic lifetime and the Weibull slope parameter are influenced by the thermal budget. Group B shows a slope parameter of 2.6. The characteristic lifetime is 590 hours. The relatively low slope parameter is an indication of thermally induced failure spots in the PCB material when compared to group A's slope of 6.2. The steeper slope indicates a more pronounced wear-out behavior which is typical for a degradation process that needs a certain time span to become effective.

Two dashed curves A* and B* are shown in Figure 7. They correspond to the results of the CAF test groups A and B, combined with the previously determined improvement factors for optimized layer buildup. The area between these curves A* and B* marks the expected failure range for the finally optimized design of the HV insulation layer. No failure data is presently available for the final design. The CAF test is continued and the first failure can be expected between 2000 hours and 8000 hours. We are currently evaluating further controlled acceleration of the tests by higher voltages up to 3000V.

The question still remains how many hours of real-life application correspond to 1000h of accelerated CAF testing. A large variety of different testing schemes are used through-

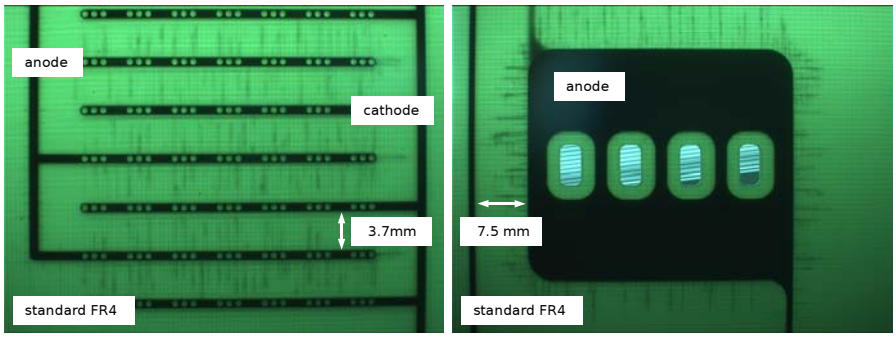

Figure 6 Standard FR4 PCB after 730h CAF testing at 1500V, 85°C and 85% rH

out the industry to assure CAF resistance in the field.

- Many OEMs adopt the CAF test developed by Sun Microsystems which incorporates 500h testing at 85°C / 85% rH [7] [10].
- EIA/JEDEC standard A101-B specifies testing at 85°C / 85% rH for 1000h.
- The widely used test to Telcordia (ex Bell-CORE) GR-78-CORE dictates 65°C, 85% rH (min.) for 500h.
- UL standard 796, section 23 (cited after [8]), requires 1344 hours testing at 35°C and 87.5% rH.
- IPC-TM-650 states a dedicated CAF test in section 2.6.25. The environmental conditions of 85°C and 87% rH are applied for 500 or 1000 hours.

New data is to be expected from the iNEMI halogen-free project which is still under investigation [9]. So far the most comprehensive treatment of CAF lifetime mapping has been published by IPC in the user guide to the test standard IPC-TM-650 2.6.25 [11]. This document is the most accepted basis for CAF lifetime testing in the electronics industry. It states that a component which is tested to IPC-TM-650 2.6.25 (85°C, 87% rH) over 1000 hours should yield less than 20% failures in the CAF test to achieve 20 years life with 95% of the devices. ·

From our own field data we know that lateral CAF such as shown in Figure 6 (730h CAF test) does not occur in real life applications after more than 15 years. Judging from all this data, our 1000h, 85°C, 85% rH CAF test at 1500V DC bias is a very harsh qualification criterion.

The expected Weibull curves A* and B* in Figure 7 for the final design run significantly lower than IPC's 20% criterion at 1000h test time. The estimated intersection with the 1000h time step is lower than 1.3% for the newly developed planar HV transformer. This would translate into roughly 0.4% failures after 20 years. These results are very promising for a new generation of high-performance gate drivers combining the versatile SCALE-2 chipset and the novel planar HV insulation platform. Actual CAF test data for the final design must now prove the estimated behavior based on current CAF test results. Because of the very high target reliability level, the final CAF test must be performed over more than 3000 hours to account for the confidence intervals of the Weibull fit. It is important to note that not just single parameters, such as material and layer buildup influence CAF resistance – the whole process chain from board material to component placement and soldering has to be optimized and controlled.

Summary

Two very distinct gate drive solutions have been presented. Both use the highly integrated SCALE-2 chipset, yet the embodiments of the HV insulation are fundamentally different.

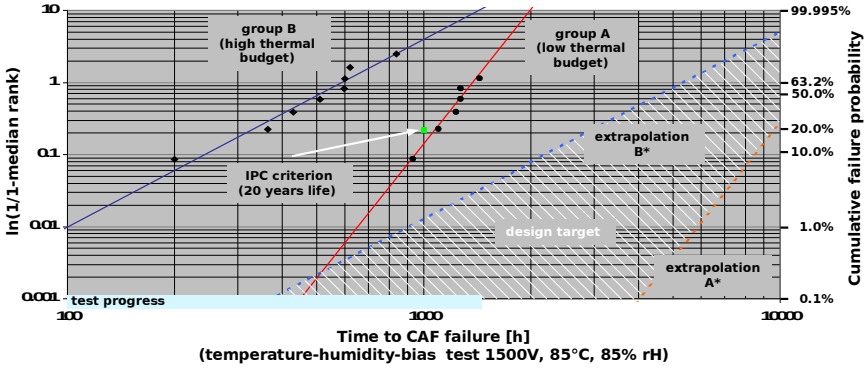

Figure 7 Weibull plot of CAF test data after 1450h

Planar integration of the HV insulation into the driver PCB is an extremely promising approach. The novel reliability-focused planar design has yielded vastly improved CAF resistance. This opens the door for planar insulation in the 1700V class and beyond. In contrast, the PrimePACK driver presented here uses tried and tested ring core transformers. It fills the need for a dedicated gate driver tailored to the successful PrimePACK IGBT module series. As a member of CONCEPT's Plug & Play driver family the driver is ready to operate out-of-the-box, with no development effort necessary at the customer side.

www.IGBT-Driver.com

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