標題	***採用 InnoSwitch™-CH INN2023K 的 10 W CV/CC USB 充電器的參考設計報告***
規格	85 VAC – 264 VAC 輸入； 5 V，2 A 輸出 (USB 纜線末端)
應用	行動電話/USB 充電器
作者	應用工程部門
文件編號	RDR-420
日期	2014 年 11 月 11 日
修訂	1.0

摘要與功能

- InnoSwitch-CH - 業界首創 AC/DC IC，具有隔離、安全額定的整合回授
- 擁有二次側控制及簡單一次側調節的所有優點
  - ±3% 定電壓、±5% 定電流調節
  - 適用於各種變壓器
  - 暫態反應不受負載時間的影響
  - 輸出電容器尺寸更小、成本更低
  - 無負載輸入功率低於 10 mW
  - 纜線壓降補償
- 內建可提高效率的同步整流

專利資訊
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目錄

重要事項：
雖然此電路板的設計符合安全隔離要求，但工程原型尚未取得相關機構之認證。因此，執行所有測試應使用隔離變壓器才能提供 AC 輸入給原型板。

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1 簡介

本工程報告文件說明採用 InnoSwitch-CH IC 系列裝置的 2 A、5.0 V USB 充電器。本設計旨在展示藉由高度整合，同時提供一貫卓越效能，兼顧高功率密度與效率的可行性。

本文件內容涵蓋電源供應器的規格、電路圖、物料表、變壓器文件、印刷電路板佈局和效能資料。

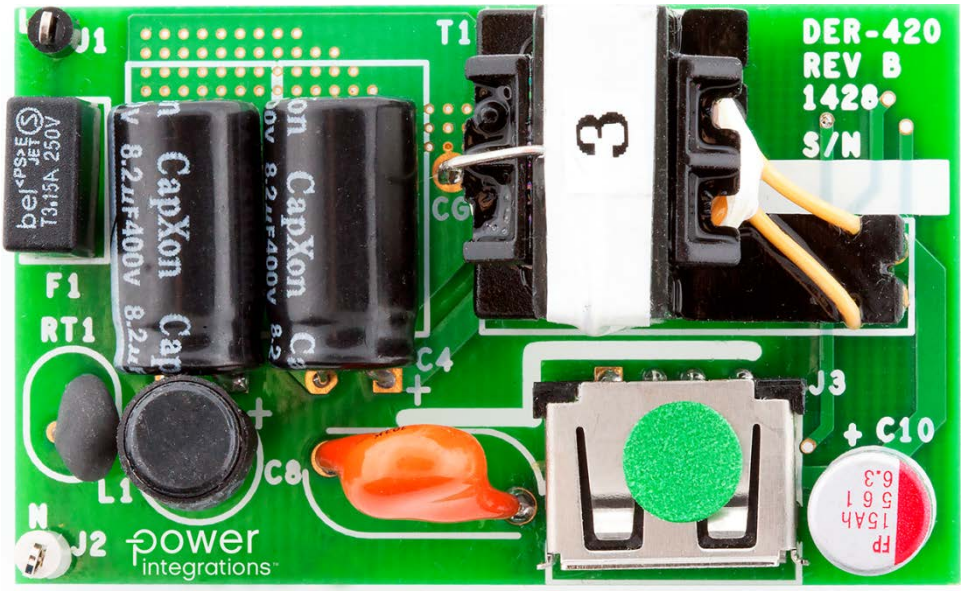

Figure 1 – Populated Circuit Board Photograph, Top.

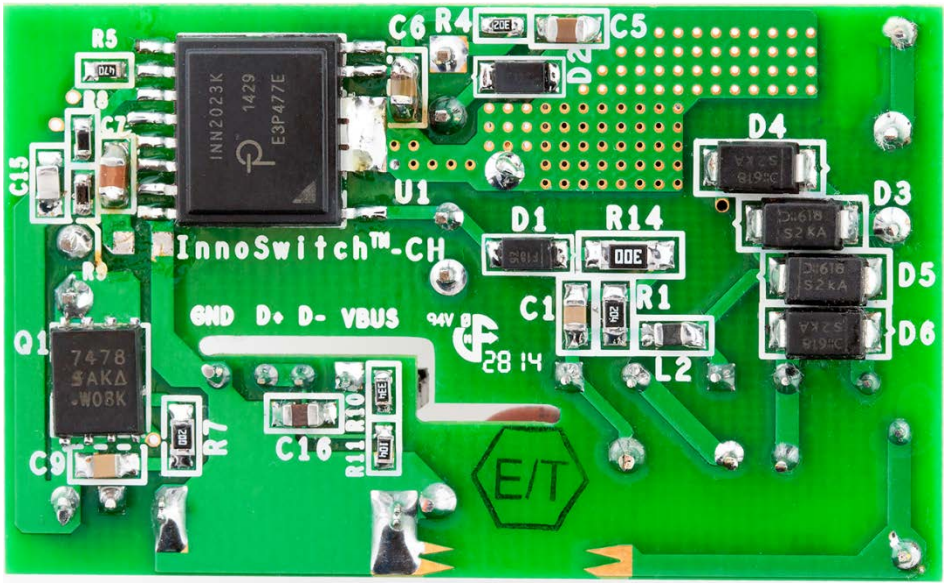

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 電源供應器規格

下表列出此設計可接受的最低效能。實際效能列在結果部分。

說明	符號	最小值	典型值	最大值	單位	註解
輸入						
電壓	V_{IN}	85		265	VAC	雙線 – 無 P.E.
頻率	f_{LINE}	50	50/60	64	Hz	
無負載輸入功率				10	mW	230 VAC
輸出						
輸出電壓	V_{OUT}	4.75	5.0	5.25	V	0.35 V 纜線電阻壓降
暫態輸出電壓	$V_{OUT(T)}$	4.2		5.5	V	0 A - 2 A - 0 A 負載步階，纜線末端位於輸出纜線末端
輸出漣波電壓	V_{RIPPLE}			150	mV	位於輸出纜線末端
輸出纜線補償	V_{CBL}	250	300	350	mV	於 2 A 輸出電流時
輸出電流 CC 點	I_{OUT}	2		2.5	A	
自動重新啟動電壓	V_{AR}	2		3.5	V	於纜線末端
開啟上升時間	t_R			20	ms	
額定輸出功率	P_{OUT}		10		W	
效率						
平均	$\eta_{AVE[BRD]}$	84			%	於 USB 插槽測量
25%、50%、75% 和 100%	$\eta_{AVE[CBL]}$	80			%	含 0.38 V 纜線電阻壓降
10%	$\eta_{10\%}$	79			%	
環境						
輸出纜線阻抗	R_{CBL}		190		mΩ	
傳導性 EMI		CISPR22B / EN55022B 浮接負載或透過人工手動接地				電阻負載，6 dB 餘裕
		連接到行動電話和電視 (已啟用 MHL 連線)				6 dB 餘裕
安全		IEC950/UL1950 第 II 級				設計本身符合
噪音				25	dB	於 3 公分處測量
線間突波 共模 (L1/L2-PE)				6	kV	振盪波，共模： 12 Ω
ESD		±16.5 ±8			kV kV	接觸 空氣放電 效能不會降低
環境溫度	T_{AMB}	0		40	°C	自然對流，海平面，密封的外殼內

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3 電路圖

		VAC			
		85	115	230	265
Efficiency at PCB (%)	Average		84.2	84.2	
	Full Load	82.6	84.2	85.1	84.8
	10% Load	78.3	78.9	78.6	78.7
No-Load Input	(mW)	7	7	8	9

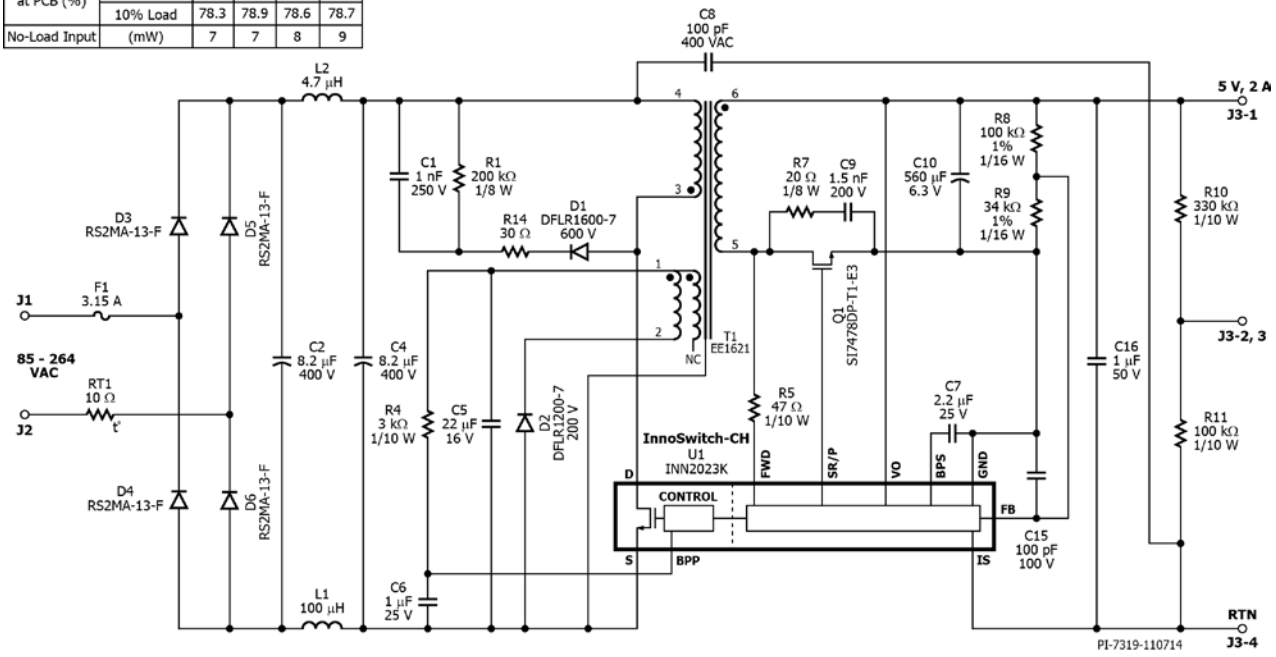

Figure 3 – Schematic.

4 電路說明

4.1 *輸入 EMI 濾波*

保險絲 F1 可防止一次側上的元件發生嚴重故障。

由於整流器二極體 (D1-D4) 的突波電流額定值低，因此需要浪湧限制熱敏電阻器 (RT1)，而極高的值會降低大電容器 C2 和 C4 的阻抗。

選用尺寸小的二極體 D1-D4 是因為空間有限，特別是 PCB 到外殼之間的高度。

電容器 C2 和 C4 提供整流 AC 輸入的濾波，並與 L1 和 L2 共同構成 π (pi) 濾波器來削減差模傳導性 EMI。值低的 Y 電容器 (C8) 可降低共模 EMI。

4.1 *InnoSwitch-CH IC 一次側*

變壓器一次側的一側連接到整流 DC 匯流排，另一側則連接到 InnoSwitch-CH IC (U1) 內的整合式 650 V 功率 MOSFET。

低成本 RCD 箝位電路是由 D1、R1、R14 和 C1 構成，可限制因為變壓器和輸出 Trace 電感的效應而產生的峰值汲極電壓。

此 IC 可自我啟動，採用內部高電壓電流源，在最初施加 AC 時為 BPP 接腳電容器 (C6) 充電。在正常運作期間，一次側區塊將由變壓器上的輔助繞組供電。此變壓器的輸出配置為返馳式繞組，透過限電流電阻器 R4 進行整流、濾波 (D2 和 C5) 及饋送到 BPP 接腳。

輸出調節是利用開/關控制來達成的，啟用的切換週期的數目會根據輸出負載來進行調整。在高負載時，會啟用大多數切換週期，而在輕負載或無負載時，大多數週期會停用或跳離。一旦啟用某個切換週期，功率 MOSFET 就會保持在開啟狀態，直到一次側電流降低至特定工作狀態的裝置限電流。一共有四種工作狀態 (限電流) 佈置，使一次側電流切換模式的含頻量維持在可聞範圍外，直到變壓器磁通密度處於輕負載，讓產生的噪音處於極低等級。

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4.2 *InnoSwitch-CH IC 二次側*

InnoSwitch-CH 的二次側提供輸出電壓、輸出電流感測，並驅動 MOSFET 提供同步整流。

變壓器二次側由 Q1 進行整流，由 C10 進行濾波。切換暫態期間會產生高頻率振盪，而且會在 Q1 上建立高電壓，並透過突波吸收器元件 R7 和 C9 降低輻射 EMI。

Q1 提供同步整流 (SR) 以降低功率消耗。Q1 的閘極會根據 IC 的 R5 和 FWD 接腳感測的繞組電壓而開啟。在連續導通模式操作下，功率 MOSFET 會在二次側控制一次側的新切換週期前關閉。在不連續模式下，MOSFET 會在 MOSFET 上的壓降降至低於臨界值時關閉。二次側控制著一次側 MOSFET，以確保其永遠不會與同步整流 MOSFET 同時開啟。MOSFET 驅動訊號是由 SR/P 接腳輸出。

此 IC 的二次側是由二次側繞組順向電壓或輸出電壓自我供電。在 CV 工作模式下，輸入電壓會饋送至 VO 接腳來為裝置供電。

在 CC 操作模式期間，當輸出電壓下降時，裝置會直接從二次側繞組自我供電。在一次側 MOSFET 開啟期間，二次側繞組上的順向電壓會用於透過 R5 和內部調節器為去耦合電容器 C7 充電。當感測到的輸出電壓低於 3 V 時，裝置會進入自動重新啟動模式。

輸出電流是在 IS 和 GND 接腳之間進行內部感測，臨界值為 35 mV，以將損失降至最低。一旦超過內部電流感測臨界值，裝置會調整啟用的切換週期的數目，以維持固定輸出電流。

低於 CC 臨界值時，裝置會在定電壓模式下運作。輸出電壓是透過分壓電阻器 R8 和 R9 感測，以 FB 接腳上的 1.265 V 參考電壓工作 (當處於調節輸出電壓時)。

5 PCB 佈局

PCB 銅箔厚度為 2 盎司 (2.8 密爾/70 µm，除非另有指定)

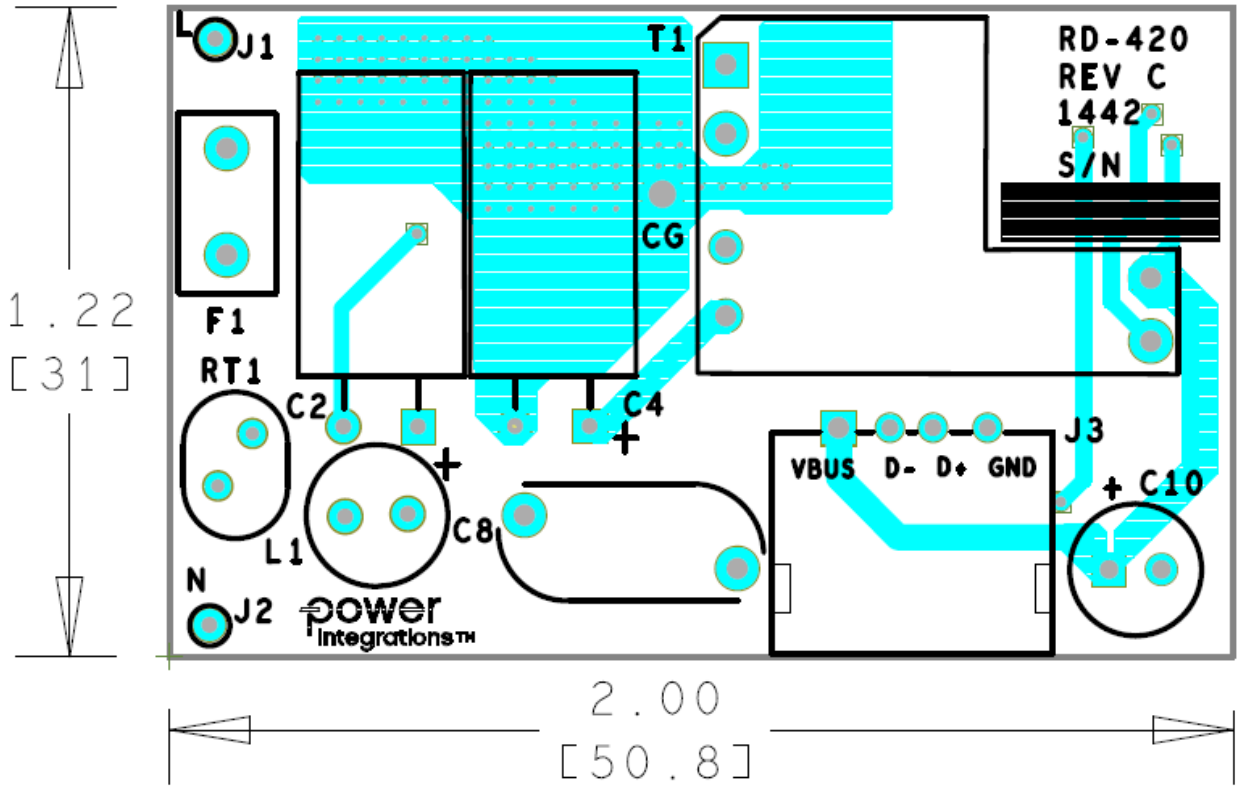

Figure 4 – Printed Circuit Layout, Top.

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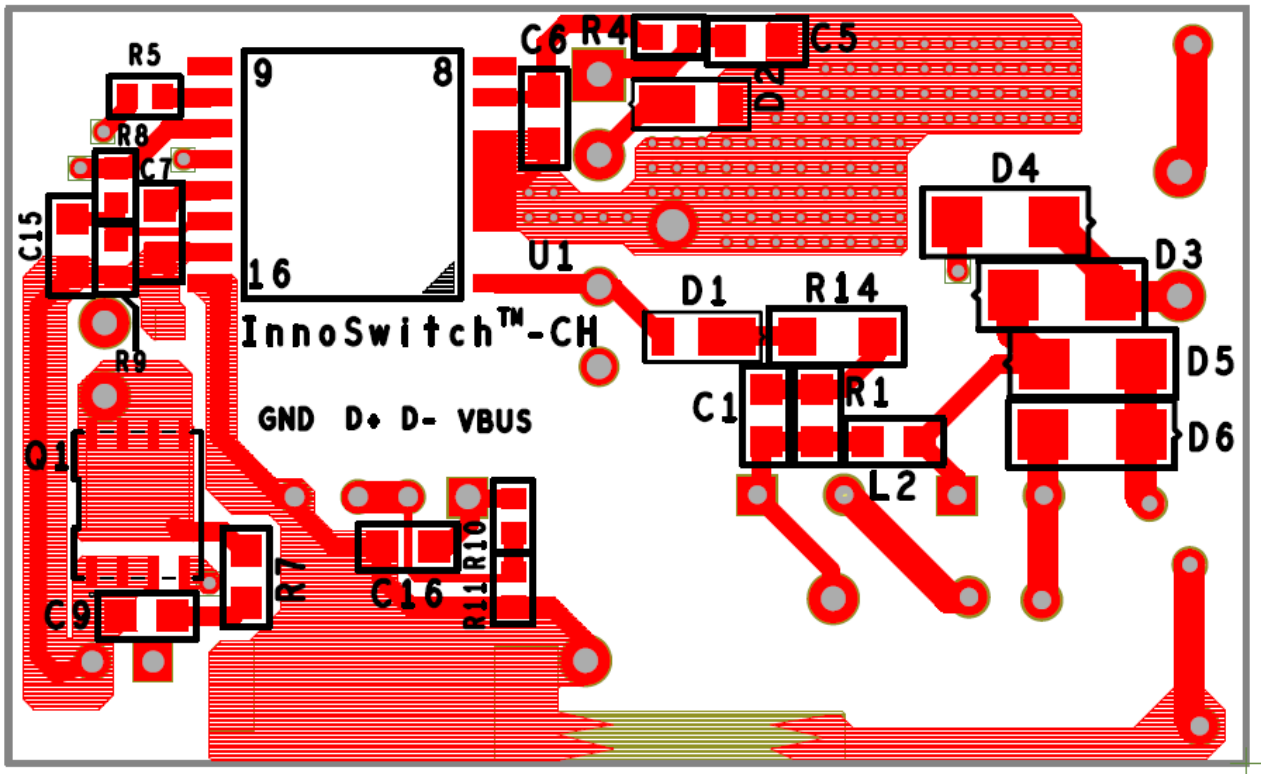

Figure 5 – Printed Circuit Layout, Bottom.

6 物料清單

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
2	2	C2 C4	8.2 μF, 400 V, Electrolytic, (8 x 14) 8.2 μF, 400 V, Electrolytic, (8 x 14), Alternate part	 400AX8.2M8X16	Capxon Rubycon
3	1	C5	22 μF, 16 V, Ceramic, X5R, 0805	C2012X5R1C226K	TDK
4	1	C6	1 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
5	1	C7	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
6	1	C8	100 pF, Ceramic, Y1	440LT10-R	Vishay
7	1	C9	1.5 nF, 200 V, 10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
8	1	C10	560 μF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
9	1	C15	100 pF 100 V 10 % X7R 0805	08051C101JAT2A	AVX
10	1	C16	1 μF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
11	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
12	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
13	4	D3 D4 D5 D6	800 V, 1.5 A, Gen Purpose, SMA 800 V, 1.5 A, Gen Purpose, SMA, Alternate part	S2KA-13-F RS2MA-13-F	Diodes, Inc. Diodes, Inc.
14	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
15	1	J1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
16	1	J2	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
17	1	J3	Connector USB Female Type A	USB-AF-DIP-094-H	GOLDCONN
18	1	L1	100 μH, 0.490 A, 20%	RL-5480-2-100	Renco
19	1	L2	4.7 μH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
20	1	Q1	60 V, 15 A, N-Channel, PowerPAK SO-8	SI7478DP-T1-E3	Vishay
21	1	R1	200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
22	1	R4	3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
23	1	R5	47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
24	1	R7	20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
25	1	R8	100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
26	1	R9	34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
27	1	R10	330 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ334V	Panasonic
28	1	R11	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
29	1	R14	30 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ300V	Panasonic
30	1	RT1	NTC Thermistor, 10 Ohms, 0.7 A	MF72-010D5	Cantherm
31	1	T1	Custom (see transformer section for material set)	SNX-R1776	Santronics
32	1	U1	InnoSwitch-CH IC eSOP-R16B	INN2023K	Power Integrations

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7 變壓器規格

7.1 *電氣圖*

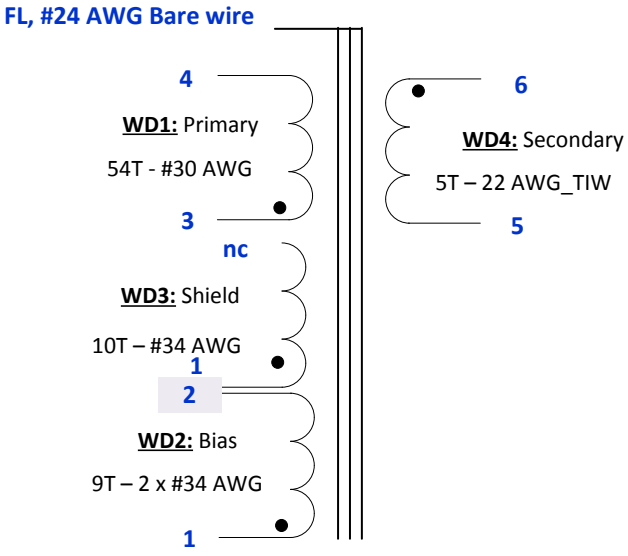

Figure 6 – Transformer Electrical Diagram.

7.2 *電氣規格*

Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	546 µH ±5%
Resonant Frequency	Pins 3-4, all other windings open.	1500 kHz (min)
Primary Leakage Inductance	Pins 3-4, with pins 5-6 shorted, measured at 100 kHz, 0.4 V_{RMS}.	25 µH (max)

7.3 *材料*

Item	Description
[1]	Core: EE1621; PC-40 or equivalent.
[2]	Bobbin: EE1621-Vertical – 8 pins (4/4) Shen Zhen Xin Yu Jia Technology Ltd.
[3]	Magnet Wire: #30 AWG, double coated.
[4]	Magnet Wire: #34 AWG, double coated.
[5]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mil thick, 5.5 mm wide.
[7]	Epoxy: Devcon, 5 Minute Epoxy, No. 14210; or equivalent.
[8]	Bus wire: #24 AWG, Belden Electronics Div; or equivalent.
[9]	Varnish: Dolph BC-359.

7.4 *變壓器建構圖*

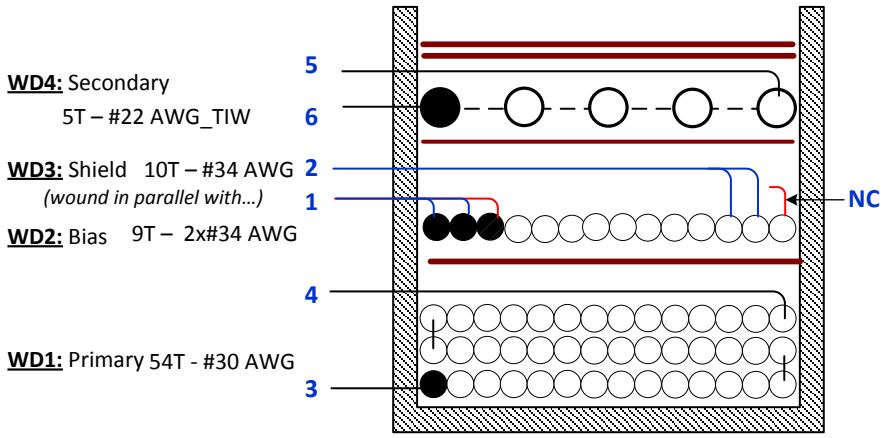

Figure 7 – Transformer Build Diagram.

7.5 *變壓器指示*

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4.
Insulation	1 layer of tape [6] for insulation.
WD2 & WD3 Bias & Shield	Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3rd wire 1 more turn and left no-connect for WD3.
Insulation	1 layer of tape [6] for insulation.
WD4 Secondary	Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5.
Insulation	2 Layer of tape [6] to secure the windings.
Finish	Gap core halves for 546 µH inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration below). Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9].

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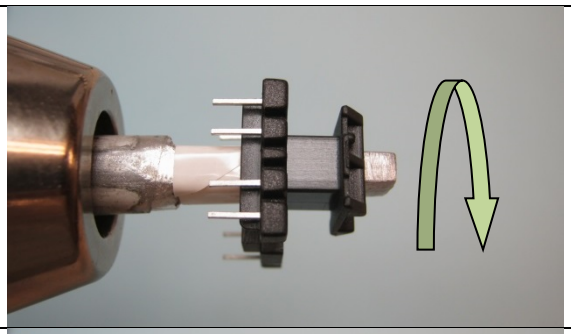
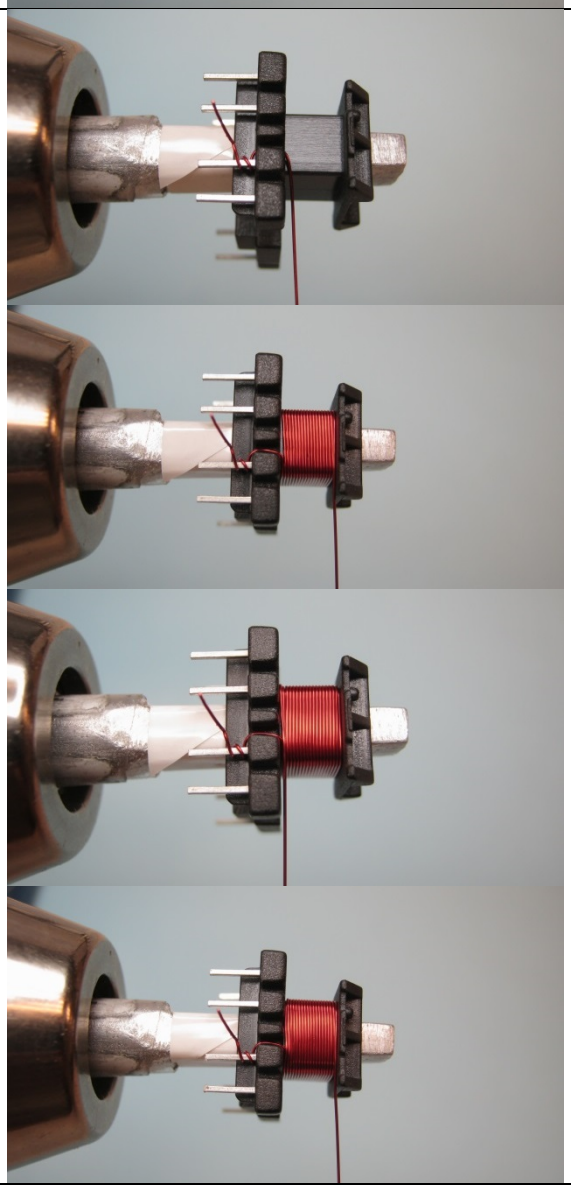
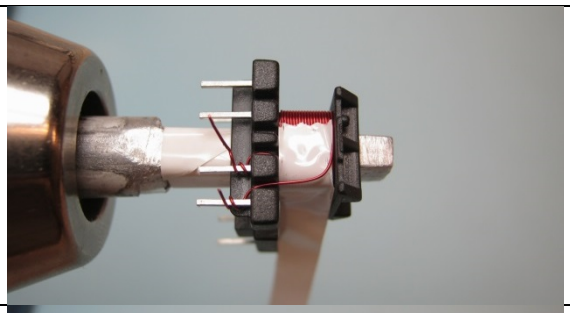
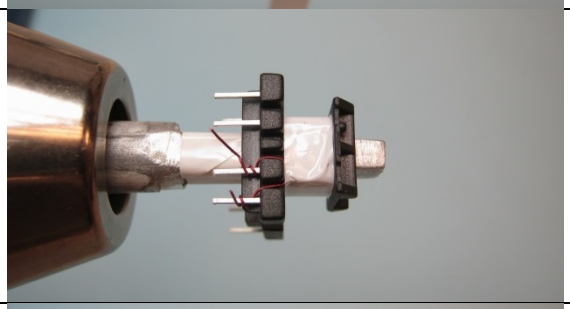
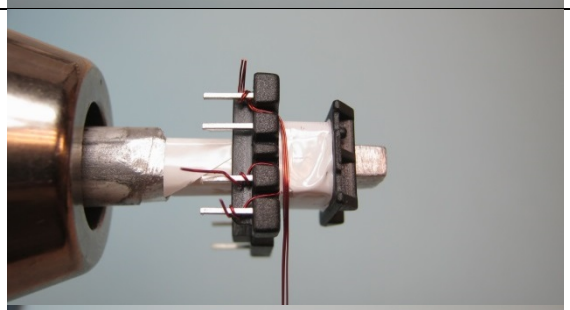
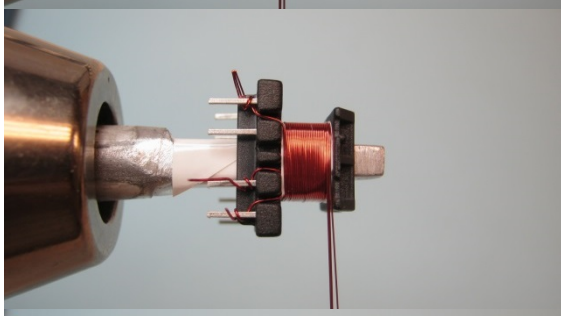
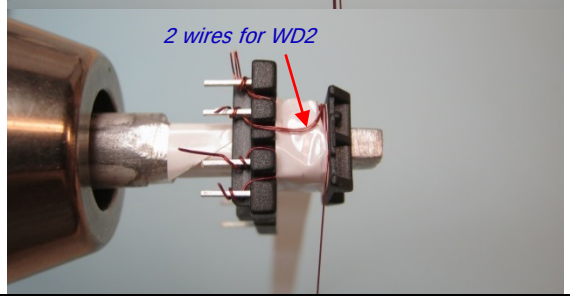
7.6 *變壓器示意圖*

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**		Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4.

		
Insulation		1 layer of tape [6] for insulation.
WD2 & WD3 Bias & Shield	  	Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3rd wire 1 more turn and left no-connect for WD3.

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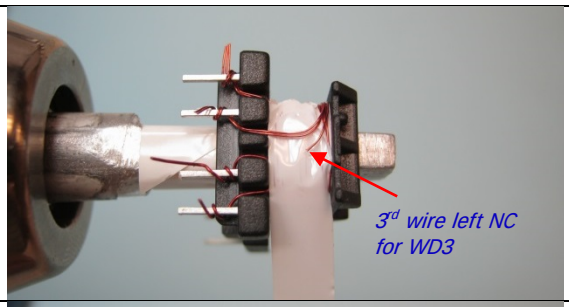
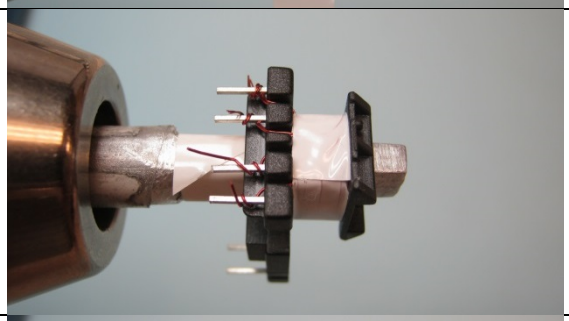
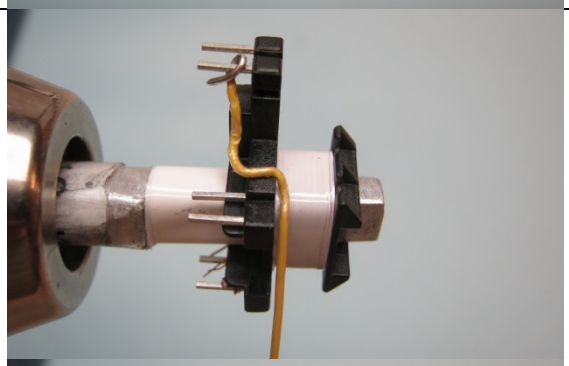
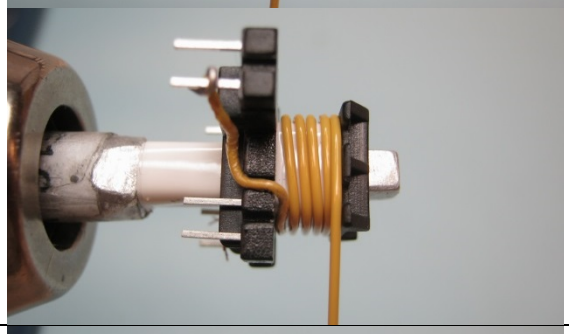
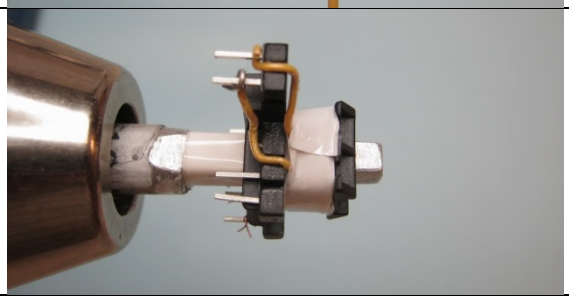
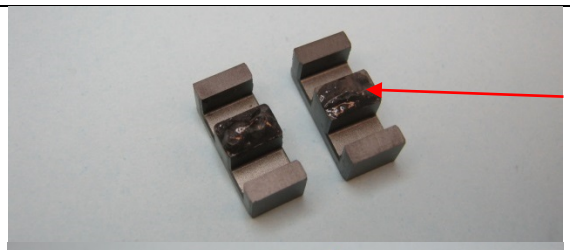
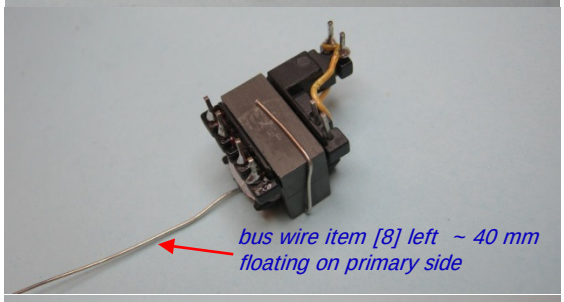
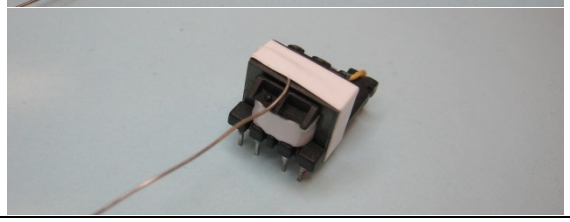
		
Insulation		1 layer of tape [6] for insulation.
WD4 Secondary	 	Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5.
Insulation		2 layer of tape [6] to secure the windings.

Finish	  	Gap core halves for 546 μH inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration beside). Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9].

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8 變壓器設計試算表

ACDC_InnoSwitch-CH_101614; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch_101614_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	5.00		5.00	V	Output Voltage (continuous power at the end of the cable)
IO	2.00		2.00	A	Power Supply Output Current (corresponding to peak power)
Power			10.6	W	Continuous Output Power, including cable drop compensation
n	0.82		0.82		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	16.40	Info	16.40	uFarad	!!! Input capacitor is too small. Recommnded to increase CIN above 19.05 uF to ensure VMIN>70 V
ENTER InnoSwitch VARIABLES					
InnoSwitch-CH	INN20x3		INN20x3		User defined InnoSwitch
Cable drop compensation	6%		6%		Select Cable Drop Compensation option
Complete Part Number			INN2023K		Final part number including package
Chose Configuration	INC		Increased Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.682	A	Minimum Current Limit
ILIMITTYP			0.75	A	Typical Current Limit
ILIMITMAX			0.818	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			47.25	A^2kHz	Worst case I2F parameter across the temperature range
VOR	58		58	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.80		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.46		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			9.32	V	Bias Winding Number of Turns
PIVB			102.59	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	Custom		Custom		Enter Transformer Core
Core	EE1621		EE1621		Enter core part number, if necessary
Bobbin			0		Enter bobbin part number, if necessary
AE	0.325		0.325	cm^2	Core Effective Cross Sectional Area
LE	3.93		3.93	cm	Core Effective Path Length
AL	2800		2800	nH/T^2	Ungapped Core Effective Inductance
BW	5.40		5.40	mm	Bobbin Physical Winding Width

M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3		Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	62	Warning	62	V	!!! Minimum DC Input Voltage < 70 Volts. Increase VACMIN or increase CIN
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.21	A	Average Primary Current
IP			0.682	A	Peak Primary Current assuming ILIMITMIN
IR			0.546	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.31	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			546	uHenry	Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 518 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			54		Primary Winding Number of Turns
ALG			187	nH/T^2	Gapped Core Effective Inductance
BM			2868	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1147	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2694		Relative Permeability of Ungapped Core
LG			0.20	mm	Gap Length (Lg > 0.1 mm)
BWE			16.2	mm	Effective Bobbin Width
OD			0.30	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.25	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			259	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			7.37	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			3.33	A	Secondary RMS Current
IRIPPLE			2.67	A	Output Capacitor RMS Ripple Current
CMS			667	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			517	V	Maximum Drain Voltage Estimate
PIVS			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.30	V	Main Output Voltage directly after output rectifier
IO1			2.00	A	Output DC Current
PO1			10.60	W	Output Power
VD1			0.06	V	Output Synchronous Rectification FET Forward Voltage Drop

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NS1			5.00	Turns	Output Winding Number of Turns
ISRMS1			3.33	A	Output Winding RMS Current
IRIPPLE1			2.67	A	Output Capacitor RMS Ripple Current
PIVS1			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			QM6006		Recommended SR FET for this output
RDSON_HOT			0.027	Ohm	RDSon at 100C
VRATED			60	V	Rated voltage of selected SR FET
CMS1			667	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.08	mm	Maximum Outside Diameter for Triple Insulated Wire

9 效能資料

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

9.1 *主動模式效率 (於 USB 插槽) 與線間對照*

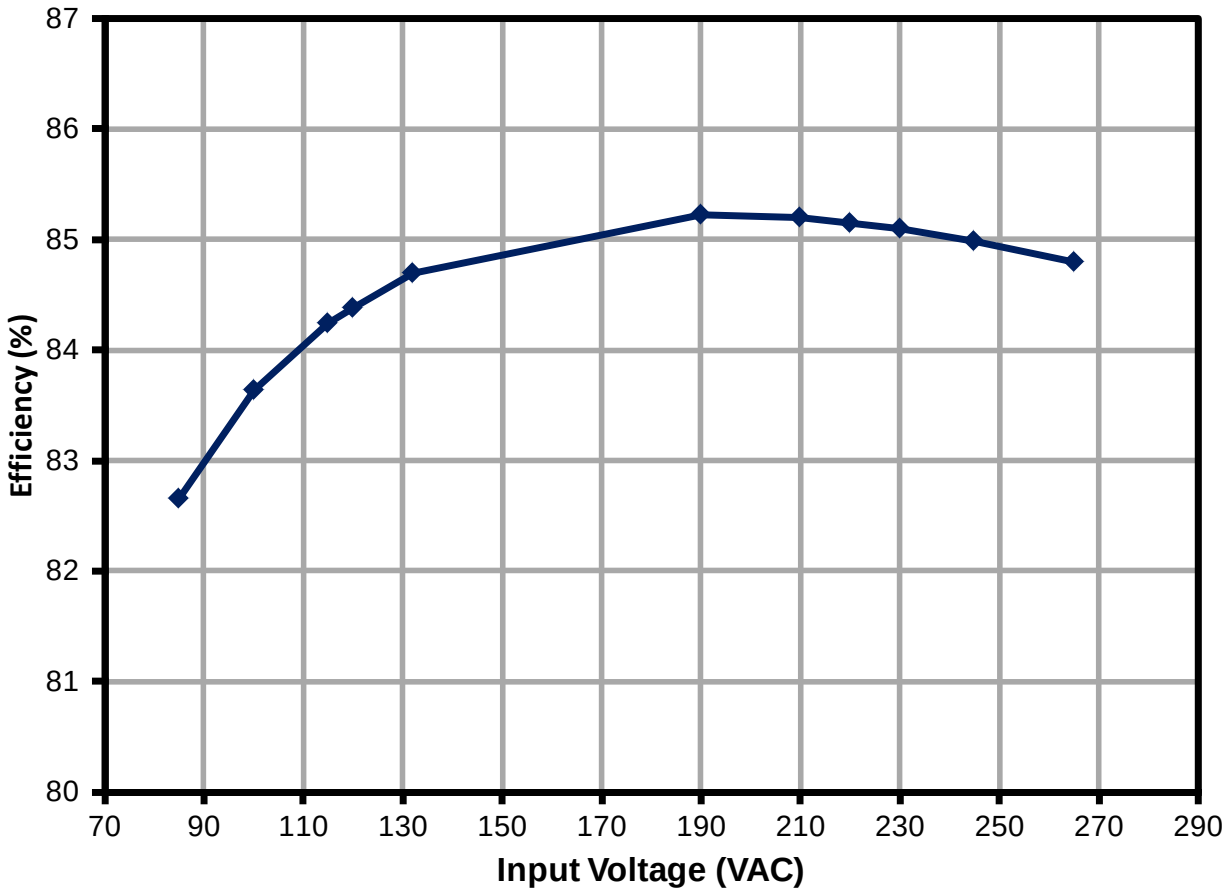

Figure 8 – Efficiency vs Line Voltage, Room Temperature

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9.2 *主動模式效率 (於 USB 插槽) 與負載對照*

9.2.1 蕭特基二極體不與 Q1 並聯的效率，SR FET

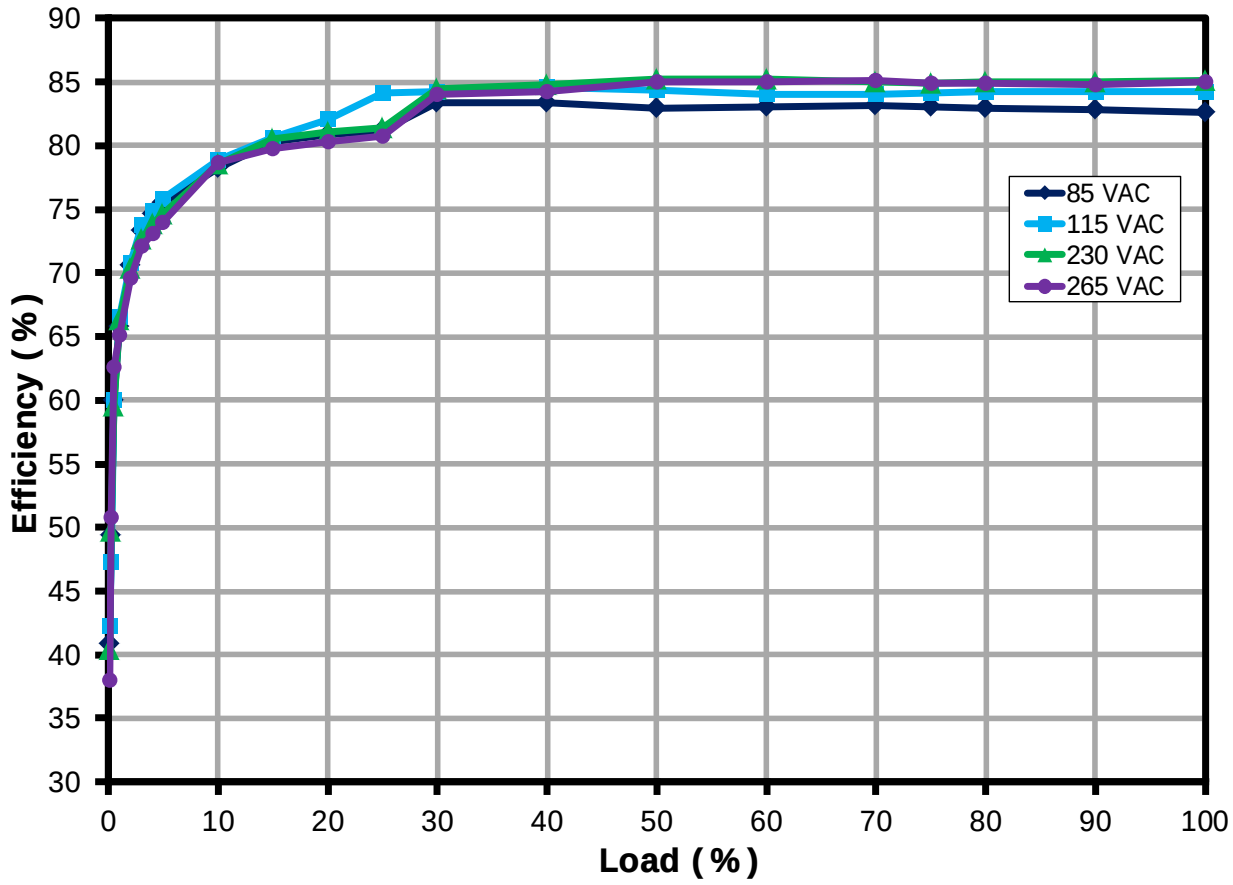

Figure 9 – Efficiency vs Load, Room Ambient

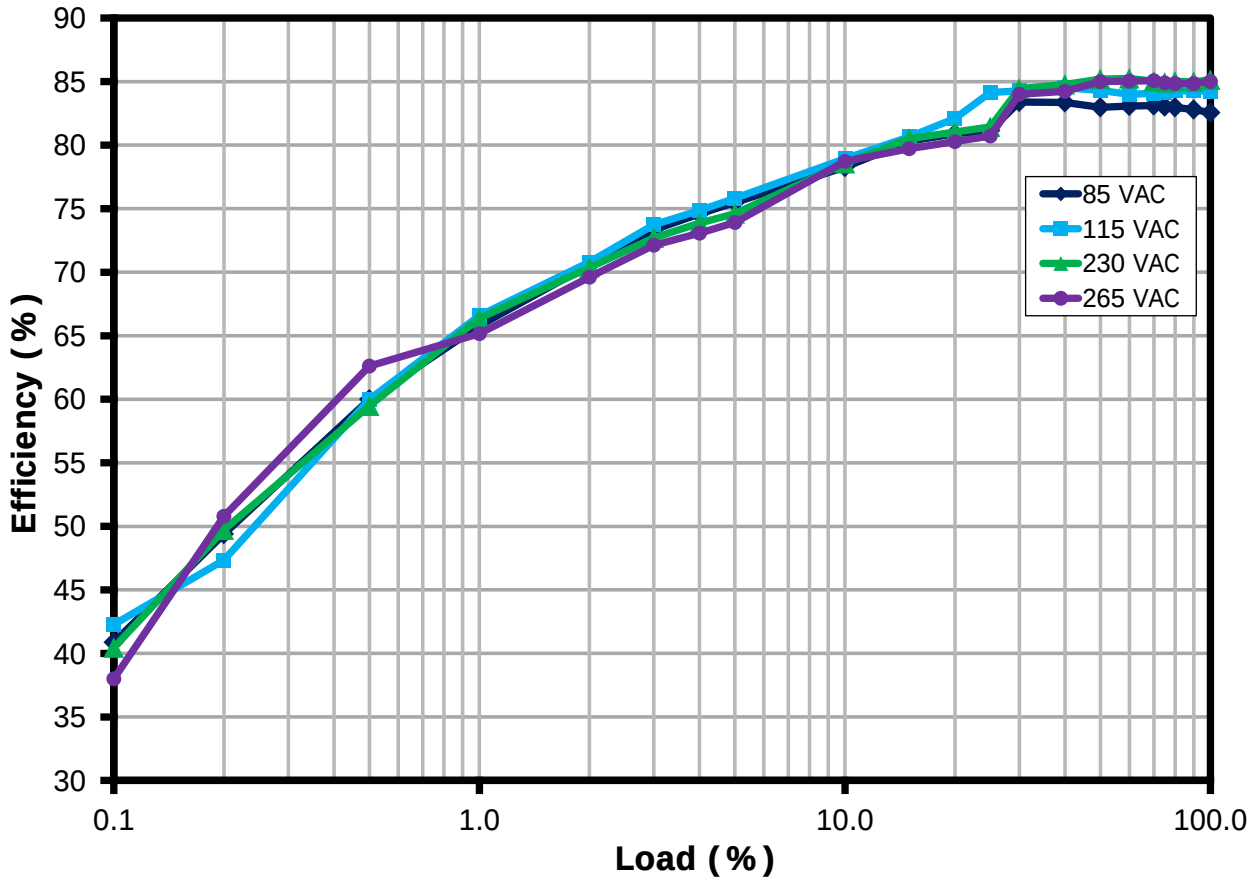

Figure 10 - Efficiency vs Load (log scale to demonstrate light load performance)

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9.2.2 蕭特基二極體 SS16 與 Q1 並聯的效率，SR FET

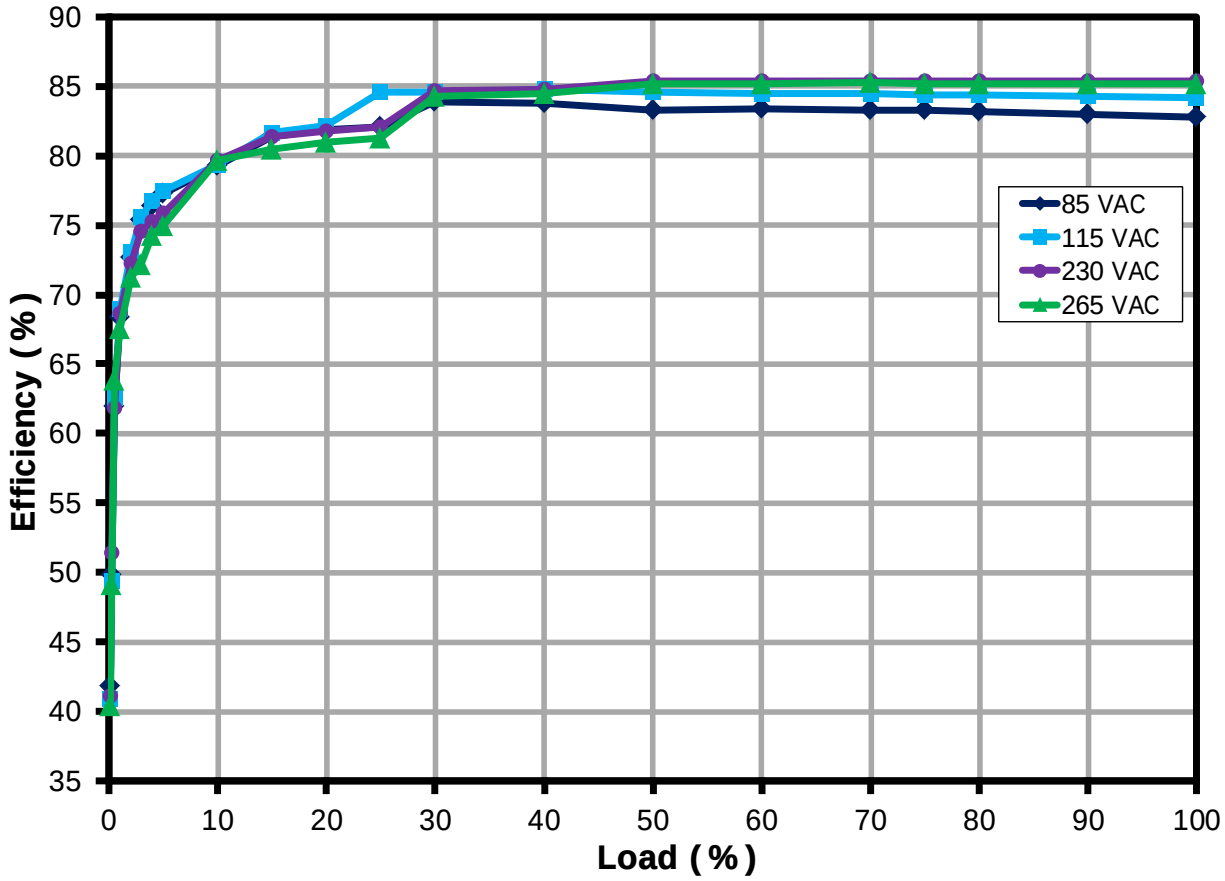

Figure 11 – Efficiency vs Load, Room Temperature, 60 Hz.

9.3 *無負載輸入功率*

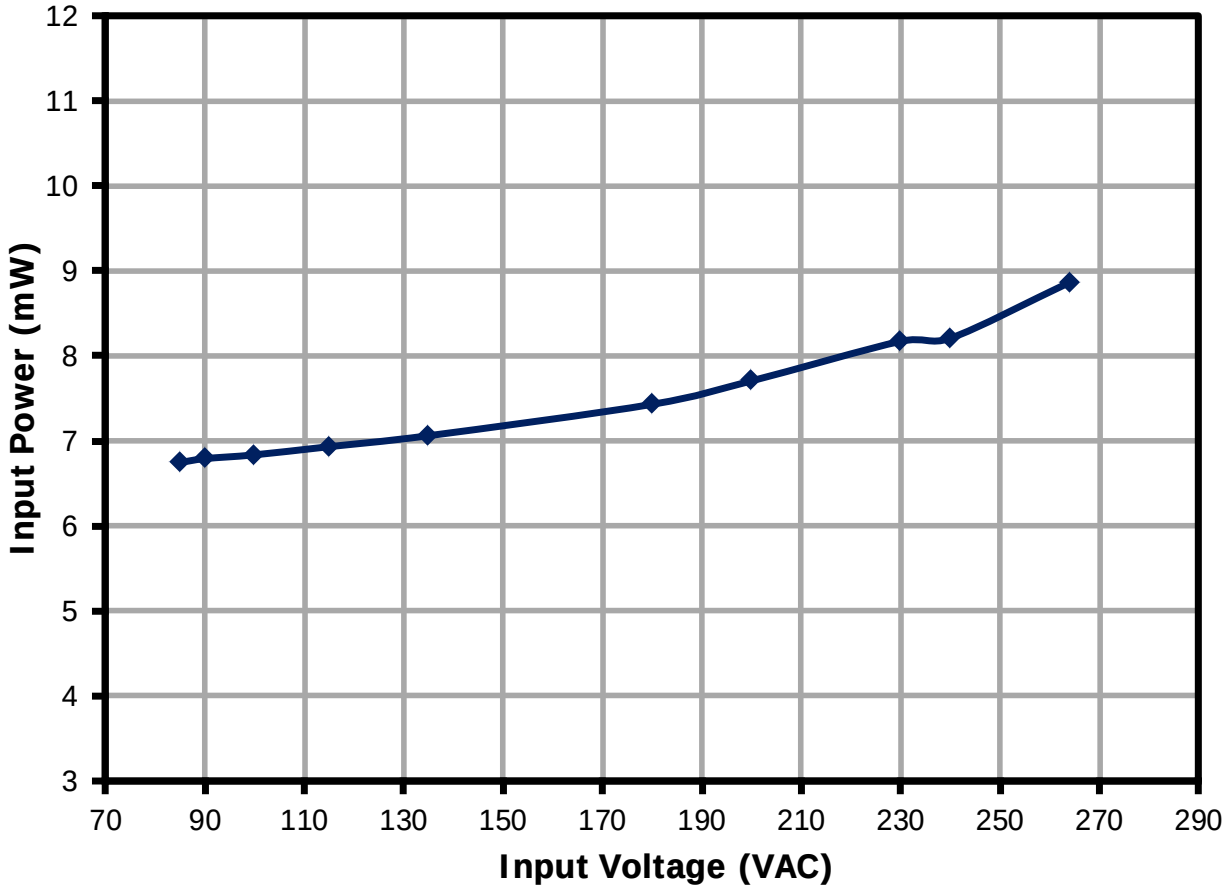

Figure 12 – No Load Input Power vs. Input Line Voltage, Room Temperature.

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9.4 *平均效率 (於 USB 插槽)*

9.4.1 效率要求

Test	Average	Average	Average	Average	10% Load	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
Effective	Now	2016	Now	2016	Now	2016
Power [W]	**Energy Star 2**	**New IESA2007**	**CoC v5 Tier 1**	**CoC v5 Tier 2**	**CoC v5 Tier 1**	**CoC v5 Tier 2**
10%	**74.2%**	**78.7%**	**76.0%**	**79.0%**	**66.6%**	**69.7%**

9.4.2 於 115 VAC 輸入條件下的平均效率

9.4.2.1 蕭特基二極體不與 Q1 並聯，SR FET

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	114.98	0.19	12.473	0.566	131	5.2575	1.999	10.509	84.26	
75	114.98	0.15	9.255	0.542	144.4	5.1950	1.499	7.789	84.16	
50	114.99	0.10	6.078	0.505	163.5	5.1300	0.999	5.124	84.30	
25	114.99	0.06	3.001	0.449	194.8	5.0550	0.500	2.525	84.14	**84.21**
10	114.99	0.03	1.266	0.392	231.7	5.0100	0.199	0.999	**78.94**	

9.4.2.2 蕭特基二極體 SS16 與 Q1 並聯，SR FET

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	114.98	0.19	12.492	0.572	129.4	5.2588	1.999	10.511	84.15	
75	114.99	0.15	9.230	0.544	143.5	5.1963	1.499	7.791	84.41	
50	114.99	0.10	6.060	0.508	162.6	5.1325	0.999	5.125	84.58	
25	114.99	0.06	2.987	0.452	193.4	5.0563	0.500	2.526	84.55	**84.42**
10	114.99	0.03	1.259	0.392	231.1	5.0113	0.199	0.999	**79.36**	

9.4.3 於 230 VAC 輸入條件下的平均效率

9.4.3.1 蕭特基二極體不與 Q1 並聯，SR FET

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	230.04	0.12	12.364	0.450	195.1	5.2663	1.999	10.527	85.14	
75	230.04	0.09	9.179	0.426	209.4	5.2000	1.499	7.797	84.94	
50	230.04	0.07	6.021	0.397	228.4	5.1363	0.999	5.130	85.20	
25	230.04	0.04	3.097	0.358	258.7	5.0488	0.500	2.522	81.43	**84.18**
10	230.04	0.02	1.273	0.312	300.9	5.0150	0.199	1.000	**78.56**	

9.4.3.2 蕭特基二極體 SS16 與 Q1 並聯，SR FET

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	230.04	0.12	12.329	0.449	195.6	5.2663	1.999	10.527	85.38	
75	230.04	0.09	9.133	0.425	210	5.2000	1.499	7.796	85.36	
50	230.04	0.07	6.007	0.397	229.2	5.1363	0.999	5.129	85.39	
25	230.04	0.04	3.073	0.357	259.5	5.0488	0.500	2.522	82.06	**84.55**
10	230.04	0.02	1.255	0.312	301.7	5.0150	0.199	1.000	**79.68**	

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9.5 *於纜線末端測得的 CV/CC 調節*

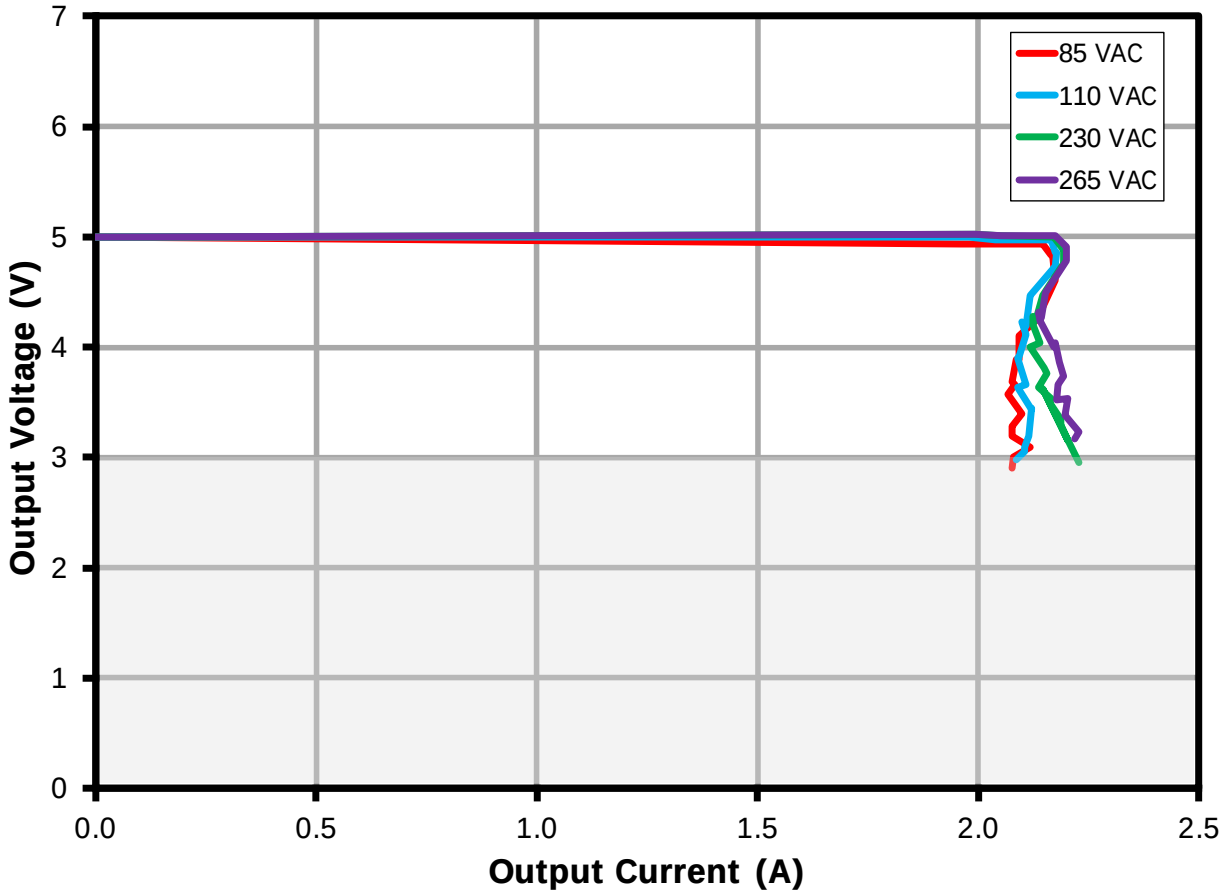

Figure 13 – Output Voltage vs, Output current, Room Temperature.

10 開放式外殼散熱效能

Room ambient.

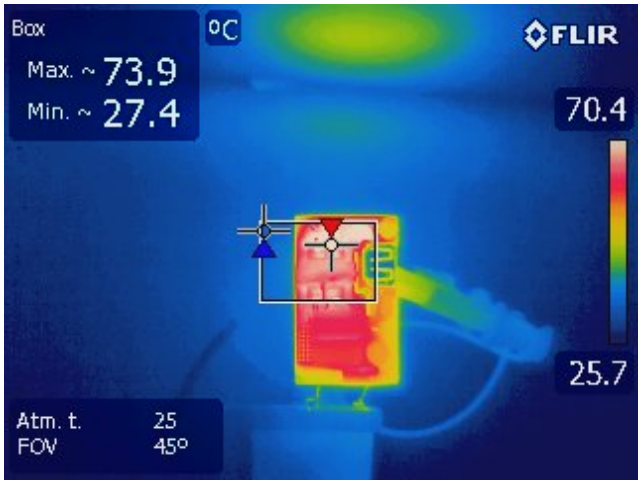

Figure 14 – Transformer Side.
85 VAC, 2 A Load.
Ambient = 26.3 ºC.

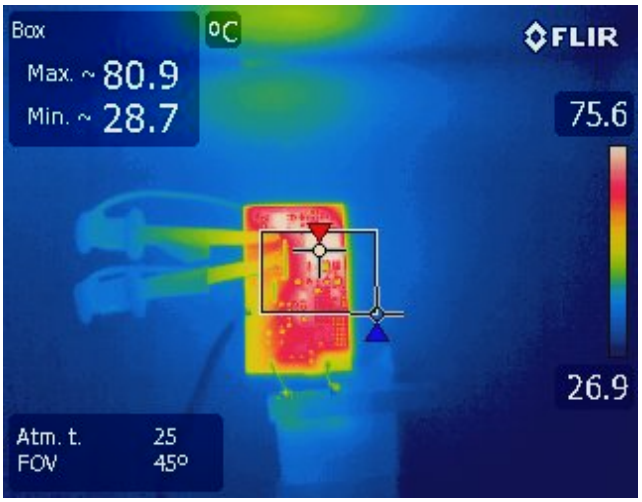

Figure 15 – InnoSwitch-CH Side.
85 VAC, 2 A Load.
Ambient = 27 ºC.

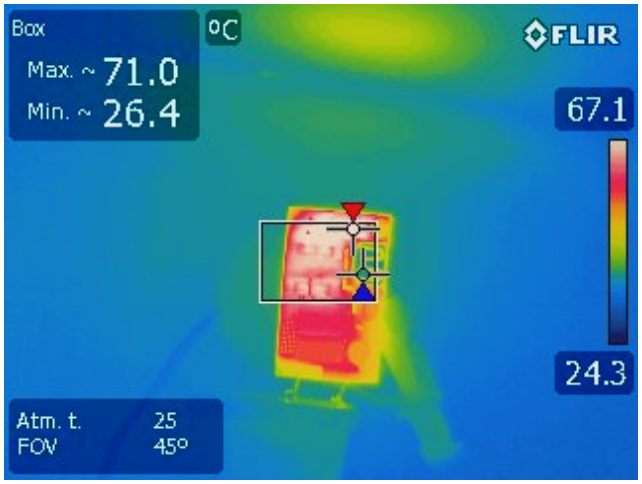

Figure 16 – Transformer Side.
110 VAC, 2 A Load.
Ambient = 26.2 ºC.

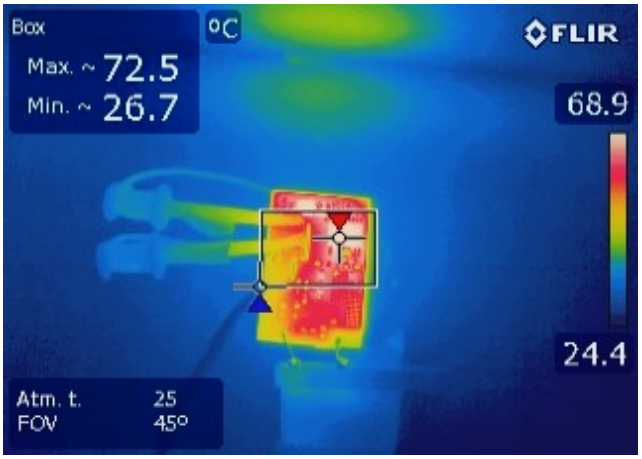

Figure 17 – InnoSwitch-CH Side.
110 VAC, 2 A Load.
Ambient = 25 ºC.

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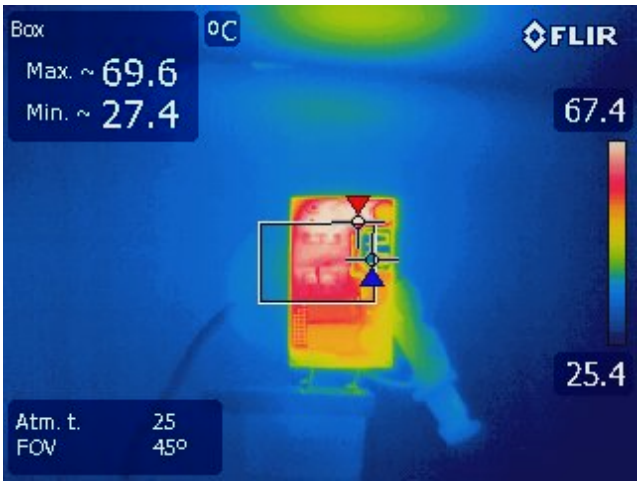

Figure 18 – Transformer Side.
230 VAC, 2 A Load.
Ambient = 26.5 ºC.

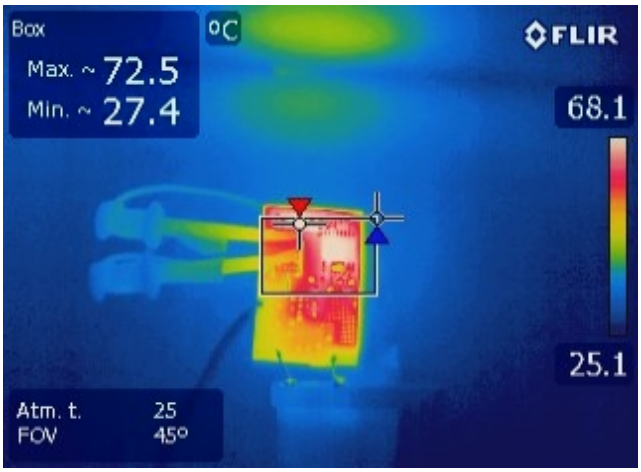

Figure 19 – InnoSwitch-CH Side.
230 VAC, 2 A Load.
Ambient = 25.4 ºC.

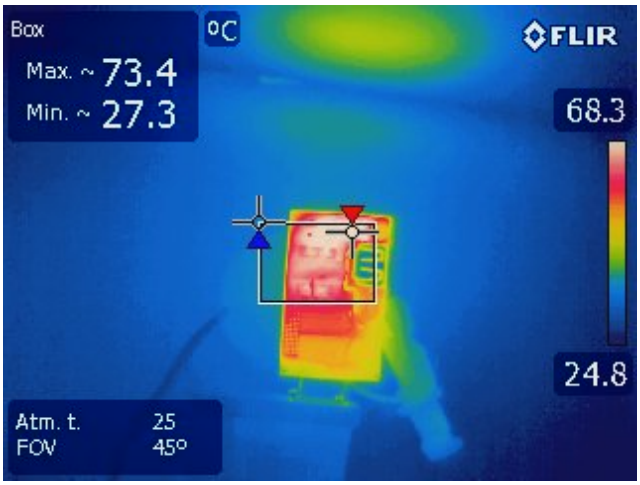

Figure 20 – Transformer Side.
265 VAC, 2 A Load.
Ambient = 26.5 ºC.

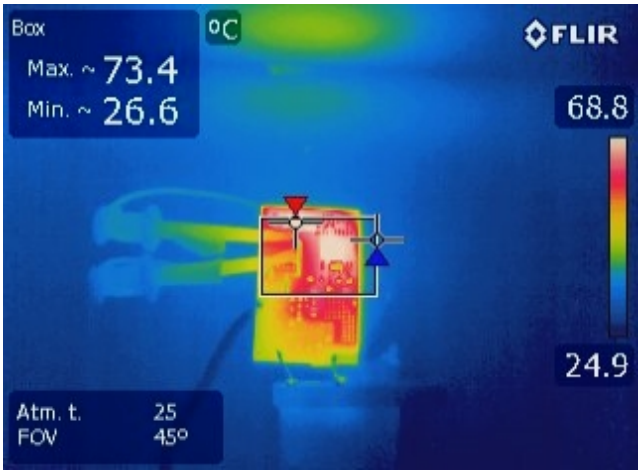

Figure 21 – InnoSwitch-CH Side.
265 VAC, 2 A Load.
Ambient = 25.3 ºC.

11 波形

11.1 *負載暫態反應 (纜線末端)*

Results were measured with 47 µF at end of cable which is the typical specified measurement condition for mobile phone chargers.

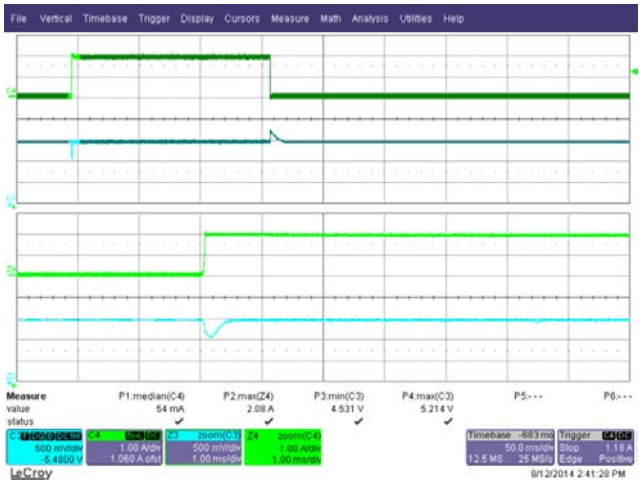

Figure 22 – Transient Response (4.5 V_{MIN}).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

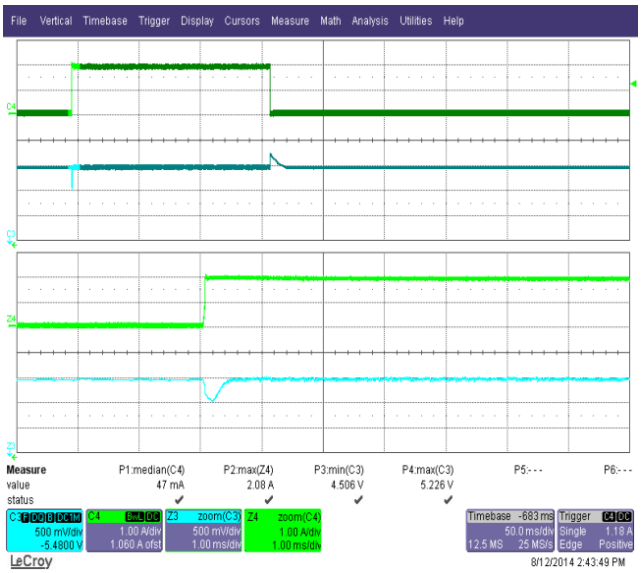

Figure 23 – Transient Response (4.5 V_{MIN}).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

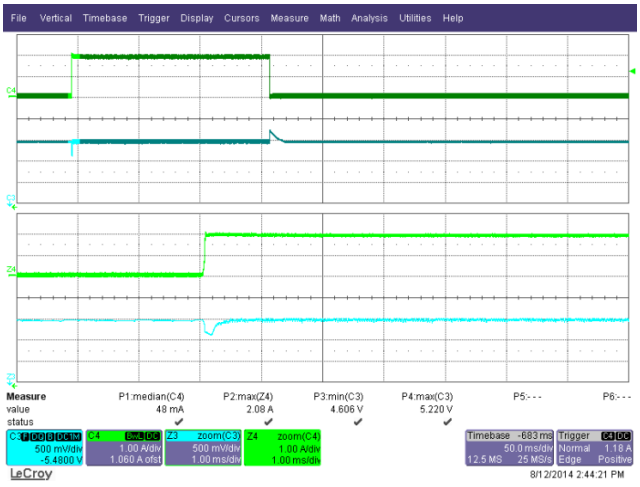

Figure 24 – Transient Response (4.6 V_{MIN}).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

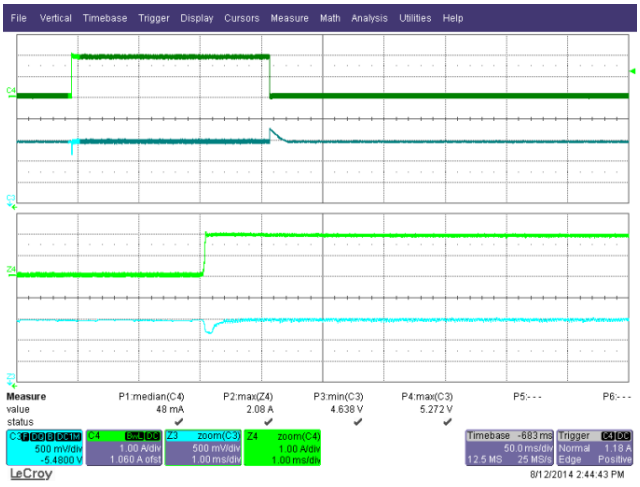

Figure 25 – Transient Response (4.6 V_{MIN}).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

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11.2 *負載暫態反應 (於 USB 插槽)*

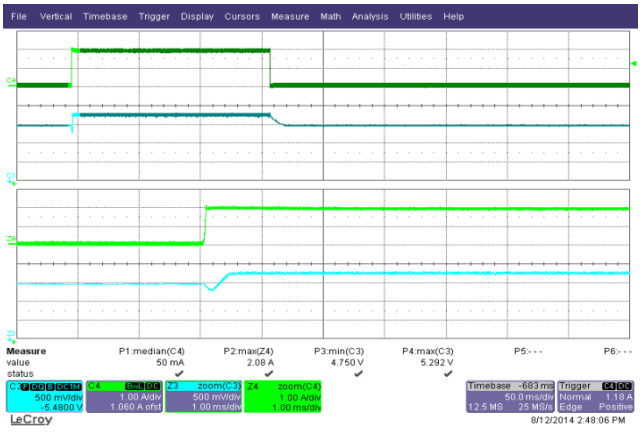

Figure 26 – Transient Response (4.75 V_{MIN}).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

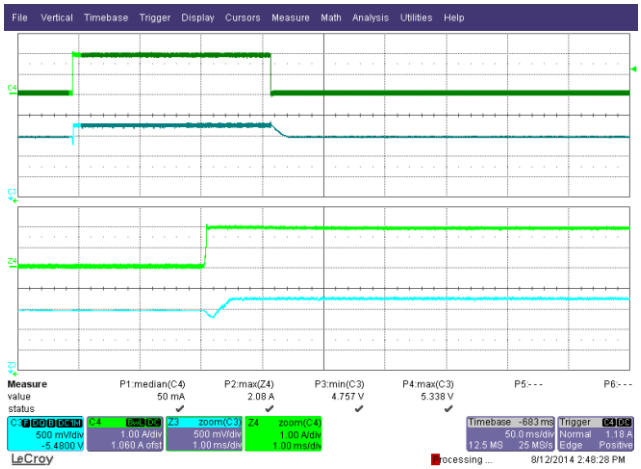

Figure 27 – Transient Response (4.75 V_{MIN}).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

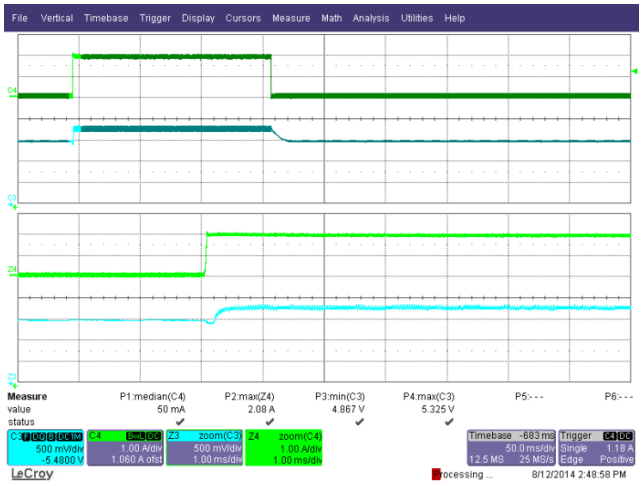

Figure 28 – Transient Response (4.85 V_{MIN}).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

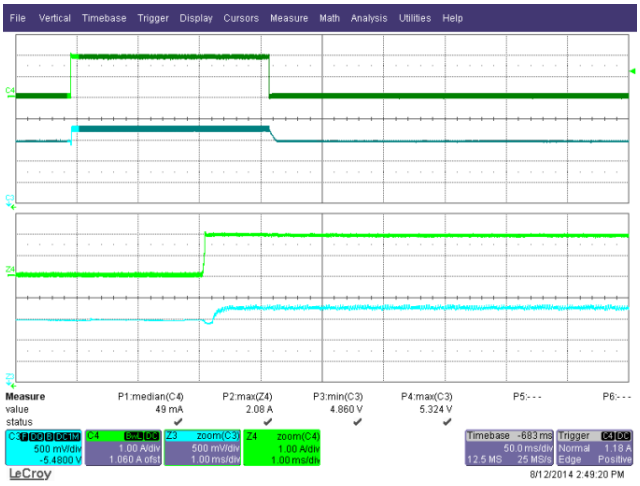

Figure 29 – Transient Response (4.86 V_{MIN}).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A /div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

11.3 *切換波形*

11.3.1 InnoSwitch-CH 波形

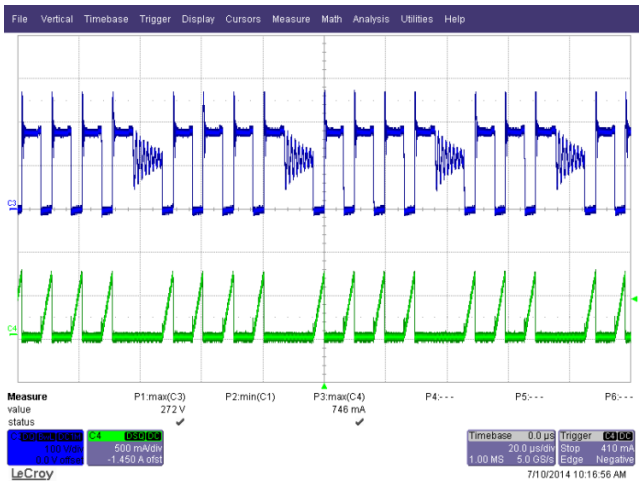

Figure 30 – Drain Voltage and Current Waveforms.
85 VAC, 2 A load,
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 100 V, 20 µs / div.

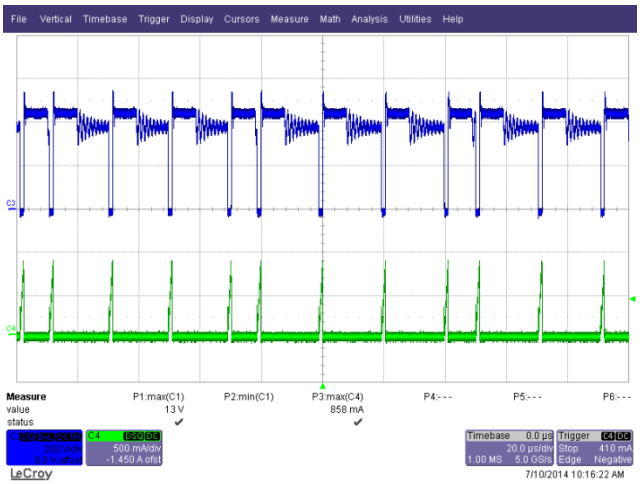

Figure 31 – Drain Voltage and Current Waveforms.
265 VAC, 2 A Load, 545 V_{MAX}.
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 20 µs / div.

11.3.2 SR FET 波形

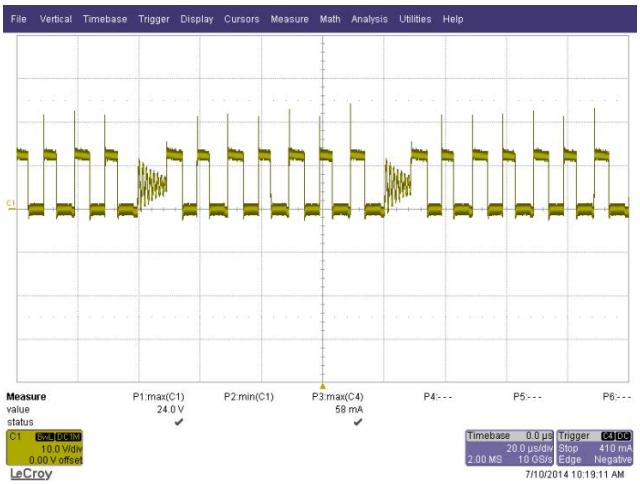

Figure 32 – SR FET Voltage Waveforms.
85 VAC Input, 2 A Load.
V_{DRAIN}, 10 V, 20 µs / div.

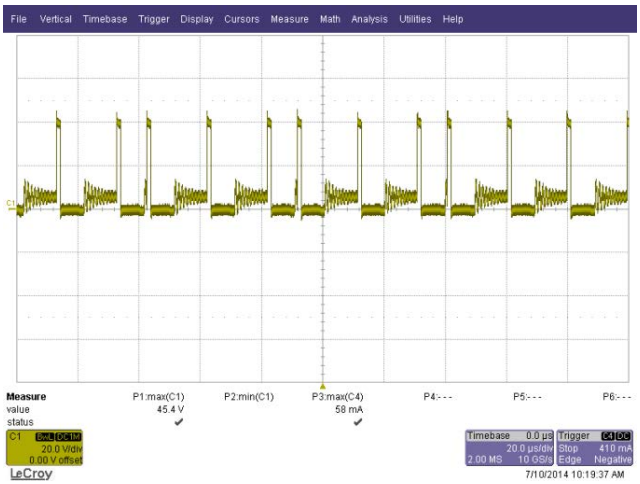

Figure 33 – SR FET Voltage Waveforms.
265 VAC Input, 2 A Load.
V_{DRAIN}, 20 V, 20 µs / div. (45.4 V_{MAX}).

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11.4 *輸出漣波測量*

11.4.1 漣波測量技術

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

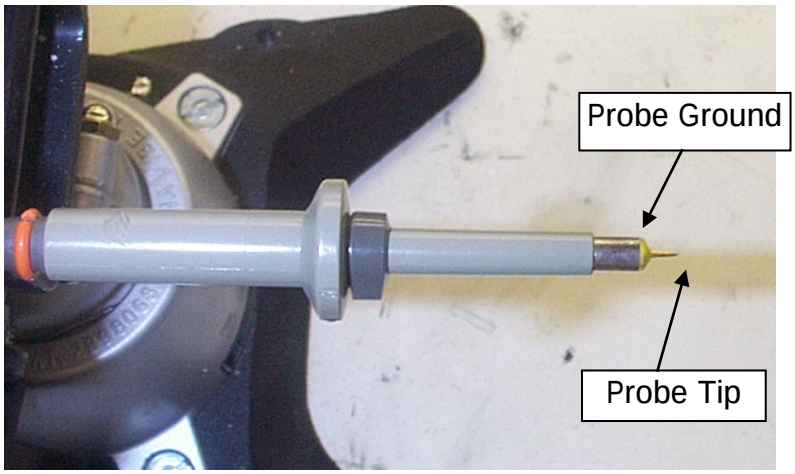

Figure 34 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

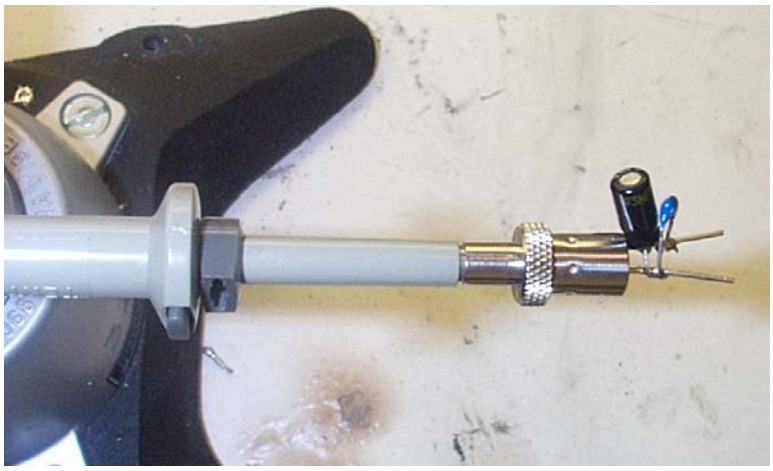

Figure 35 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.4.2 測量結果

Measured at the end of cable.

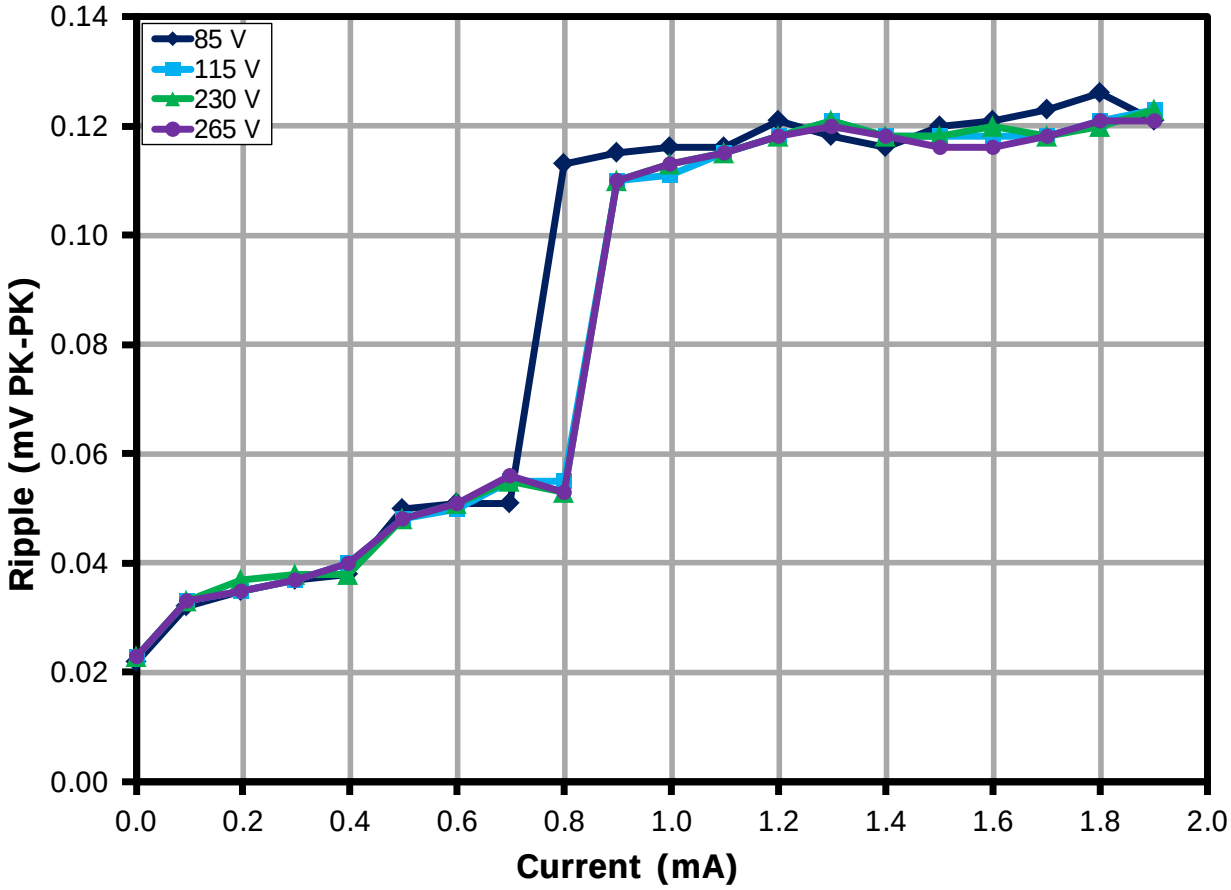

Figure 36 – Output Ripple Voltage.

RIPPLE (mV PK-PK) 85 V	RIPPLE (mV PK-PK) 115 V	RIPPLE (mV PK-PK) 230 V	RIPPLE (mV PK-PK) 265 V
0.126	0.123	0.123	0.121

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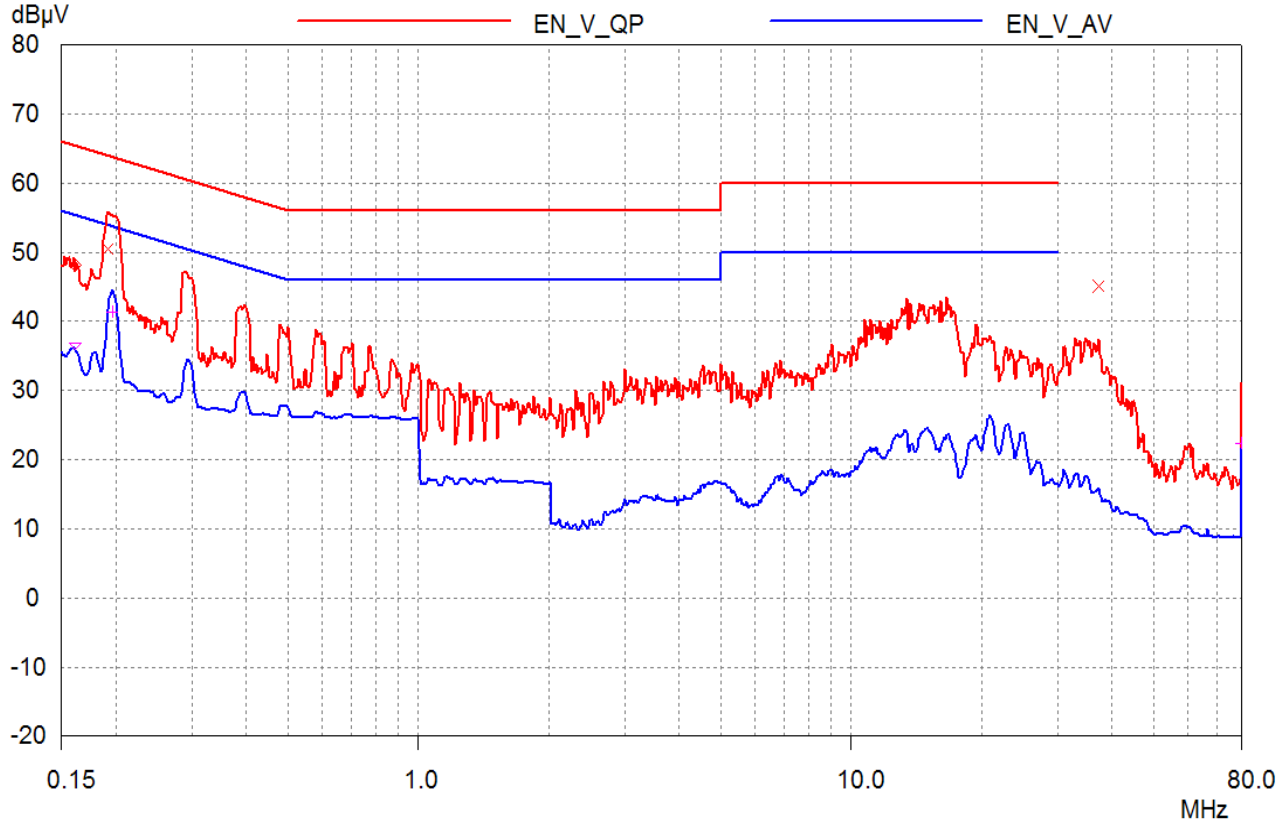
12 傳導性 EMI

12.1 *2 A 電阻負載，浮接輸出 (PK / AV)*

After running 5 minutes.



Freq (MHz)	QP	Limit	Margin
0.19	50.48	63.95	13.47

Figure 37 – Floating Ground EMI at 115 VAC.

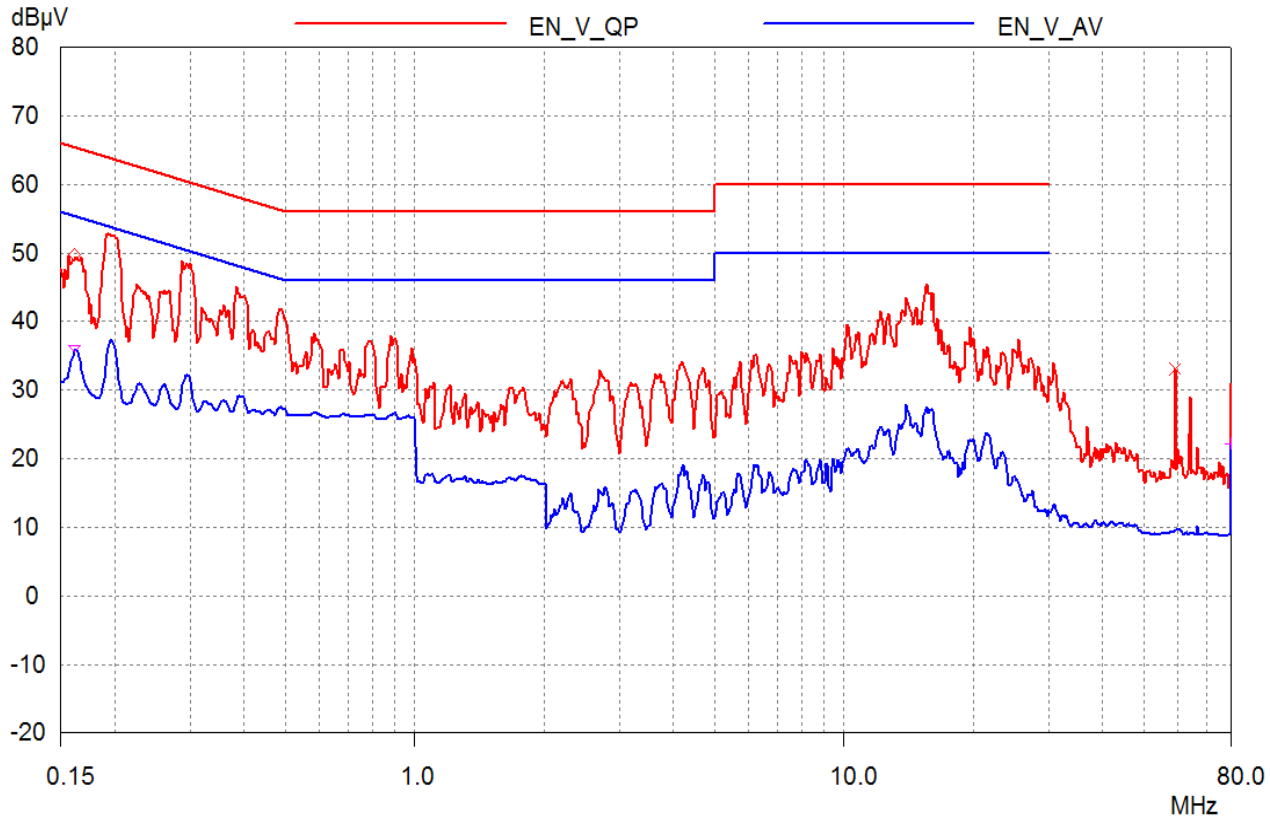


Figure 38 – Floating Ground at 230 VAC.

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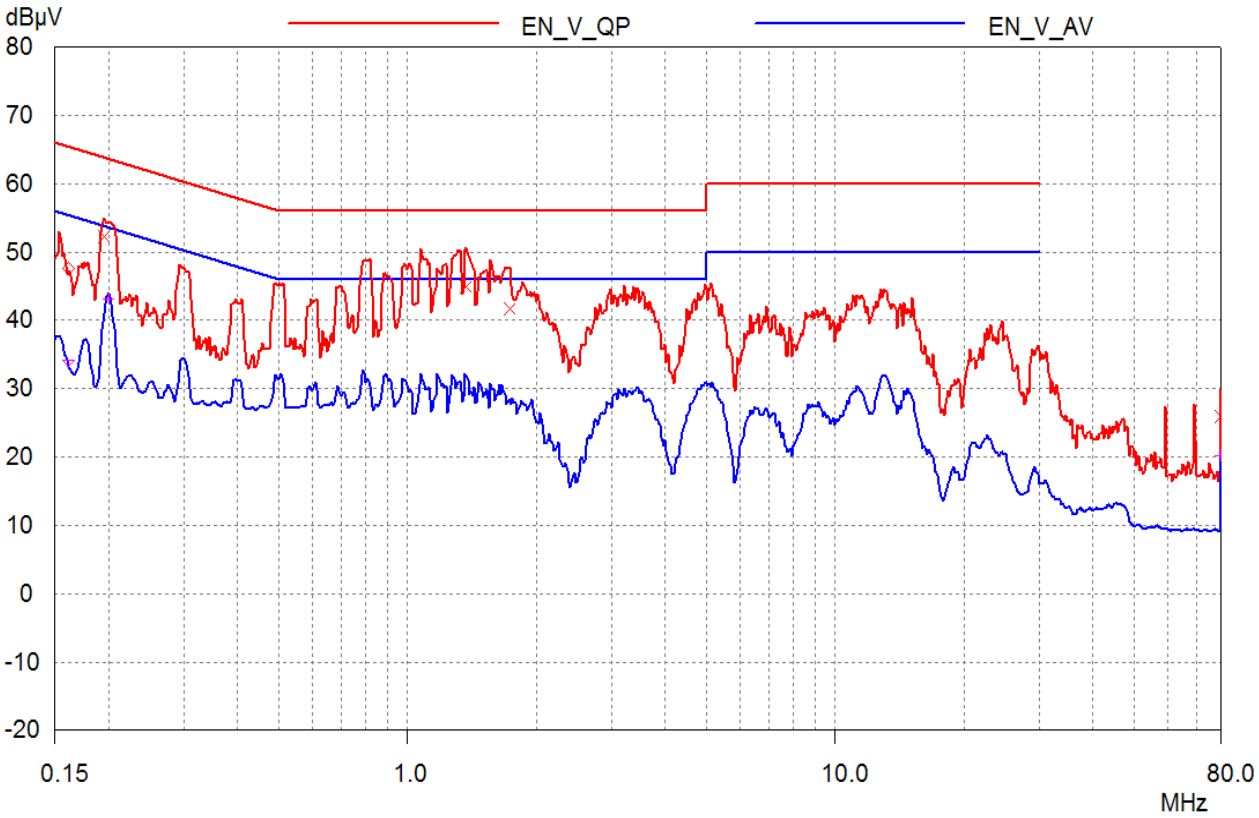
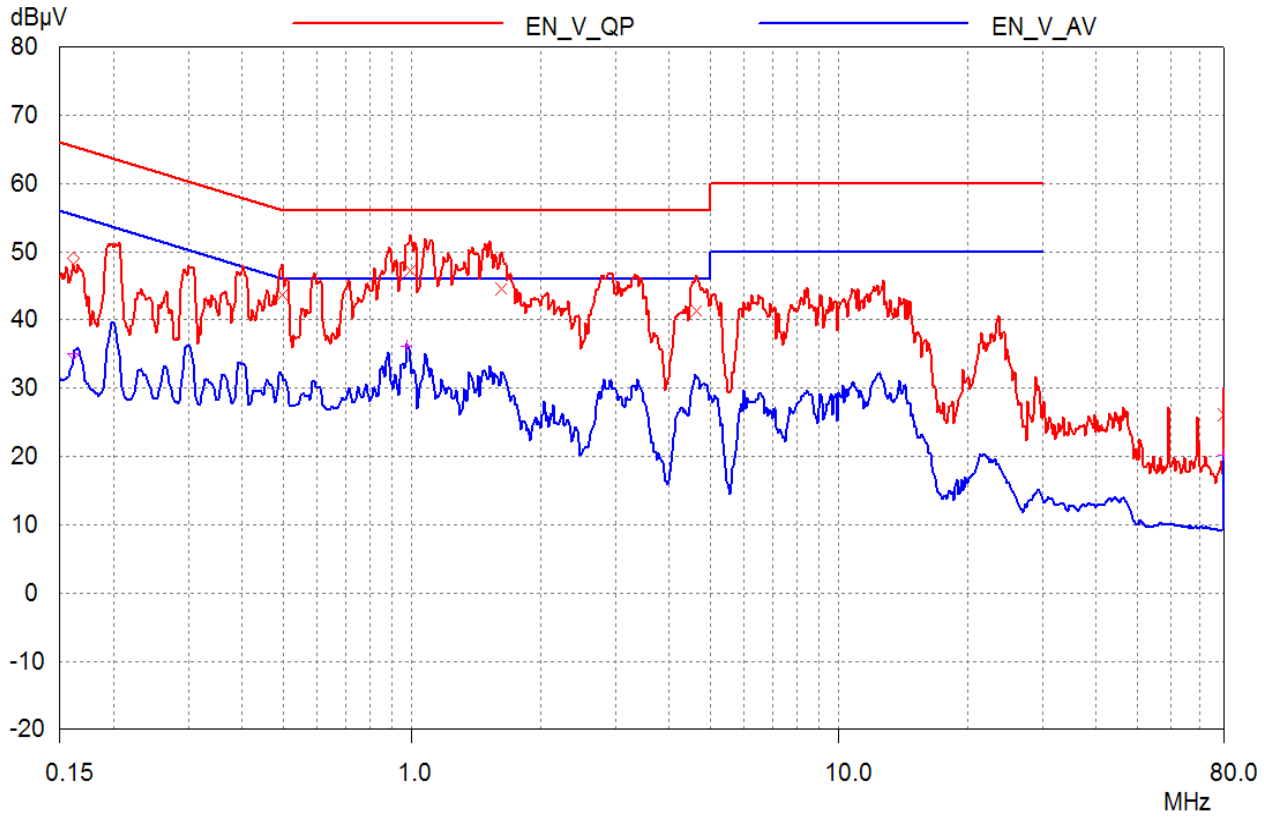
12.2 *2 A 電阻負載，人工手動接地 (PK/AV)*



FREQ (MHZ)	QP	LIMIT	MARGIN
0.20	52.26	63.82	11.56
1.37	44.97	56	11.03
1.73	41.65	56	14.35

Figure 39 – Artificial Ground at 115 VAC.



FREQ (MHZ)	QP	LIMIT	MARGIN
0.50	43.6	56.07	12.47
0.99	47.3	56	8.7
1.62	44.51	56	11.49
4.65	41.37	56	14.63

Figure 40 – Artificial Ground at 230 VAC.

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12.3 *含監視器設置 (HDMI) 的智慧型手機 (QP/AV)*

Phone is connected to charger and LCD monitor. The monitor connection increases capacitance to earth ground.

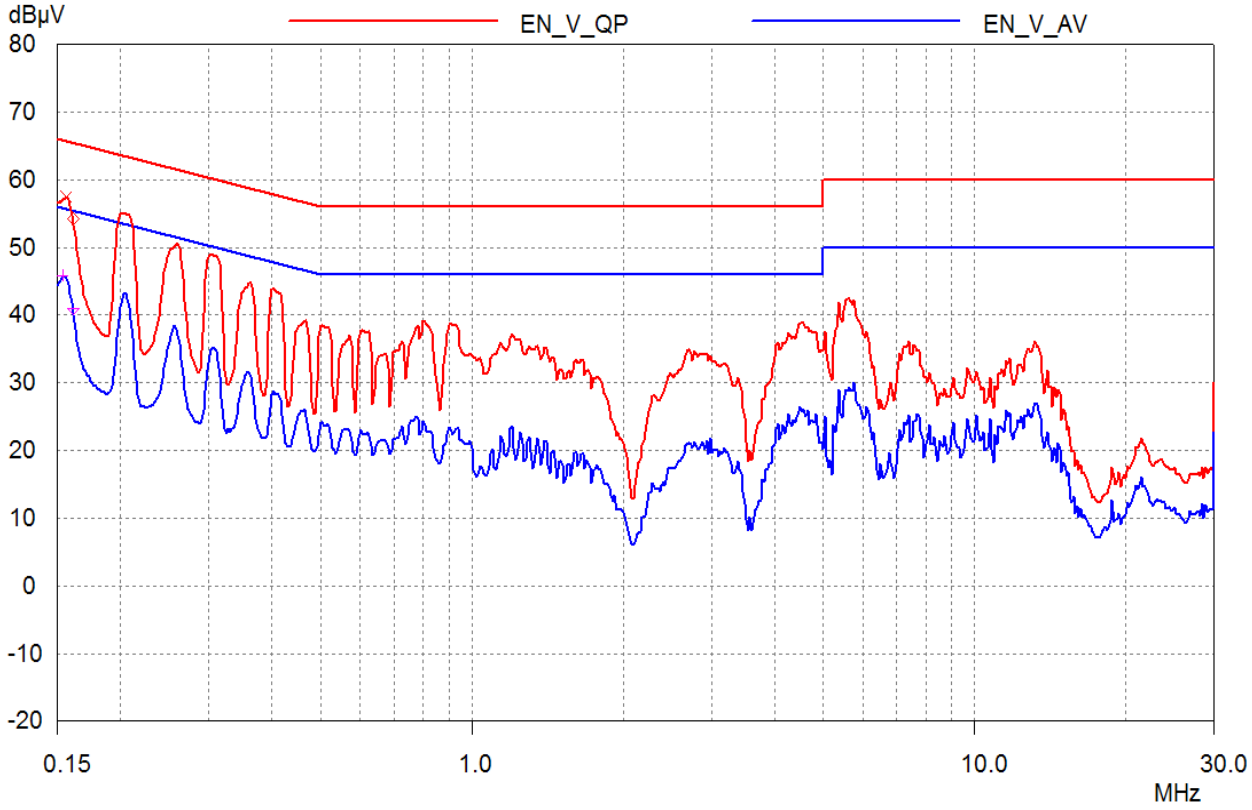

Figure 41 – HDMI at 115 VAC.

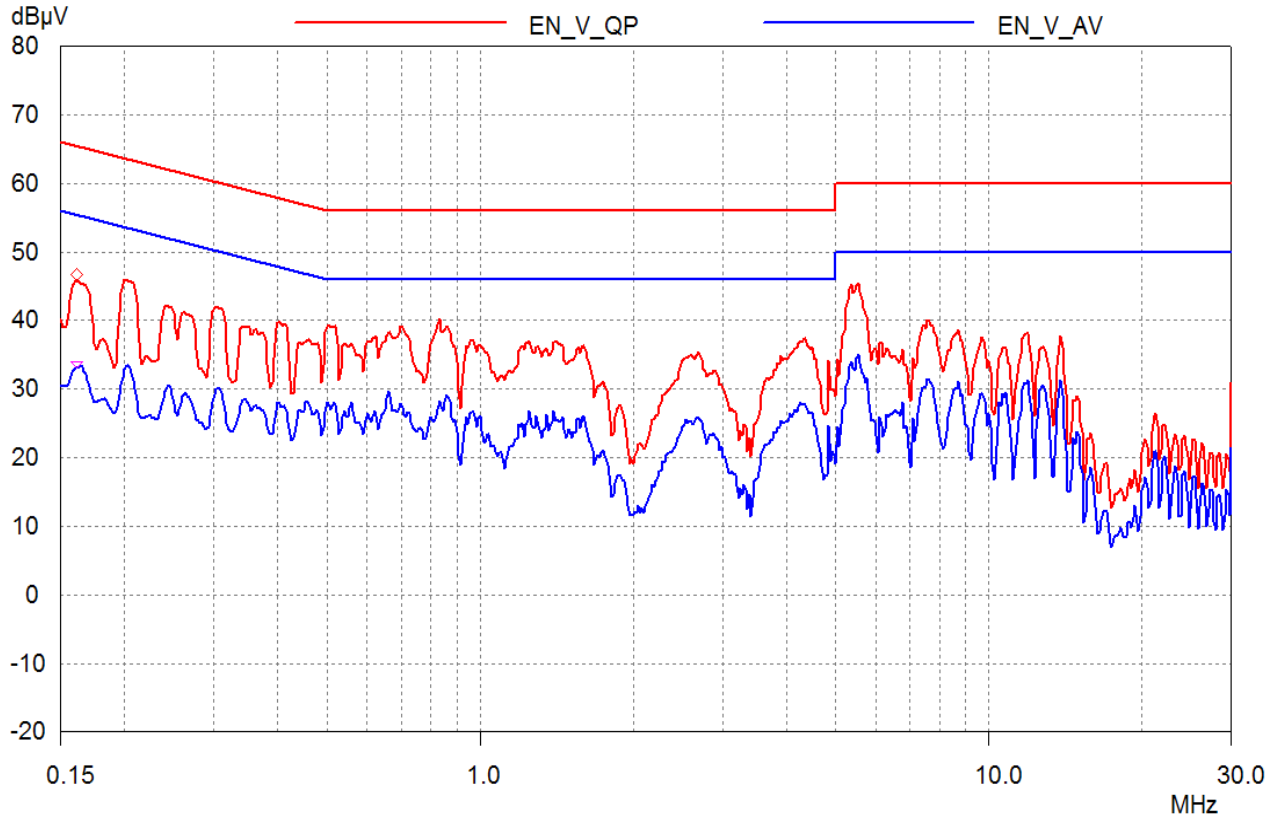

Figure 42 – HDMI at 230 VAC**.**

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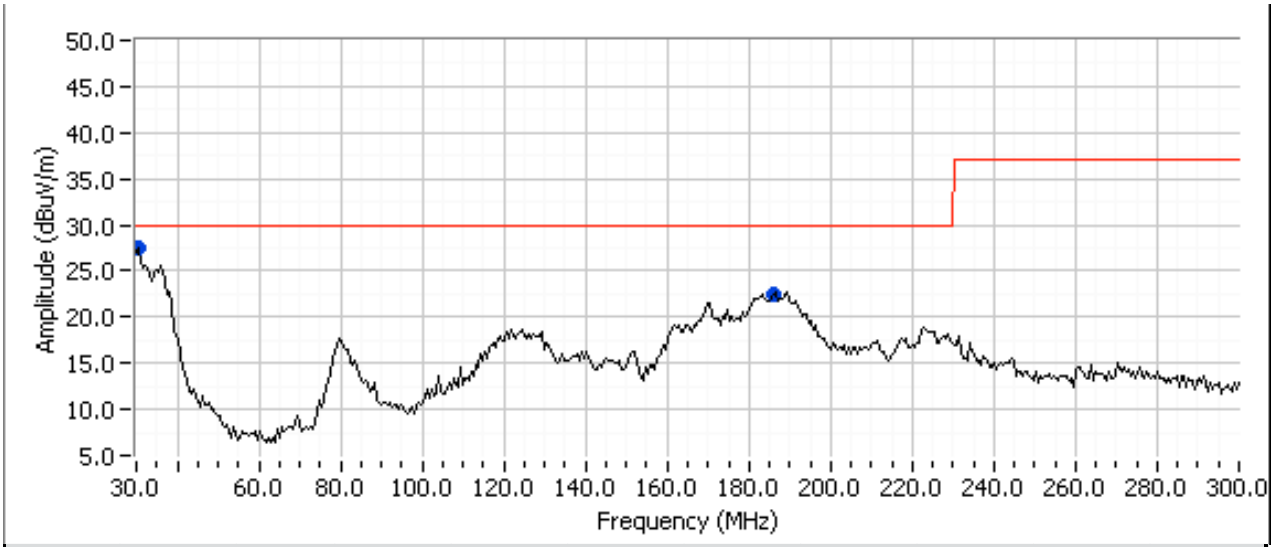
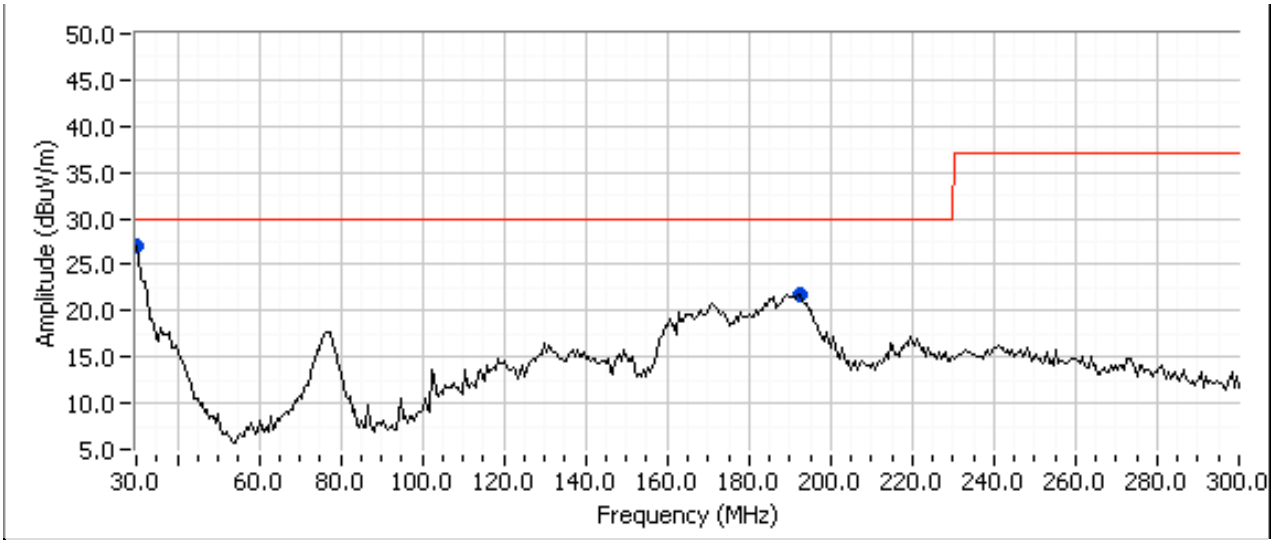
13 輻射 EMI



Maximized quasi-peak readings (NO manipulation of EUT interface cables)

Frequency	Level	Pol	Class B		Detector	Azimuth	Height	Comments
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters	
30.234	23.7	V	30.0	-6.3	QP	4	1.0	QP (1.00s)
185.989	19.4	H	30.0	-10.6	QP	116	4.0	QP (1.00s)

Figure 43 – Radiation at 110 VAC.



Maximized quasi-peak readings (NO manipulation of EUT interface cables)

Frequency	Level	Pol	Class B		Detector	Azimuth	Height	Comments
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters	
30.287	23.8	V	30.0	-6.2	QP	57	1.0	QP (1.00s)
191.605	19.9	H	30.0	-10.1	QP	121	4.0	QP (1.00s)

Figure 44 – Radiation at 230 VAC**.**

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14 噪音

Test performed inside case with microphone placed 3 mm from case surface on long side of case, transformer facing towards microphone.

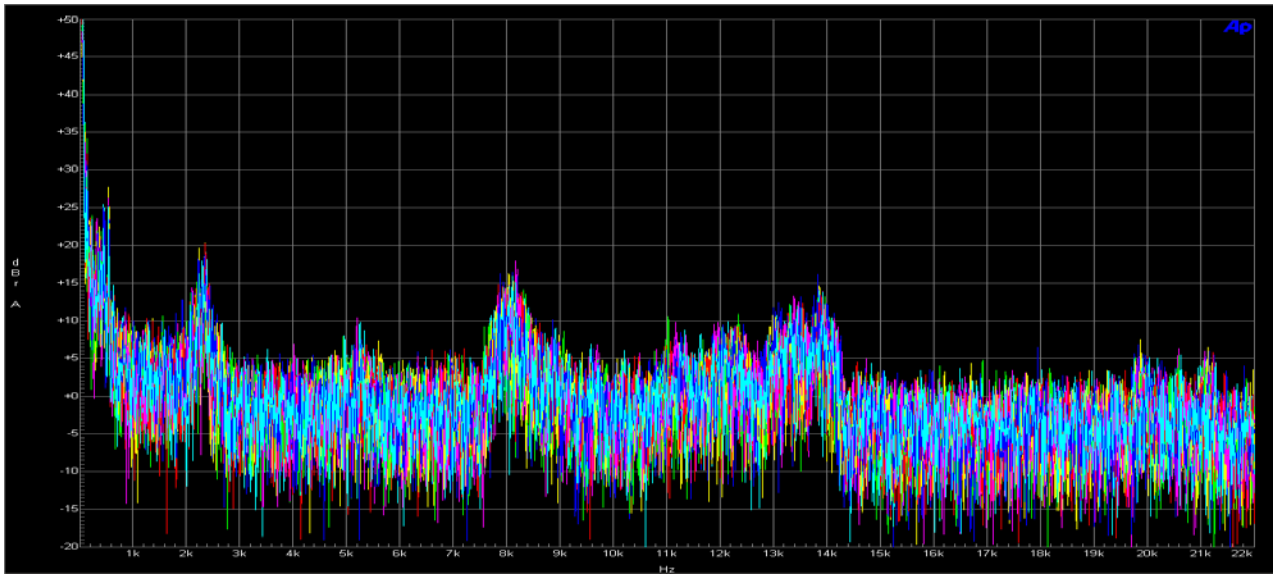

Figure 45 – Audible Noise Spectrum: No-load, V_{IN} Swept from 85 VAC to 264 VAC.

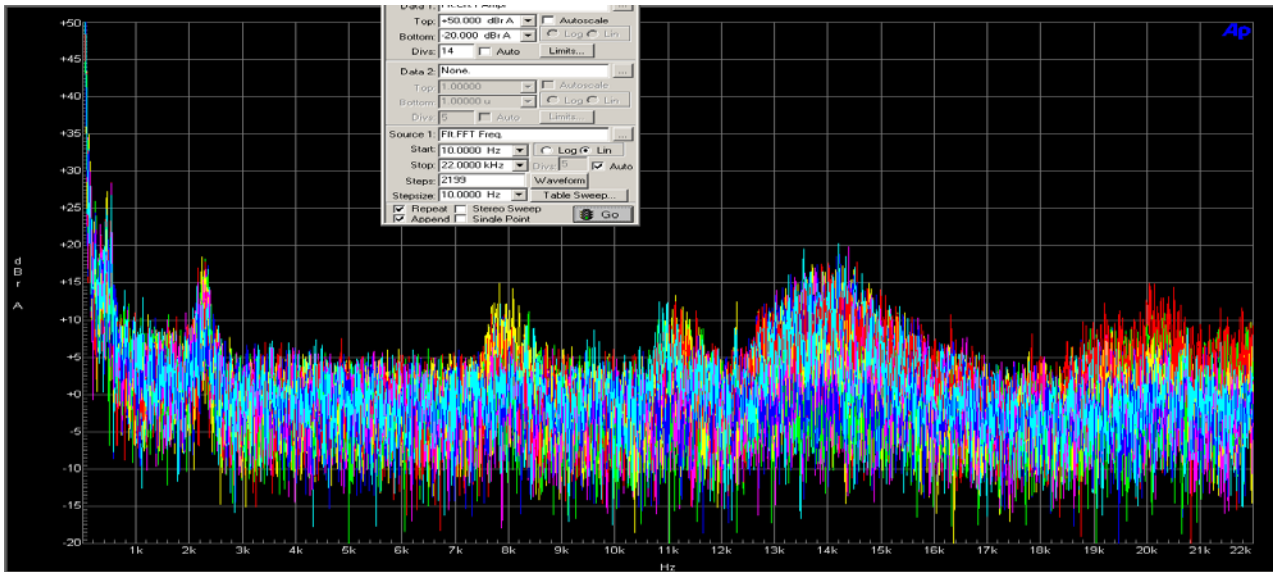

Figure 46 – Audible Noise Spectrum: 85 VAC, I_{OUT} Swept from 0 A to 2.0 A.

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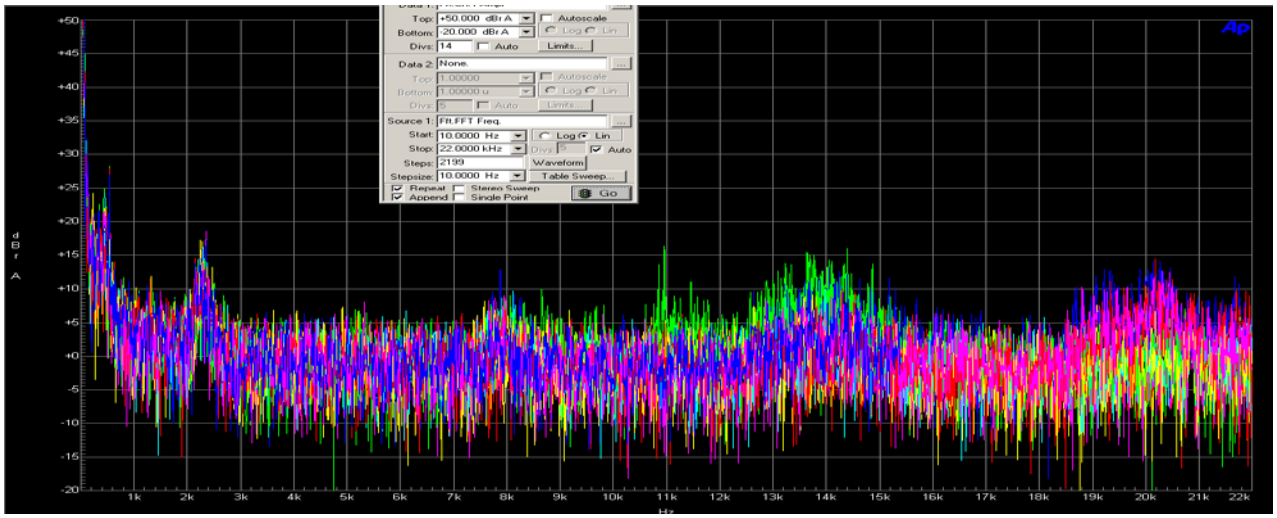

Figure 47 – Audible Noise Spectrum: 110 VAC, I_{OUT} Swept from 0 A to 2.0 A.

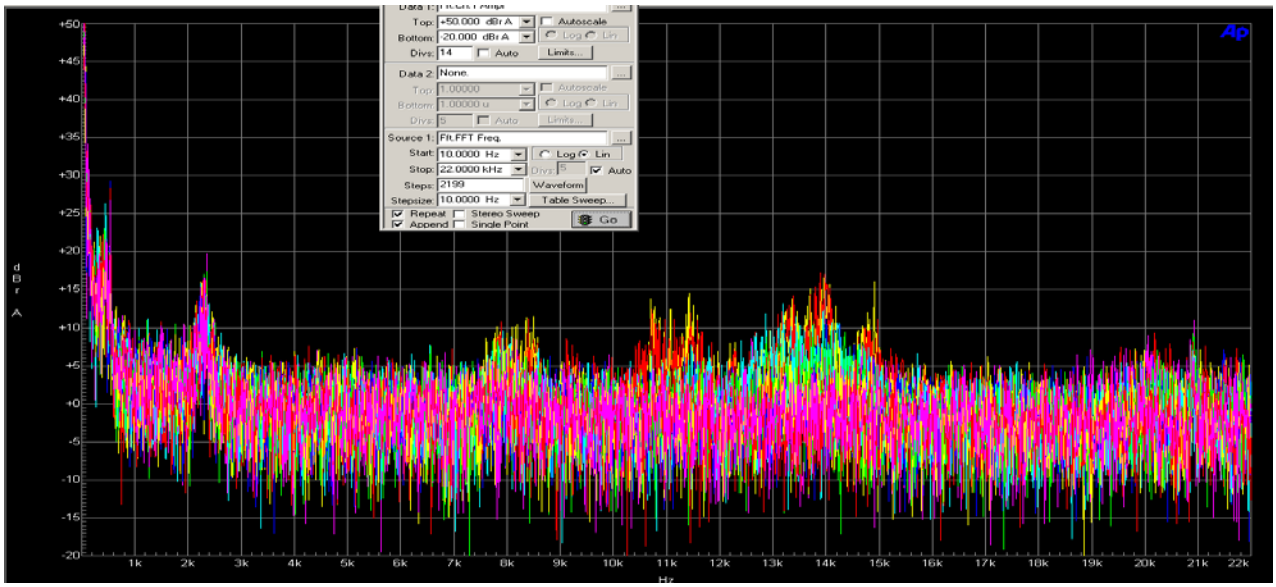

Figure 48 – Audible Noise Spectrum: 220 VAC, I_{OUT} Swept from 0 A to 2.0A.

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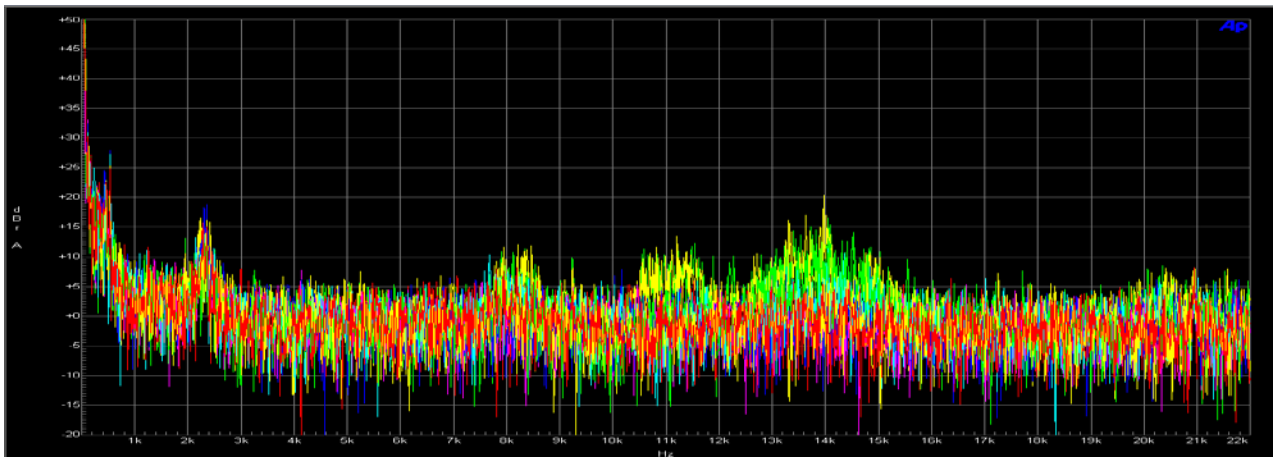

Figure 49 – Audible Noise Spectrum: 265 VAC, I_{OUT} Swept from 0 A to 2.0 A.

15 雷擊突波與 ESD 測試

15.1 *差模測試*

Passed ±1 kV, 500 A surge test

15.2 *共模測試*

Passed ±6 KV, 500 A ring wave test.
Need to install plastic barrier for >5 kV ring wave common mode surge test.

15.3 *ESD 測試*

Passed ±16.5 kV air, 8 kV contact.
Need to install plastic barrier to pass ESD test.

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16 修訂記錄

日期	作者	修訂	說明與變更	已審核
2014 年 11 月 11 日	DK	1.0	初始版本	行銷與應用部門

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