标题	***参考设计报告：使用 InnoSwitch™-CH INN2023K 设计的 10 W 恒压/恒流 USB 充电器***
规格	85 VAC – 264 VAC 输入； 5 V/2 A 输出（USB 电缆末端）
应用	手机/USB 充电器
作者	应用工程部
文档编号	RDR-420
日期	2014 年 11 月 11 日
修订版本	1.0

特色概述

- InnoSwitch-CH – 业界首款具备隔离式、高安全等级的集成反馈功能的 AC/DC IC
- 具备次级侧控制的所有优势，同时初级侧调节极为简单
  - ±3%恒压、±5%恒流调节
  - 对变压器变化不敏感
  - 瞬态响应与负载时序无关
  - 尺寸更小、成本更低的输出电容
  - 空载输入功率功耗<10 mW
  - 电缆压降补偿
- 内置的同步整流，可提高效率

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目录

重要说明：
虽然本电路板的设计满足安全隔离要求，但工程原型尚未获得机构认证。因此，必须使用隔离变压器向原型板提供 AC 输入，以执行所有测试。

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1 简介

本文档是一份工程报告，介绍使用 InnoSwitch-CH 系列 IC 器件设计的一款 2 A/5.0 V USB 充电器。本设计旨在展示最新 IC 的高集成度所带来的高功率密度和高效率，同时它仍能提供出色的性能。

本文档包括电源规格、电路原理图、物料清单、变压器规格文件、印刷电路板布局及性能数据。

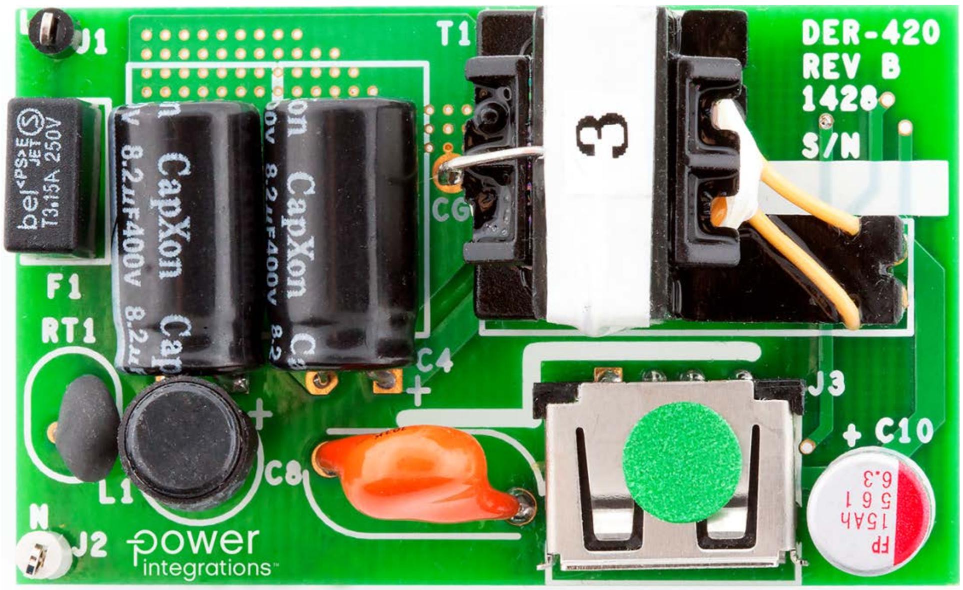

Figure 1 – Populated Circuit Board Photograph, Top.

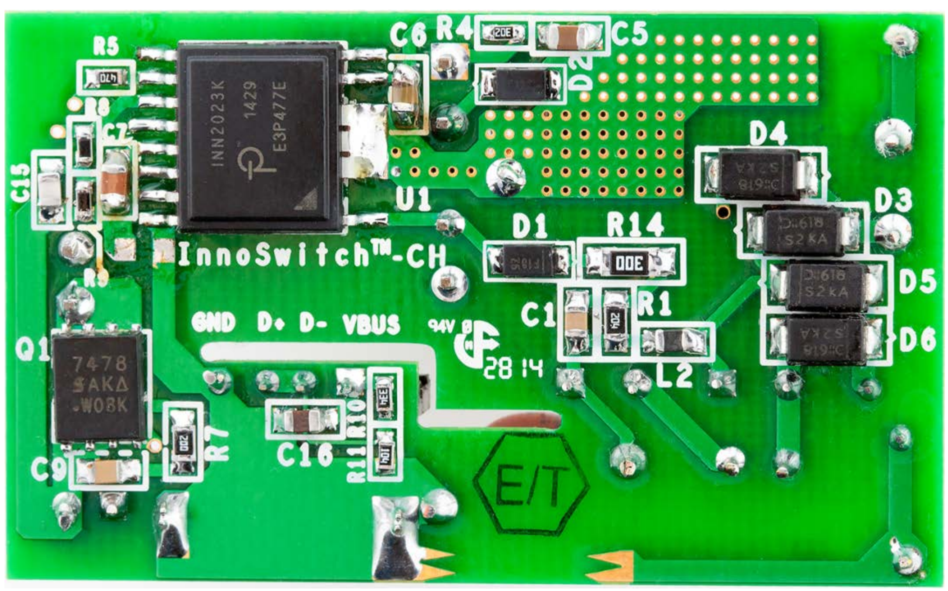

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 电源规格

下表所列为设计的最低可接受性能。实际性能可参考测量结果部分。

说明	符号	最小值	典型值	最大值	单位	备注
输入						
电压	$\mathbf{V_{IN}}$	85		265	VAC	双导线 – 无 P.E.
频率	$\mathbf{f_{LINE}}$	50	50/60	64	Hz	
空载输入功率				10	mW	230 VAC
输出						
输出电压	$\mathbf{V_{OUT}}$	4.75	5.0	5.25	V	0.35 V 电缆电阻压降
瞬态输出电压	$\mathbf{V_{OUT(T)}}$	4.2		5.5	V	0 A - 2 A - 0 A 负载阶跃（电缆末端） 输出电缆末端
输出纹波电压	$\mathbf{V_{RIPPLE}}$			150	mV	输出电缆末端
输出电缆压降补偿	$\mathbf{V_{CBL}}$	250	300	350	mV	2 A 输出电流
输出电流恒流点	$\mathbf{I_{OUT}}$	2		2.5	A	
自动重启动电压	$\mathbf{V_{AR}}$	2		3.5	V	电缆末端
导通上升时间	$\mathbf{t_R}$			20	ms	
额定输出功率	$\mathbf{P_{OUT}}$		10		W	
效率						
平均	$\eta_{AVE[BRD]}$	84			%	在 USB 插口测得
25%、50%、75%和 100%	$\eta_{AVE[CBL]}$	80			%	带有 0.38 V 电缆电阻压降
10%	$\eta_{10\%}$	79			%	
环境						
输出电缆电阻	R_{CBL}		190		mΩ	
传导 EMI		CISPR22B / EN55022B 负载浮动或通过假手接地				电阻性负载，6 dB 裕量
		连接手机或电视机（采用 MHL 连接）				6 dB 裕量
安全		IEC950 / UL1950 Class II				设计符合
音频噪声				25	dB	3 cm 处测得
输入浪涌 共模(L1/L2-PE)				6	kV	振铃波，共模： 12 Ω
ESD		±16.5 ±8			kV kV	接触 空气放电 性能无任何下降
环境温度	$\mathbf{T_{AMB}}$	0		40	°C	自然对流，海平面，密闭壳体

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3 电路原理图

		VAC			
		85	115	230	265
Efficiency at PCB (%)	Average		84.2	84.2	
	Full Load	82.6	84.2	85.1	84.8
	10% Load	78.3	78.9	78.6	78.7
No-Load Input	(mW)	7	7	8	9

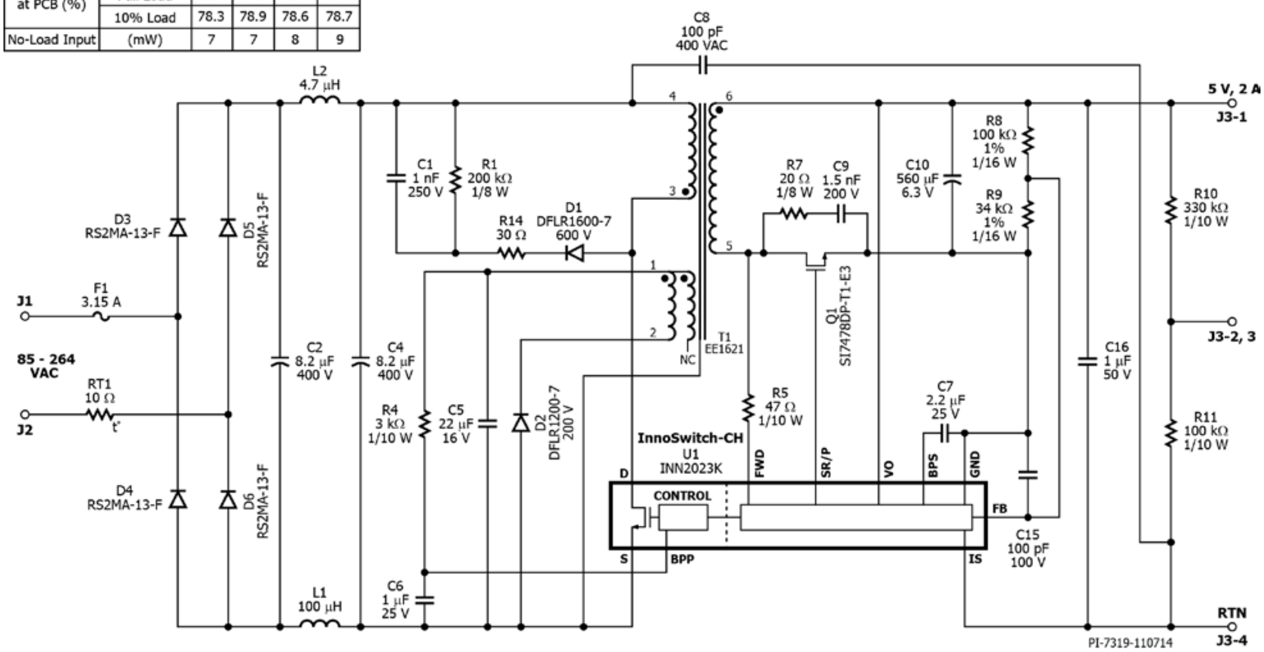

Figure 3 – Schematic.

4 电路描述

4.1 *输入 EMI 滤波*

保险丝 F1 为初级侧元件提供严重故障保护。

有必要使用一个浪涌限制热敏电阻(RT1)，因为整流二极管(D1-D4)的浪涌电流额定值较低，并且大容量电容 C2 和 C4 的值相对较高且具低阻抗。

D1-D4 选用了小尺寸的二极管，因为空间受限，特别是 PCB 到壳体的高度较小。

电容 C2 和 C4 对整流 AC 输入提供滤波，与 L1 和 L2 一起形成 π 型滤波器，对差模 EMI 进行衰减。低值 Y 电容(C8)可降低共模 EMI。

4.1 *InnoSwitch-CH IC 初级*

变压器初级的一端连接到整流 DC 总线，另一端连接到 InnoSwitch-CH IC (U1)内集成的 650 V 功率 MOSFET。

由 D1、R1、R14 和 C1 形成的低成本 RCD 箝位可限制峰值漏极电压（受变压器和输出走线电感影响而产生）。

IC 具有自启动功能，当首次 AC 上电时，它使用内部高压电流源对 BPP 引脚电容(C6)进行充电。在正常工作期间，初级侧控制从变压器的辅助绕组获得供电。其输出采用反激式绕组，通过电流限制电阻 R4 进行整流和滤波（D2 和 C5）并馈入 BPP 引脚。

输出稳压通过采用 ON/OFF 控制来实现，使能开关周期的数量根据输出负载进行调整。在重负载下，大部分开关周期都被使能；在轻载或空载下，大部分周期都被禁止或跳过。一旦周期使能后，功率 MOSFET 将保持导通，直到初级电流逐渐增大到特定工作状态的器件限流点。该 IC 设定了四种工作状态（限流点），以使初级电流开关模式的频率分量保持在音频范围之外，直到轻载时，变压器磁通密度以及因此产生的音频噪声都处于极低水平。

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4.2 *InnoSwitch-CH IC 次级*

InnoSwitch-CH 的次级侧提供输出电压、输出电流检测并驱动提供同步整流的 MOSFET。

变压器的次级由 Q1 整流，由 C10 滤波。开关瞬态期间的高频率振铃通过缓冲器元件 R7 和 C9 降低，而开关瞬态期间会产生 Q1 高压和辐射 EMI。

为降低耗散，同步整流(SR)由 Q1 提供。Q1 的栅极根据通过 R5 和 IC 的 FWD 检测到的绕组电压进行导通。在连续导通模式下，功率 MOSFET 就在次级侧下达初级侧请求的新开关周期指令之前关断。在非连续导通模式下，MOSFET 会在 MOSFET 的电压降低于阈值时关断。对初级侧 MOSFET 的次级侧控制可确保它永不会与同步整流 MOSFET 同时导通。MOSFET 驱动信号是 SR/P 引脚的输出。

IC 的次级侧从次级绕组正向电压或输出电压自行供电。在恒压(CV)工作期间，输出电压为器件供电，馈入 VO 引脚。

在恒流(CC)工作期间，当输出电压降低时，器件将直接从次级绕组自行供电。在初级侧 MOSFET 导通期间，出现于次级绕组的正向电压用于通过 R5 和内部稳压器对去耦电容 C7 充电。当检测到的输出电压低于 3 V 时，电源进入自动重启动。

输出电流通过一个 35 mV 的阈值在 IS 与 GND 引脚之间进行内部检测，用以降低损耗。一旦超过内部电流检测阈值，器件将调节使能的开关周期数以维持固定的输出电流。

低于恒流阈值时，器件在恒压模式下工作。输出电压通过电阻分压器 R8 和 R9 的工作情况进行检测 — 当处于稳压输出电压时，FB 引脚的参考电压为 1.265 V。

5 PCB 布局

PCB 铜线厚度为 2 盎司(2.8 mils / 70 μm)，另有说明者除外。

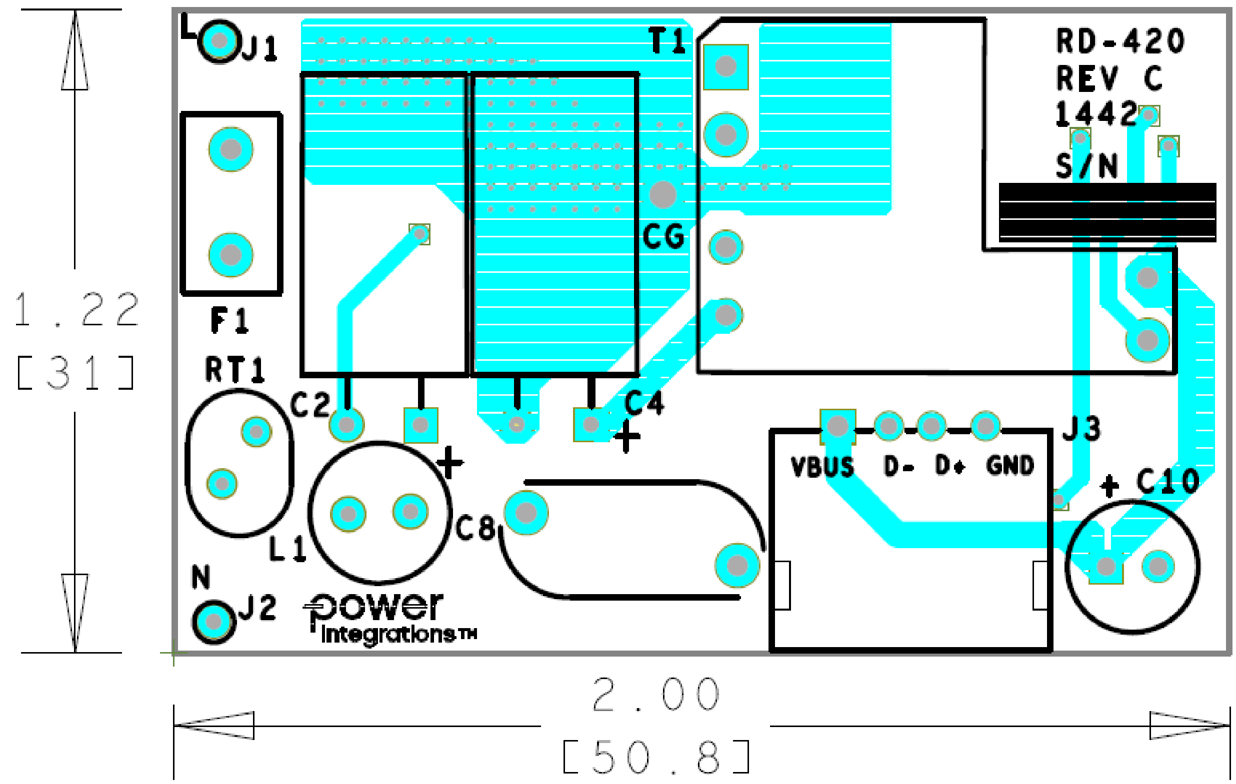

Figure 4 – Printed Circuit Layout, Top.

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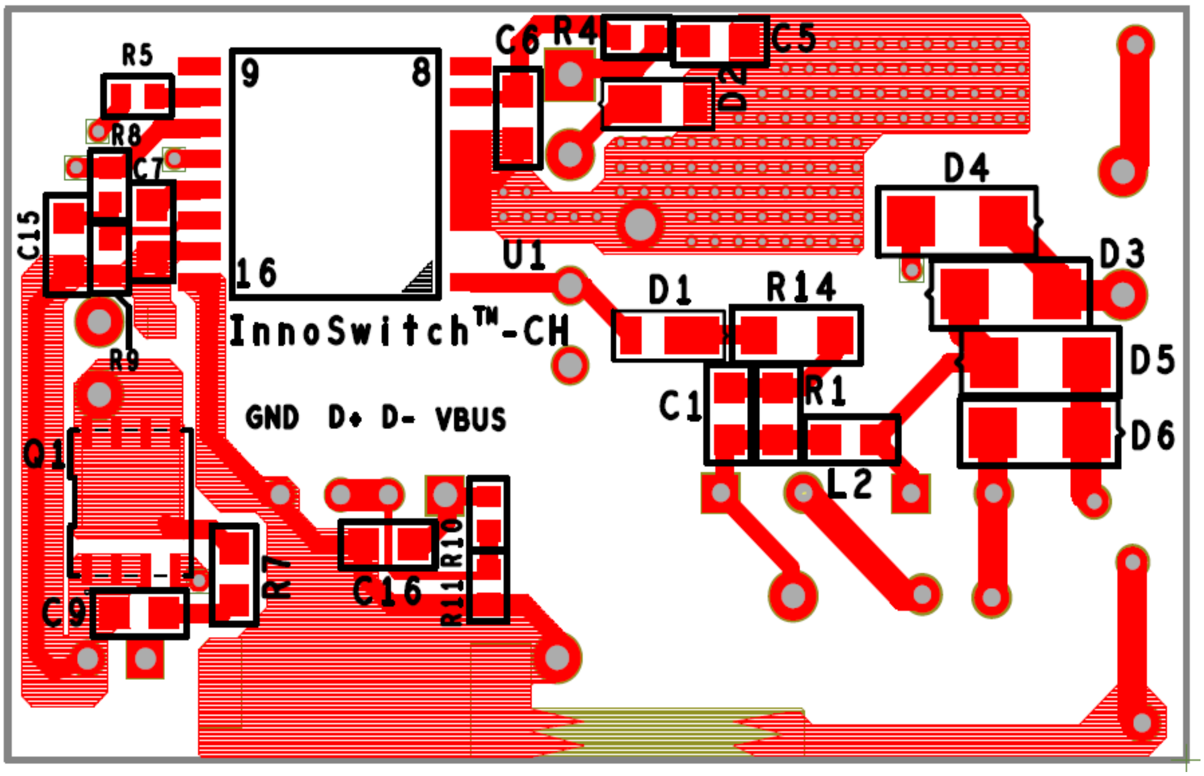

Figure 5 – Printed Circuit Layout, Bottom.

6 物料清单(BOM)

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
2	2	C2 C4	8.2 μF, 400 V, Electrolytic, (8 x 14) 8.2 μF, 400 V, Electrolytic, (8 x 14), Alternate part	400AX8.2M8X16	Capxon Rubycon
3	1	C5	22 μF, 16 V, Ceramic, X5R, 0805	C2012X5R1C226K	TDK
4	1	C6	1 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
5	1	C7	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
6	1	C8	100 pF, Ceramic, Y1	440LT10-R	Vishay
7	1	C9	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
8	1	C10	560 μF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
9	1	C15	100 pF 100 V 10 % X7R 0805	08051C101JAT2A	AVX
10	1	C16	1 μF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
11	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
12	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
13	4	D3 D4 D 5 D6	800 V, 1.5 A, Gen Purpose,SMA 800 V, 1.5 A, Gen Purpose,SMA, Alternate part	S2KA-13-F RS2MA-13-F	Diodes, Inc.Diodes, Inc.
14	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
15	1	J1	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
16	1	J2	Test Point, WHT,Miniature THRU-HOLE MOUNT	5002	Keystone
17	1	J3	Connector USB Female Type A	USB-AF-DIP-094-H	GOLDCONN
18	1	L1	100 μH, 0.490 A, 20%	RL-5480-2-100	Renco
19	1	L2	4.7 μH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
20	1	Q1	60 V, 15 A, N-Channel, PowerPAK SO-8	SI7478DP-T1-E3	Vishay
21	1	R1	200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
22	1	R4	3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
23	1	R5	47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
24	1	R7	20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
25	1	R8	100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
26	1	R9	34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
27	1	R10	330 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ334V	Panasonic
28	1	R11	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
29	1	R14	30 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ300V	Panasonic
30	1	RT1	NTC Thermistor, 10 Ohms, 0.7 A	MF72-010D5	Cantherm
31	1	T1	Custom (see transformer section for material set)	SNX-R1776	Santronics
32	1	U1	InnoSwitch-CH IC eSOP-R16B	INN2023K	Power Integrations

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7 变压器规格

7.1 *电气原理图*

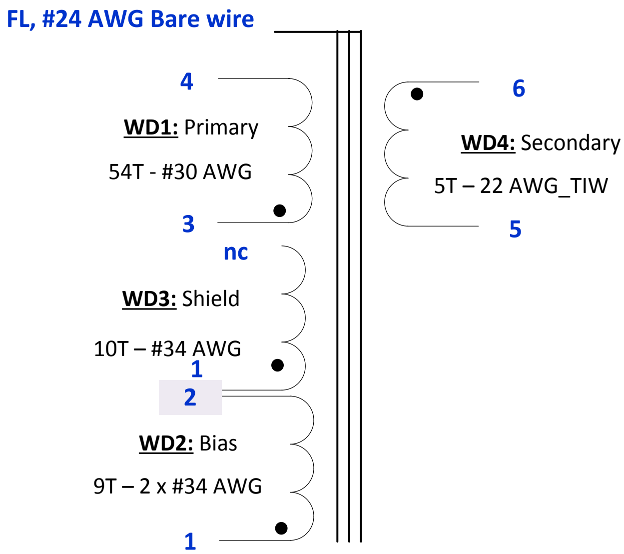

Figure 6– Transformer Electrical Diagram.

7.2 *电气规格*

Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	546µH ±5%
Resonant Frequency	Pins 3-4, all other windings open.	1500 kHz (min)
Primary Leakage Inductance	Pins 3-4, with pins 5-6 shorted, measured at 100 kHz, 0.4 V_{RMS}.	25 µH (max)

7.3 *材料*

Item	Description
[1]	Core: EE1621; PC-40 or equivalent.
[2]	Bobbin: EE1621-Vertical – 8pins (4/4) Shen Zhen Xin Yu Jia Technology Ltd.
[3]	Magnet Wire: #30 AWG, double coated.
[4]	Magnet Wire: #34 AWG, double coated.
[5]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mil thick, 5.5 mm wide.
[7]	Epoxy: Devcon, 5 Minute Epoxy, No. 14210; or equivalent.
[8]	Bus wire: #24 AWG, Belden Electronics Div; or equivalent.
[9]	Varnish: Dolph BC-359.

7.4 *变压器结构图*

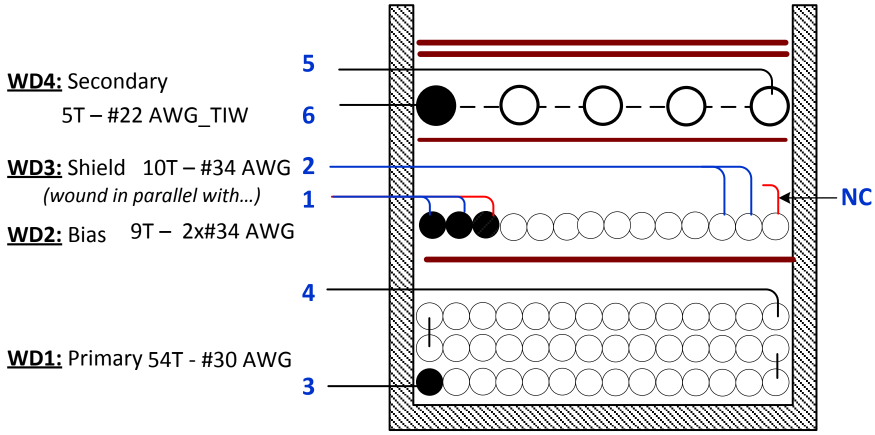

Figure 7– Transformer Build Diagram.

7.5 *变压器构建说明*

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4.
Insulation	1 layer of tape [6] for insulation.
WD2 & WD3 Bias & Shield	Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3rd wire 1 more turn and left no-connect for WD3.
Insulation	1 layer of tape [6] for insulation.
WD4 Secondary	Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5.
Insulation	2 Layer of tape [6] to secure the windings.
Finish	Gap core halves for 546μH inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration below). Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9].

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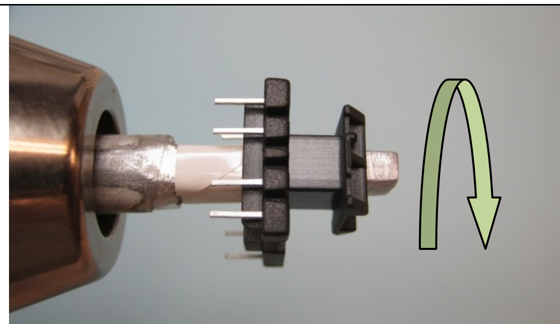
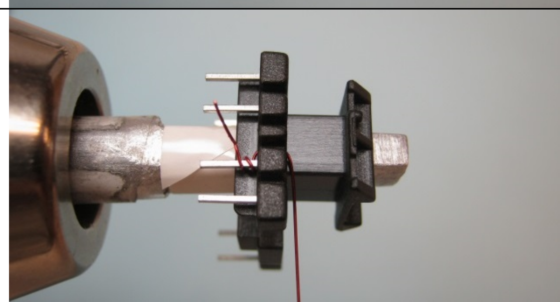
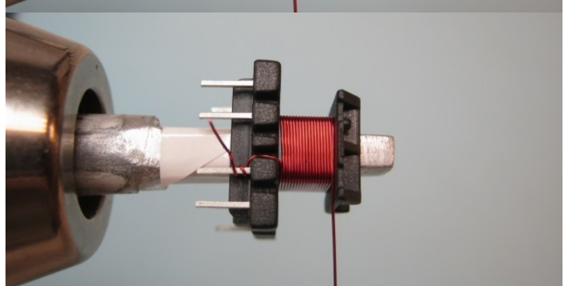
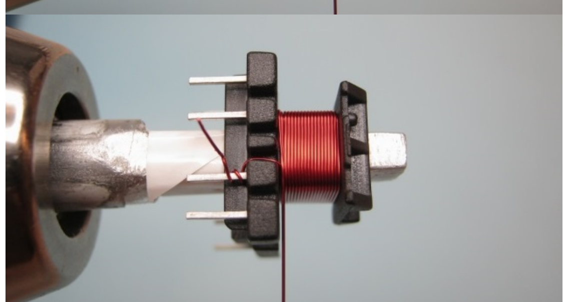
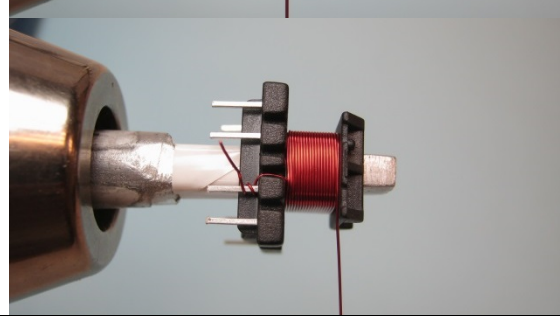
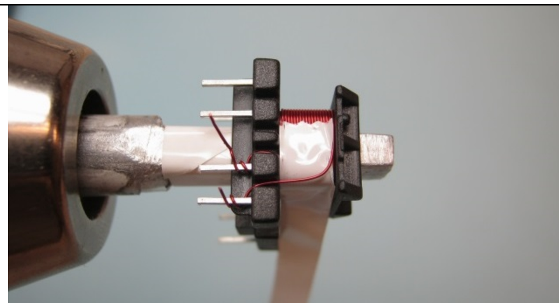
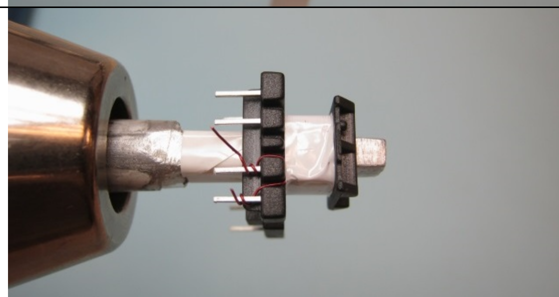
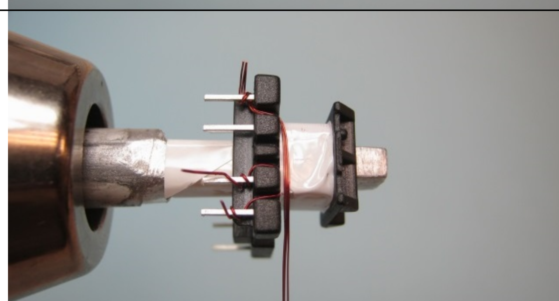
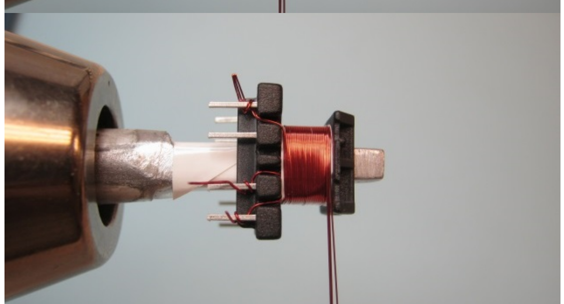
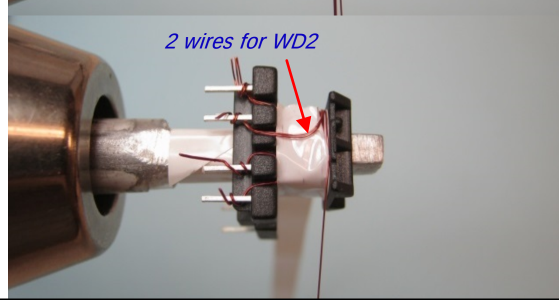
7.6 *变压器绕制演示*

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**		Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4.

		
Insulation		1 layer of tape [6] for insulation.
WD2 & WD3 Bias & Shield	  	Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3rd wire 1 more turn and left no-connect for WD3.

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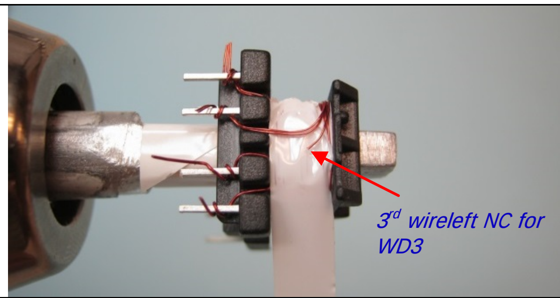
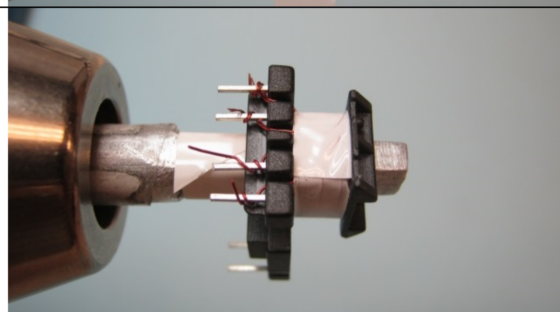
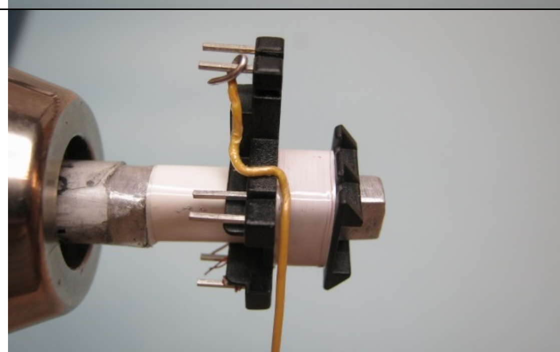
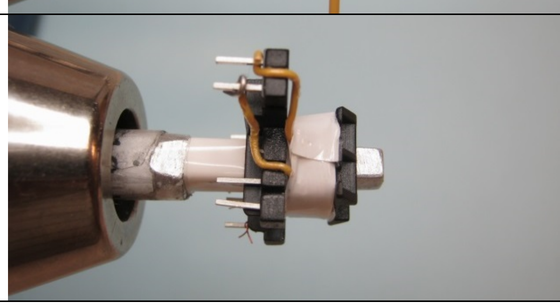
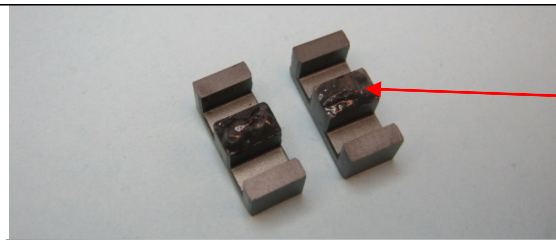
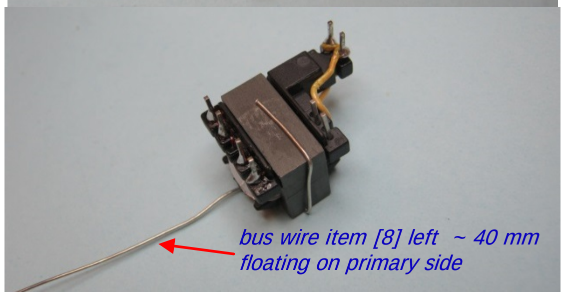
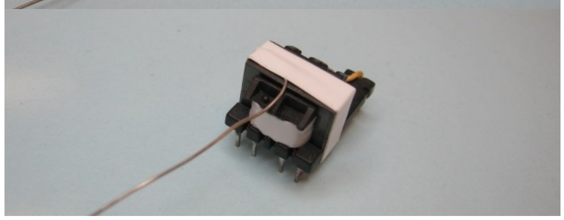
		
Insulation		1 layer of tape [6] for insulation.
WD4 Secondary	 	Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5.
Insulation		2 layer of tape [6] to secure the windings.

Finish	  	Gap core halves for 546µH inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration beside). Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9].

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8 变压器设计表格

ACDC_InnoSwitch-CH_101614; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch_101614_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	5.00		5.00	V	Output Voltage (continuous power at the end of the cable)
IO	2.00		2.00	A	Power Supply Output Current (corresponding to peak power)
Power			10.6	W	Continuous Output Power, including cable drop compensation
n	0.82		0.82		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	16.40	Info	16.40	uFarad	!!! Input capacitor is too small. Recommnded to increase CIN above 19.05 uF to ensure VMIN>70 V
ENTER InnoSwitch VARIABLES					
InnoSwitch-CH	INN20x3		INN20x3		User defined InnoSwitch
Cable drop compensation	6%		6%		Select Cable Drop Compensation option
Complete Part Number			INN2023 K		Final part number including package
Chose Configuration	INC		Increased Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.682	A	Minimum Current Limit
ILIMITTYP			0.75	A	Typical Current Limit
ILIMITMAX			0.818	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			47.25	A^2kHz	Worst case I2F parameter across the temperature range
VOR	58		58	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.80		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.46		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			9.32	V	Bias Winding Number of Turns
PIVB			102.59	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	Custom		Custom		Enter Transformer Core
Core	EE1621		EE1621		Enter core part number, if necessary
Bobbin			0		Enter bobbin part number, if necessary
AE	0.325		0.325	cm^2	Core Effective Cross Sectional Area
LE	3.93		3.93	cm	Core Effective Path Length
AL	2800		2800	nH/T^2	Ungapped Core Effective Inductance
BW	5.40		5.40	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary

					Creepage Distance)
L	3		3		Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	62	Warning	62	V	!!! Minimum DC Input Voltage < 70 Volts. Increase VACMIN or increase CIN
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.21	A	Average Primary Current
IP			0.682	A	Peak Primary Current assuming ILIMITMIN
IR			0.546	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.31	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			546	uHenry	Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 518 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			54		Primary Winding Number of Turns
ALG			187	nH/T^2	Gapped Core Effective Inductance
BM			2868	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1147	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2694		Relative Permeability of Ungapped Core
LG			0.20	mm	Gap Length (Lg> 0.1 mm)
BWE			16.2	mm	Effective Bobbin Width
OD			0.30	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.25	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			259	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			7.37	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			3.33	A	Secondary RMS Current
IRIPPLE			2.67	A	Output Capacitor RMS Ripple Current
CMS			667	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			517	V	Maximum Drain Voltage Estimate
PIVS			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.30	V	Main Output Voltage directly after output rectifier
IO1			2.00	A	Output DC Current
PO1			10.60	W	Output Power
VD1			0.06	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			5.00	Turns	Output Winding Number of Turns
ISRMS1			3.33	A	Output Winding RMS Current
IRIPPLE1			2.67	A	Output Capacitor RMS Ripple Current
PIVS1			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming

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					the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			QM6006		Recommended SR FET for this output
RDSON_HOT			0.027	Ohm	RDSon at 100C
VRATED			60	V	Rated voltage of selected SR FET
CMS1			667	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.08	mm	Maximum Outside Diameter for Triple Insulated Wire

9 性能数据

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

9.1 *带载模式效率（USB 插口处）相对于输入电压的变化*

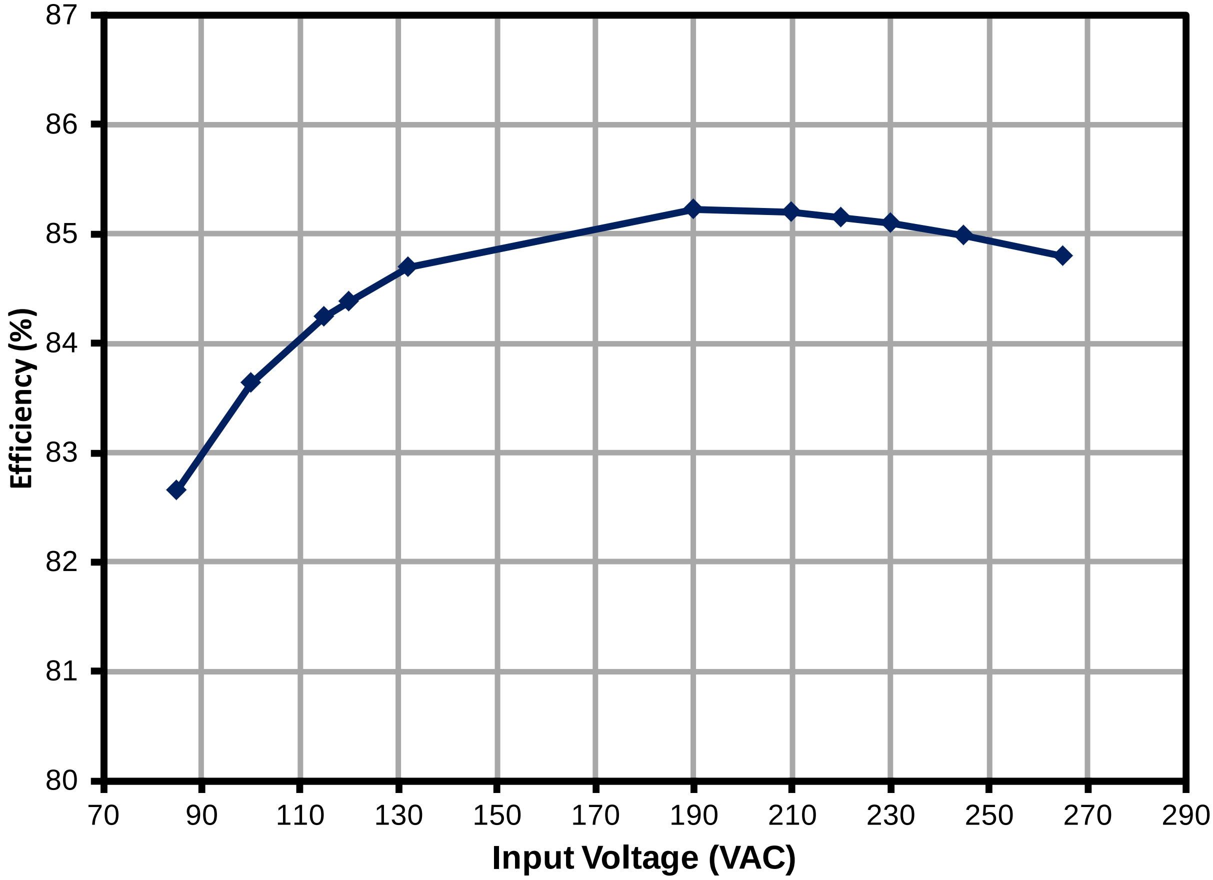

Figure 8– Efficiency vs Line Voltage, Room Temperature

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9.2 *带载模式效率（USB 插口处）相对于负载的变化*

9.2.1 未使用与 Q1, SR FET 并联的肖特基二极管时的效率

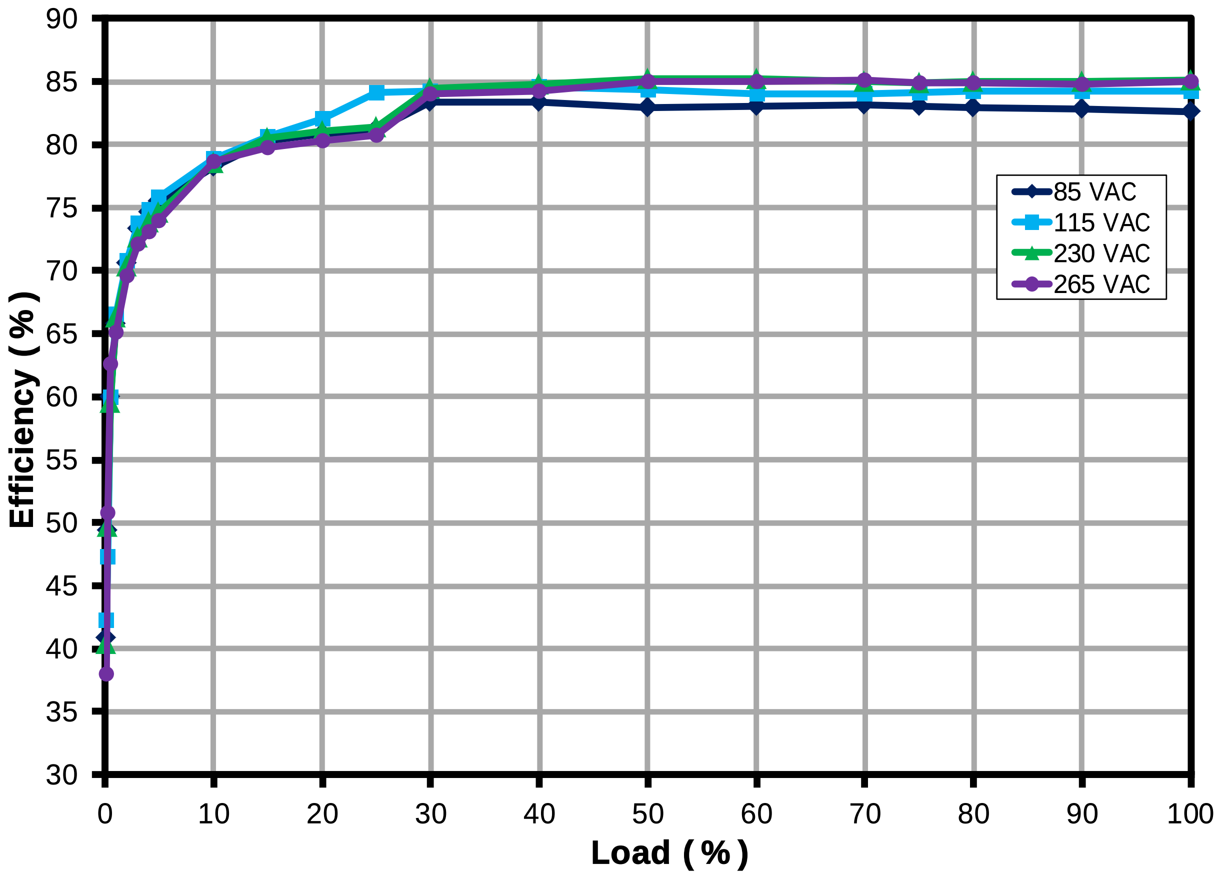

Figure 9– Efficiency vs Load, Room Ambient

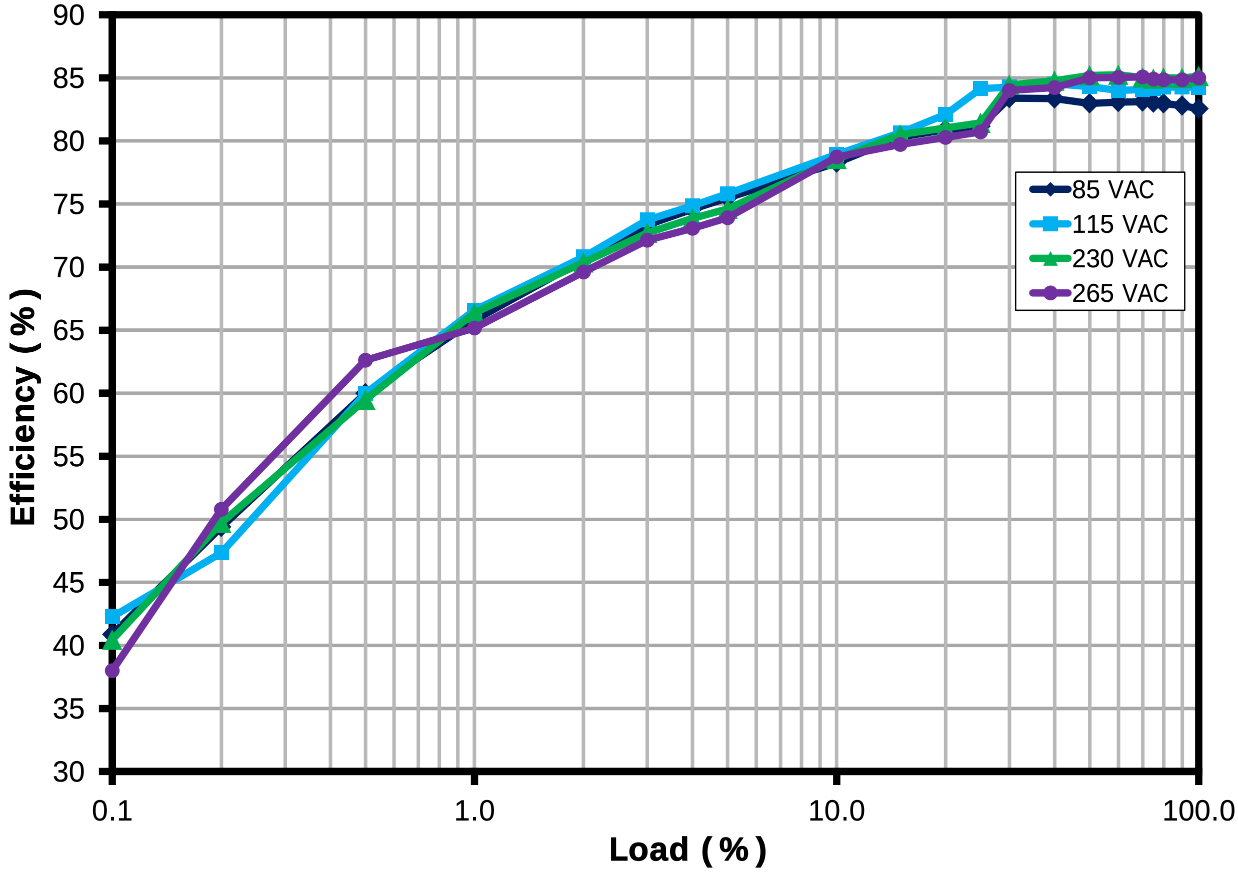

Figure 10 - Efficiency vs Load (log scale to demonstrate light load performance)

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9.2.2 使用与 Q1, SR FET 并联的肖特基二极管(SS16)时的效率

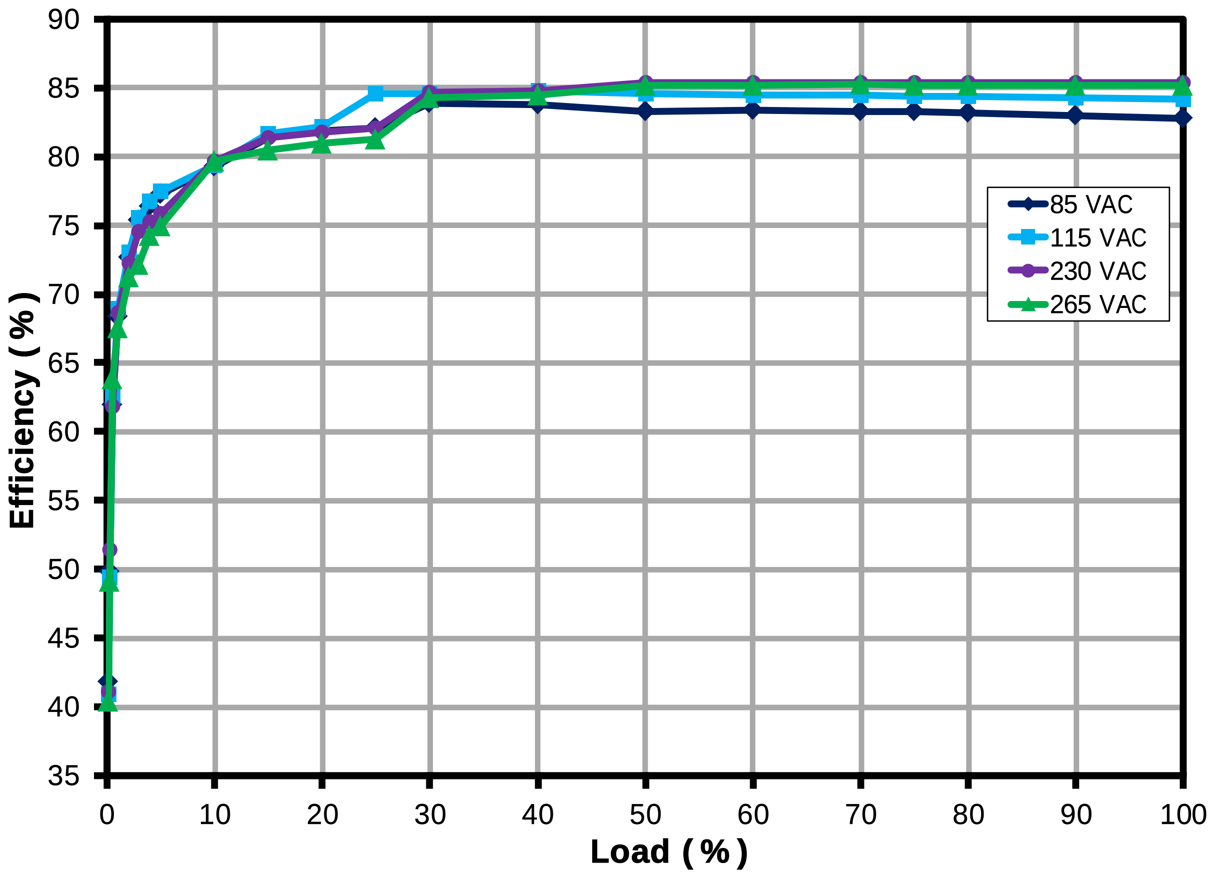

Figure 11– Efficiency vs Load, Room Temperature, 60 Hz.

9.3 *空载输入功率*

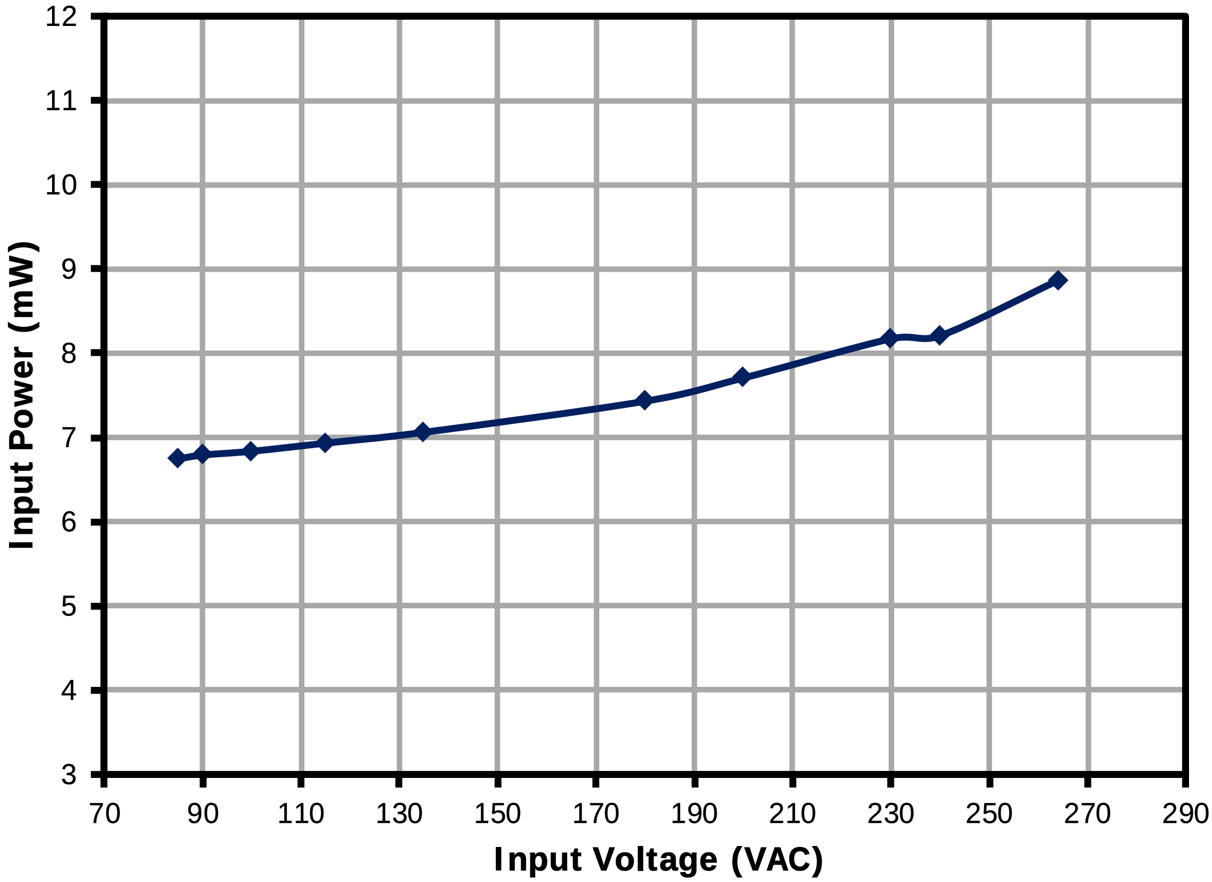

Figure 12– No Load Input Power vs. Input Line Voltage, Room Temperature.

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9.4 平均效率（USB 插口处）

9.4.1 效率要求

Test	Average	Average	Average	Average	10% Load	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
Effective	Now	2016	Now	2016	Now	2016
Power [W]	Energy Star 2	New IESA2007	CoC v5 Tier 1	CoC v5 Tier 2	CoC v5 Tier 1	CoC v5 Tier 2
10%	74.2%	78.7%	76.0%	79.0%	66.6%	69.7%

9.4.2 115 VAC 输入下的平均效率

9.4.2.1 未使用与 Q1, SR FET 并联的肖特基二极管

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	% ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	114.98	0.19	12.473	0.566	131	5.2575	1.999	10.509	84.26	
75	114.98	0.15	9.255	0.542	144.4	5.1950	1.499	7.789	84.16	
50	114.99	0.10	6.078	0.505	163.5	5.1300	0.999	5.124	84.30	
25	114.99	0.06	3.001	0.449	194.8	5.0550	0.500	2.525	84.14	**84.21**
10	114.99	0.03	1.266	0.392	231.7	5.0100	0.199	0.999	**78.94**	

9.4.2.2 肖特基二极管(SS16)与 Q1, SR FET 并联

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	% ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	114.98	0.19	12.492	0.572	129.4	5.2588	1.999	10.511	84.15	
75	114.99	0.15	9.230	0.544	143.5	5.1963	1.499	7.791	84.41	
50	114.99	0.10	6.060	0.508	162.6	5.1325	0.999	5.125	84.58	
25	114.99	0.06	2.987	0.452	193.4	5.0563	0.500	2.526	84.55	**84.42**
10	114.99	0.03	1.259	0.392	231.1	5.0113	0.199	0.999	**79.36**	

9.4.3 230 VAC 输入下的平均效率

9.4.3.1 未使用与 Q1, SR FET 并联的肖特基二极管

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	230.04	0.12	12.364	0.450	195.1	5.2663	1.999	10.527	85.14	
75	230.04	0.09	9.179	0.426	209.4	5.2000	1.499	7.797	84.94	
50	230.04	0.07	6.021	0.397	228.4	5.1363	0.999	5.130	85.20	
25	230.04	0.04	3.097	0.358	258.7	5.0488	0.500	2.522	81.43	**84.18**
10	230.04	0.02	1.273	0.312	300.9	5.0150	0.199	1.000	**78.56**	

9.4.3.2 肖特基二极管(SS16)与 Q1, SR FET 并联

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	230.04	0.12	12.329	0.449	195.6	5.2663	1.999	10.527	85.38	
75	230.04	0.09	9.133	0.425	210	5.2000	1.499	7.796	85.36	
50	230.04	0.07	6.007	0.397	229.2	5.1363	0.999	5.129	85.39	
25	230.04	0.04	3.073	0.357	259.5	5.0488	0.500	2.522	82.06	**84.55**
10	230.04	0.02	1.255	0.312	301.7	5.0150	0.199	1.000	**79.68**	

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9.5 ***在电缆末端测得的 CV/CC 调整***

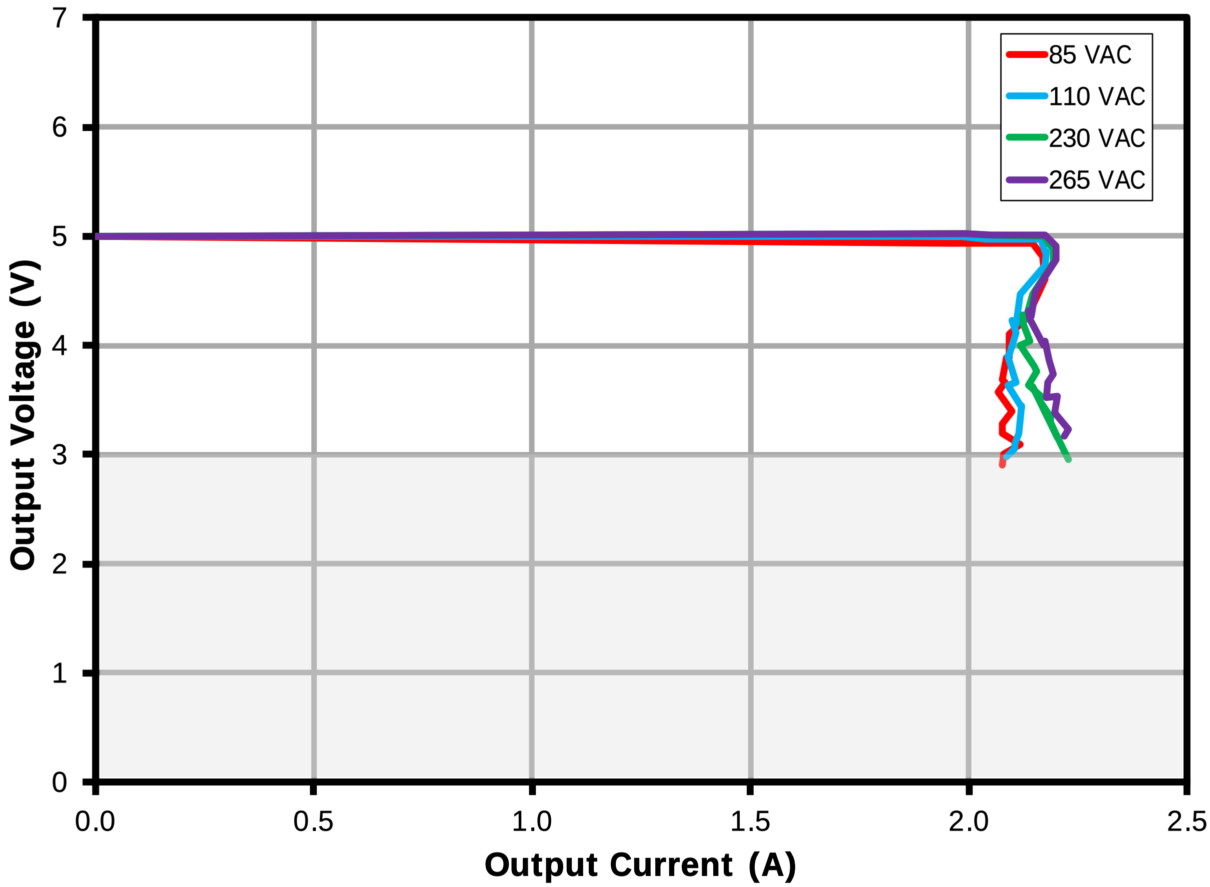

Figure 13– Output Voltage vs, Output current, Room Temperature.

10 敞开式外壳热性能

Room ambient.

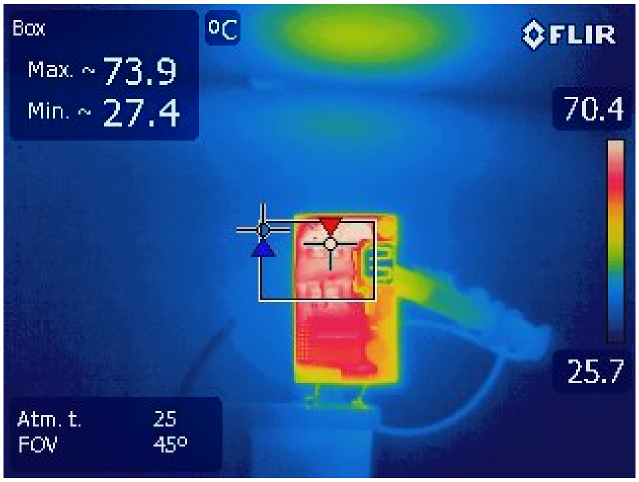

Figure 14– Transformer Side.
85 VAC, 2 A Load.
Ambient = 26.3 ºC.

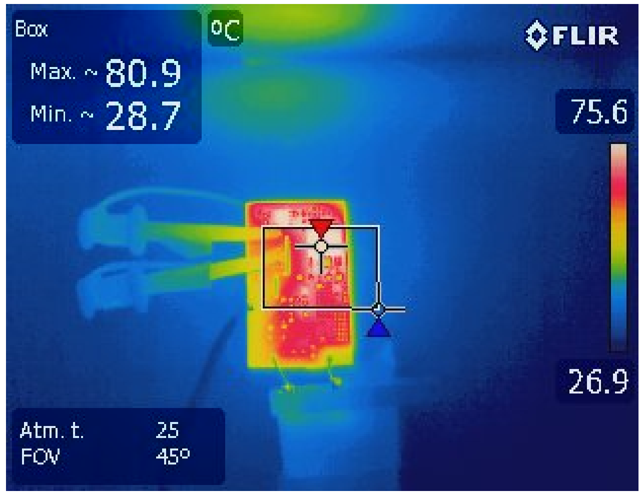

Figure 15– InnoSwitch-CH Side.
85 VAC, 2 A Load.
Ambient = 27 ºC.

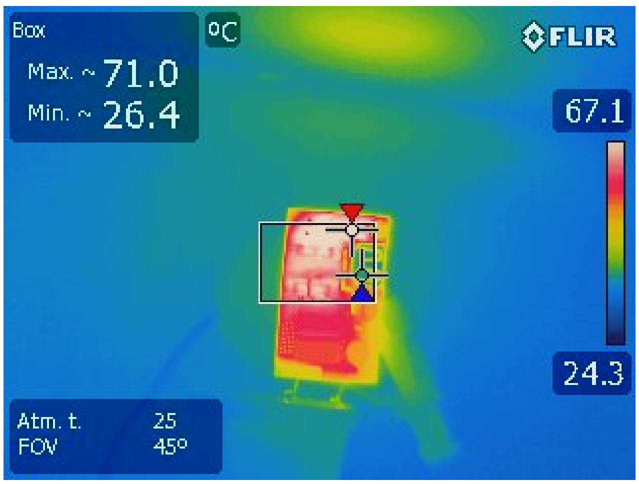

Figure 16– Transformer Side.
110 VAC, 2 A Load.
Ambient = 26.2 ºC.

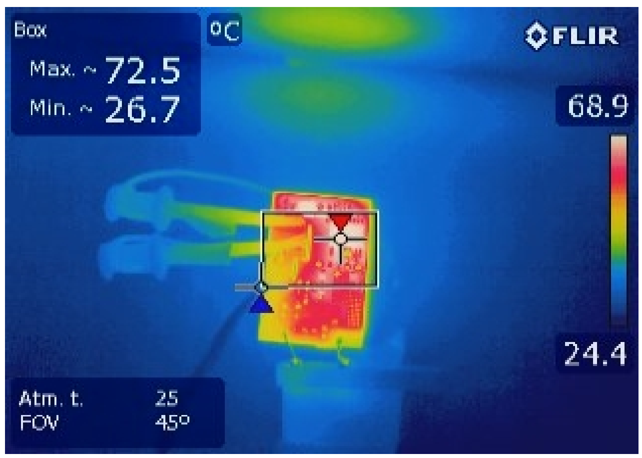

Figure 17– InnoSwitch-CH Side.
110 VAC, 2 A Load.
Ambient = 25 ºC.

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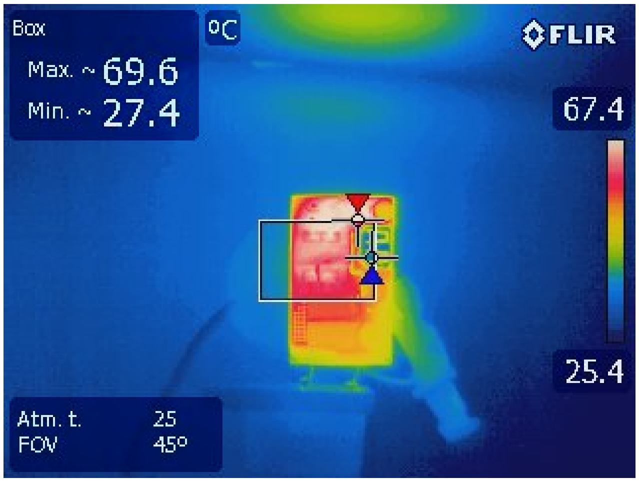

Figure 18– Transformer Side.
230 VAC, 2 A Load.
Ambient = 26.5 ºC.

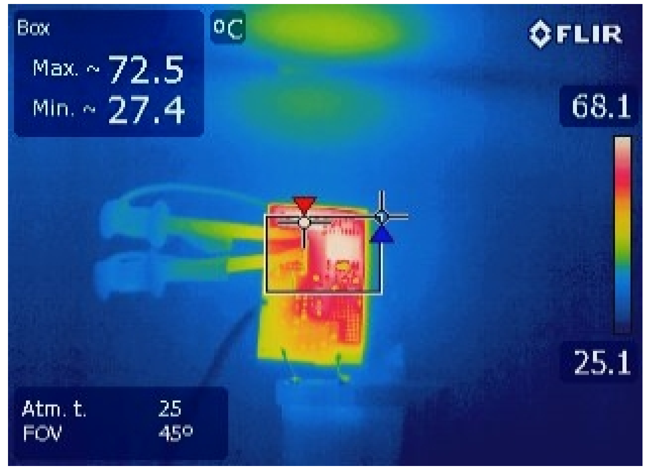

Figure 19– InnoSwitch-CH Side.
230 VAC, 2 A Load.
Ambient = 25.4 ºC.

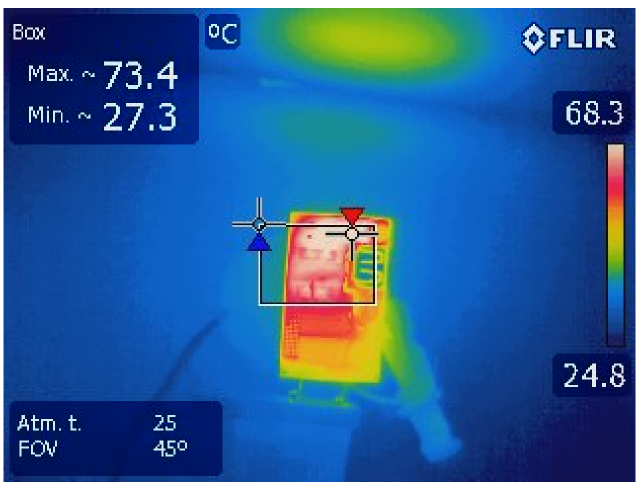

Figure 20– Transformer Side.
265 VAC, 2 A Load.
Ambient = 26.5 ºC.

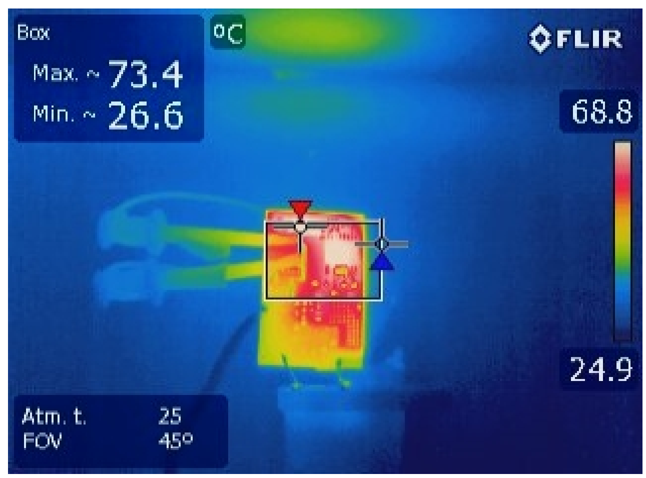

Figure 21– InnoSwitch-CH Side.
265 VAC, 2 A Load.
Ambient = 25.3 ºC.

11 波形

11.1 *负载瞬态响应（电缆末端）*

Results were measured with 47 µF at end of cable which is the typical specified measurement condition for mobile phone chargers.

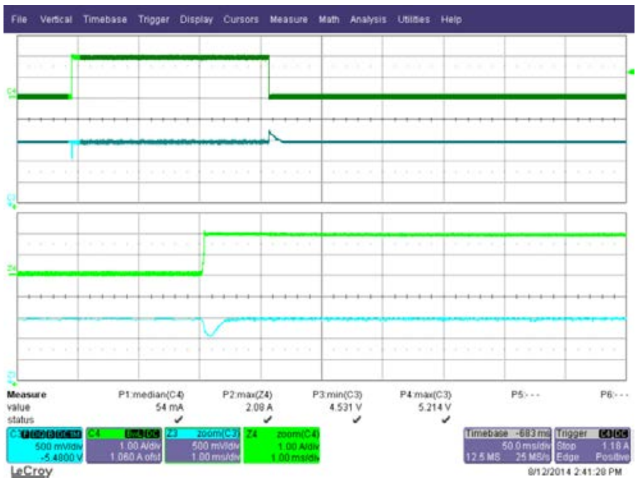

Figure 22– Transient Response (4.5 V_{MIN}).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

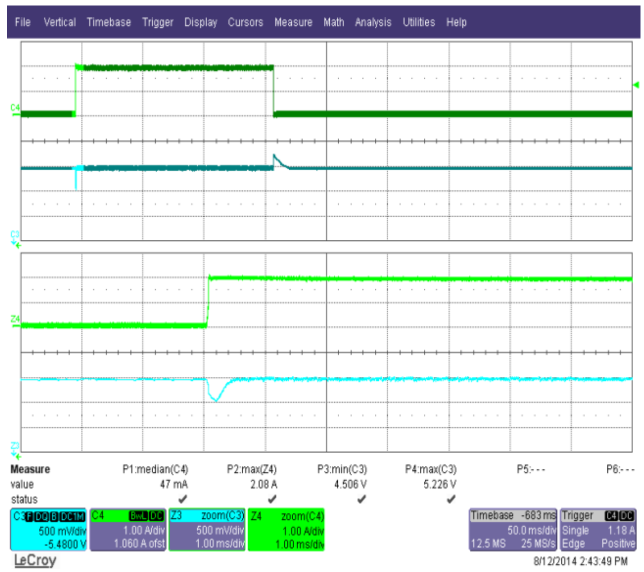

Figure 23– Transient Response (4.5 V_{MIN}).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

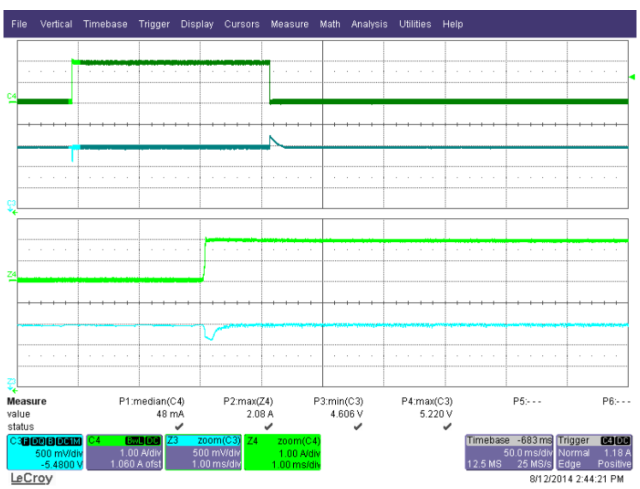

Figure 24– Transient Response (4.6 V_{MIN}).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.

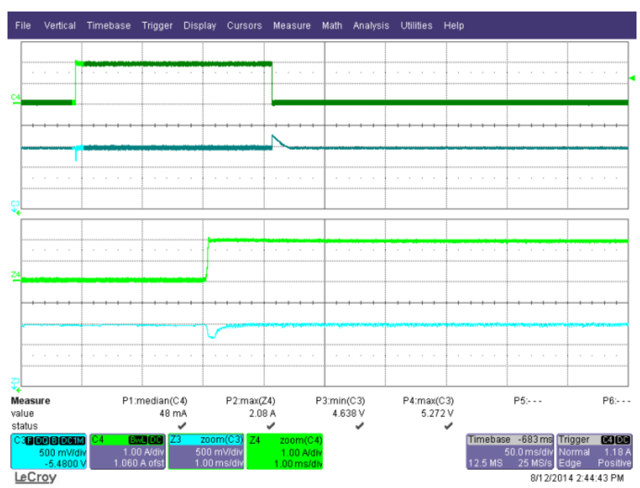

Figure 25– Transient Response (4.6 V_{MIN}).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.

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Lower: V_{OUT}, 500 mV, 50 ms / div.

Lower: V_{OUT}, 500 mV, 50 ms / div.

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11.2 *负载瞬态响应（USB 插口处）*

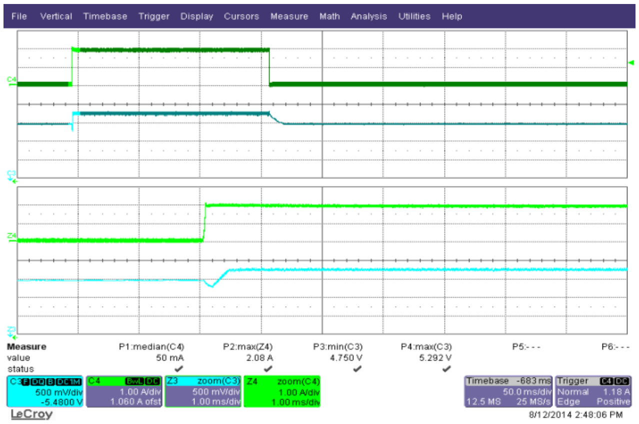

Figure 26– Transient Response (4.75 V_{MIN}).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

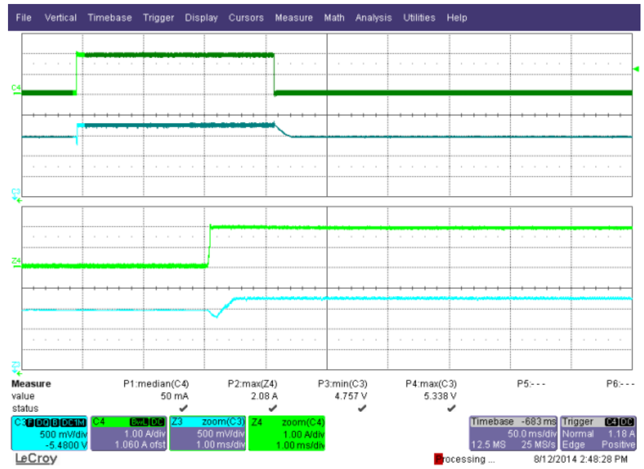

Figure 27– Transient Response (4.75 V_{MIN}).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

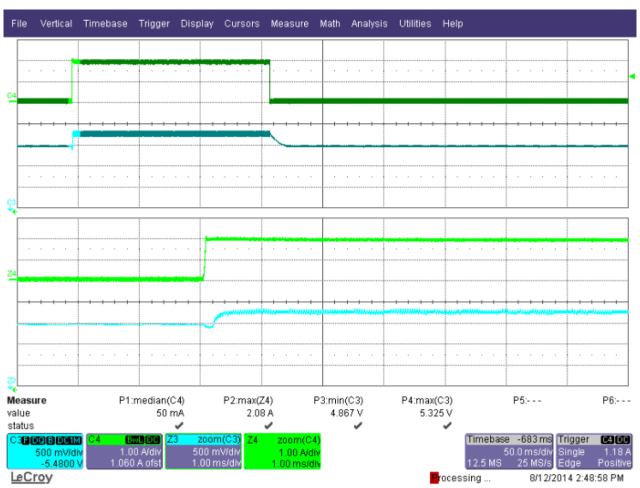

Figure 28– Transient Response (4.85 V_{MIN}).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

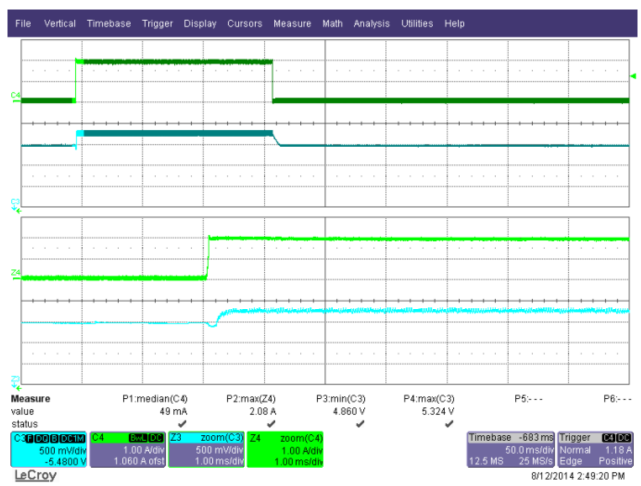

Figure 29– Transient Response (4.86 V_{MIN}).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A /div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

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11.3 *开关波形*

11.3.1 InnoSwitch-CH 波形

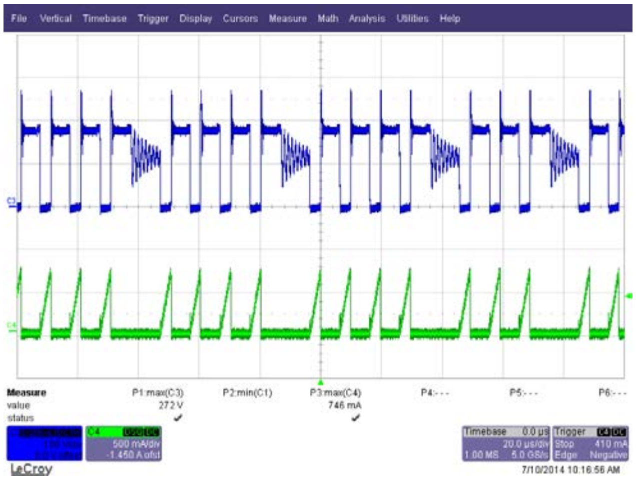

Figure 30– Drain Voltage and Current Waveforms.
85 VAC, 2 A load,
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 100 V, 20 µs / div.

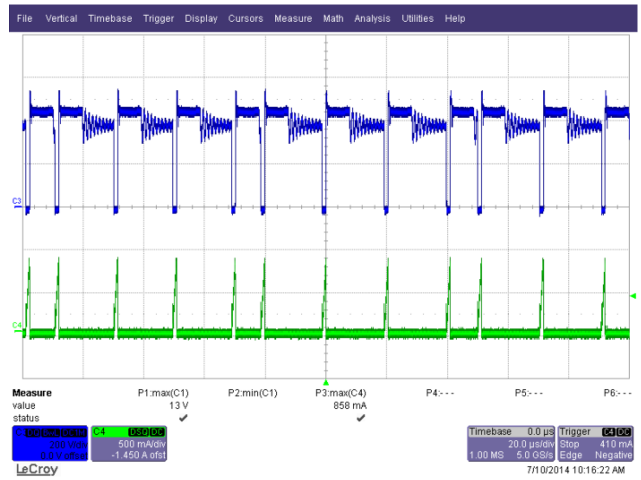

Figure 31– Drain Voltage and Current Waveforms.
265 VAC, 2 A Load, 545 V_{MAX}.
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 20 µs / div.

11.3.2 SR FET 波形

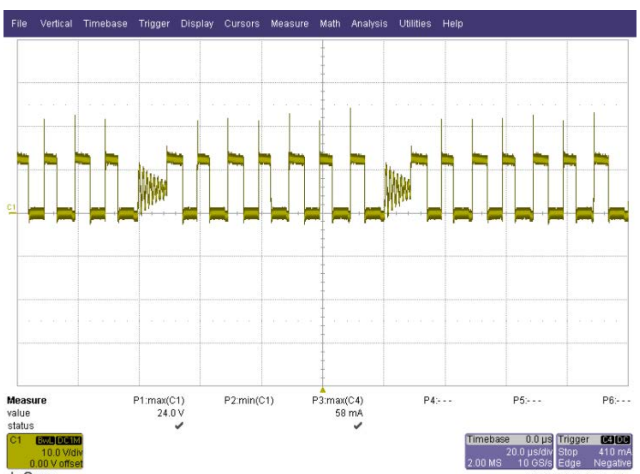

Figure 32– SR FET Voltage Waveforms.
85 VAC Input, 2 A Load.
V_{DRAIN}, 10 V, 20 µs / div.

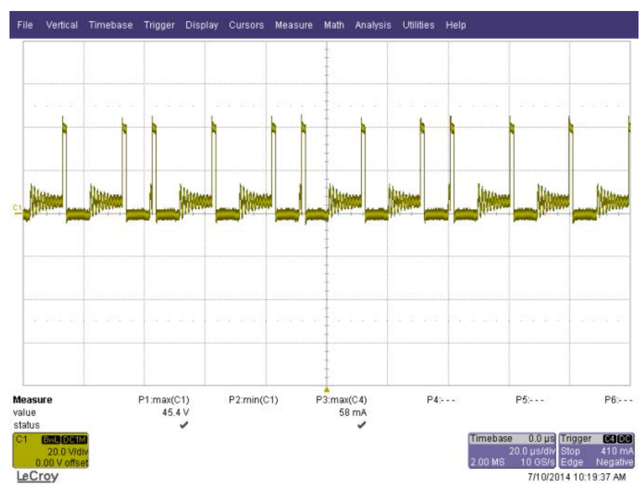

Figure 33– SR FET Voltage Waveforms.
265 VAC Input, 2 A Load.
V_{DRAIN}, 20 V, 20 µs / div. (45.4V_{MAX}).

11.4 *输出纹波测量*

11.4.1 纹波测量方法

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

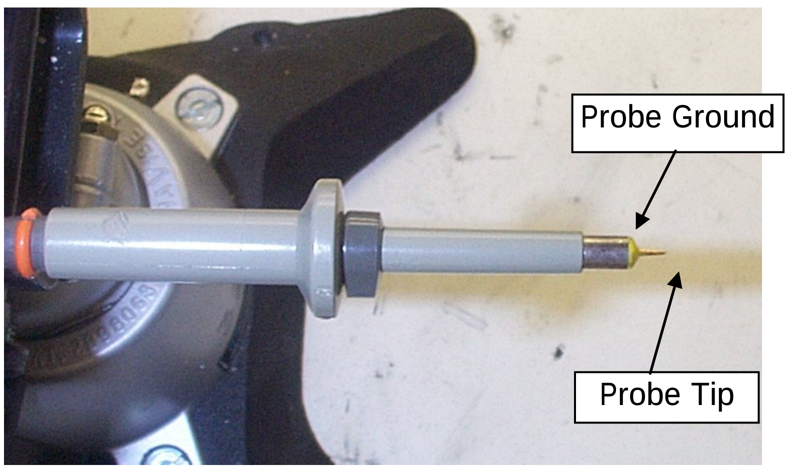

Figure 34– Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 35– Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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11.4.2 测量结果

Measured at the end of cable.

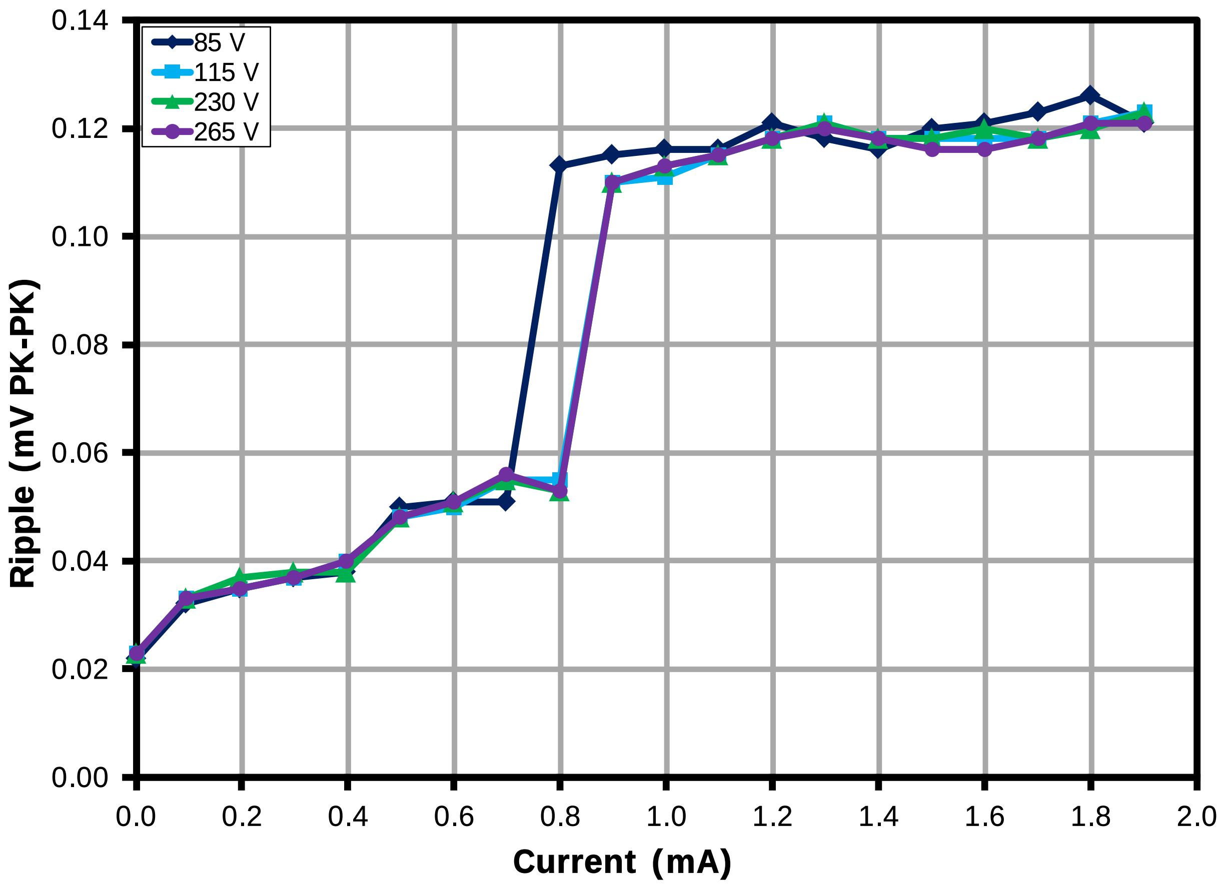


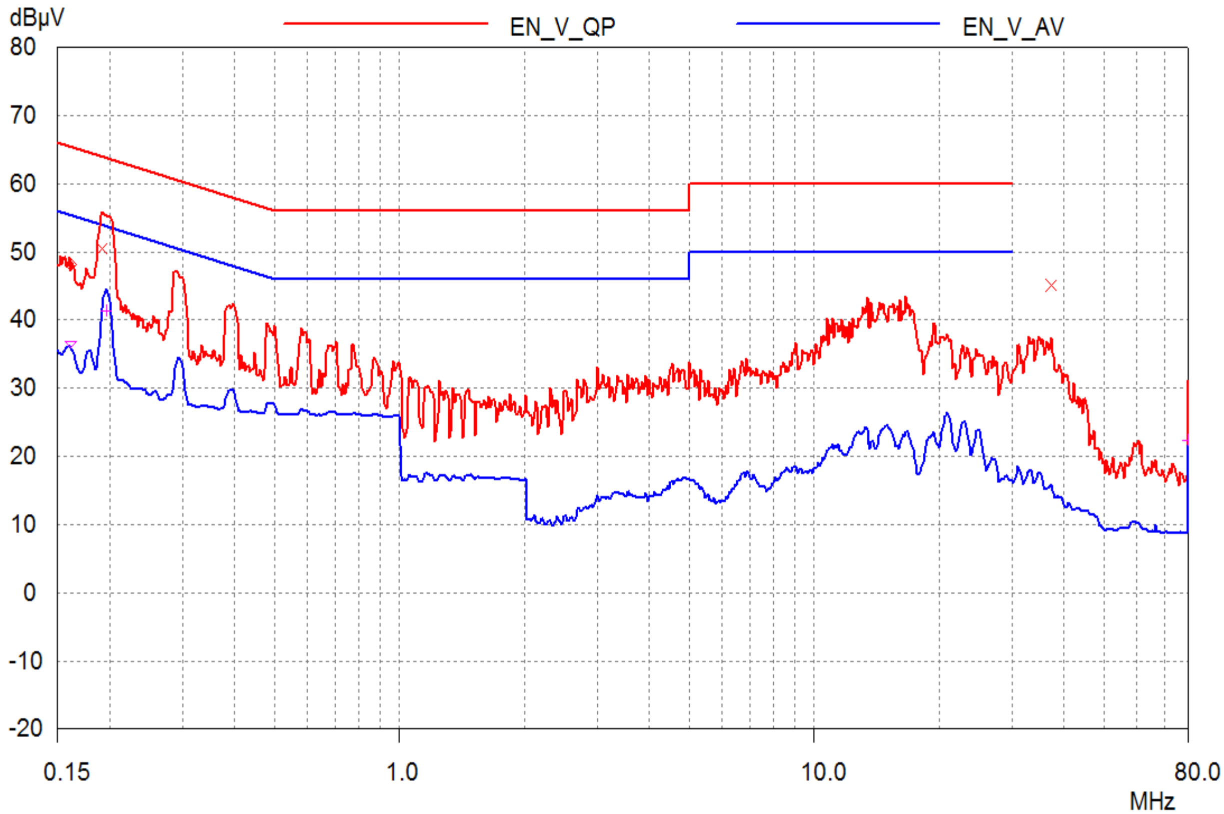
Figure 36–Output Ripple Voltage.

RIPPLE (mV PK-PK) 85 V	RIPPLE (mV PK-PK) 115 V	RIPPLE (mV PK-PK) 230 V	RIPPLE (mV PK-PK) 265 V
0.126	0.123	0.123	0.121

12 传导 EMI

12.1 *2 A 电阻性负载，浮动输出(PK / AV)*

After running 5 minutes.



Freq (MHz)	QP	Limit	Margin
0.19	50.48	63.95	13.47

Figure 37–Floating Ground EMI at 115 VAC.

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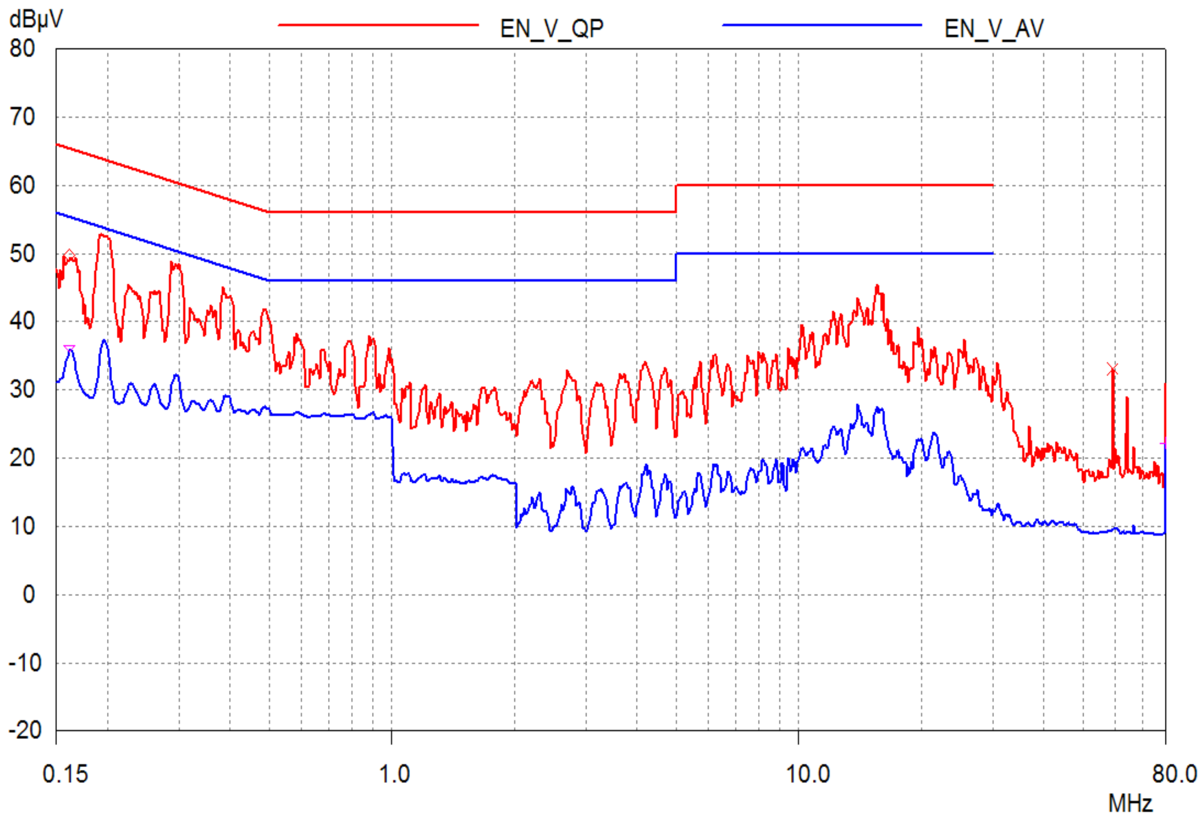
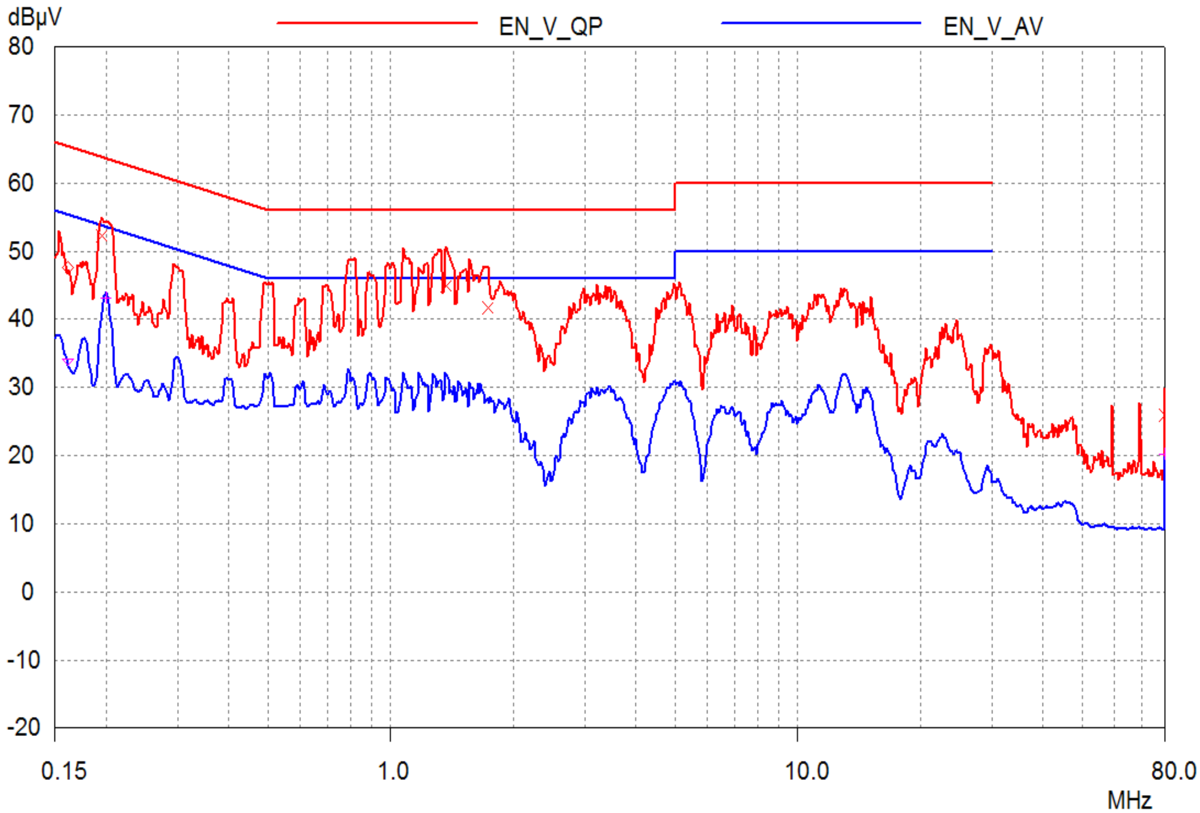


Figure 38–Floating Ground at 230 VAC.

12.2 *2 A 电阻性负载，假手接地(PK / AV)*



FREQ (MHZ)	QP	LIMIT	MARGIN
0.20	52.26	63.82	11.56
1.37	44.97	56	11.03
1.73	41.65	56	14.35

Figure 39–Artificial Ground at 115 VAC.

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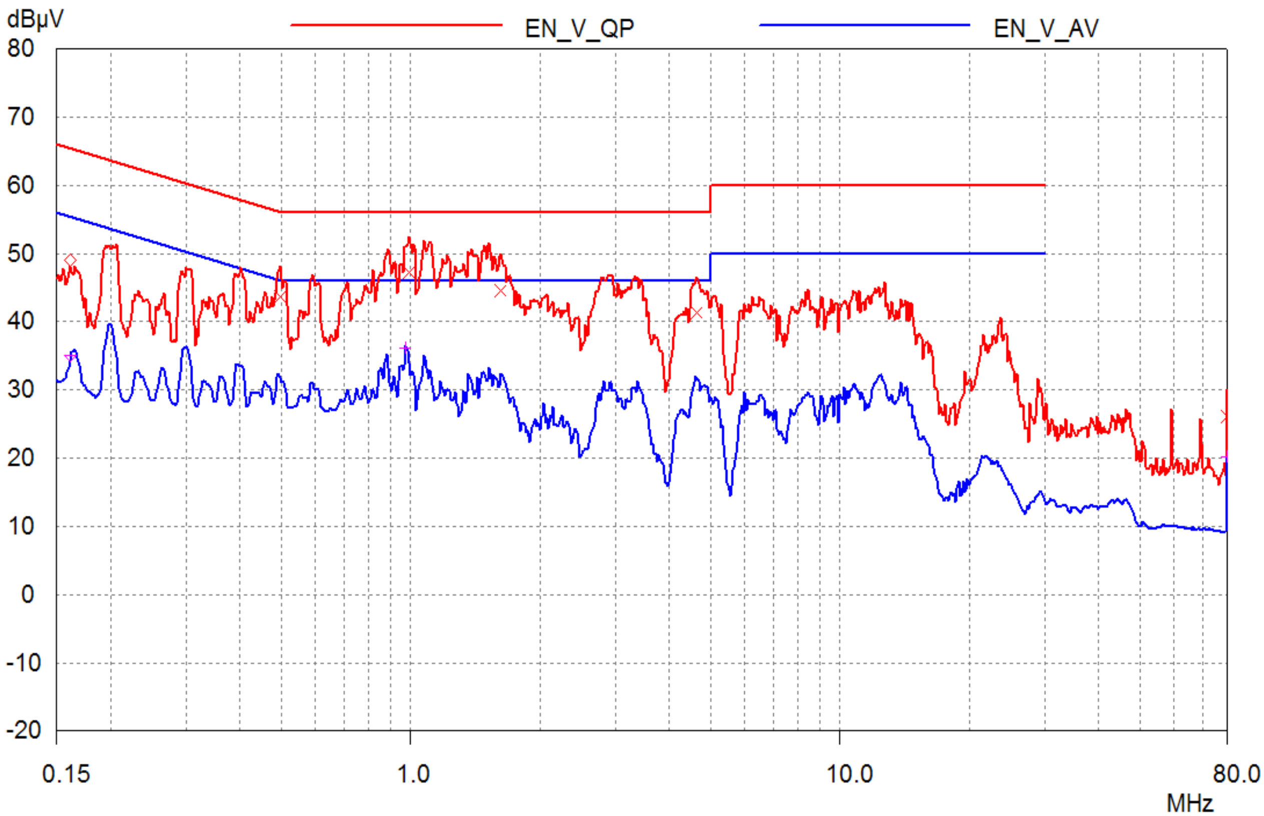

FREQ (MHZ)	QP	LIMIT	MARGIN
0.50	43.6	56.07	12.47
0.99	47.3	56	8.7
1.62	44.51	56	11.49
4.65	41.37	56	14.63

Figure 40–Artificial Ground at 230 VAC.

12.3 *连接显示器的智能手机(HDMI) (QP / AV)*

Phone is connected to charger and LCD monitor. The monitor connection increases capacitance to earth ground.

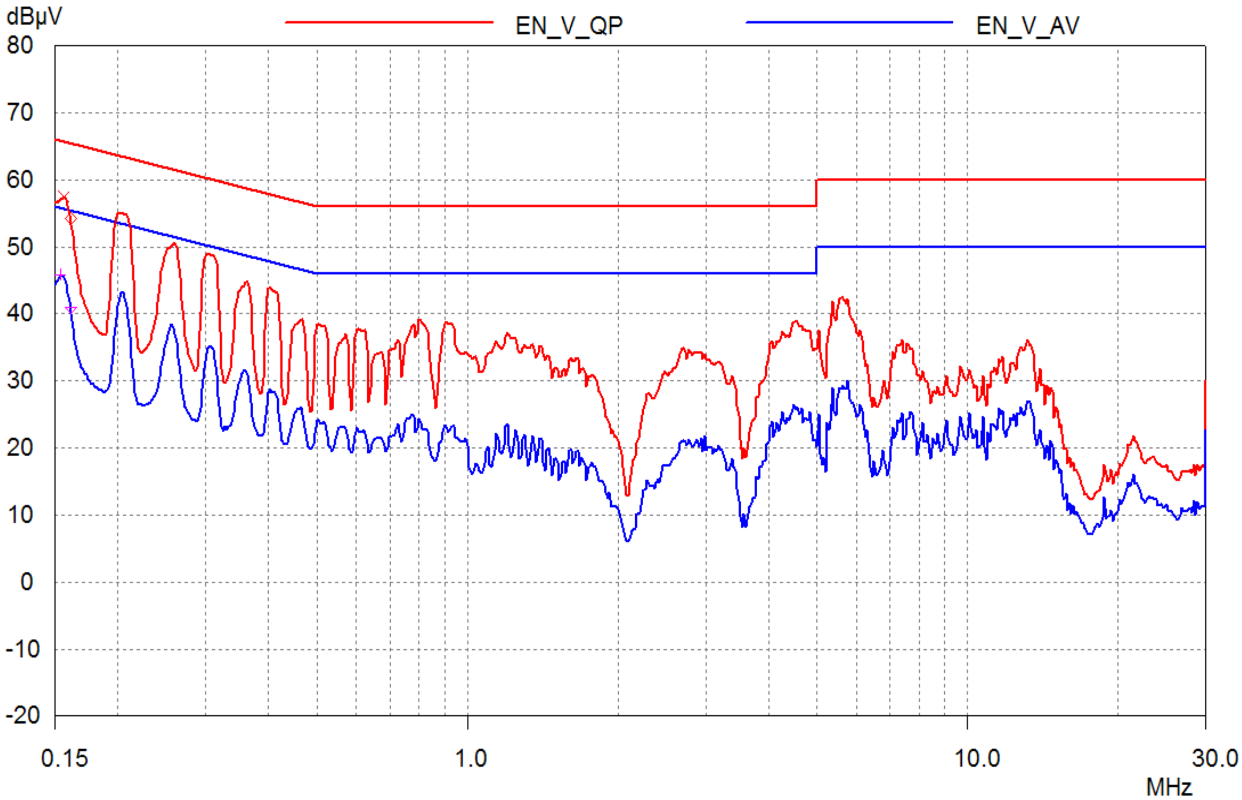

Figure 41–HDMI at 115 VAC.

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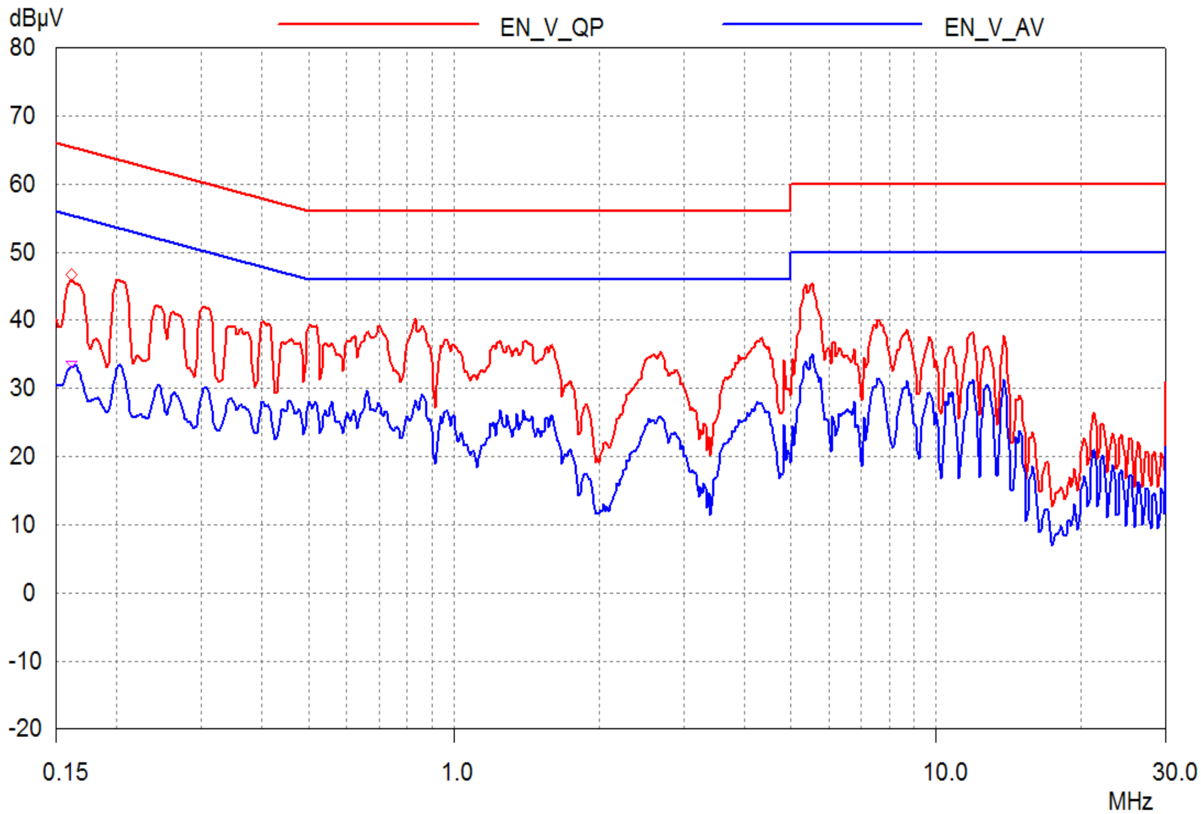
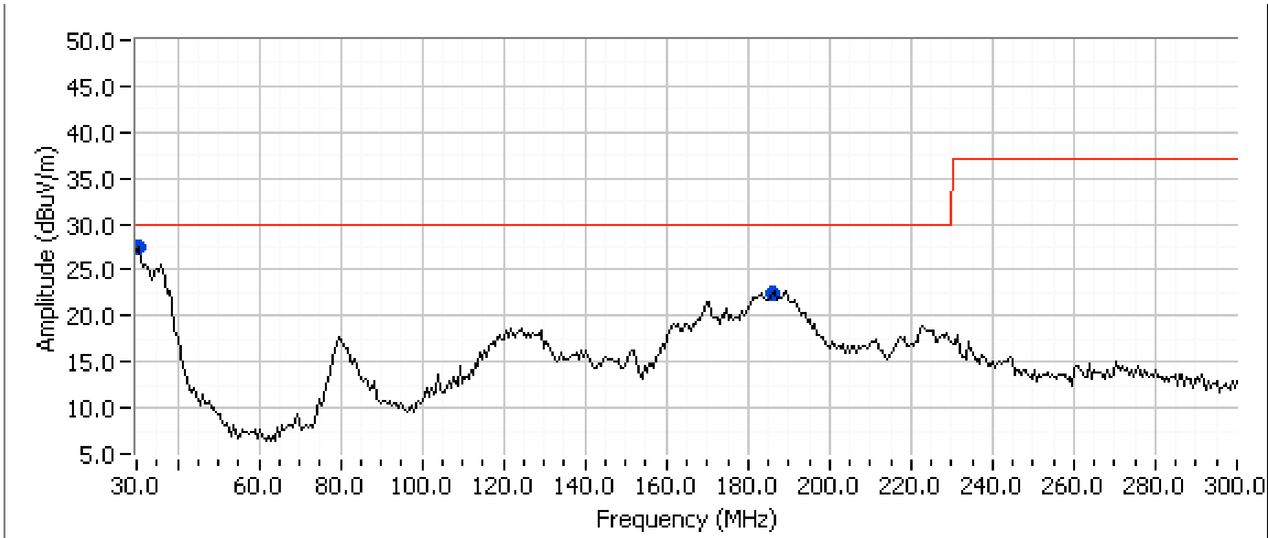


Figure 42–HDMI at 230 VAC**.**

13 辐射 EMI



Maximized quasi-peak readings (NO manipulation of EUT interface cables)								
Frequency	Level	Pol	Class B		Detector	Azimuth	Height	Comments
MHz	dBμV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters	
30.234	23.7	V	30.0	-6.3	QP	4	1.0	QP (1.00s)
185.989	19.4	H	30.0	-10.6	QP	116	4.0	QP (1.00s)

Figure 43–Radiation at 110 VAC.

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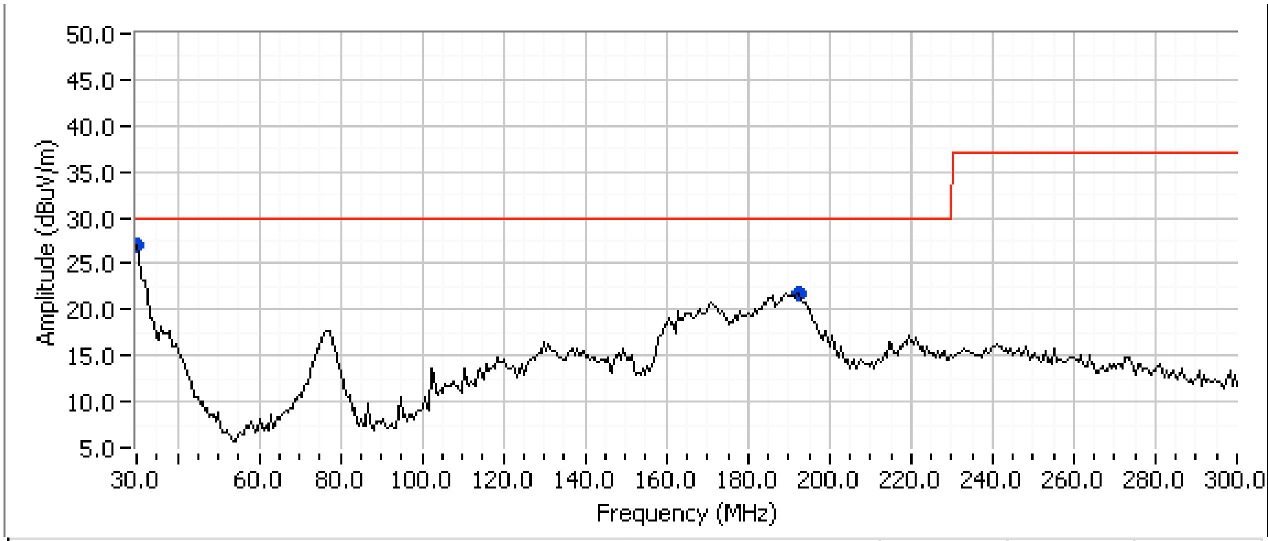

Maximized quasi-peak readings (NO manipulation of EUT interface cables)								
Frequency	Level	Pol	Class B		Detector	Azimuth	Height	Comments
MHz	dBμV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters	
30.287	23.8	V	30.0	-6.2	QP	57	1.0	QP (1.00s)
191.605	19.9	H	30.0	-10.1	QP	121	4.0	QP (1.00s)

Figure 44–Radiation at 230 VAC**.**

14 音频噪声

Test performed inside case with microphone placed 3 mm from case surface on long side of case, transformer facing towards microphone.

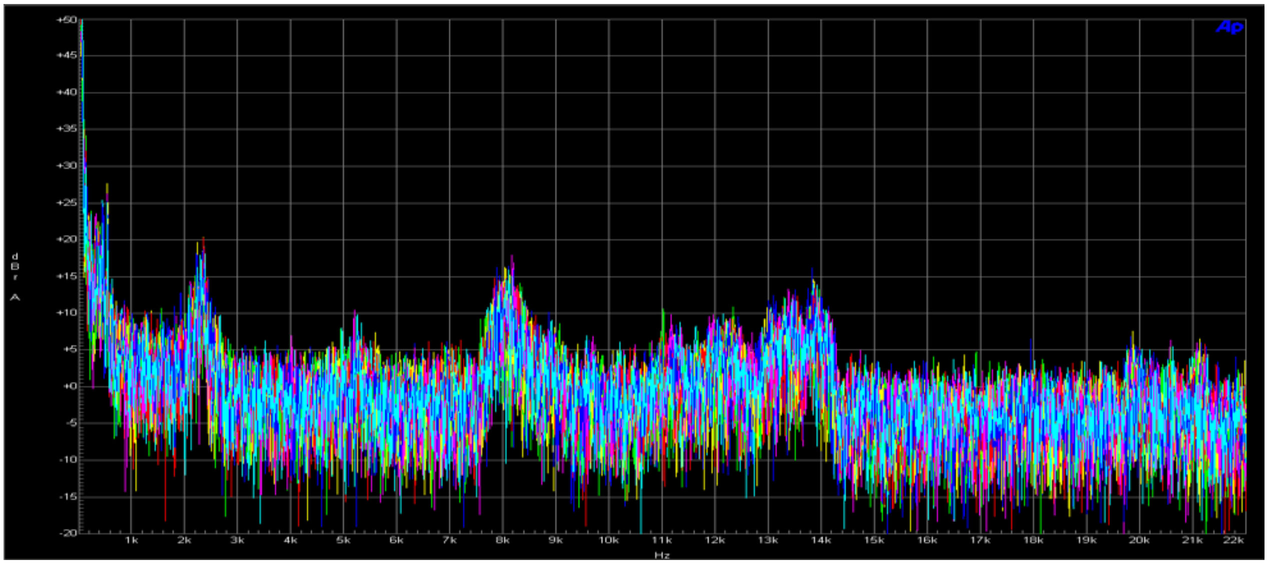

Figure 45–Audible Noise Spectrum: No-load, V_{IN}Swept from 85 VAC to 264 VAC.

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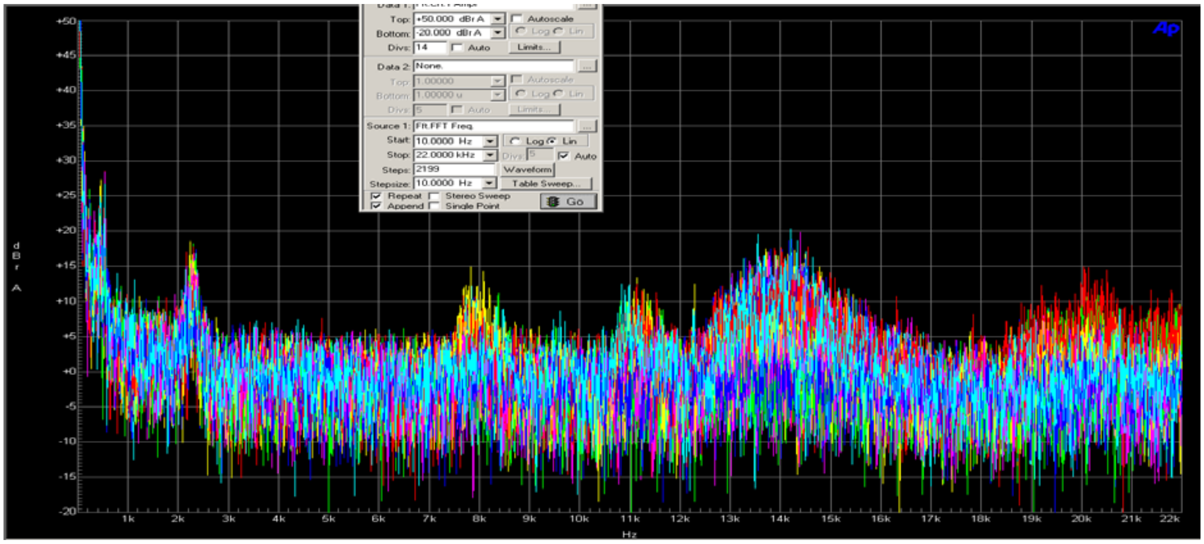

Figure 46–Audible Noise Spectrum: 85 VAC, I_{OUT} Swept from 0 A to 2.0 A.

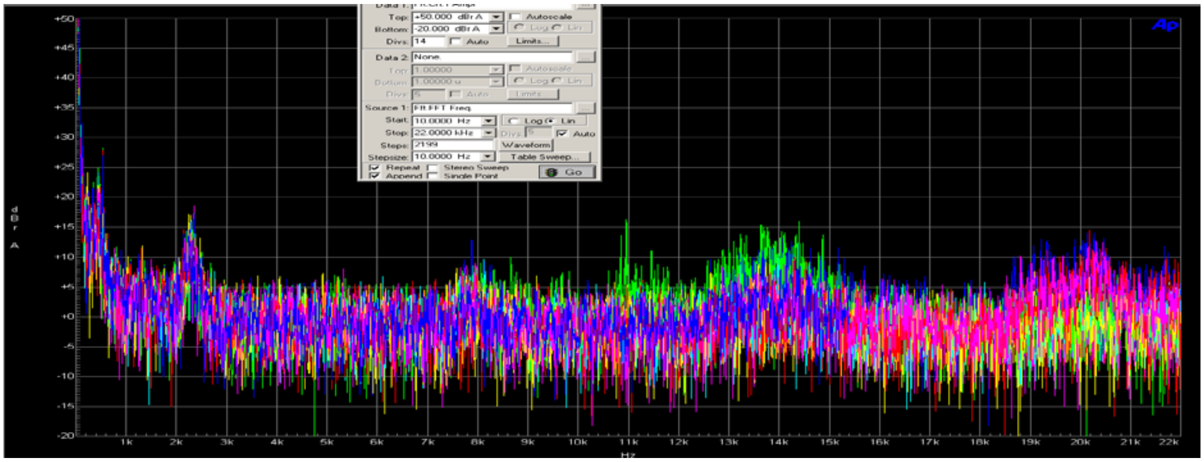

Figure 47–Audible Noise Spectrum: 110 VAC, I_{OUT} Swept from 0 A to 2.0 A.

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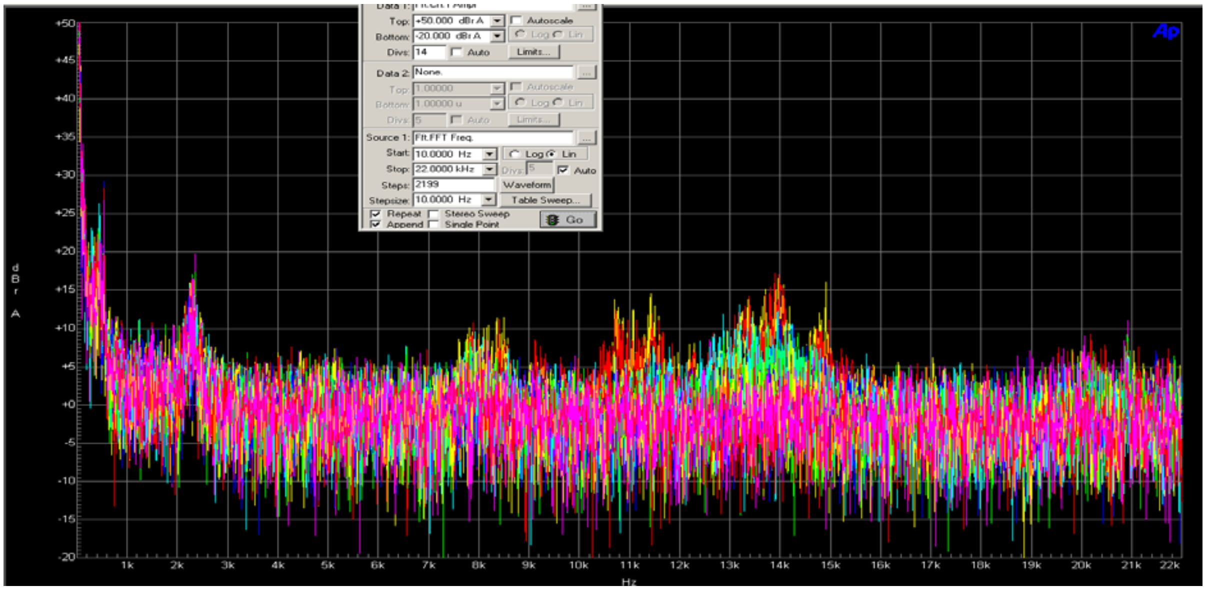

Figure 48–Audible Noise Spectrum: 220 VAC, I_{OUT} Swept from 0 A to 2.0A.

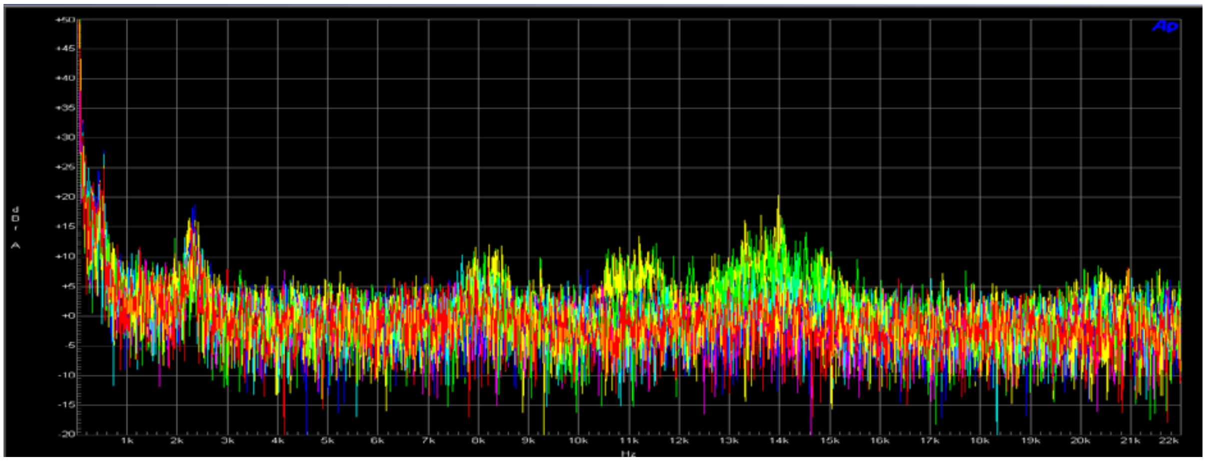

Figure 49–Audible Noise Spectrum: 265 VAC, I_{OUT} Swept from 0 A to 2.0 A.

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15 雷击浪涌和 ESD 测试

15.1 *差模测试*

Passed ±1 kV, 500 A surge test

15.2 *共模测试*

Passed ±6 KV, 500 A ring wave test.
Need to install plastic barrier for >5 kV ring wave common mode surge test.

15.3 *ESD 测试*

Passed ±16.5 kV air, 8 kV contact.
Need to install plastic barrier to pass ESD test.

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16 版本历史

日期	作者	修订版本	说明和变更	审核者
2014 年 11 月 11 日	DK	1.0	初始版本	Mktg& Apps

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