役職	***HiperPFS™ -2 (PFS7326H) 及び HiperLCS™ (LCS702HG) 使用の力率改善回路付き 150 W LLC 電源のデザイン例レポート***
仕様	90 VAC – 265 VAC 入力、 150 W (43 V 以下、0 - 3.5 A) 出力 (定電流)
アプリケーション	LED 街路灯
作成者	アプリケーション技術部門
ドキュメント番号	RDR-382
日付	2014 年 5 月 28 日
改訂	6.2

概要と機能

- PFC および LLC コンバータが内蔵され、部品点数が少ない設計
- 低コストなフェライト コアを使用した連続モード PFC
- 超小型トランス対応高周波 (250 kHz) LLC。
- PFC 効率 95% 以上 (最大負荷、115 VAC 時)
- 最大負荷時 LLC 効率 95% 以上
  - システム効率 91% 及び 93% (115 VAC/230 VAC 時)
- 起動回路により個別のバイアス電源が不要
- 電流レギュレーションとアナログ調光搭載

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重要な注意点:
この電源は絶縁に関する安全要件を満たすよう設計されていますが、評価プロトタイプは認証機関の承認を得られていません。すべての試験は、プロトタイプ電源に絶縁トランスを使用して、AC 入力を供給する必要があります。
この設計には個別のバイアスコンバータがないため、電源の停止直後に 280 VDC 以下が整流コンデンサに生じます。安全のため、このコンデンサに触れる前に、適切な抵抗 (適切な値は 10 k / 2 W) で放電するか、最長 10 分そのままの状態で放置します。

1 はじめに

この技術レポートには、90-265 VAC LED 街路灯及びその他の大電力照明アプリケーション用の 43 V (定格)、150 W の設計例が記載されています。電源は、43 V で 150 W LED パネルを直接駆動するために、定電流出力に対応した設計となっています。

この設計は、PFC フロント エンドに PFS7326H を、LLC 出力部に LCS702HG を使用しています。

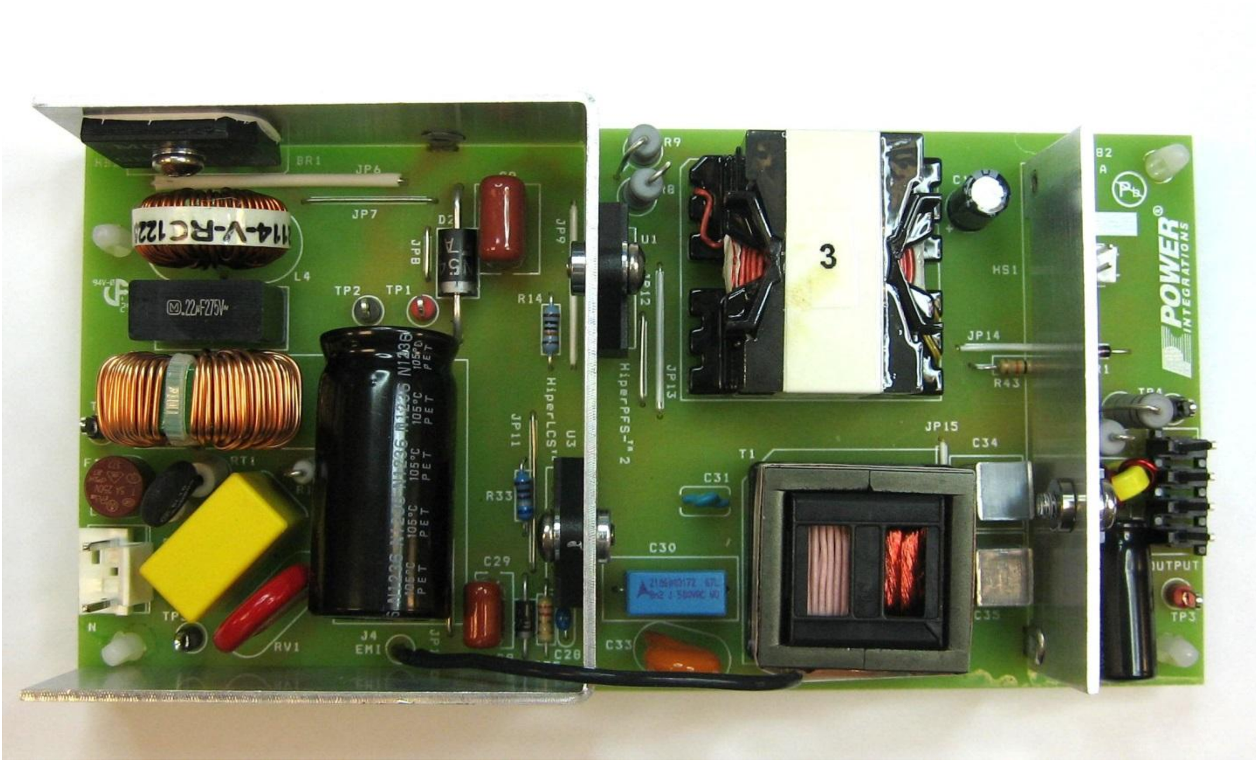

Figure 1 – RD-382 Photograph, Top View.

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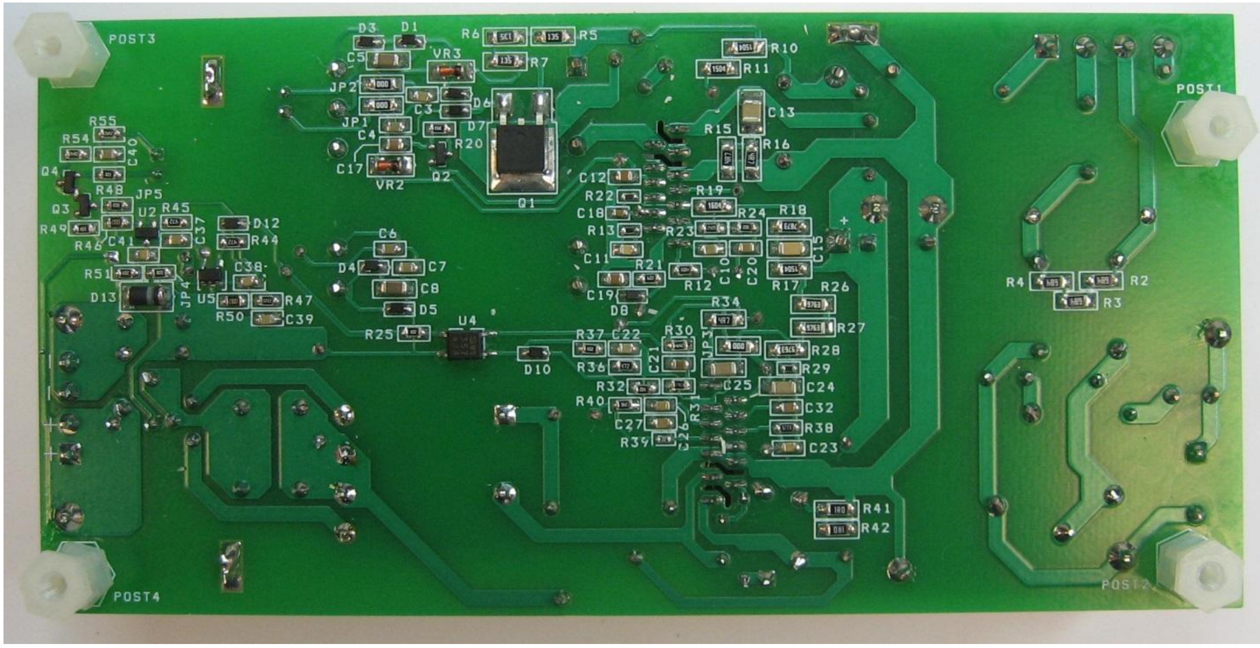

Figure 2 – RD-382 Photograph, Bottom View.

2 電源仕様

次のテーブルは、設計上の概要特性です。実際の性能は、「性能データ」のセクションを参照してください。

概要	記号	最小	標準	最大	単位	コメント
入力						
電圧	V_{IN}	90		265	VAC	3 ワイヤ入力。
周波数	f_{LINE}	47	50/60	64	Hz	
力率	**PF**	0.97				最大負荷、230 VAC
メイン コンバータの出力						
出力電圧	V_{LG}		43		V	43 VDC (定格 - LED 負荷により定義)
出力リップル	$V_{RIPPLE(LG)}$			300	mV P-P	20 MHz バンド幅
出力電流	I_{LG}	0.00	3.5		A	無負荷状態時に保護するための定出力電流
出力電力の合計						
連続出力電力	P_{OUT}		150	N/A	W	
ピーク出力電力	$P_{OUT(PK)}$				W	
効率						
システム全体 (最大負荷時)	$\eta_{メイン}$		91 93		%	115 VAC、最大負荷時の測定 230 VAC、最大負荷時の測定
環境						
伝導 EMI		CISPR22B/EN55022B に適合				
安全規格		IEC950/UL1950 クラス II に適合するように設計				
サージ						1.2/50 μs サージ、IEC 1000-4-5、ディファレンシャル モード:2 Ω コモン モード: 12 Ω
差動		2			kV	
コモンモード		4			kV	
周囲温度	T_{AMB}	0		60	^oC	条件については熱に関するセクションを参照してください

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3 回路図

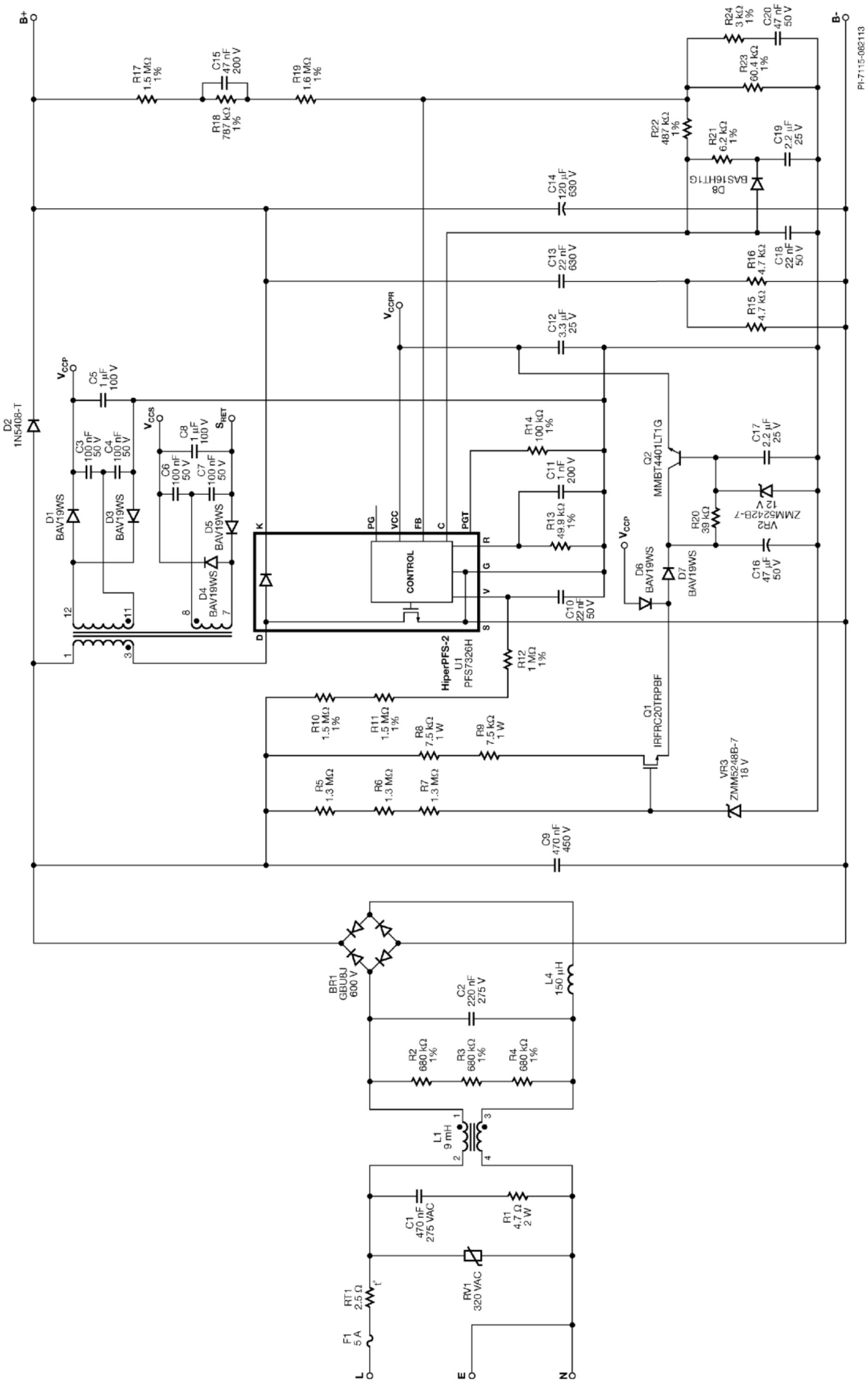

Figure 3 – Schematic RD-382 Street Light Power Supply Application Circuit - Input Filter, PFC Power Stage, and Bias Supplies.

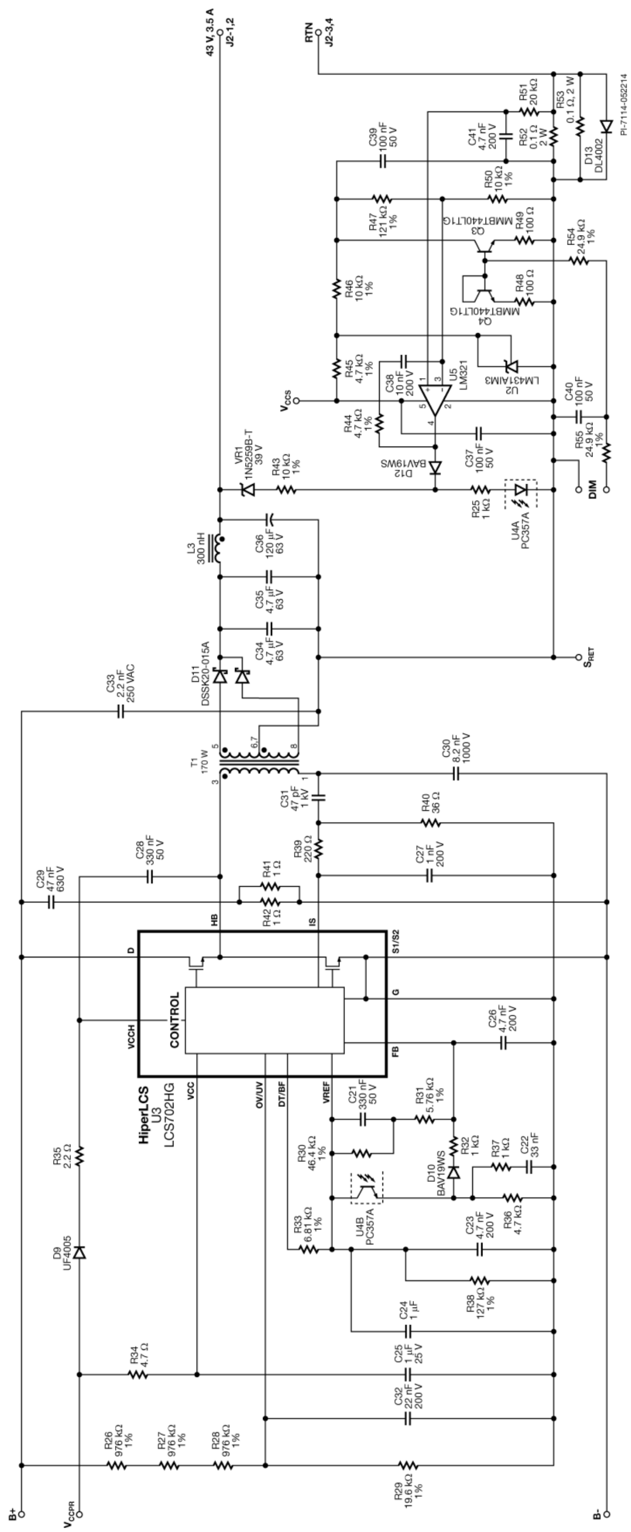

Figure 4 – Schematic of RD-382 Street light Power Supply Application Circuit, LLC Stage.

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4 回路の説明

4.1 *入力フィルタ、昇圧型コンバータ、バイアス回路*

図 3 の回路図は、入力 EMI フィルタ、PFC コンバータ、一次バイアス回路、及び起動回路を示しています。力率改善回路には、PFS7326H を使用します。一次及び二次バイアス電力は、PFC インダクタ (L2) の巻線から供給されます。

4.2 *EMI フィルタリング及び突入電流制限*

コンデンサ C1 及び C2 は、ディファレンシャルモードのノイズを制御するために使用されます。抵抗 R1 は、ダンピング、力率の改善、及び EMI の削減に使用されます。抵抗 R2-4 は、AC 電源が除去された場合に C1 と C2 を放電します。インダクタ L1 は、コモン モードの EMI を制御します。U1 と U3、及び BR1 のヒート シンクは一次リターンに接続され、伝導及び容量結合されたノイズの発生源となることを防ぎます。サーミスタ RT1 は、突入電流制限を行います。コンデンサ C33 (図 4) は、コモン モードの EMI をフィルタリングします。インダクタ L4 ディファレンシャルモードの EMI をフィルタリングします。

4.3 *メイン PFC コンバータ*

コンポーネント R17 ～ 19 及び R23 は、出力電圧のフィードバックを提供します。コンデンサ C15 は、PFC 回路の高速アンダーシュートまたはオーバーシュートに対し U1 FB ピンに高速 dv/dt フィードバックを行います。周波数補償は、C19、C20、R21、R22、R24 により行われます。抵抗 R10-12 (C10 によるフィルタリング) は、U1 に入力電圧情報を提供します。抵抗 R13 (C11 によりフィルタリング) は、U1 を [効率] モード用にプログラムします。HiperPFS-2 の効率モードについての詳細は、「HiperPFS-2 データシート」を参照してください。抵抗 R14 は、U1 の機能を強化するスレッシュホールドをプログラムします。

コンデンサ C12 は、U1 のローカル用バイパス コンデンサです。ダイオード D2 は、AC が最初に入力された場合に、PFC インダクタ L2 と U1 の内部出力ダイオードとは別のルートから PFC 出力コンデンサ (C14) を充電します。コンデンサ C13 と R15-16 は、部品 U1 と C14 周辺の高周波ループを低減するのに使用され、EMI を削減します。C13 と直列の抵抗は、中間周波数領域の EMI ピークを減衰します。入力 AC は、BR1 によって整流され、C9 によってフィルタリングされます。コンデンサ C9 は、低損失ポリプロピレン タイプとして選択され、UI の ON 時間中に L2 を通して高いピーク電流を供給します。サーミスタ RT1 は、起動時に突入電流を制限します。

4.4 *一次バイアス回路及び起動*

部品 R5-7、R8～R9、Q1、及び VR3 は、U1 の起動時のバイアス回路です。U1 が起動すると、部品 D1、D3、及び C3-5 は、PFC チョーク L2 上の巻線を通して一次バイアス回路を形成します。これは電源の PFC 及び LLC コンバータの両方に電力供給するために使用されます。一次バイアス回路電圧が立ち上がると、ダイオード D6 を通して MOSFET Q1 をオフにするため

に使用され、電力消費を削減します。抵抗 R8 及び Q1 は、電源が起動しない場合に過度な電力消費から Q1 を保護します。

部品 D7、Q2、C16～17、及び VR2 は、U1 と U3 のバイアス回路電圧を制御します。部品 D4、D5、及び C6 ～ 8 は、L2 の 3 層絶縁線を通して二次側制御回路のバイアス回路を形成します。

4.5 *LLC コンバータ*

図 4 の回路図は、LCS702HG を使った定電流出力対応 43 V、150 W LLC DC-DC コンバータを示しています。

4.6 *一次側*

IC U3 には、LLC 共振ハーフブリッジ (HB) コンバータに必要な制御回路、ドライバ、出力 MOSFET が内蔵されています。U3 の HB 出力は、ブロッキング及び共振コンデンサ (C30) 経由で出力トランス T1 を駆動します。このコンデンサは、動作リップル電流に対応しており、異常状態時の高電圧に耐えます。

トランス T1 は 49 μH の漏れインダクタンスに対応し、設計されました。この値と共振コンデンサ C30 の値から、以下の方程式に基づき一次直列共振周波数が 259 kHz 以下に設定されます。

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

この方程式の f_R は、直列共振周波数 (単位ヘルツ) です。L_L は、トランスの漏れインダクタンス (単位ヘンリー) です。そして、C_R は、共振コンデンサ (C11) の値 (単位ファラッド) です。

トランスの巻線比は、最大負荷時の定格入力電圧の動作周波数が前述の共振周波数をわずかに下回るように一次巻線を調整することによって設定されました。

250 kHz の動作周波数は、トランスのサイズ、セラミック及びフィルム コンデンサを可能にする出力フィルタ コンデンサ、及び効率の優れた妥協点となるよう設計されています。

また、二次巻線数は、コア損失と銅損失のバランスをとり選択されました。一次巻線には AWG #42 リッツ線を使用し、二次巻線には AWG #44 リッツ線を使用しています。この組み合わせにより動作周波数 (250 kHz 以下) で高効率が実現されます。それぞれのリッツ巻線ゲージ内のストランド数は、巻線の収まり具合と銅損失のバランスをとって選択されました。

選択されたコア材料は PW4 (Itacoil 製) です。この材料は性能を向上し、低損失を実現します。

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部品 D9、R35、及び C28 はブートストラップ回路を構成して、U3 の内蔵ハイサイド ドライバを供給します。

部品 R34 及び C25 は、U1 の V_{CC} 電源である +12 V 入力のフィルタリングおよびバイパス供給を行います。*注:15 V 以上の V_{CC} 電圧は U3 を損傷する場合があります。*

電圧分圧器 R26 ～ R29 は、U1 の高電圧ターンオン、ターンオフ、及び過電圧スレッシュホールドを設定します。分圧器の値は、入力過電圧ターン オフ ポイント 473 VDC で、LLC ターンオン ポイントが 360 VDC、ターンオフ ポイントが 285 VDC となるように選択されています。内蔵ヒステリシスは、低入力電圧ターンオフ ポイントを 280 VDC に設定します。

コンデンサ C29 は +380 V 入力用の高周波バイパス コンデンサで、U3 の D 及び S1/S2 ピン間で短い配線で接続されます。直列接続抵抗 R41 ～ 42 は、EMI を低減します。

コンデンサ C31 は、C30 とともに電流分割器を形成します。C31 は、一次電流の一部をサンプリングするのに使用されます。抵抗 R40 がこの電流を検出します。その信号は、R39 と C27 によってフィルタされます。コンデンサ C31 の定格は、異常状態時のピーク電圧に対応する必要があります。また、C12 には、金属化フィルム、SL セラミック、NPO セラミック、COG セラミックなどの安定した低損失誘電体を使用する必要があります。RD-382 で使用されているコンデンサは、CCFL チューブのドライバで一般的に使用される、"SL" 温度特性のセラミック ディスクです。選択された値に基づいて、以下の方程式から 1 サイクル (高速) のカレントリミットが 4.25 A に、7 サイクル (低速) のカレントリミットが 2.35 A に設定されます。

$$I_{CL} = \frac{0.5}{\left(\frac{C31}{C30 + C31}\right) \times R40}$$

I_{CL} は、7 サイクルのカレントリミット (単位アンペア) です。R40 は、カレントリミット抵抗 (単位オーム) です。C30 と C31 は、それぞれ共振コンデンサと電流サンプリング コンデンサの値 (単位ナノファラッド) です。1 サイクルのカレントリミットについては、上記の方程式で 0.5 V の代わりに 0.9 V を使用します。

抵抗 R39 とコンデンサ C27 は、IS ピンへの一次電流信号をフィルタします。抵抗 R39 は、推奨最小値の 220 Ω, に設定されています。C27 の値は、ノイズによる誤動作を防ぐために 1 nF に設定されています。ただし、この値は、前述の計算によるカレントリミット設定値に大きく影響するほど高くはありません。これらの部品は、最大の効果が得られるように IS ピンの近くに配置する必要があります。IS ピンは負電流を許容できるので、電流センスに複雑な整流回路は必要ありません。

R33 と R38 のテブナン等価回路は、デッドタイムを 330 nS に設定し、U3 の最大動作周波数を 847 kHz に設定します。U3 の DT 及び BF は、C23 によりフィルタリングされます。また、R33 と R38 の組み合わせにより、U3 に対してバースト モード "1" が選択されます。この結果、下側と上側のバースト スレッシュホールド周波数がそれぞれ 382 kHz と 437 kHz に設定されます。

FEEDBACK ピンには、FEEDBACK ピンに流れる 1 μA あたり 2.6 kHz という近似特性があります。FEEDBACK ピンへの電流は、U3 の動作周波数を増加させるため、出力電圧を軽減します。R30 と R31 の直列接続により、U3 の最小動作周波数が 160 kHz 以下に設定されます。この値は、最大負荷かつ最小整流コンデンサ電圧でのレギュレーションに必要な周波数より少し低く設定されています。抵抗 R30 は C21 によってバイパスされます。これは、フィードバック ループ オープン時、最初により大きな電流が FEEDBACK ピンに流れるようにすることによって、起動時の出力ソフトスタートを実現するためです。この結果、スイッチング周波数が高い周波数から始まり、その後、出力電圧がレギュレーションになるまで小さくなります。抵抗 R31 は通常、ソフトスタート時の初期周波数が R33 及び R38 で設定される最大スイッチング周波数と等しくなるように、R33 と R38 の並列の組み合わせとして同じ値に設定されます。R31 の値がこれより小さいと、入力電圧が印加されたとき、スイッチング開始前に遅延が発生します。

フォトカプラ U4 は、FEEDBACK ピンへの最大フォトカプラ電流を制限する R32 経由で U3 FEEDBACK ピンを駆動します。コンデンサ C26 は、FEEDBACK ピンをフィルタします。抵抗 R36 は、フォトカプラ出力に負荷をかけて比較的高い電源消費電流で動作させ、ゲインを増やします。抵抗 R32 及び R36 は、大信号ステップ応答とバースト モード出力リップルも改善します。ダイオード D10 は、F_{MAX}/ソフトスタート回路から R36 を絶縁します。

4.7 *出力整流*

トランス T1 の出力は、D11 と C34 ～ 35 によって整流及びフィルタされます。これらのコンデンサは、出力リップル電流定格よりポリエステル誘電体が選択されました。出力整流ダイオード D11 は、効率の高さで 150 V ショットキー ダイオードが選択されました。トランスの二次側の半分をツイストすると (トランス構造のセクションを参照)、二次側の半分の間の漏れインダクタンスが減少するので、24 V 出力整流ダイオードの最悪条件のピーク逆電圧が 57 V に減少します。その結果、高効率対応の 150V ショットキー ダイオードの使用も可能になります。追加の出力フィルタは、L3 及び C36 によって行われます。また、コンデンサ C36 は、LLC "仮想" 出力直列 R-L と出力コンデンサ C34 ～ C15 によって生じた 30 kHz 以下の LLC 出力インピーダンス ピークを減衰させます。

4.8 *出力電流及び電圧の制御*

出力電流は、抵抗 R52 及び R53 を経由して検出されます。これらの抵抗は、ダイオード D13 によりクランプされ、出力短絡中に電流制御回路への損傷を防止します。部品 R45 と U2 は、電圧検出アンプ U5 の電圧基準を提供します。基準電圧は R46 ～ 47 及び R50 により分割され、C39 によりフィルタリングされます。電流センス抵抗からの電圧は、R51 及び C41 によりフ

ィルタリングされ、U5 の 非反転入力に入力されます。オペアンプ U5 は、D12 及び R25 を通してフォトカプラ U4 を駆動します。部品 R25、R44、R51、C38、及び C41 は、カレント ループの周波数補償を行います。部品 VR1 および R43 は、出力電圧検出を行い、出力負荷オープン時に、電源を保護します。これらの部品は、R43 には比較的大きな値、VR1 には比較的低い電圧が使われ、ゆるやかな電圧制限特性を提供します。これは、 V-I 曲線の肩での発振を予防し、特定の LED 負荷接続時の電源起動特性を改善します。

部品 J3、Q3-4、R48 ～ 49、R54-55、R46、及び C40 は、リモート調光機能を提供します。 J3 の調光電圧は、R54 及び R55 により電流に変換され、カレント ミラー Q3 ～ Q4 を通して R46 に入力されます。この電流は、基準電圧で電圧検出アンプ U5 にプルダウンし、プログラムされた出力電流を削減します。調光電圧の 0 ～ 10 VDC が出力電流範囲 (0 V で 100%、10 VDC 入力で 20% 以下) を提供します。

5 PCB レイアウト

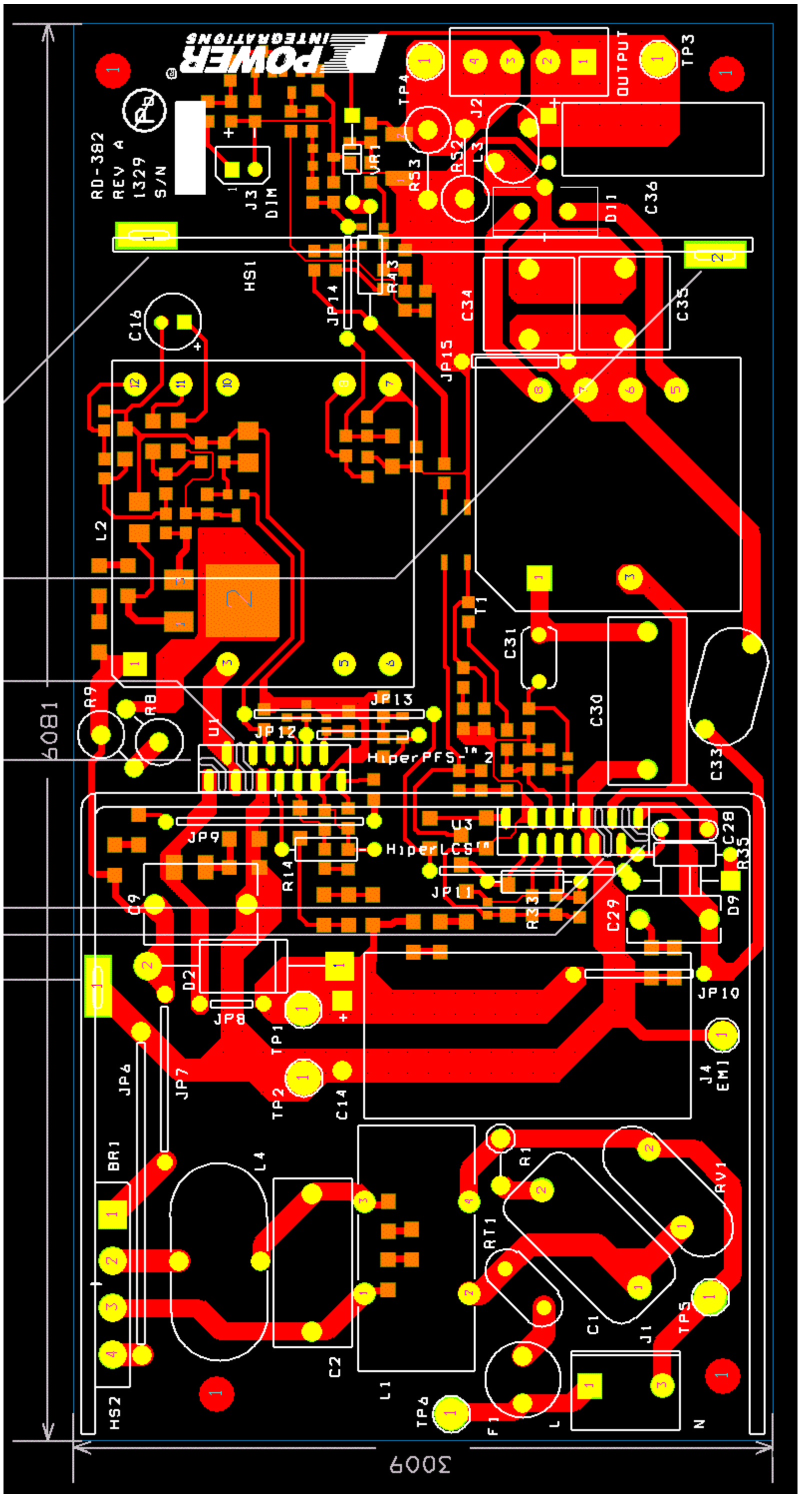

Figure 5 – Printed Circuit Layout, Top Side.

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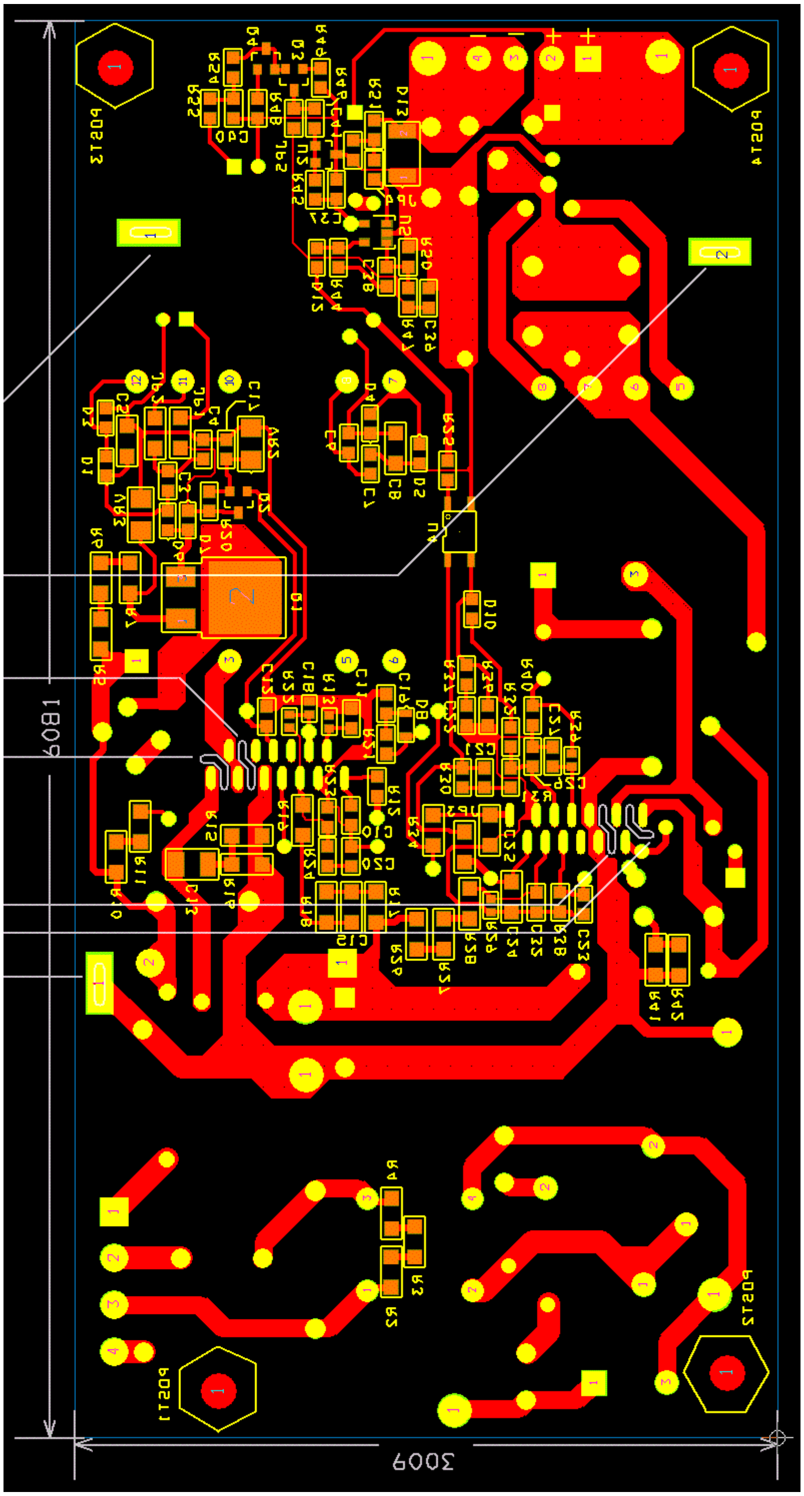

Figure 6 – Printed Circuit Layout, Bottom Side.

6 部品表

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial
2	1	C1	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli
3	1	C2	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
4	7	C3 C4 C6 C7 C37 C39 C40	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
5	2	C5 C8	1 μF, 100 V, Ceramic, X7R, 1206	HMK316B7105KL-T	Taiyo Yuden
6	1	C9	470 nF, 450 V, METALPOLYPRO	ECW-F2W474JAQ	Panasonic
7	1	C10	22 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H223K	Panasonic
8	1	C11	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	1	C12	3.3 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
10	1	C13	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
11	1	C14	120 μF, 450 V, Electrolytic, 20 %, (18 x 37mm)	450BXW120MEFC18X35	Rubycon
12	1	C15	47 nF, 200 V, Ceramic, X7R, 1206	12062C473KAT2A	AVX
13	1	C16	47 μF, 50 V, Electrolytic, 20 %, (6.3 x 12.5 mm)	50YXM47MEFC6.3X11	Rubycon
14	2	C17 C19	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
15	1	C18	22 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H223K	TDK
16	1	C20	47 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H473KA01L	Murata
17	1	C21	330 nF, 50 V, Ceramic, X7R, 0805	GRM219R71H334KA88D	Murata
18	1	C22	33 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB333	Yageo
19	3	C23 C26 C41	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
20	2	C24 C25	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
21	1	C27	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
22	1	C28	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
23	1	C29	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
24	1	C30	8.2 nF, 1000V VDC, Film	B32671L0822J000	Epcos
25	1	C31	47 pF, 1 kV, Disc Ceramic	DEA1X3A470JC1B	Murata
26	1	C32	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX
27	1	C33	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
28	2	C34 C35	4.7 μF, 63 V, Polyester Film	B32560J475K	Epcos
29	1	C36	120 μF, 63 V, Electrolytic, Gen. Purpose, (8 x 22)	EEU-FR1J121LB	Panasonic
30	1	C38	10 nF, 200 V, Ceramic, X7R, 0805	08052C103KAT2A	AVX
31	2	CLIP_LCS_PFS1 CLIP_LCS_PFS2	Heat sink Hardware, Clip LCS_II/PFS	EM-285V0	Kang Yang Hardware Enterprise
32	8	D1 D3 D4 D5 D6 D7 D10 D12	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
33	1	D2	1000 V, 3 A, Recitifier, DO-201AD	1N5408-T	Diodes, Inc.
34	1	D8	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semi
35	1	D9	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
36	1	D11	150 V, 20 A, Schottky, TO-220AB	DSSK 20-015A	IXYS
37	1	D13	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002-13-F	Diodes, Inc.
38	1	F1	5 A, 250V, Slow, TR5	37215000411	Wickman
39	1	HS1	HEAT SINK, Custom, Al, 3003, 0.062" Thk		Custom
40	1	HS2	HEAT SINK, Custom, Al, 3003, 0.062" Thk		Custom
41	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	B3P-VH	JST
42	1	J2	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
43	1	J3	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
44	3	JP1 JP2 JP3	0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic

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45	2	JP4 JP5	0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
46	1	JP6	Wire Jumper, Insulated, TFE, #18 AWG, 1.4 in	C2052A-12-02	Alpha
47	1	JP7	Wire Jumper, Non insulated, #22 AWG, 0.7 in	298	Alpha
48	1	JP8	Wire Jumper, Non insulated, #22 AWG, 0.3 in	298	Alpha
49	1	JP9	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable
50	1	JP10	Wire Jumper, Non insulated, #22 AWG, 0.6 in	298	Alpha
51	1	JP11	Wire Jumper, Non insulated, #22 AWG, 0.8 in	298	Alpha
52	2	JP12 JP15	Wire Jumper, Non insulated, #22 AWG, 0.5 in	298	Alpha
53	1	JP13	Wire Jumper, Insulated, #24 AWG, 0.8 in	C2003A-12-02	Gen Cable
54	1	JP14	Wire Jumper, Insulated, #24 AWG, 0.5 in	C2003A-12-02	Gen Cable
55	1	L1	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
56	1	L2	Custom, RD-382 PFC Choke, 437 uH, PQ32/30, Vertical, 9 pins		Power Integrations
57	1	L3	Output Inductor, Custom, 300 nH, ±15%, constructed on Micrometals T30-26 toroidal core		Power Integrations
58	1	L4	150 μH, 3.4 A, Vertical Toroidal	2114-V-RC	Bourns
59	4	POST1 POST2 POST3 POST4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
60	1	Q1	400 V, 2 A, 4.4 Ohm, 600 V, N-Channel, DPAK	IRFRC20TRPBF	Vishay
61	3	Q2 Q3 Q4	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
62	1	R1	4.7 Ω, 2 W, Flame Proof, Pulse Withstanding, Wire Wound	WHS2-4R7JA25	IT Elect_Welwyn
63	3	R2 R3 R4	680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
64	3	R5 R6 R7	1.3 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ135V	Panasonic
65	2	R8 R9	7.5 kΩ, 5%, 1 W, Metal Oxide	RSF100JB-7K5	Yageo
66	3	R10 R11 R17	1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
67	1	R12	1 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1004V	Panasonic
68	1	R13	49.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4992V	Panasonic
69	1	R14	100 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-100K	Yageo
70	3	R15 R16 R34	4.7 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ4R7V	Panasonic
71	1	R18	787 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7873V	Panasonic
72	1	R19	1.60 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1604V	Panasonic
73	1	R20	39 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ393V	Panasonic
74	1	R21	6.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ622V	Panasonic
75	1	R22	487 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4873V	Panasonic
76	1	R23	60.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6042V	Panasonic
77	1	R24	3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ302V	Panasonic
78	3	R25 R32 R37	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
79	3	R26 R27 R28	976 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
80	1	R29	19.6 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1962V	Panasonic
81	1	R30	46.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4642V	Panasonic
82	1	R31	5.76 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5761V	Panasonic
83	1	R33	6.81 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-6K81	Yageo
84	1	R35	2.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
85	3	R36 R44 R45	4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
86	1	R38	127 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1273V	Panasonic
87	1	R39	220 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic
88	1	R40	36 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ360V	Panasonic
89	2	R41 R42	1 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ1R0V	Panasonic
90	1	R43	10 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo

91	2	R46 R50	10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
92	1	R47	121 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1213V	Panasonic
93	2	R48 R49	100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
94	1	R51	20 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
95	2	R52 R53	0.1 Ω, 5%, 2 W, Thick Oxide	MO200J0R1B	Synton-Tech
96	2	R54 R55	24.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2492V	Panasonic
97	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SL10 2R505	Ametherm
98	4	RTV1 RTV2 RTV3 RTV4	Thermally conductive Silicone Grease	120-SA	Wakefield
99	1	RV1	320 V, 80 J, 14 mm, RADIAL	V320LA20AP	Littlefuse
100	4	SCREW1 SCREW2 SCREW3 SCREW4	SCREW MACHINE PHIL 6-32 X 5/16 SS	PMSSS 632 0031 PH	Building Fasteners
101	2	SPACER_CER1 SPACER_CER2	SPACER RND, Steatite C220 Ceramic	CER-2	Richco
102	1	T1	Integrated Resonant Transformer, Horizontal, 8 pins	TRLEV25043A	Itacoil
103	2	TP1 TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
104	4	TP2 TP4 TP5 TP6	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
105	1	U1	HiperPFS-2, ESIP16/13	PFS7326H	Power Integrations
106	1	U2	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
107	1	U3	HiperLCS, ESIP16/13	LCS702HG	Power Integrations
108	1	U4	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N1TJ00F	Sharp
109	1	U5	OP AMP SINGLE LOW PWR SOT23-5	LM321MF	National Semi
110	1	VR1	39 V, 5%, 500 mW, DO-35	1N5259B-T	Diodes, Inc.
111	1	VR2	12 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5242B-7	Diodes, Inc.
112	1	VR3	18 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5248B-7	Diodes, Inc.
114	4	WASHER1 WASHER2 WASHER3 WASHER4	Washer Flat #6, SS, Zinc Plate, 0.267 OD x 0.143 ID x 0.032 Thk	620-6Z	Olander

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7 LED パネルの特性評価

A commercial 150 W LED streetlight was used to test the RD-382 power supply. The LED array consisted of (6) 7 X 4 panels, as 4 wide, 7 deep. For the purposes of testing, the six panels were connected in series-parallel, resulting in an LED array 12 wide, 14 deep (see Figures 8 and 9). The V-I characteristic of the LED panels connected in this manner is shown below in Figure 7.

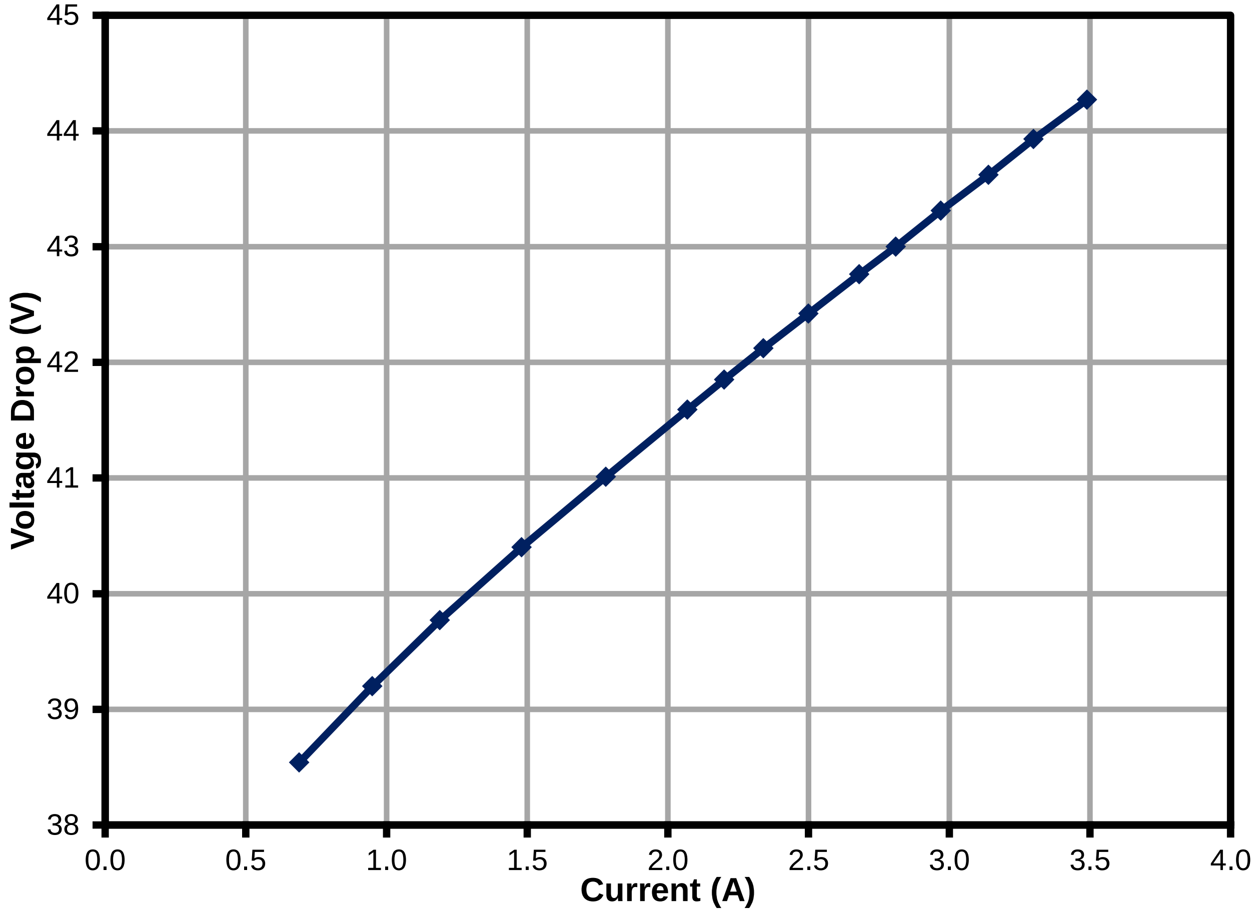

Figure 7 – Streetlight LED Array V-I Characteristic.

7.1 LED パネルのカレント シェアリング

For the purpose of this report, the six LED panels in the street light were partitioned into 3 sections, each section consisting of two LED panels in series. Each panel was internally connected as an array of LEDs 4 wide and 7 deep so that two panels connected in series consisted of an array of LEDS 4 wide by 14 deep. The three sections were connected in parallel, forming a total LED load 12 wide and 14 deep. Using a DC current probe, the current in each 4 wide by 14 deep section was measured to determine the current distribution between sections, with results shown below.

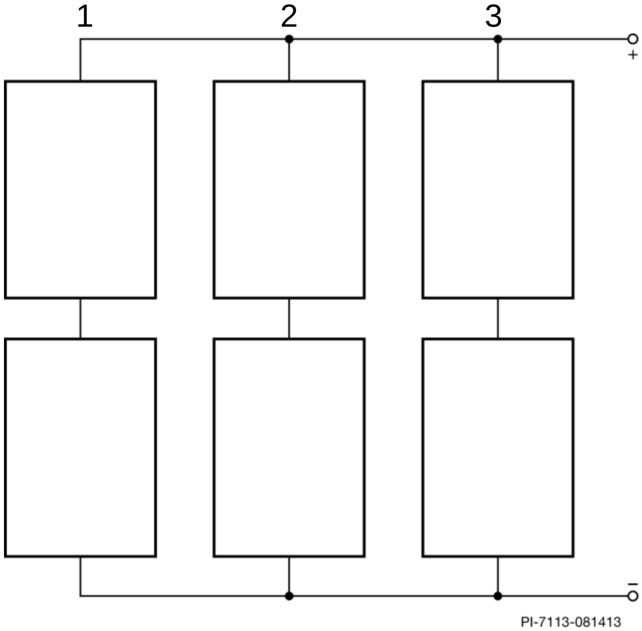

Figure 8 – LED Test Panel Layout.

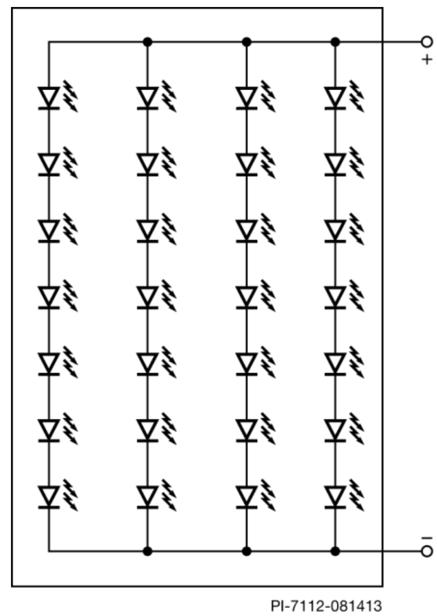

Figure 9 – Array of LEDs in Each Test Panel.

Section #	1	2	3
Current (A)	1.113 A	1.159 A	1.126 A

Maximum difference between sections was <5%.

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7.2 ***定電圧負荷***

Since this power supply has a constant current output tailored for a relatively fixed constant voltage load, the usual constant current electronic load cannot be used for testing. For bench testing at maximum power, a constant resistance load can be used, set such that the supply output is at maximum current and an output voltage of 43-44 V, as indicated by the V-I curve shown in Figure 7. Other testing, including dimming and gain-phase, will require the actual LED load or a constant voltage load that closely mimics its characteristics.

The streetlight LED as a load was both large and heavy. In order to facilitate EMI and surge testing, a constant voltage load was constructed to emulate the behavior of the LED array in a much smaller package. The circuit is shown in Figure 8. The load consists of paralleled power Darlington transistors Q1-5, each with an emitter resistor (R1-5) to facilitate current sharing. Base resistors R6-10 help prevent oscillation. A string of thirteen 3 mm blue LEDs (D1-13) are used as a voltage reference to mimic the characteristics of the LED panel. Resistor R11 is adjusted to vary the voltage at which the load turns on to match the characteristics of the LED panel. Resistors R12-14 add extra impedance in series with the load to approximate the characteristics of the LED panel. The completed array with heat sink is shown in Figure 9. A small fan was used to cool the heat sink when the load was operated for extended periods at full power. The V-I characteristics of the CV load are shown superimposed on those of the LED array in Figure 10. An electronic load with appropriate rating and a constant voltage option (with some series resistance) could also be used for testing, but this load has the advantage that no external AC power is needed.

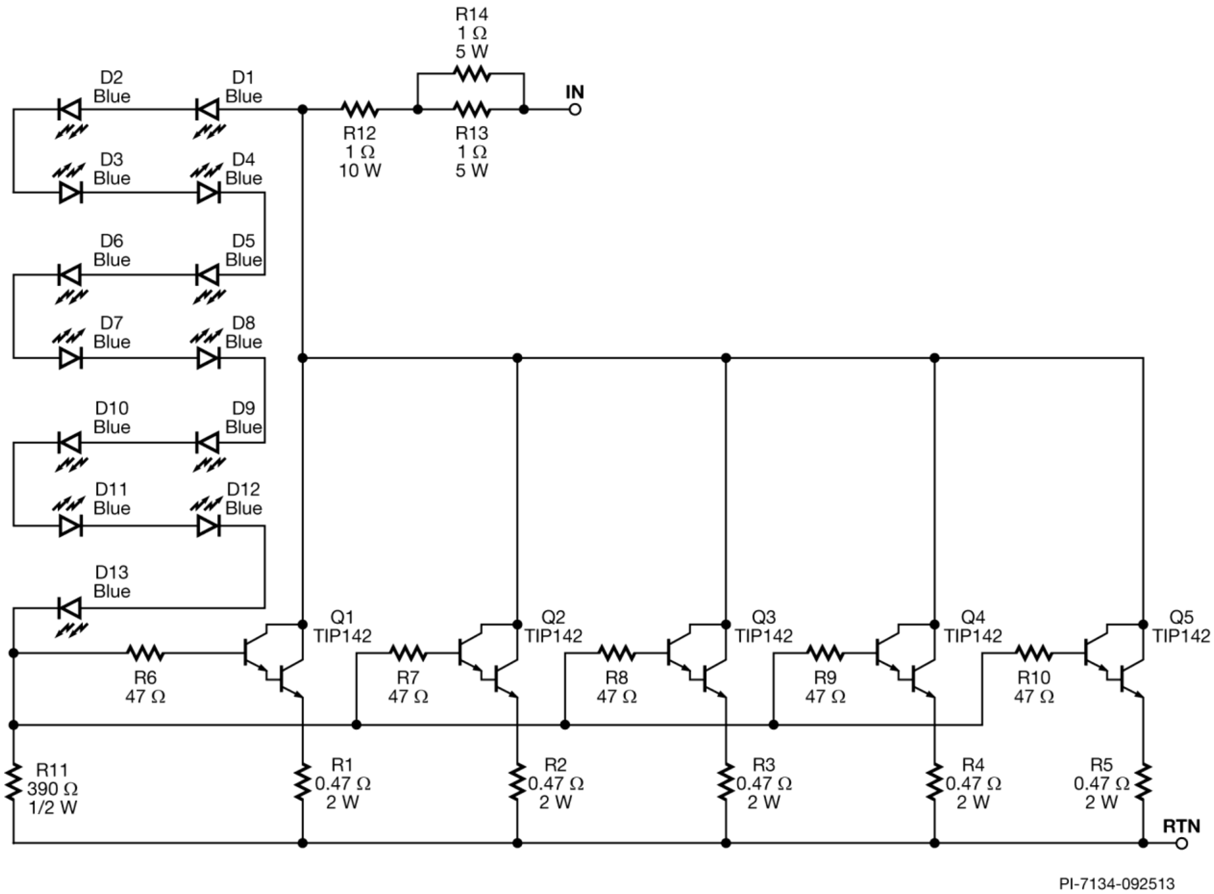

Figure 10 – Constant Voltage Load Schematic.

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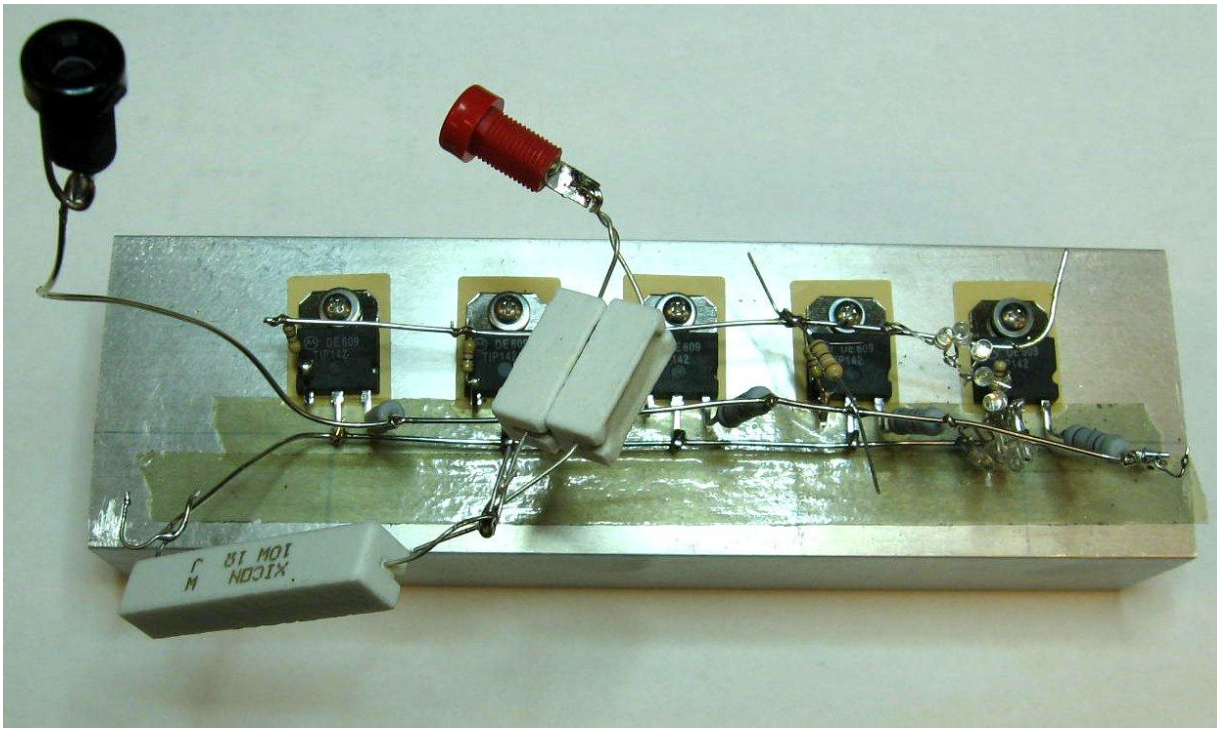

Figure 11 – Constant Voltage Load with Heat Sink.

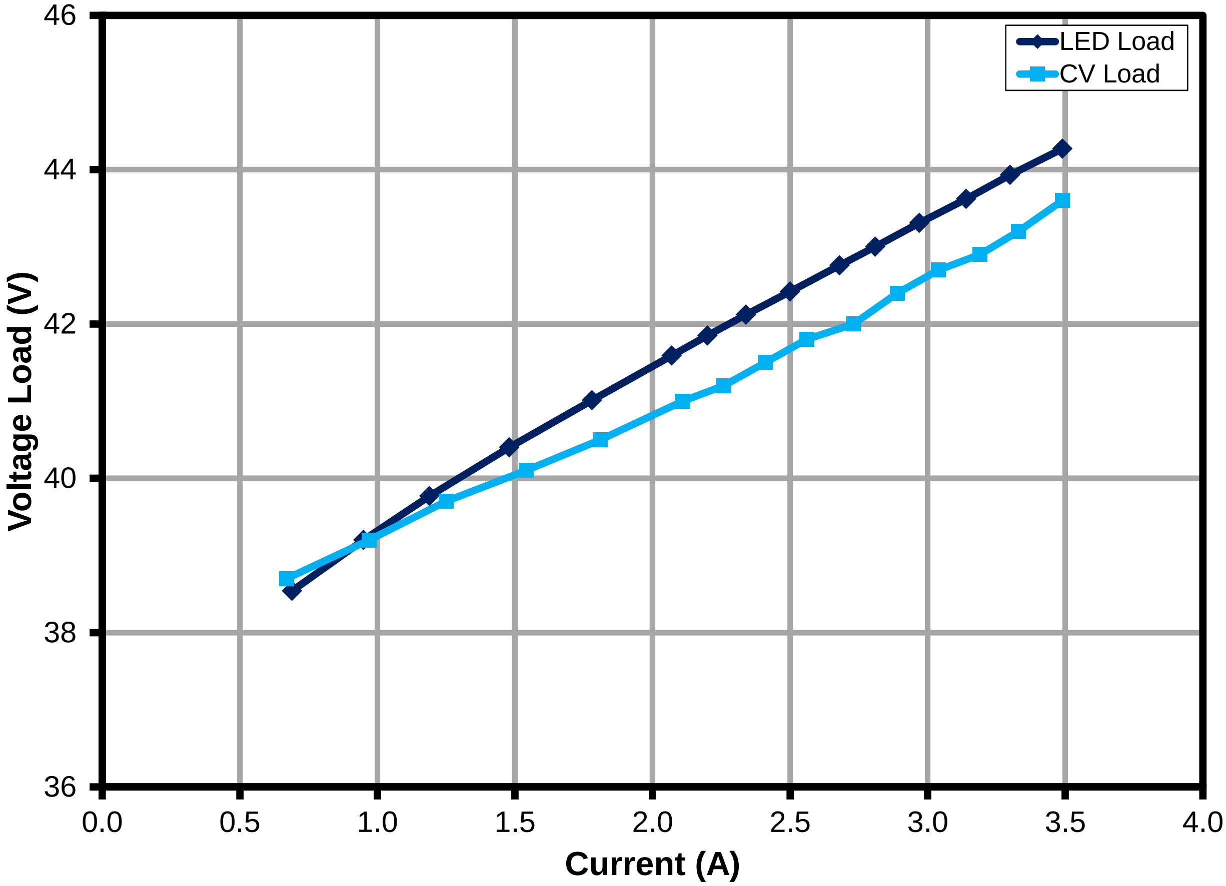

Figure 12 – Comparison of Streetlight LED Array V-I Characteristic with CV Load**.**

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8 磁気部品

8.1 *PFC チョーク(L2) の仕様*

8.1.1 *回路図*

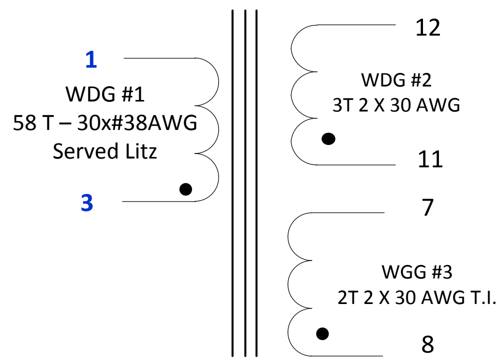

Figure 13 – PFC Choke Electrical Diagram.

8.1.2 *電気仕様*

Inductance	Pins 1-3 measured at 100 kHz, 0.4 V_{RMS}.	437 μH +5%
Resonant Frequency	Pins 1-3. N/A	kHz (Min.)

8.1.3 *材料*

Item	Description
[1]	Core: TDK Core: PC44PQ32/20Z, gap for A_{LG} of 130 nH/T^2.
[2]	Bobbin: BPQ32/20-112CPFR – TDK.
[3]	Litz Wire: 30 x #38 AWG Single Coated Solderable, Served.
[4]	Tape, Polyester Film: 3M 1350-F1 or equivalent, 9.0 mm wide.
[5]	Magnet Wire, 30 AWG, Solderable Double Coated.
[6]	Triple Insulated Wire, 30 AWG, Furukawa TEX-E or equivalent.
[7]	Varnish: Dolph BC-359, or equivalent.

8.1.4 *構造図*

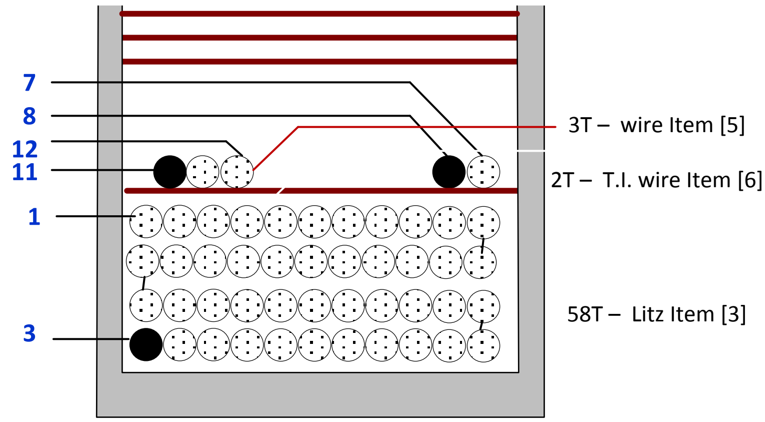

Figure 14 – PFC Inductor Build Diagram.

8.1.5 *巻線概要*

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 3, wind 58 turns of Litz wire item [3], finish at pin 1.
Insulation	Apply one layer of tape item [4]
Winding #2	Starting at pin 11, wind 3 bifilar turns of wire, item [5]. Spread turns evenly across bobbin window. Finish at Pin 12.
Winding #3	Starting at pin 8, wind 2 bifilar turns of wire, item [6], directly on top of previous winding. Spread turns evenly across bobbin window. Finish at pin 7.
Insulation	Apply 3 layers of tape item [4].
Final Assembly	Grind core to specified inductance. Secure core halves with tape. Remove pins 2, 4, and 9. Dip varnish with item [7].

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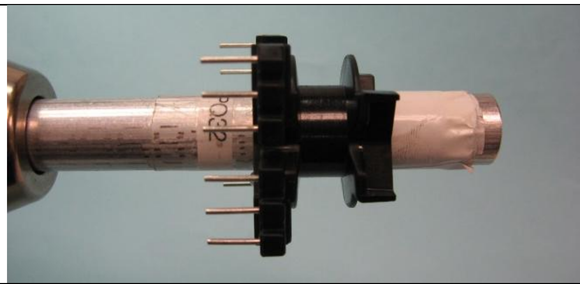
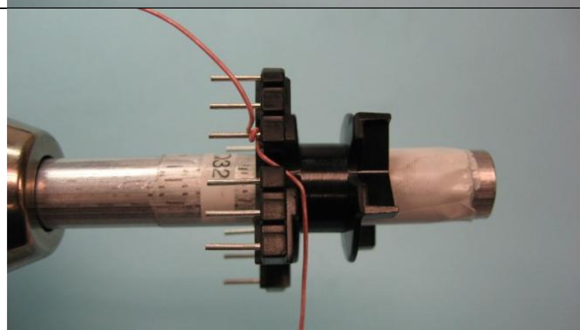
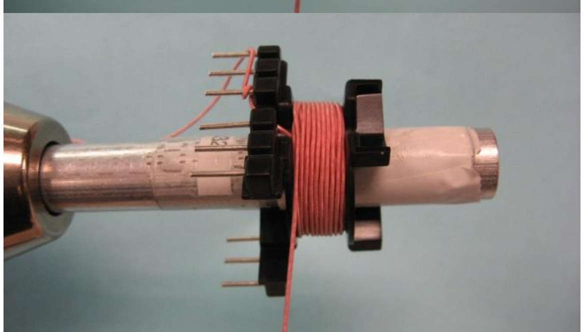
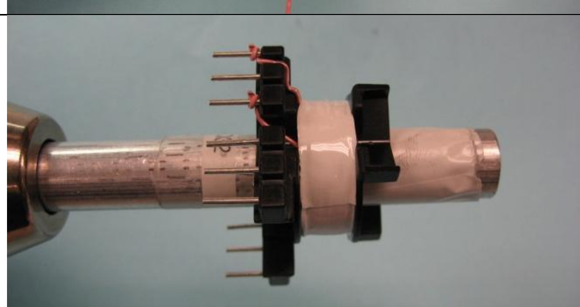
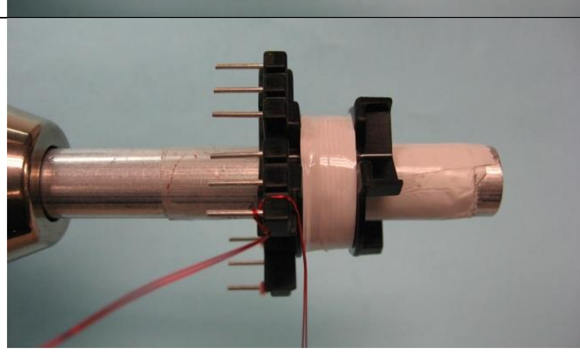
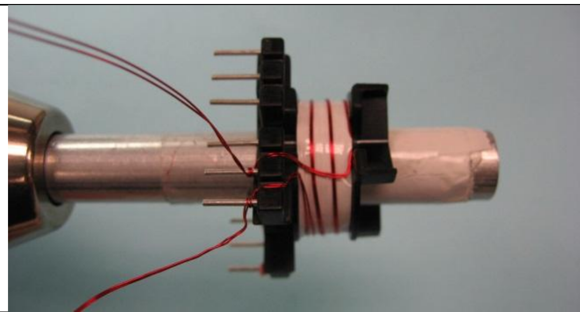
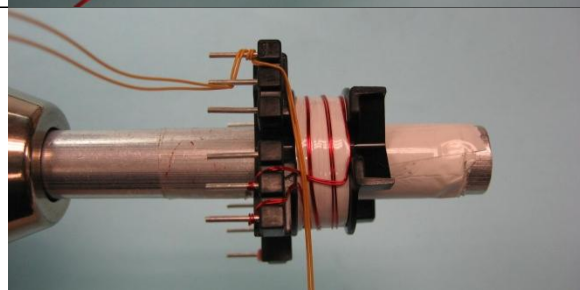
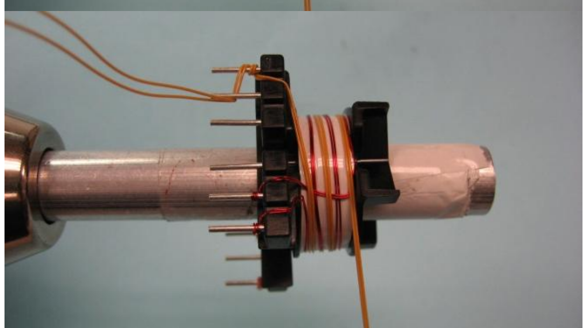
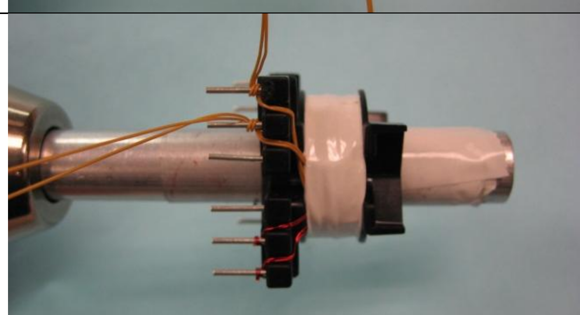
8.1.6 *巻線手順*

Winding Preparation		Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction
Winding #1	 	Starting at pin 3, wind 58 turns with 30x #38 served Litz wire, item [3].
Insulation		Apply 1 layer of insulating tape, item [4]. Terminate wire at pin 1
Winding #2		Starting at pin 11, wind 3 bifilar turns with #30 AWG double coated wire, item [5].

		Terminate wire at pin 12. Do not apply insulating tape to this winding.
Winding #3	 	Starting at pin 8, wind 2 bifilar turns with #30 AWG triple insulated wire, item [6].
Insulation		Apply 3 layers of insulating tape, item [4]. Terminate wire at pin 7
Solder Terminations		Solder all wire terminations at pins 1, 3, 7, 8, 11, and 12

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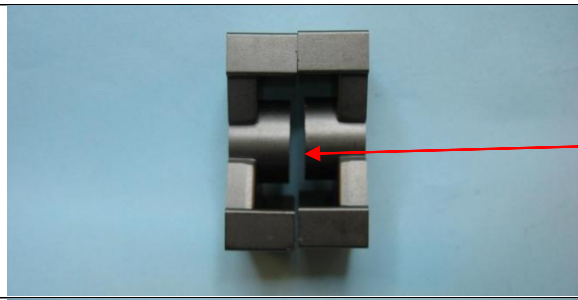
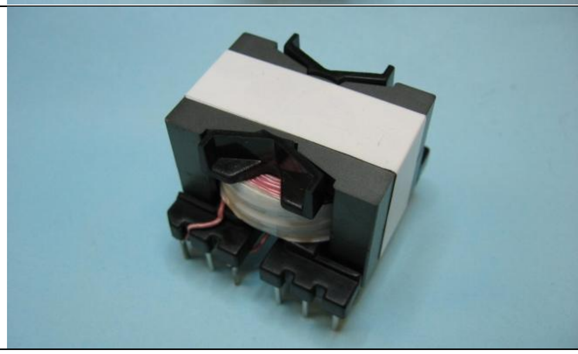
Core Grinding		Grind core for specified inductance.
Final Assembly		Secure core halves with tape. Remove pins 2, 4, and 9.

8.2 *LLC トランス (T1) の仕様*

8.2.1 *回路図*

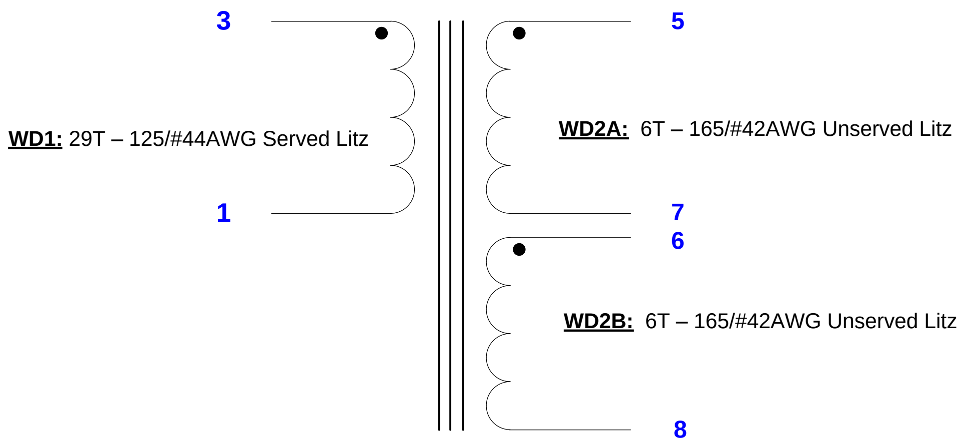


Figure 15 – LLC Transformer Schematic.

8.2.2 *電気仕様*

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 5-8.	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	340 µH ±10%
Resonant Frequency	Pins 2-5, all other windings open.	1800 kHz (Min)
Primary Leakage Inductance	Pins 1-5, with pins 5-8 shorted, measured at 100 kHz, 0.4 $V_{RMS.}$	49 µH ±5%

8.2.3 *材料*

Item	Description
[1]	Core Pair: Itacoil NFEV25A, PW4 material, gap for A_{LG} of 404 nH/T^2.
[2]	Bobbin: Itacoil RCEV25A.
[3]	Bobbin Cover, Itacoil GSEV25A.
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 12 mm wide.
[5]	Litz wire: 165/#42 Single Coated, Unserved.
[6]	Litz wire: 125/#44 Single Coated, Served.
[7]	Copper Tape, 3M-1181; or equivalent, 10 mm wide.
[8]	Wire, 20 AWG, Black, Stranded, UL 1015 Alpha 3073 BK or equivalent.

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8.2.4 *構造図*

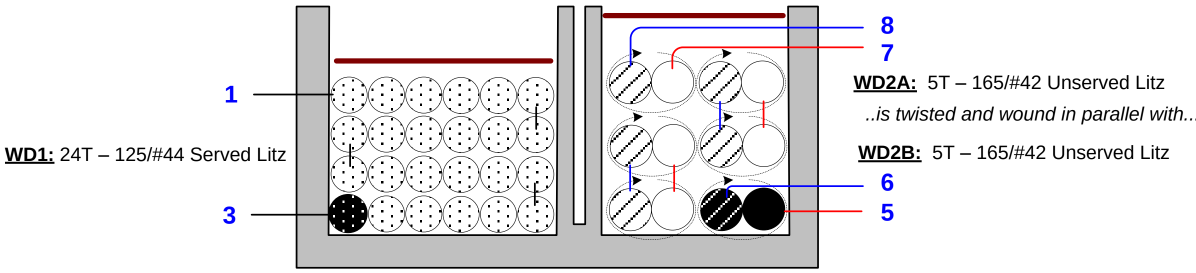
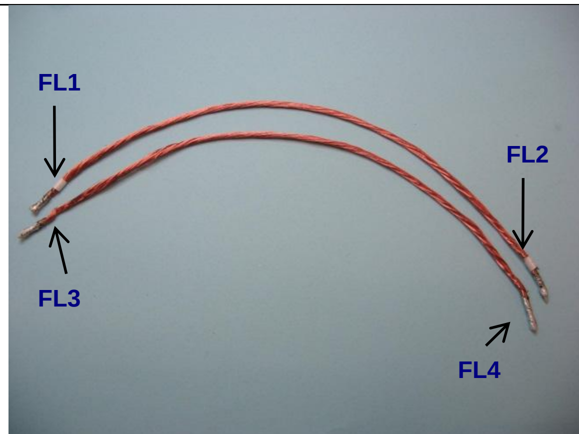
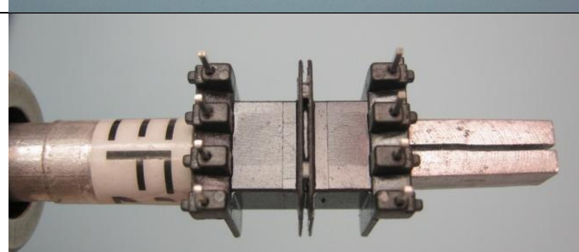
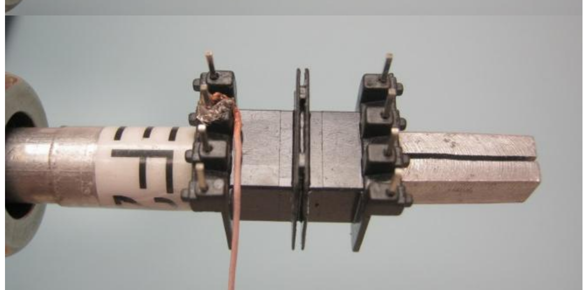
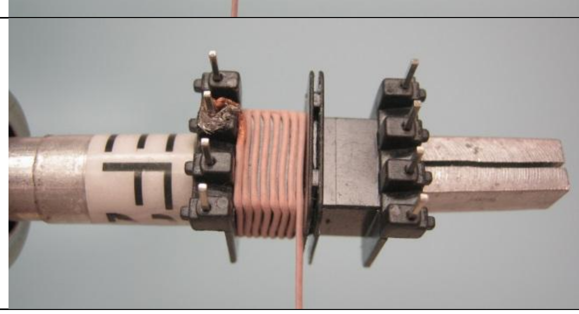


Figure 16 – LLC Transformer Build Diagram.

8.2.5 *巻線概要*

Secondary Wire Preparation	Prepare 2 strands of wire item [5] 12” length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1” free at each end. See pictures below.
WD1 (Primary)	Place the bobbin item [2] on the mandrel with primary chamber on the left side. Note: primary chamber is wider than secondary chamber. Starting on pin 3, wind 29 turns of served Litz wire item [6] in 5 layers, and finish on Pin 1.
WD2A & WD2B (Secondary)	Using unserved Litz assembly prepared in step 1, start with FL1 on pins 5 and FL3 on pin 6, tightly wind 6 turns in secondary chamber. Finish with FL2 on pin 6 and FL4 on pin 8.
Bobbin Cover	Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish	Remove pins 2, 4 of bobbin. Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of copper tape [7] as shown, overlap ends, and solder. Solder 3” termination lead of stranded wire item [8] to core band close to pin 4 as shown, secure with two turns of tape item [4].

8.2.6 *巻線手順*

Secondary Wire Preparation		Prepare 2 strands of wire item [7] 12" length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1" free at each end.
WD1 **(Primary)**		Place the bobbin item [2] on the mandrel with primary chamber on the left side. Note: primary chamber is wider than secondary chamber. Starting on pin 3,
WD1 **(Primary)** **(Cont'd)**		Wind 29 turns of served Litz wire item [6] in 5 layers, and finish on pin 1.

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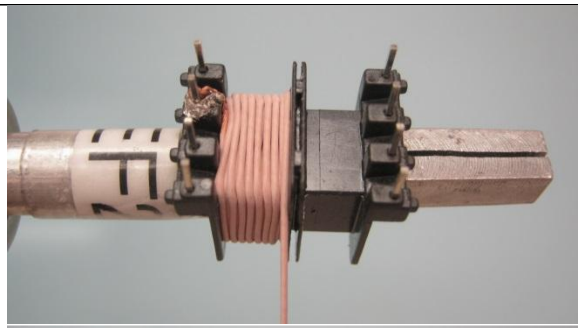
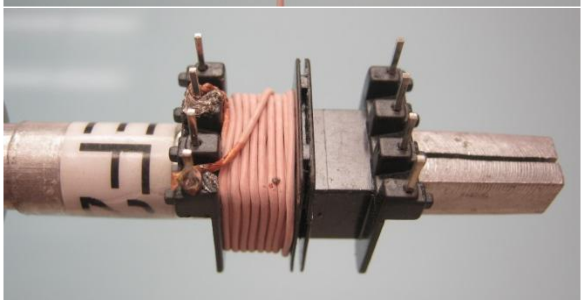
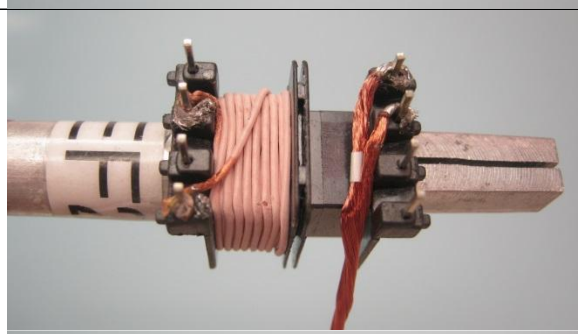
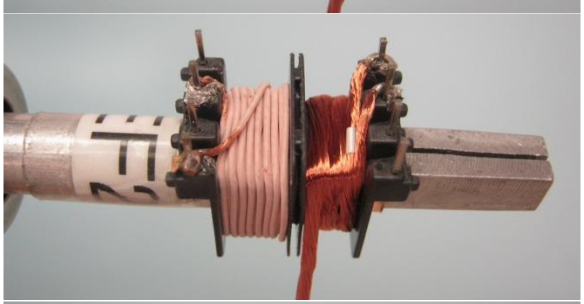
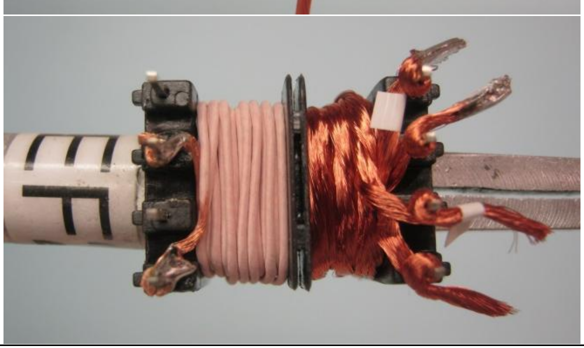
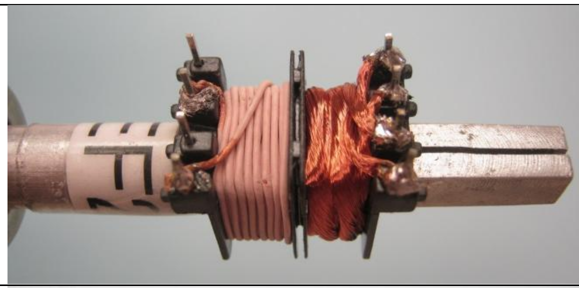
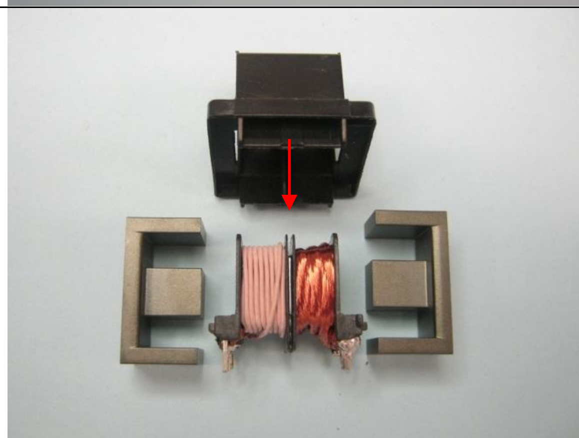
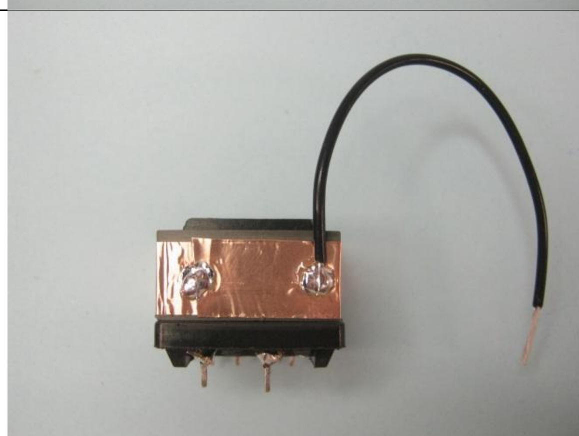
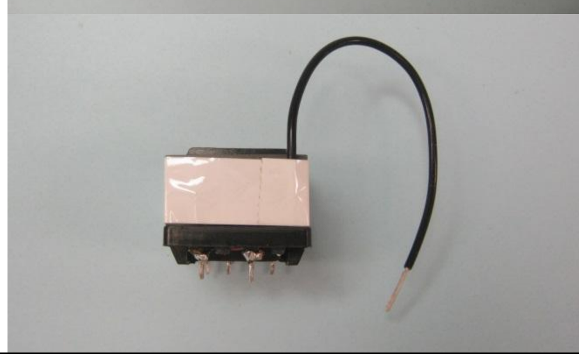
	 	
WD2A & WD2B **(Secondary)**	  	Using unserved Litz assembly prepared in step 1, start with FL1 on pins 5 and FL3 on pin 6, tightly wind 6 turns in secondary chamber. Finish with FL2 on pin 6 and FL4 on pin 8.

<table>
<tr><td></td><td></td><td></td></tr>
<tr><td>Bobbin Cover</td><td></td><td>Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.</td></tr>
<tr><td>Finish</td><td>
</td><td>Remove pins 2, 4 of bobbin. Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of copper tape [7] as shown, overlap ends, and solder. Solder 3” termination lead of stranded wire item [8] to core band close to pin 4 as shown, secure with two turns of tape item [4].</td></tr>
</table>

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	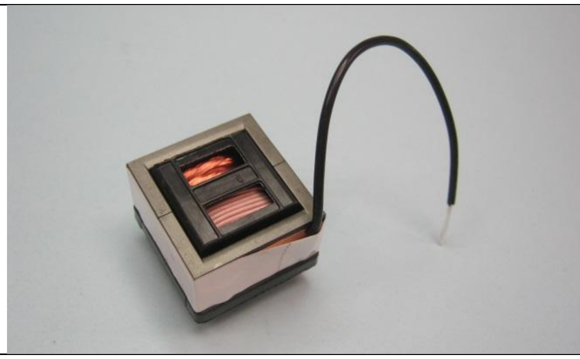	

8.3 *出力インダクタ (L3) の仕様*

8.3.1 *回路図*

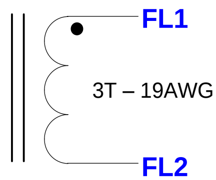

Figure 17 – Inductor Electrical Diagram.

8.3.2 *電気仕様*

Inductance	Pins FL1-FL2, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	300 nH, ±15%

8.3.3 *材料リスト*

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26.
[2]	Magnet wire: #19 AWG Solderable Double Coated.

8.3.4 *構造*

Figure 16 – Finished Part, Front View. Tin Leads to within ~ 1/8" of Toroid Body.

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9 PFC の設計計算シート

In this design, the spreadsheet generated warnings concerning the high value of KP selected, and for the operating current density of the Litz wire size selected for this design.

A high KP value can impact power factor and distortion, so a design generating this warning should be checked for any adverse impact. **This design met the requirements for power factor and harmonic distortion, and the high KP value allowed selection of a ferrite core for the PFC inductor, with consequent efficiency improvement.**

A warning for current density indicates that the design should be checked in its initial stages for excessive temperature rise in the PFC inductor. The guidelines incorporated the spreadsheet are conservative, so that a warning does not necessarily mean that a given design will fail thermally. **The measured temperature rise for this design was satisfactory.**

Hiper_PFS-II_Boost_062013; Rev.1.1; Copyright Power Integrations 2013	INPUT	INFO	OUTPUT	UNITS	Hiper_PFS-II_Boost_062013_Rev1-1.xls; Continuous Mode Boost Converter Design Spreadsheet
Enter Applications Variables					
Input Voltage Range			Universal		Input voltage range
VACMIN			90	V	Minimum AC input voltage
VACMAX			265	V	Maximum AC input voltage
VBROWNIN			76.69		Expected Minimum Brown-in Voltage
VBROWNOUT			68.33	V	Specify brownout voltage.
VO			385.00	V	Nominal Output voltage
PO	160.00		160.00	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	deg C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN
KP	0.750	*Warning*	0.75		!!!Warning. KP is too high. Reduce KP to below 0.675 for Ferrite cores and to below 0.8 for other core types
VO_MIN			365.75	V	Minimum Output voltage
VO_RIPPLE_MAX			20	V	Maximum Output voltage ripple
tHOLDUP	18.00		18	ms	Holdup time
VHOLDUP_MIN			310	V	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	no		no		Enter "Yes" for Forced air cooling. Otherwise enter "No"
PFS Parameters					
PFS Part Number	PFS7326H		PFS7326H		Selected PFS device
MODE	EFFICIENCY		EFFICIENCY		Mode of operation of PFS. For full mode enter "FULL" otherwise enter "EFFICIENCY" to indicate efficiency mode
R_RPIN			49.9	k-ohms	R pin resistor value
C_RPIN			1.00	nF	R pin capacitor value
IOCP min			6.80	A	Minimum Current limit

IOCP typ			7.20	A	Typical current limit
IOCP max			7.50	A	Maximum current limit
RDSON			0.62	ohms	Typical RDSon at 100 'C
RV1			1.50	Mohms	Line sense resistor 1
RV2			1.50	Mohms	Line sense resistor 2
RV3			1.00	Mohms	Line sense resistor 3
C_VCC			3.30	uF	Supply decoupling capacitor
R_VCC			15.00	ohms	VCC resistor
C_V			22.00	nF	V pin decoupling capacitor
C_C			22.00	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333.00	V	Power good Vo lower threshold voltage
PGT set resistor			103.79	kohm	Power good threshold setting resistor
FS_PK			60.2	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			50.2	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
IP			3.97	A	MOSFET peak current
PFS_IRMS			1.67	A	PFS MOSFET RMS current
PCOND_LOSS_PFS			1.73	W	Estimated PFS conduction losses
PSW_LOSS_PFS			0.78	W	Estimated PFS switching losses
PFS_TOTAL			2.51	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			15.30	degC/W	Maximum thermal resistance of heatsink
Basic Inductor Calculation					
LPFC			437	uH	Value of PFC inductor at peak of VACMIN and Full Load
LPFC (0 Bias)			437	uH	Value of PFC inductor at No load. This is the value measured with LCR meter
LP_TOL	5.00		5	%	Tolerance of PFC Inductor Value
LPFC_RMS			1.97	A	Inductor RMS current (calculated at VACMIN and Full Load)
Inductor Construction Parameters					
Core Type	Ferrite		Ferrite		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	Auto		PC44		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44 or equivalent for Ferrite cores. Fixed at 52 material for Pow Iron cores.
Core Geometry	Auto		PQ		Select from Toroid or EE for Sendust cores and from EE, or PQ for Ferrite cores
Core	PQ32/20		PQ32/20		Core part number
AE			170	mm^2	Core cross sectional area
LE			55.5	mm	Core mean path length
AL			6530	nH/t^2	Core AL value
VE			9.44	cm^3	Core volume
HT			5.12	mm	Core height/Height of window
MLT			67.1	cm	Mean length per turn
BW			8.98	mm	Bobbin width
NL			58		Inductor turns
LG			2.06	mm	Gap length (Ferrite cores only)
ILRMS			1.97	A	Inductor RMS current
Wire type	LITZ		LITZ		Select between "Litz" or "Regular" for double coated magnet wire
AWG	38		38	AWG	Inductor wire gauge
Filar	30		30		Inductor wire number of parallel strands

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OD			0.102	mm	Outer diameter of single strand of wire
AC Resistance Ratio			1.01		Ratio of AC resistance to the DC resistance (using Dowell curves)
J		*Warning*	8.11	A/mm^2	!!! Warning Current density is too high and may cause heating in the inductor wire. Reduce J
BP_TARGET			3500	Gauss	Target flux density at VACMIN (Ferrite cores only)
BM			1757	Gauss	Maximum operating flux density
BP			3487	Gauss	Peak Flux density (Estimated at VBROWNOUT)
LPFC_CORE_LOSS			0.09	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			1.80	W	Estimated Inductor copper losses
LPFC_TOTAL LOSS			1.89	W	Total estimated Inductor Losses
FIT			79.72%	%	Estimated FIT factor for inductor
Layers			5.1		Estimated layers in winding
Critical Parameters					
IRMS			1.91	A	AC input RMS current
IO_AVG			0.42	A	Output average current
Output Diode (DO)					
Part Number	Auto		INTERNAL		PFC Diode Part Number
Type			SPECIAL		Diode Type - Special - Diodes specially catered for PFC applications, SiC - Silicon Carbide type, UF - Ultrafast recovery type
Manufacturer			PI		Diode Manufacturer
VRRM			600	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
TRR			31	ns	Diode Reverse recovery time
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			0.61	W	Estimated Diode conduction losses
PSW_DIODE			0.16	W	Estimated Diode switching losses
P_DIODE			0.77	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.85	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			15.30	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
CO	Auto		120.00	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			11.9	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			19.5	ms	Expected holdup time with selected Output capacitor
ESR_LF			1.38	ohms	Low Frequency Capacitor ESR
ESR_HF			0.55	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.29	A	Low Frequency Capacitor RMS current
IC_RMS_HF			0.85	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.12	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.39	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.51	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
I^2t Rating			8.43	A^2s	Minimum I^2t rating for fuse
Fuse Current rating			3.00	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			1.86	A	Input average current at 70 VAC.

PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			3.10	W	Estimated Bridge Diode conduction loss
CIN			0.47	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT			9.37	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
Feedback Components					
R1			1.50	Mohms	Feedback network, first high voltage divider resistor
R3			1.60	Mohms	Feedback network, third high voltage divider resistor
R2			787.00	kohms	Feedback network, second high voltage divider resistor
C1			47.00	nF	Feedback network, loop speedup capacitor
R4			60.40	kohms	Feedback network, lower divider resistor
R6			487.00	kohms	Feedback network - pole setting resistor
R7			6.98	kohms	Feedback network - zero setting resistor
C2			47.00	nF	Feedback component- noise suppression capacitor
R5			3.00	kohms	Damping resistor in serise with C3
C3			2.20	uF	Feedback network - compensation capacitor
D1			BAV116		Feedback network - capacitor failure detection Diode
Loss Budget (Estimated at VACMIN)					
PFS Losses			2.51	W	Total estimated losses in PFS
Boost diode Losses			0.77	W	Total estimated losses in Output Diode
Input Bridge losses			3.10	W	Total estimated losses in input bridge module
Inductor losses			1.89	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.51	W	Total estimated losses in Output capacitor
Total losses			8.78	W	Overall loss estimate
Efficiency			0.95		Estimated efficiency at VACMIN. Verify efficiency at other line voltages

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10 LLC の設計計算シート

HiperLCS_040312; Rev.1.3; Copyright Power Integrations 2012	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_040312_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom			380	V	Nominal LLC input voltage
Vbrownout	287		287	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			362	V	Startup threshold on bulk capacitor
VOV_shut			476	V	OV protection on bulk voltage
VOV_restart			459	V	Restart voltage after OV protection.
CBULK	120.00		120	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			23.8	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	43.00		43.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	3.50		3.5	A	Main output maximum current
VD1	0.70		0.70	V	Forward voltage of diode in Main output
PO1			151	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			151	W	Specified LLC output power
LCS Device Selection					
Device	LCS702		LCS702		LCS Device
RDS-ON (MAX)			1.39	ohms	RDS-ON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.5	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			103	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			27	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	380		380	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			153	W	LLC output power including diode loss
Vo			43.70	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target			250	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			291	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri			341	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom
Lres	50.00		50.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			5.8		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	8.20		8.2	nF	Series resonant capacitor. Red background cells produce red

				graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec		14.618	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m		50	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq		4.47		Turns ratio of LLC equivalent circuit ideal transformer
Npri	29.0	29.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	6.0	6.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted		227	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res		249	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout		155	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par		95	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion		135	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion		247	V	LLC full load gain inversion point input voltage
Vres_expected		390	V	
RMS Currents and Voltages				
IRMS_LLC_Primary		1.03	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current		2.8	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current		1.8	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current		0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current		0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms		88	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)				
New primary turns		29.0		Trial transformer primary turns; default value is from resonant section
New secondary turns		6.0		Trial transformer secondary turns; default value is from resonant section
New Lpri		341	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres		8.2	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above
New estimated Lres		50.0	uH	Trial transformer estimated Lres
New estimated Lpar		291	uH	Estimated value of Lpar for trial transformer
New estimated Lsec		14.618	uH	Estimated value of secondary leakage inductance
New Kratio		5.8		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio		4.47		Estimated effective transformer turns ratio
V powertrain inversion new		247	V	Input voltage at LLC full load gain inversion point
f_res_trial		249	kHz	New Series resonant frequency
f_predicted_trial		227	kHz	New nominal operating frequency
IRMS_LLC_Primary		1.03	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current		2.7	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape

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Lower Secondary Voltage Capacitor RMS current		1.6	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current		2.7	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current		0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial		390	V	Expected value of input voltage at which LLC operates at resonance.
Transformer Core Calculations (Calculates From Resonant Parameter Section)				
Transformer Core	Auto	EEL25		Transformer Core
Ae	0.76	0.76	cm^2	Enter transformer core cross-sectional area
Ve	5.35	5.35	cm^3	Enter the volume of core
Aw		107.9	mm^2	Area of window
Bw	15.50	15.5	mm	Total Width of Bobbin
Loss density		200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT	5.20	5.2	cm	Mean length per turn
Nchambers	2	2		Number of Bobbin chambers
Wsep	1.60	1.6	mm	Winding separator distance (will result in loss of winding area)
Ploss		1.1	W	Estimated core loss
Bpkfmin		155	mT	First Quadrant peak flux density at minimum frequency.
BAC		211	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding				
Npri		29.0		Number of primary turns; determined in LLC resonant section
Primary gauge	44	44	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge		0.050	mm	Equivalent diameter of wire in metric units
Primary litz strands	125	125		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor		50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P		48	mm^2	Winding window area for primary
Fill Factor		25%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary		75.42	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C		113.73	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C		152.40	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current		1.03	A	Measured RMS current through the primary winding
ACR_Trf_Primary		259.81	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss		0.27	W	Total primary winding copper loss at 85 C
Primary Layers		3.02		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)				**Note - Power loss calculations are for each winding half of secondary**
Output Voltage		43.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns		6.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)		2.8	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)		1.75	A	DC component of winding current
Winding current (AC RMS component)		2.17	A	AC component of winding current
Sec 1 Wire gauge		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge		0.060	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	165	165		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1		35.93	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1		11.21	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1		15.02	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1		0.37	W	Estimated Power loss due to DC resistance (both secondary

			phases)
ACR_Sec1	15.25	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1	0.14	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses	0.51	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current	1.8	A	Output capacitor RMS current
Co1	1.8	uF	Secondary 1 output capacitor
Capacitor ripple voltage	3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current	2.8	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers	1.00		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)			**Note - Power loss calculations are for each winding half of secondary**
Output Voltage	0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns	0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)	2.8	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)	0.0	A	DC component of winding current
Winding current (AC RMS component)	0.0	A	AC component of winding current
Sec 2 Wire gauge	42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge	0.060	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2	59292.53	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT	5.20	cm	Mean length per turn
DCR_25C_Sec2	0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2	0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1	0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2	0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2	0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses	0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current	0.0	A	Output capacitor RMS current
Co2	N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage	N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current	0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers	1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations			Does not include fringing flux loss from gap
Primary copper loss (from Primary section)	0.27	W	Total primary winding copper loss at 85 C
Secondary copper Loss	0.51	W	Total copper loss in secondary winding
Transformer total copper loss	0.78	W	Total copper loss in transformer (primary + secondary)
AW_S	48.38	mm^2	Area of window for secondary winding
Secondary Fill Factor	19%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values			
f_min	155	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time	320	ns	Dead time
Burst Mode 1	1		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max	847	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start	382	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period

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f_burst_stop	437	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor	6.79	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor	129	k-ohms	Resistor from DT/BF pin to G pin
Rstart	5.79	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay	0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin	46.2	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart	0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto	1.2	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor 19.60	19.6	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor	2.93	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit			
Slow current limit	2.35	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit	4.24	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor	47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor	37.3	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor	220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor	1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency	724	kHz	This pole attenuates IS pin signal
Loss Budget			
LCS device Conduction loss	1.5	W	Conduction loss at nominal line and full load
Output diode Loss	2.5	W	Estimated diode losses
Transformer estimated total copper loss	0.78	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss	1.1	W	Estimated core loss
Total transformer losses	1.9	W	Total transformer losses
Total estimated losses	5.8	W	Total losses in LLC stage
Estimated Efficiency	96%	%	Estimated efficiency
PIN	156	W	LLC input power

11 ヒートシンク

11.1 *一次側ヒート シンク*

11.1.1 *一次側ヒート シンクのシート メタル*

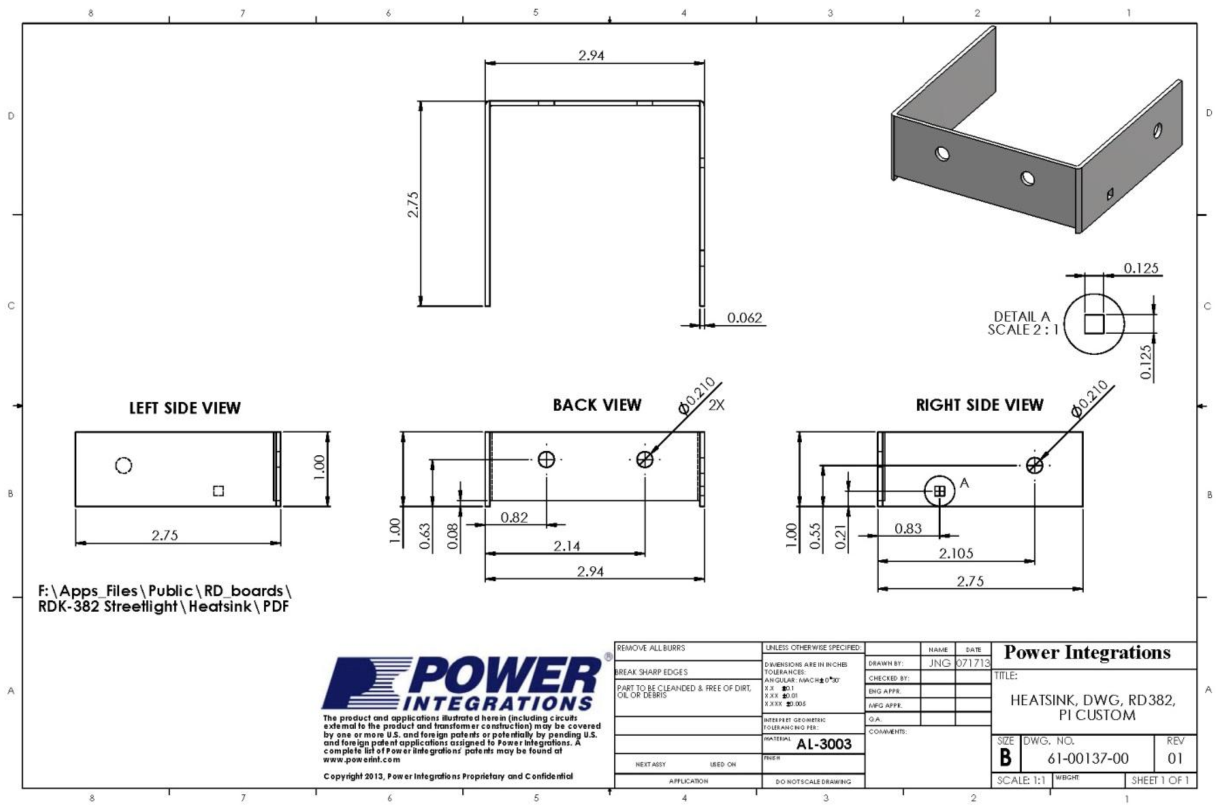

Figure 18 – RD-382 Primary Heat Sink Sheet Metal Drawing.

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11.1.2 一次側ヒート シンクと留め具

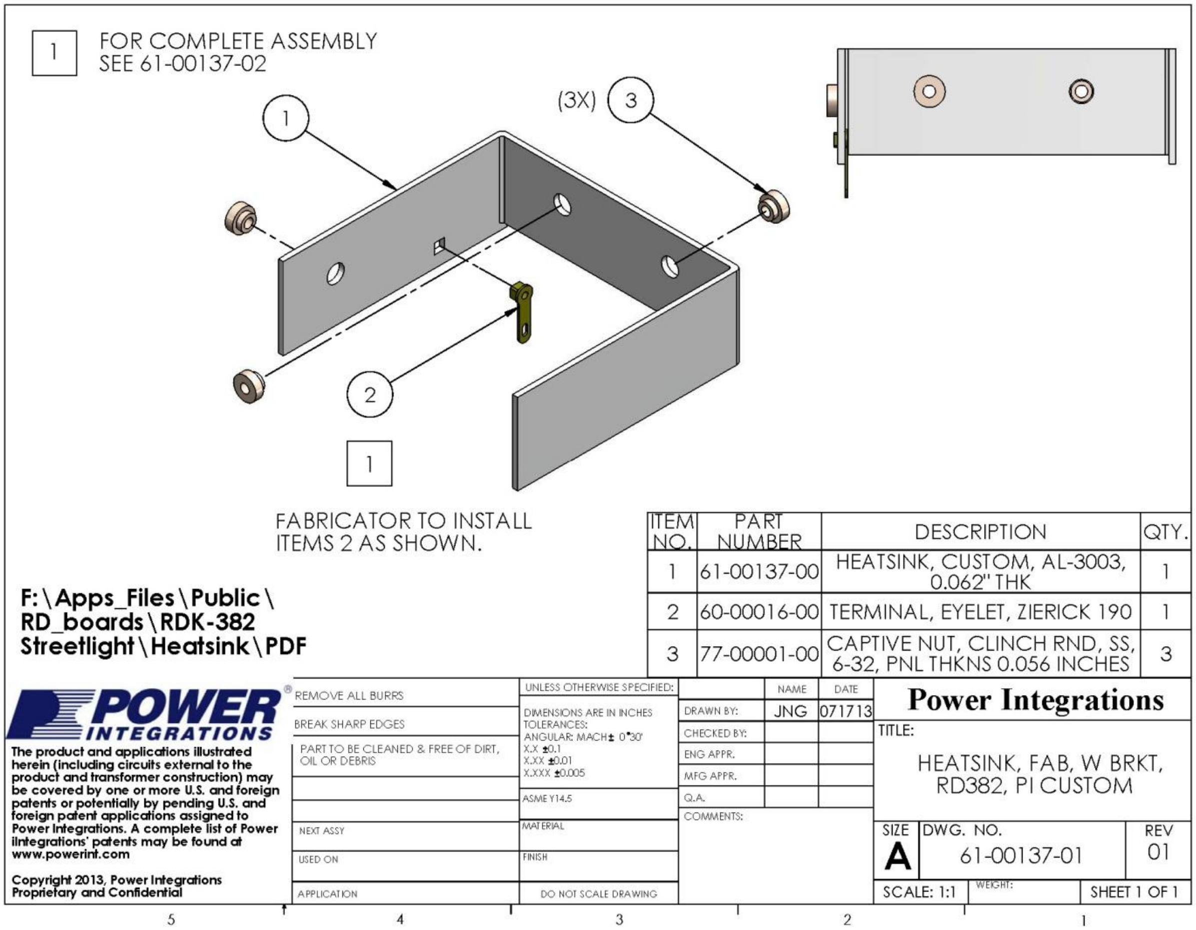

Figure 19 – Finished Primary Heat Sink Drawing with Installed Fasteners.

11.1.3 一次側ヒート シンク アセンブリ

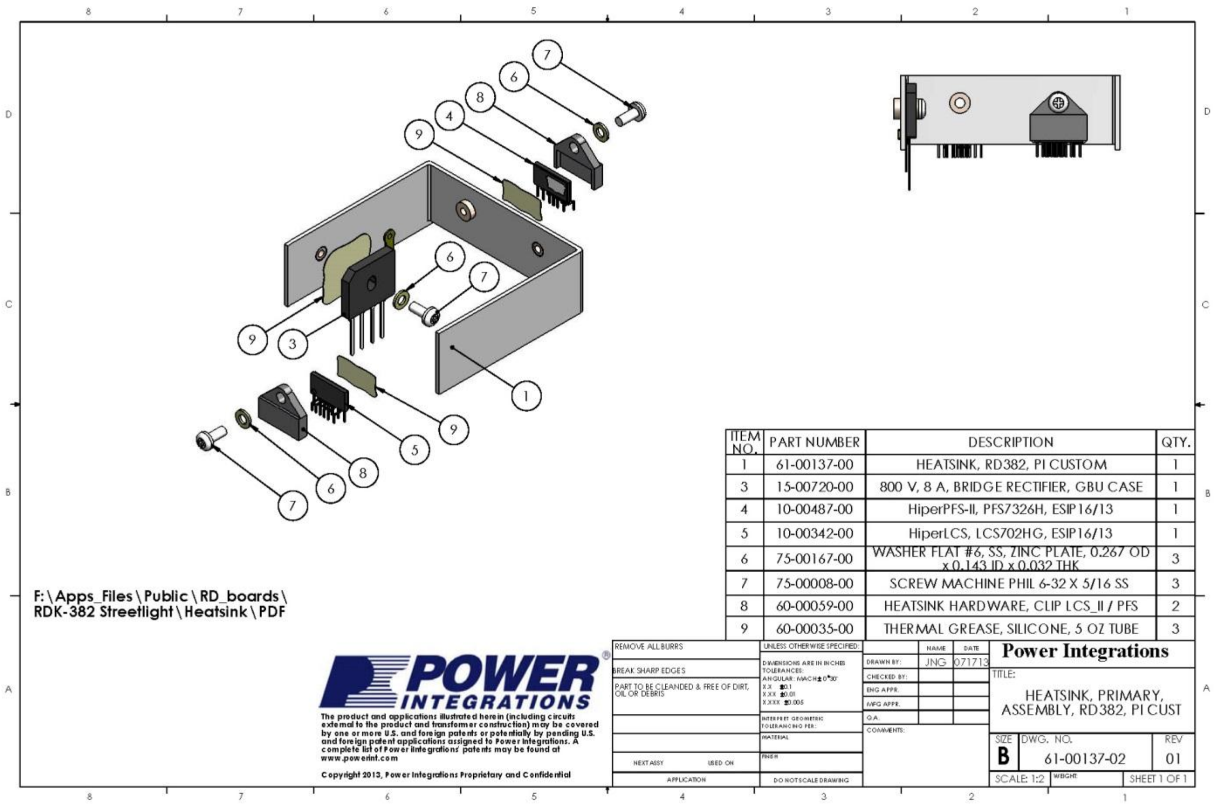

Figure 20 – RD-382 Primary Heat Sink Assembly.

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11.2 *二次側ヒート シンク*

11.2.1 *二次側ヒート シンクのシート メタル*

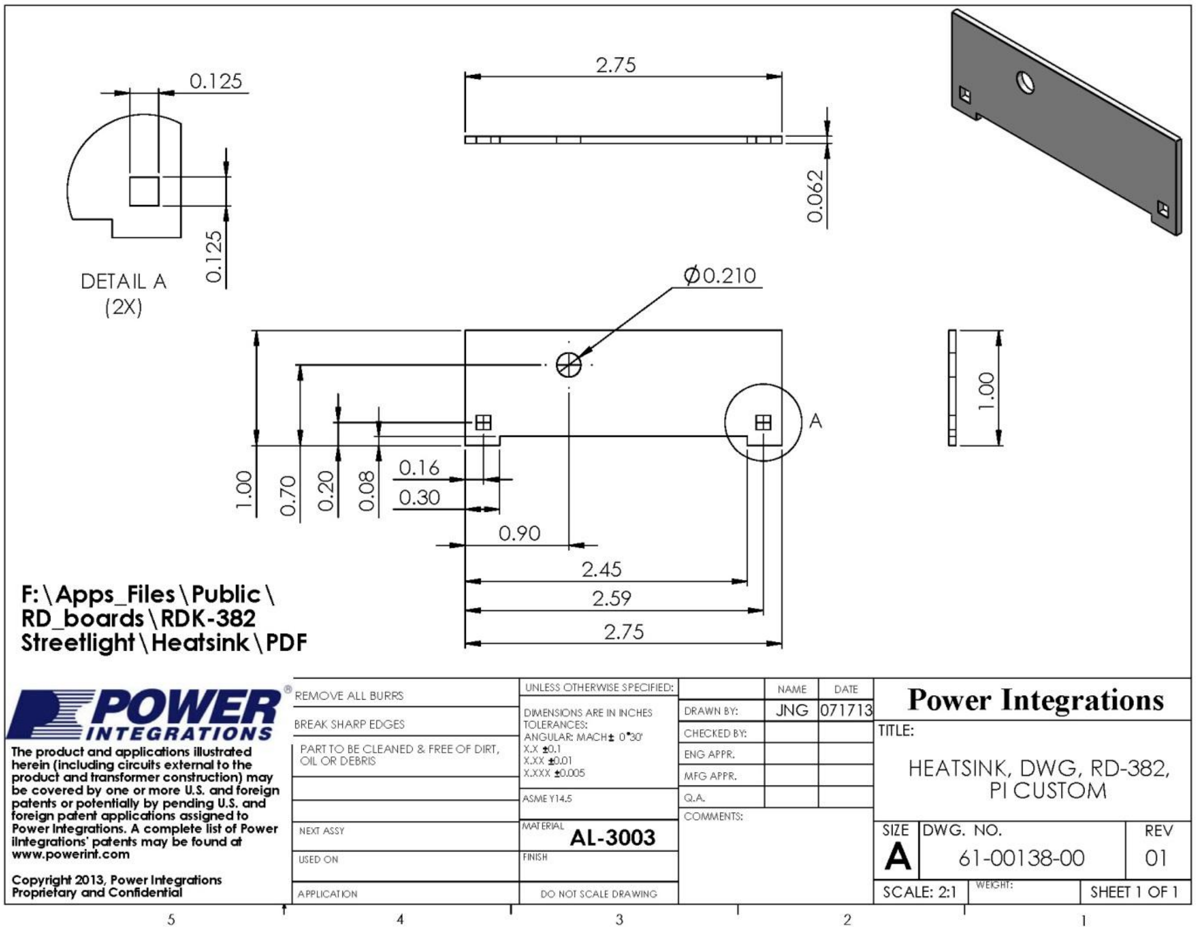

Figure 21 – Secondary Heat Sink Sheet Metal Drawing.

11.2.2 二次側ヒートシンクと留め具

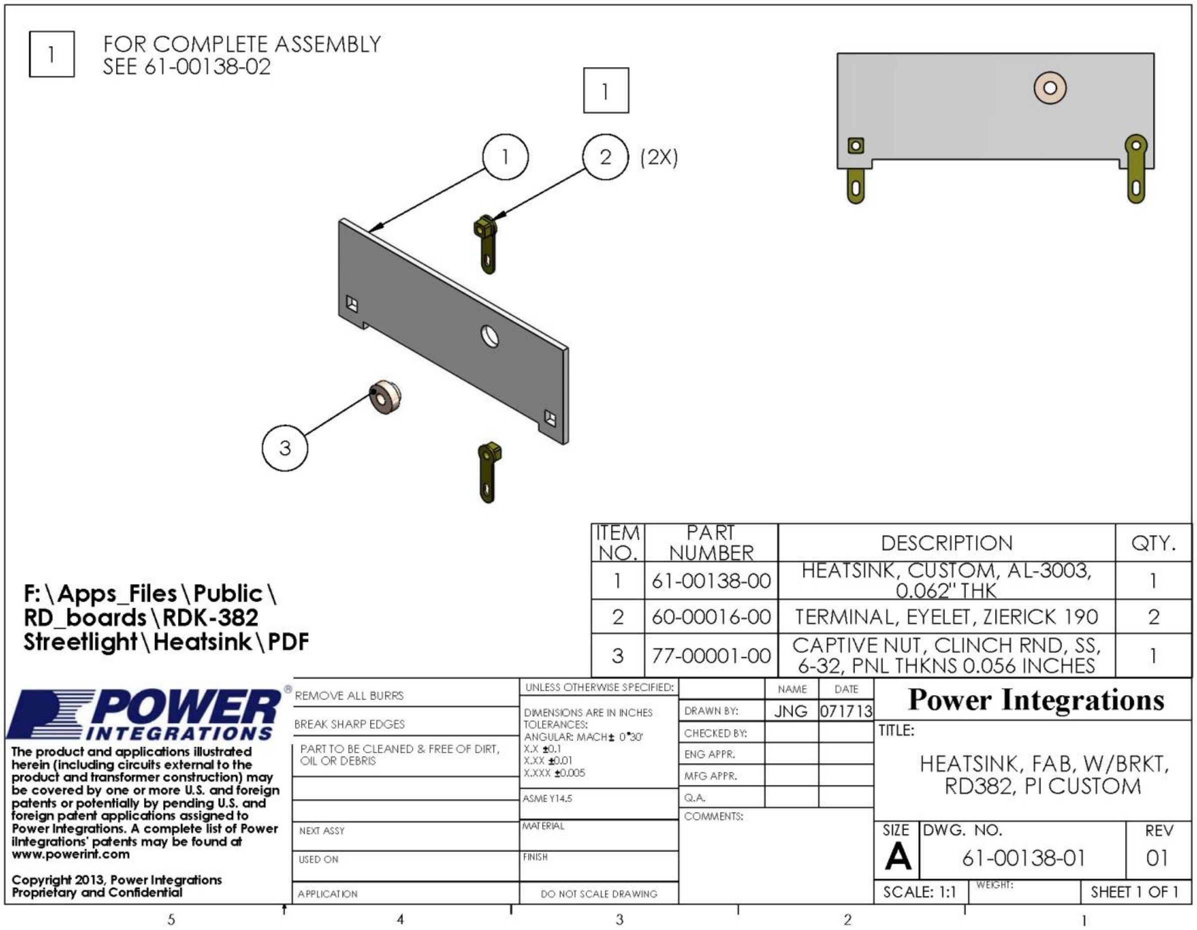

Figure 22 – Finished Secondary Heat Sink with Installed Fasteners.

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11.2.3 *二次側ヒート シンク アセンブリ*

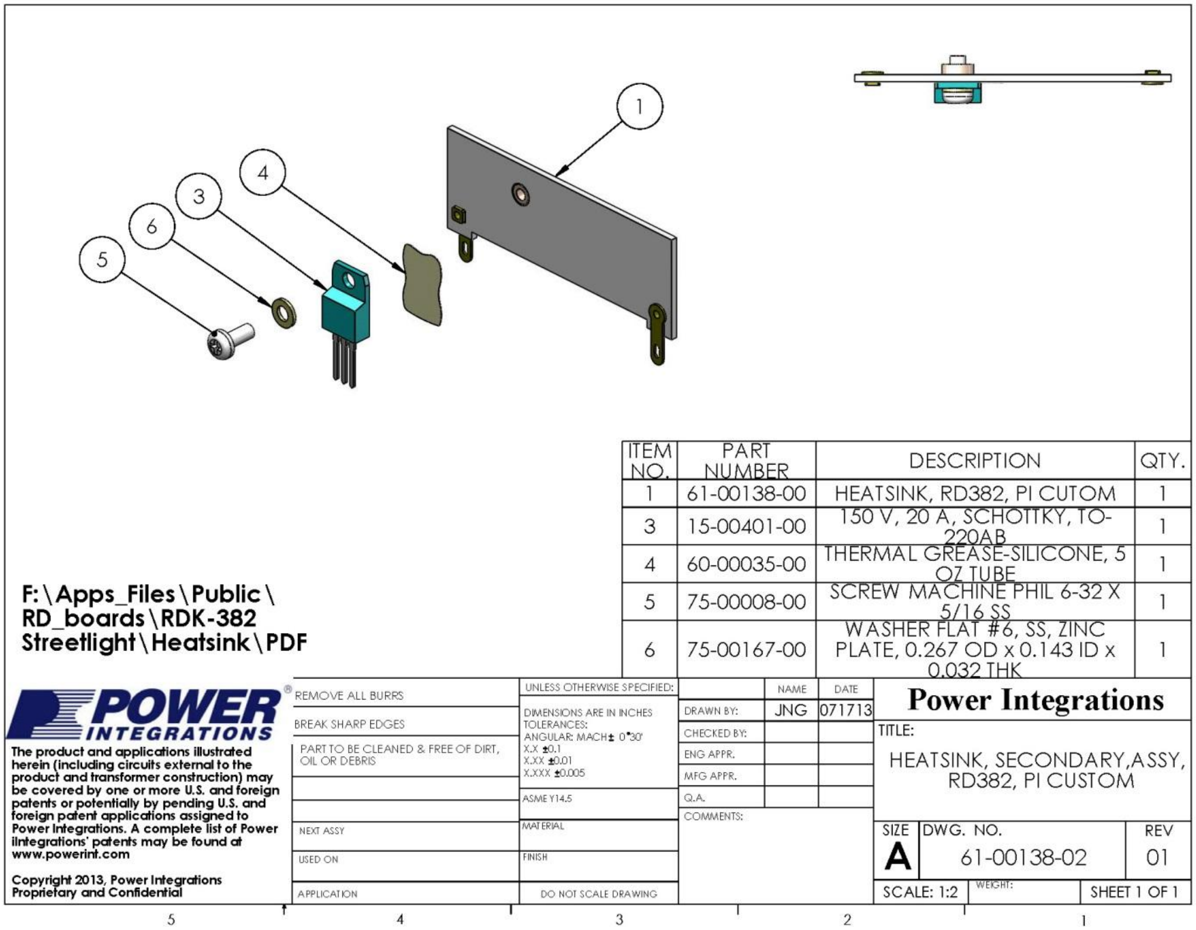

Figure 23 – RD-382 Secondary Heat Sink Assembly.

12 RD-382 の性能データ

All measurements were taken at room temperature and 60 Hz (input frequency) unless otherwise specified. Output voltage measurements were taken at the output connectors.

12.1 *LLC コンバータの効率*

To make this measurement, the LLC stage was supplied by connecting an external 380 VDC source across bulk capacitor C14, with a 2-channel bench supply to source the primary and secondary bias voltages. The output of the supply was used to power the LED streetlight described in Section 7, and the dimming input of the supply was used to program the current delivered to this load in order to vary the output power.

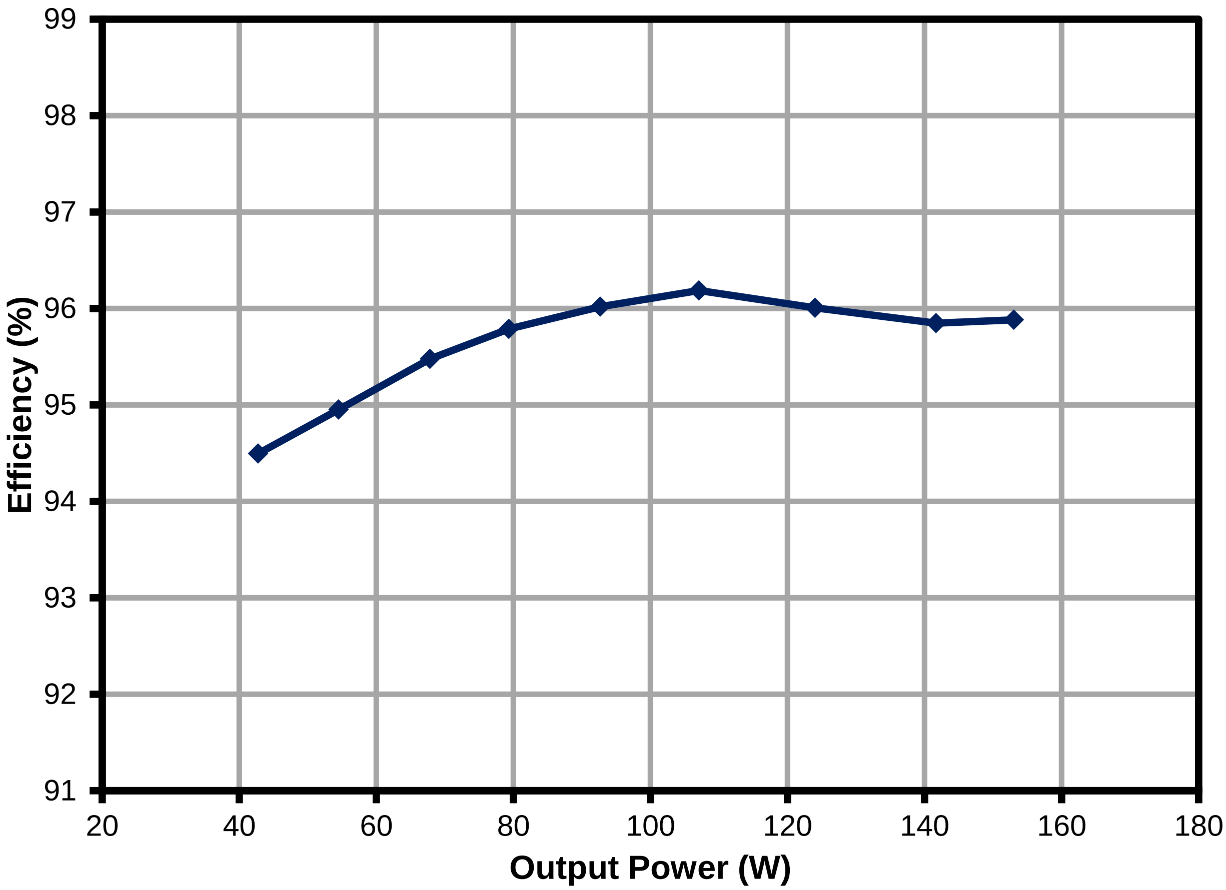

Figure 24 – LLC Stage Efficiency vs. Load, 380 VDC Input.

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12.2 ***総合効率***

Figures below show the total supply efficiency (PFC and LLC stages). AC input was supplied using a sine wave source. The output was loaded with an electronic load set for constant resistance, with the load adjusted for maximum output current (3.5 A) and 43 V output voltage.

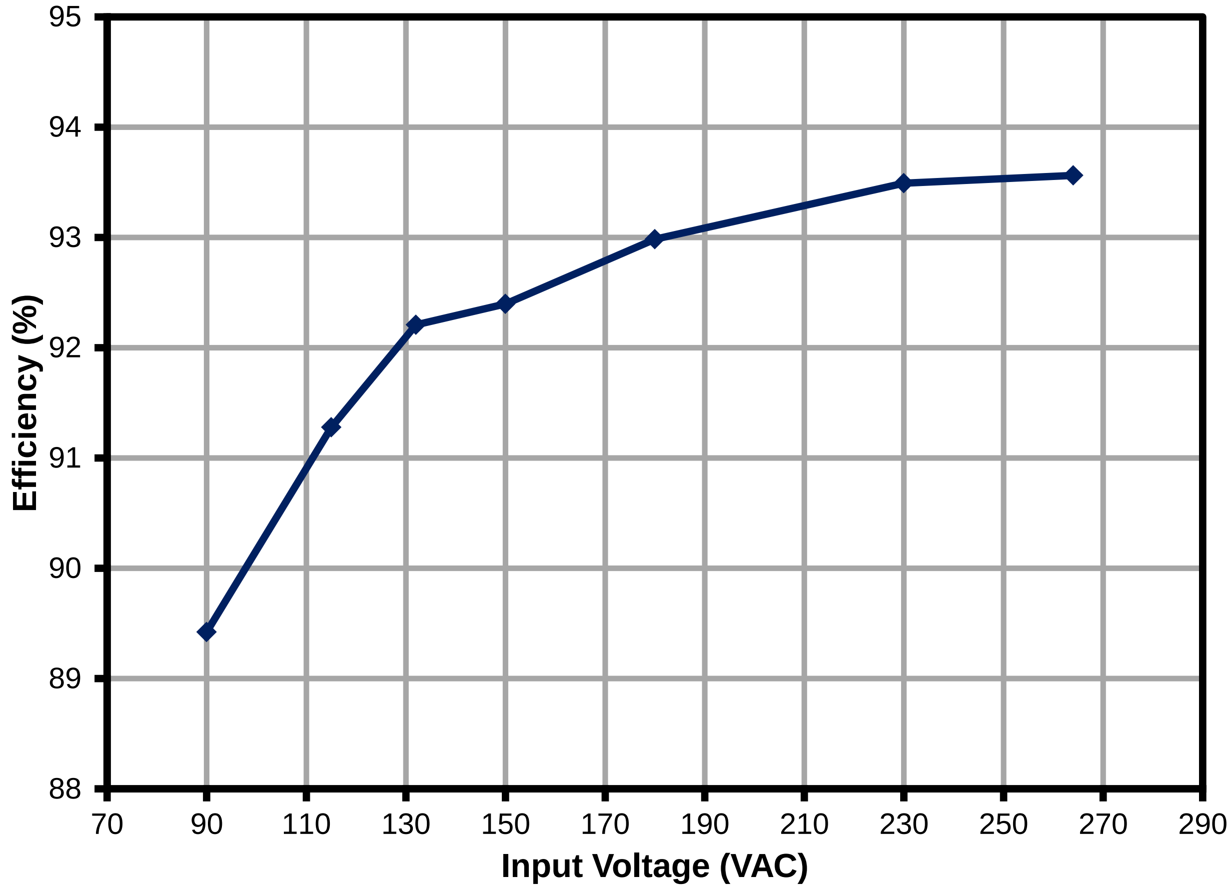

Figure 25 – Total Efficiency vs. Input Voltage, 100% Load.

12.3 力率

Power factor measurements were made using a sine wave AC source and a constant resistance electronic load as described in section 12.2.

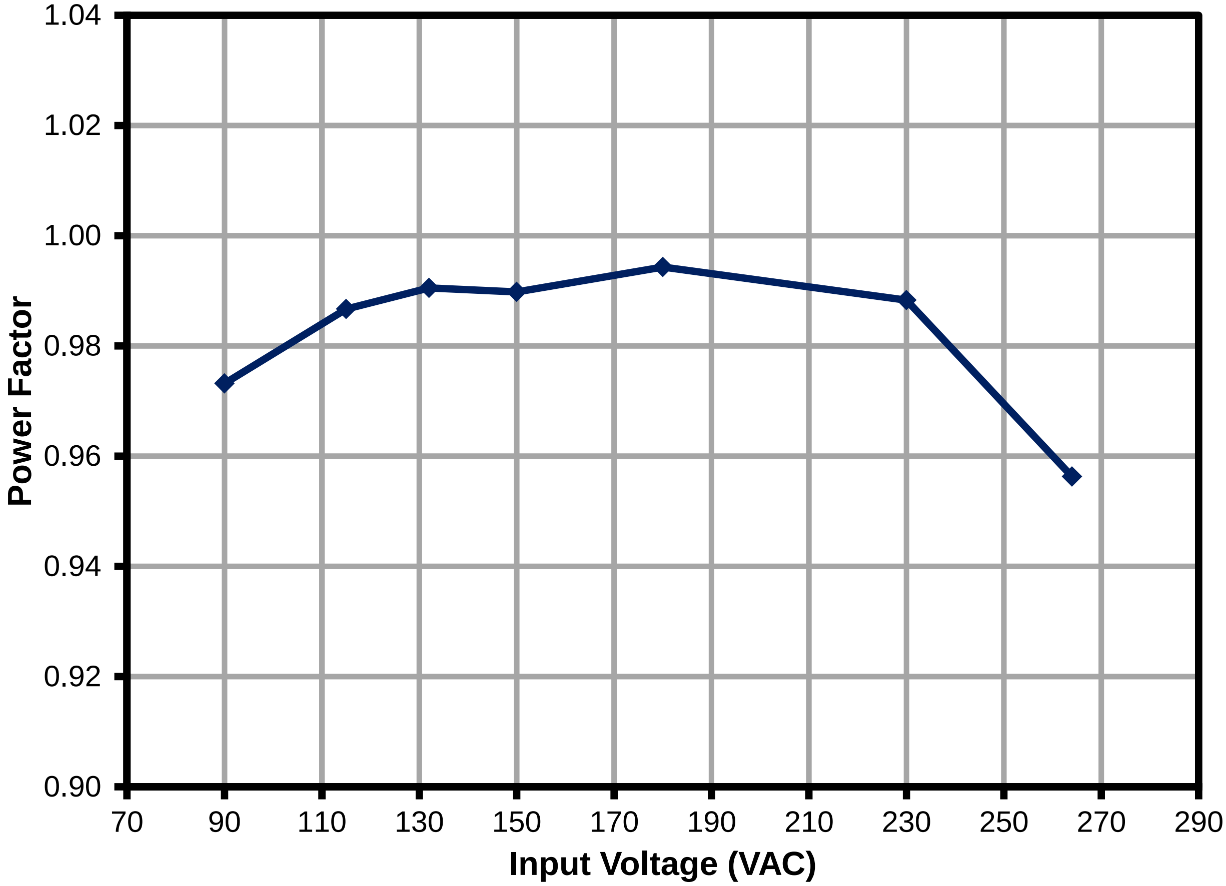

Figure 26 – Power Factor vs. Input Voltage, 100% Load.

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12.4 *高調波データ*

Input current harmonic distribution was measured using a sine wave source and an LED load (Section 7).

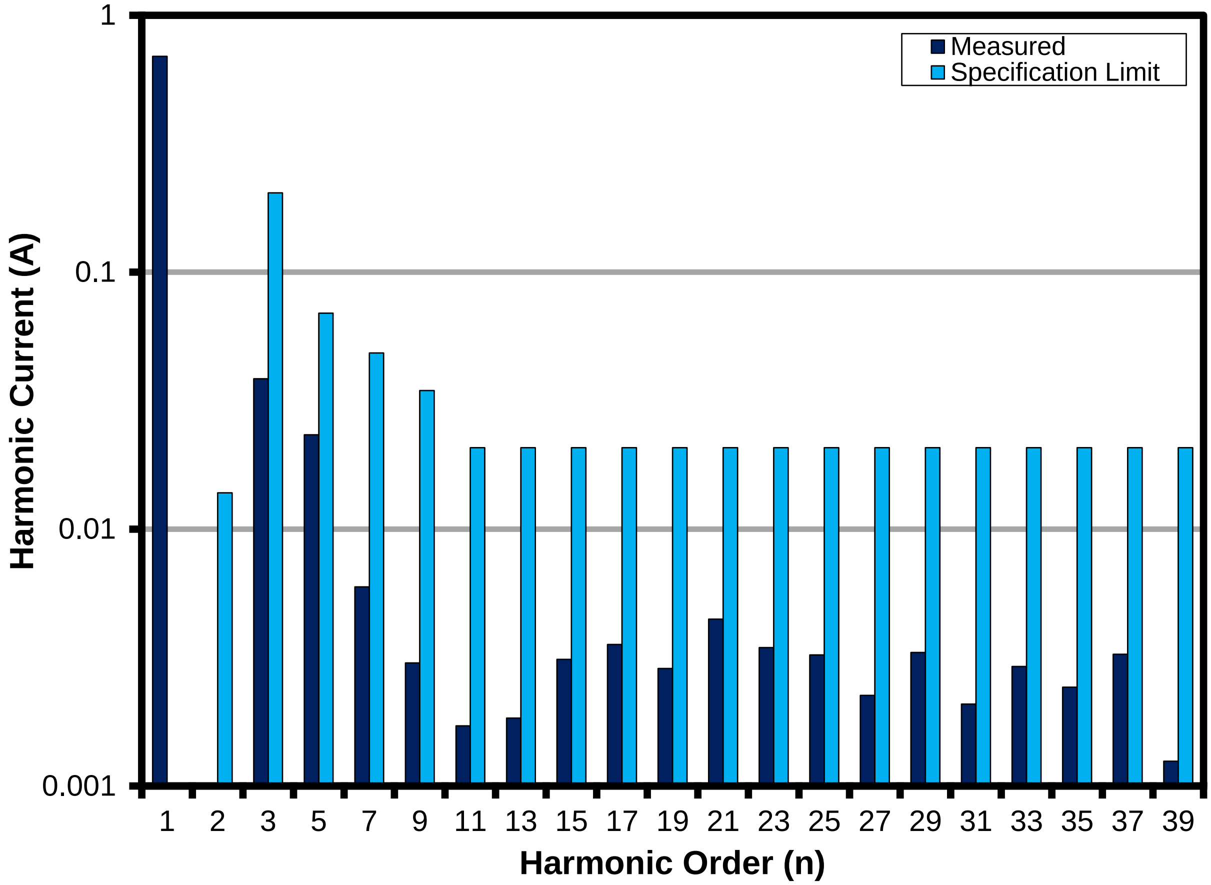

Figure 27 – Input Current Harmonic Distribution, 230 VAC / 50 Hz Input, 100% Load.

12.5 *THD、100% 負荷時*

THD was measured using the LED streetlight load described in Section 7 of this report.

Input Voltage (VAC)	Frequency (Hz)	THD (%)
115	60	8.30
230	50	7.38

12.6 ***出力電流対調光時の入力電圧***

Output dimming characteristics were measured using a sine wave AC source and the streetlight LED array described in Section 7. Dimming voltage was provided using a bench supply.

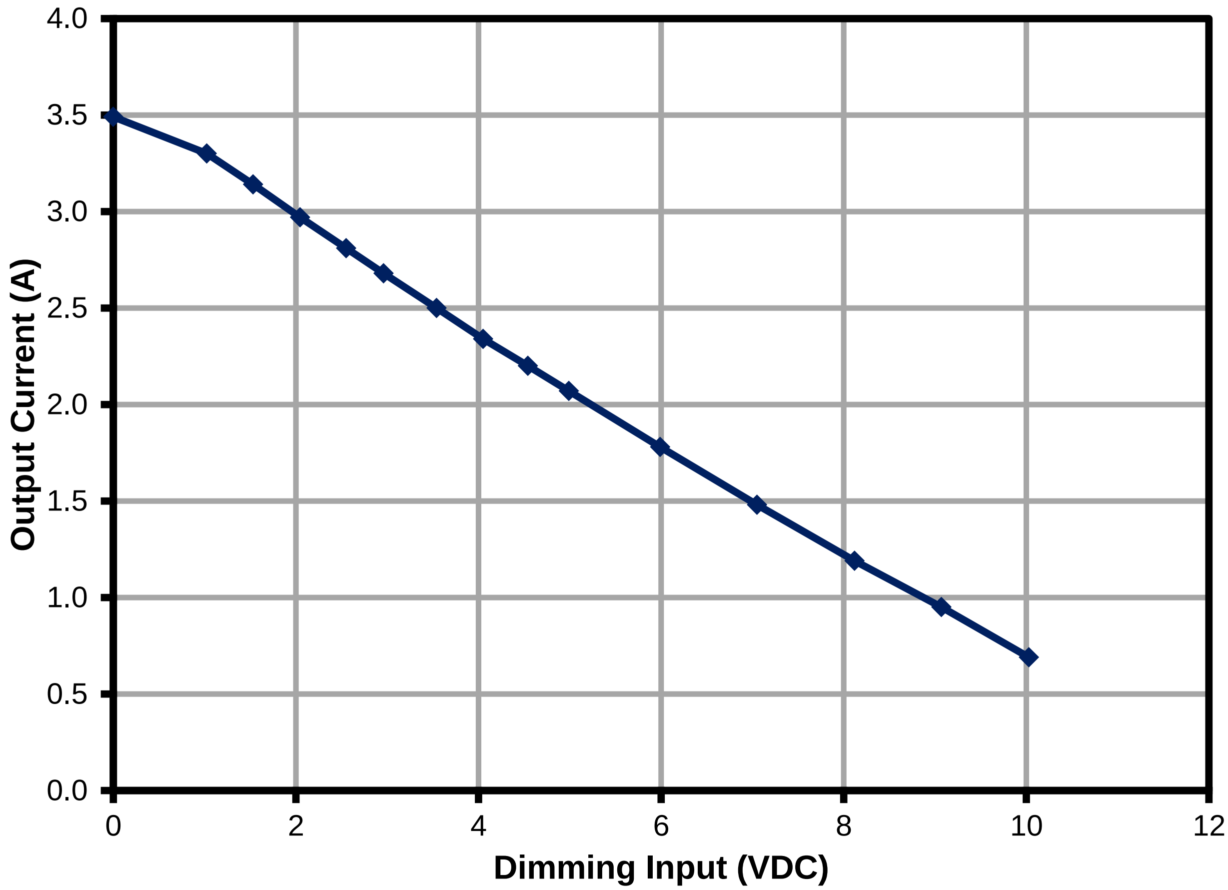

Figure 28 – RD-382 Output Current vs. Dimming Voltage.

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13 波形

13.1 *入力電流、100% 負荷時*

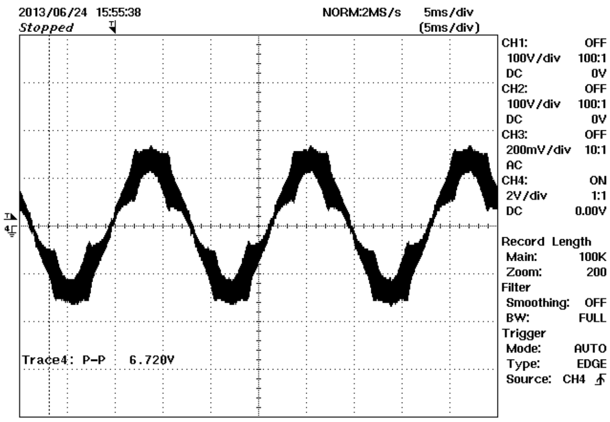

Figure 29 – Input Current, 90 VAC, 150 W Load, 2 A, 5 ms / div

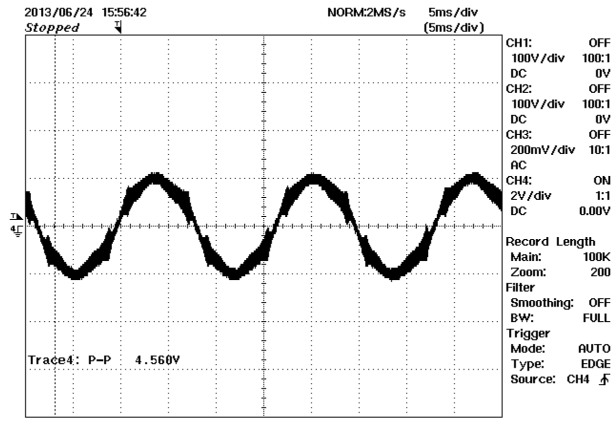

Figure 30 – Input Current, 115 VAC, 150 W Load, 2 A, 5 ms / div.

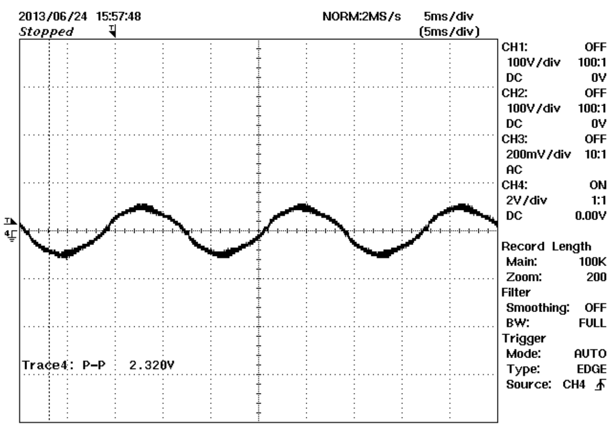

Figure 31 – Input Current, 230 VAC, 150 W Load, 2 A, 5 ms / div.

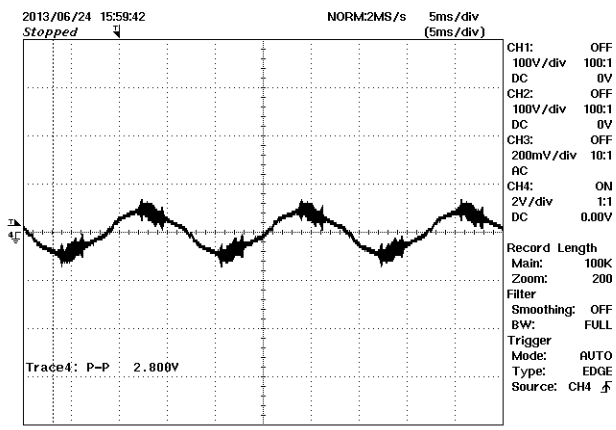

Figure 32 – Input Current, 265 VAC, 150 W Load, 2 A, 5 ms / div.

13.2 ***LLC 一次側電圧と電流***

The LLC stage current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C30 that measures the LLC transformer (T2) primary current. The output was loaded with an electronic load set for constant resistance, with the load adjusted for maximum output current and 43 V output voltage.

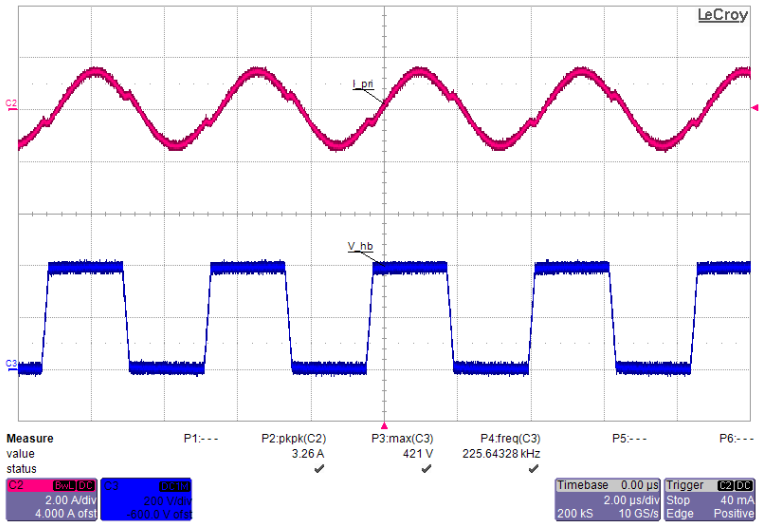

Figure 33 – LLC Stage Primary Voltage and Current, 100% Load.
Upper**:** Current, 2 A / div.
Lower**:** Voltage, 200 V, 2 µs / div.

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13.3 *出力整流器のピーク逆電圧*

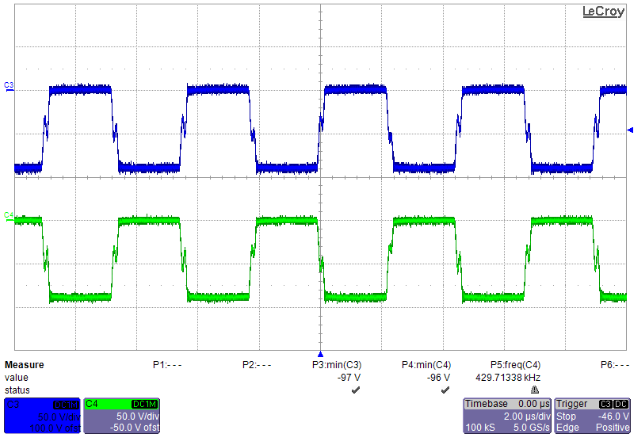

Figure 34 – Output Rectifier (D11) Reverse Voltage, 100% Load. Top and Bottom Traces Show Voltages on Each Half of D11, at 50 V, 2 µs / div.

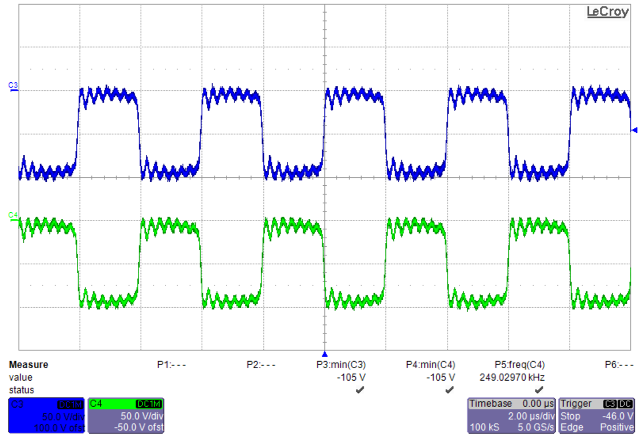

Figure 35 – Output Rectifier (D11) Reverse Voltage, No-Load. Top and Bottom Traces Show Voltages on Each Half of D11, at 50 V, 2 µs / div.

13.4 ***PFC インダクタ + スイッチ電圧と電流、100% 負荷時***

Since the PFC in this power supply utilizes the internal output diode of the HiperPFS-2, the measured drain current cannot be separated from the PFC inductor current.

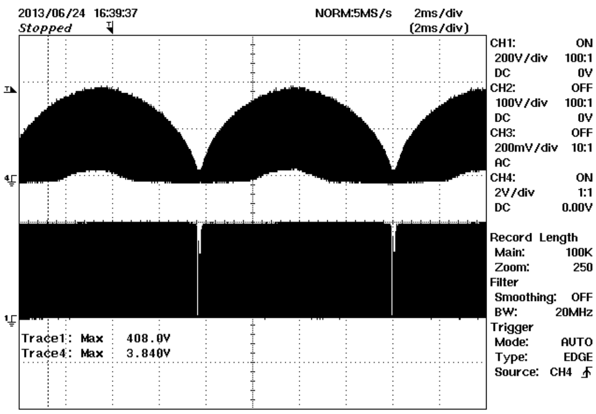

Figure 36 – PFC Stage Drain Voltage and Current, Full Load, 115 VAC.
Upper: Switch + Inductor Current, 2 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

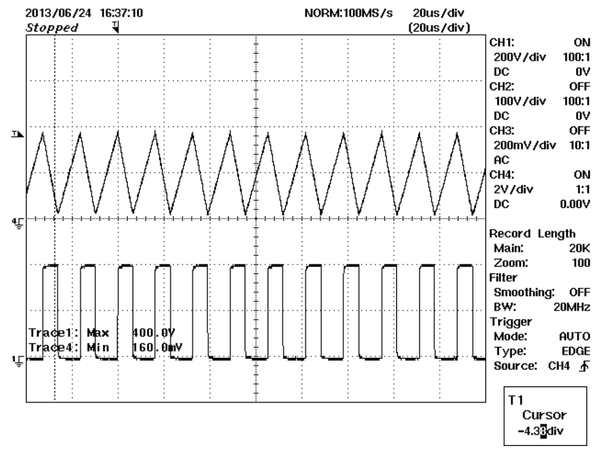

Figure 37 – PFC Stage Drain Voltage and Current, Full Load, 115 VAC.
Upper: Switch + Inductor Current, 2 A / div.
Lower: V_{DRAIN}, 200 V, 20 μs / div.

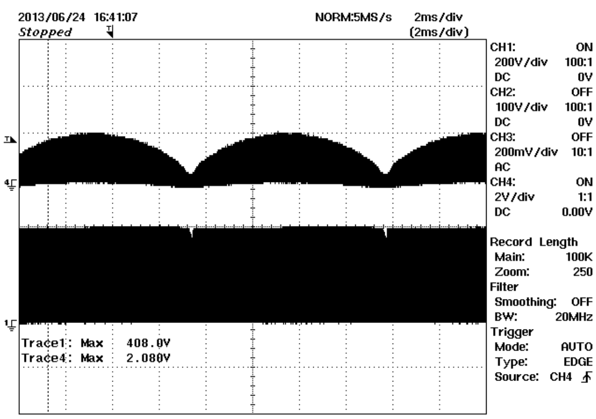

Figure 38 – PFC Stage Drain Voltage and Current, Full Load, 230 VAC.
Upper: Switch + Inductor Current, 2 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

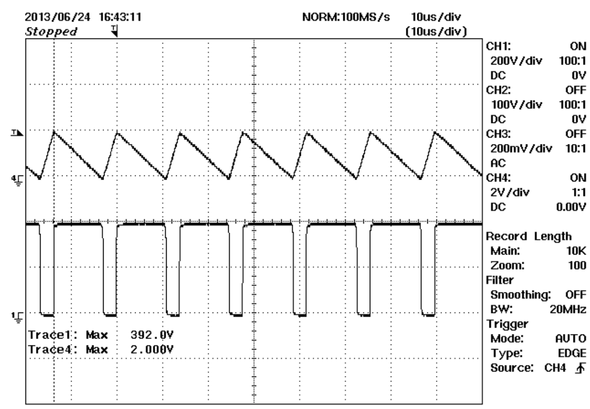

Figure 39 – PFC Stage Drain Voltage and Current, Full Load, 230 VAC.
Upper: Switch + Inductor Current, 2 A / div.
Lower: V_{DRAIN}, 200 V, 10 μs / div.

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13.5 *起動時の AC 入力電流と PFC 出力電流*

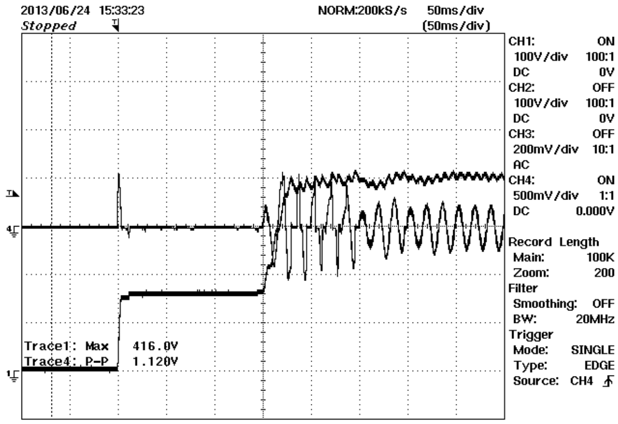

Figure 40 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 115 VAC.
Upper: AC Input Current, 25 A /div.
Lower: PFC Voltage, 100 V, 50 ms / div.

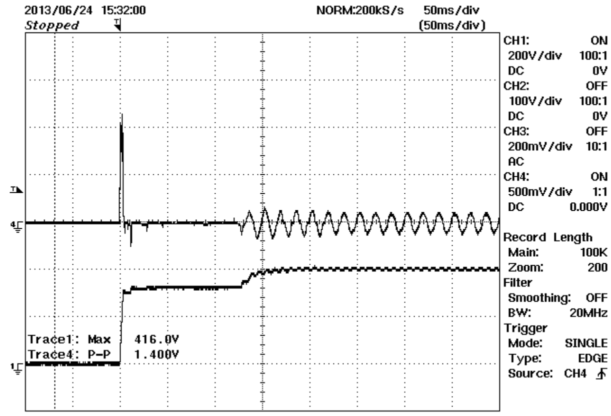

Figure 41 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 230 VAC.
Upper: AC Input Current, 5 A / div.
Lower: PFC Voltage, 200 V, 50 ms / div.

13.6 *LED 出力負荷時の LLC 起動出力電圧とトランスの一次電流*

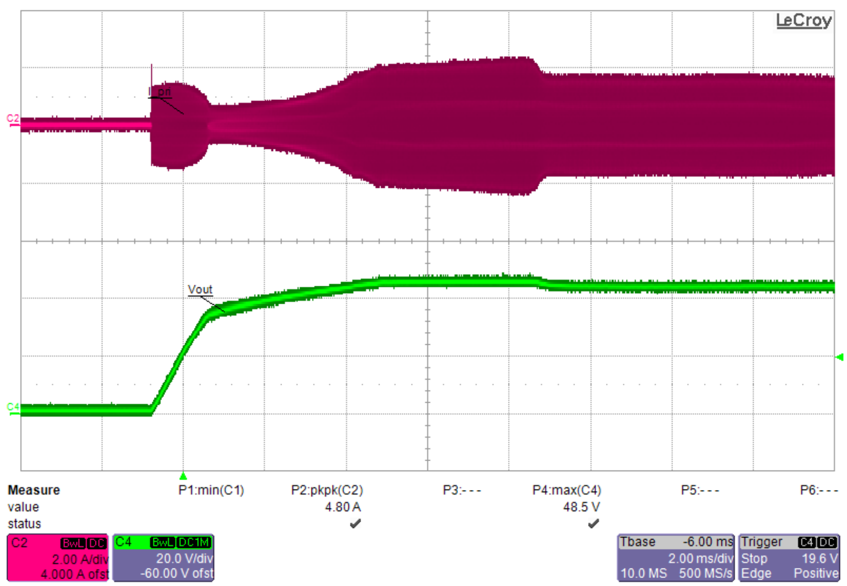

Figure 42 – LLC Start-up. 115 VAC, 100% Load.
Upper: LLC Primary Current, 2 A / div.
Lower: LLC V_{OUT}, 20 V, 2 ms / div.

13.7 ***LED 負荷使用時の起動時出力電圧及び出力電流***

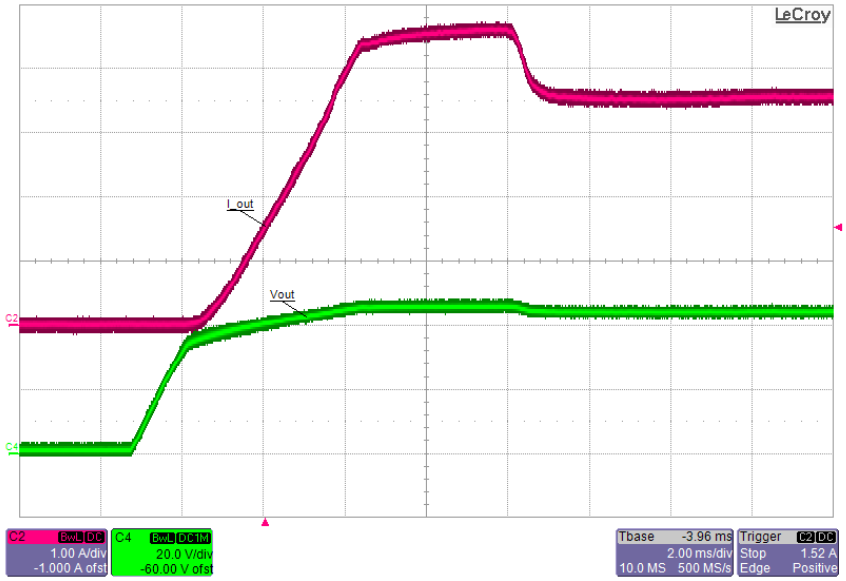

Figure 43 – LLC Start-up. 115 VAC, 100% Load, LED Load.
Upper: LLC I_{OUT}, 1 A / div.
Lower: LLC V_{OUT}, 20 V, 2 ms / div.

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13.8 *LLC 出力短絡保護回路*

The figure below shows the effect of an output short circuit on the LLC primary current and on the output current. A mercury displacement relay was used to short the output to get a fast, bounce-free connection.

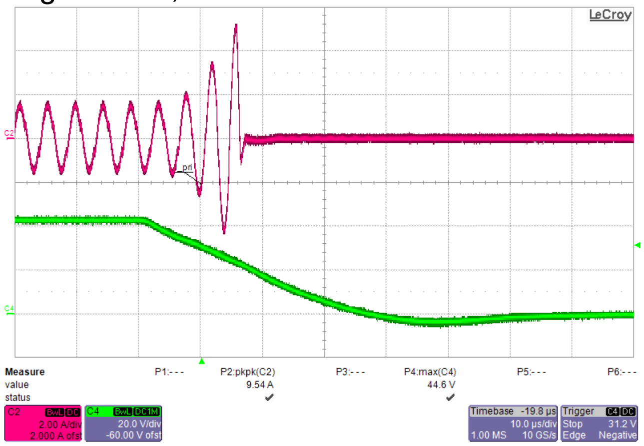

Figure 44 – Output Short-Circuit Test.
Upper: LLC Primary Current, 2 A / div.
Lower: LLC V_{OUT}, 20 V, 10 µs / div**.**

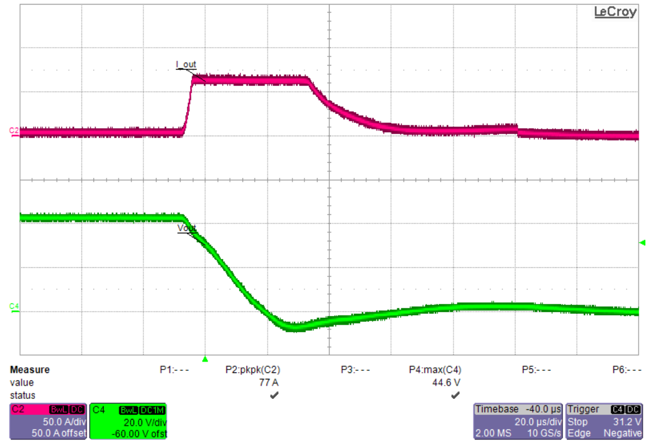

Figure 45 – Output Short-Circuit Test.
Upper: LLC I_{OUT}, 50 A / div.
Lower: LLC V_{OUT}, 20 V, 10 µs / div.

13.9 *出力リップルの測定*

13.9.1 *リップルの測定方法*

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

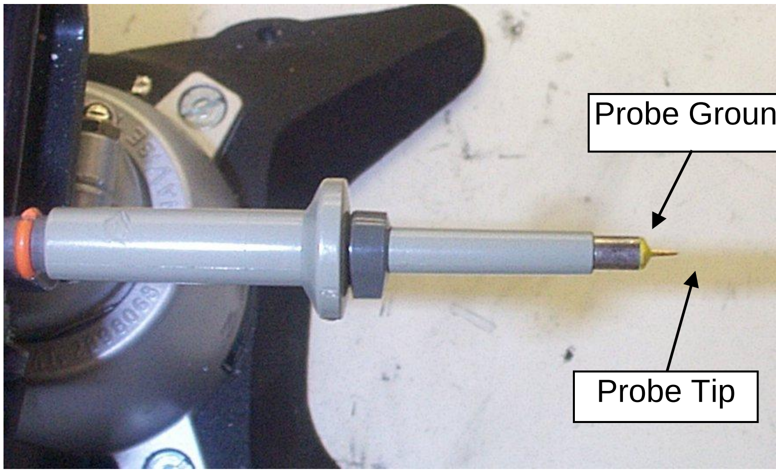

Figure 46 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

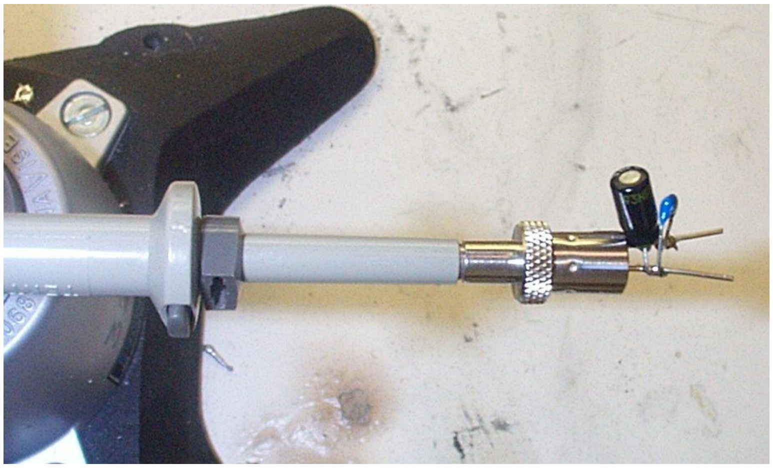

Figure 47 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

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13.9.2 *リップル測定*

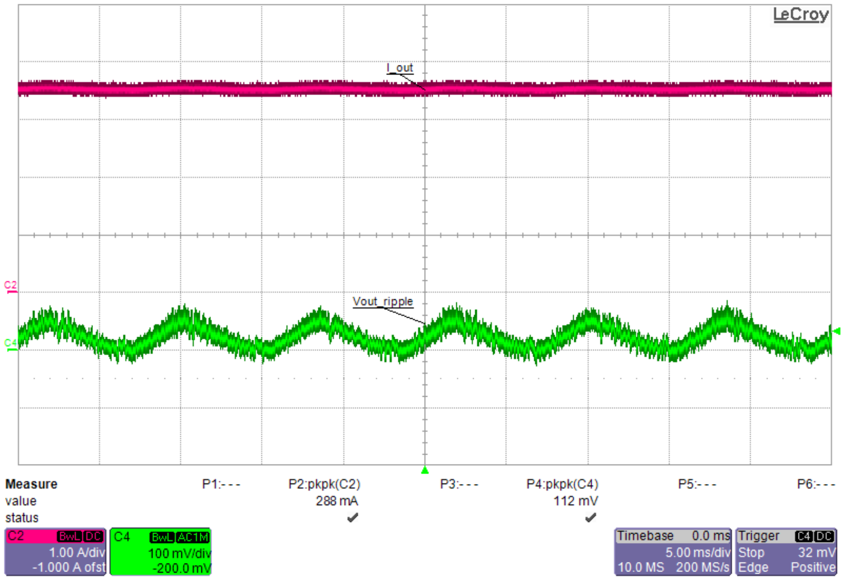

Figure 48 – Output Ripple, Full Load, 115 VAC.
Upper: I_{OUT}, 1 A / div.
Lower: Output Voltage Ripple, 100 mV, 5 ms / div.

14 温度プロファイル

The board was operated at room temperature, with output set at maximum using a constant resistance load. For each test condition the unit was allowed to thermally stabilize (~1 hr) before measurements were made.

14.1 *90 VAC、60 Hz、150 W 出力、室温*

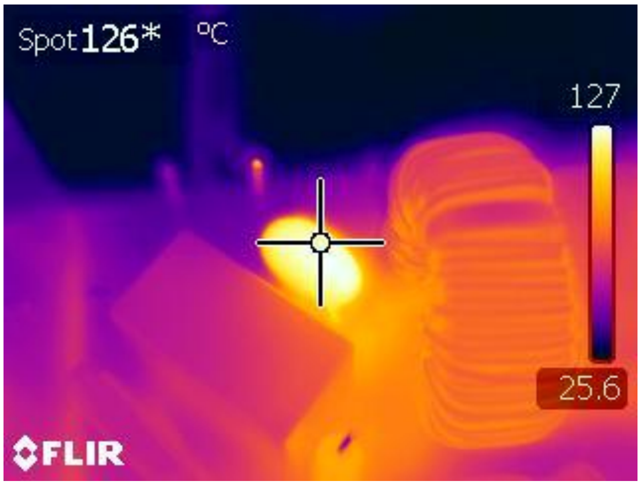

Figure 49 – Inrush Limiting Thermistor (RT1), 90 VAC Input, 100% Load, Room Temperature.

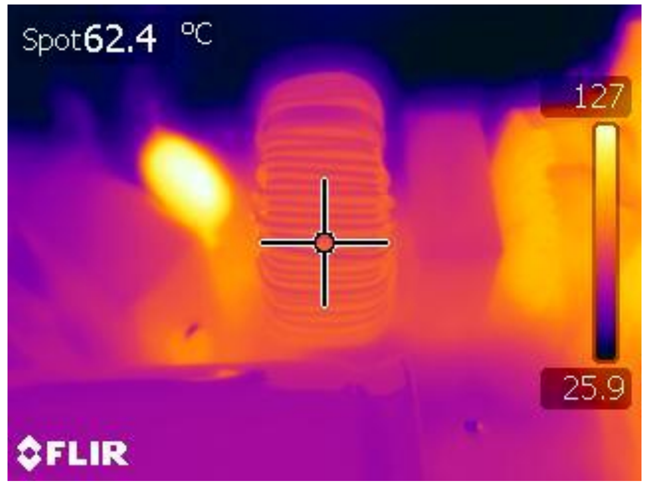

Figure 50 – Common Mode Choke (L1), 90 VAC Input, 100% Load, Room Temperature.

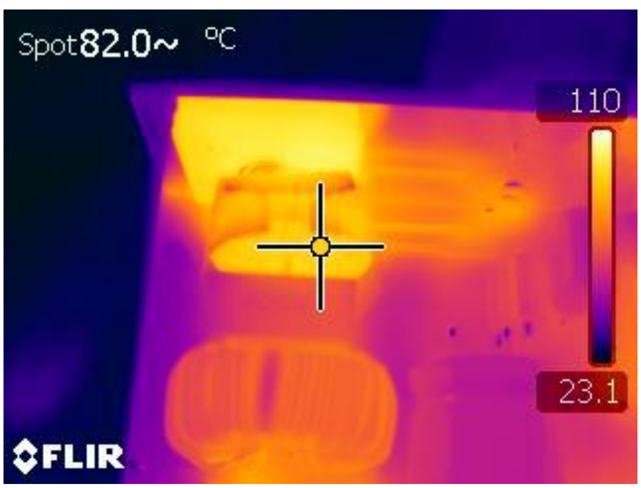

Figure 51 – Differential Mode Choke (L4), 90 VAC Input, 100% Load, Room Temperature.

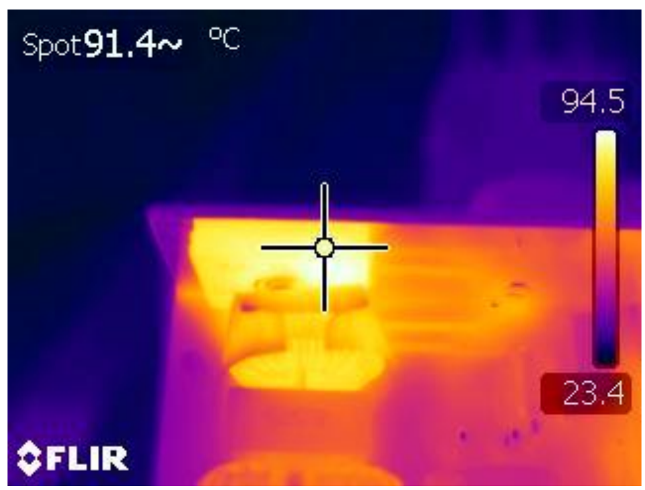

Figure 52 – Input Rectifier Bridge (BR1), 90 VAC Input, 100% Load, Room Temperature.

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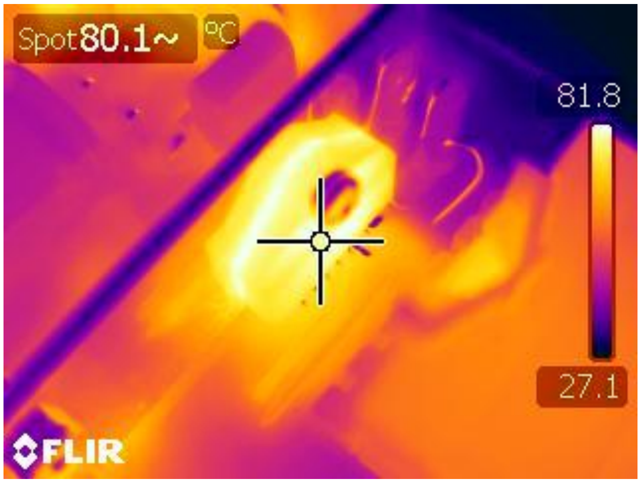

Figure 53 – PFC IC (U1), 90 VAC Input, 100% Load, Room Temperature.

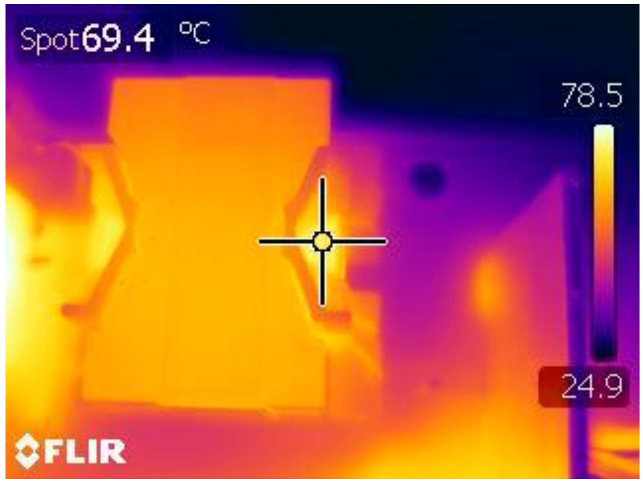

Figure 54 – PFC Inductor (L2), 90 VAC Input, 100% Load, Room Temperature.

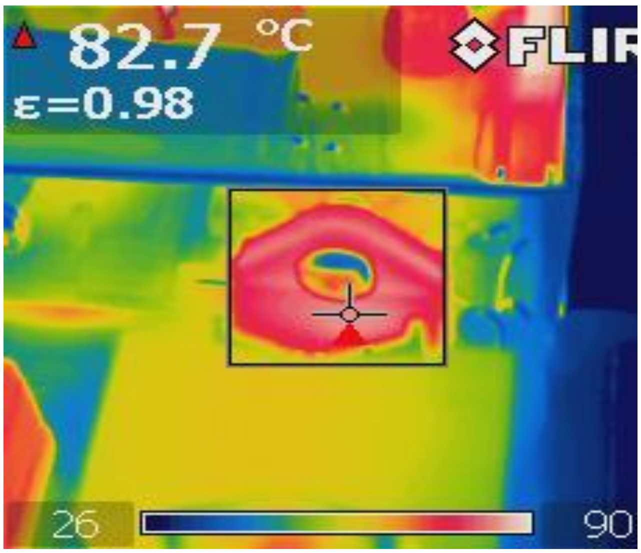

Figure 55 – LLC IC (U3), 90 VAC Input, 100% Load, Room Temperature.

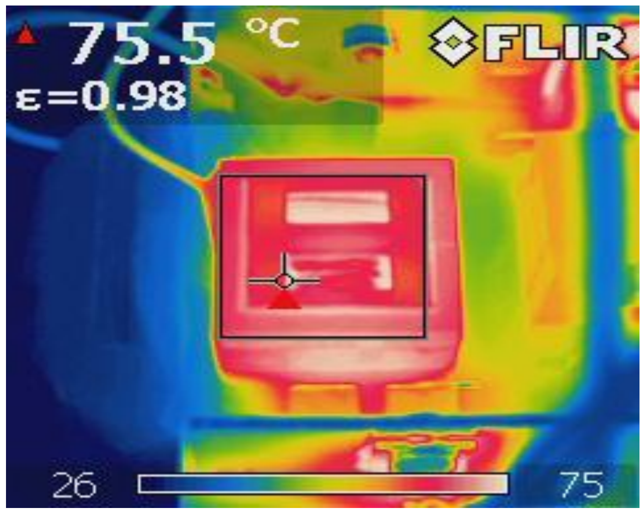

Figure 56 – LLC Transformer (T2), 90 VAC Input, 100% Load, Room Temperature.

Figure 57 – Output Rectifier (D11), 90 VAC Input, 100% Load, Room Temperature.

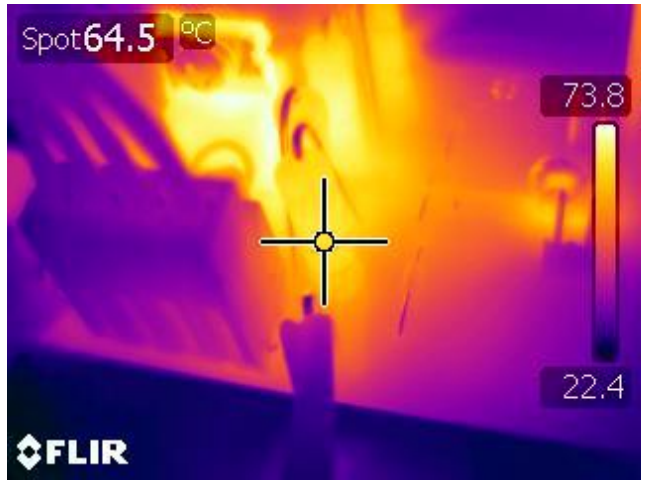

Figure 58 – Current Sense Resistor (R53), 90 VAC Input, 100% Load, Room Temperature.

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14.2 *115 VAC、60 Hz、150 W 出力、室温*

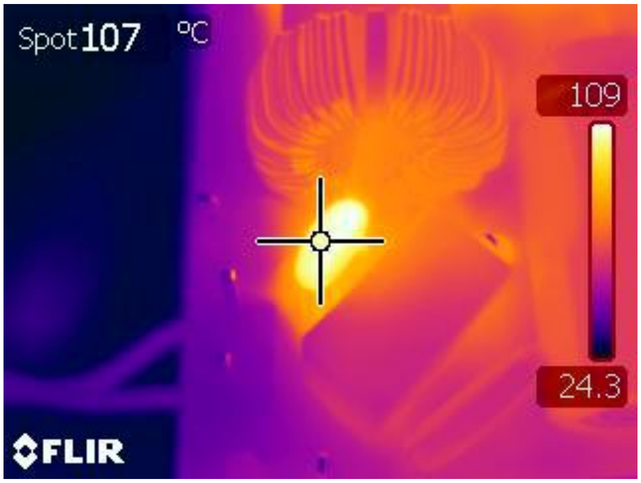

Figure 59 – Inrush Limiting Thermistor (RT1), 115 VAC Input, 100% Load, Room Temperature.

Figure 60 – Common Mode Choke (L1), 115 VAC Input, 100% Load, Room Temperature.

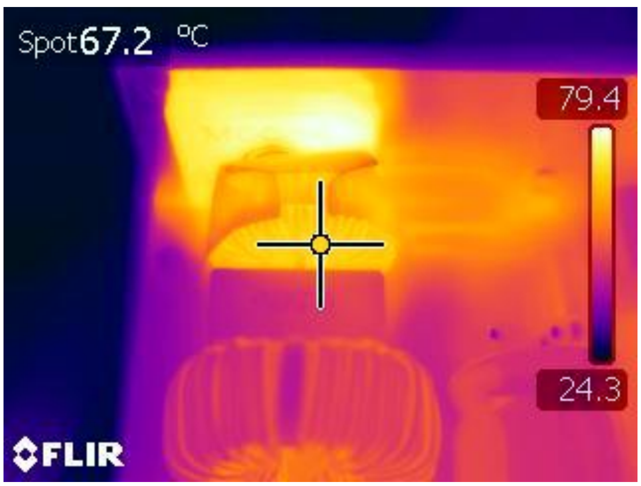

Figure 61 – Differential Mode Choke (L4), 115 VAC Input, 100% Load, Room Temperature.

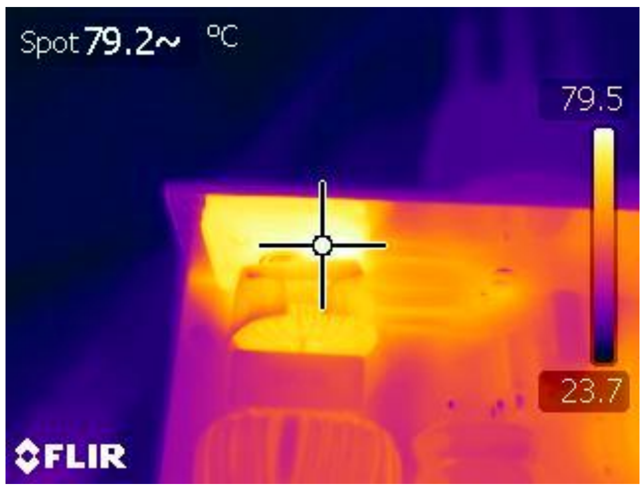

Figure 62 – Input Rectifier Bridge (BR1), 115 VAC Input, 100% Load, Room Temperature.

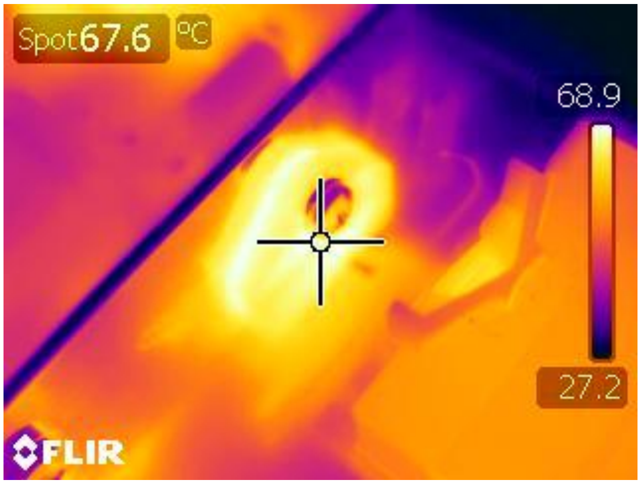

Figure 63 – PFC IC (U1), 115 VAC Input,
100% Load, Room Temperature.

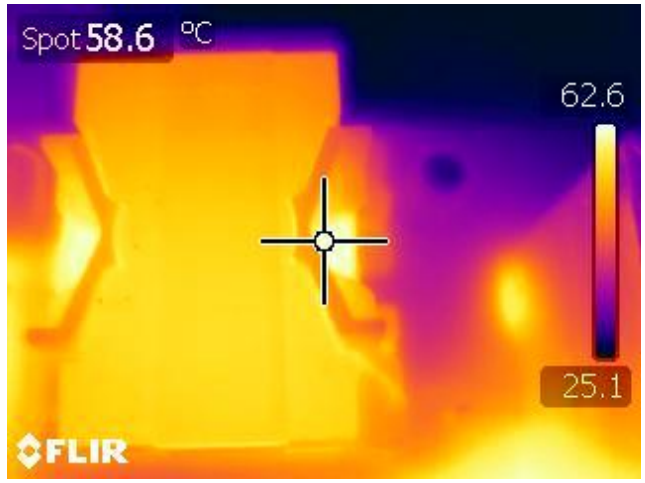

Figure 64 – PFC Inductor (L2), 115 VAC Input,
100% Load, Room Temperature

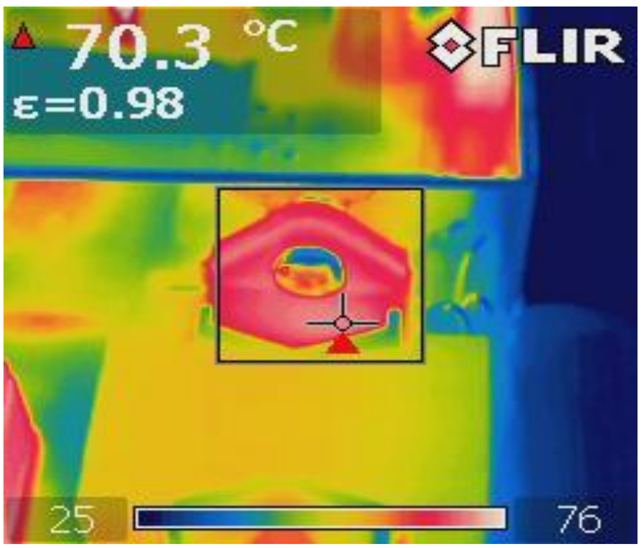

Figure 65 – LLC IC (U3), 115 VAC Input,
100% Load, Room Temperature.

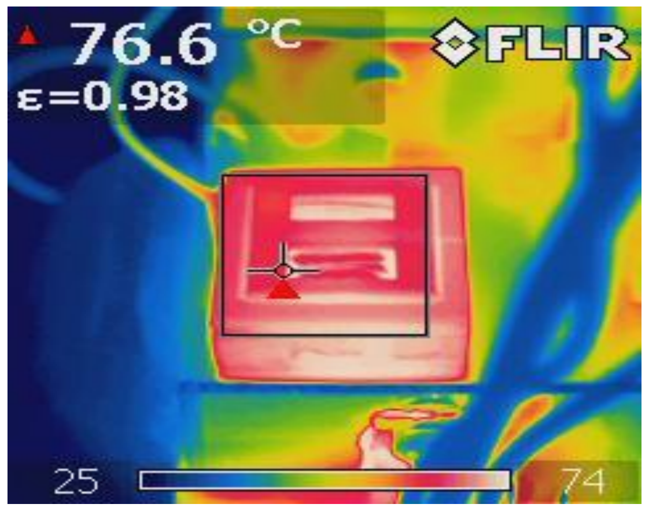

Figure 66 – LLC Transformer (T1), 115 VAC Input,
100% Load, Room Temperature**.**

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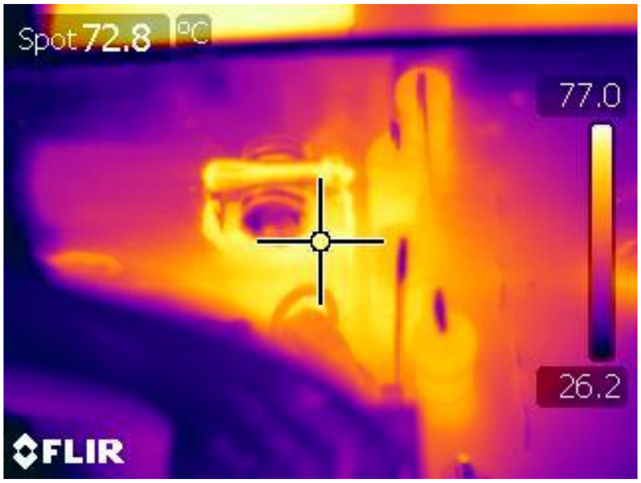

Figure 67 – Output Rectifier (D11), 115 VAC Input, 100% Load, Room Temperature.

Figure 68 – Current Sense Resistor (R53), 115 VAC Input, 100% Load, Room Temperature.

14.3 ***230 VAC、50 Hz、150 W 出力、室温***

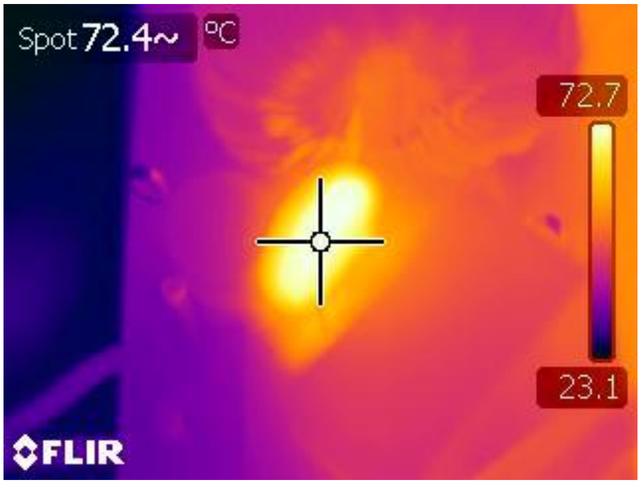

Figure 69 – Inrush Limiting Thermistor (RT1), 230 VAC Input, 100% Load, Room Temperature.

Figure 70 – Common Mode Choke (L1), 230 VAC Input, 100% Load, Room Temperature.

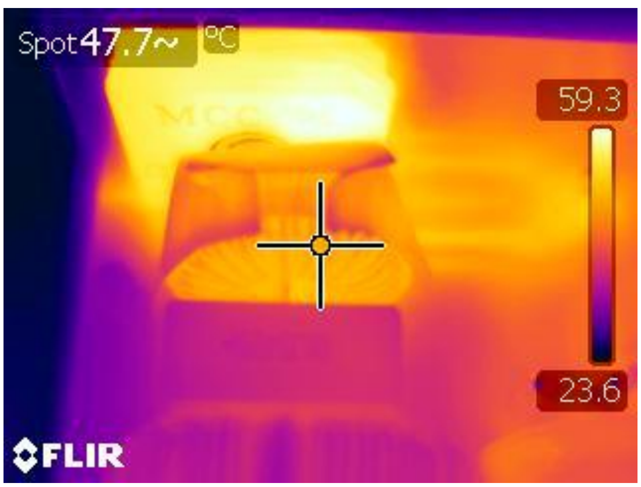

Figure 71 – Differential Mode Choke (L4), 230 VAC Input, 100% Load, Room Temperature.

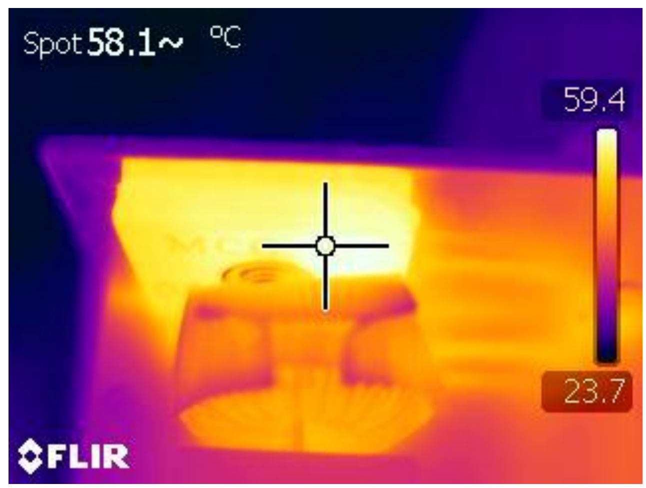

Figure 72 – Input Rectifier Bridge (BR1), 230 VAC Input, 100% Load, Room Temperature.

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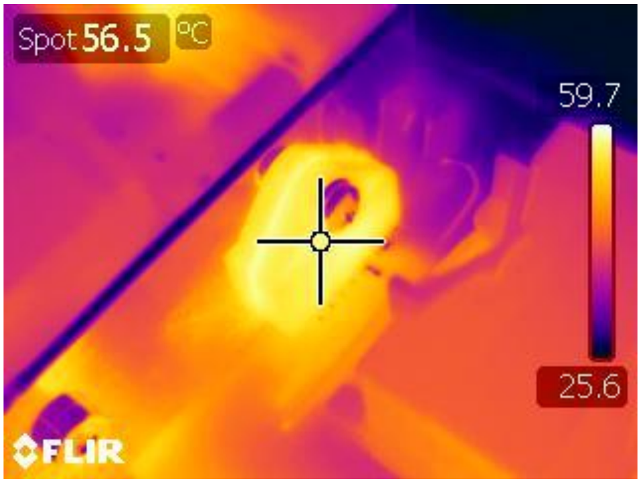

Figure 73 – PFC IC (U1), 230 VAC Input, 100% Load, Room Temperature.

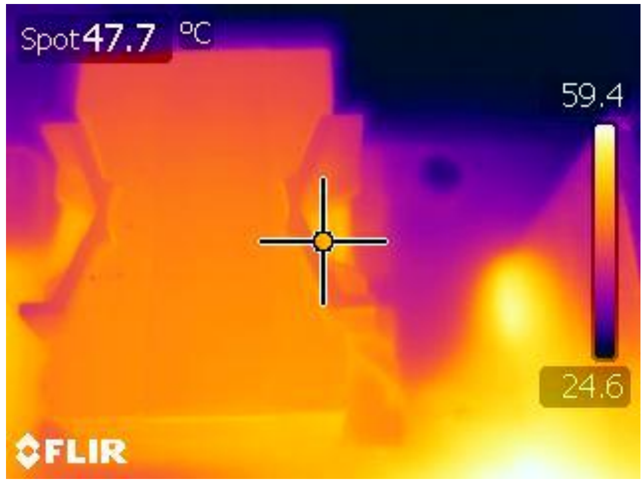

Figure 74 – PFC Inductor (L2), 230 VAC Input, 100% Load, Room Temperature

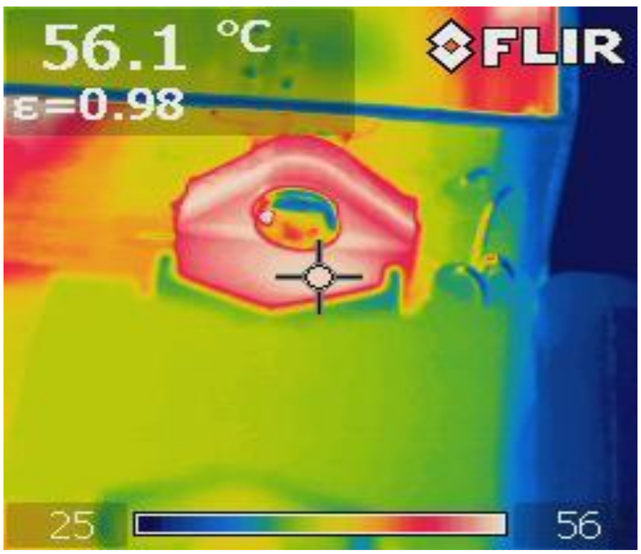

Figure 75 – LLC IC (U3), 230 VAC Input, 100% Load, Room Temperature.

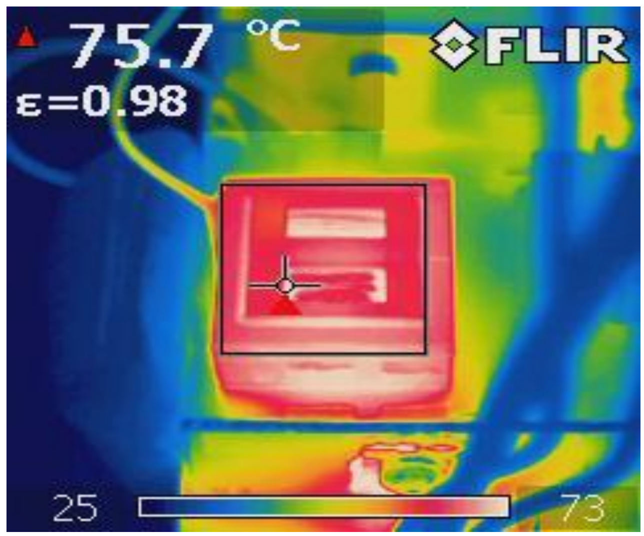

Figure 76 – LLC Transformer (T1), 230 VAC Input, 100% Load, Room Temperature**.**

Figure 77 – Output Rectifier (D11), 230 VAC Input, 100% Load, Room Temperature**.**

Figure 78 – Current Sense Resistor (R53), 230 VAC Input, 100% Load, Room Temperature**.**

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15 出力ゲイン位相

Gain-phase was tested a maximum load using the constant voltage load described in Section 7.1. It is important to use the actual LED load or a load with similar characteristics during gain-phase testing, as a load with different output characteristic will yield inaccurate results.

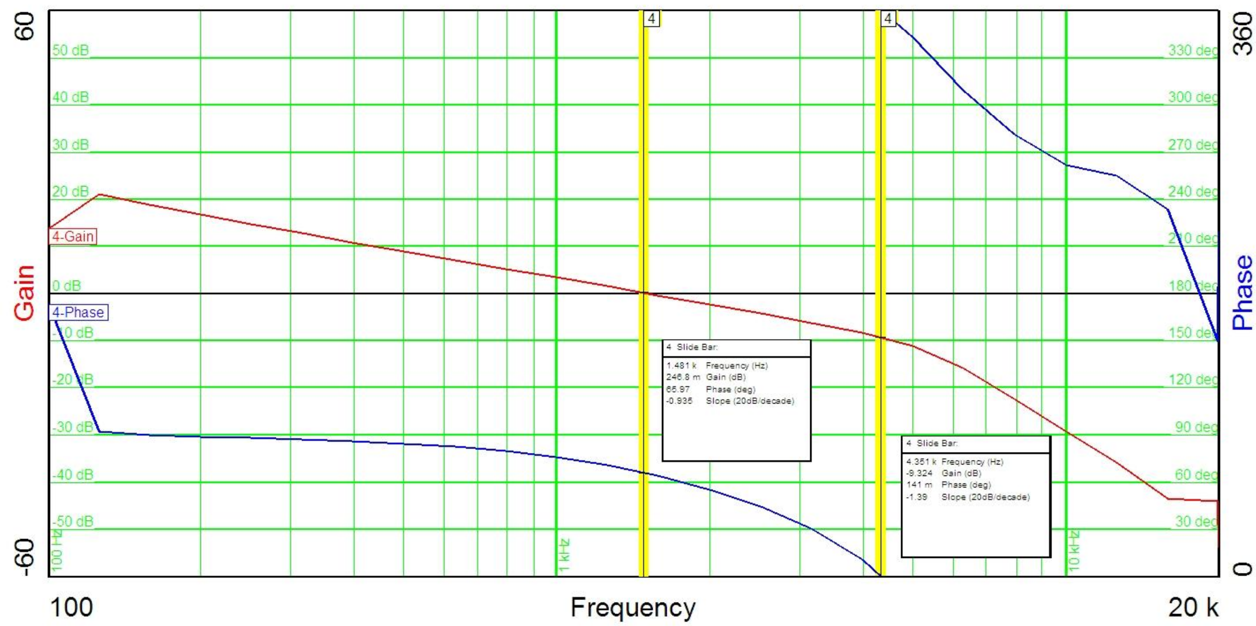

Figure 79 – LLC Converter Gain-Phase, 100% Load Crossover Frequency – 1.5 kHz, Phase Margin - 66°.

16 伝導 EMI

Conducted EMI tests were performed using the constant voltage load described in Section 7.1. The output return was connected to the LISN artificial hand to simulate the capacitance of a typical set of LED panels to chassis ground. The step change in readings at 80 MHz is due to an automatic 10 dB scale change of the EMI receiver rather than an actual peak at 80 MHz.

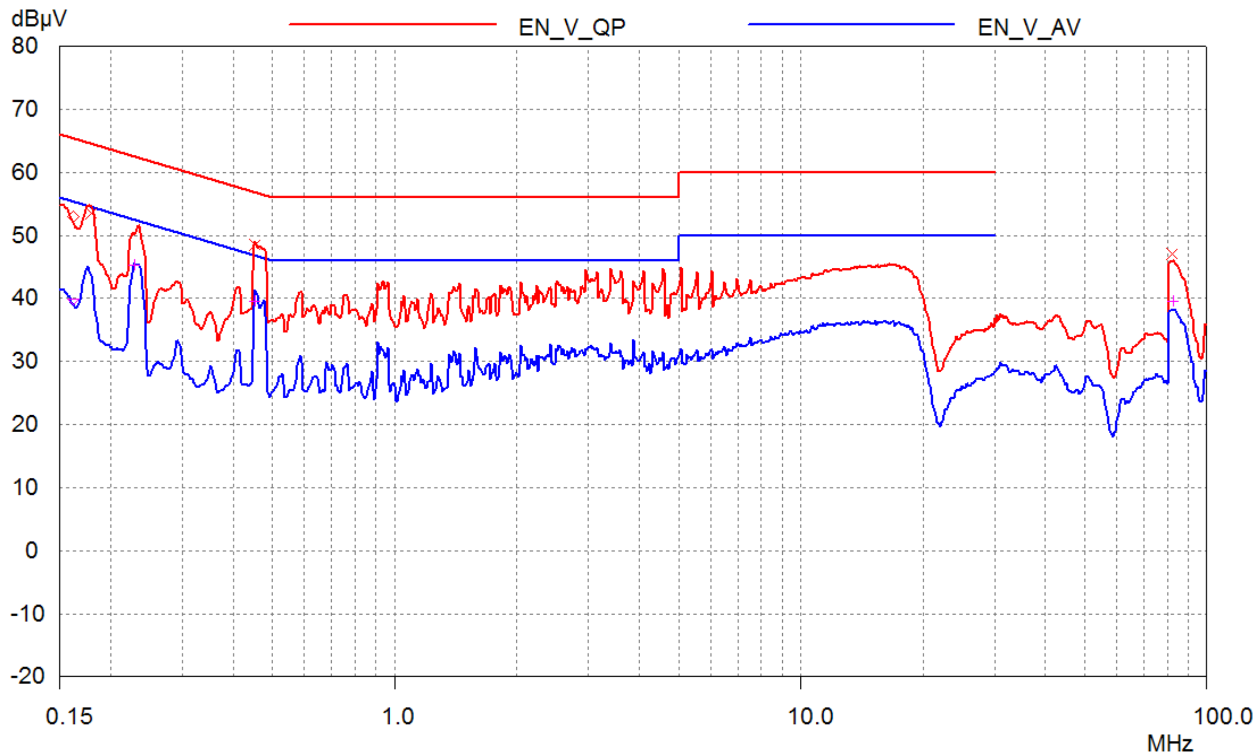

Figure 80 – Conducted EMI, 115 VAC, Full Load.

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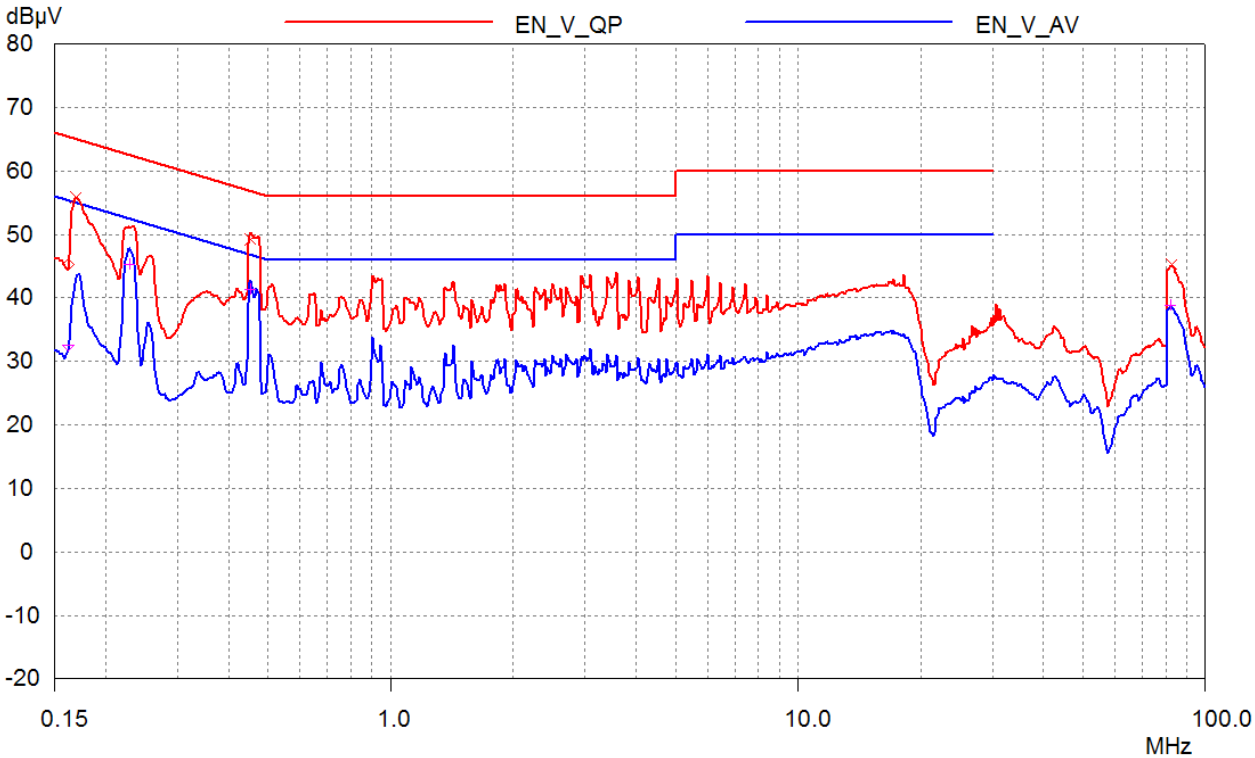

Figure 81 – Conducted EMI, 230 VAC, Full Load.

17 入力サージ試験

17.1 *入力サージ試験のセットアップ*

The picture below shows the power supply set-up for surge testing. The supply is placed on a ground plane approximately the size of the power supply. A piece of single-sided copper clad printed circuit material was used in this case, but a piece of aluminum sheet with appropriate insulation would also work. An IEC AC connector was wired to the power supply AC input, with the safety ground connected to the ground plane. The CV output load (described in section 7) was placed on top of the ground plane so that it would capacitively couple to the safety ground. A 48 V fan was located inside the plastic shroud shown in the figure, and used to cool the CV load during testing. An indicator consisting of a GaP yellow-green led in series with a 39 V Zener diode and a 100 ohm resistor was placed across the output of the supply and used as a sensitive output dropout detector during line surge testing.

The UUT was tested using a Teseq NSG 3060 surge tester. Results of common mode and differential mode surge testing are shown below. A test failure was defined as a non-recoverable output interruption requiring supply repair or recycling AC input voltage.

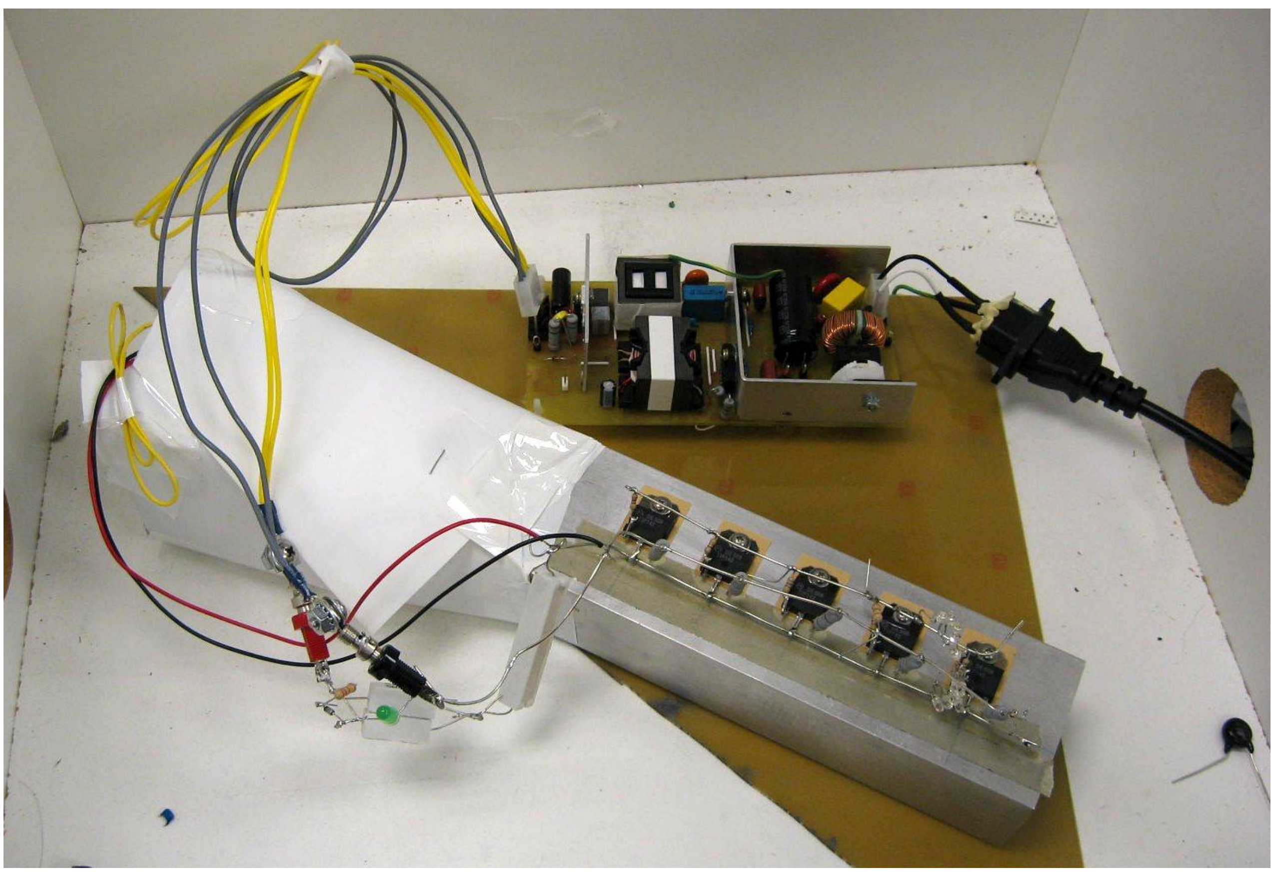

Figure 82 – Line Surge Physical Set-up.

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17.2 *ディファレンシャル モード サージ (1.2/50 μ秒)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+2	90	2	10	PASS
115	-2	90	2	10	PASS
115	+2	270	2	10	PASS
115	-2	270	2	10	PASS
115	+2	0	2	10	PASS
115	-2	0	2	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	90	2	10	PASS
230	-2	90	2	10	PASS
230	+2	270	2	10	PASS
230	-2	270	2	10	PASS
230	+2	0	2	10	PASS
230	-2	0	2	10	PASS

17.3 *コモン モード サージ (1.2/50 μ秒)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+4	90	12	10	PASS
115	-4	90	12	10	PASS
115	+4	270	12	10	PASS
115	-4	270	12	10	PASS
115	+4	0	12	10	PASS
115	-4	0	12	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4	90	12	10	PASS
230	-4	90	12	10	PASS
230	+4	270	12	10	PASS
230	-4	270	12	10	PASS
230	+4	0	12	10	PASS
230	-4	0	12	10	PASS

18 改訂履歴

Date	Author	Revision	Description and Changes	Reviewed
04-Mar-14	RH	6.1	Initial Release	Apps & Mktg
28-May-14	RH	6.2	Schematic Updated	

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