20 W Single Stage Flyback Power Supply With PFC for LED Ballasts

![Diagram of 20 W Single Stage Power Factor Corrected LED Driver Power Supply, Using a TOP247YN Device.](image)

**Application** | **Device** | **Power Output** | **Input Voltage** | **Output Voltage** | **Topology**
--- | --- | --- | --- | --- | ---
LED Ballast | TOP247YN | 20 W | 85 – 277 VAC | 12 V – 18 V, 1.67 A | PFC Flyback

**Design Highlights**
- Universal input range allows single design to be used worldwide
- Single stage PFC based CV/CC power supply
- Meets minimum PF requirement of 0.9 for commercial environment (ENERGY STAR SSL VER 1.0)
- Meets harmonic content limits as specified in IEC 61000-3-2 for Class C Equipment (see Figure 2)
- High efficiency (~80%) across entire input range
- Meets minimum PF requirement of 0.9 for commercial environment
- Single stage PFC based CV/CC power supply
- Universal input range allows single design to be used worldwide
- Meets EN55015 B conducted EMI limits with >10 dBμV margin
- High efficiency (~80%) across entire input range
- High power factor is achieved by designing the loop gain crossover to be well below 100 Hz, the lowest rectified AC frequency. For this design, gain crossover occurs at ~30 Hz at low line and ~40 Hz at high line.

For high power factor and low harmonic content, U1 must operate at constant duty cycle over an AC input line frequency cycle. This is achieved by designing the loop gain crossover to be well below 100 Hz, the lowest rectified AC frequency. For this design, gain crossover occurs at ~30 Hz at low line and ~40 Hz at high line.

Capacitor C10 and R6 set the dominant pole at approximately 0.02 Hz, with R7 creating a zero at 200 Hz to improve phase margin at gain crossover. To isolate C10 from the CONTROL pin, where it would change the startup and auto-restart timing, Q1 is configured as an emitter follower driven by the output of U2B. Looking into the emitter, C10 appears to be larger (C10 × Q1hfe), and R6 appears to be smaller (R6 / Q1hfe). This provides an equivalent capacitance value that is large enough to maintain a constant current into the CONTROL pin of U1 and therefore duty cycle over an AC line cycle.

The CONTROL pin bypass capacitor (C5) is just large enough to allow proper startup as well as steady state operation. A larger value of C5 would increase start-up delay time.

An optional soft-start circuit is formed by D12, C15, C16, R18 to allow proper start-up as well as steady state operation. A larger value of C5 would increase start-up delay time.

Resistors R11, R12, R23, Q2, Q3, Q4 and their associated circuitry, together with the LED in U2, form a low-drop CC sense circuit and program the average load current to 1.67 A. At no-load, the output voltage is limited to about 18 V by R16 and VR2.

For high power factor and low harmonic content, U1 must operate at constant duty cycle over an AC input line frequency cycle. This is achieved by designing the loop gain crossover to be well below 100 Hz, the lowest rectified AC frequency. For this design, gain crossover occurs at ~30 Hz at low line and ~40 Hz at high line.

Capacitor C10 and R6 set the dominant pole at approximately 0.02 Hz, with R7 creating a zero at 200 Hz to improve phase margin at gain crossover. To isolate C10 from the CONTROL pin, where it would change the startup and auto-restart timing, Q1 is configured as an emitter follower driven by the output of U2B. Looking into the emitter, C10 appears to be larger (C10 × Q1hfe), and R6 appears to be smaller (R6 / Q1hfe). This provides an equivalent capacitance value that is large enough to maintain a constant current into the CONTROL pin of U1 and therefore duty cycle over an AC line cycle.

The CONTROL pin bypass capacitor (C5) is just large enough to allow proper startup as well as steady state operation. A larger value of C5 would increase start-up delay time.

An optional soft-start circuit is formed by D12, C15, C16, R18 to R21 and Q5. Prior to the output reaching regulation, Q5 is biased...
on while C16 charges to $V_{BEQ} - V_{BEQ5}$. Current is fed into the 
CONTROL pin of U1 via U2, which ensures that the output 
reaches regulation without glitching (due to entering auto-restart). 
At power down, C16 is reset by discharging via R18.

The two secondary windings of the transformer are rectified by 
D10 and D11, filtered by C11 and C12.

The primary clamp circuit is formed by D7, R2, R3, C6 and VR1. 
During normal operation, R3 and C6 set the clamping voltage, 
with VR1 defining the maximum clamp voltage during start-up and 
load transients. Slow glass passivated diode D7 has a reverse 
recovery time of 2 µs and helps recover some of the leakage 
energy thereby improving efficiency. Resistor R2 damps out high 
frequency ringing and helps reduce EMI.

**Key Design Points**
- On application of AC input, the inductance in the line causes a 
voltage spike. Startup capacitor C4 stabilizes the DC bus voltage 
as it charges through diode D5. Once in steady state, the 
capacitor is effectively decoupled from the circuit by D5. Resistor 
R1 is the bleeder to discharge C4 during power down. This 
arrangement also provides protection against differential mode 
voltage surges.
- Use PIxls spreadsheet to design the transformer. Enter the peak 
power (33 W), which corresponds to the average power of 
20 W. Enter a minimum DC voltage equal to the peak of the 
minimum input AC voltage to determine the correct value of 
primary inductance.
- Set the value of KP to 1.0 to ensure critically discontinuous 
mode at the peak of minimum AC input voltage. Ensure that the 
converter operates in discontinuous mode (during steady state 
operation) at all times.
- Ensure that gain crossover occurs below 40 Hz. A higher 
bandwidth is undesirable as this degrades power factor by 
increasing the third harmonic content in the input current 
waveform.
- The size of the transformer should be based on thermal 
evaluation. Due to higher RMS currents in windings and core 
AC flux, a larger transformer is typically required than a standard 
DC fed flyback.
- Diode D6 must be an ultra-fast type. It prevents reverse 
currents from flowing through the TOPSwitch during its off time, 
the result of the small input capacitance.
- The secondary is split into 2 parallel windings and 2 separate 
diodes for improved efficiency.