

# DI-124 Design Idea

## LinkSwitch-TN™

### Ultrawide Input Range (57 – 580 VAC) Flyback Power Supply

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Metering / Industrial	LNK304PN	3 W	57 – 580 VAC	12 V, 250 mA	StackFET Flyback

#### Design Highlights

- StackFET™ flyback topology delivers full load over extremely wide input voltage range
- E-Shield™ transformer construction for reduced common-mode EMI (>10 dBμV margin)
- 66 kHz switching frequency with jitter reduces conducted EMI
- Simple ON/OFF controller – no feedback compensation required
- Auto-restart function for automatic and self-resetting open-loop, overload and short-circuit protection
- Built-in hysteretic thermal shutdown at 135 °C

#### Operation

The AC input is rectified and filtered and the resultant DC applied to one end of the transformer primary winding. The 450 V input capacitors are stacked with parallel balancing resistors to meet the required voltage rating. Resistors R1 to R4 provide fusing in case of a catastrophic failure. Inductor L1, C1 and transformer E-Shield windings allow the design to meet EN55022 B conducted limits with good margin.

A 600 V MOSFET, Q1, and U1 are arranged in the StackFET configuration (cascode). The drain of U1 drives the source of Q1

while the drain of Q1 drives the transformer primary. The drain voltage of U1 is limited to 450 V by VR1-3. This extends the maximum peak composite drain voltage of U1 and Q1 to 1050 V. The resistor chain R6-R8 provides startup charge for the gate of Q1 and R9 dampens high-frequency ringing. Once the converter is operating, the gate is largely driven by the charge stored in the capacitance of VR1-3. Zener VR4 limits the gate to source voltage of Q1. Leakage inductance energy is clamped by VR5 and D9 with R10 added to reduce ringing and thereby, EMI.

The operation of U1 is unaffected by the StackFET configuration. When the internal MOSFET turns on, Q1 is also turned on, applying the input voltage across the transformer primary. Once the primary current reaches the internal current limit of U1, the MOSFET is turned off and the energy stored is delivered to the output. Regulation is maintained using ON/OFF control. Switching cycles are enabled/disabled based on current into the FEEDBACK pin of U1. This is ideal as it results in a lowering of the effective switching frequency with load, scaling switching losses and maximizing efficiency. The use of LinkSwitch-TN further improves efficiency due to its 66 kHz switching frequency.

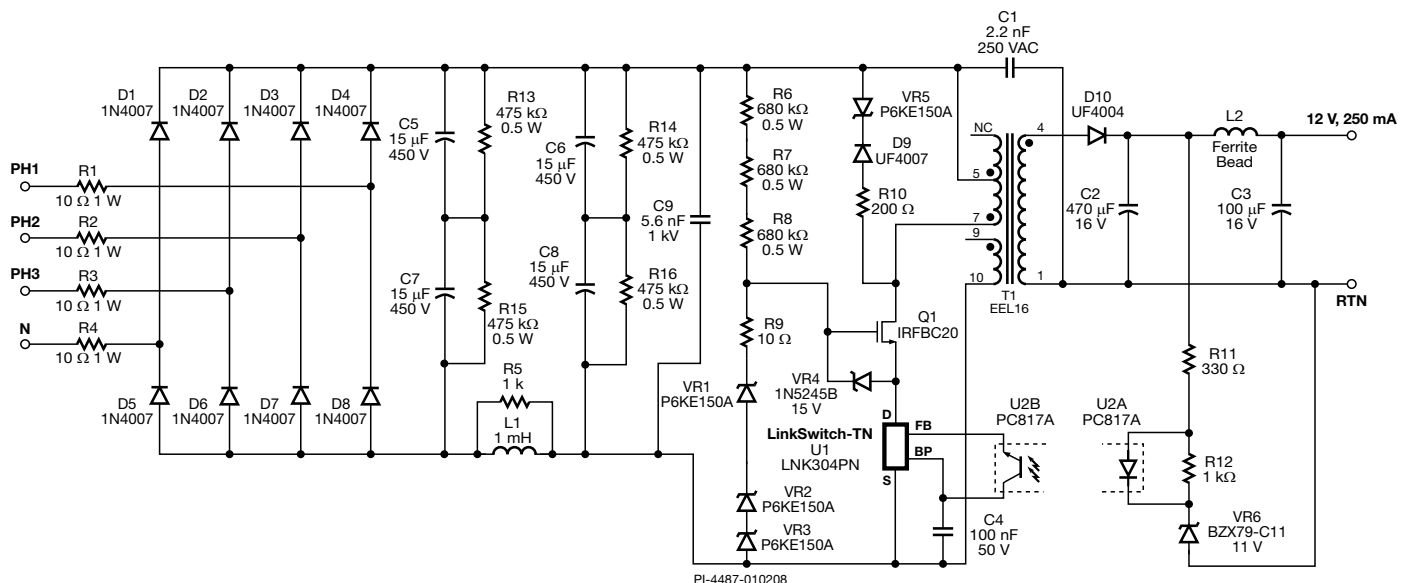


Figure 1. Schematic Diagram of 3 W Bias Supply Using LinkSwitch-TN in StackFET Configuration.

## Key Design Points

- The input stage (to the left of C9) can be omitted in applications that have a high-voltage DC bus. Capacitor C9 is still required to provide local decoupling.
- Long cores (EEL) are ideal for this application to provide greater bobbin width to accommodate the increased margins required to meet safety spacings at the high operating voltage.
- Zener diodes VR1-3 should have a combined voltage rating of less than 80% of the  $BV_{DSS}$  of the LinkSwitch-TN IC (<560 V). A single high-voltage Zener may also be used.
- The value of capacitors C5 to C8 can be reduced to 10  $\mu\text{F}$  if operation down to 57 VAC is not required (100 VAC minimum).
- Use 0.5 W resistors for R13-16 and R6-8 to provide adequate voltage rating.
- Efficiency falls at high line due to switching losses. Reducing transformer capacitance by adding layers of tape between the primary winding layers minimizes this.

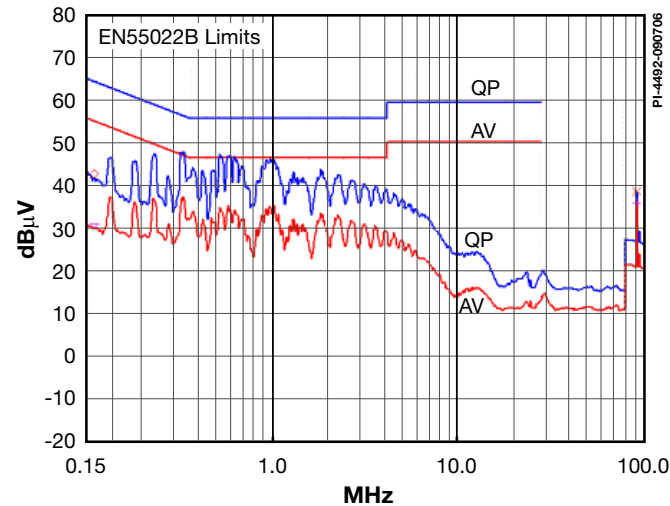


Figure 2. Conducted EMI (230 VAC, EN55022B Limits, AV and QP Results).

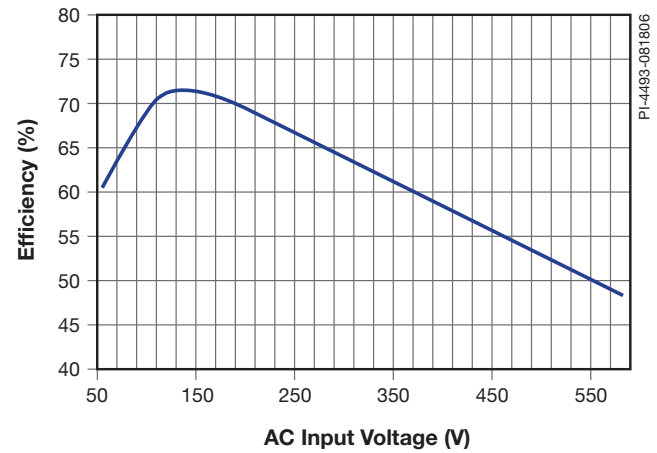


Figure 3. Full Load Efficiency vs. Input Voltage.

## Transformer Parameters

<b>Core Material</b>	EEL16, gapped for $A_{LG}$ of 70 $\text{nH}/\text{t}^2$
<b>Bobbin</b>	6+4 pin (Ying Chin YC-1604-1) with 3 mm + 3 mm tape margins
<b>Winding Details</b>	Shield: 23T, 2 $\times$ 36 AWG Primary: 184T, 36 AWG Shield: 12T, 2 $\times$ 36 AWG Secondary: 30T, 29 AWG
<b>Winding Order (pin numbers)</b>	Shield (5-NC), tape Primary (7-5), tape between layers Shield (9-10), tape, 12 V / (4-1), tape 12 V (8-6)
<b>Inductance</b>	Primary: 3.5 mH $\pm$ 10% Leakage: 160 $\mu\text{H}$ (maximum)
<b>Primary Resonant Frequency</b>	500 kHz (minimum)

Table 1. Transformer Parameters. (TIW = Triple Insulated Wire, NC = No Connection, FL = Flying Lead)

Power Integrations  
5245 Hellyer Avenue  
San Jose, CA 95138, USA.  
Main: +1 408-414-9200  
Customer Service  
Phone: +1-408-414-9665  
Fax: +1-408-414-9765  
Email: [usasales@powerint.com](mailto:usasales@powerint.com)

On the Web  
[www.powerint.com](http://www.powerint.com)

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS. The products and applications illustrated herein (transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.powerint.com](http://www.powerint.com). Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

The PI logo, TOPSwitch, TinySwitch, LinkSwitch, LYTSwitch, DPA-Switch, PeakSwitch, CAPZero, SENZero, LinkZero, HiperPFS, HiperTFS, HiperLCS, Qspeed, EcoSmart, Clampless, E-Shield, Filterfuse, StakFET, PI Expert and PI FACTS are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©2012, Power Integrations, Inc.