Design Example Report

Title	***10 W, 3-way Dimmable Non-Isolated Buck LED Driver Using LYTSwitch™-1 LYT1403D***
Specification	90 VAC – 132 VAC Input; 50 V_{TYP}, 205 mA_{TYP} Output
Application	LED Downlight
Author	Applications Engineering Department
Document Number	DER-607
Date	May 30, 2017
Revision	1.0

Summary and Features

- Single-stage power factor corrected, PF >0.9
- Accurate constant current regulation, ±5%
- Highly energy efficient, 89% at 115 V
- Low cost and low component count for compact PCB solution
- 3-way dimming capable (Variable resistor, PWM, and 0-10Vdc)
- Integrated protection features
  - No-load output protection
  - Output short-circuit protection
  - Overcurrent protection
  - Thermal fold-back protection
  - Over temperature protection
  - No damage during line brown-out or brown-in conditions
- Meets IEC 2.5 kV ring wave, 1 kV differential surge
- Meets EN55015 conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 50 V, 205 mA LED downlight driver with 3-way dimming functionality. It works off the low line input voltage mains (90 VAC to 132 VAC) and makes use of LYTSwitch-1 to deliver constant current, high efficiency, low component count and low cost solution in a non-isolated buck topology.

LYTSwitch-1 is a family of devices which is ideal for single-stage, high PF, constant current LED bulbs and tubes. The family incorporates a high-voltage power MOSFET with a variable on-time CrM controller in a SO8 package. Extensive protection features with minimum external components provide industry leading power density and functionality. The devices can be used in high-side or low-side non-isolated buck topology.

High efficiency, accurate constant current regulation, 3-way dimming functionality and low component count were the target design goals.

This document is composed of the power supply specification, schematic, bill of materials (BOM), printed circuit layout, design spreadsheet, and performance data.

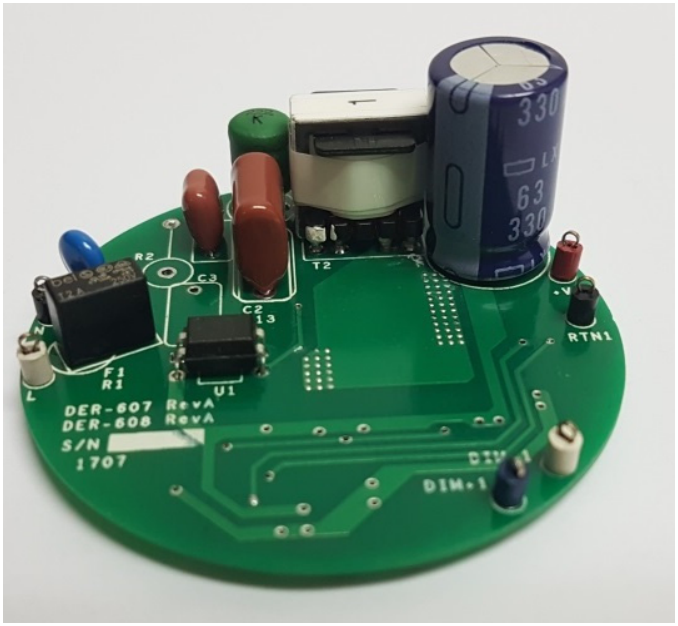

Figure 1 – Populated Circuit Board.

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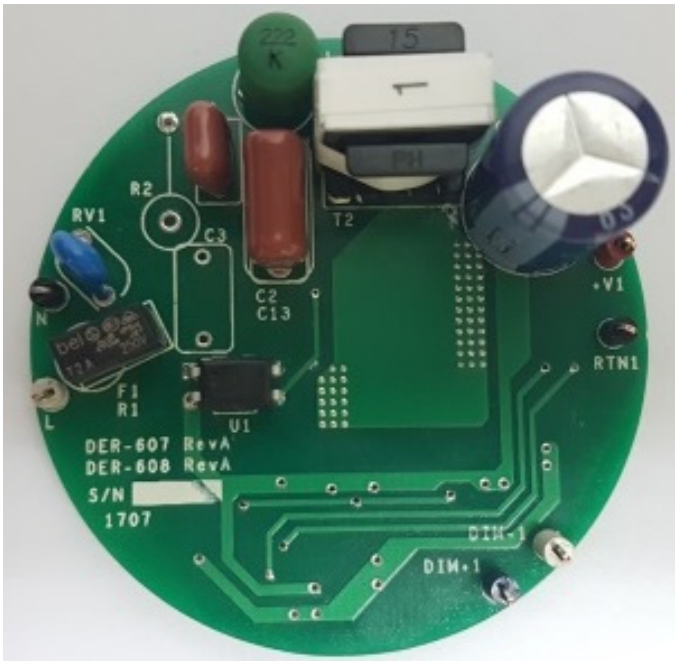

Figure 2 – Populated Circuit Board, Top View.

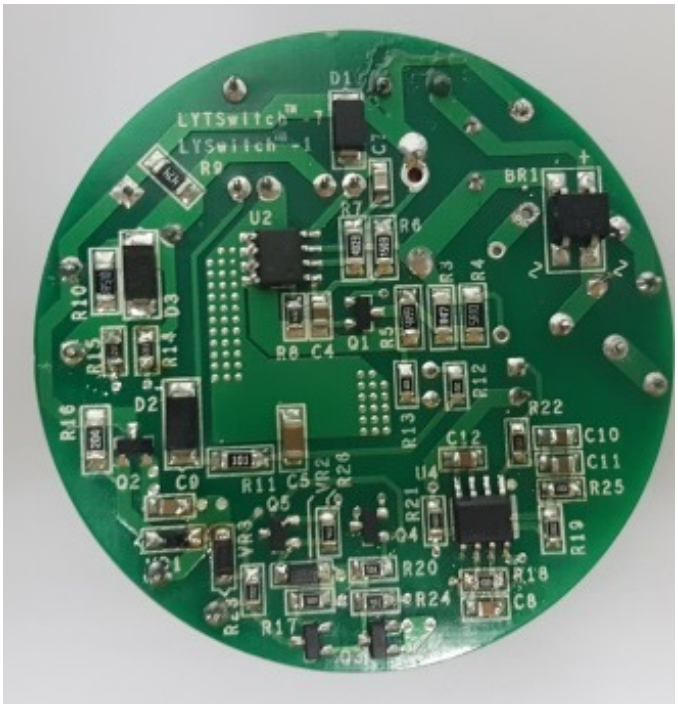

Figure 3 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		60		Hz	
Output						
Output Voltage	V_{OUT}		50		V	
Output Current	I_{OUT}		205		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		10		W	
Efficiency						
Full Load	η		89		%	115 V / 60 Hz at 25 ºC.
Environmental						
Conducted EMI			CISPR 15B / EN55015B			
Safety			Non-Isolated			
Ring Wave (100 kHz)			2.5		kV	
Differential Mode (L1-L2)			1.0		kV	
Power Factor			0.9			Measured at 115 VAC / 60 Hz.
Ambient Temperature	T_{AMB}			65	°C	Free Convection, Sea Level.

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3 **Schematic**

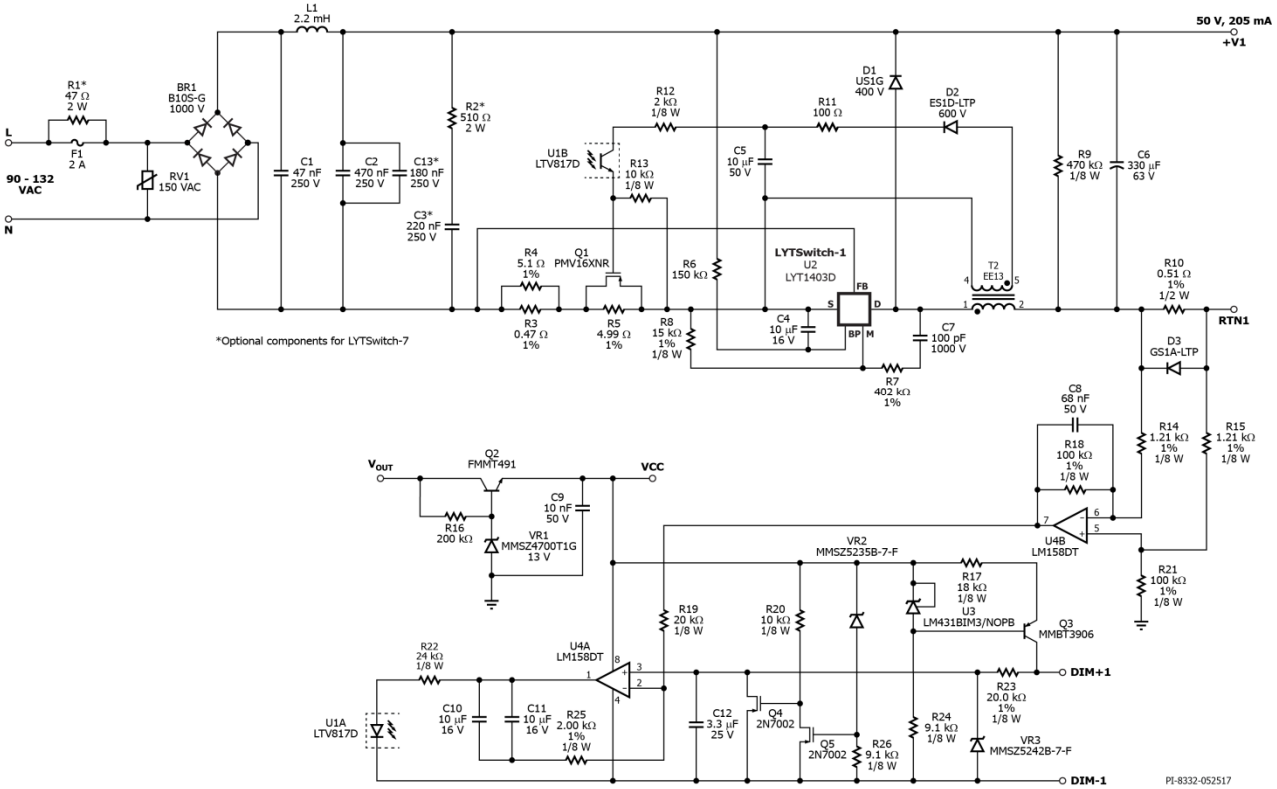

Figure 4 – Schematic.

* Denotes optional components

4 Circuit Description

The LYTSwitch-1 (LYT1403D) combines a high-voltage power MOSFET switch with a power supply CrM controller in a single SO8 package. The LYTSwitch-1 controller provides single-stage power factor correction, LED current control and high efficiency. A variable impedance circuit is incorporated into the design to facilitate 3-way dimming.

4.1 Input Stage

Input fuse F1 provides protection against component failure. Varistor RV1 is used to protect the LED driver against lightning surge. The varistor is chosen to limit the LYT1403D Dain voltage below 725 V. The AC input is rectified to a pulsating DC through the full wave bridge rectifier BR1.

4.2 EMI Filter

After the rectified input voltage an EMI π filter is cascaded. The circuit is composed of a differential choke inductor L1 and input filter capacitors C1 and C2. The EMI filter, together with the LYTSwitch-1 electronically quiet source pins and frequency jitter provide substantial EMI margin.

4.3 LYTSwitch-1 Control Circuit

The topology is a low side, non-isolated buck converter. During turn-on of the LYT1403D internal power MOSFET, current ramps up through the buck inductor (T2) to the output. The freewheeling diode (D1) is reverse biased during the LYTSwitch-1 on time. Once the LYTSwitch-1 turns off, the buck inductor reverses polarity. The freewheeling diode turns on and provides a path for the inductor current to ramp down to the output. Output capacitor (C6) provides filtering to limit the output current ripple. A 470 kΩ pre-load resistor is connected to the output to discharge the output capacitor when the LED is disconnected.

During start-up the bypass capacitor (C4) is charged to 5.25 V from an internal high-voltage current source internally fed from the DRAIN (D) pin of the LYTSwitch-1. The bypass capacitor provides power to the LYTSwitch-1 during the switch on-time. The IC internal regulator draws power from the high-voltage D pin and charges the bypass capacitor during the power switch off-time. A pull up resistor (R6) charges the bypass capacitor from the output rail to provide a stable BYPASS (BP) pin voltage. This results in lower device dissipation for improved efficiency and thermal performance.

LYTSwitch-1 forces a constant peak current to regulate the output current. The ratio between the constant peak current period and the buck dead zone is then maintained constant by the device to provide good output regulation. LYT1403DG has a ratio of 2 which was chosen for good output regulation.

The FEEDBACK (FB) pin directly senses the source or inductor current during the power MOSFET on-time using external current sense resistors R3 and R4. This feedback voltage

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is used by the LYTSwitch-1 IC to set the constant inductor peak current (I_{PK}) by comparing the sensed voltage to the reference current limit threshold ($V_{FBth} \geq 0.28V$, $I_{PK} = 0.28\ V / R_{SENSE}$). Output LED current is computed as $I_{LED} = I_{PK} / 3$ for LYT1403D device.

During the power MOSFET on-time, the MULTIFUNCTION (M) pin provides line OVP detection. The M pin is shorted internally to S pin to detect line OVP by sampling the voltage across the inductor (V_{IN}-V_{OUT}) and the current flowing out of the M pin. This current is defined by resistor R7 ($I_M = (V_{IN}-V_{OUT})/R7$). The M pin line OVP current threshold is $I_{MOVL} = 1\ mA_{\ TYP}$.

During the power MOSFET off-state, the M pin provides zero current detection and output OVP detection through sampling resistors R7 and R8. The ZCD is to guarantee critical conduction mode operation which means that the power MOSFET must be turned on immediately after the inductor has been demagnetized. The inductor demagnetization is sensed when the voltage across the inductor begins to collapse towards zero as flywheel diode D1 conduction expires. The OVP detection is achieved through R7 and R8 voltage divider network. The OVP threshold is set at 120% of steady state value (2.0 V). Resistor R8 is set to fixed value of 402 kΩ ±1% to minimize power loss during power MOSFET on-duration and ease of OVL detection for all output voltage designs.

Any output short-circuit at the output will be detected once the M pin voltage falls below the undervoltage threshold (VO_{UV}) of 1 V typical, the IC will inhibit switching and initiate auto-restart to limit the average input power to less than 1 W, preventing any component from overheating.

4.4 3-Way Dimming Control Circuit

The idea in the variable impedance dimming circuit is to vary the peak inductor current by varying the total sense resistance seen across FB and SOURCE (S) pins of U2 (LYTSwitch-1). This is done by varying the ohmic resistance across drain-to-source of Q1 depending on the set voltage, PWM duty cycle, or resistance across the dimming input terminals, DIM+ and DIM-. IC U4 is a dual op-amp in a single IC. The first op-amp, U4A, monitors the voltage from the dimming input and compares it with the voltage coming from the second op-amp, U4B, which serves as reference by providing output current information. U4B is configured as a differential amplifier which monitors the level of the output current I_{OUT}. The following considerations are made to simplify the voltage equation at pin 7 of U4B (V1):

If $\boldsymbol{R14 = R15} \quad \boldsymbol{and} \quad \boldsymbol{R18 = R21}$

Then $\boldsymbol{V_1 = (I_{OUT} * R10)\ \frac{R18}{R14}}$

The output of U4A drives the gate of Q1 to maintain the output current to a level that corresponds to a zero difference in voltage between its inverting (pin 2) and non-inverting (pin 3) terminals. For example, if the voltage at its non-inverting pin increases,

its output also increases to drive Q1 harder (decreasing the drain-to-source resistance), resulting to larger I_{OUT} and, thereby, increasing V1 to the level equal to the voltage at non-inverting pin of U4A. Since the voltage at the non-inverting pin of U4A is proportional to the voltage (or duty cycle, in case of PWM input) across DIM+ to DIM-, the output current could be controlled via these terminals. If no input is applied to DIM+ and DIM-, the capacitor C12 will charge to the level of V_{CC} which is also the voltage at the non-inverting (pin 3) of U4A. This will result to maximum output voltage at pin1 driving Q1 at its minimum $R_{DS(ON)}$. The minimum $R_{DS(ON)}$ of Q1 is chosen to be very small compared to the parallel combination of R3 and R4 such that at this condition, the maximum output current will be dictated by R3 and R4.

The supply voltage of the dimming circuit comes from a linear regulator consisting of Q2, R16, and VR1. Capacitor C9 serves as a bypass filter to the supply pin (pin 8) of U4. This bypass capacitor is especially helpful in filtering unwanted noise when the regulator and the ICs have to be quite far in the PCB layout and there are high dv/dt or di/dt traces (critical loops) nearby.

Components Q4, Q5, R20, R26, and VR2 form a one shot, blanking circuit to discharge whatever voltage there is at C12 during start-up and ensure it will start charging from around 0 V. This avoids non-monotonic, output current overshoot during start-up especially when there's already a voltage applied across DIM+ to DIM- before powering-up the unit.

Zener diode VR3 serves as protection in case the DIM+ terminal is accidentally connected to the output terminal by preventing excessive voltage at the non-inverting pin of U4A. It also protects against negative input to the non-inverting pin of U4A in case the DIM+ and DIM- are accidentally interchanged.

Resistor R19 is necessary to cancel the effect of input bias current. Thus, its value is set to be equal to R23. C10, C11 and R25 form the frequency compensation for U4A, adding a pole and a zero to the frequency response characteristics of the circuit.

4.4.1 0 VDC to 10 VDC Dimming

When a voltage is applied across DIM+ to DIM-, C12 will be charged up to this voltage level via R23. Essentially, the voltage at the dimming input terminals will also be the voltage at the non-inverting pin of U4A. U4A will respond to this input by increasing/decreasing its output, driving Q1 to adjust the output current to a level that will result to a voltage level at V1 equal to the dimming input voltage. The dimming input range is from 0 V to 10 V – applying 0 V will result to minimum output current while applying 10 V will result to maximum output current.

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4.4.2 Variable Duty PWM Input (10 V Peak)

When a PWM signal is applied across DIM+ to DIM-, the averaging filter composed of R23 and C12 will result to a voltage at the non-inverting (pin 3) terminal of U4A proportional to the PWM duty cycle. That is,

$$V_{+\ of\ U4A} = D * V_{peak}$$

Where:

V_{+} of U4A – voltage at the non-inverting pin of U5A
D – PWM duty cycle
V_{PEAK} – max. voltage of the PWM signal

The maximum voltage of the PWM input should be 10 V and the minimum frequency should be 300 Hz. The value of R23 and C123 are chosen such that the resulting time constant (RC product) is much larger than the period of the minimum PWM frequency to ensure effective filtering.

4.4.3 Variable Resistance (0 Ω – 100 kΩ)

A voltage divider bias PNP transistor circuit is used to convert the resistance dimming input into dimming voltage input. It uses a 2.5 V constant reference voltage from LM431 (U3) to accurately regulate the collector current.

$I_C = (2.5\text{-}V_{BE})/R_{17}$

The Q3 collector current (I_C) drives the dimming input resistor to come up with dimming input voltage from 0 V to 10 V which basically same dimming profile with 0 V to 10 V dimming.

$V_{DIM} = I_C \times R_{DIM} = 0$ V to 10 V

5 PCB Layout

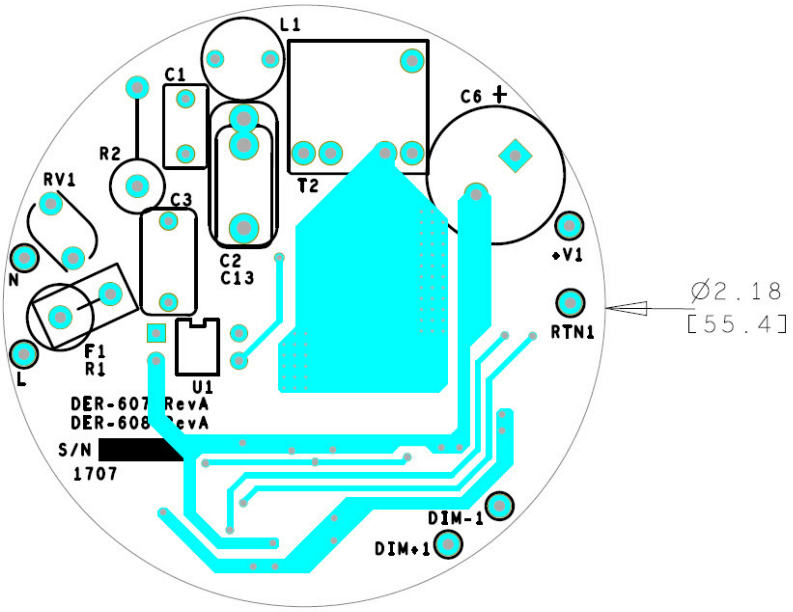

Figure 5 – Top Side.

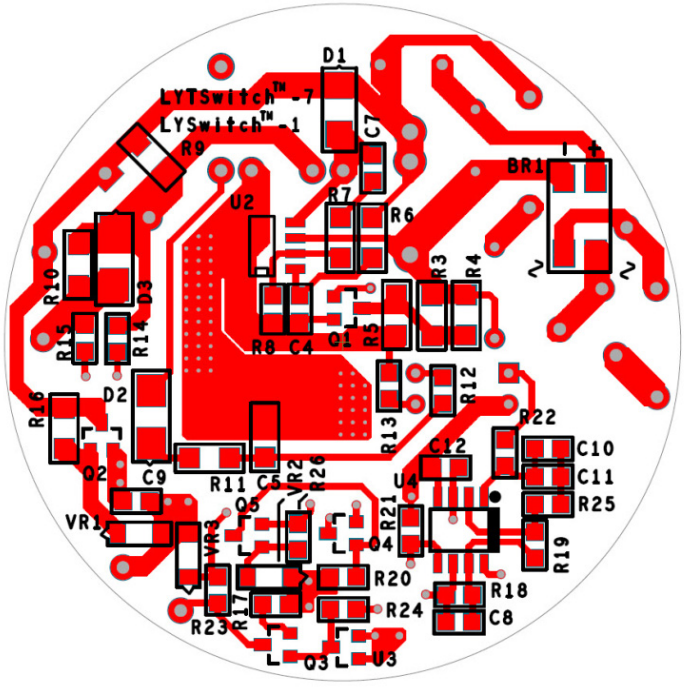

Figure 6 – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	+V1	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
2	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
3	1	C1	47 nF, 250 V, Film	ECQ-E2473KB	Panasonic
4	1	C2	470 nF, 250 V, Film	ECQ-E2474KB	Panasonic
5	3	C4 C10 C11	10 µF, ±10%, 16 V, X7R, Ceramic Capacitor, -55°C ~ 125°C, SMT, MLCC 0805 (2012 Metric), 0.079" L x 0.049" W (2.00 mm x 1.25 mm)	CL21B106KOQNNNE	Samsung
6	1	C5	10 µF, 10%, 50V, Ceramic, X7R, -55°C ~ 125°C, 1206 (3216 Metric), 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	CL31B106KBHNNNE	Samsung Electro-Mechanics America,
7	1	C6	330 µF, 63, Electrolytic, Low ESR, 85 mOhm, (12.5 x 20)	ELXZ630ELL331MK20S	Nippon Chemi-Con
8	1	C7	100 pF, 1000 V, Ceramic, NPO, 0805	C0805C101MDGACTU	Kemet
9	1	C8	68 nF, 50 V, Ceramic, X7R, 0805	C0805C683K5RACTU	Kemet
10	1	C9	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
11	1	C12	3.3 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
12	1	D1	DIODE ULTRA FAST, GPP, 400 V, 1 A SMA	US1G-13-F	Diodes, Inc.
13	1	D2	200 V, 1 A, Super Fast, 35 ns, DO-214AC, SMA	ES1D-LTP	Micro Commercial
14	1	D3	50 V, 1 A, DO-214AC	GS1A-LTP	Micro Commercial
15	1	DIM+1	Test Point, BLUE, Miniature THRU-HOLE MOUNT	5117	Keystone
16	2	DIM-1 N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
17	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
18	2	L RTN1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
19	1	L1	2.2 mH, 0.20 A, Ferrite Core	CTH7RF-222K	CT Parts
20	1	Q1	MOSFET, N-CH, 20 V, SOT23	PMV16XNR	NXP Semi
21	1	Q2	NPN,60 V 1000 mA, SOT-23	FMMT491TA	Zetex
22	1	Q3	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3906LT1G	On Semi
23	2	Q4 Q5	60 V, 115 mA, SOT23-3	2N7002-7-F	Diodes, Inc.
24	1	R3	RES, SMD, 0.47 Ω, 1%, 1/4W, 1206	ERJ-8RQFR47V	Panasonic
25	1	R4	RES, 5.1 Ω, 1%, 1/4 W, Thick Film, 1206	RC1206FR-075R1L	Yageo
26	1	R5	RES, 4.99 Ω, 1%, 1/4 W, Thick Film, 1206	RC1206FR-074R99L	Yageo
27	1	R6	RES, 150 k, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ154V	Panasonic
28	1	R7	RES, 402 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4023V	Panasonic
29	1	R8	RES, 15 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1502V	Panasonic
30	1	R9	RES, 470 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic
31	1	R10	RES, SMD,0.51 Ω±1% 0.5 W, ½ W SMT Resistor Thick Film ±250 ppm / °C 1206	ERJ-8BQFR51V	Panasonic
32	1	R11	RES, 100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ101V	Panasonic
33	1	R12	RES, 2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ202V	Panasonic
34	2	R13 R20	RES, 10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
35	2	R14 R15	RES, 1.21 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1211V	Panasonic
36	1	R16	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
37	1	R17	RES, 18 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ183V	Panasonic
38	2	R18 R21	RES, 100 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
39	1	R19	RES, 20 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
40	1	R22	RES, 24 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ243V	Panasonic
41	1	R23	RES, 20 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
42	2	R24 R26	RES, 9.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ912V	Panasonic
43	1	R25	RES, 2.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2001V	Panasonic
44	1	RV1	150 VAC, 7.5 J, 5 mm, RADIAL	S05K150E2	Epcos
45	1	T2	Bobbin, EE13, Vertical, 10 pins	P-1302-2	Pin Shine
46	1	U1	Optocoupler, 35 V, CTR 300-600%, 4-DIP	LTV-817D	Liteon
47	1	U2	LYTSwitch-1, Non-Dimmable, SO-8	LYT1403D	Power Integrations
48	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431BIM3/NOPB	National Semi

49	1	U4	IC, OpAmp, Dual, R2R, 8-SOIC	LM158DT	ST Micro
50	1	VR1	13 V, 5%, 500 Mw, SOD-123	MMSZ4700T1G	ON Semi
51	1	VR2	DIODE ZENER 6.8 V 500 MW SOD123	MMSZ5235B-7-F	Diodes, Inc.
52	1	VR3	DIODE ZENER 12 V 500 MW SOD123	MMSZ5242B-7-F	Diodes, Inc.

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7 Inductor Specification

7.1 Electrical Diagram

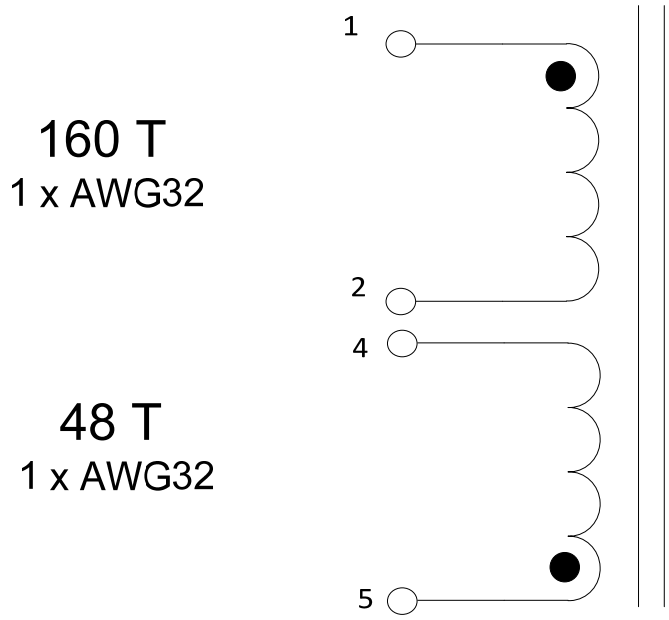

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 2.	1300 µH
Tolerance	Tolerance of primary inductance.	±5%

Item	Description
[1]	Core: EE13.
[2]	Bobbin: EE13, Vertical, 10 pins. P/N: 25-01023-00
[3]	Magnet Wire: #32 AWG.
[4]	Transformer Tape: 7.7 mm.
[5]	Transformer Tape: 5.5 mm.

7.3 Inductor Build Diagram

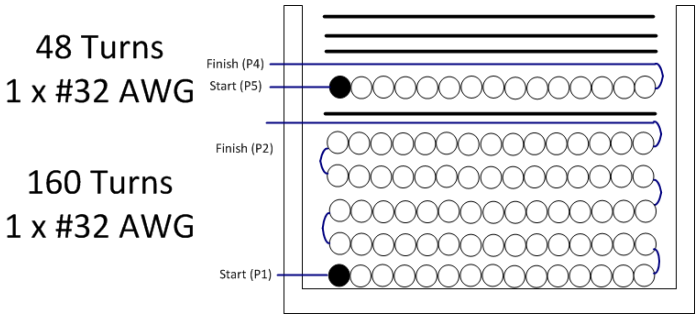

Figure 8 – Inductor Electrical Diagram

7.4 Inductor Construction

Winding Directions	Bobbin is oriented on winder jig such that terminal pin 1-5 is on the left side. The winding direction is counterclockwise.
Winding 1	Use wire item [3], start at pin 1 and wind 160 turns. On the last layer spread winding evenly across the bobbin width. Terminate the winding on pin 2.
Insulation	Add 1 layer of tape, Item [4], for insulation.
Winding 2	Use wire item [3], start at pin 5 and wind 48 turns. On the last layer spread winding evenly across the bobbin width. Terminate the winding on pin 4.
Insulation	Add 3 layers of tape, Item [4], for insulation.
Core Grinding	Grind the center leg of one core until it meets the nominal inductance of 1300 μH.
Assemble Core	Assemble the 2 core halves on the bobbin and wrap with 3 layers of tape, item (5).
Fix Core	Wrap item [4] tape around core and winding to prevent core from moving.
Pins	Pull out terminal pin no. 3, 7, 8, 9 and 10.
Finish	Dip the transformer assembly in varnish.

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8 Inductor Design Spreadsheet

ACDC_LYTSwitch1_ Buck_020317; Rev.1.1; Copyright Power Integrations 2017	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-1 Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			Low Line		AC line voltage range
VACMIN	90		90	V	Minimum AC line voltage
VACTYP	115		115	V	Typical AC line voltage
VACMAX	132		132	V	Maximum AC line voltage
FL	60		60	Hz	AC mains frequency
VO	50		50	V	Output Voltage
IO	205		205	mA	Average output current specification
EFFICIENCY			0.90		Efficiency estimate
PO			10.25	W	Continuous output power
VD			0.70	V	Output diode forward voltage drop
OPTIMIZATION PARAMETER	BOM		BOM		BOM selects IC with lowest peak current. THD selects IC for lowest THD.
ENTER LYTSWITCH-1 VARIABLES					
DEVICE BREAKDOWN VOLTAGE			725	V	This Spreadsheet supports 725V device only
DEVICE	LYT1x03D		LYT1403D		Actual LYTSwitch-1 device
ILIMITMIN			1.06	A	Minimum Current Limit
ILIMITTYP			1.15	A	Typical Current Limit
ILIMITMAX			1.24	A	Maximum Current Limit
TON			13	us	On-time during the fixed on-time region at VACTYP
FSW			43	kHz	Maximum switching frequency in the fixed current limit region at VACTYP
DMAX			0.92		Maximum duty cycle possible in the fixed on-time region
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
CORE	EE13		EE13		Enter Transformer Core
CUSTOM CORE NAME					If custom core is used - Enter part number here
AE			17.10	mm^2	Core effective cross cectional area
LE			30.20	mm	Core effective path length
AL			1130.00	nH/turn^2	Core ungapped effective inductance
AW			21.28	mm^2	Window Area of the bobbin
BW			7.40	mm	Bobbin physical winding width
LAYERS	6.0		6.0		Number of Layers
INDUCTOR DESIGN PARAMETERS					
LP_MIN			215	uH	Absolute minimum design inductance
LP_TYP	1300		1300	uH	Typical design inductance
LP_TOLERANCE	5		5	%	Tolerance of the design inductance
LP_MAX			1613	uH	Absolue maximum design inductance
TURNS			160	Turns	Number of inductor turns
ALG			50.78	nH/turn^2	Inductance per turns squared
BMAX			3682	Gauss	Actual saturation flux density in the fixed peak current region
BAC			1850	Gauss	AC flux density in the fixed peak current region
LG			0.404	mm	Core air gap
BWE			44.40	mm	Effective bobbin width
OD			0.28	mm	Outer diameter of the wire with insulation
INS			0.05	mm	Wire insulation
DIA			0.23	mm	Outer diameter of the wire without insulation
AWG			32		AWG of the bare wire.
CM			64	Cmils	Bare wire circular mils
CMA			229	Cmils/A	Bare wire circular mils per ampere
CURRENT DENSITY			4.6	A/mm^2	Bare wire current density
BOBBIN FILL FACTOR			57.91%		Area of the bobbin occupied by wire

CURRENT WAVEFORM SHAPE PARAMETERS					
IAVERAGE_INDUCTOR			0.20	A	Average inductor current at VACTYP obtained from half-line cycle emulation
IPEAK_MOSFET			0.62	A	MOSFET peak current at VACTYP when operating in the current limit region
IRMS_MOSFET			0.17	A	MOSFET RMS current at VACTYP obtained from half-line cycle emulation
IRMS_DIODE			0.22	A	Diode RMS current at VACTYP obtained from half-line cycle emulation
IRMS_INDUCTOR			0.28	A	Inductor RMS current at VACTYP obtained from half-line cycle emulation
LYTSWITCH EXTERNAL COMPONENTS					
FB Pin Resistor					
RFB_T			0.455	Ohms	Theoretical calculation of the feedback pin sense resistor
RFB			0.453	Ohms	Standard 1% value of the feedback pin sense resistor
M Pin Components					
BUCK_CONFIG	Low Side Buck				Buck Topology Switch Configuration
RUPPER			402.00	kOhms	Upper resistor on the M-pin divider network (E96 / 1%)
RLOWER			14.70	kOhms	Lower resistor on the M-pin divider network (E96 /1%)
VO_OVP		Info1	67.3	V	!!Info1. The VO_OVP is 1.35 * VO.
Line_OVP			452	V	Line overvoltage threshold
CC			100	pF	Coupling Capacitor for Low Side Buck Configuration
RPRELOAD			50	kOhms	Minimum Output Preload Resistor
CBP			4.7	uF	BP Capacitor
VOLTAGE STRESS PARAMETERS					
VDRAIN			187	V	Estimated worst case drain voltage
PIVD			187	V	Output Rectifier Maximum Peak Inverse Voltage

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9 Performance Data

All measurements were performed at room temperature using LED load. 1 minute soak time was applied before measurement with AC source turned-off for 5 seconds every succeeding input line measurement.

9.1 Efficiency

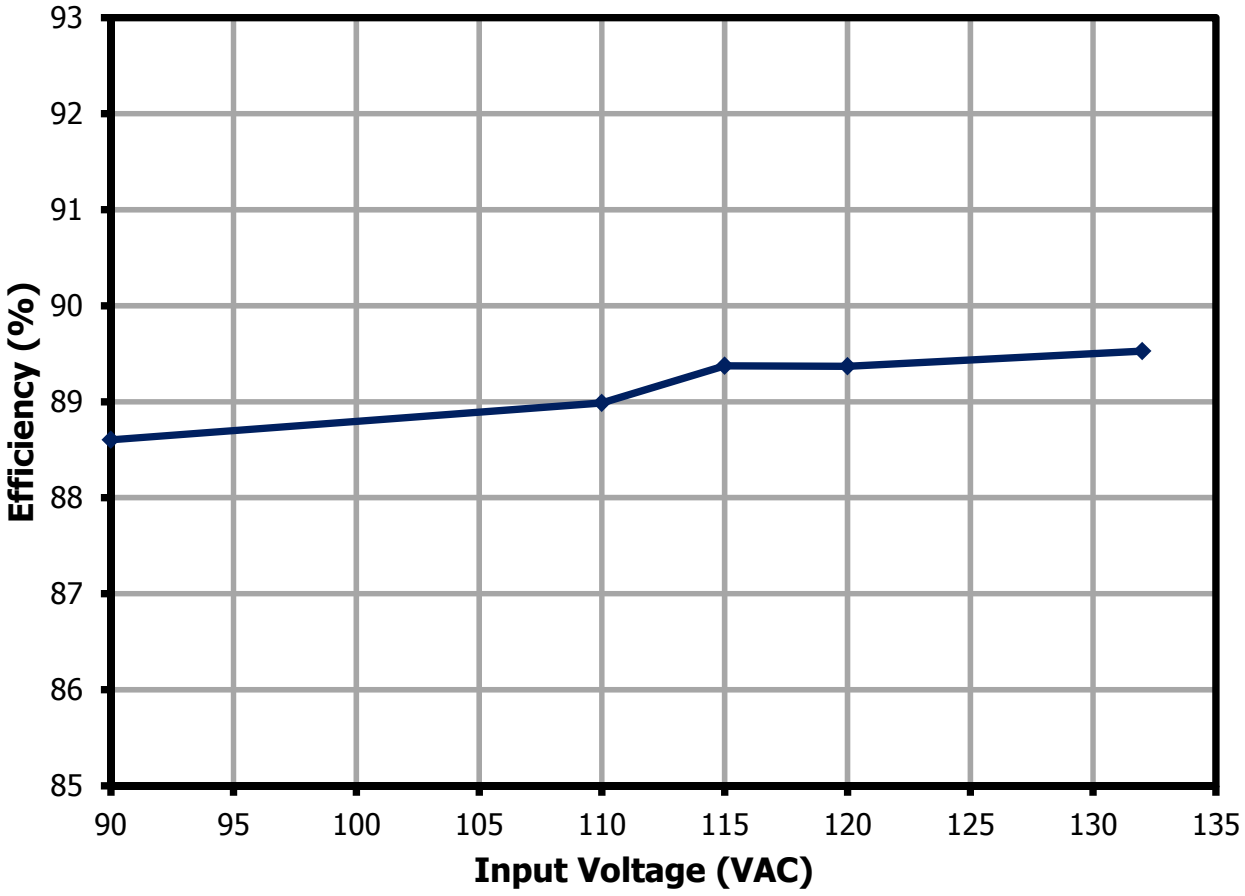

Figure 9 – Efficiency vs. Line.

9.2 Line Regulation

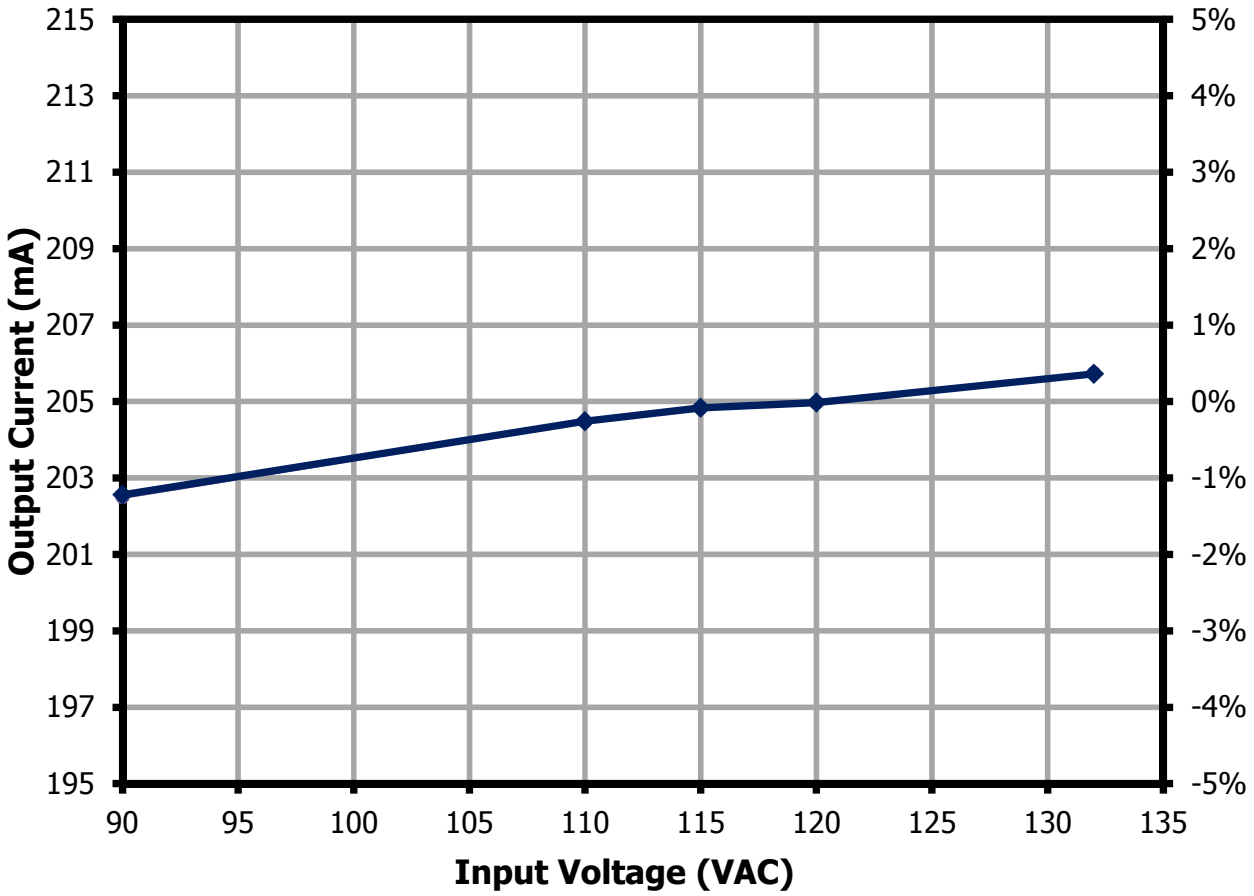

Figure 10 – Regulation vs. Line.

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9.3 Power Factor

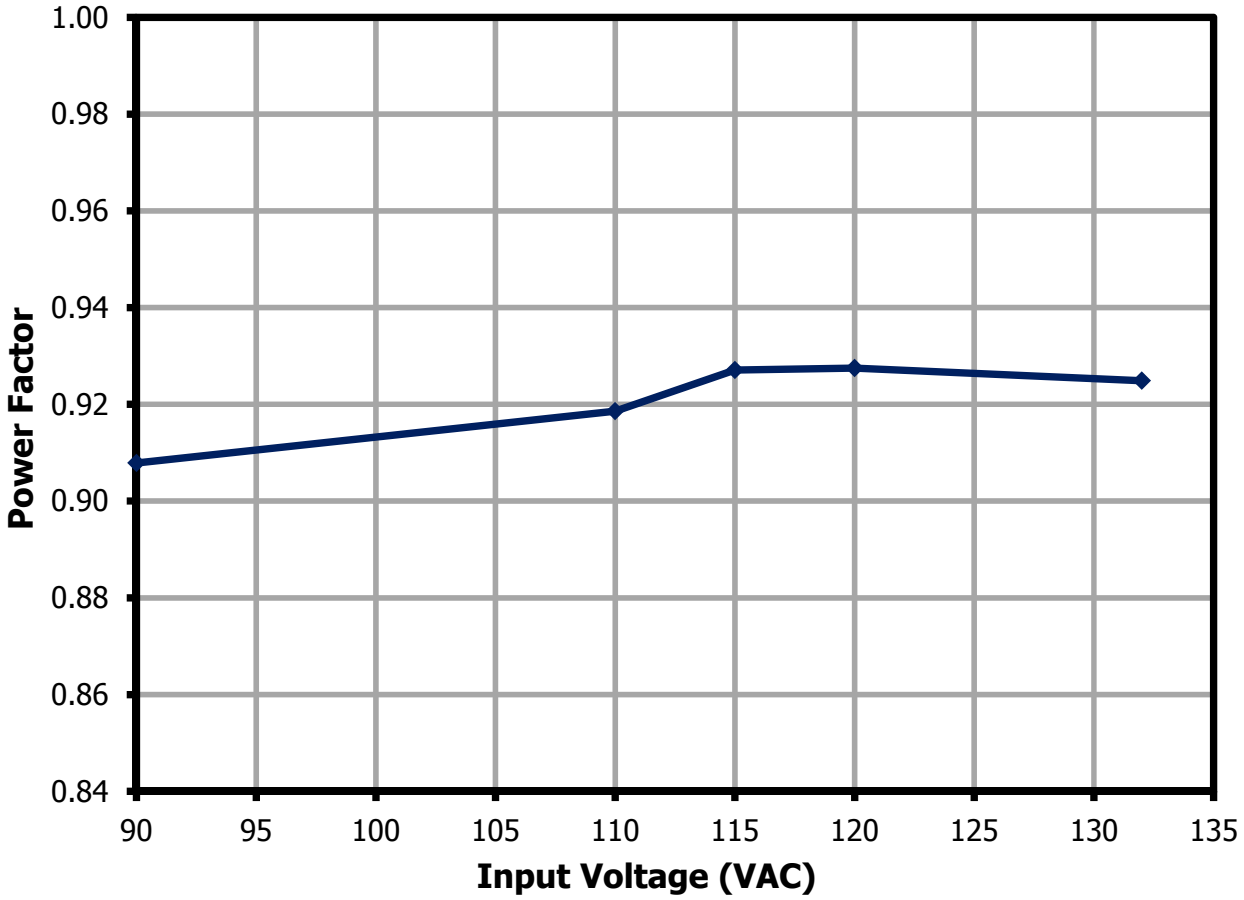

Figure 11 – Power Factor vs. Line.

9.4 %ATHD

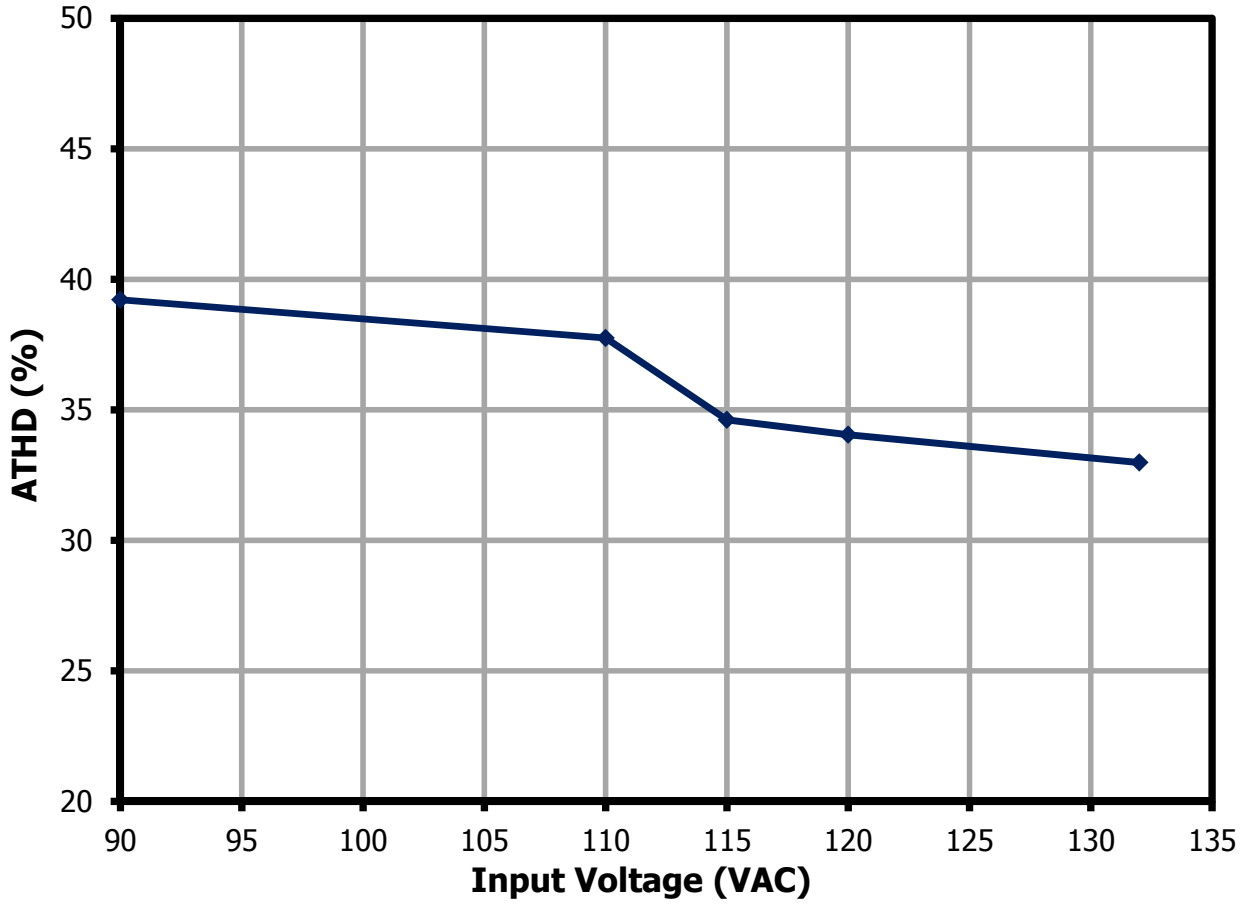

Figure 12 – %ATHD vs. Line.

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9.5 Individual Harmonics Content

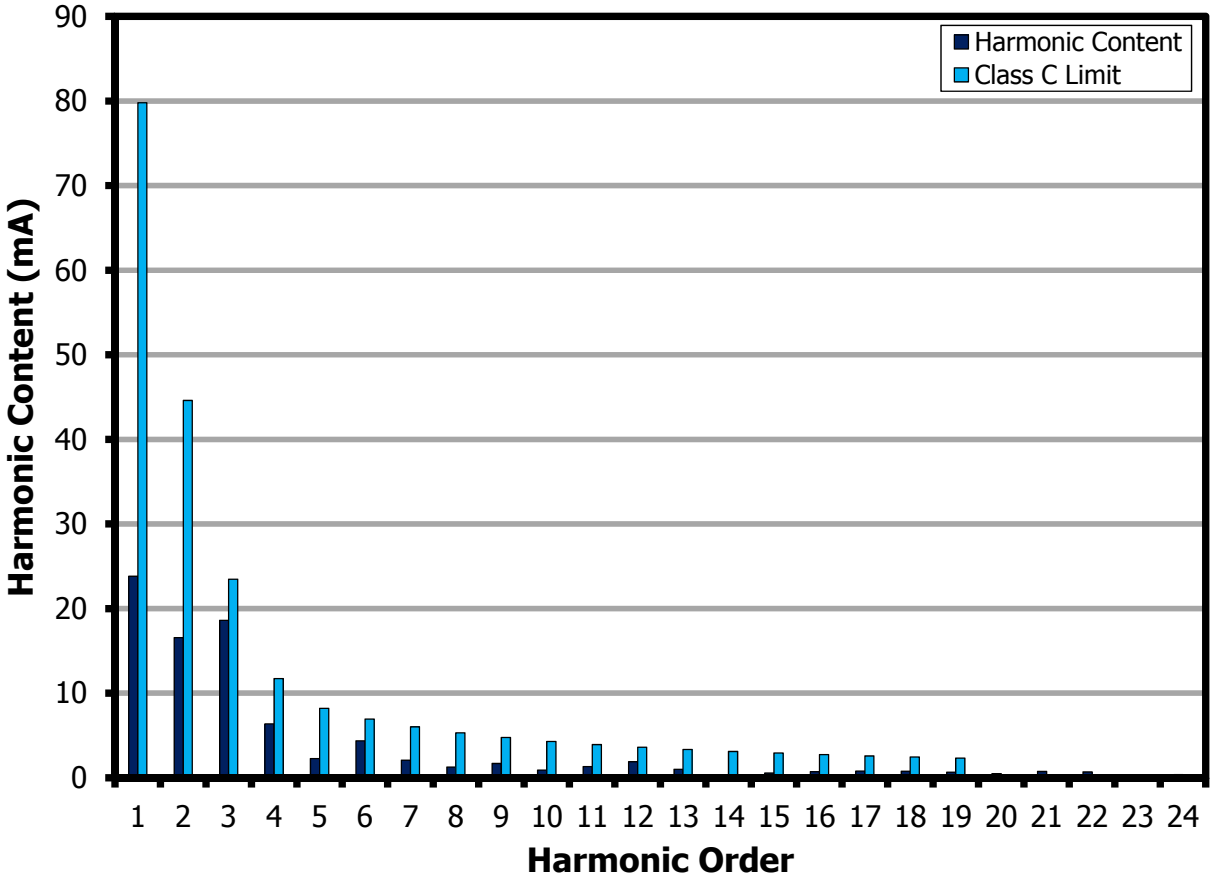

Figure 13 – 50 V LED Load Input Current Harmonics at 115 VAC, 60 Hz.

9.6 Dimming Performance

9.6.1 Variable Resistance

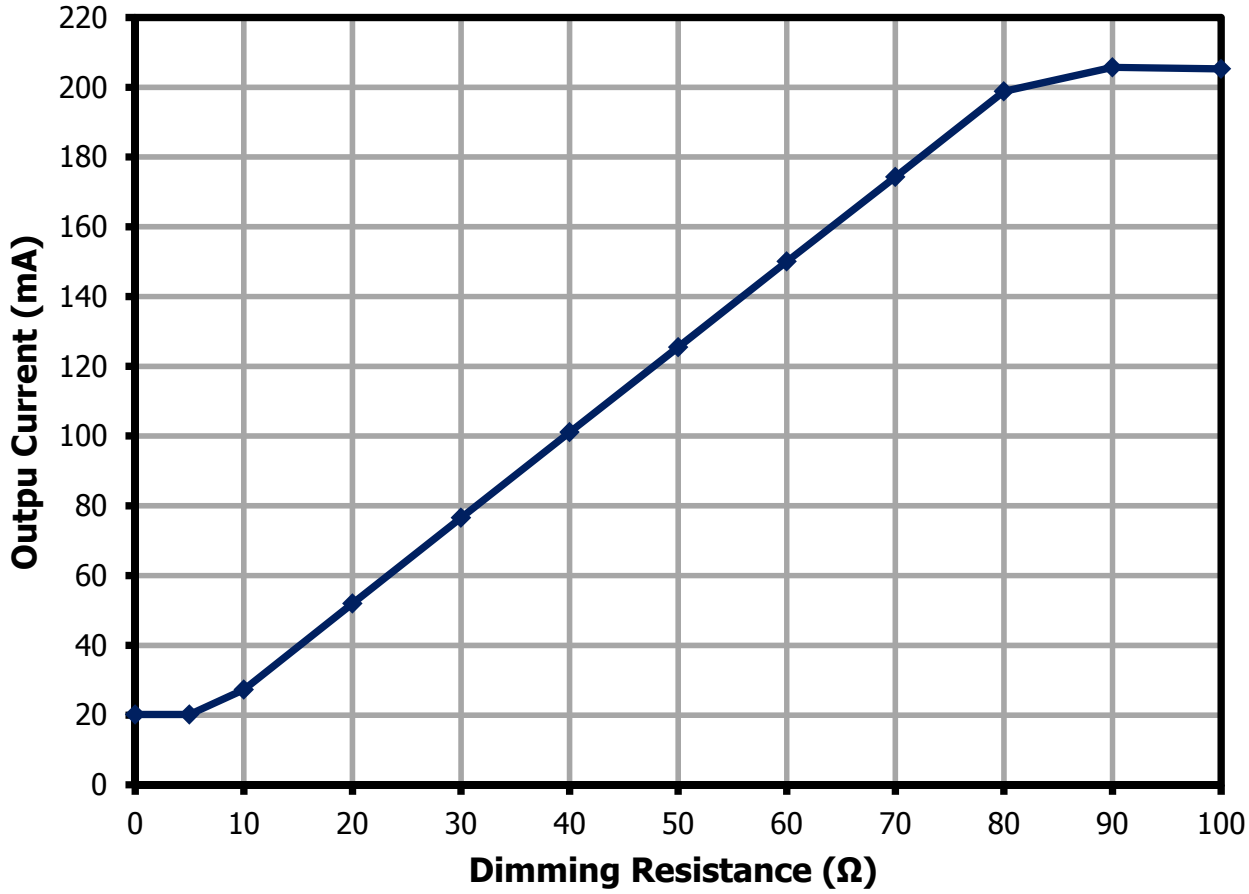

Figure 14 – Output Current vs. Dimming Resistance.

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9.6.2 PWM Dimming

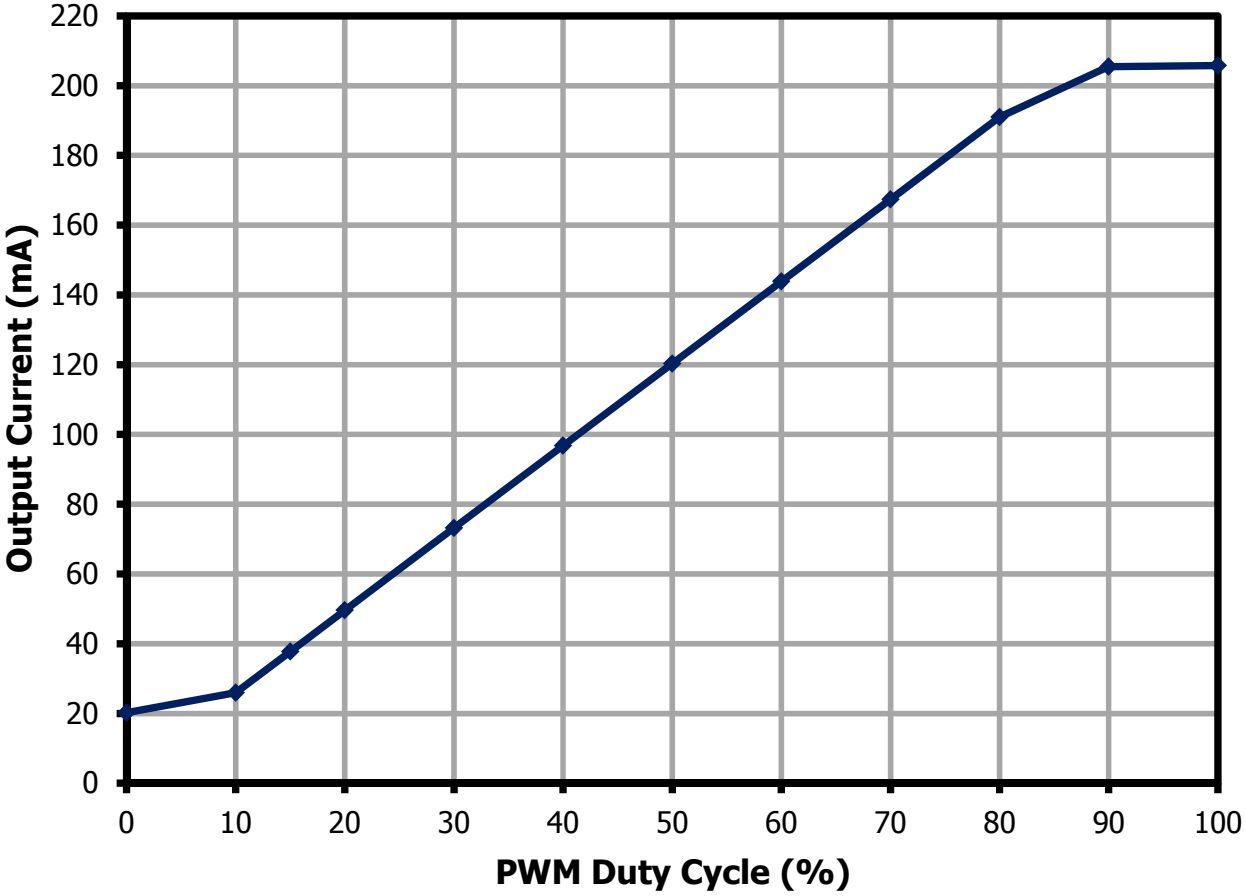

Figure 15 – Output Current vs. PWM Duty Cycle.

9.6.3 0 VDC to 10 VDC Dimming

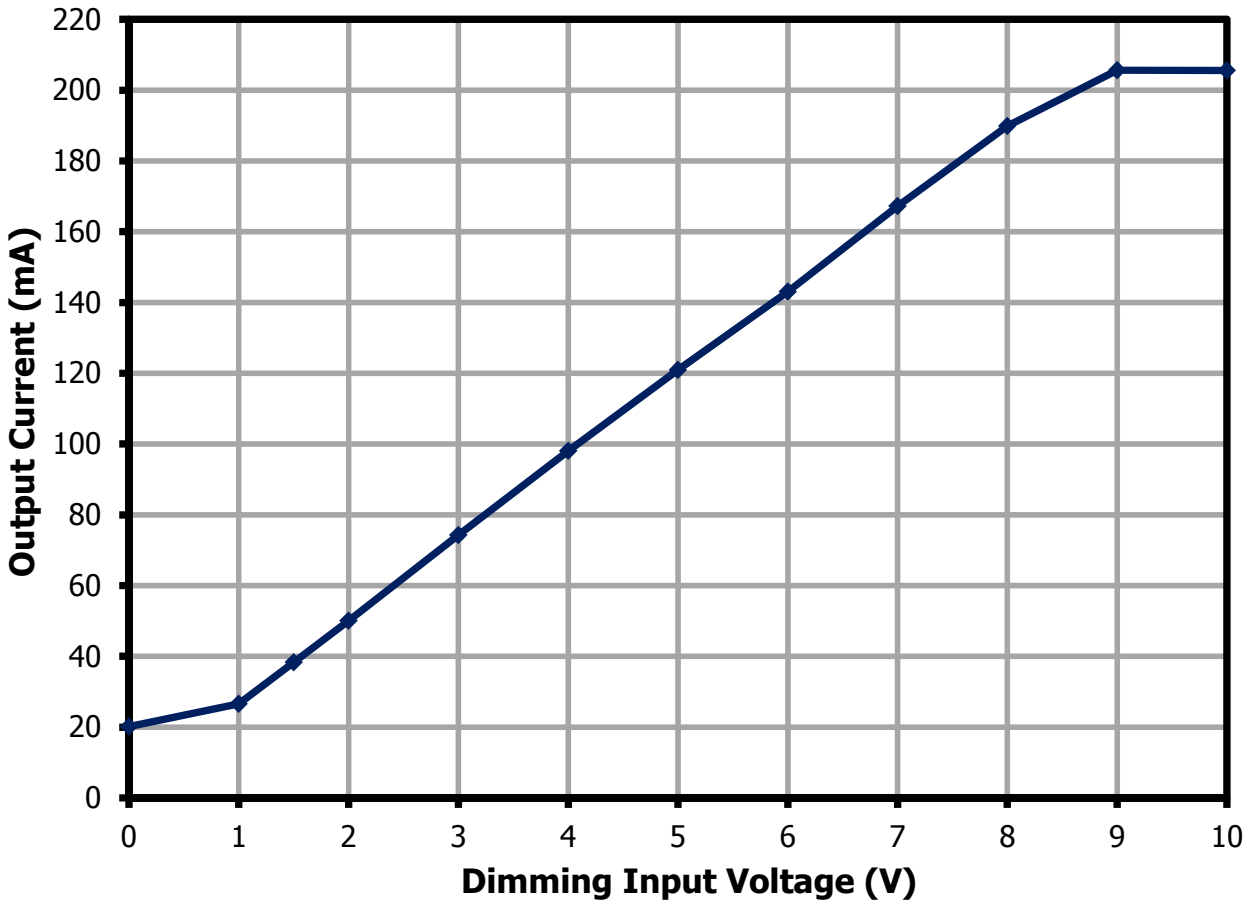

Figure 16 – Output Current vs. Dimming Input Voltage.

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10 **Test Data**

10.1 Test Data, 50 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
90	60	89.88	142.48	11.63	0.91	39.2	50.85	202.50	10.30	88.60
110	60	99.91	128.33	11.78	0.92	37.7	51.23	204.47	10.48	88.99
115	60	114.90	110.17	11.74	0.93	34.6	51.18	204.83	10.49	89.37
120	60	119.87	105.60	11.74	0.93	34.0	51.17	204.97	10.49	89.37
132	60	131.93	96.41	11.76	0.92	33.0	51.17	205.74	10.53	89.53

10.2 Test Data, Harmonic Content at 115 VAC, 50 V LED Load

V	Freq	I (mA)	P	PF	%THD
115	60.00	110.17	11.74	0.93	34.62
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
1	98.67				
2	0.31	0.00		0.02	
3	23.83	0.24	79.80	0.28	Pass
5	16.57	0.17	44.59	0.10	Pass
7	18.61	0.19	23.47	0.07	Pass
9	6.37	0.06	11.74	0.05	Pass
11	2.27	0.02	8.21	0.03	Pass
13	4.37	0.04	6.95	0.03	Pass
15	2.09	0.02	6.02	0.03	Pass
17	1.27	0.01	5.32	0.03	Pass
19	1.68	0.02	4.76	0.03	Pass
21	0.90	0.01	4.30	0.03	Pass
23	1.32	0.01	3.93	0.03	Pass
25	1.91	0.02	3.61	0.03	Pass
27	1.00	0.01	3.35	0.03	Pass
29	0.07	0.00	3.12	0.03	Pass
31	0.56	0.01	2.91	0.03	Pass
33	0.71	0.01	2.74	0.03	Pass
35	0.79	0.01	2.58	0.03	Pass
37	0.76	0.01	2.44	0.03	Pass
39	0.66	0.01	2.32	0.03	Pass
41	0.48	0.00			
43	0.74	0.01			
45	0.70	0.01			
47	0.26	0.00			
49	0.39	0.00			

11 Thermal Performance

11.1 Thermal Performance at 25 °C Ambient (Open Frame)

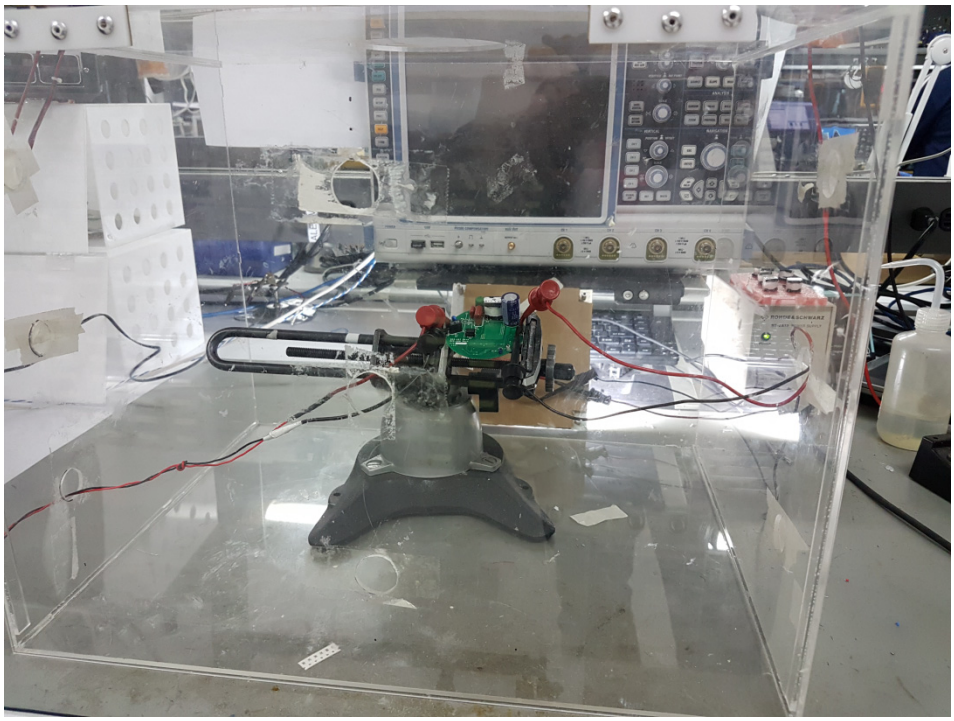

Figure 17 – 25 °C Ambient Test Set-up.

Unit was placed inside an acrylic enclosure to prevent airflow that might affect the thermal measurements. Temperature was measured using FLIR thermal camera. The ambient temperature is 28 ºC.

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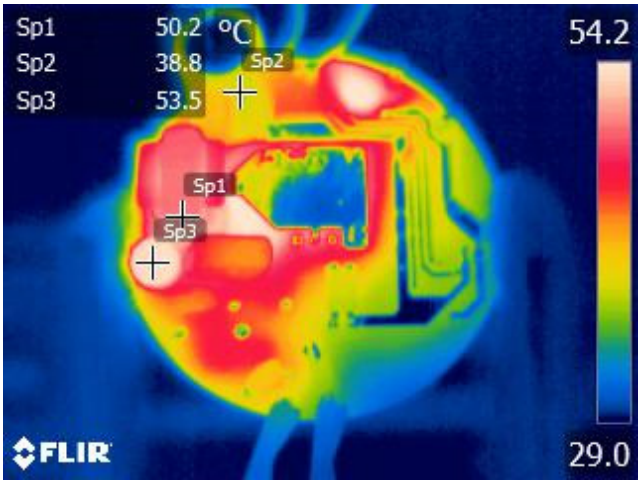

Figure 18 – 90 VAC, 50 V LED Load.
Spot 1: Buck Inductor (T2): 50.2 ºC.
Spot 2: Output Capacitor (C6): 38.8 ºC.
Spot 3: Input Inductor (L1): 53.5 ºC.

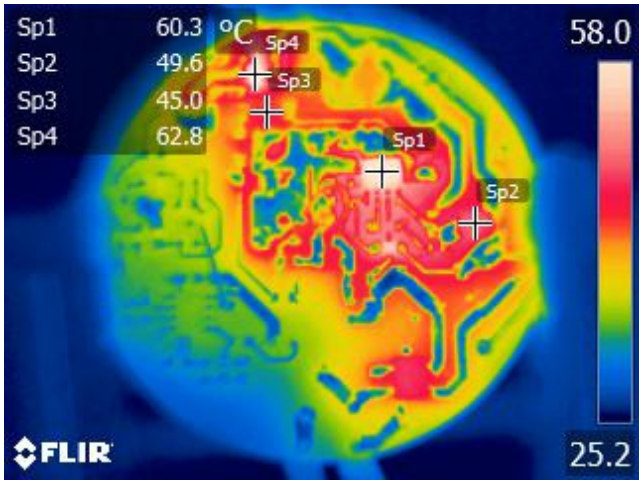

Figure 19 – 90 VAC, 50 V LED Load.
Spot 1: LYTSwitch-1 (U2): 60.3 ºC.
Spot 2: Freewheeling Diode (D1): 49.6 ºC.
Spot 3: Auxiliary Diode (D2): 45 ºC.
Spot 4: Series Pass Transistor (Q2): 62.8 ºC.

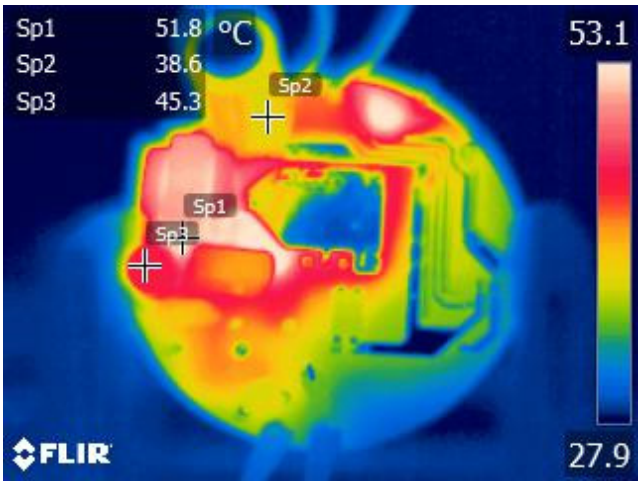

Figure 20 – 132 VAC, 50 V LED Load.
Spot 1: Buck Inductor (T2): 51.8 ºC.
Spot 2: Output Capacitor (C6): 38.6 ºC.
Spot 3: Input Inductor (L1): 45.3 ºC.

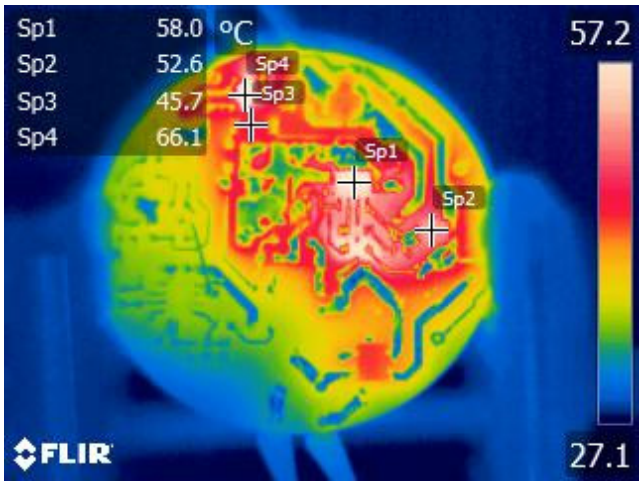

Figure 21 – 132 VAC, 50 V LED Load.
Spot 1: LYTSwitch-1 (U2): 58 ºC.
Spot 2: Freewheeling Diode (D1): 52.6 ºC.
Spot 3: Auxiliary Diode (D2): 45.7 ºC.
Spot 4: Series Pass Transistor (Q2): 66.1 ºC.

11.2 Thermal Performance at 65 °C Ambient (Open Frame)

Unit in open frame was placed inside an enclosure to prevent airflow that might affect the thermal measurements. Ambient temperature inside enclosure is 65 ºC. Temperature was measured using type T thermocouple.

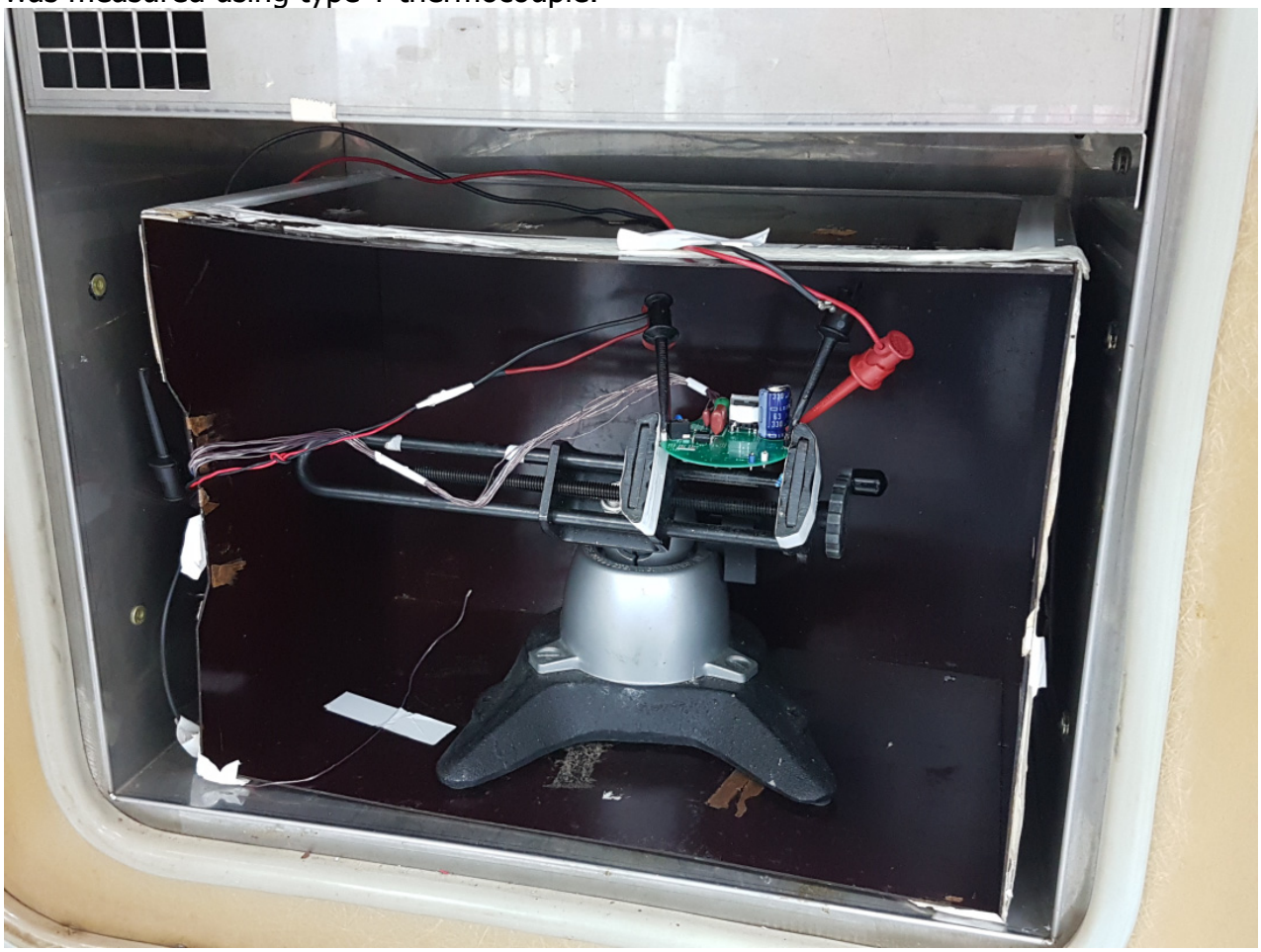

Figure 22 – 65 °C Ambient Test Set-up.

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Measurement	Ambient	LYTSwitch-1	T2	C9	L1	D1	Q2	U4	D2
Maximum (ºC)	64	92.2	88.5	76.1	90.2	83.7	87.3	73.2	81.3
Final (ºC)	64	92.2	88.5	76.1	90.2	83.7	87.3	73.1	81.2

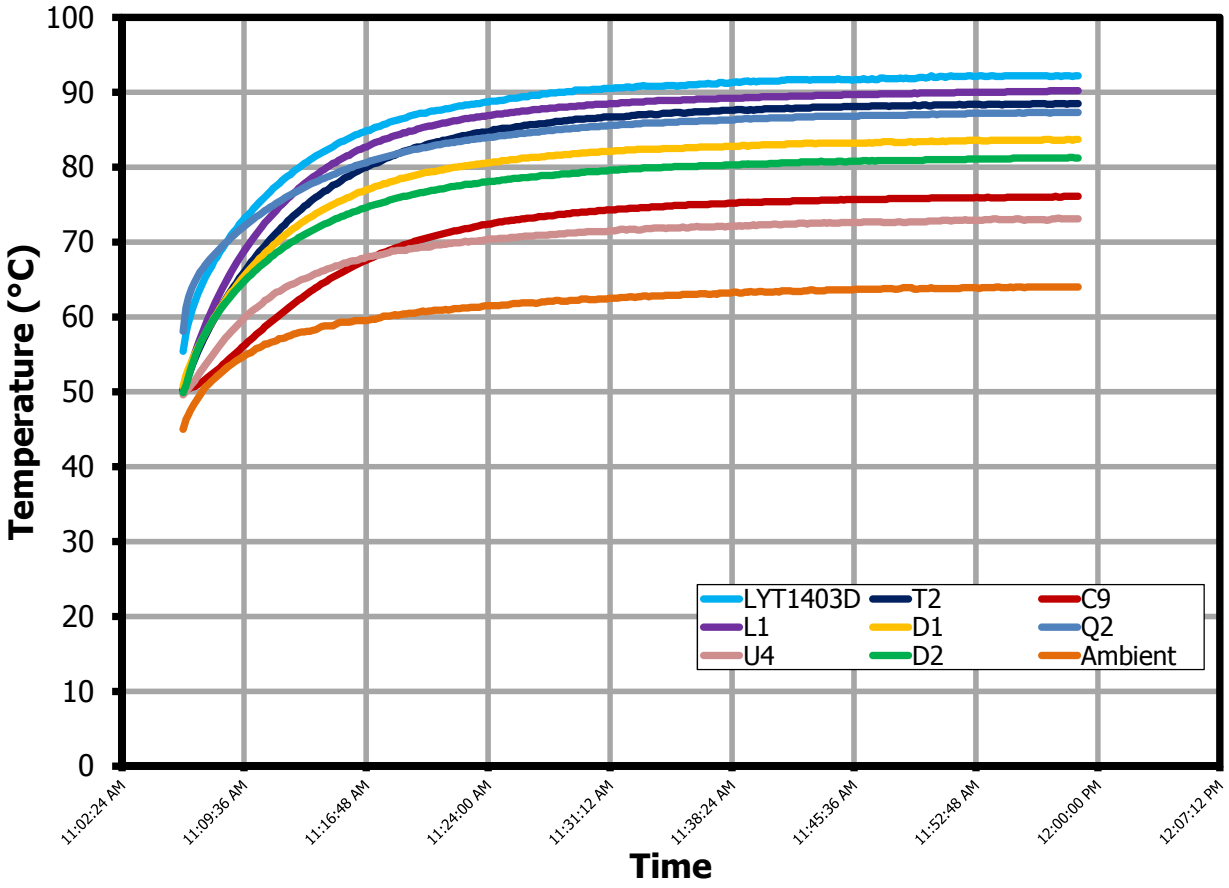

Figure 23 – Temperature Measurements. 90 VAC, 50 V LED Load.

Measurement	Ambient	LYTSwitch-1	T2	C9	L1	D1	Q2	U4	D2
Maximum (ºC)	64.7	88.6	88	75.8	84.7	83.6	87.2	73.1	80
Final (ºC)	64.6	88.4	87.9	75.7	83.4	83.5	87.1	73	79.9

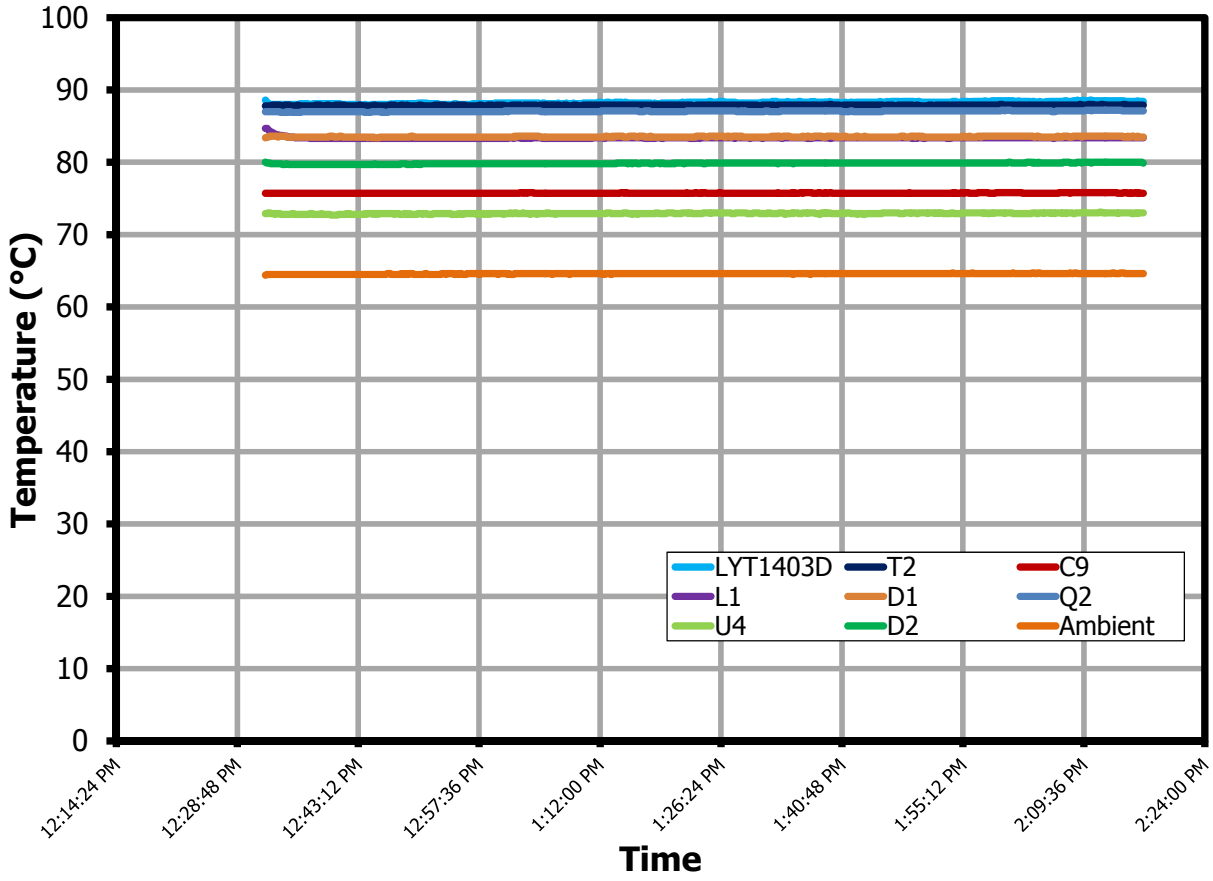

Figure 24 – Temperature Measurements. 132 VAC, 50 V LED Load.

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12 Waveforms

12.1 Input Voltage and Input Current Waveforms

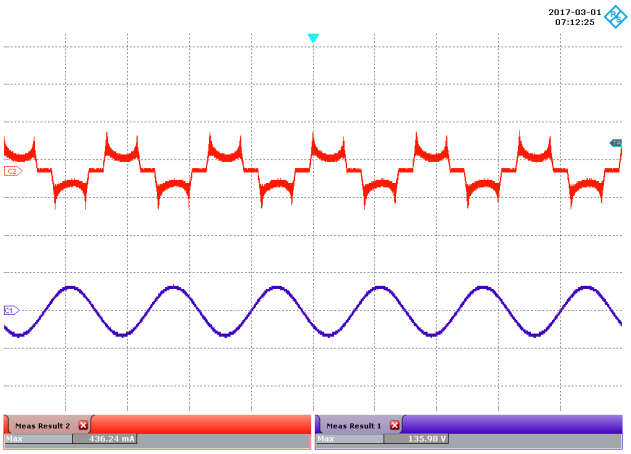

Figure 25 – 90 VAC, 50 V LED Load.
Upper: I_{IN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 10 ms / div.

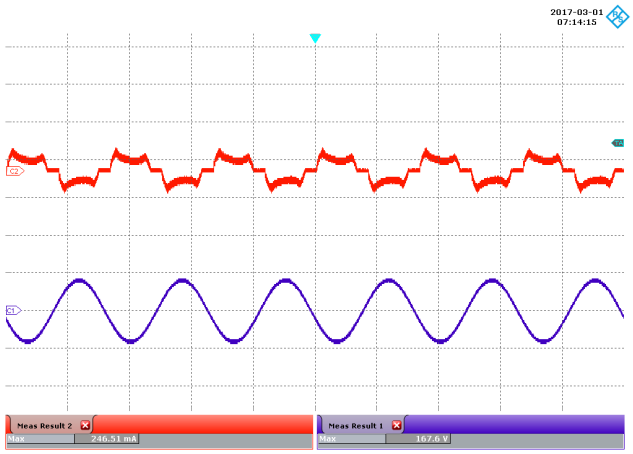

Figure 26 – 115 VAC, 50V LED Load.
Upper: I_{IN}, 400 mA / div.
Lower: V_{IN}, 100 V / div., 10 ms / div.

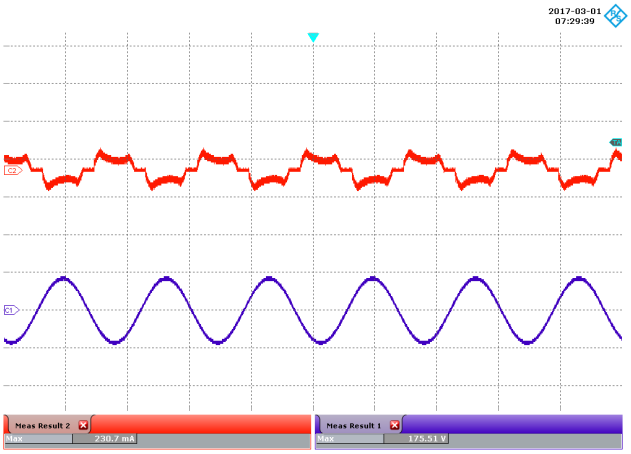

Figure 27 – 120 VAC, 50 V LED Load.
Upper: I_{IN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 10 ms / div.

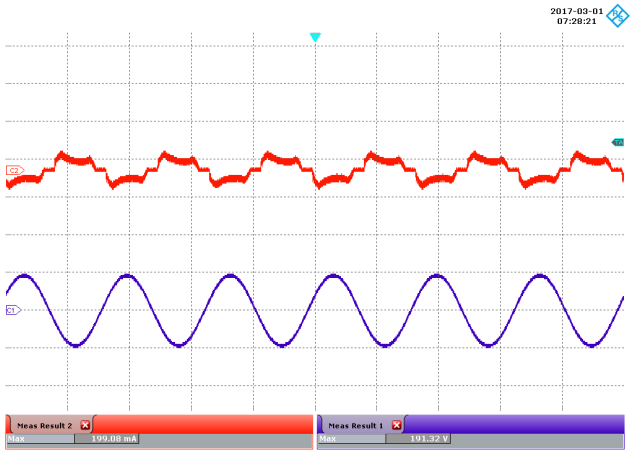

Figure 28 – 132 VAC, 50 V LED Load.
Upper: I_{IN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 10 ms / div.

12.2 Start-up Profile

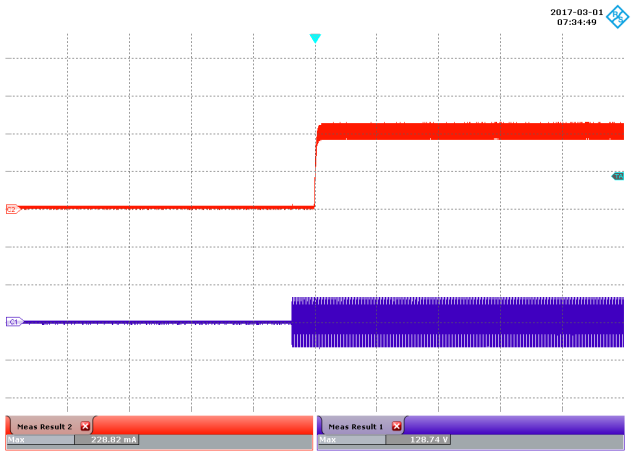

Figure 29 – 90 VAC, 50 V LED, Output Rise.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 1 s / div.

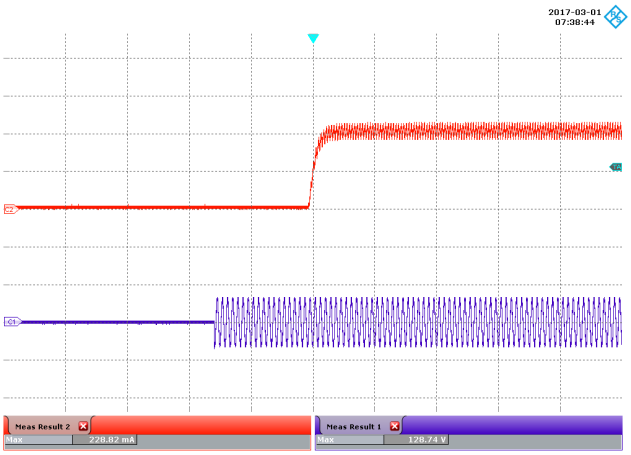

Figure 30 – 90 VAC, 50 V LED, Output Rise.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 200 ms / div.

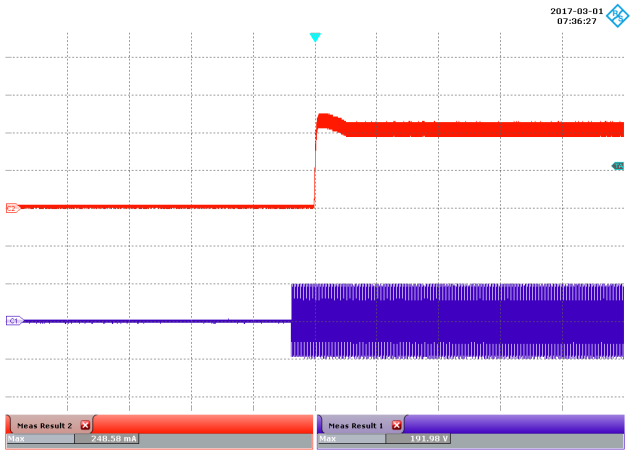

Figure 31 – 132 VAC, 50 V LED, Output Rise.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 1 s / div.

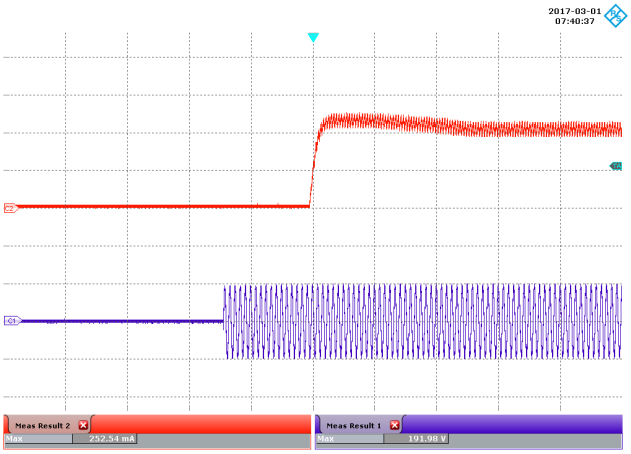

Figure 32 – 132 VAC, 50 V LED, Output Rise.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 200 ms / div.

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12.3 Output Current Fall

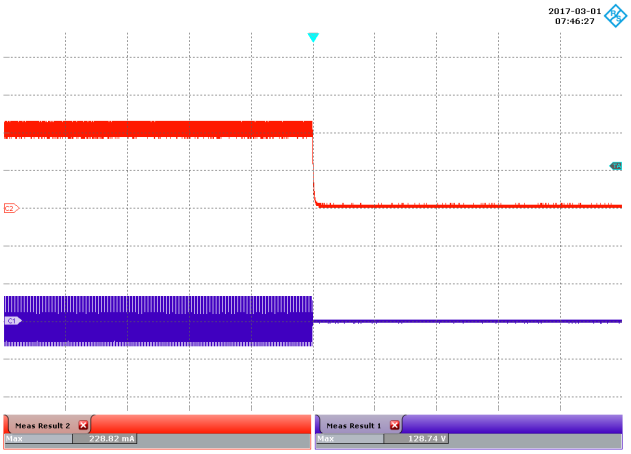

Figure 33 – 90 VAC, 50 V LED, Output Fall.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 1 s / div.

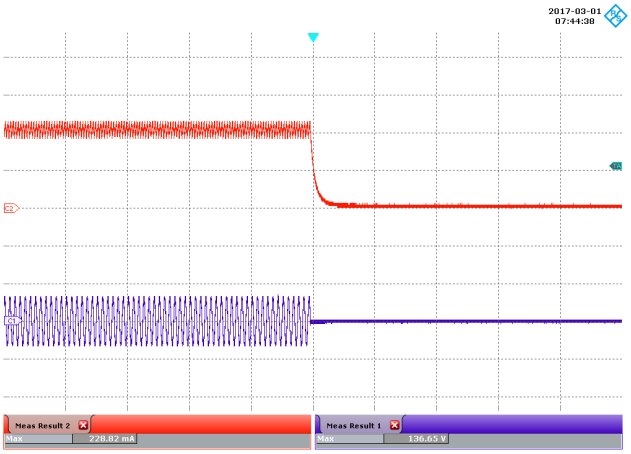

Figure 34 – 90 VAC, 50 V LED, Output Fall.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 200 ms / div.

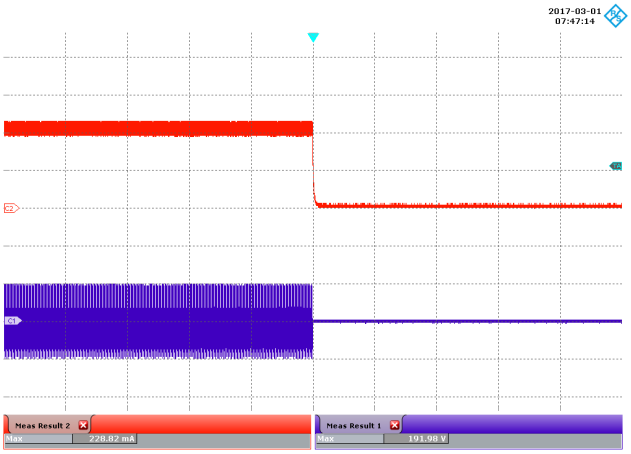

Figure 35 – 132 VAC, 50 V LED, Output Fall.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 1 s / div.

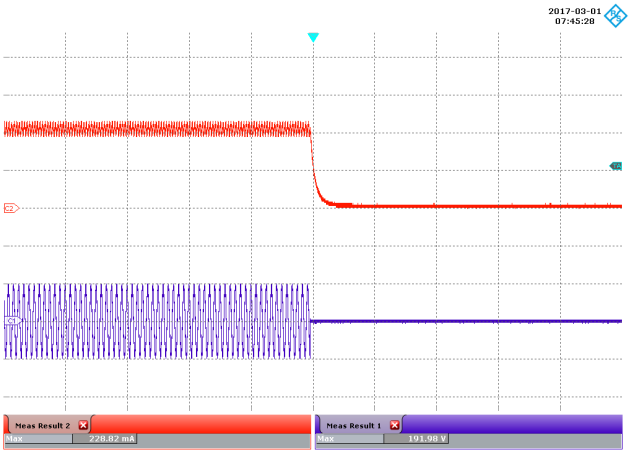

Figure 36 – 132 VAC, 50 V LED, Output Fall.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 200 V / div., 200 ms / div.

12.4 Drain Voltage and Current in Normal Operation

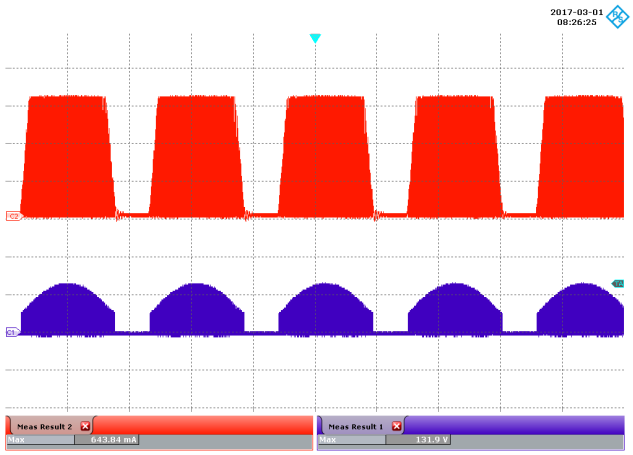

Figure 37 – 90 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100V / div., 4 ms / div.

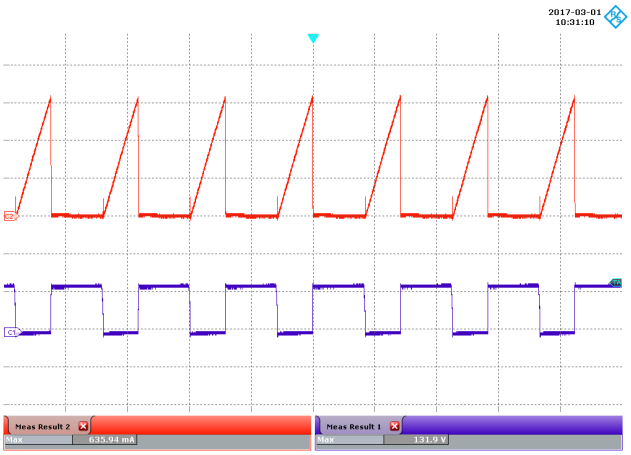

Figure 38 – 90 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 µs / div.

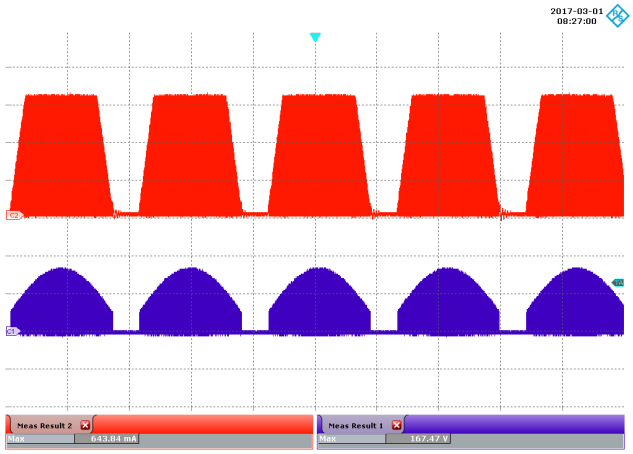

Figure 39 – 115 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100V / div., 4 ms / div.

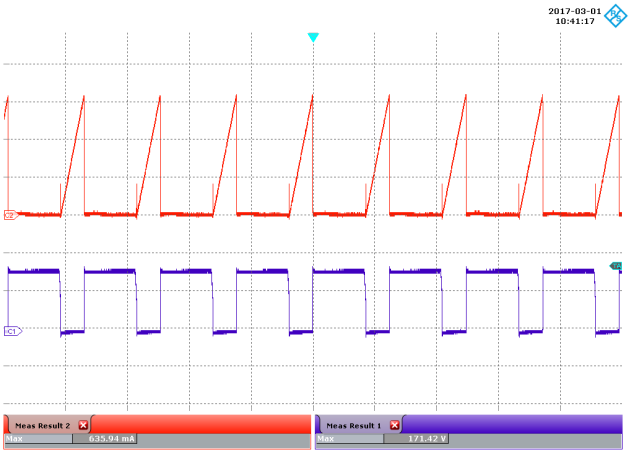

Figure 40 – 115 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 µs / div.

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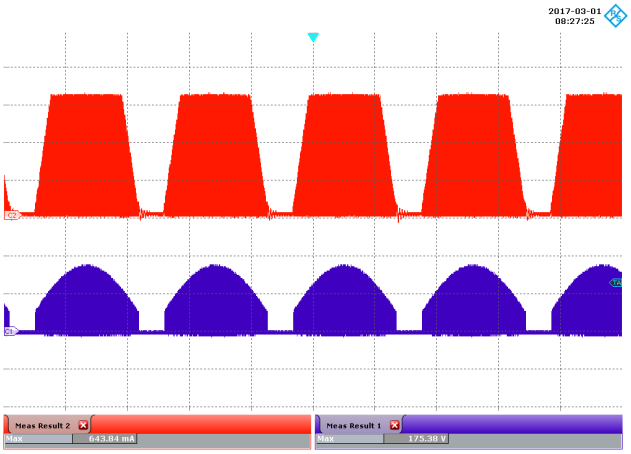

Figure 41 – 120 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100V / div., 4 ms / div.

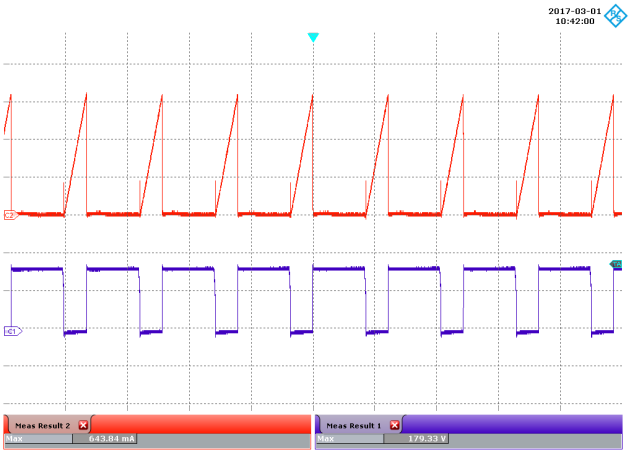

Figure 42 – 120 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 μs / div.

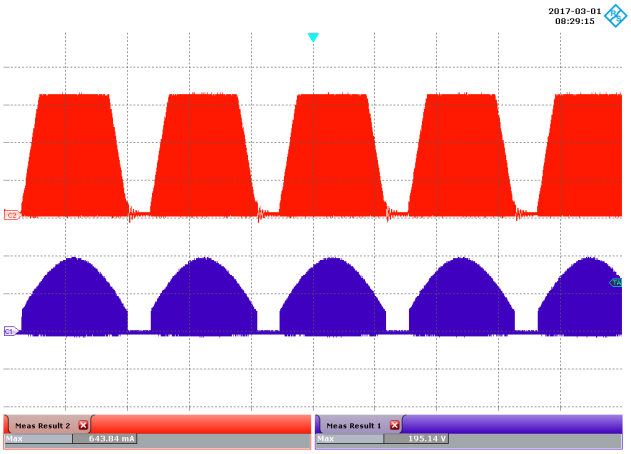

Figure 43 – 132 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100V / div., 4 ms / div.

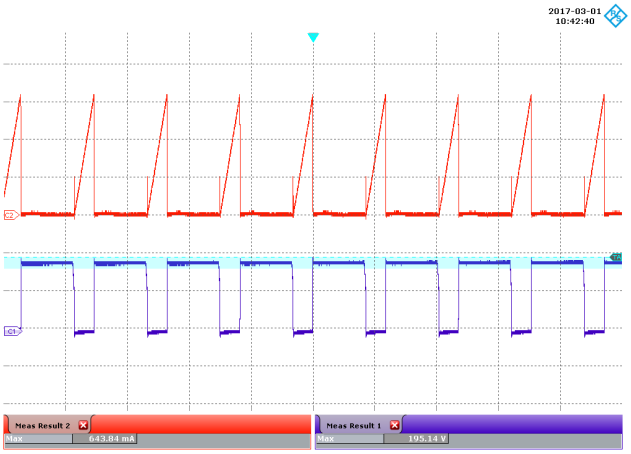

Figure 44 – 132 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 μs / div.

12.5 Drain Voltage and Current Start-up Profile

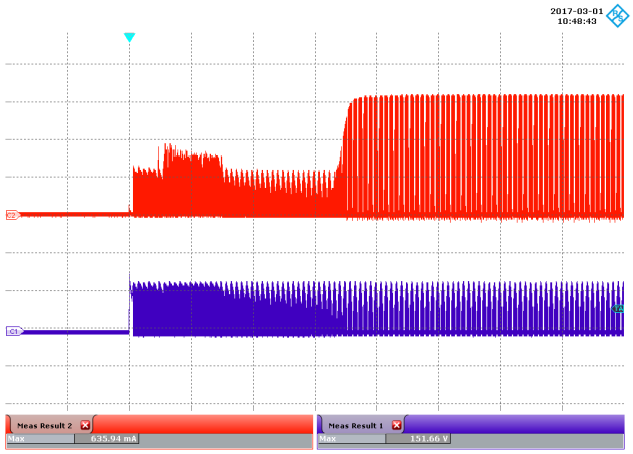

Figure 45 – 90 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 100 ms / div.

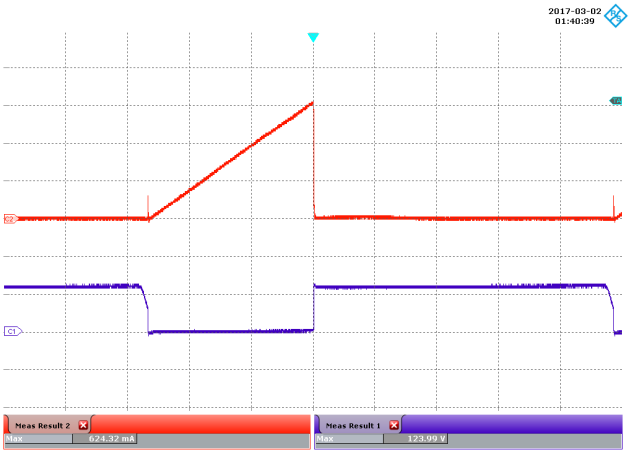

Figure 46 – 90 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 4 us / div.

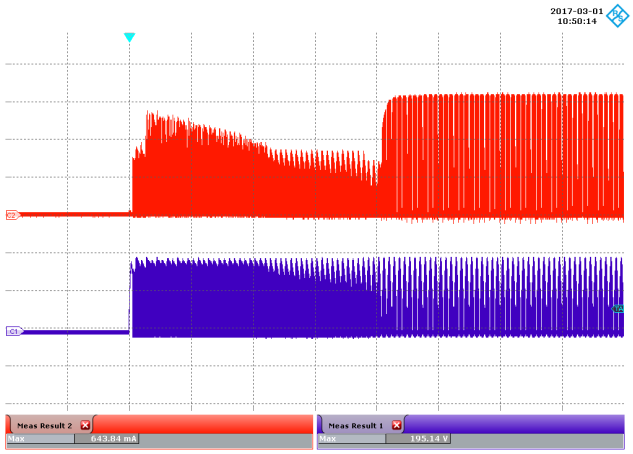

Figure 47 – 132 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 100 ms / div.

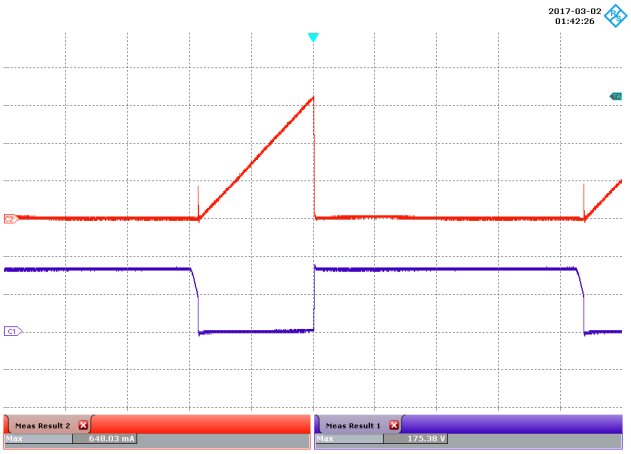

Figure 48 – 132 VAC, 50 V LED Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 4 us / div.

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12.6 Drain Voltage and Current During Output Short-Circuit

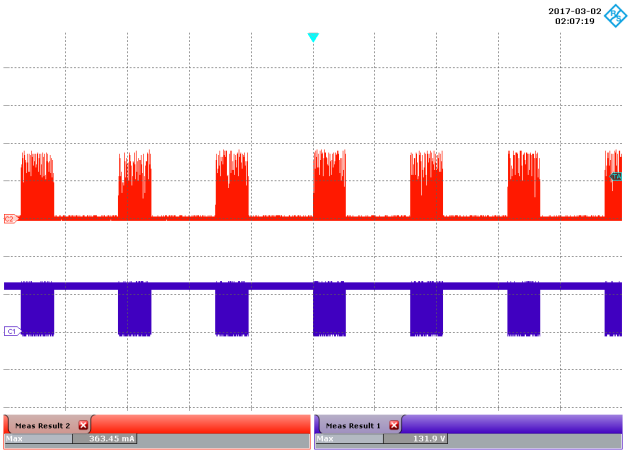

Figure 49 – 90 VAC, Output Short-Circuit.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 1 s / div.

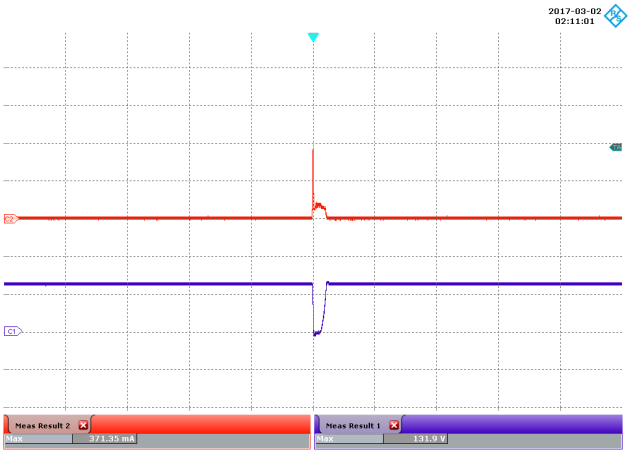

Figure 50 – 90 VAC, Output Short-Circuit.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 μs / div.

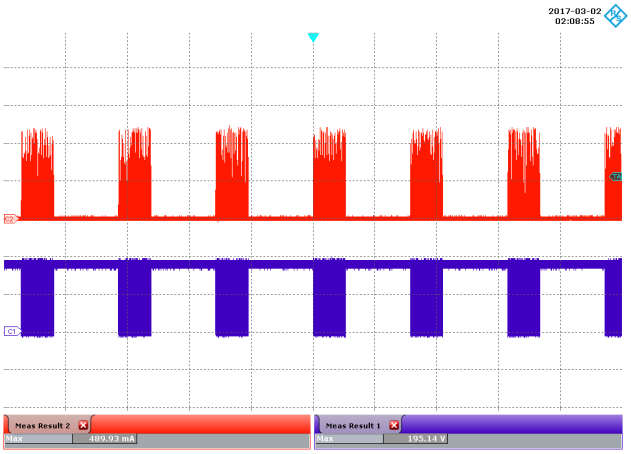

Figure 51 – 132 VAC, Output Short-Circuit.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 1 s / div.

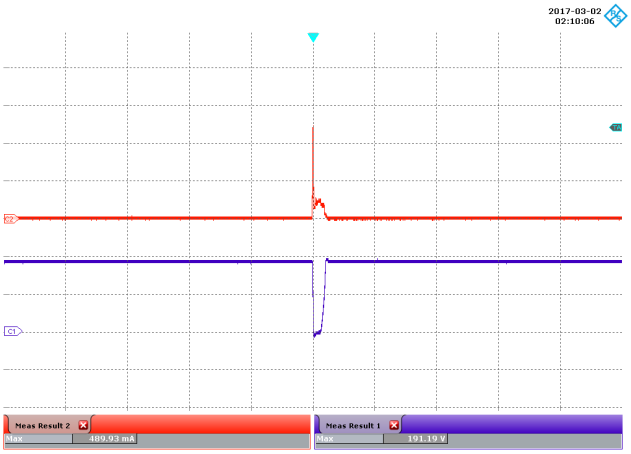

Figure 52 – 132 VAC, Output Short-Circuit.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V / div., 20 μs / div.

Input Power During Short-Circuit		
VAC (V_{RMS})	**Freq (Hz)**	**P (W)**
90	60	0.1076
115	60	0.1706
120	50	0.1859
132	50	0.2257

12.7 Output Diode Voltage and Current in Normal Operation

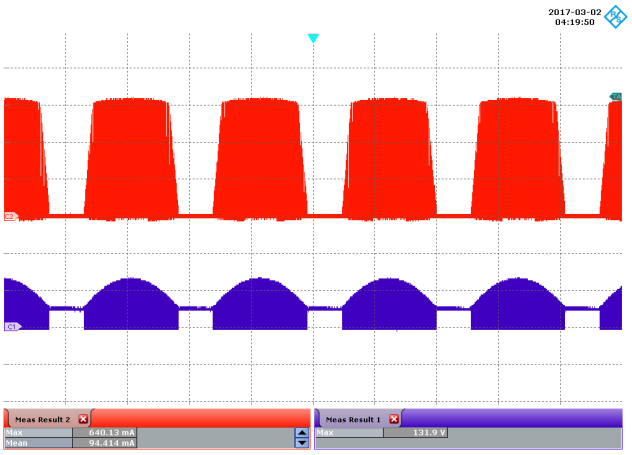

Figure 53 – 90 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_D, 100 V / div., 4 ms / div.

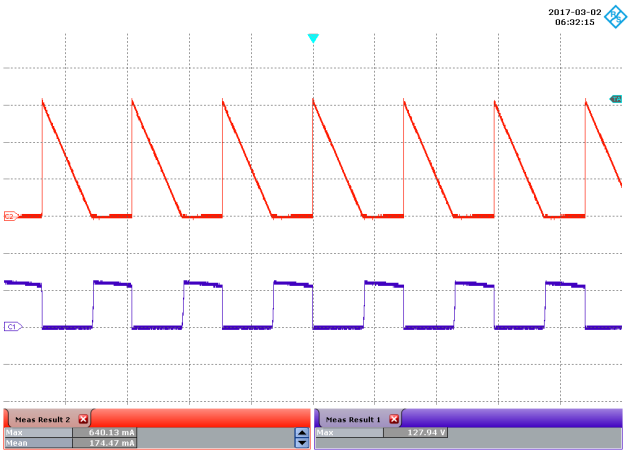

Figure 54 – 90 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_{D1}, 100 V / div., 20 µs / div.

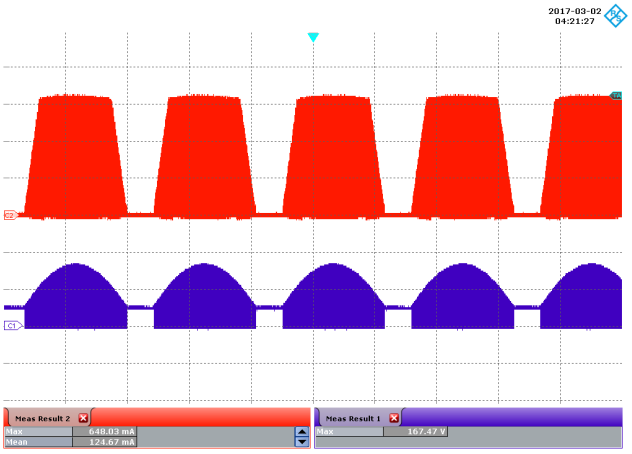

Figure 55 – 115 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_D, 100 V / div., 4 ms / div.

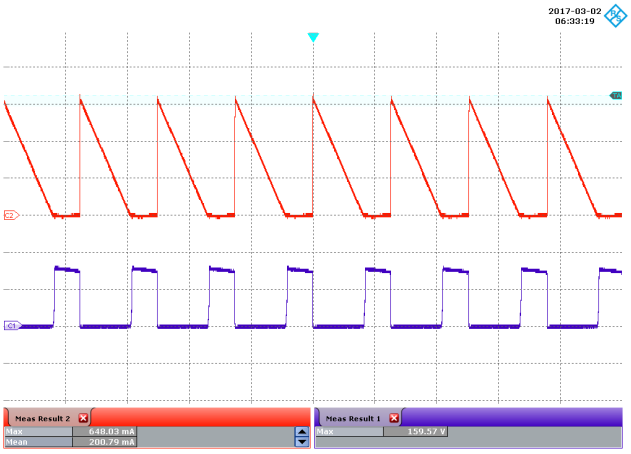

Figure 56 – 115 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_{D1}, 100 V / div., 20 µs / div.

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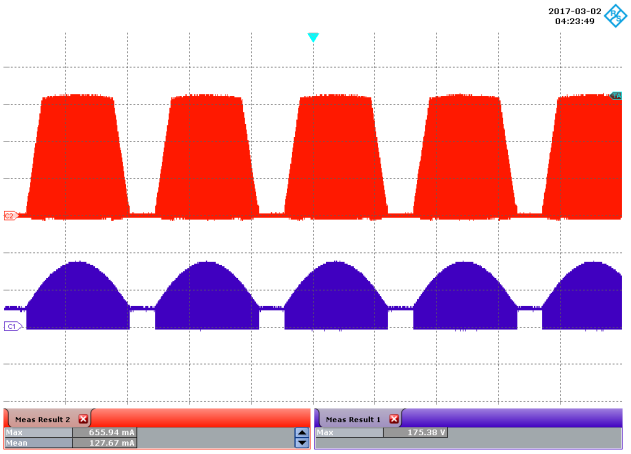

Figure 57 – 120 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_D, 100 V / div., 4 ms / div.

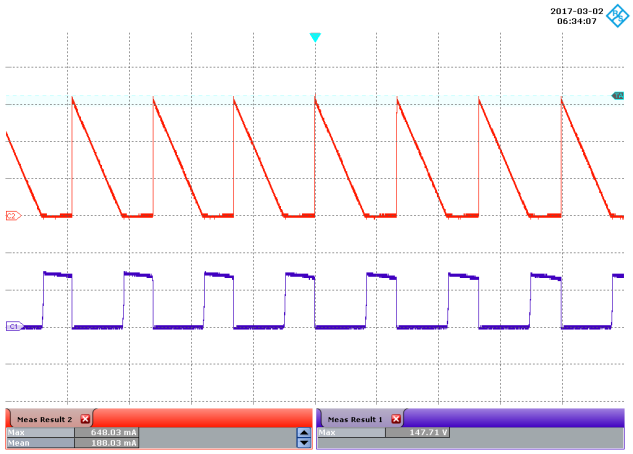

Figure 58 – 120 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_{D1}, 100 V / div., 20 μs / div.

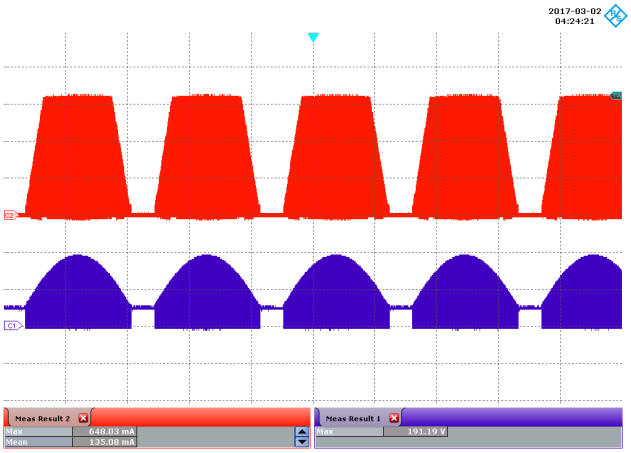

Figure 59 – 132 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_D, 100 V / div., 4 ms / div.

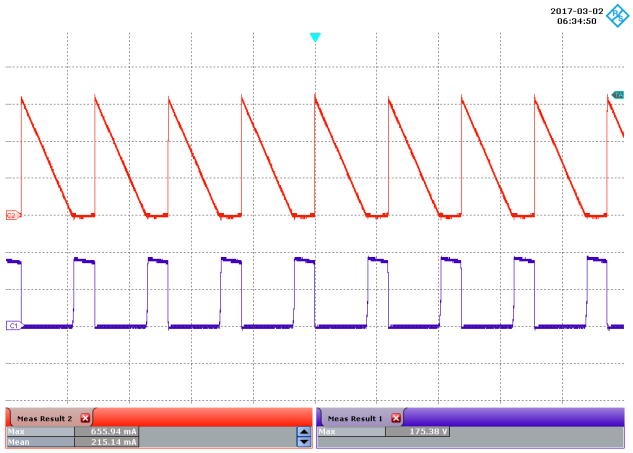

Figure 60 – 132 VAC, 50 V LED Load.
Upper: I_D, 200 mA / div.
Lower: V_{D1}, 100 V / div., 20 μs / div.

12.8 Output Voltage and Current – Open Output LED Load

Maximum measured no-load output voltage is below the surge voltage rating of the output capacitor.

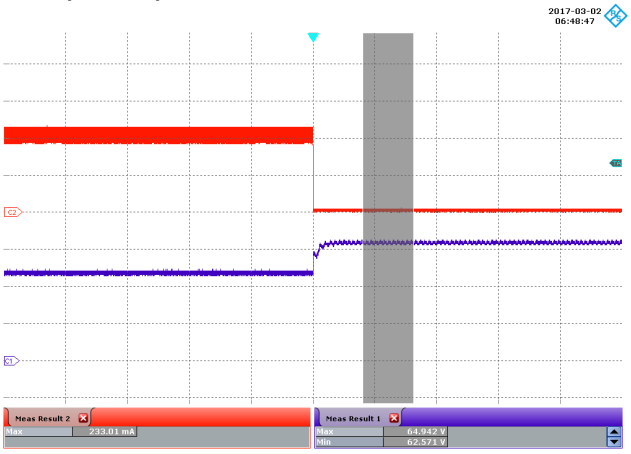

Figure 61 – 90 VAC, 50 V LED Load.
Running Open Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V / div., 2 s / div.

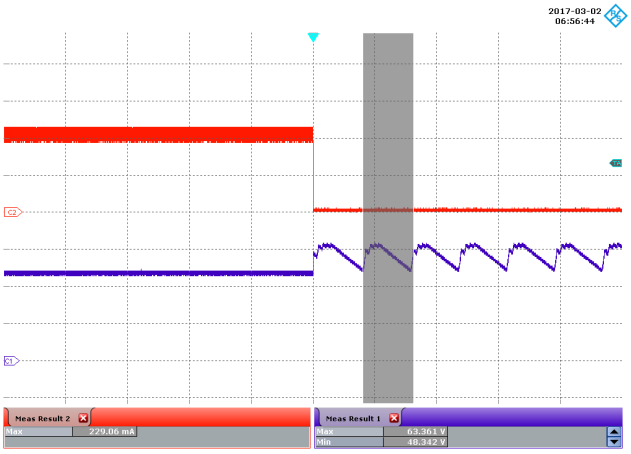

Figure 62 – 132 VAC, 50 V LED Load.
Running Open Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V / div., 2 s / div.

12.9 Output Voltage and Current – Start-up at Open Output Load

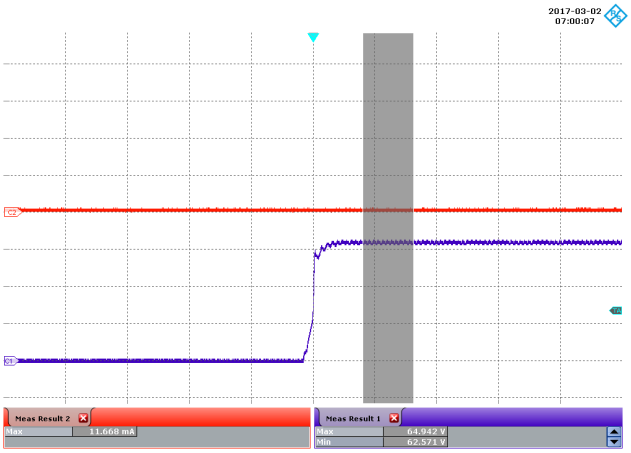

Figure 63 – 90 VAC, Open Load.
Open Load Start-up.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V / div., 2 s / div.

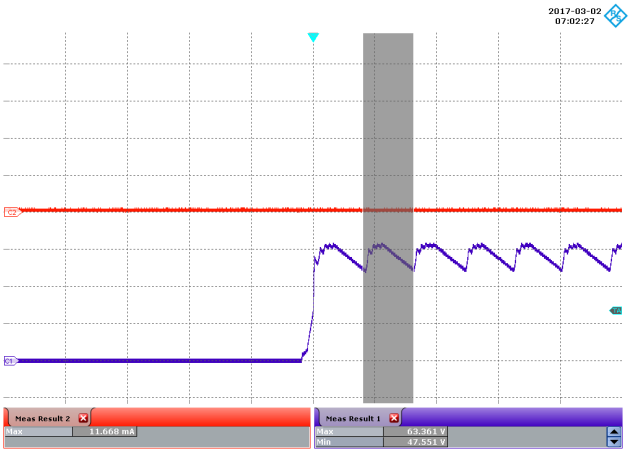

Figure 64 – 132 VAC, Open Load.
Open Load Start-up.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V / div., 2 s / div.

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12.10 Output Ripple Current

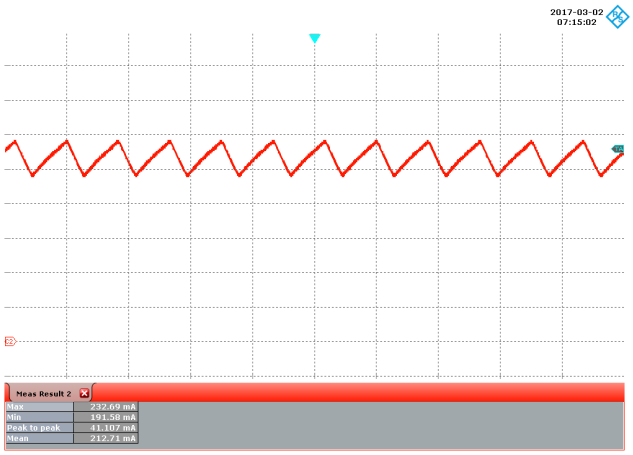

Figure 65 – 90 VAC, 60 Hz, 50 V LED Load.
Upper: I_{OUT}, 40 mA / div., 10 ms / div.

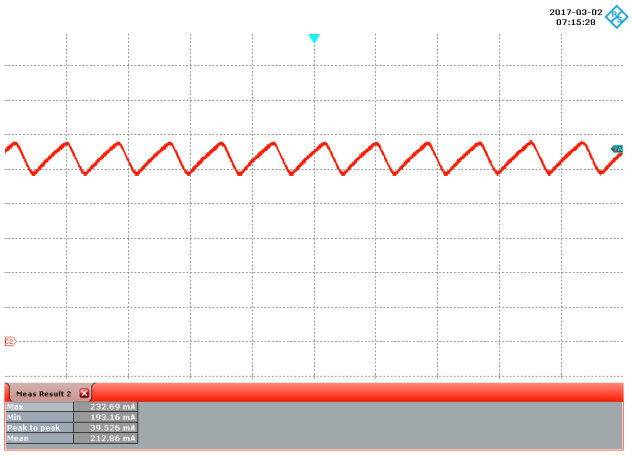

Figure 66 – 115 VAC, 60 Hz, 50 V LED Load.
Upper: I_{OUT}, 40 mA / div., 10 ms / div.

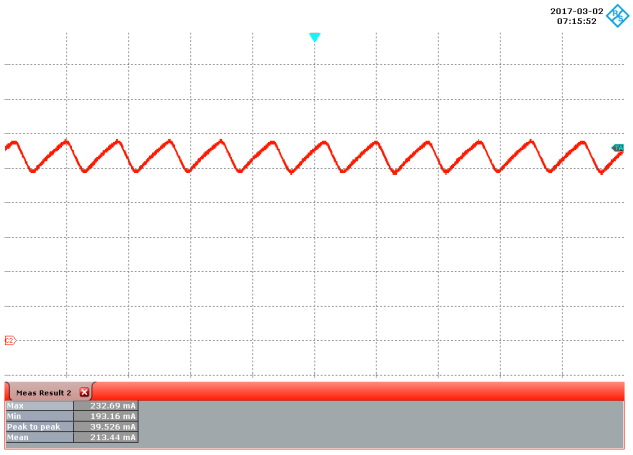

Figure 67 – 120 VAC, 60 Hz, 50 V LED Load.
Upper: I_{OUT}, 40 mA / div., 10 ms / div.

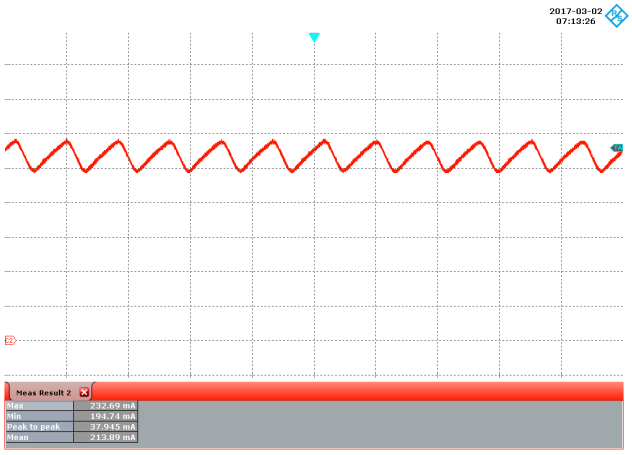

Figure 68 – 132 VAC, 60 Hz, 50 V LED Load.
Upper: I_{OUT}, 40 mA / div., 10 ms / div.

V_{IN} (VAC)	$I_{OUT(MAX)}$ (mA)	$I_{OUT(MIN)}$ (mA)	I_{MEAN} (mA)	Ripple Ratio (I_{RP-P}/I_{MEAN})	% Flicker 100 x (I_{RP-P} / $I_{OUT(MAX)}$+$I_{OUT(MIN)}$)
90	232.69	191.58	212.71	0.19	9.69
115	232.69	193.16	212.86	0.19	9.28
120	232.69	193.16	213.44	0.19	9.28
132	232.69	194.74	213.89	0.18	8.88

13 **AC Cycling Test**

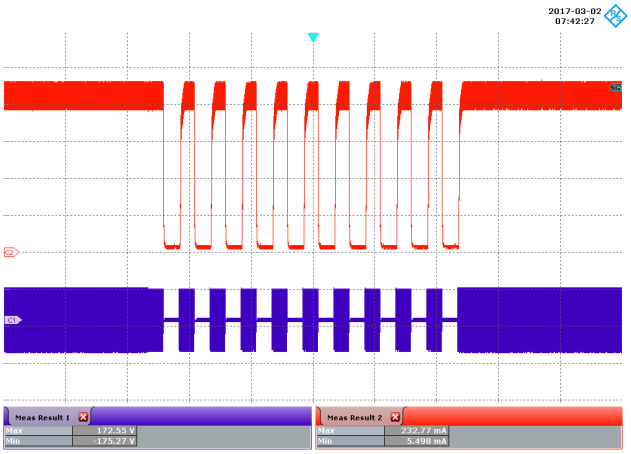

Figure 69 – 115 VAC, 50 V LED Load.
1 s On – 1 s Off.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{IN}, 200 V / div., 4 s / div.

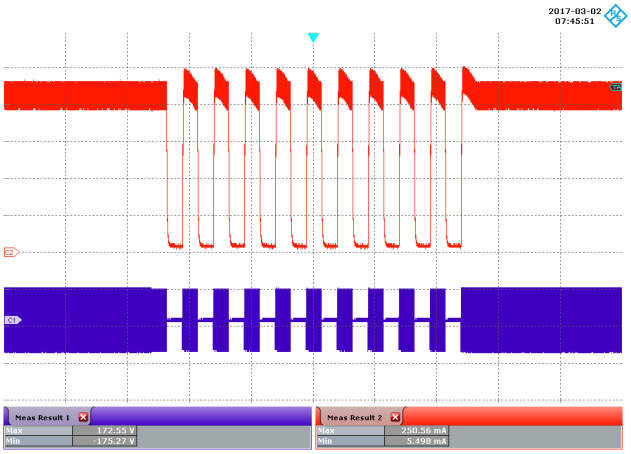

Figure 70 – 115 VAC, 50 V LED Load.
0.5 s On – 0.5 s Off.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{IN}, 200 V / div., 2 s / div.

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14 **Conducted EMI**

14.1 Test Set-up

14.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. 50 V LED load with input voltage set at 115 VAC.

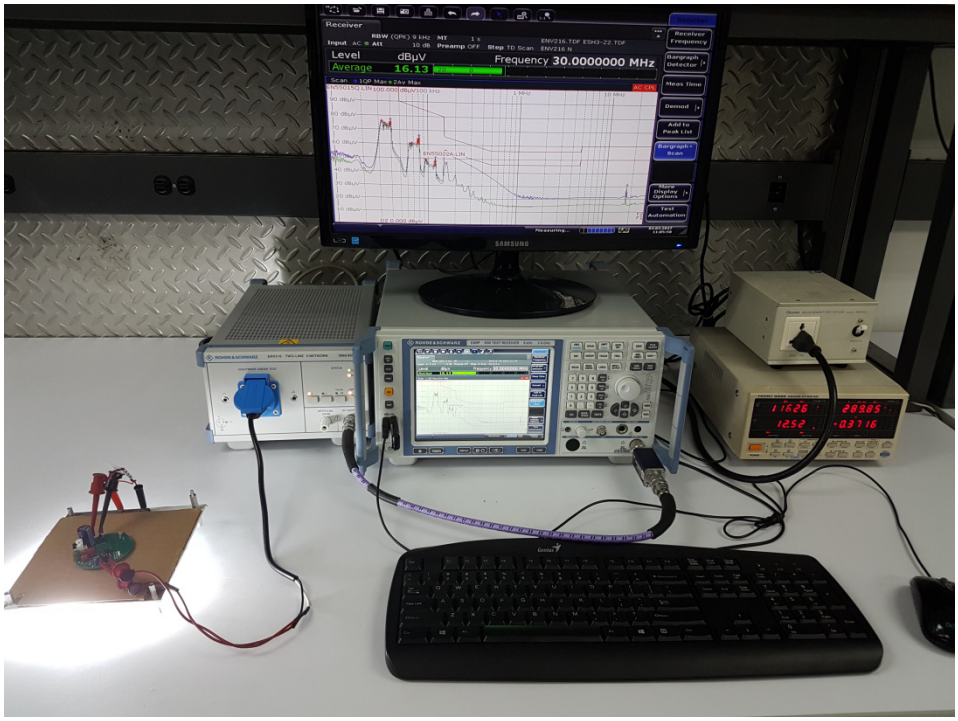
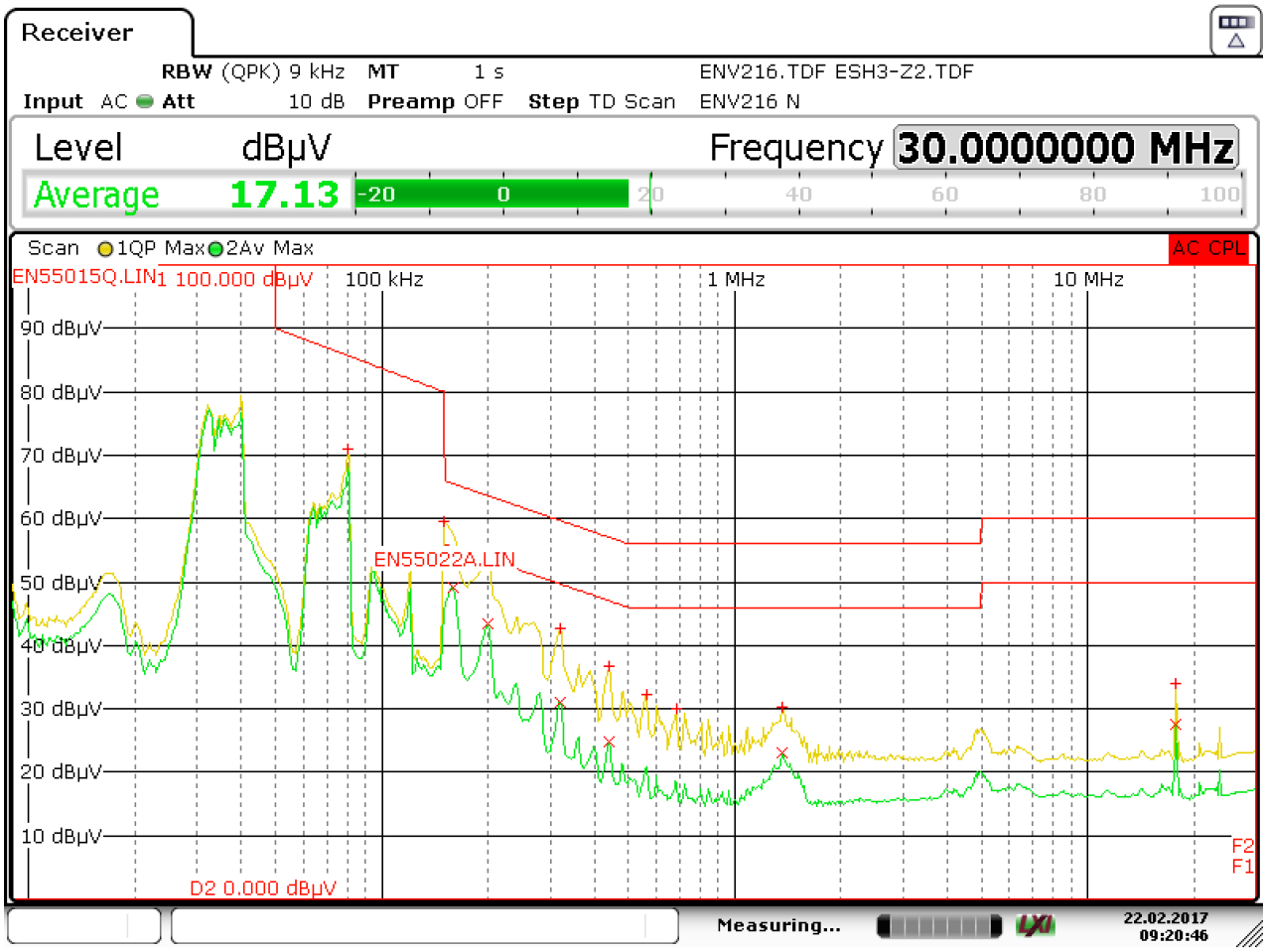


Figure 71 – Conducted EMI Test Set-up.

14.2 7EMI Test Result



Date: 22.FEB.2017 09:20:46

Figure 72 – Conducted EMI QP Scan at 50 V LED Load, 115 VAC, 60 Hz, and EN55015 B Limits.

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Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	159.0000 kHz	49.11 N	-6.41 dB
1 Quasi Peak	150.0000 kHz	59.52 N	-6.48 dB
2 Average	199.5000 kHz	43.37 N	-10.26 dB
1 Quasi Peak	80.1500 kHz	70.86 L1	-14.84 dB
1 Quasi Peak	321.0000 kHz	42.70 L1	-16.98 dB
2 Average	321.0000 kHz	31.09 N	-18.59 dB
1 Quasi Peak	442.5000 kHz	36.66 L1	-20.35 dB
2 Average	440.2500 kHz	24.78 L1	-22.28 dB
2 Average	17.7878 MHz	27.46 N	-22.54 dB
2 Average	1.3673 MHz	23.10 L1	-22.90 dB
1 Quasi Peak	561.7500 kHz	32.38 L1	-23.62 dB
1 Quasi Peak	1.3673 MHz	30.22 L1	-25.78 dB
1 Quasi Peak	683.2500 kHz	29.91 L1	-26.09 dB
1 Quasi Peak	17.7945 MHz	33.91 N	-26.09 dB

Figure 73 – Conducted EMI Data at 115 VAC, 50 V LED Load.

15 Line Surge

The unit was subjected to ±2500 V, 100 kHz ring wave and ±1000 V differential surge with 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	115	L to N	0	Pass
-1000	115	L to N	0	Pass
+1000	115	L to N	90	Pass
-1000	115	L to N	90	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	115	L to N	0	Pass
-2500	115	L to N	0	Pass
+2500	115	L to N	90	Pass
-2500	115	L to N	90	Pass

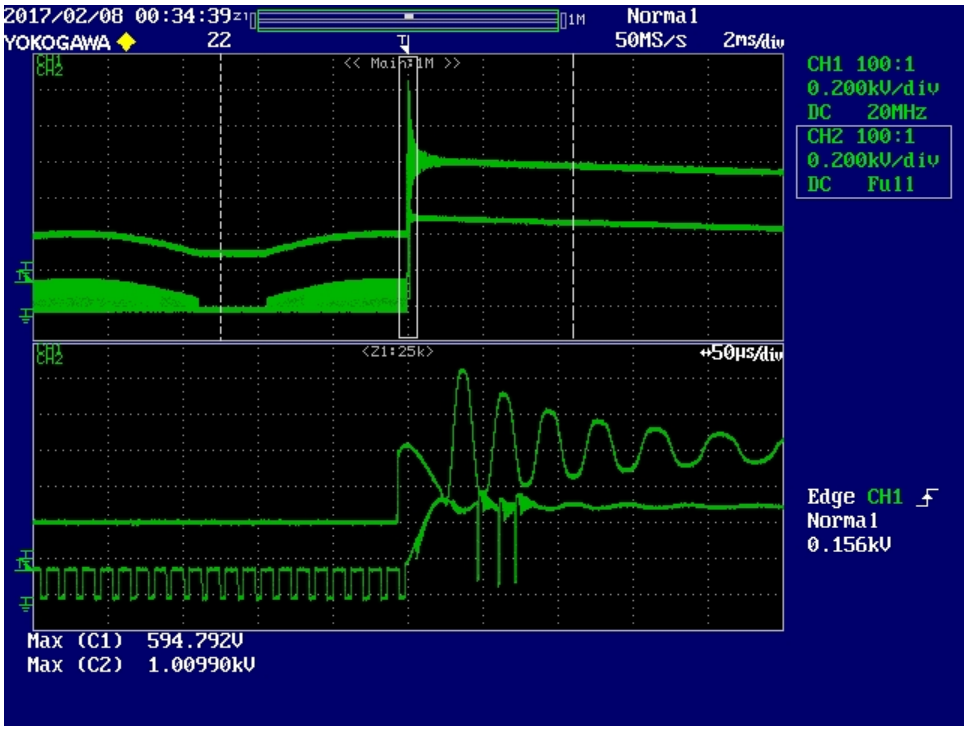

Figure 74 – +1000 kV Differential Surge, 90º Phase Angle.
V_{DRAIN}, 200 V / div., 2 ms / div.
V_{BULK}, 200 V / div., 2 ms / div.
Peak V_{DRAIN}: 594.79 V.

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16 Brown-in / Brown-out Test

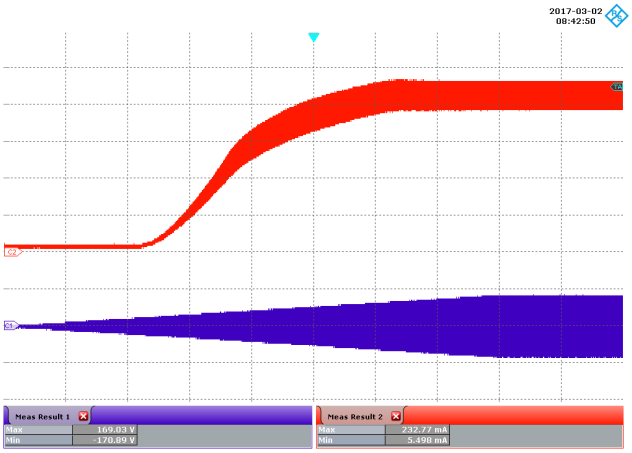

Figure 75 – 115 VAC Brown-in Test at 0.5 V / s.
Ch1: I_{OUT}, 50 mA / div.
Ch2: V_{IN}, 200 V / div.
Time Scale: 30 s / div.

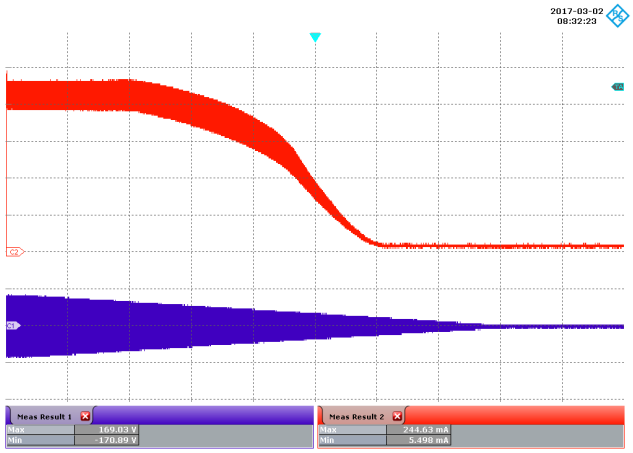

Figure 76 – 115 VAC Brown-out Test at 0.5 V / s.
Ch1: I_{OUT}, 50 mA / div.
Ch2: V_{IN}, 100 V / div.
Time Scale: 30 s / div.

17 **Revision History**

Date	Author	Revision	Description and Changes	Reviewed
30-May-17	AM	1.0	Initial release	Apps & Mktg

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