Design Example Report

Title	***18 W Constant Voltage / Constant Current (CV / CC), Universal Input, Isolated Flyback Converter Using LinkSwitch™-4 LNK4115D***
Specification	85 VAC – 265 VAC Input; 12 V, 1.5 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	DER-554
Date	January 11, 2016
Revision	1.0

Summary and Features

- Single-stage, constant voltage (CV) and constant current (CC) converter
- Primary-side regulated (no optocoupler)
- Cable voltage drop compensation function
- Highly optimized BJT drive for low switching loss and higher overall efficiency
- Meets CoC and DoE efficiency requirement using 1 meter, #22 AWG cable
- ±3% constant voltage (CV) regulation
- ±5% constant current (CC) regulation
- <40 mW no-load input power
- <150 mV_{PK-PK} voltage ripple
- At least 5 dB to 6 dB conducted EMI margin (with earth)
- Accurate regulation for line input and output load variations

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 1.5 A, 12 V isolated flyback converter utilizing the LinkSwitch-4 family of ICs. This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

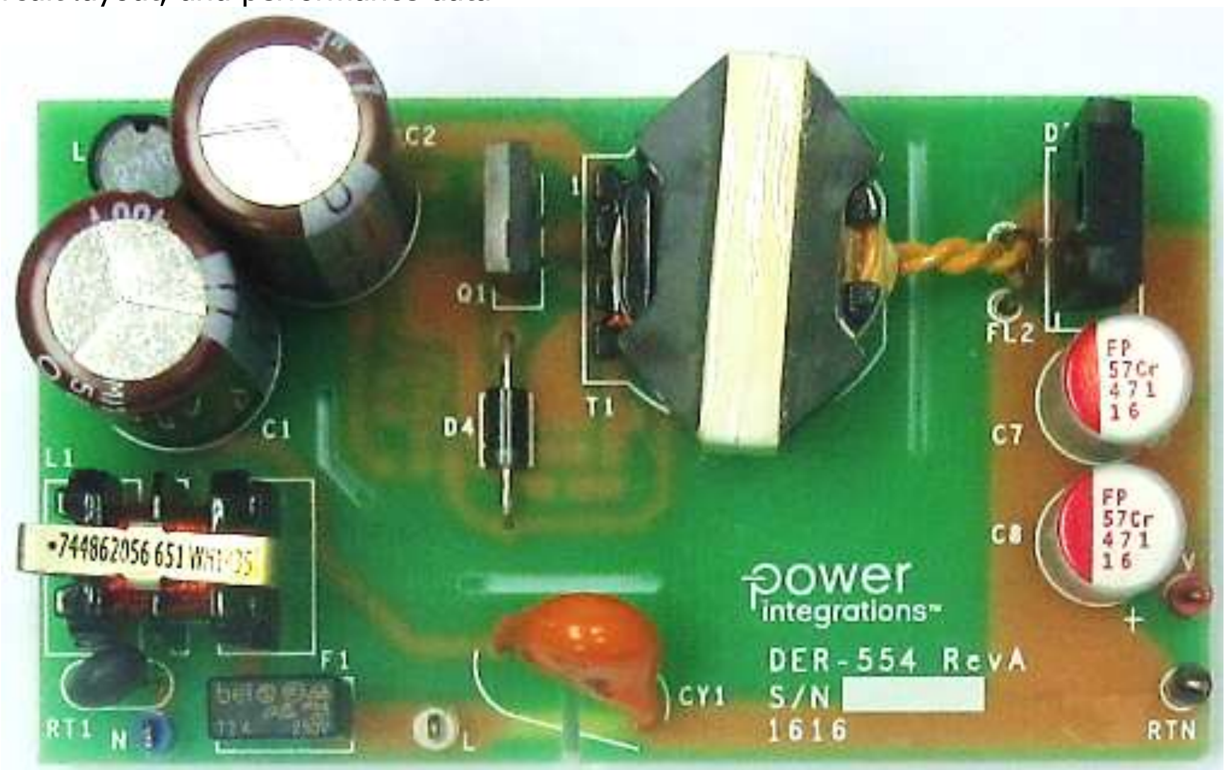

Figure 1 – Populated Circuit Board, Top.

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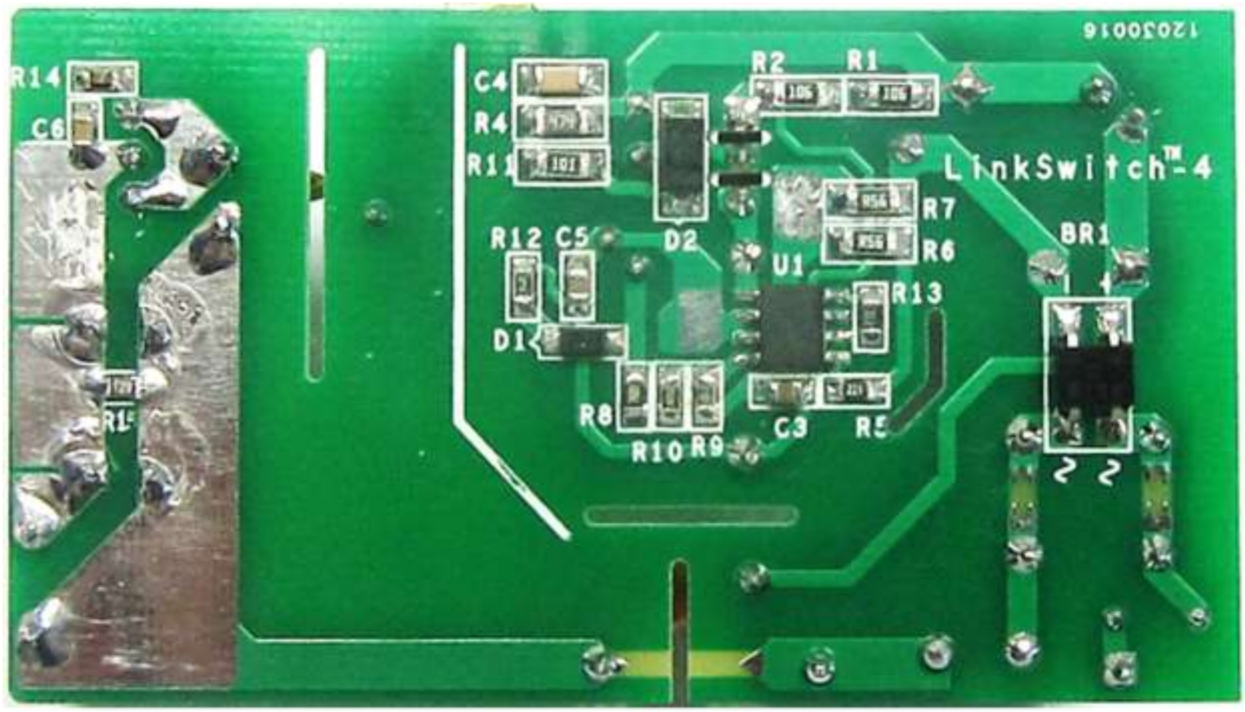

Figure 2 – Populated Circuit Board, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				75	mW	Less than 75 mW.
Output						
Output Voltage	V_{OUT}	11.64	12	12.36	V	Measured at the End of Cable.
Transient Output Voltage	$V_{OUT(T)}$	11.4		12.6	V	At the End of Cable.
Output Ripple Voltage	V_{RIPPLE}			150	mV	Output Ripple Voltage Measured at the End of Output Cable.
Output Cable Compensation	V_{CBL}		360		mV	At 1.5 A Output Current.
Output Current CC point	I_{OUT}	1.7	1.8	1.9	A	
Turn on Rise Time	t_R			20	ms	
Rated Output Power	P_{OUT}		18		W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	86			%	Measured at the End of Cable.
10%	$\eta_{10\%}$	84			%	Measured at the End of Cable.
Environmental						
Conducted EMI		CISPR22B / EN55022B Load floating or grounded via artificial hand				With 6 dB Margin Using Resistive Load and Earth Connected.
Line Surge Differential Mode (L1/L2)				1	kV	Differential Mode: 2 Ω
Line Surge Common Mode (L1/L2-PE)				6	kV	Ring Wave, Common Mode: 12 Ω.
ESD		±15 ±8			kV kV	Air Discharge Voltage and with No Degradation in Performance After Test. Contact Discharge Voltage with No Degradation in Performance After Test.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

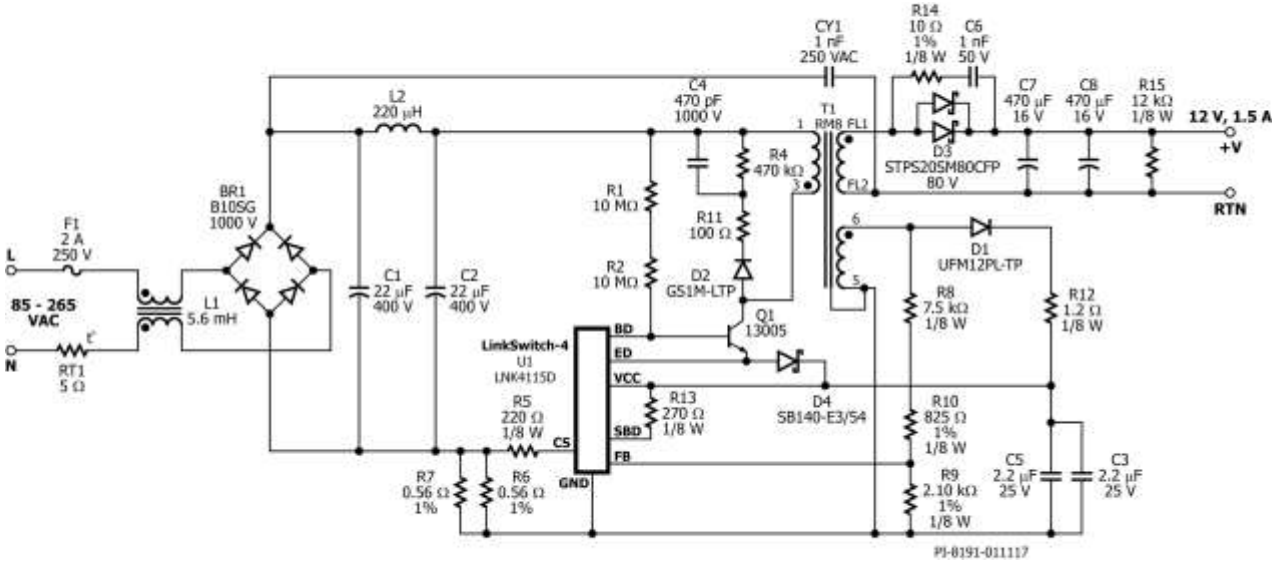

Figure 3 – Schematic.

4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 provides protection against catastrophic failure of components on the primary side.

An inrush-current limiting thermistor (RT1) protects bridge rectifier BR1 and limits inrush current.

Capacitor C1 and C2 provide filtering of the rectified AC input and together with inductor L2 to attenuate differential mode EMI. A Y capacitor (CY1) reduces common mode EMI.

4.2 Primary

Component U1 (LNK4115D) is the controller IC and driver for the main high-voltage switch, Q1, which is a very low-cost 700 V BJT.

A low-cost RCD clamp formed by D2, R11, R4 and C4 limits the peak drain voltage due to the effects of transformer leakage inductance.

The IC and BJT together are self-starting. Resistor R1 and R2 provide a very low current into the base of Q1. This current is amplified at the emitter. The emitter current flows into the EMITTER DRIVE (ED) pin which during start-up, charges up the VOLTAGE SUPPLY (VCC) pin capacitor. When the VCC pin voltage is already established, the IC will go from sleep to initialize mode. In this mode a single short switching pulse is periodically applied to Q1 so as to enable the FEEDBACK (FB) pin to sense the bulk capacitor voltage through the auxiliary winding and the combination of resistors R8, R10, and R9.

During normal operation, the VCC pin is powered by the auxiliary winding of the transformer. Output of the auxiliary winding is rectified by diode D1. Resistor R12 and capacitors C3 and C5 form a low pass filter that filters out any narrow voltage spikes.

Output voltage is indirectly sensed by the FB pin through the auxiliary winding voltage and sampled at the end of the secondary conduction time via voltage divider resistors R8, R10, and R9.

The primary current is sensed by the paralleled current sense resistors R6 and R7, through R5.

Output current regulation is achieved by sensing primary current and secondary conduction time.

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Resistor R13 sets the supplementary base drive magnitude. This is extra base current over the base drive period that ensures transistor Q1 remains in saturation.

4.3 Secondary

The secondary of the transformer is rectified by diode D3 and filtered by capacitors C7 and C8. Peak voltage stress of diode D3 is reduced by snubber components R14 and C6 which damp the high frequency ringing during switching transients. This also reduces radiated EMI.

Resistor R15 provides a small pre-load to reduce the output voltage rise at light load condition.

5 PCB Layout

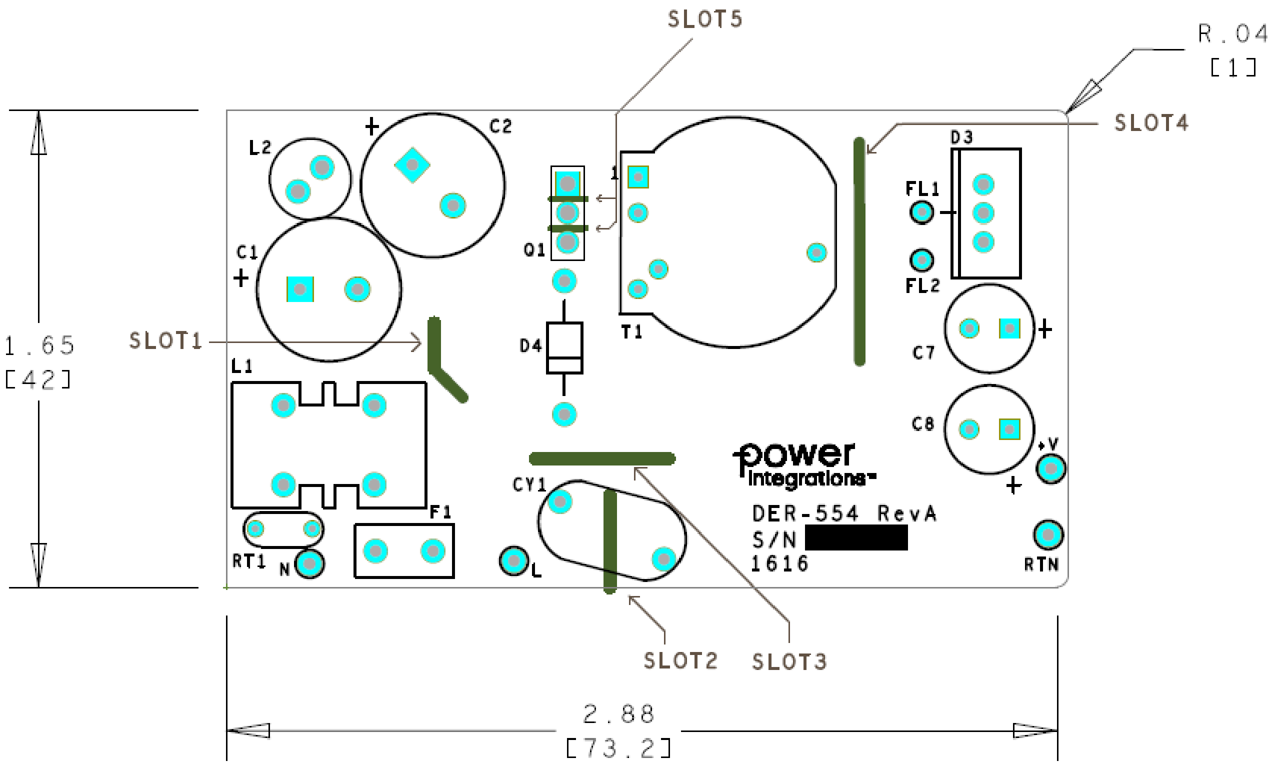

Figure 4 – Printed Circuit Layout, Top.

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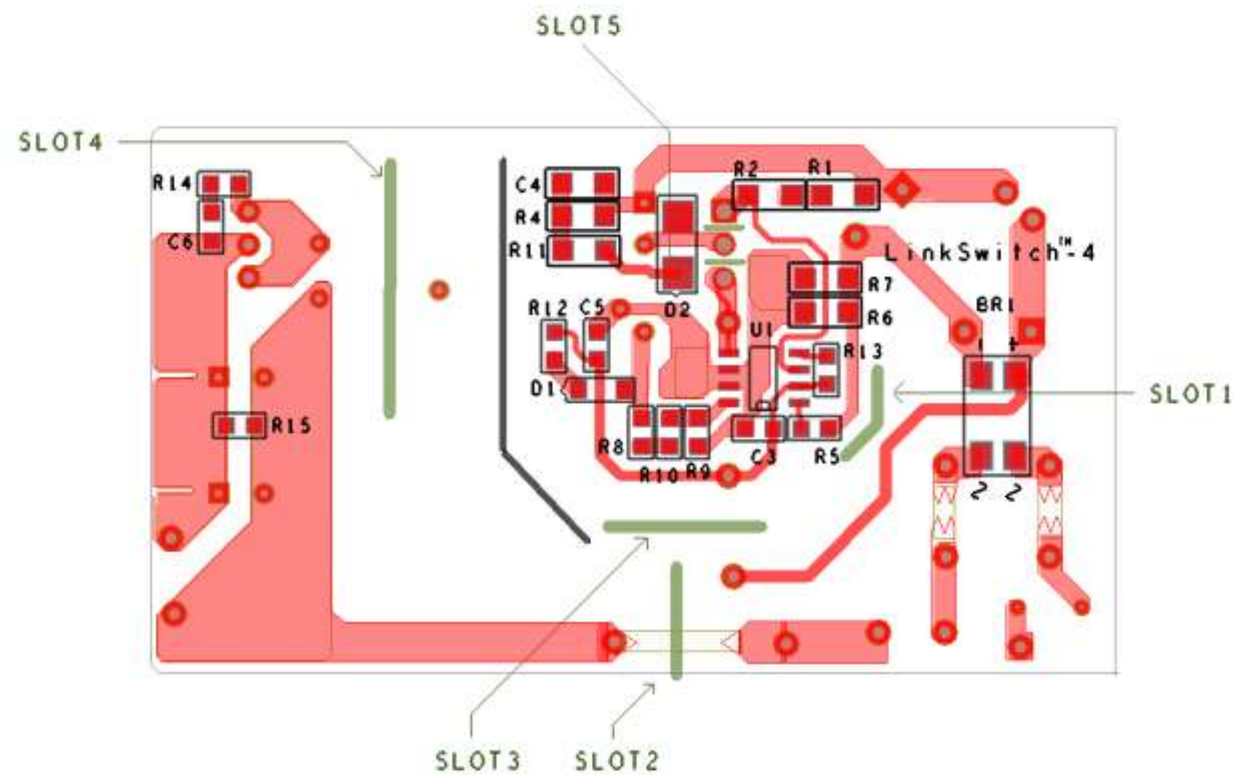

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	22 μF, 400 V, Electrolytic, (12.5 x 20)	UCS2G220MHD	Nichicon
3	1	C2	22 μF, 400 V, Electrolytic, (12.5 x 20)	UCS2G220MHD	Nichicon
4	1	C3	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
5	1	C4	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay-Vitramon
6	1	C5	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
7	1	C6	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
8	1	C7	470 μF, 16 V,Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
9	1	C8	470 μF, 16 V,Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
10	1	CY1	1 nF, Ceramic, Y1	440LD10-R	Vishay
11	1	D1	100 V, 1 A, Standard Recovery, SOD-123FL	UFM12PL-TP	Micro Commercial
12	1	D2	1000 V, 1 A, DO-214AC	GS1M-LTP	Micro Commercial
13	1	D3	DIODE, ARRAY, SCHOTTKY, 80V, TO220FP	STPS20SM80CFP	ST Micro
14	1	D4	40 V, 1 A, Schottky, DO-41	SB140-E3/54	Vishay
15	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
16	1	L1	CHOKE, COM MODE, 2 X 5.6MH, .6A	744862056	Wurth
17	1	L2	Inductor, Fixed, 220 μH 0.43 A 5.4 MHz, Radial Lead	22R224C	Murata
18	1	Q1	NPN, 450 V, 3.2A,TO126	APT13005SU-G1	Diodes, Inc.
19	1	R1	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
20	1	R2	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
21	1	R4	RES, 470 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic
22	1	R5	RES, 220 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ221V	Panasonic
23	1	R6	RES, SMD, 0.56 Ω, 1%, 1/4 W, 1206	ERJ-8RQFR56V	Panasonic
24	1	R7	RES, SMD, 0.56 Ω, 1%, 1/4 W, 1206	ERJ-8RQFR56V	Panasonic
25	1	R8	RES, 7.5 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ752V	Panasonic
26	1	R9	RES, 2.10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2101V	Panasonic
27	1	R10	RES, 825 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8250V	Panasonic
28	1	R11	RES, 100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ101V	Panasonic
29	1	R12	RES, 1.2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ1R2V	Panasonic
30	1	R13	RES, 270 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ271V	Panasonic
31	1	R14	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
32	1	R15	RES, 12 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ123V	Panasonic
33	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
34	1	T1	Bobbin, RM8, Vertical, 8 pins (6 x 2)	RM8(SX-814)	ShenZhen SanXiangYuan
35	1	U1	LinkSwitch-4, 18 W, SO-8	LNK4115D	Power Integrations

Test Points and Fly Leads:

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
36	1	FL1	Flying Lead, Hole size 30 mils	N/A	N/A
37	1	FL2	Flying Lead, Hole size 30 mils	N/A	N/A
38	1	+V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
39	1	RTN	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
40	1	L	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
41	1	N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone

NOTE: Test points and fly leads are not included in the total parts count.

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7 Transformer Specification

7.1 Electrical Diagram

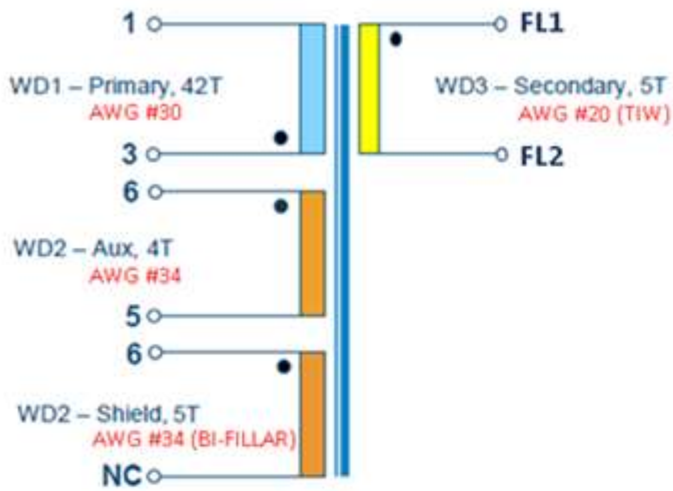

Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Primary Inductance	Pins 1 and 3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	900 µH ±5%
Primary Leakage Inductance	Pins 1 and 3, with pins FL1-FL2 and pins 5-6 shorted, then measured at 100 kHz, 0.4 V_{RMS}.	25 uH

7.3 Material List

Item	Description
[1]	Core:HP95 – RM8/6 HONGKANG MAGNETIC ELECTRONIC CO., LTD .
[2]	Bobbin: RM8, Vertical, 8 pins (6 x 2). PI#: 25-01081-00. ShenZhen SanXiangYuan Elect Tech Co. Ltd.
[3]	Magnet Wire: #30 AWG.
[4]	Magnet Wire: #34 AWG.
[5]	Triple Insulated Wire: #20 AWG (TIW).
[6]	Tape: Polyester Film, 3M 1350-1, 9 mm Wide.
[7]	Bus Wire: #24 AWG, Belden Electronics Div; or Equivalent.
[8]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

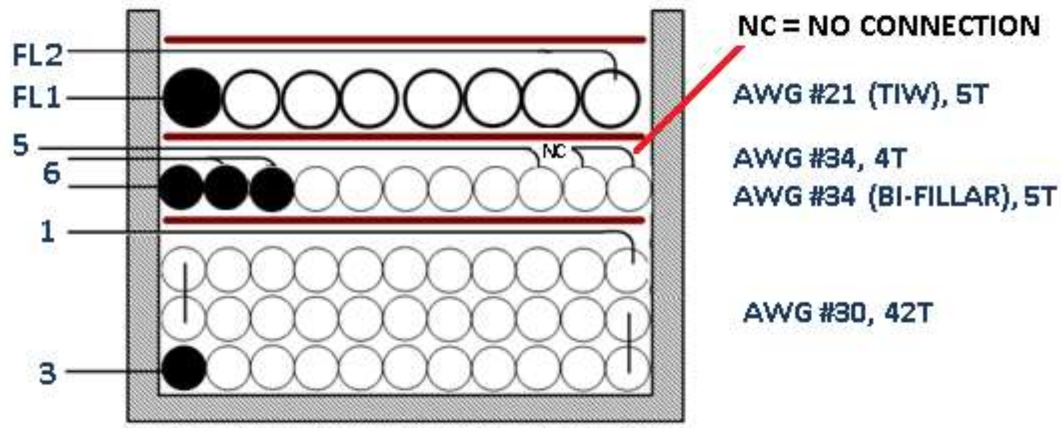

Figure 7 – Transformer Build Diagram.

7.5 Transformer Instructions

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
Primary Winding	Start at pin 3. Wind 42 turns of item [3] in approximately 3 layers. Finish at pin 1.
Insulation	Use 1 layer of item [6] for insulation.
Bias Winding and Shield Winding	Use 3 wires (trifillar) of item [4], start at pin 6 and wind 4 turns from left to right. After the 4th turn bring 1 wire to the left and terminate at pin 5 for bias winding. Continue winding the remaining bifilar wire with 1 more turn and leave it with no-connection for shield winding.
Insulation	Use 1 layer of item [6] for insulation.
Secondary Winding	Mark start as FL1. Wind 5 turns of item [5] in approximately 2 layers. Mark finish as FL2.
Insulation	Use 2 layers of item [6] to secure the windings.
Final Assembly	Gap core halves to achieve 900 μH inductance. Wrap core halves with bus wire item [7] and tape item [6] (see illustration below). Finally varnish the transformer with item [8] and cut bobbin pins 2, 4, and 8.

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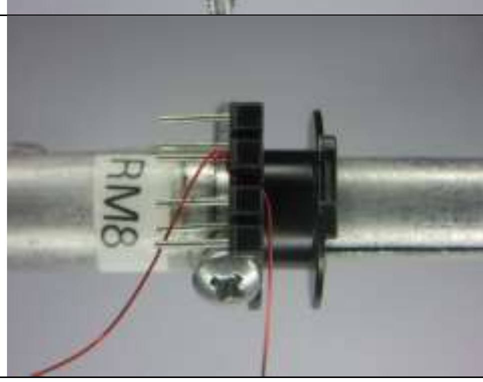
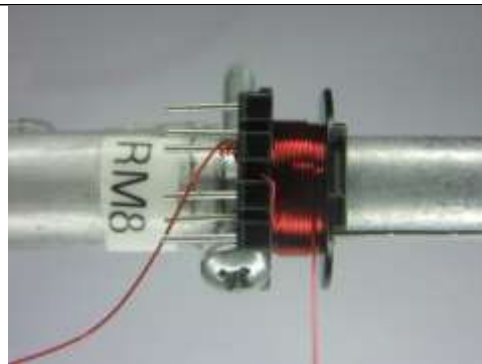
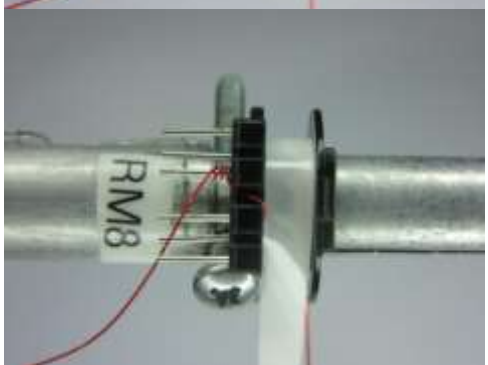
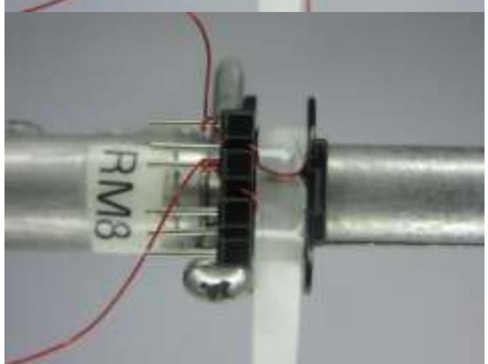
7.6 Transformer Construction Illustrations

Bobbin Preparation	 Take note of the bobbin pin configuration.  	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
Primary Winding		Start at pin 3.

Primary Winding		Wind 42 turns of item [3] in approximately 3 layers. Finish at pin 1.
Insulation		Use 1 layer of item [6] for insulation.

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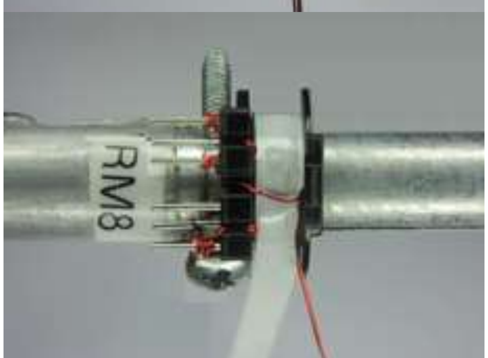
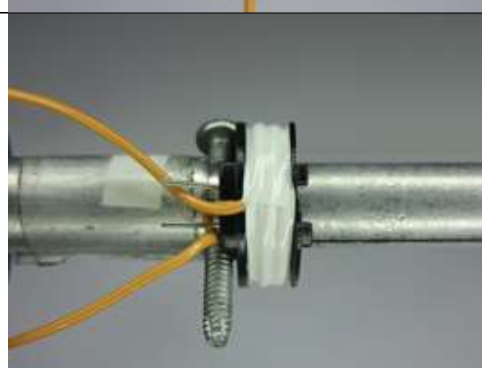
Bias Winding and Shield Winding		Use 3 wires (trifillar) of item [4], start at pin 6 and wind 4 turns from left to right.
		
		After the 4th turn bring 1 wire to the left and terminate at pin 5 for bias winding. Continue winding the remaining bifilar wire with 1 more turn and leave it with no-connection for shield winding.
Insulation		Use 1 layer of item [7] for insulation.

Secondary Winding		Mark start as FL1.
		Wind 5 turns of item [5] in approximately 2 layers. Mark finish as FL2.
Insulation		Use 2 layers of item [6] to secure the windings.
Final Assembly		Gap core halves to achieve 900µH inductance.

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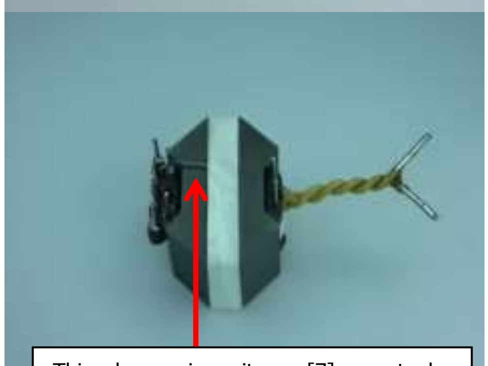
Final Assembly	  	Wrap core halves with bus wire item [7] and tape item [6] (see illustration).
Final Assembly		Finally varnish the transformer with item [8] and cut bobbin pins 2, 4, and 8.

		Finished transformer assembly.

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8 Transformer Design Spreadsheet

ACDC_LinkSwitch-4_071615; Rev.2.0; Copyright Power Integrations 2015	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-4_071615: LinkSwitch-4 Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85		85	Volts	Minimum AC Input Voltage
VACMAX	265		265	Volts	Maximum AC Input Voltage
fL	47		47	Hertz	AC Mains Frequency
VO	12.00		12.00	Volts	Output Voltage at the end of the cable
VO_PCB			12.36	Volts	Output Voltage at PCB. Changes with cable compensation selection
VD			0.40	Volts	Output Winding Diode Forward Voltage Drop
IO	1.50		1.50	Amps	Full load rated current. Used for all waveshape related calculations.
ICC	1.65		1.65	Amps	CC setpoint. Must be >= IO+7%. Affects Rcs.
PO			18.54	Watts	Rated output power including cable drop compensation. Calculated from IO
n	0.86		0.86	%/100	Efficiency Estimate
CIN	44.0		44.0	uFarads	Total input bulk Capacitance
ENTER LINKSWTCH-4 VARIABLES					
LinkSwitch-4	**LNK41X5D**				Select LNK-4
Cable drop compensation option	**3%**		3%		Select level of cable drop compensation
DEVICE		*Info*	LNK4115D		Output Power is greater than datasheet PO for this part number. Please verify performance on bench or select a bigger part
FSW			65000	Hertz	LinkSwitch-4 typical switching frequency
ILIM_MAX			1.10	A	Maximum emitter pin sink current
Transistor					
PART_NUMBER			TS13005		Example transistor for the current application
HFE_STARTUP			12		Minimum DC current gain at no load and startup. Affects start-up delay
HFE			25		Minimum DC current gain for load transient
VSWMAX			700	Volts	Switch Breakdown voltage
V_CGND_ON			3.0	Volts	BJT + LNK-4 on-state Collector to ground Voltage (3V if no better information available)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Custom**		RM8		Core Type
Custom Core (Optional)	**RM8**				If Custom core is used - Enter Part number here
Bobbin	**RM*-SX-814**	RM*-SX-814		P/N:	
AE	0.61		0.61	cm^2	Core Effective Cross Sectional Area
LE	3.18		3.18	cm	Core Effective Path Length
AL	2800		2800	nH/T^2	Ungapped Core Effective Inductance
BW	5.80		5.80	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
BWE			5.8	mm	Effective Bobbin Width
MAIN OPTIMIZATION INPUTS					
Turns and ratio					
VOR	107.00		107.00	Volts	Reflected Output Voltage. Use Goal Seek to get VCRMV to desired value.
NS	5		5		Number of Secondary Turns. Adjusting up or down along with VOR may improve efficiency.
NP			42		Primary Winding Number of Turns
DC INPUT VOLTAGE PARAMETERS					
VCRMV		Warning	115	Volts	Value > VMIN+15 risks LF ripple. Adjust VOR

					or NS to lower this
VMIN			81.7	Volts	Bulk cap "trough" voltage at VACMIN. Leave blank to calculate from capacitance and load.
VMAX			375	Volts	Maximum DC Input Voltage
VBROWN			63	Volts	Bulk voltage it loses regulation
PRIMARY WAVEFORM PARAMETERS					
F_RES			400	kHz	Anticipated resonant frequency on the primary side (180<Ftrf<1200)
KCRMV		*Info*	0.65		KP below 0.95 may mean early CRMV operation with nominal L and IP.
IRMS			0.41	Amps	Primary RMS Current (calculated at load=IO, VMIN)
IP			0.97	Amps	Peak Primary Current (calculated at load=IO, VMIN)
IOCP			1.13	Amps	Pulse by pulse current limit. Appears during large load transients and brownout operation.
IAVG			0.26	Amps	Average Primary Current (calculated at load=IO, VMIN)
IP_CRMV			0.82	Amps	Ipeak when Vin=Vcrm
F_CRMV			65000	Hz	Fsw when Vin=Vcrm
FVMIN			49230	Hz	Fsw at VMIN. If < 65kHz, is in frequency reduction mode
VCS_VMIN			0.308	Volts	Vcs_pk at VMIN and load = IO
RCS			0.317	Ohm	Calculated RCS value. Changes with Icc and VOR
SECONDARY WAVEFORM PARAMETERS					
ISP			8.14	Amps	Peak Secondary Current @ VMIN
ISRMS			2.79	Amps	Secondary RMS Current @ VMIN
IRIPPLE			2.35	Amps	Output Capacitor RMS Ripple Current @ VMIN
TRANSFORMER CORE PARAMETERS					
BP			4080	Gauss	Peak Flux Density @ max IOCP & max LP. 3900 Gauss. Lower BP may reduce efficiency
LP			901	uHenries	Nominal Primary Inductance
LP Tolerance			5		Tolerance of Primary Inductance. Tighter tolerance allows better average efficiency across production.
ALG			511	nH/T^2	Gapped Core Effective Inductance
BM			3415	Gauss	Maximum Flux Density at PO, VMIN, LP (BM<3000)
BAC			1707	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1165		Relative Permeability of Ungapped Core
LG			0.12	mm	Gap Length (Lg > 0.1 mm)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
L	3.0		3.0		Number of Primary Layers
OD			0.37	mm	Maximum Primary Wire Diameter including insulation to fill layers
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.31	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
Primary Current Density (J)			3.75	Amps/mm^2	!!! Info. Primary current density is low. Can increase Primary current density. Reduce primary layers, or use smaller core
Bias/Feedback Winding					
NB			4	Turns	Suggested number of turns for the bias / feedback winding
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
VB_NOLOAD	8.00		8.00	Volts	Desired Minimum Bias voltage at no load
PB_NOLOAD			5.46	mW	Bias winding power consumption estimate at

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					no load
VB_NOLOAD_MEASURED			9.22	Volts	Measured Bias voltage at no load
TRANSFORMER SECONDARY DESIGN PARAMETERS					
LS			1.0		Number of Secondary Layers
FilarS			1		# of paralleled secondary wires
ODS			1.10	mm	Maximum Secondary Wire Diameter including insulation to fill layers
INSS			0.20	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIAS			0.90	mm	Bare conductor diameter
AWGS			20	AWG	Secondary Wire Gauge (Rounded to next smaller standard AWG value)
Secondary Current Density (J)			4.37	Amps/mm^2	Winding Current density (3.8 < J < 10)
VOLTAGE STRESS PARAMETERS					
SWITCH_DERATING			0.10	%/100	Desired derating factor for switch
VCOLLECTOR			619	Volts	Maximum Collector Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			66	Volts	Output Rectifier Maximum Peak Inverse Voltage includes spike
PIVB			59	Volts	Bias Rectifier Maximum Peak Inverse Voltage includes spike
Additional Parameters					
Zero-load Collector peak current					
VCS_MIN	**56**		56	mV	Drives peak current at zero load. Affects zero load frequency and consumption, and 0-100% load step
RCS2			100	Ohm	Resistance for setting VCS_MIN
Bias Capacitor					
CBIAS	2.00		2.00	uF	Auxiliary capacitor. Default value assumes 100 mV of ripple on bias winding.
DELTAV_BIAS			238	mV	Voltage ripple on VCC capacitor at zero-load (should be between 0.05V and 1.6V
Output Capacitor					
LOAD_TYPE	**CC Load**		CC Load		Select load type for startup testing. This will help estimate the maximum output capacitance that will allow proper startup under any normal operating conditions
ICC_STARTUP			1.13	A	CC load at startup
R_LOAD		*Info*	8.24	Ohm	Not used for CC startup calculation
COUT_ADVISED			169	uF	Maximum Cout to guarantee proper startup and stability
COUT_FINAL		*Warning*	940	uF	Total output capacitance on the secondary of the power supply
Load step and undershoot					
RCABLE_EST			0.240	Ohm	Estimated charger cable resistance
I_LOADSTEP			1.50	A	Required maximum current load step from zero load
V_UNDERSHOOT			8.88	V	Accepted undershoot during maximum load step
FSW_UNDERSHOOT		*Info*	578	Hz	Fsw_noload may be lower than the minimum frequency required to fulfill the undershoot specification. This test does not include standard 47uF capacitance at end of cable. Verify performance or try to increase the pre load, increase Cout, or lower VCSmin
Dummy load and no load					
R_PRELOAD	33000		33000	Ohm	Pre load resistor (1%). Affects FSW_NOLOAD, zero load consumption, and 0-100% load step dip
P_PRELOAD			4.6	mW	Preload resistor power consumption at no load

FSW_NOLOAD			1262	Hz	Estimated switching frequency at no load. Adjust with VCS_MIN and R_PRELOAD
Startup					
STARTUP_TIME			1.00	second	Desired startup delay time
R_STARTUP			25.50	MOhm	Startup resistor (default calculation assumes a standard resistor for desired startup)
STARTUP_TIME_FINAL			1.02	second	Final startup time assuming resistor value Rstartup
Feedback Resistors					
V_UV+			87.8	V	DC voltage at which power supply will start up
RFB1			7870	Ohm	Initial estimate for top feedback resistor (std value, use 1% tolerance)
RFB2			1910	Ohm	Initial estimate for bottom feedback resistor (std value, use 1% tolerance)
NO LOAD POWER ESTIMATOR					
EFF_NOLOAD			0.60	%/100	Assumed efficiency at no load (0.6 if no better data available)
VAC_INPUT			230	Volts	AC input voltage for no load power estimation
PB_NOLOAD			5.5	mW	Bias winding power consumption estimate at no load
P_PRELOAD			4.6	mW	Preload resistor power consumption at no load
P_STARTUPRES			4.1	mW	Energy dissipated by the startup resistor
PSW			9.1	mW	Power losses of the switch and clamp
P_NOLOAD_TOTAL			30	mW	Estimated no load power consumption. Affected by Vcs_min

NOTE: Ripple warning on the spreadsheet was verified in actual operation and is less than the maximum 150mVpk-pk requirement.

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9 Performance Data

The following data below shows the performance of LNK4115D with respect to efficiency, output regulation, constant voltage and constant current characteristic, no load input power, thermal performance, load transient, brown-in/brown out, short circuit, output ripple, conducted EMI, surge, and ESD test. In addition, pertinent waveforms were also captured to further verify the LNK4115D performance.

All measurements at the end of the cable were performed using a 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

Figure 8 – Unit Under Test with the Equivalent 100 mΩ Cable.

9.1 Efficiency

The following data/result is the efficiency data of the LNK4115D measured at the main output terminal and at the end of the cable. Efficiency was taken at different line condition (85 VAC, 115 VAC, 230 VAC, 265 VAC), maximum load, as well as different load percentage. The average efficiency was also taken at 25%, 50%, 75%, and 100% loading condition. All measurements were performed at room ambient temperature.

9.2 Efficiency at Different Line Condition – Main Output Terminal, Full Load

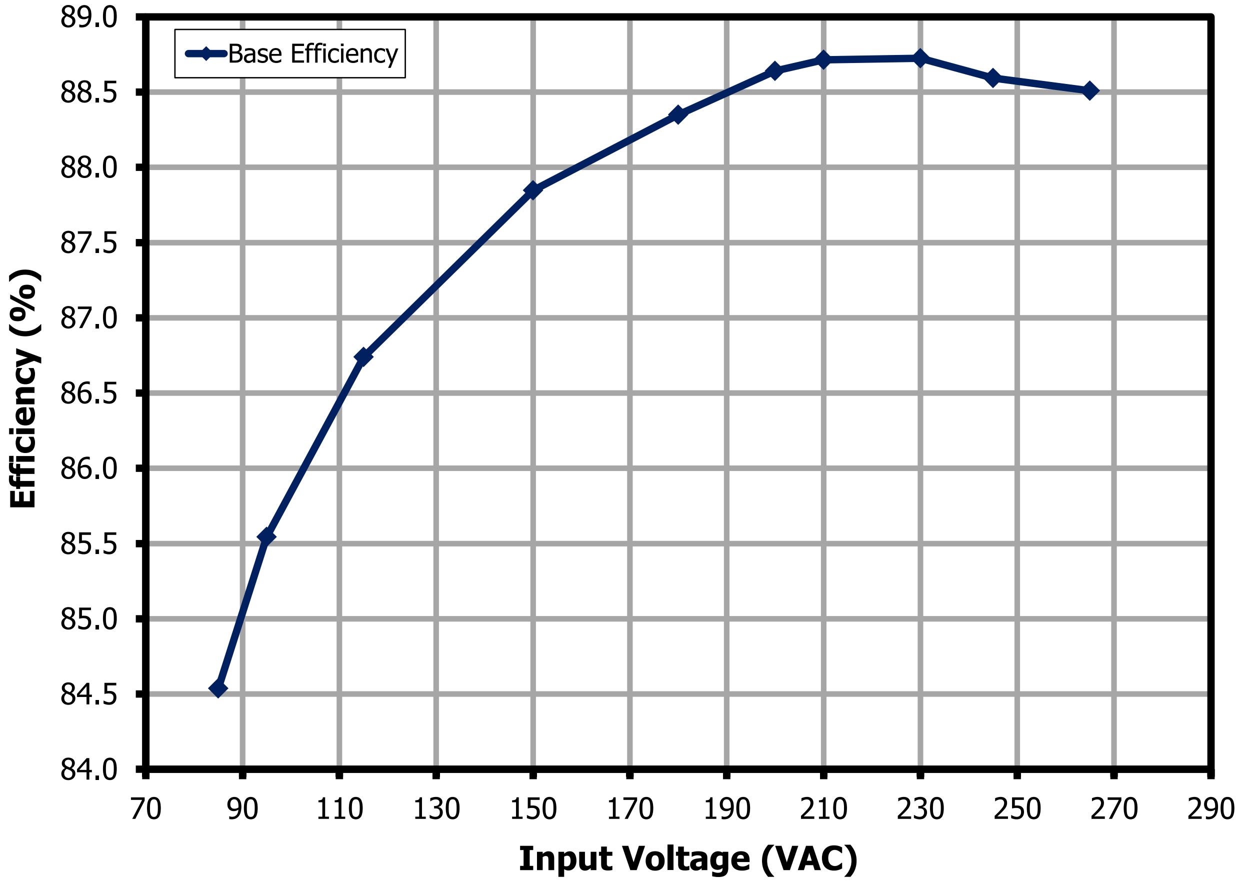

Figure 9 – Efficiency vs Line Voltage Graph, Main Output Terminal, Full Load, Room Temperature.

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Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
85	60	84.98	0.42	21.95	0.612	12.37	1.50	18.56	84.54
95	60	94.91	0.39	21.70	0.591	12.38	1.50	18.56	85.54
115	60	114.97	0.34	21.41	0.554	12.38	1.50	18.57	86.74
150	60	150.03	0.28	21.14	0.504	12.38	1.50	18.57	87.85
180	60	180.03	0.25	21.02	0.475	12.38	1.50	18.57	88.35
200	60	200.08	0.23	20.96	0.459	12.39	1.50	18.58	88.64
210	60	210.03	0.22	20.95	0.453	12.40	1.50	18.59	88.71
230	60	230.07	0.21	20.94	0.440	12.39	1.50	18.58	88.72
245	60	245.07	0.20	20.98	0.433	12.40	1.50	18.59	88.59
265	60	265.14	0.19	21.00	0.423	12.40	1.50	18.59	88.51

Figure 10 – Efficiency vs Line Voltage Data Table, Main Output Terminal, Full Load, Room Temperature.

9.3 Efficiency at Different Line Condition – End of Cable, Full Load

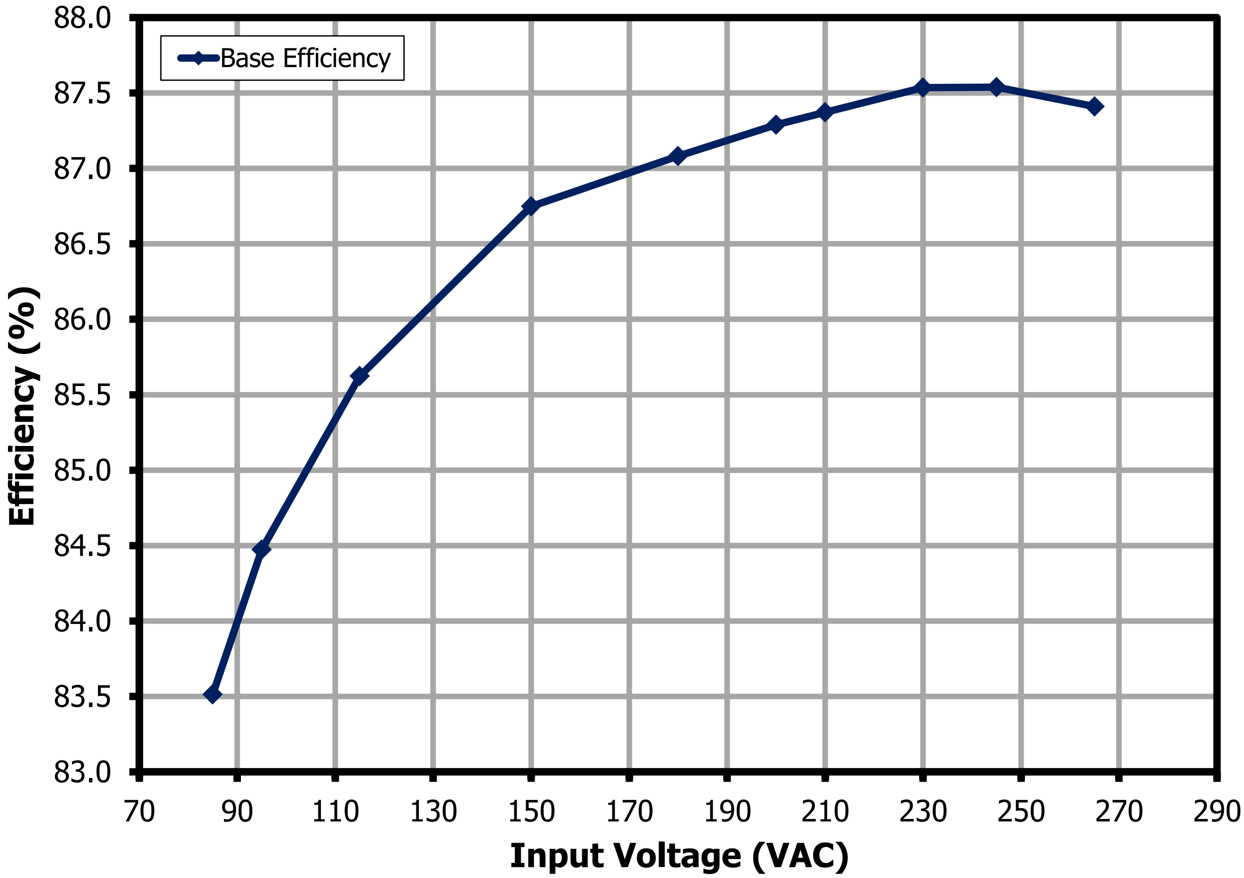

Figure 11 – Efficiency vs Line Voltage Graph, End of Cable, Full Load, Room Temperature.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

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Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
85	60	84.98	0.42	21.94	0.61	12.22	1.50	18.32	83.51
95	60	94.91	0.39	21.70	0.59	12.22	1.50	18.33	84.47
115	60	114.97	0.34	21.41	0.55	12.22	1.50	18.33	85.62
150	60	150.03	0.28	21.14	0.50	12.23	1.50	18.34	86.75
180	60	180.02	0.25	21.05	0.48	12.22	1.50	18.33	87.08
200	60	200.08	0.23	21.00	0.46	12.22	1.50	18.33	87.29
210	60	210.03	0.22	20.98	0.45	12.22	1.50	18.33	87.37
230	60	230.07	0.21	20.95	0.44	12.23	1.50	18.34	87.54
245	60	245.07	0.20	20.94	0.43	12.22	1.50	18.33	87.54
265	60	265.14	0.19	20.98	0.42	12.23	1.50	18.34	87.41

Figure 12 – Efficiency vs Line Voltage Data Table, End of Cable, Full Load, Room Temperature.

9.4 Efficiency at Different Line Condition – Summary of Graphs, Full Load

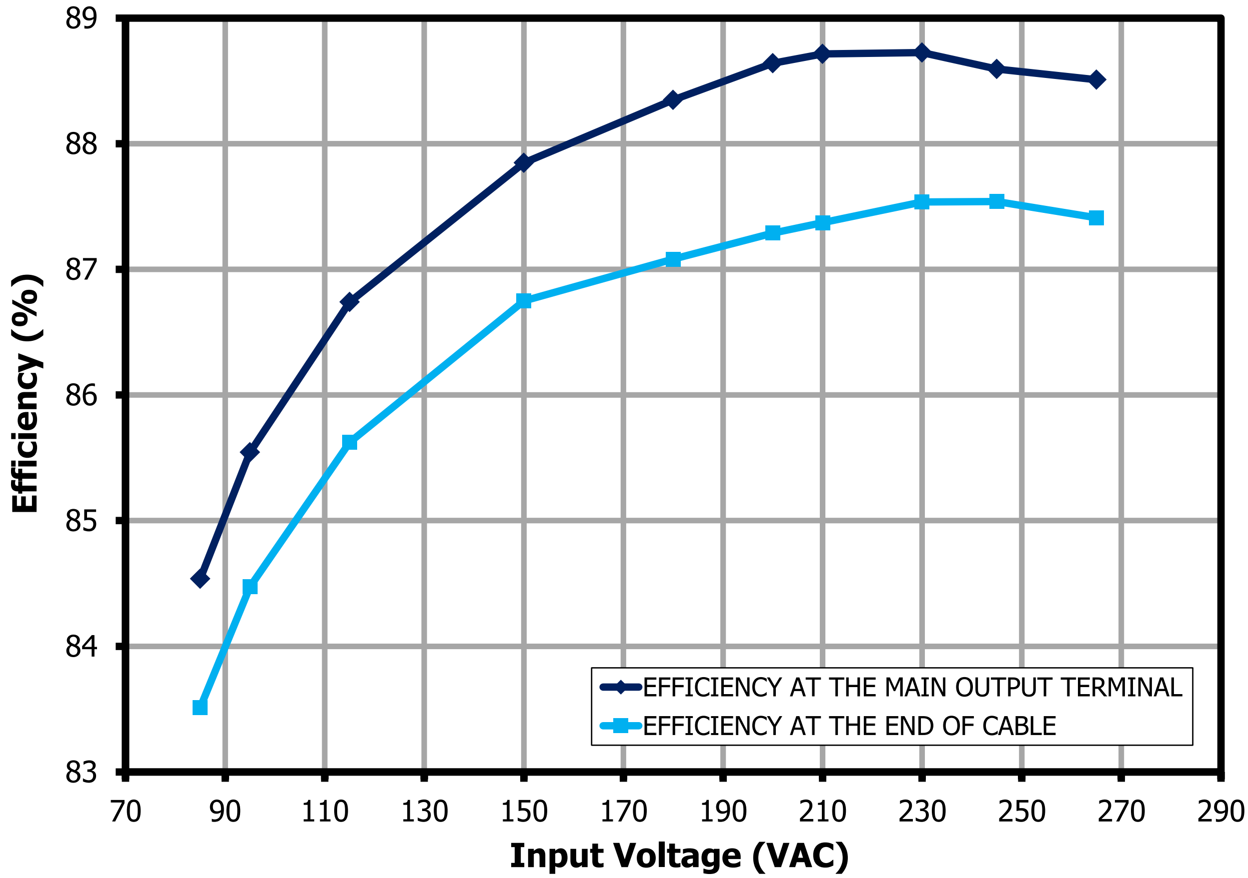

Figure 13 – Efficiency vs Line Voltage Summary of Graphs, Full Load, Room Temperature.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

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9.5 Average Efficiency Requirements

Test	Average	Average	Average	Average	10% Load	10% Load
Model	>6 V Voltage	>6 V Voltage	>6 V Voltage	>6 V Voltage	>6 V Voltage	>6 V Voltage
Effective	2014	2016	2014	2016	2014	2016
Regulation	**Energy Star 2**	**New IESA2007**	**CoC v5 Tier 1**	**CoC v5 Tier 2**	**CoC v5 Tier 1**	**CoC v5 Tier 2**
Required Efficiency	**81.1%**	**85%**	**82.7%**	**85.5%**	**72.7%**	**75.5%**

Figure 14 – Average Efficiency Requirement Table.

9.5.1 Average Efficiency – Main Output Terminal

9.5.1.1 Average Efficiency at 115 VAC

Load Setting		Input Measurement				Load Measurement			Efficiency (%)	Average Efficiency (%)
Load (%)	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)		
100	1.5	114.97	0.33	21.49	0.568	12.36	1.50	18.54	86.27	**87.04**
75	1.125	114.98	0.26	15.91	0.535	12.32	1.12	13.85	87.04	
50	0.75	115.00	0.18	10.49	0.504	12.24	0.75	9.17	87.46	
25	0.375	115.01	0.10	5.21	0.456	12.16	0.37	4.55	87.39	
10	0.150	115.02	0.05	2.09	0.396	12.12	0.15	1.81	**86.71**	

Figure 15 – Average Efficiency at 115 VAC, Main Output Terminal.

9.5.1.2 Average Efficiency at 230 VAC

Load Setting		Input Measurement				Load Measurement			Efficiency (%)	Average Efficiency (%)
Load (%)	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)		
100%	1.5	230.07	0.20	20.98	0.455	12.36	1.50	18.54	88.36	**88.29**
75%	1.125	230.08	0.16	15.61	0.428	12.32	1.12	13.85	88.72	
50%	0.75	230.09	0.11	10.37	0.404	12.24	0.75	9.17	88.47	
25%	0.375	230.09	0.06	5.20	0.367	12.17	0.37	4.56	87.60	
10%	0.150	230.10	0.03	2.13	0.322	12.12	0.15	1.81	**85.05**	

Figure 16 – Average Efficiency at 230 VAC, Main Output Terminal.

9.5.2 Average Efficiency – End of Cable

NOTE: A 1 meter, #22 AWG twisted pair of wire (100 mΩ in total resistance) was put in series with the positive and negative rail of the main output voltage.

9.5.2.1 Average Efficiency at 115 VAC

Load Setting		Input Measurement				Load Measurement			Efficiency (%)	Average Efficiency (%)
Load (%)	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)		
100	1.5	114.98	0.33	21.52	0.570	12.19	1.50	18.28	84.95	**86.26**
75	1.125	114.99	0.26	15.91	0.535	12.19	1.12	13.70	86.13	
50	0.75	115.00	0.18	10.51	0.504	12.16	0.75	9.11	86.68	
25	0.375	115.02	0.10	5.20	0.455	12.12	0.37	4.54	87.29	
10	0.150	115.02	0.05	2.11	0.399	12.10	0.15	1.81	**85.74**	

Figure 17 – Average Efficiency at 115 VAC, End of Cable.

9.5.2.2 Average Efficiency at 230 VAC

Load Setting		Input Measurement				Load Measurement			Efficiency (%)	Average Efficiency (%)
Load (%)	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)		
100	1.5	230.07	0.20	20.97	0.455	12.19	1.50	18.28	87.18	**87.54**
75	1.125	230.08	0.16	15.60	0.428	12.19	1.12	13.70	87.84	
50	0.75	230.08	0.11	10.39	0.406	12.16	0.75	9.11	87.67	
25	0.375	230.09	0.06	5.19	0.366	12.12	0.37	4.54	87.46	
10	0.150	230.10	0.03	2.15	0.324	12.10	0.15	1.81	**84.14**	

Figure 18 – Average Efficiency at 230 VAC, End of Cable.

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10 Output Voltage Regulation

NOTE: A 1 meter, #22 A twisted pair of wire (100 mΩ in total resistance) was put in series with the positive and negative rail of the main output voltage to simulate the cable drop. The regulation was then measured at the end of the series cable with the LNK4115D providing cable compensation especially at heavy load.

10.1 Output Voltage Regulation at Different Line Condition – End of Cable, Full Load

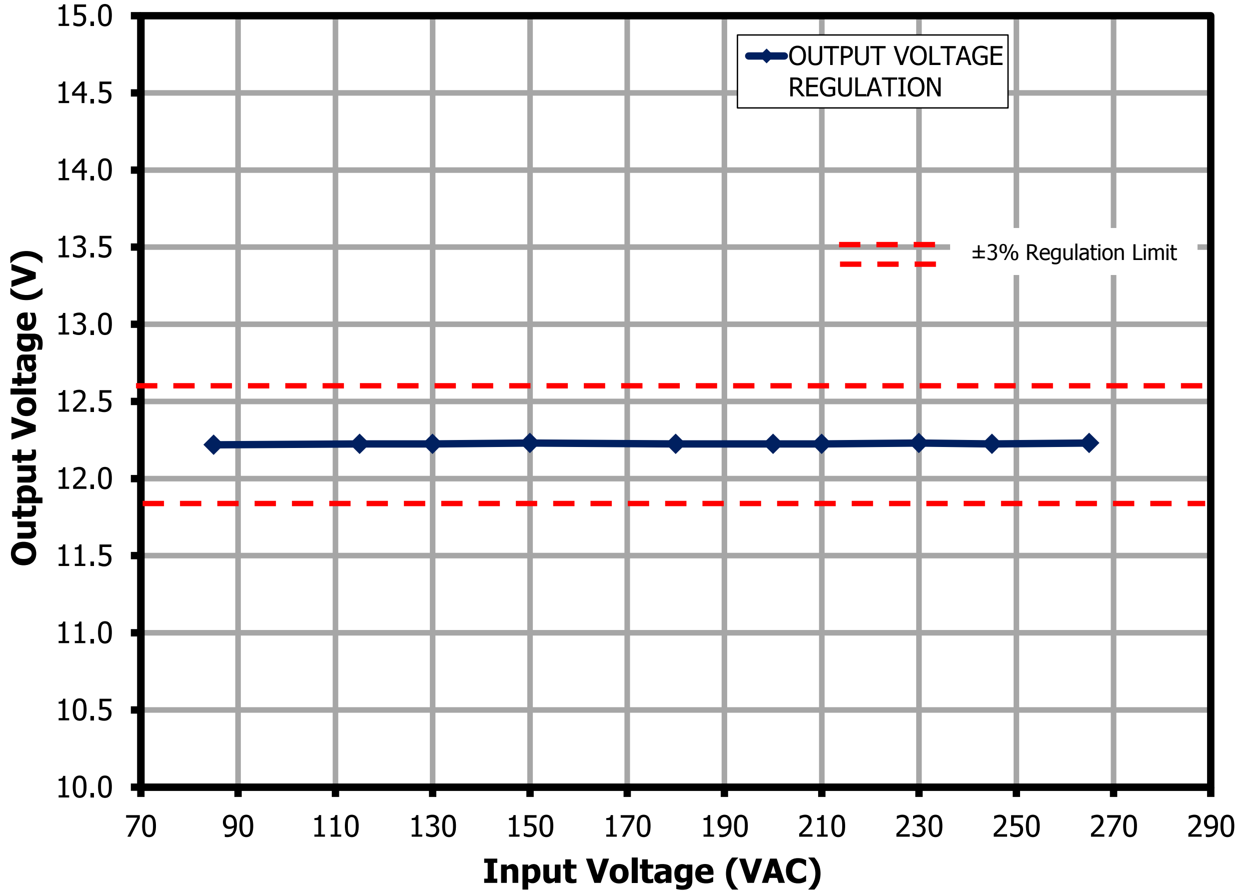

Figure 19 – Output Voltage Regulation at Different Line Condition, End of Cable, Full Load.

Input		Input Measurement				Load Measurement		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
85	60	84.98	0.42	21.94	0.611	12.22	1.50	18.32
115	60	94.91	0.39	21.70	0.590	12.22	1.50	18.33
130	60	114.97	0.34	21.41	0.553	12.22	1.50	18.33
150	60	150.03	0.28	21.14	0.504	12.23	1.50	18.34
180	60	180.02	0.25	21.05	0.475	12.22	1.50	18.33
200	60	200.08	0.23	21.00	0.460	12.22	1.50	18.33
210	60	210.03	0.22	20.98	0.454	12.22	1.50	18.33
230	60	230.07	0.21	20.95	0.440	12.23	1.50	18.34
245	60	245.07	0.20	20.94	0.432	12.22	1.50	18.33
265	60	265.14	0.19	20.98	0.422	12.23	1.50	18.34

Figure 20 – Output Voltage Regulation at Different Line Condition Data Table, End of Cable, Full Load.

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10.2 Output Voltage Regulation at Different Load and Line Condition – End of Cable

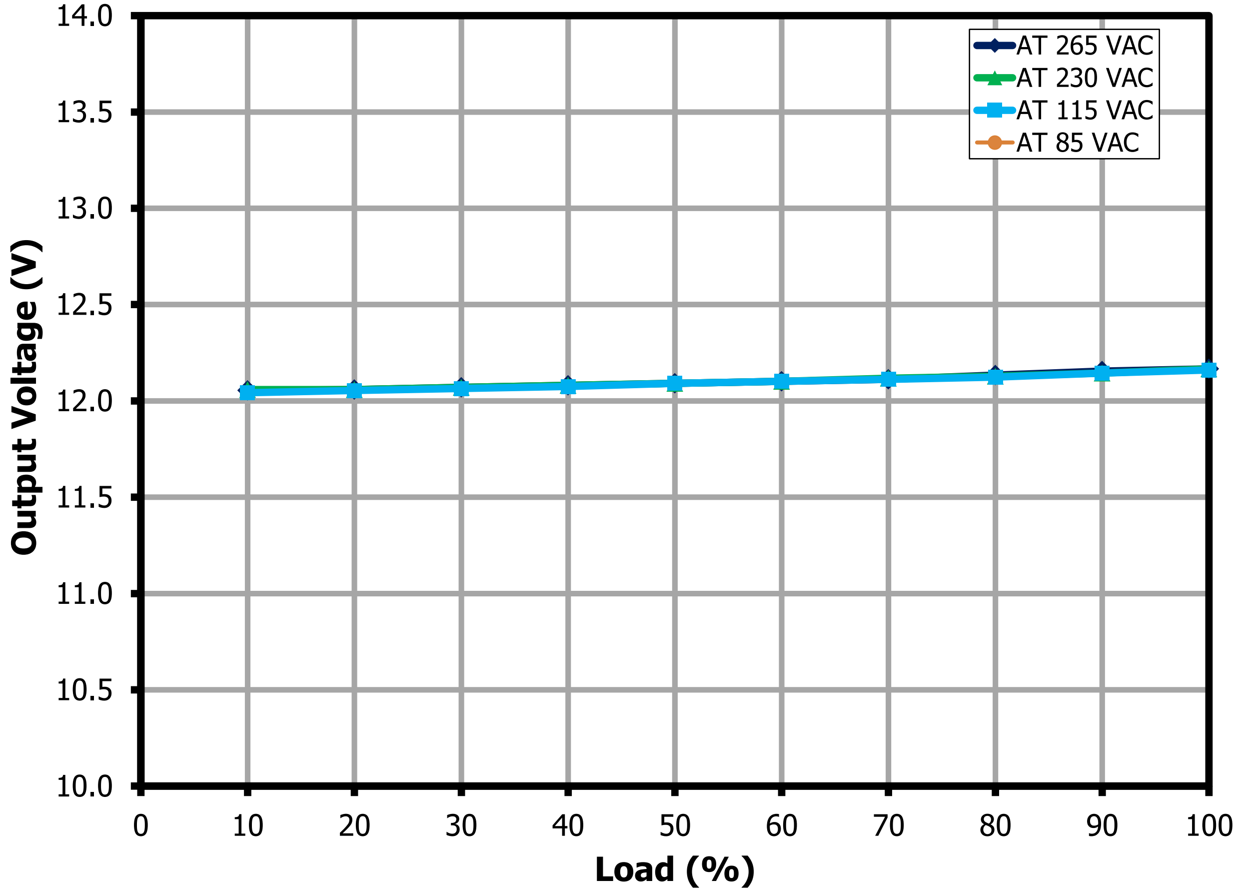

Figure 21 – Output Voltage Regulation at Different Load Condition, End of Cable.

	AT 85 VAC		AT 115 VAC		AT 230 VAC		AT 265 VAC	
Load Percentage (%)	**V (V_{DC})**	**I (A_{DC})**	**V (V_{DC})**	**I (A_{DC})**	**V (V_{DC})**	**I (A_{DC})**	**V (V_{DC})**	**I (A_{DC})**
10	12.06	0.15	12.04	0.15	12.06	0.15	12.05	0.15
20	12.07	0.30	12.05	0.30	12.06	0.30	12.06	0.30
30	12.07	0.45	12.06	0.45	12.07	0.45	12.07	0.45
40	12.09	0.60	12.08	0.60	12.08	0.60	12.08	0.60
50	12.10	0.75	12.09	0.75	12.09	0.75	12.09	0.75
60	12.11	0.90	12.10	0.90	12.10	0.90	12.10	0.90
70	12.12	1.05	12.11	1.05	12.12	1.05	12.11	1.05
80	12.13	1.20	12.12	1.20	12.13	1.20	12.13	1.20
90	12.14	1.35	12.14	1.35	12.14	1.35	12.16	1.35
100	12.17	1.50	12.16	1.50	12.17	1.50	12.17	1.50

Figure 22 – Output Voltage Regulation at Different Load and Line Condition Data Table, End of Cable.

11 Constant Voltage and Constant Current Charactertistic (CVCC) – End of Cable

11.1 At 85 VAC – End of Cable

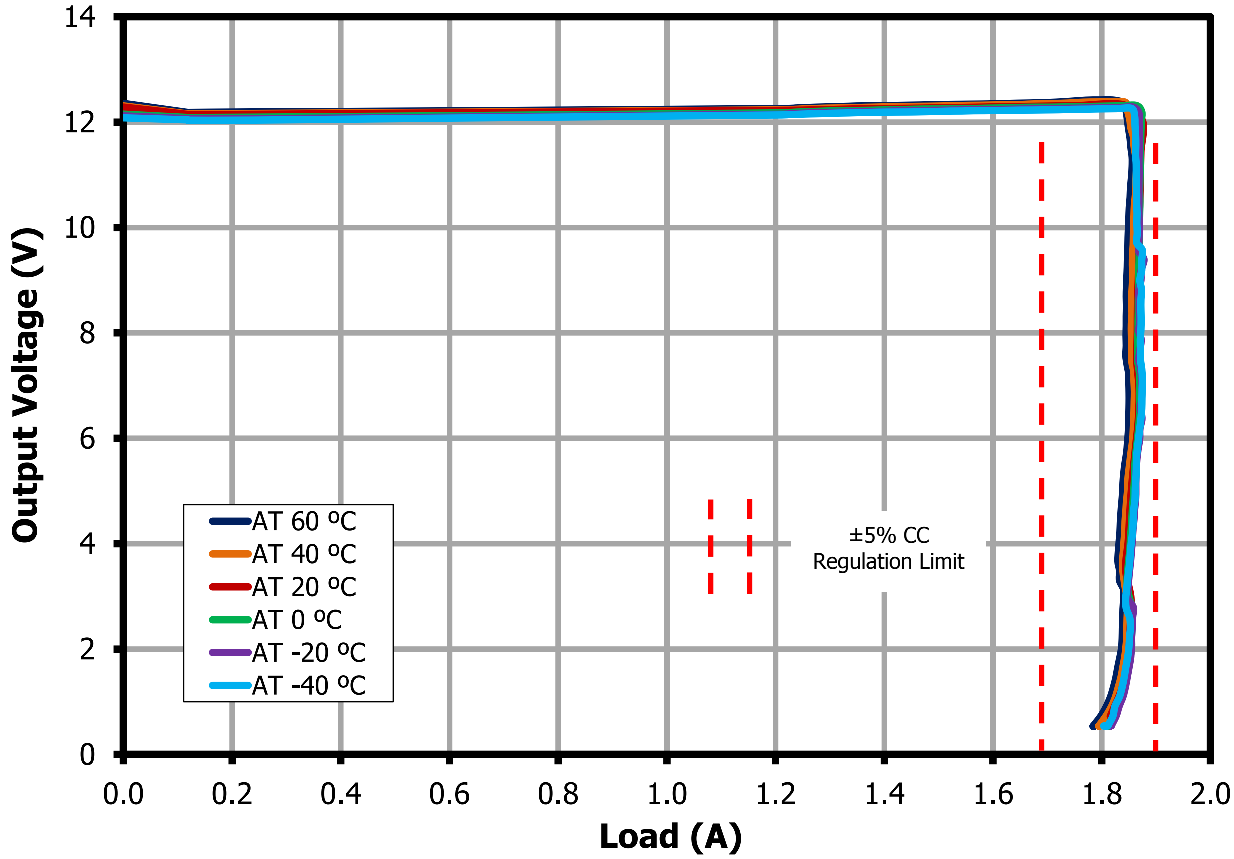

Figure 23 – CVCC Graph at 85 VAC, End of Cable.

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11.2 At 115 VAC – End of Cable

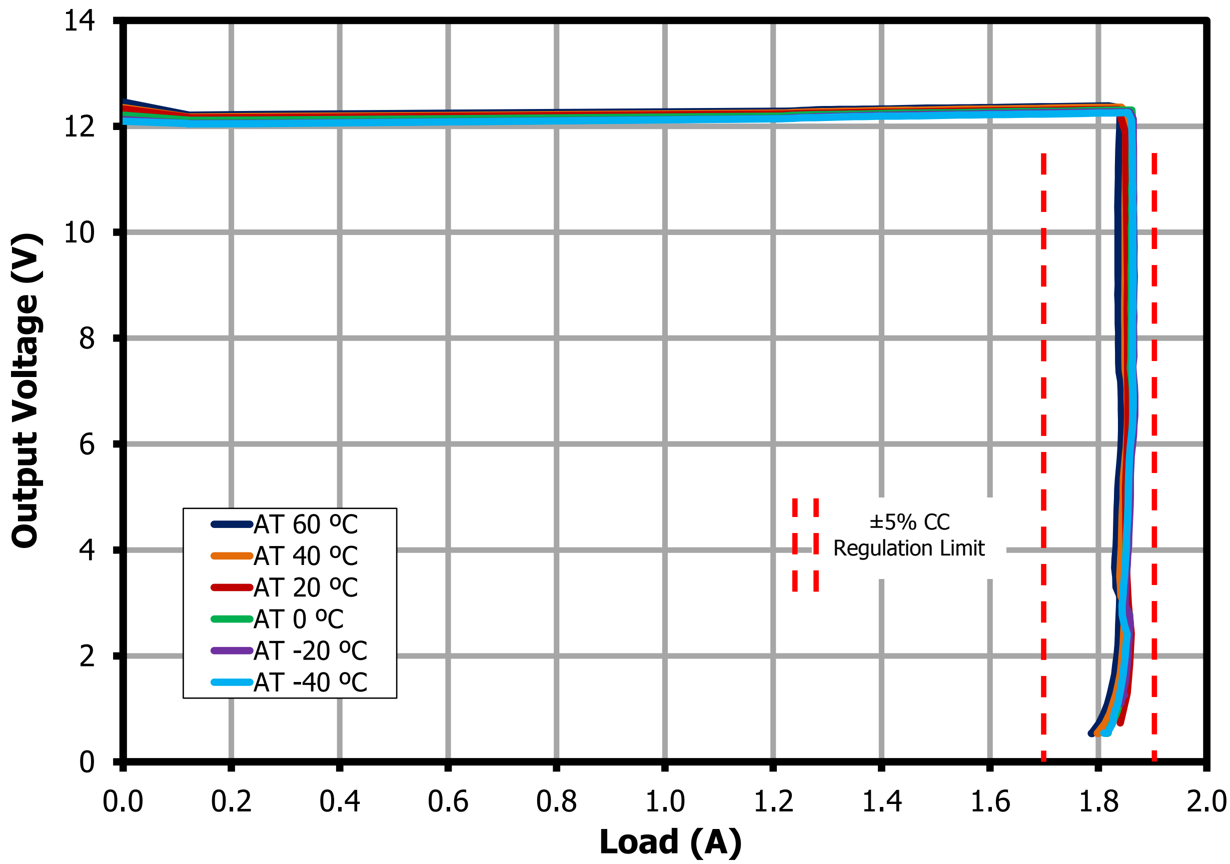

Figure 24 – CVCC Graph at 115 VAC, End of Cable.

11.3 At 230 VAC – End of Cable

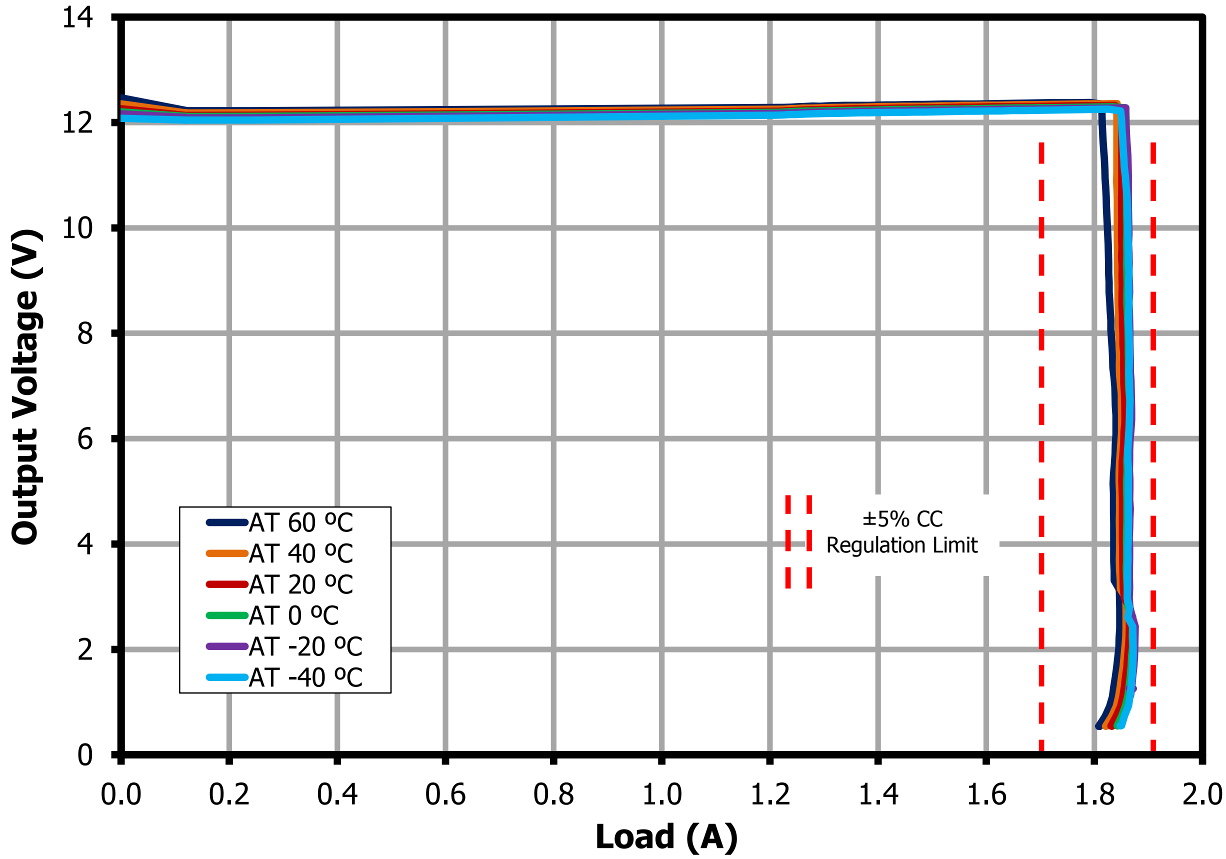

Figure 25 – CVCC Graph at 230 VAC, End of Cable.

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11.4 At 265 VAC – End of Cable

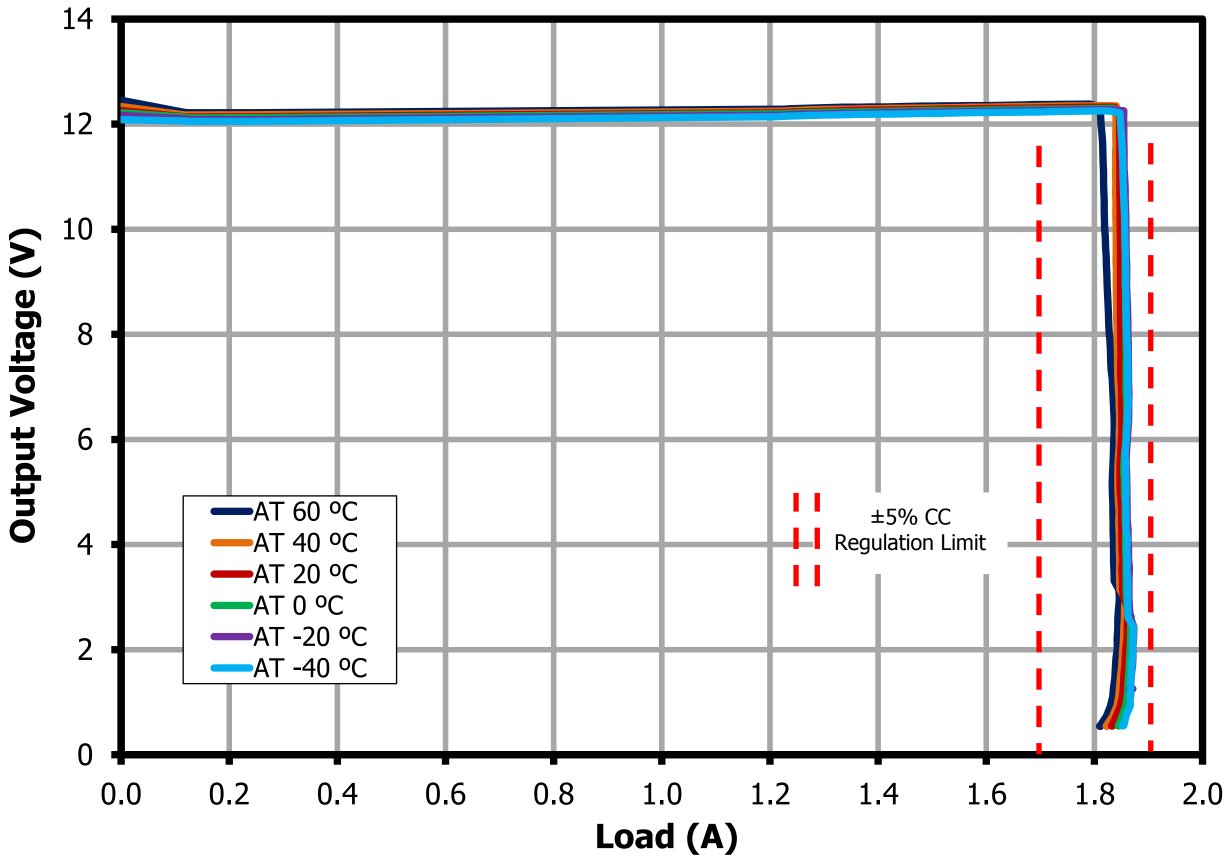

Figure 26 – CVCC Graph at 265 VAC, End of Cable.

12 No-Load Input Power

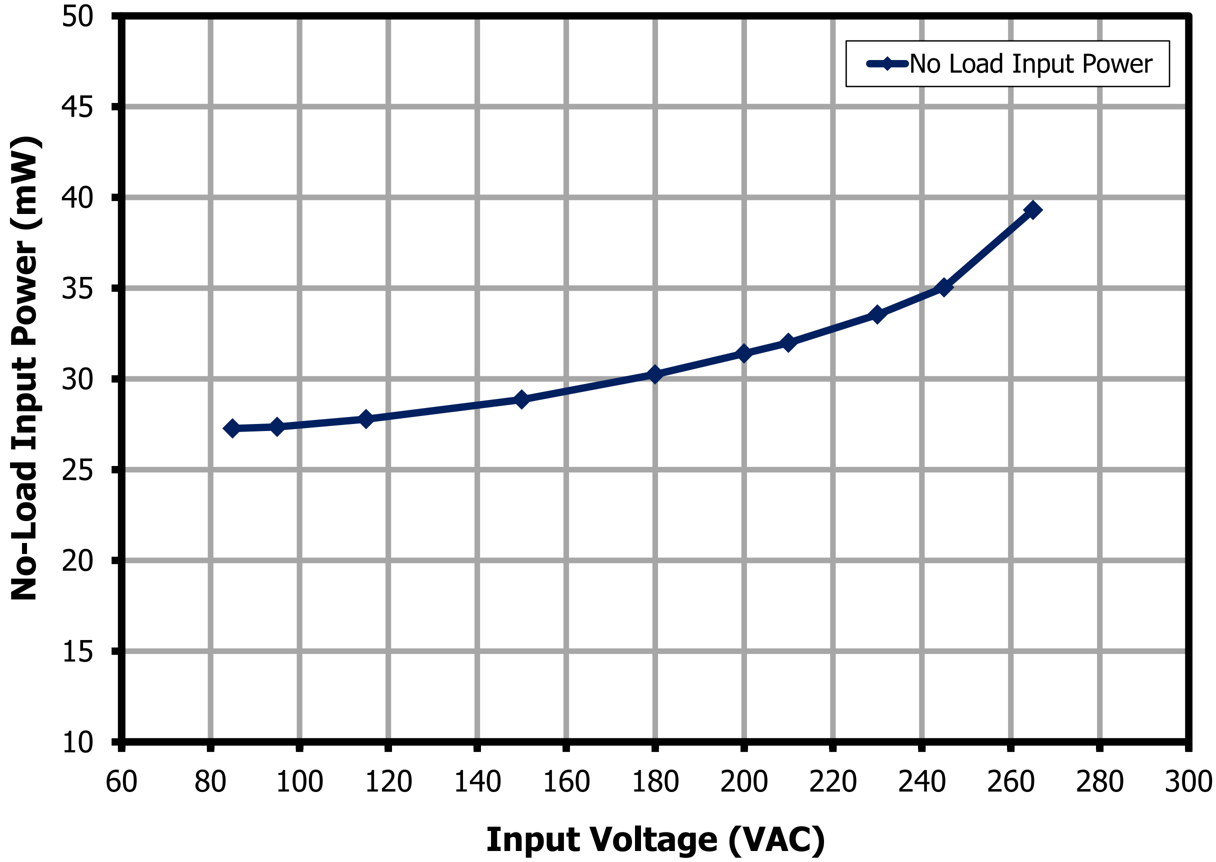

Figure 27 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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Input		Input Measurement (Integration)
VAC (V_{RMS})	Freq (Hz)	P (mW)
85	50	27.27
95	50	27.35
115	50	27.77
150	60	28.87
180	60	30.25
200	50	31.40
210	50	31.99
230	50	33.54
245	50	35.04
265	50	39.31

Figure 28 – No-Load Input Power vs. Input Line Voltage Data Table, Room Temperature.

13 Thermal Performance

The following measurements and test data exhibit the thermal performance of the flyback converter as well as the LNK4115D controller. The thermal performance was measured at different line input voltage (85 VAC and 265 VAC) and full load condition (1.5 A load). Overall test was performed at room temperature while the measurements were done after 1 hour soak time.

13.1 Thermals at 85 VAC

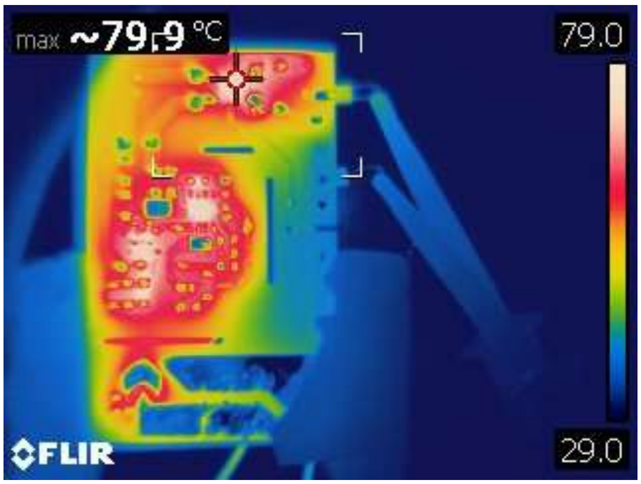

Figure 29 – Ambient = 27 ºC.
Input Bridge Rectifier = 79.9 ºC.

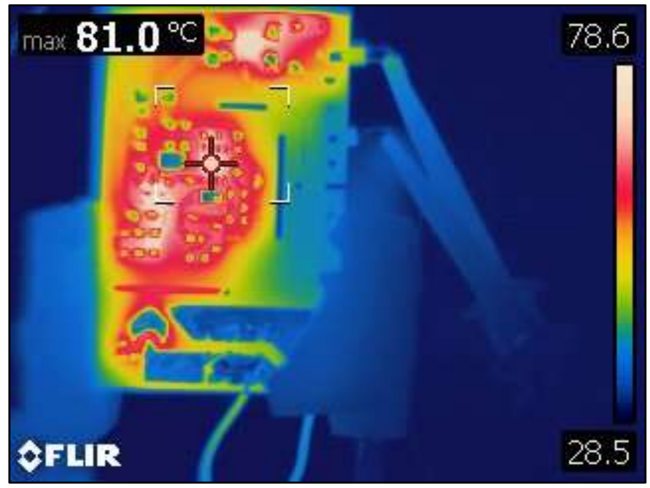

Figure 30 – Ambient = 27 ºC.
LinkSwitch-4 IC = 81.0 ºC.

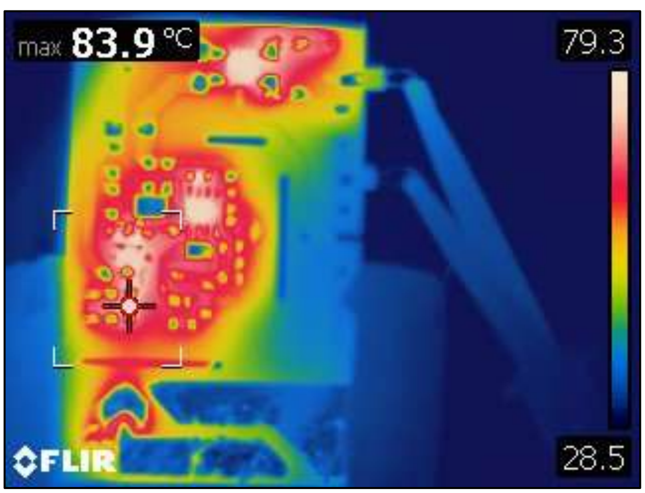

Figure 31 – Ambient = 27 ºC.
Primary Snubber Diode = 83.9 ºC.

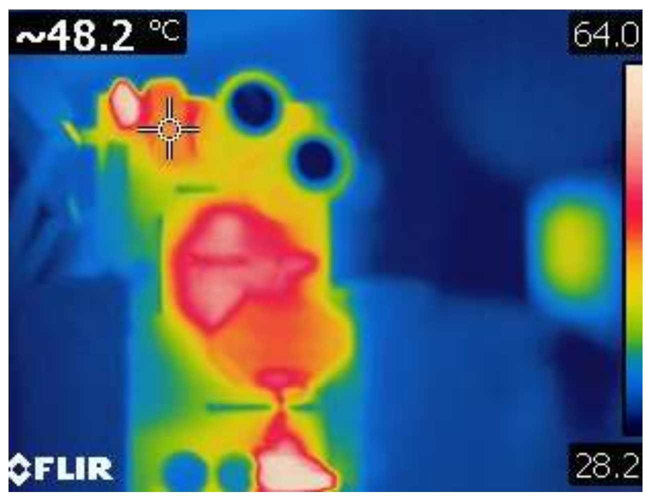

Figure 32 – Ambient = 27 ºC.
CMC Choke = 48.2 ºC.

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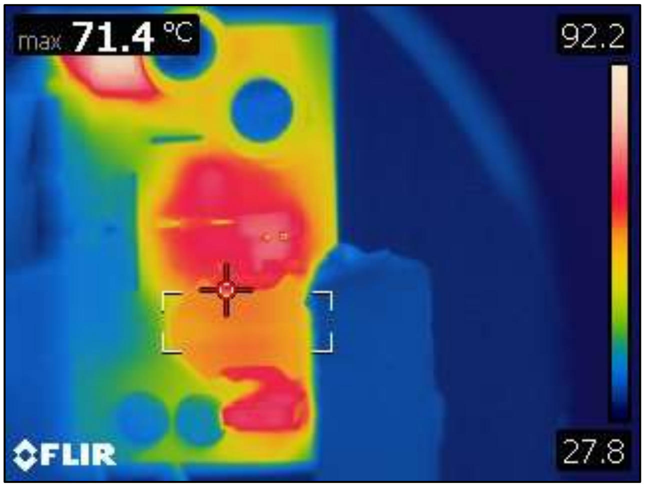

Figure 33 – Ambient = 27 ºC.
Transformer = 71.4 ºC.

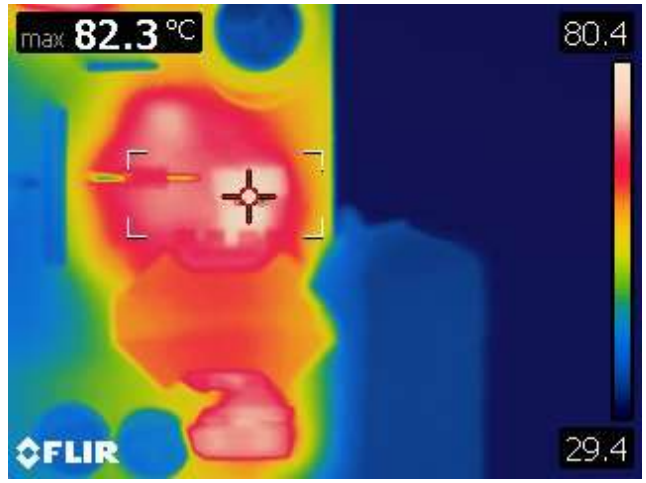

Figure 34 – Ambient = 27 ºC.
BJT = 82.3 ºC.

Figure 35 – Ambient = 27 ºC.
Secondary Diode = 76.9 ºC.

13.2 Thermals at 265 VAC

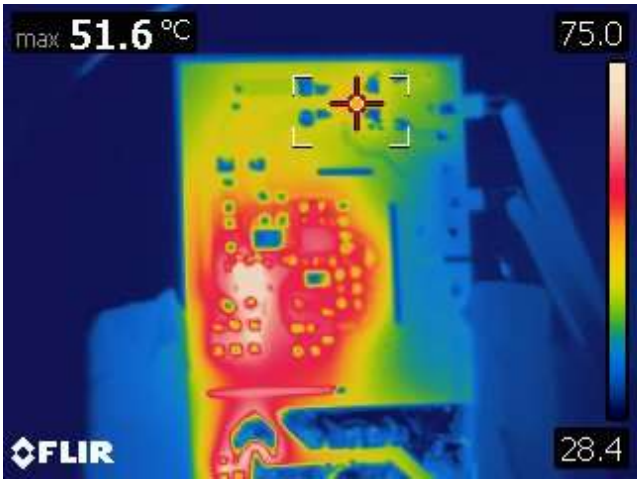

Figure 36 – Ambient = 27 ºC.
Input Bridge Rectifier = 51.6 ºC.

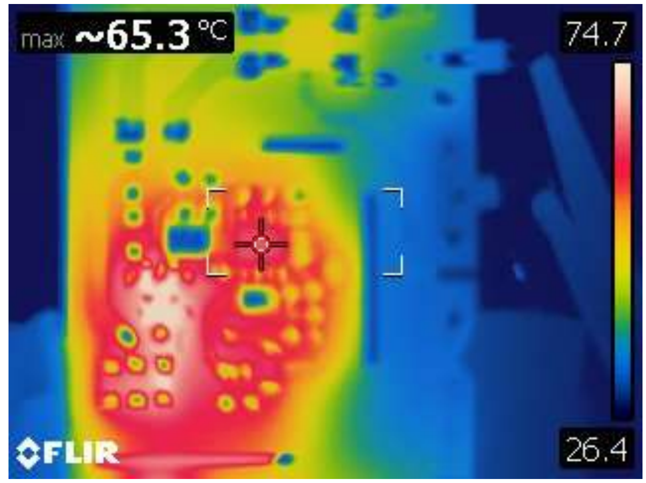

Figure 37 – Ambient = 27 ºC.
LinkSwitch-4 IC = 65.3 ºC.

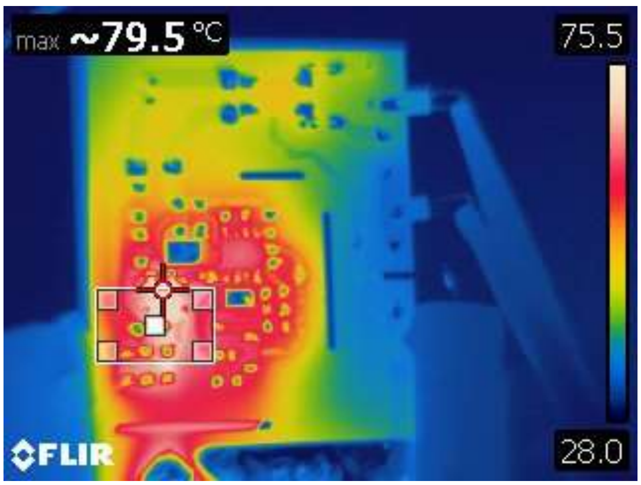

Figure 38 – Ambient = 27 ºC.
Primary Snubber Diode = 79.5 ºC.

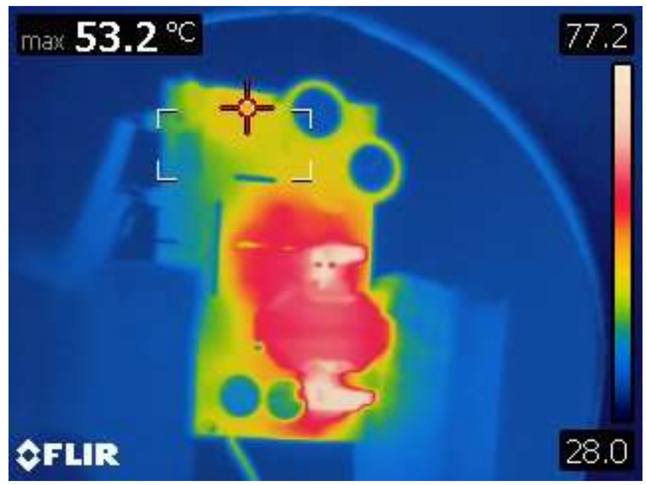

Figure 39 – Ambient = 27 ºC.
CMC Choke = 53.2 ºC.

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Figure 40 – Ambient = 27 ºC.
Transformer = 70.2 ºC.

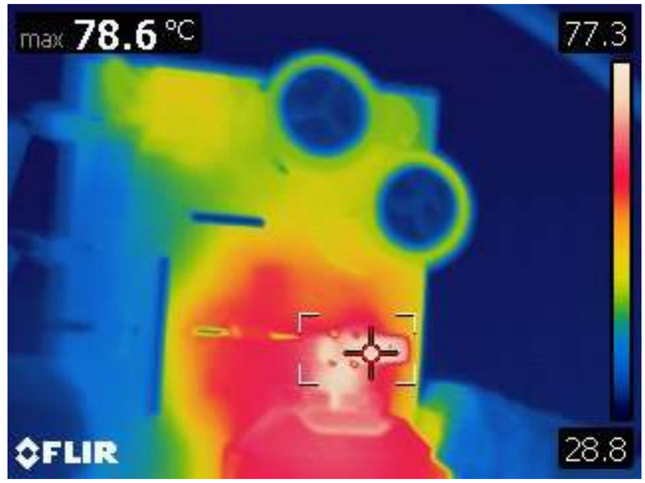

Figure 41 – Ambient = 27 ºC.
BJT = 78.6 ºC.

Figure 42 – Ambient = 27 ºC.
Secondary Diode = 75.5 ºC.

13.3 Thermal Measurement Summary Table

COMPONENT	TEMPERATURE at 85 VAC (ºC)	TEMPERATURE at 265 VAC (ºC)
Input Bridge Rectifier	79.9	51.6
LinkSwitch-4 IC	81.0	65.3
Primary Snubber Diode	83.9	79.5
CMC Choke	48.2	53.2
Transformer	71.4	70.2
BJT	82.3	78.6
Secondary Diode	76.9	75.5

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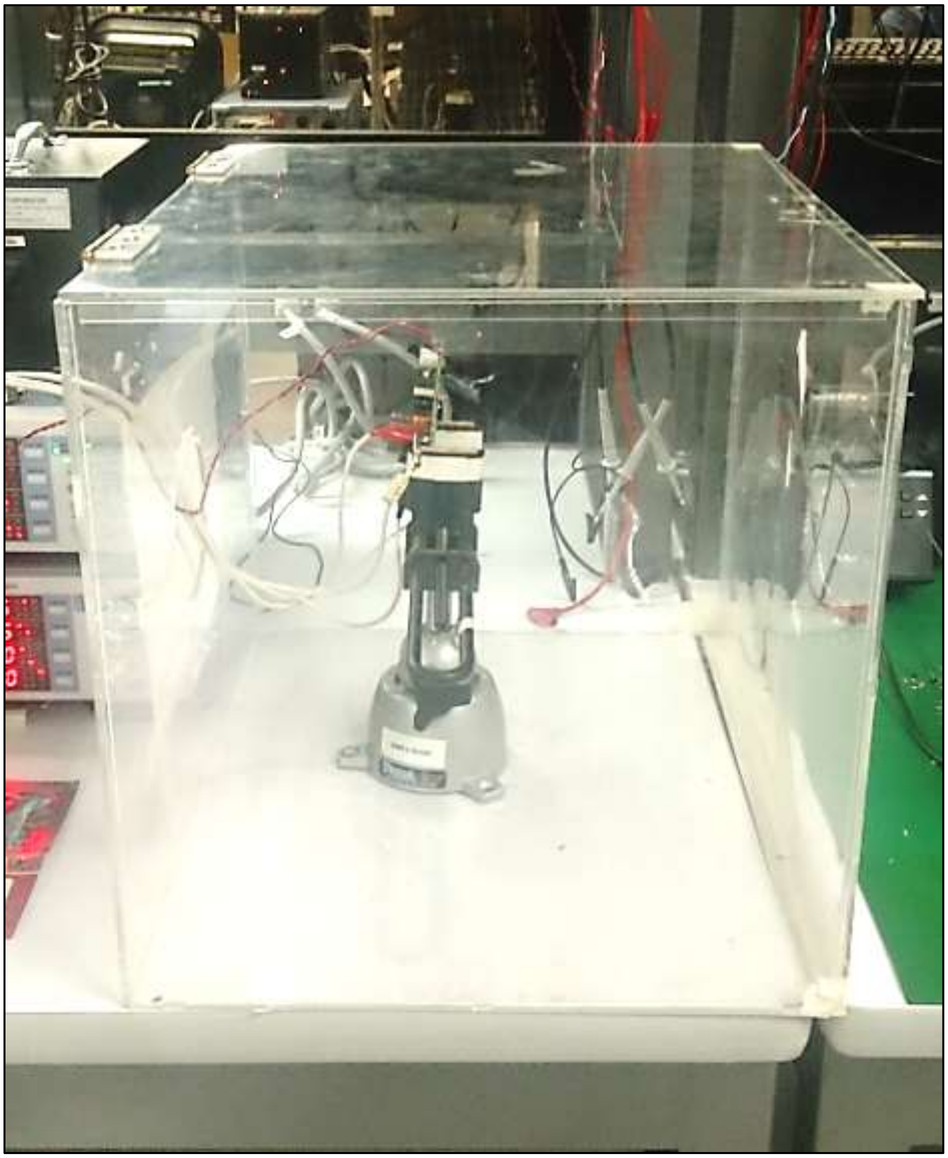
13.4 Thermal Set-Up



13.5 Test Conditions

1. THERMALS MEASURED AT FULL LOAD CONDITION, 1.5 A.
2. UNIT WAS ENCLOSED IN AN ACRYLIC BOX.
3. UNIT THERMAL MEASUREMENT PERFORMED AFTER 1 HOUR SOAK TIME.
4. DATA GATHERED FOR 85 VAC AND 265 VAC INPUT LINE.

14 Waveforms

14.1 Output Voltage Start-up

NOTE: THE INPUT AND OUTPUT VOLTAGE (AT THE MAIN OUTPUT TERMINAL) WERE CAPTURED AND TESTED WITH THE UNIT AT 1.5 A FULL LOAD (CONSTANT CURRENT SETTING FOR THE ELECTRONIC LOAD).

14.1.1 0% Load

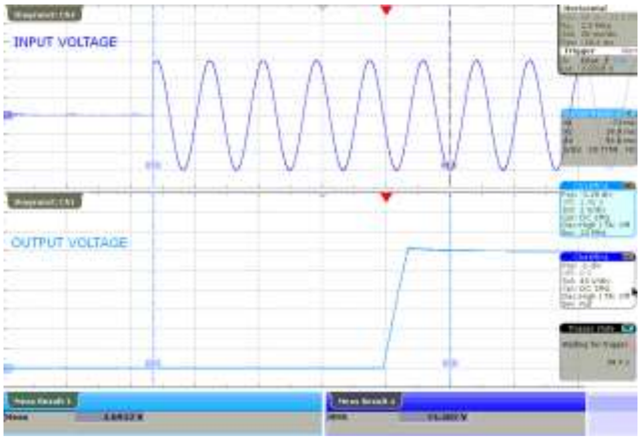


Figure 43 – 85 VAC, No-Load.
Upper: V_{IN}, 40 V / div., 20 ms/div.
Lower: V_{OUT}, 2 V / div., 20 ms / div.
Measured Time from AC ON to V_{OUT} = 92 ms.
Measured V_{OUT} Rise Time = 8 ms.

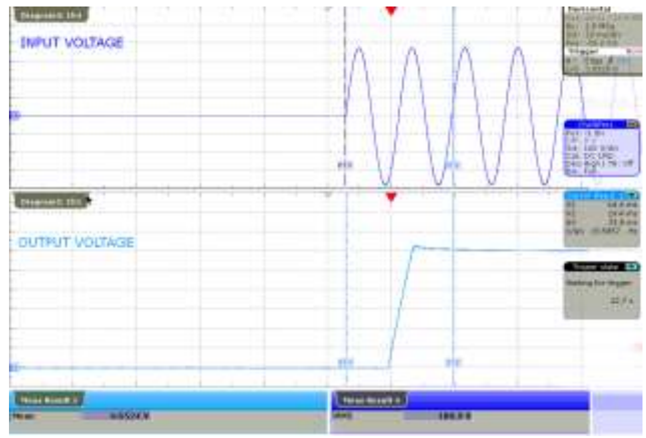


Figure 44 – 265 VAC, No-Load.
Upper: V_{IN}, 100 V / div., 20 ms /div.
Lower: V_{OUT}, 2 V / div., 20 ms / div.
Measured Time from AC ON to V_{OUT} = 33 ms.
Measured V_{OUT} Rise Time = 8 ms.

14.1.2 100% Load

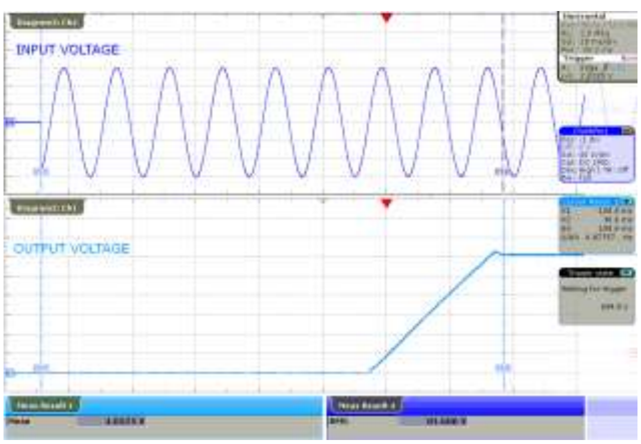


Figure 45 – 85 VAC, Full Load.
Upper: V_{IN}, 40 V / div., 20 ms/div.
Lower: V_{OUT}, 2 V / div., 20 ms / div.
Measured Time from AC ON to V_{OUT} = 145 ms
Measured V_{OUT} Rise Time = 42 ms.

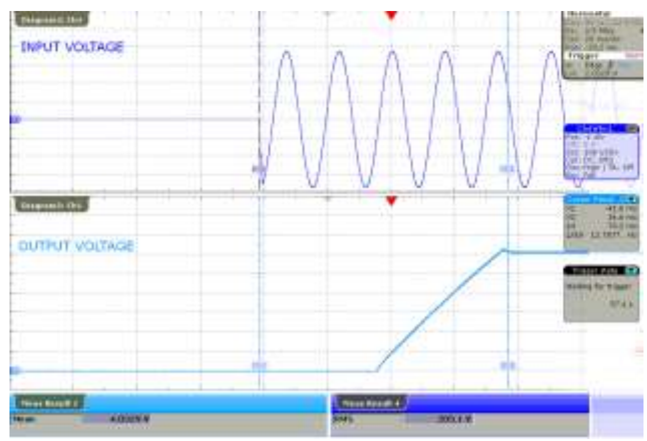


Figure 46 – 265 VAC, Full Load.
Upper: V_{IN}, 100 V / div., 20 ms /div.
Lower: V_{OUT}, 2 V / div., 20 ms / div.
Measured Time from AC ON to V_{OUT} = 78 ms
Measured V_{OUT} Rise Time = 42 ms.

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14.2 Aux Voltage

14.2.1 0% Load

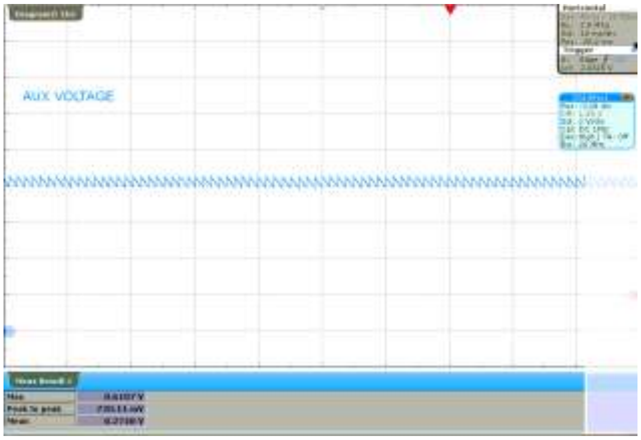

Figure 47 – 85 VAC, No-Load.
V_{AUX}, 2 V / div., 10 ms / div.
Measured Peak to Peak Voltage = 720 mV_{PK-PK}.
Measured Mean Voltage = 8.27 V.

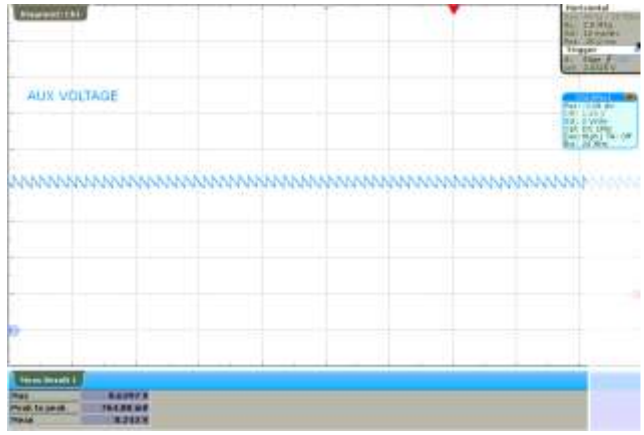

Figure 48 – 265 VAC, No-Load.
V_{AUX}, 2 V / div., 10 ms / div.
Measured Peak to Peak Voltage = 764 mV_{PK-PK}.
Measured Mean Voltage = 8.24 V.

14.2.2 100% Load

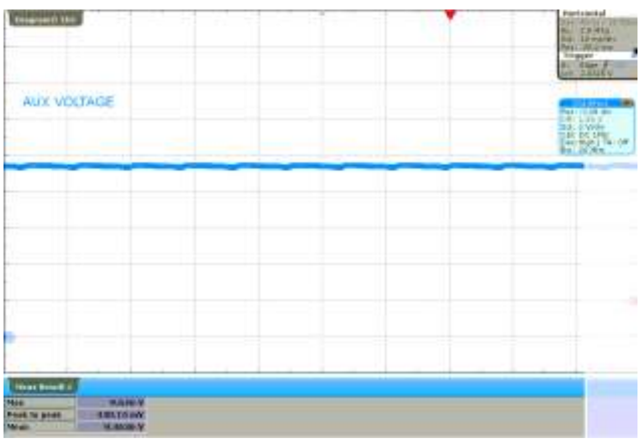

Figure 49 – 85 VAC, Full Load.
V_{AUX}, 2 V / div., 10 ms / div.
Measured Peak to Peak Voltage = 430 mV_{PK-PK}.
Measured Mean Voltage = 9.46 V.

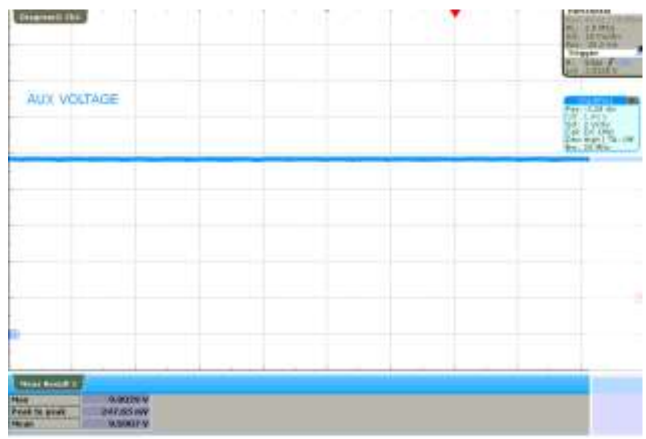

Figure 50 – 265 VAC, Full Load.
V_{AUX}, 2 V / div., 10 ms / div.
Measured Peak to Peak Voltage = 247 mV_{PK-PK}.
Measured Mean Voltage = 9.69 V.

14.3 Collector-Emitter Voltage

NOTE: THE COLLECTOR-EMITTER VOLTAGE WAS CAPTURED AND TESTED WITH THE UNIT AT NO-LOAD AND FULL LOAD (CONSTANT CURRENT SETTING FOR THE ELECTRONIC LOAD AT 1.5 A) CONDITION.

14.3.1 0% Load

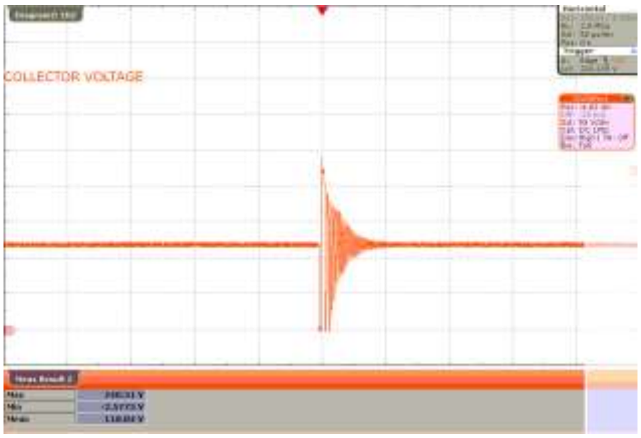

Figure 51 – 85 VAC, No-Load.
V_{COL}, 100 V / div., 50 μs / div.
Maximum Peak Collector Voltage = 240 V_{PK}.

Figure 52 – 265 VAC, No-Load.
V_{COL}, 100 V / div., 50 μs / div.
Maximum Peak Collector Voltage = 496 V_{PK}.

14.3.2 100% Load

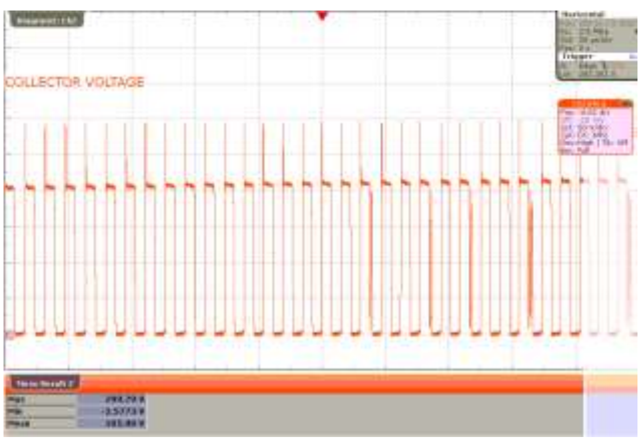

Figure 53 – 85 VAC, Full Load.
V_{COL}, 50 V / div., 50 μs / div.
Maximum Peak Collector Voltage = 299 V_{PK}.

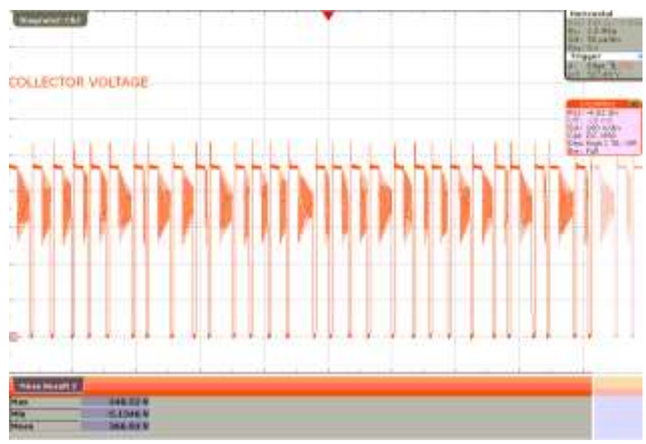

Figure 54 – 265 VAC, Full Load.
V_{COL}, 100 V / div., 50 μs / div.
Maximum Peak Collector Voltage = 540 V_{PK}.

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14.4 Secondary Diode Voltage

NOTE: THE SECONDARY DIODE VOLTAGE WAS CAPTURED AND TESTED WITH THE UNIT AT NO LOAD AND FULL LOAD (CONSTANT CURRENT SETTING FOR THE ELECTRONIC LOAD AT 1.5 A) CONDITION.

14.4.1 0% Load

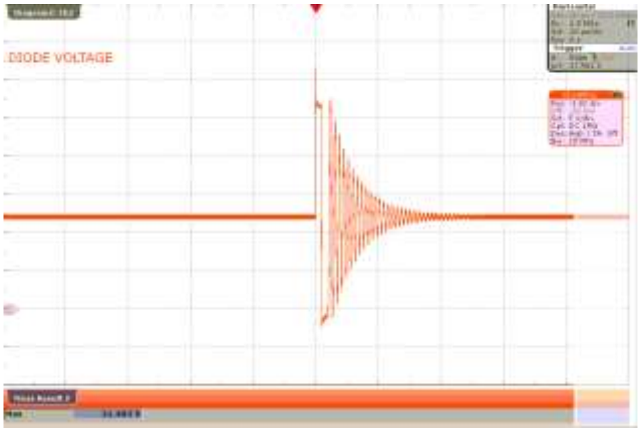

Figure 55 – 85 VAC, No-Load.
V_{COL}, 5 V / div., 20 μs / div.
Maximum Peak Diode Voltage = 31 V_{PK}.

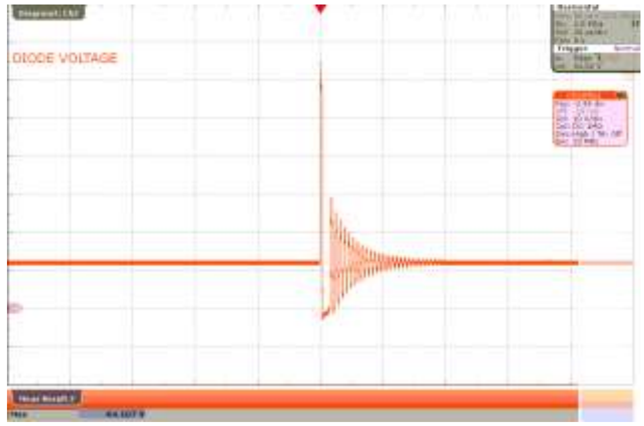

Figure 56 – 265 VAC, No-Load.
V_{COL}, 10 V / div., 20 μs / div.
Maximum Peak Diode Voltage = 64 V_{PK}.

14.4.2 100% Load

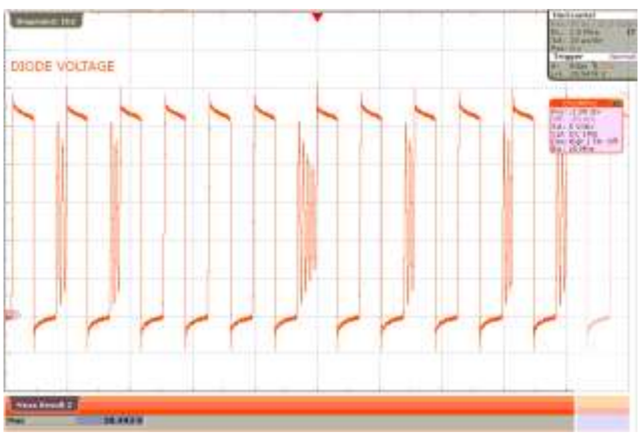

Figure 57 – 85 VAC, Full Load.
V_{COL}, 5 V / div., 20 μs / div.
Maximum Peak Diode Voltage = 30 V_{PK}.

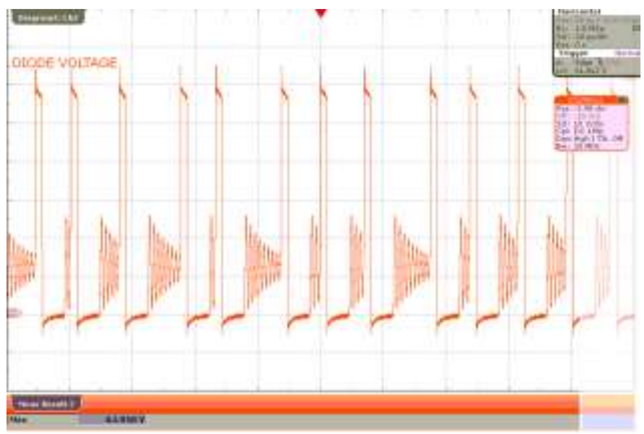

Figure 58 – 265 VAC, Full Load.
V_{COL}, 10 V / div., 20 μs / div.
Maximum Peak Diode Voltage = 64 V_{PK}.

14.5 Load Transient Response – End of 1 Meter #22 AWG Cable

NOTE: THE LOAD TRANSIENT WAS PERFORMED/TESTED WITH THE UNIT AT FULL LOAD (1.5 A LOAD). HIGH TIME (1.5 A LOAD) WAS SET AT 5 ms WHILE THE LOW TIME (AT 0.1 A, 0.25 A, and 0.5 A LOAD) WAS ALSO SET AT 5 ms. THE CURRENT SLEW RATE IS AT 100 mA / µs.

14.5.1 Load Transient Response at 85 VAC (End of Cable)

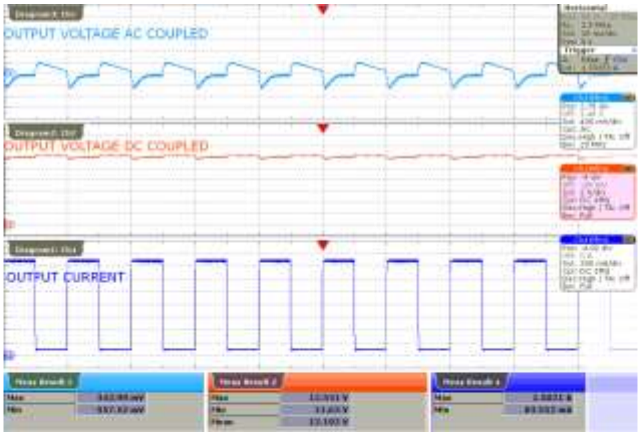

Figure 59 – Transient Response at 85 VAC.
0.1 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.53 V_{PK}.
Measured Min Peak Voltage = 11.63 V_{PK}.

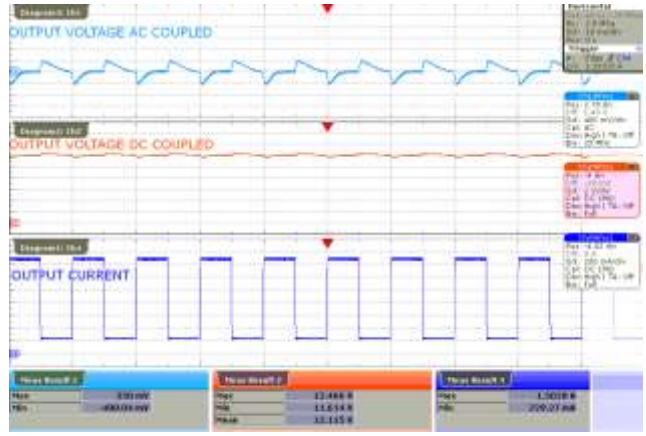

Figure 60 – Transient Response at 85 VAC.
0.25 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.46 V_{PK}.
Measured Min Peak Voltage = 11.61 V_{PK}.

Figure 61 – Transient Response at 85 VAC.
0.5 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.36 V_{PK}.
Measured Min Peak Voltage = 11.68 V_{PK}.

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14.5.2 Load Transient Response at 265 VAC (End of Cable)

Figure 62 – Transient Response at 265 VAC.
0.1 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.52 V_{PK}.
Measured Min Peak Voltage = 11.60 V_{PK}.

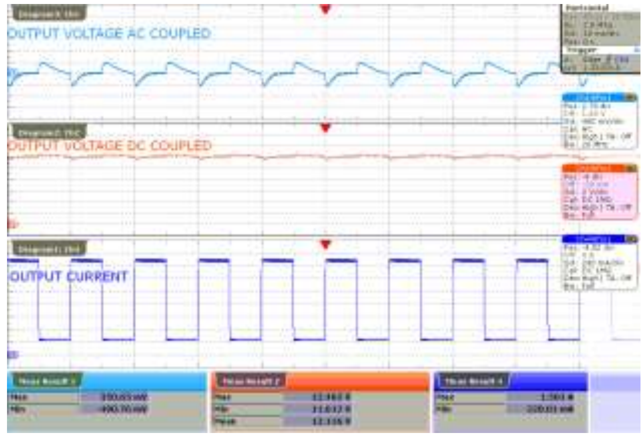

Figure 63 – Transient Response at 265 VAC.
0.25 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.46 V_{PK}.
Measured Min Peak Voltage = 11.61 V_{PK}.

Figure 64 – Transient Response at 265 VAC.
0.5 A - 1.5 A Load Step.
Upper: $V_{OUT(AC)}$, 400 mV / div., 10 ms / div.
Middle: $V_{OUT(DC)}$, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Measured Max Peak Voltage = 12.38 V_{PK}.
Measured Min Peak Voltage = 11.70 V_{PK}.

14.6 Brown-In / Brown-Out

NOTE: THE BROWN-IN/BROWN-OUT TEST WAS PERFORMED / TESTED AT 85VAC WITH THE UNIT AT 0%, 50%, AND 100% LOAD (0 A, 0.75 A, AND 1.5 A LOAD). THE INPUT VOLTAGE SLEW RATE WAS SET AT 0.1 V / sec. or 6 V / min.

14.6.1 0% Load

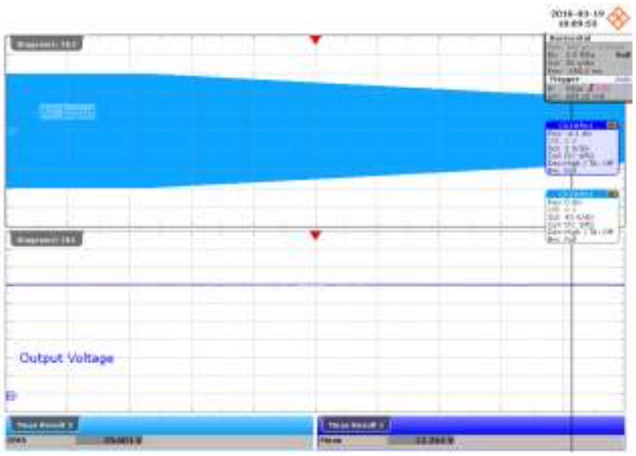

Figure 65 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

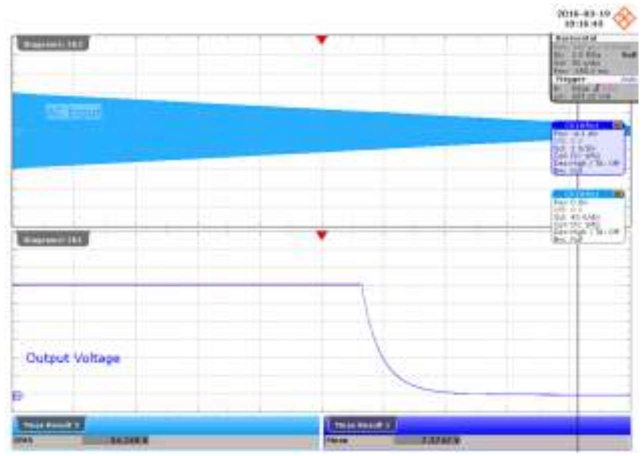

Figure 66 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

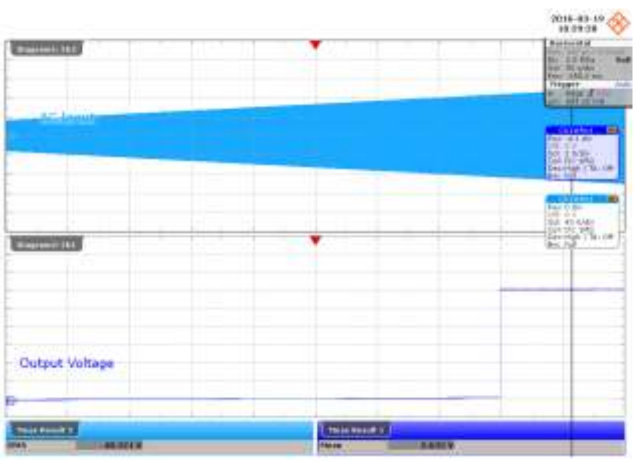

Figure 67 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

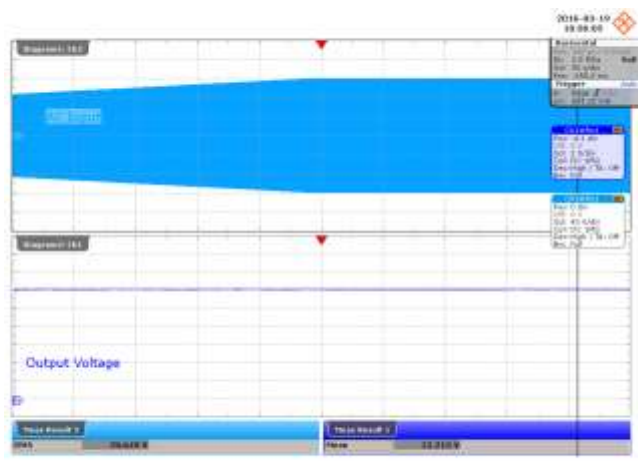

Figure 68 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

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14.6.2 50% Load

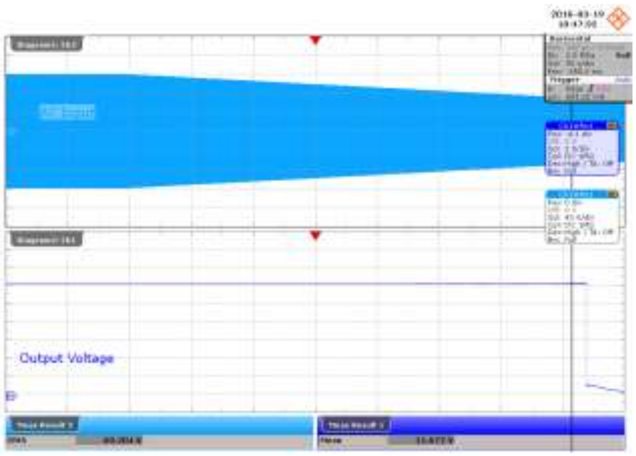

Figure 69 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

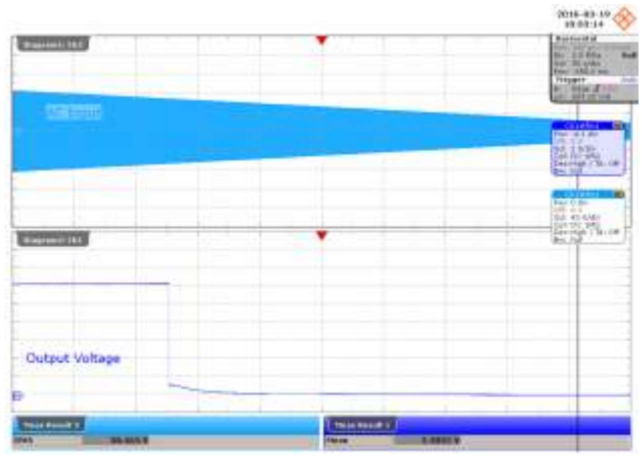

Figure 70 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

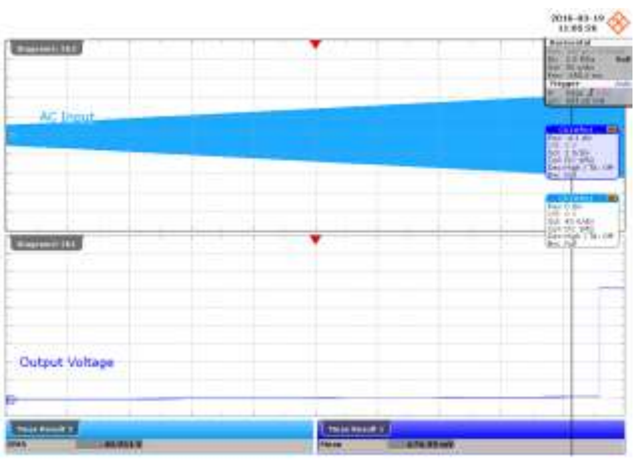

Figure 71 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

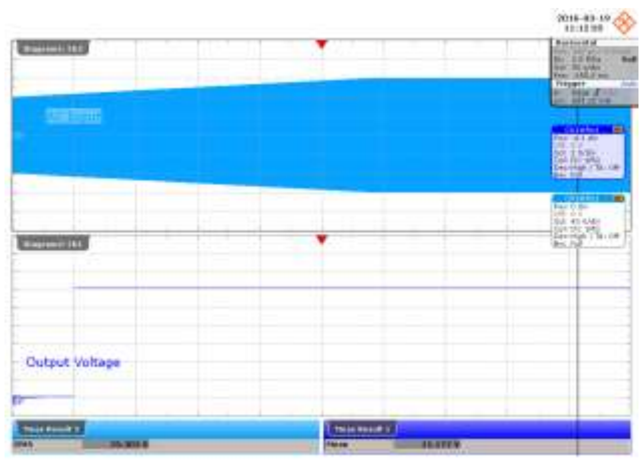

Figure 72 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

14.6.3 100% Load

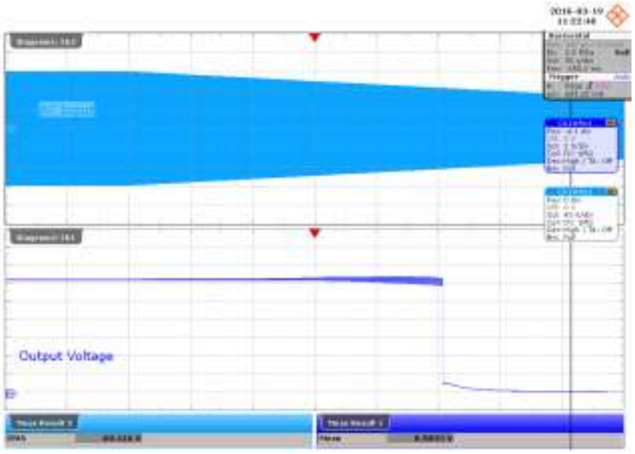

Figure 73 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

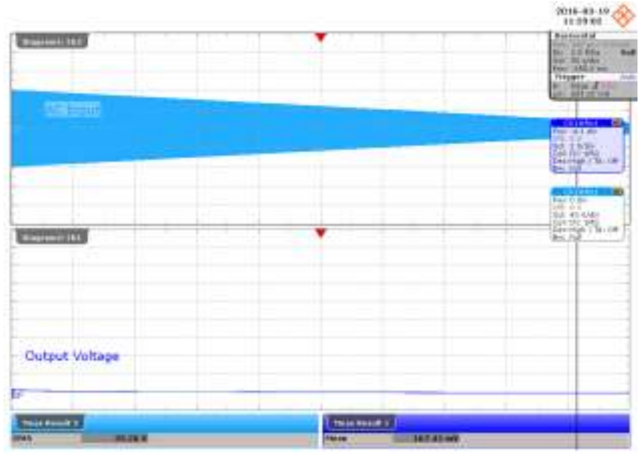

Figure 74 – 85 VAC, 60 Hz. Brown-out.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

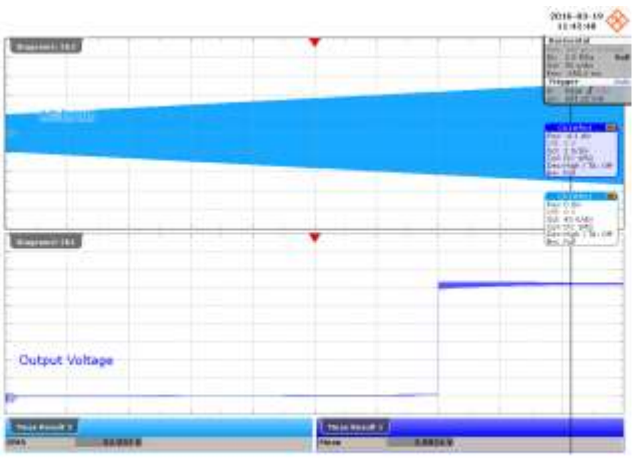

Figure 75 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

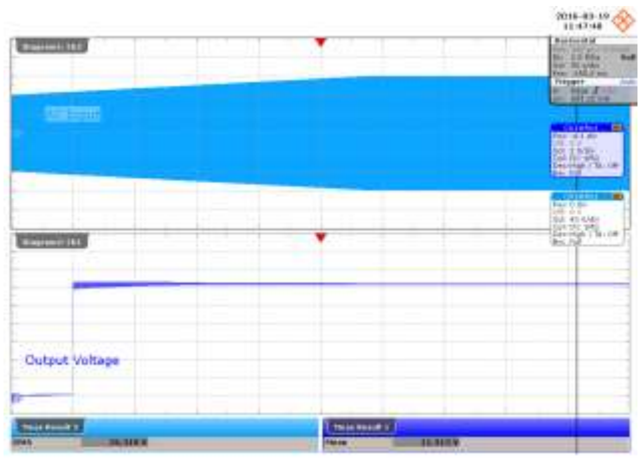

Figure 76 – 85 VAC, 60 Hz. Brown-in.
Upper: V_{AC}, 40 V / div., 50 s / div.
Lower: V_{OUT}, 2 V / div., 50 s / div.

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14.7 Start-up short

NOTE: THE UNIT WAS SHORTED AT THE MAIN OUTPUT (HARD SHORT) AND THE COLLECTOR VOLTAGE, OUTPUT VOLTAGE, AND OUTPUT CURRENT (ACROSS SHORT) WAS MONITORED FOR 85 VAC AND 265 VAC LINE INPUT.

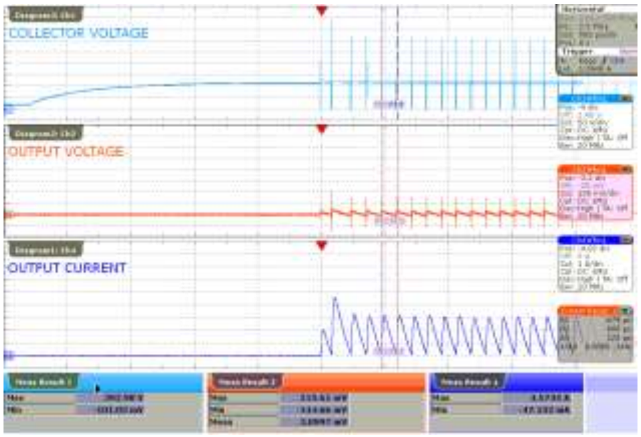

Figure 77 – Start-up Short at 85 VAC.
Upper: V_{COL}, 50 V / div., 500 µs / div.
Middle: V_{OUT}, 100 mV / div., 500 µs / div.
Lower: I_{OUT}, 1 A / div., 500 µs / div.
Measured Max Collector Peak Voltage = 392 V_{PK}.
Measured Max Output Short Current = 4.57 V_{PK}.
Measured Interval Time = 125 µs.

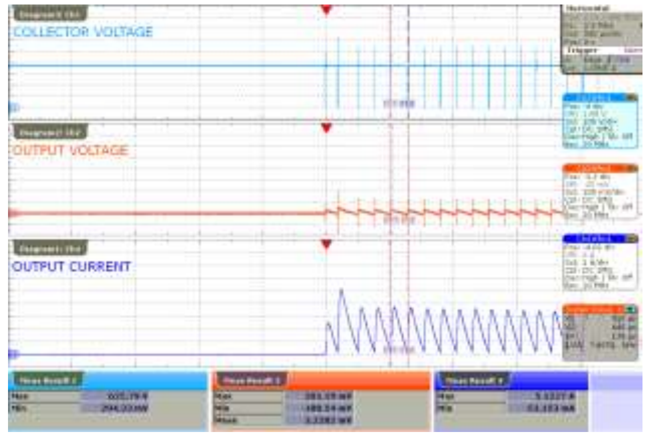

Figure 78 – Start-up Short at 265 VAC.
Upper: V_{COL}, 100 V / div., 500 µs / div.
Middle: V_{OUT}, 100 mV / div., 500 µs / div.
Lower: I_{OUT}, 1 A / div., 500 µs / div.
Measured Max Collector Peak Voltage = 625 V_{PK}.
Measured Max Output Short Current = 5.12 V_{PK}.
Measured Interval Time = 135 µs.

14.8 Running Short

NOTE: THE UNIT WAS SHORTED AT THE MAIN OUTPUT (HARD SHORT) WHILE IT IS RUNNING AT FULL LOAD. THE COLLECTOR-EMITTER VOLTAGE, OUTPUT VOLTAGE, AND OUTPUT CURRENT (MEASURED AFTER THE SHORT) WAS MONITORED FOR 85 VAC AND 265 VAC LINE INPUT.

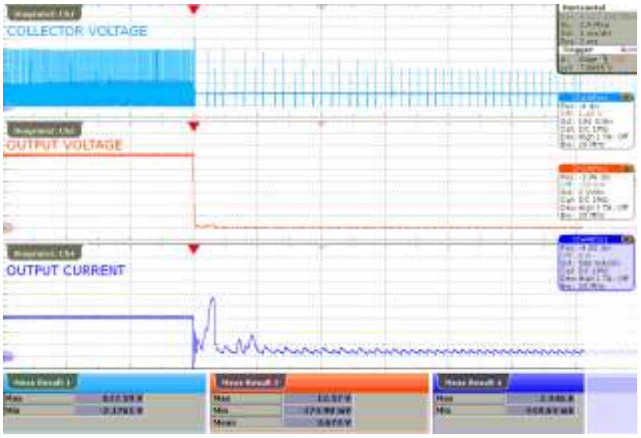

Figure 79 – Running Short at 85 VAC.
Upper: V_{COL}, 100 V / div., 1 ms / div.
Middle: V_{OUT}, 2 V / div., 1 ms / div.
Lower: I_{OUT}, 500 mA /div., 1 ms / div.
Measured Max Collector Peak Voltage = 617 V_{PK}.

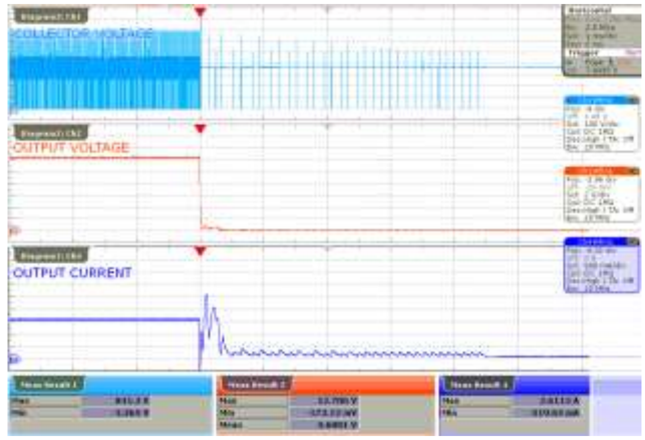

Figure 80 – Running Short at 265 VAC.
Upper: V_{COL}, 100 V / div., 1 ms / div.
Middle: V_{OUT}, 2 V / div., 1 ms / div.
Lower: I_{OUT}, 500 mA /div., 1 ms / div.
Measured Max Collector Peak Voltage = 841 V_{PK}.

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14.9 Output Ripple

14.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

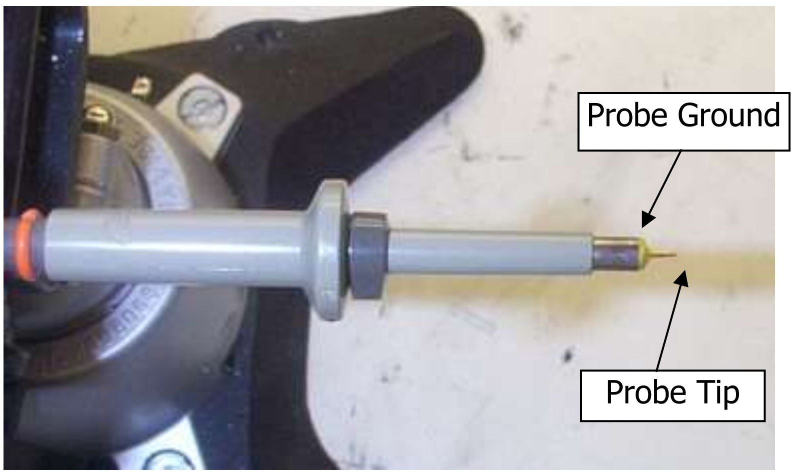

Figure 81 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 82 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

14.9.2 Output Ripple Voltage at 100% Loading Condition, End of Cable

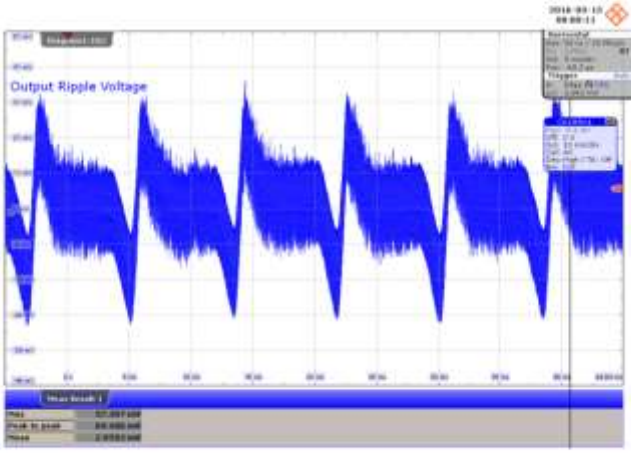

Figure 83 – At 85 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 5 ms / div.
Measured V_{OUT} Ripple = 69 mV_{PK-PK}.

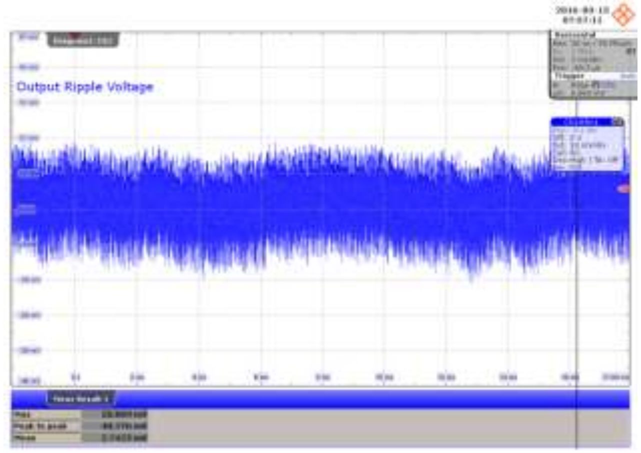

Figure 84 – At 115 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 40 mV_{PK-PK}.

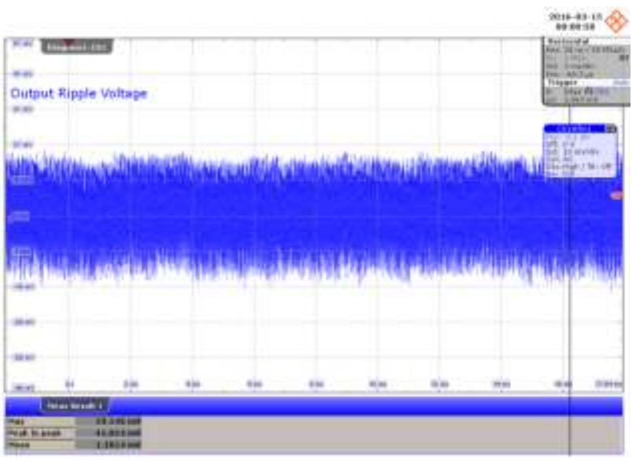

Figure 85 – At 230 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 41 mV_{PK-PK}.

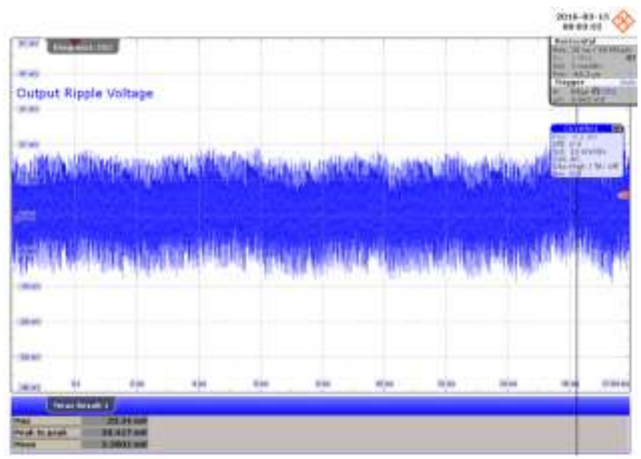

Figure 86 – At 265 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 39 mV_{PK-PK}.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

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14.9.3 Output Ripple Voltage at 75% Loading Condition, End of Cable

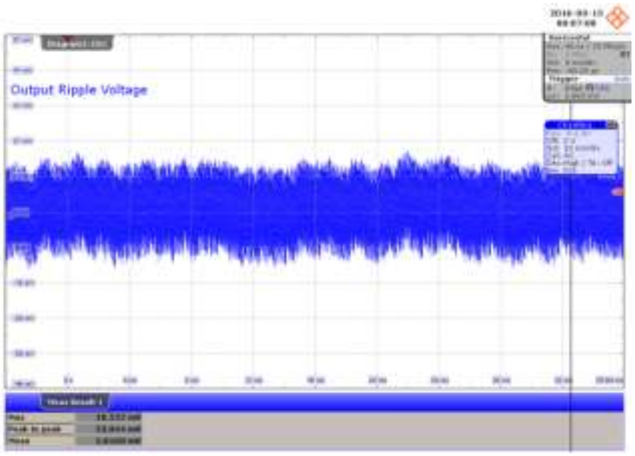

Figure 87 – At 85 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 4 ms / div.
Measured V_{OUT} Ripple = 33 mV_{PK-PK}.

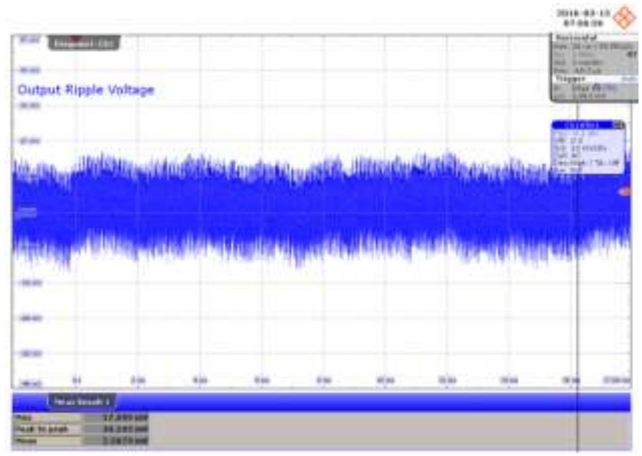

Figure 88 – At 115 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 34 mV_{PK-PK}.

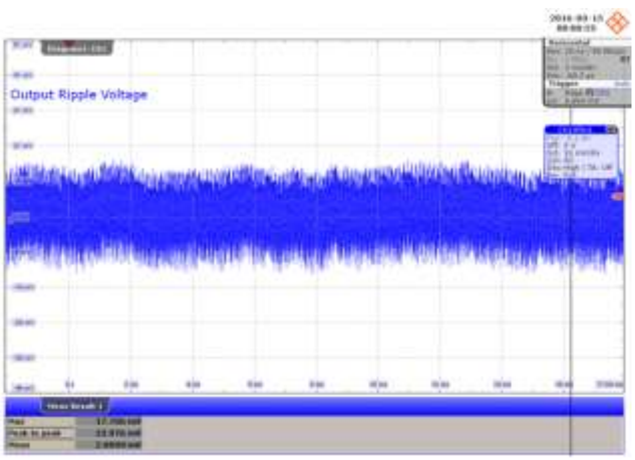

Figure 89 – At 230 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 32 mV_{PK-PK}.

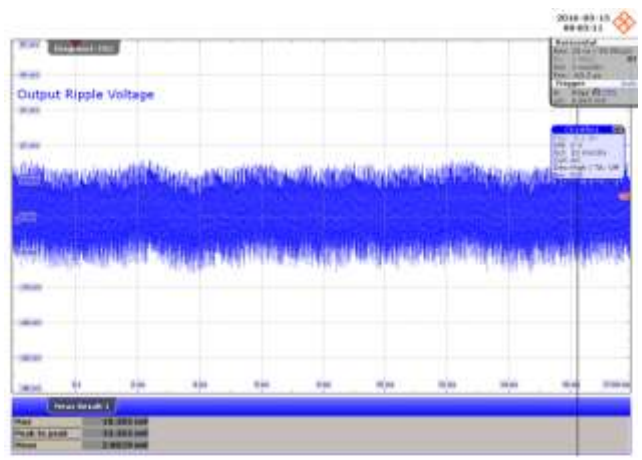

Figure 90 – At 265 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 33 mV_{PK-PK}.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

14.9.4 Output Ripple Voltage at 50% Loading Condition, End of Cable

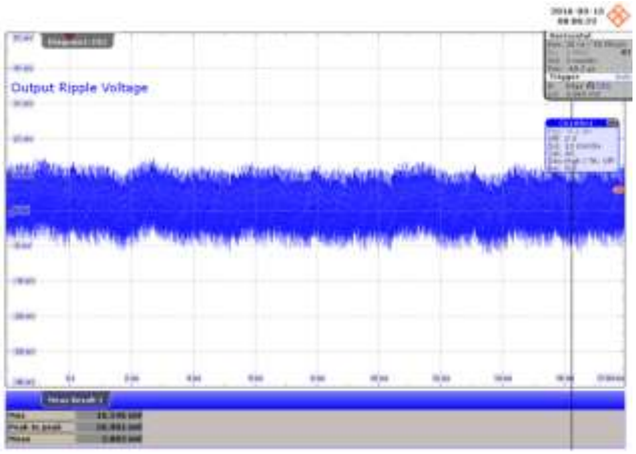

Figure 91 – At 85 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 26 mV_{PK-PK}.

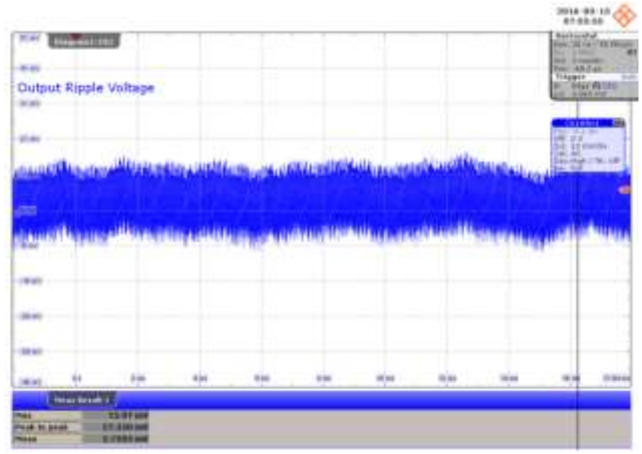

Figure 92 – At 115 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 27 mV_{PK-PK}.

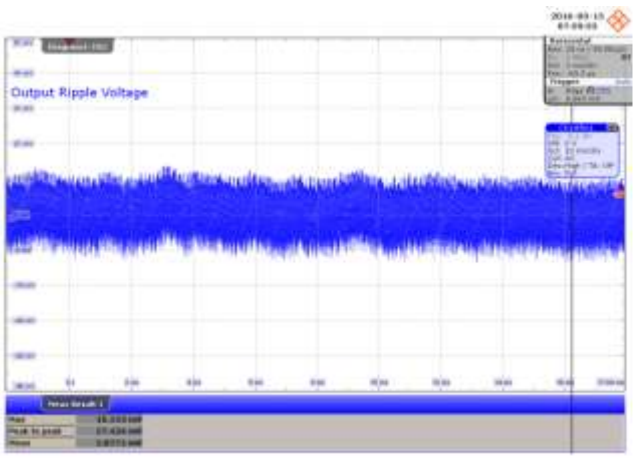

Figure 93 – At 230 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 27 mV_{PK-PK}.

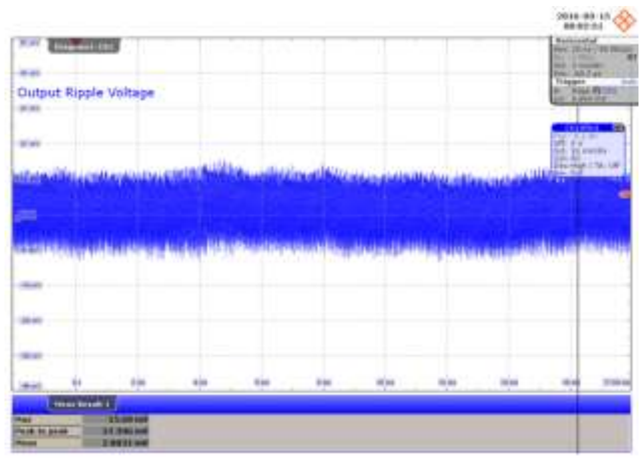

Figure 94 – At 265 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 27 mV_{PK-PK}.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

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14.9.5 Output Ripple Voltage at 10% Loading Condition, End of Cable

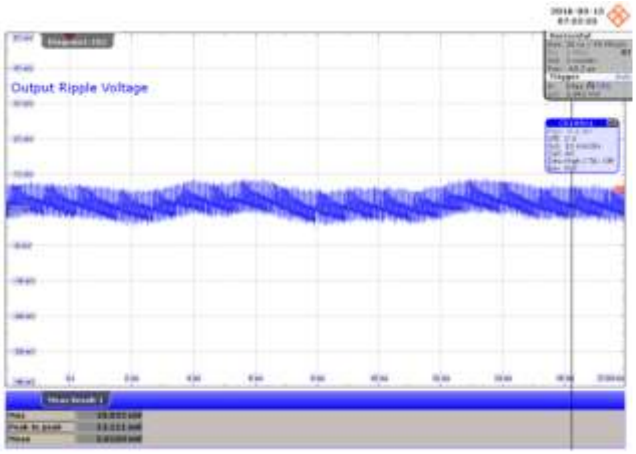

Figure 95 – At 85 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 13 mV_{PK-PK}.

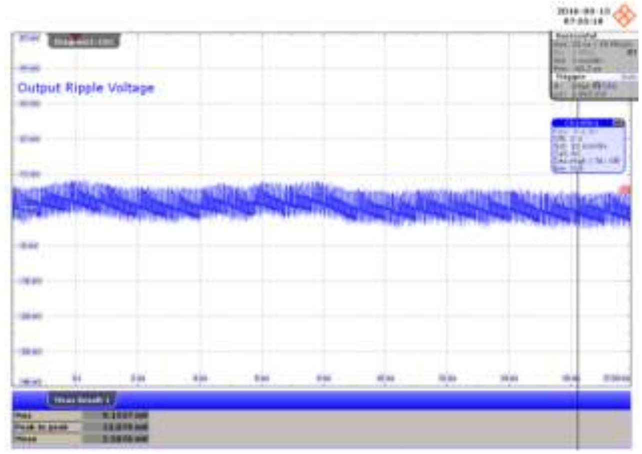

Figure 96 – At 115 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 13 mV_{PK-PK}.

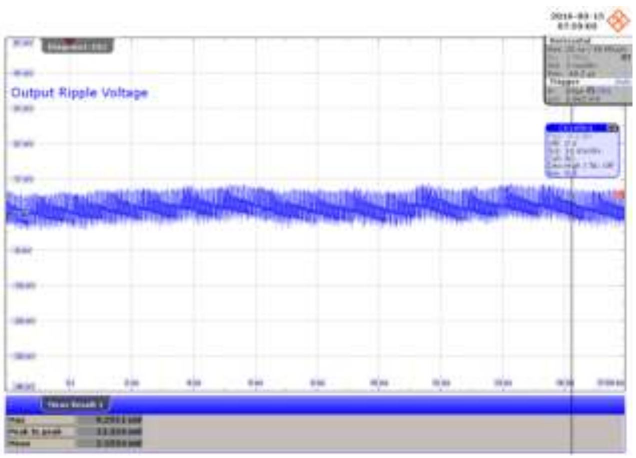

Figure 97 – At 230 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 13 mV_{PK-PK}.

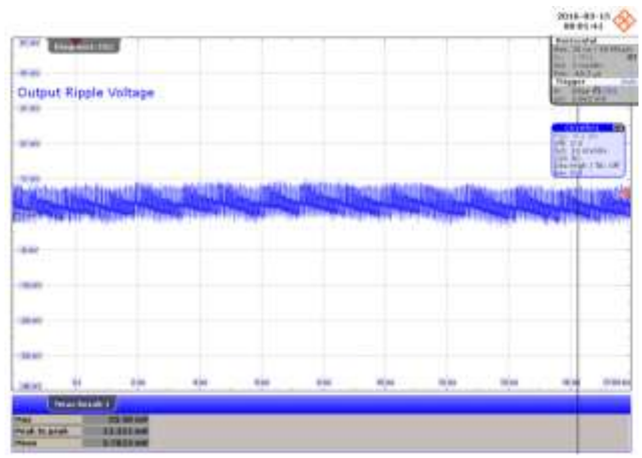

Figure 98 – At 265 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 13 mV_{PK-PK}.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

14.9.6 Output Ripple Voltage at 0% Loading Condition, End of Cable

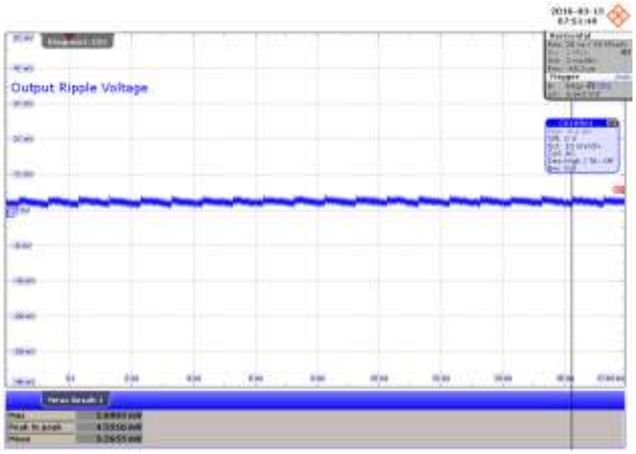

Figure 99 – At 85 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 4 mV_{PK-PK}.

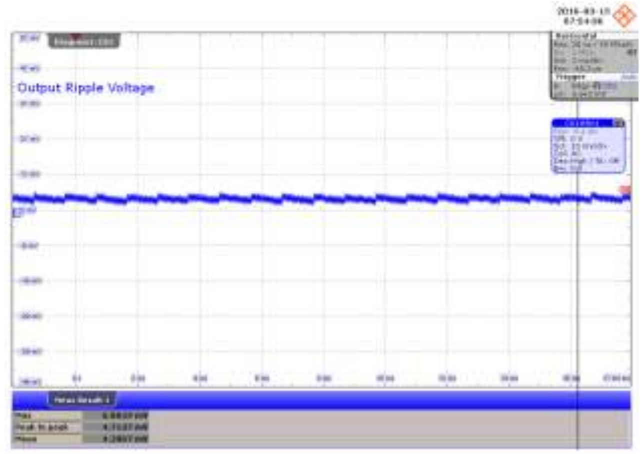

Figure 100 – At 115 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 4 mV_{PK-PK}.

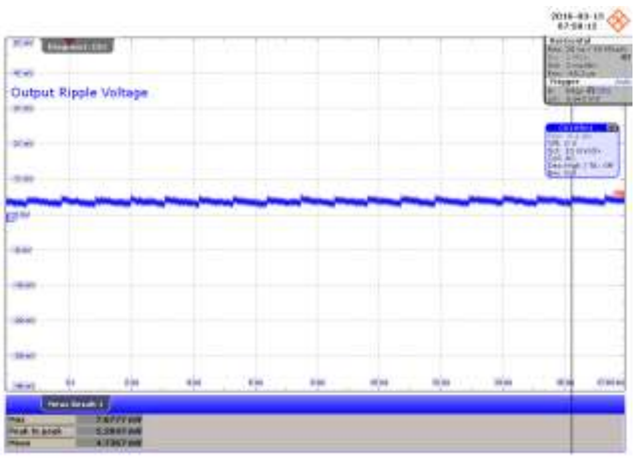

Figure 101 – At 230 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 5 mV_{PK-PK}.

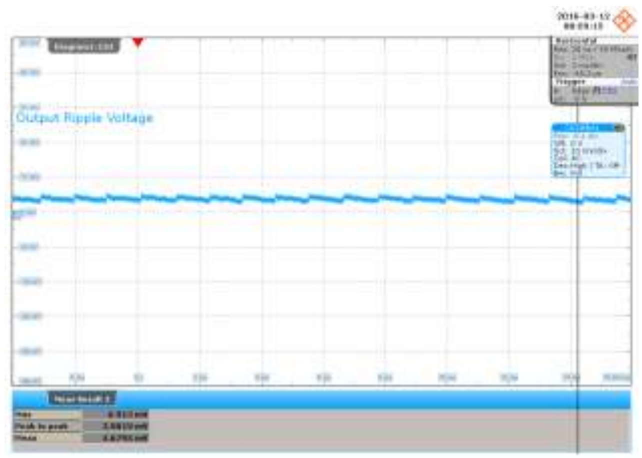

Figure 102 – At 265 VAC.
$V_{OUT(RIPPLE)}$, 10 mV / div., 2 ms / div.
Measured V_{OUT} Ripple = 3 mV_{PK-PK}.

NOTE: Cable used is 1 meter, #22 AWG twisted pair of wire with an equivalent total resistance of 100 mΩ.

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15 Conducted EMI

15.1 Conducted EMI Scan with 1.5 A Resistive Load (Floating)

15.1.1 Conducted EMI Scan at 115 VAC Input Line

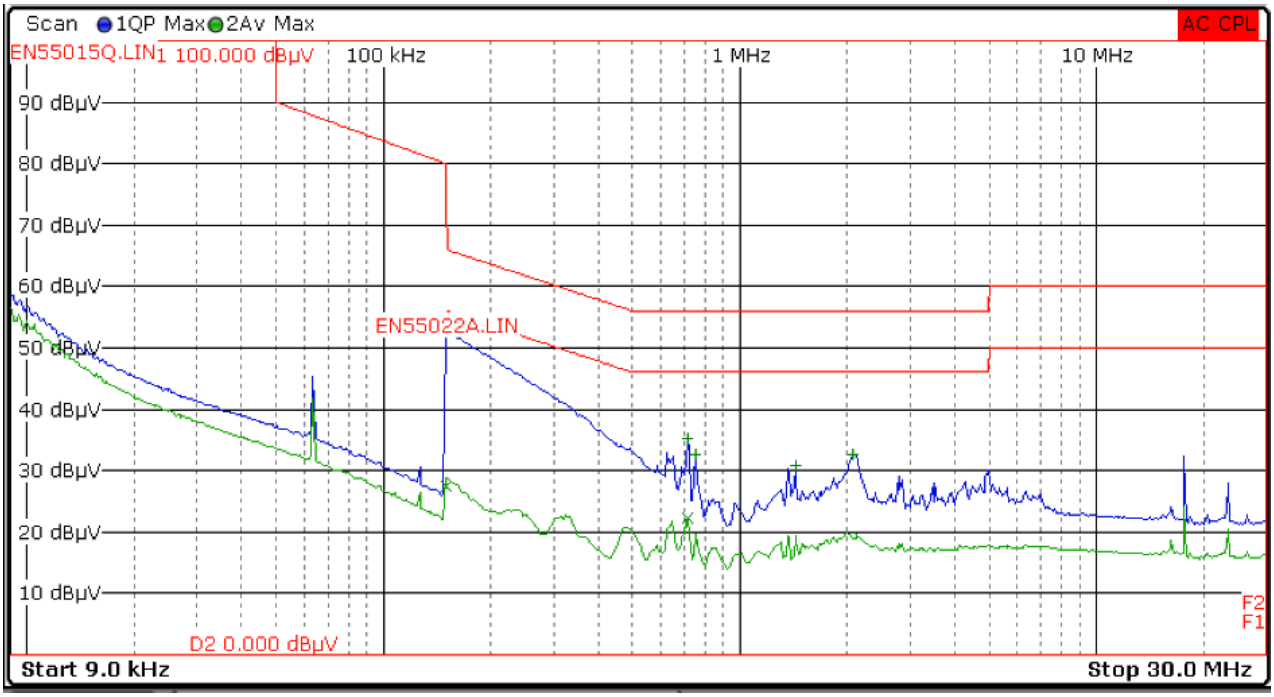

Figure 103 – EMI Scan Result at 115 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	150.0000 kHz	54.36 N	-11.64 dB
2 Average	150.0000 kHz	27.59 N	-28.41 dB
2 Average	712.5000 kHz	22.38 L1	-23.62 dB
1 Quasi Peak	717.0000 kHz	35.26 N	-20.74 dB
1 Quasi Peak	750.7500 kHz	32.59 L1	-23.41 dB
1 Quasi Peak	1.4325 MHz	30.86 N	-25.14 dB
1 Quasi Peak	2.0873 MHz	32.61 N	-23.39 dB

Figure 104 – EMI Scan Data / Reading at 115 VAC Line Input.

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15.1.2 Conducted EMI Scan at 230 VAC Input Line

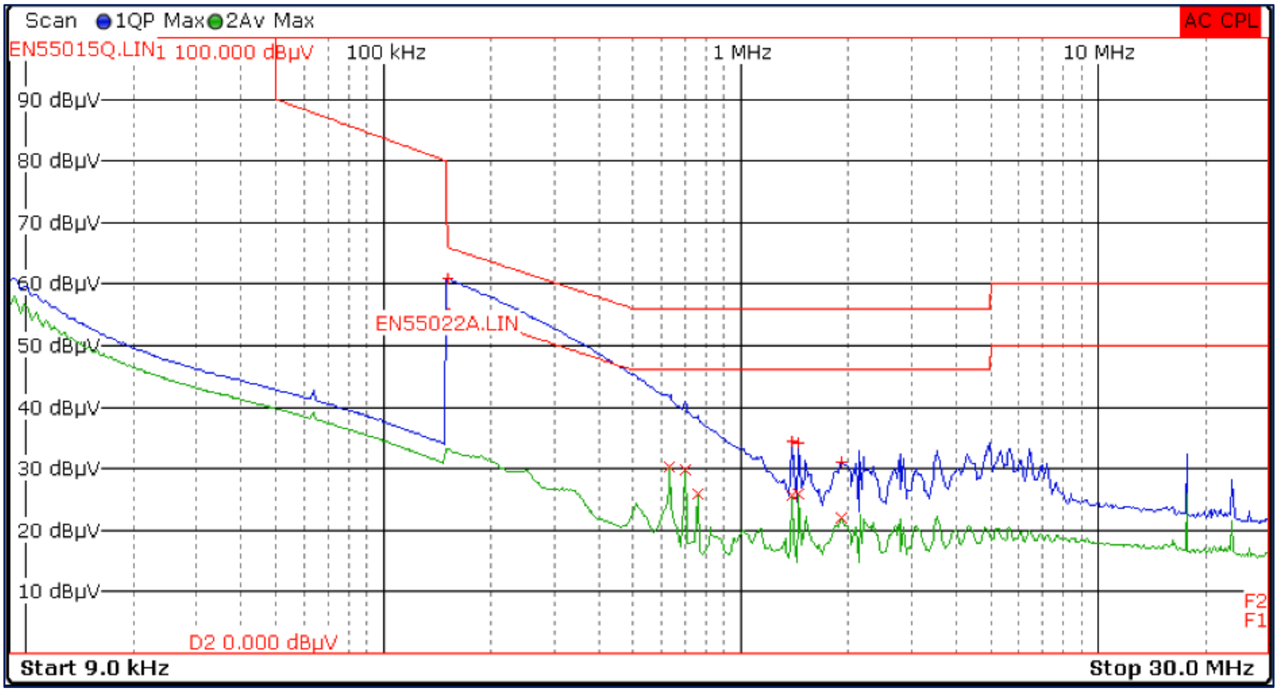

Figure 105 – EMI Scan Result at 230 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	152.2500 kHz	60.83 N	-5.05 dB
2 Average	633.7500 kHz	30.30 L1	-15.70 dB
2 Average	696.7500 kHz	29.76 L1	-16.24 dB
2 Average	759.7500 kHz	25.82 L1	-20.18 dB
1 Quasi Peak	1.3920 MHz	34.55 N	-21.45 dB
2 Average	1.3943 MHz	25.61 N	-20.39 dB
1 Quasi Peak	1.4550 MHz	34.07 N	-21.93 dB
2 Average	1.4573 MHz	26.03 N	-19.97 dB
2 Average	1.9073 MHz	22.09 N	-23.91 dB
1 Quasi Peak	1.9118 MHz	31.07 N	-24.93 dB

Figure 106 – EMI Scan Data / Reading at 230 VAC Line Input.

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15.2 Conducted EMI Scan with 1.5 A Resistive Load (With Artificial Hand)

15.2.1 Conducted EMI Scan at 115 VAC Input Line

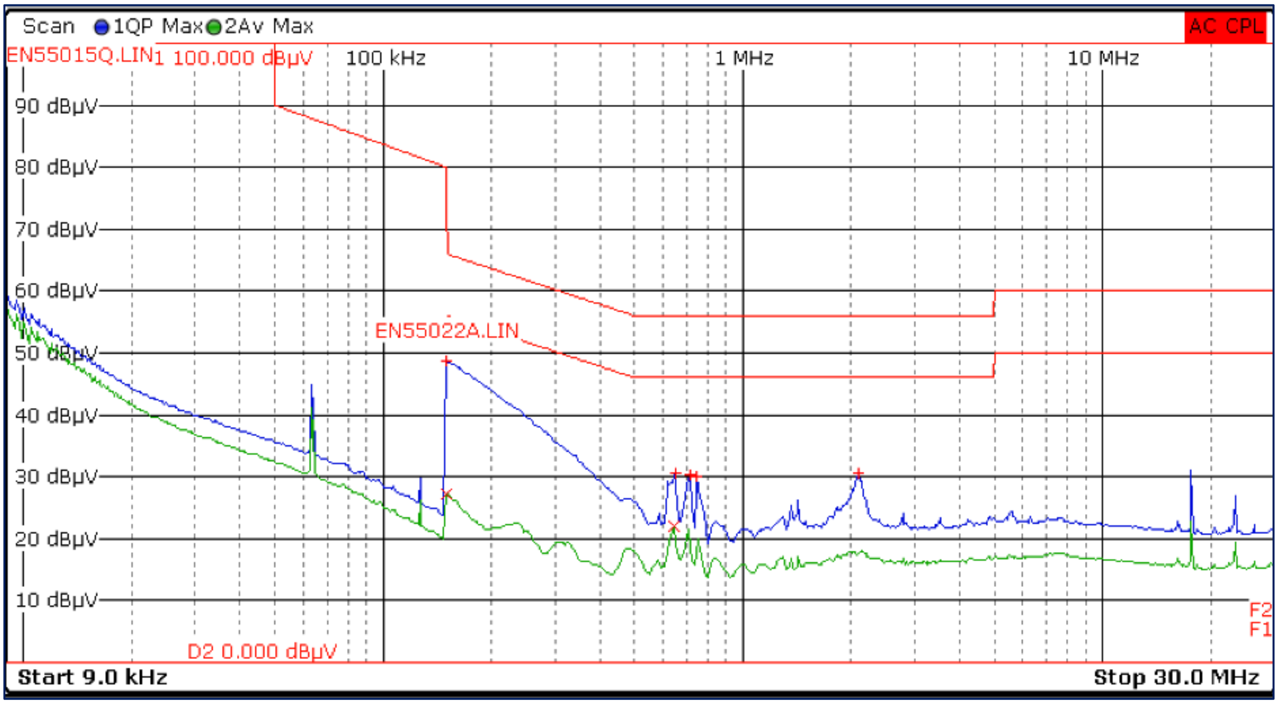

Figure 107 – EMI Scan Result at 115 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	150.0000 kHz	48.68 L1	-17.32 dB
2 Average	150.0000 kHz	27.18 L1	-28.82 dB
2 Average	647.2500 kHz	22.10 N	-23.90 dB
1 Quasi Peak	649.5000 kHz	30.54 N	-25.46 dB
1 Quasi Peak	714.7500 kHz	30.24 N	-25.76 dB
1 Quasi Peak	746.2500 kHz	30.00 N	-26.00 dB
1 Quasi Peak	2.1098 MHz	30.50 L1	-25.50 dB

Figure 108 – EMI Scan Data / Reading at 115 VAC Line Input.

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15.2.2 Conducted EMI Scan at 230 VAC Input Line

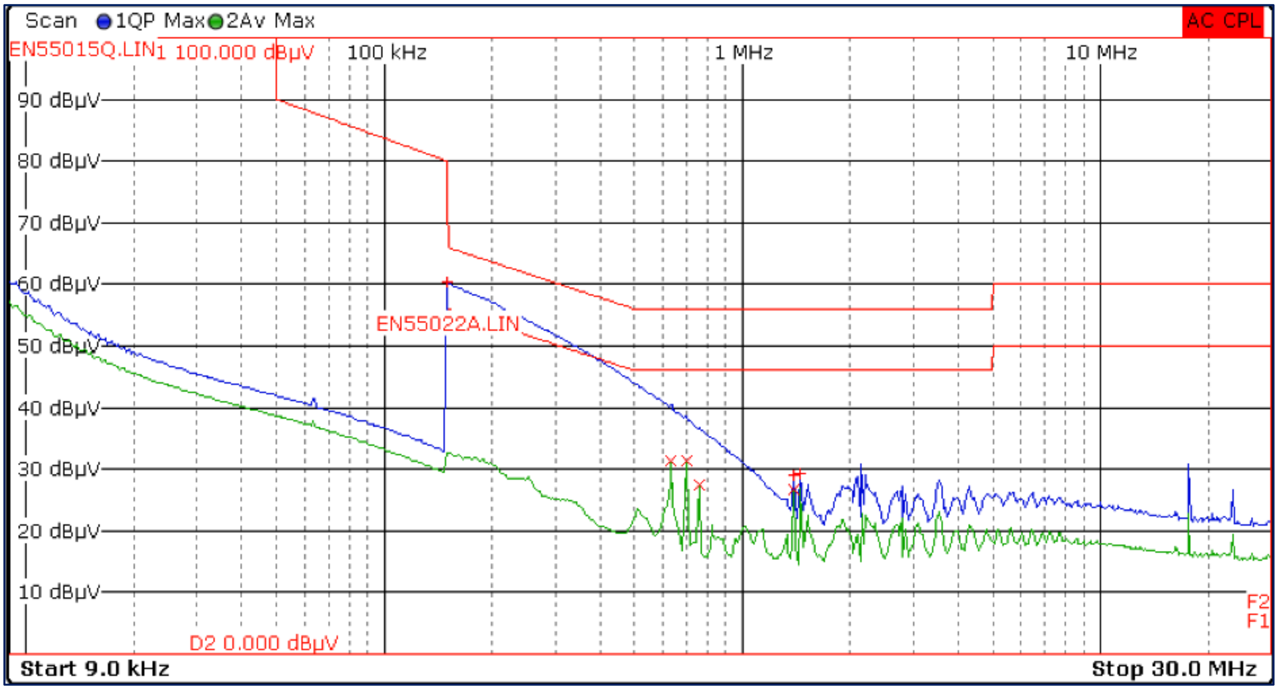

Figure 109 – EMI Scan Result at 230 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	150.0000 kHz	60.25 N	-5.75 dB
2 Average	633.7500 kHz	31.39 L1	-14.61 dB
2 Average	696.7500 kHz	31.23 L1	-14.77 dB
2 Average	759.7500 kHz	27.41 L1	-18.59 dB
1 Quasi Peak	1.3943 MHz	28.98 L1	-27.02 dB
2 Average	1.3943 MHz	26.57 L1	-19.43 dB
1 Quasi Peak	1.4573 MHz	29.37 L1	-26.63 dB

Figure 110 – EMI Scan Data / Reading at 230 VAC Line Input.

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15.3 Conducted EMI Scan with 1.5 A Resistive Load (With Earth)

15.3.1 Conducted EMI Scan at 115 VAC Input Line

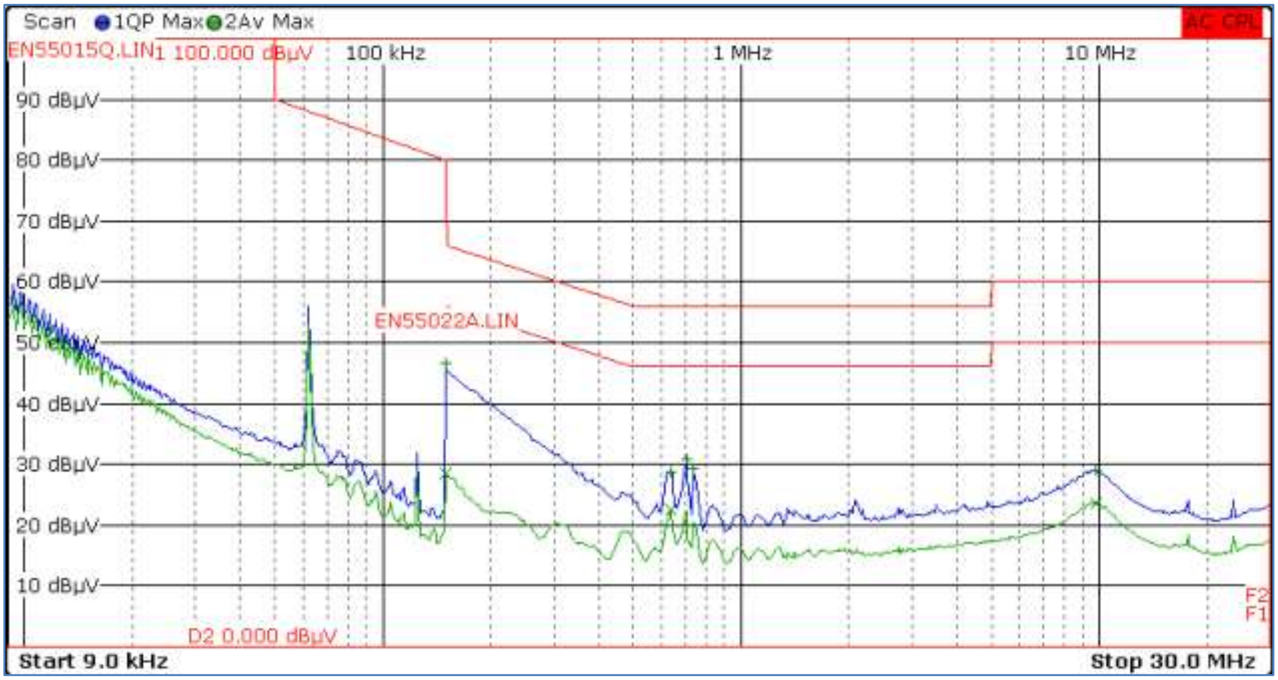

Figure 111 – EMI Scan Result at 115 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	150.0000 kHz	46.57 L1	-19.43 dB
2 Average	150.0000 kHz	28.50 L1	-27.50 dB
1 Quasi Peak	636.0000 kHz	28.88 N	-27.12 dB
2 Average	638.2500 kHz	22.46 N	-23.54 dB
1 Quasi Peak	705.7500 kHz	30.75 N	-25.25 dB
1 Quasi Peak	737.2500 kHz	29.30 N	-26.70 dB
1 Quasi Peak	9.7755 MHz	29.05 N	-30.95 dB
2 Average	9.8430 MHz	23.63 N	-26.37 dB

Figure 112 – EMI Scan Data / Reading at 115 VAC Line Input.

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15.3.2 Conducted EMI Scan at 230 VAC Input Line

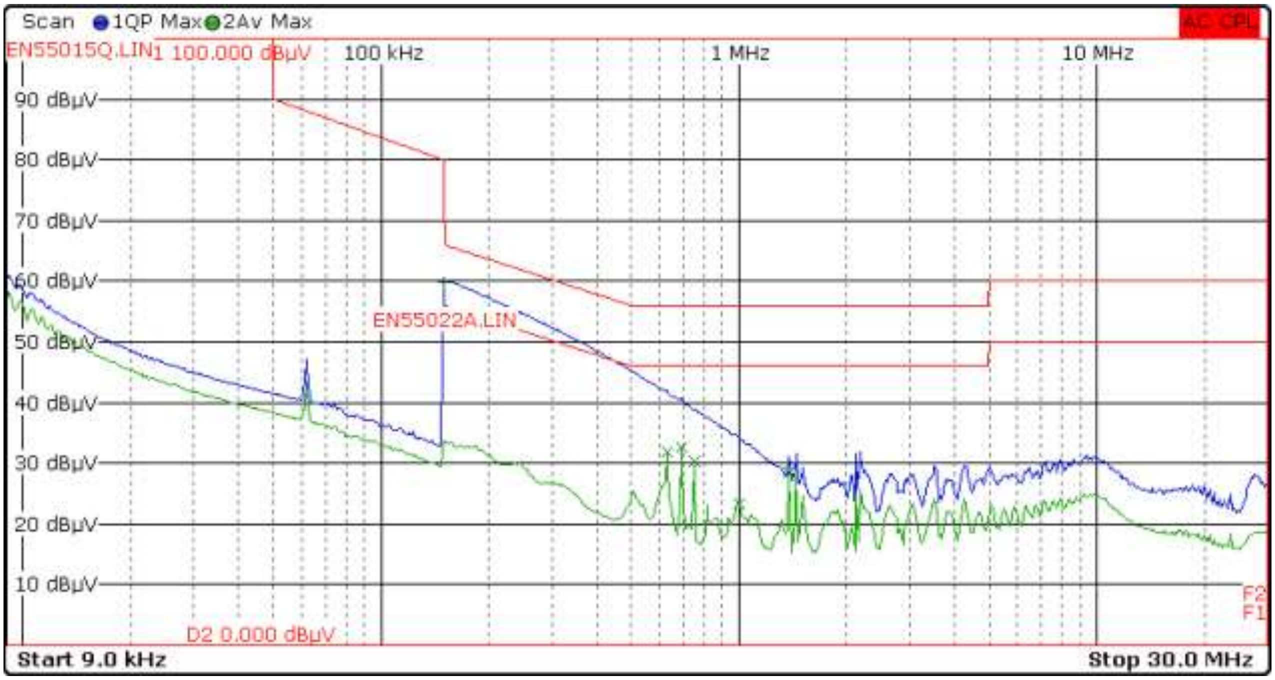

Figure 113 – EMI Scan Result at 230 VAC.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	150.0000 kHz	59.92 N	-6.08 dB
2 Average	629.2500 kHz	31.84 N	-14.16 dB
2 Average	690.0000 kHz	32.70 N	-13.30 dB
2 Average	753.0000 kHz	30.23 N	-15.77 dB
2 Average	998.2500 kHz	23.31 N	-22.69 dB
2 Average	1.3808 MHz	28.39 N	-17.61 dB

Figure 114 – EMI Scan Data / Reading at 230 VAC Line Input.

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15.4 Conducted EMI Test Set-up

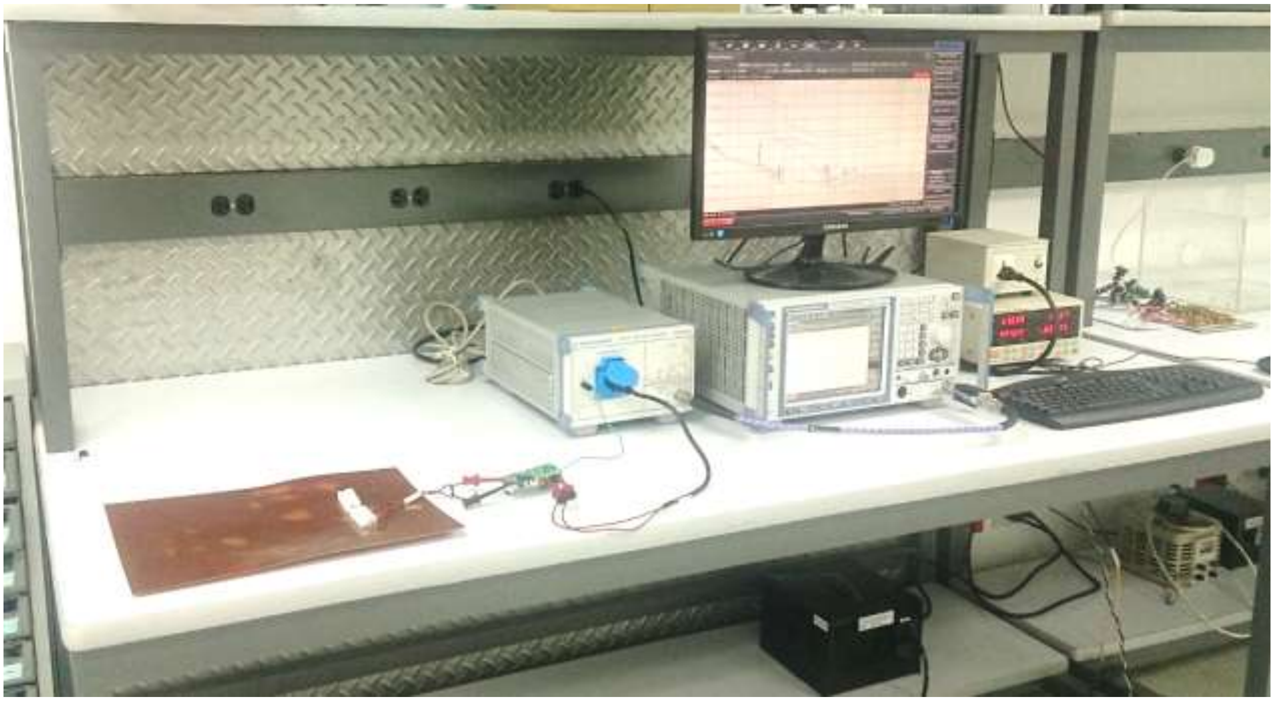

Figure 115 – Conducted EMI Test Set-up.

15.5 Equipment and Load Used and Test Condition

1. ROHDE & SCHWARZ ENV216 TWO LINE V-NETWORK
2. ROHDE & SCHWARZ ESRP EMI TEST RECEIVER
3. HIOKI 3322 POWER HiTESTER
4. CHROMA MEASUREMENT TEST FIXTURE
5. RESISTOR LOAD TO CATER 18W FULL LOAD POWER.
6. INPUT VOLTAGE SET AT 115 VAC AND 230 VAC.

16 Line Surge

The unit was subjected to ±6000 V, 100 kHz ring wave and ±1000 V differential surge test using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

16.1 Differential Surge Test Summary

Differential Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

16.2 Ring Wave Test Summary

Ring Wave Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+6000	230	L,N to PE	0	Pass
-6000	230	L,N to PE	0	Pass
+6000	230	L,N to PE	90	Pass
-6000	230	L,N to PE	90	Pass
+6000	230	L,N to PE	270	Pass
-6000	230	L,N to PE	270	Pass

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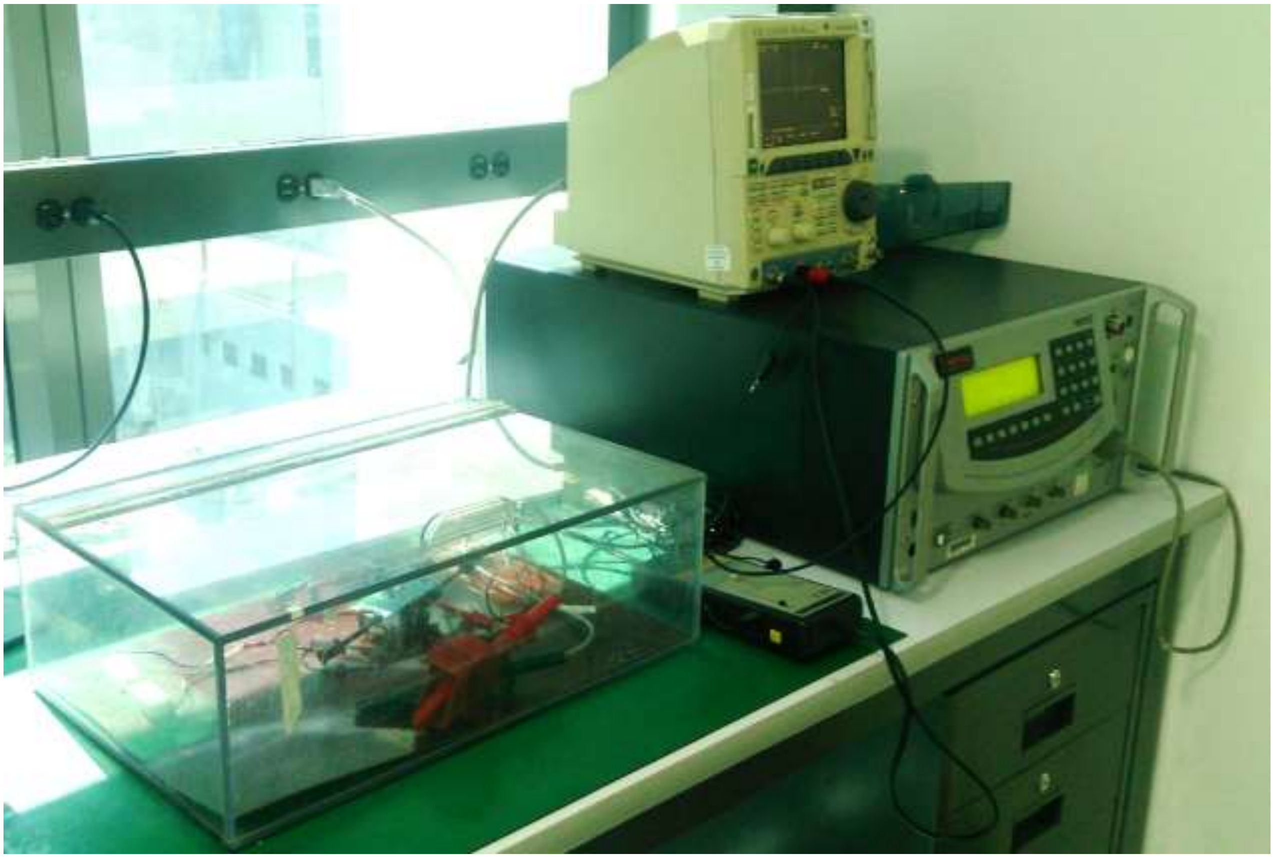
16.3 Line Surge Test Set-up



16.4 Equipment / Load Used and Test Condition

1. THERMO SCIENTIFIC SURGE TEST EQUIPMENT
2. YOKOGAWA DL1740 OSCILLOSCOPE
3. YOKOGAWA 701926 DIFFERENTIAL PROBE (FOR MEASURING DRAIN VOLTAGE)
4. RESISTOR LOAD TO CATER 18 W FULL LOAD POWER.
5. INPUT VOLTAGE SET AT 230 VAC.

17 ESD Test

17.1 ESD Test Result for Contact and Air Discharge

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
+8000	230	Contact	10	**Pass**
+15000	230	Air	10	**Pass**

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
-8000	230	Contact	10	**Pass**
-15000	230	Air	10	**Pass**

Note: The ESD test was performed for both the positive and negative rail of the main output (12 V main output rail and ground respectively).

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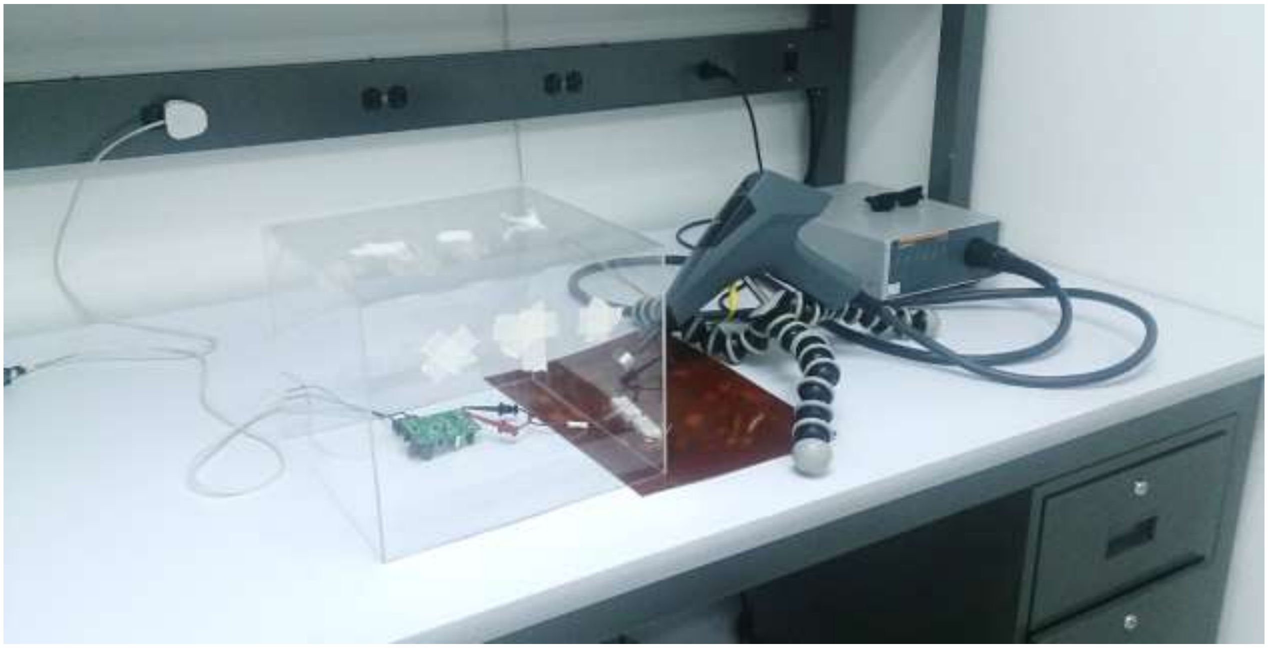
17.2 ESD Test Set-up



17.3 Equipment Used and Test Condition

1. Used EMTEST ESD equipment for the testing.
2. Line input is set at 230 VAC.
3. Total output power is 18 W using a resistive load.
4. Contact discharge test is set at ±8 kV for both the positive and negative rail of the 12 V output.
5. Air discharge test is set at ±15 kV for both the positive and negative rail of the 12 V output.

18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
11-Jan-17	JMQC	1.0	Initial Release	Mktg & Apps

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Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

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