Design Example Report

Title	*4.7 W Non-Dimmable, High Efficiency (>89%), Power Factor Corrected, Non-Isolated Buck LED Driver Using LYTSwitch™-1 LYT1602D*
Specification	185 VAC – 265 VAC Input; 90 V_{TYP}, 52 mA_{TYP} Output
Application	Candelabra
Author	Applications Engineering Department
Document Number	DER-542
Date	June 22, 2016
Revision	1.0

Summary and Features

- Single-stage power factor corrected, PF >0.9
- Accurate constant current regulation, ±5%
- Meets <30% flicker percent requirement
- Highly energy efficient, >89 % at 230 V
- Low cost and low component count for compact PCB solution
- Integrated Auto-restart protection features
  - No-load/ open-load output
  - Output short-circuit
  - Line surge or line overvoltage
- Thermal foldback for power reduction
- Over temperature shutdown with hysteretic automatic power recovery
- No damage during line brown-out or brown-in conditions
- Meets IEC 2.5 kV ring wave, 1 kV differential surge
- Meets EN55015 conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a low-component-count, non-isolated, non-dimmable LED driver in the Buck topology, designed to drive a 90 V LED voltage string at 52 mA output current from an input voltage range of 185 VAC to 265 VAC. The LED driver utilizes the LYT1602D from the LYTSwitch-1 family of devices.

LYTSwitch-1 is a SO-8 package LED driver controller IC designed for non-isolated buck topology applications. The LYTSwitch-1 provides high efficiency, high power factor and accurate LED current regulation. LYTSwitch-1 incorporates a high-voltage power MOSFET and Variable Frequency / Variable On-Time, Critical Conduction Mode Control Engine for tight current regulation, high power factor and proprietary FET utilization for high efficiency. The controller also integrates protection features such as input and output overvoltage protection, thermal fold-back, over temperature shutdown, output short-circuit and overcurrent protection.

DER-542 offers a compact size solution for 4.7 W LED drivers ideal for candelabra applications. The key design goals were high efficiency, accurate constant current regulation, and low component count.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet, and performance data.

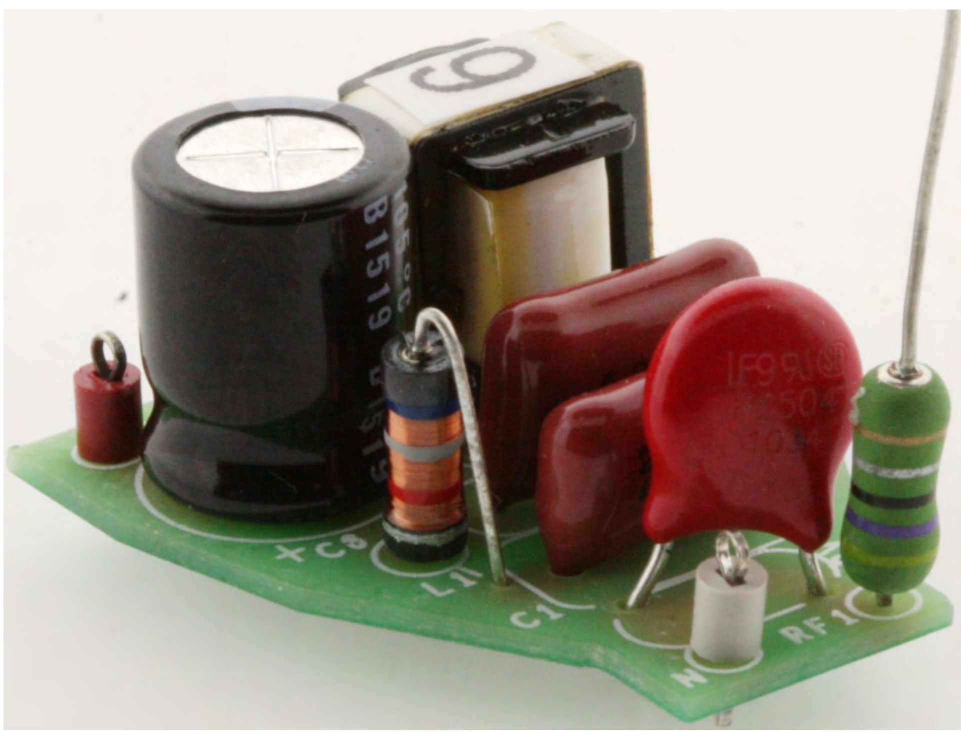

Figure 1 – Populated Circuit Board.

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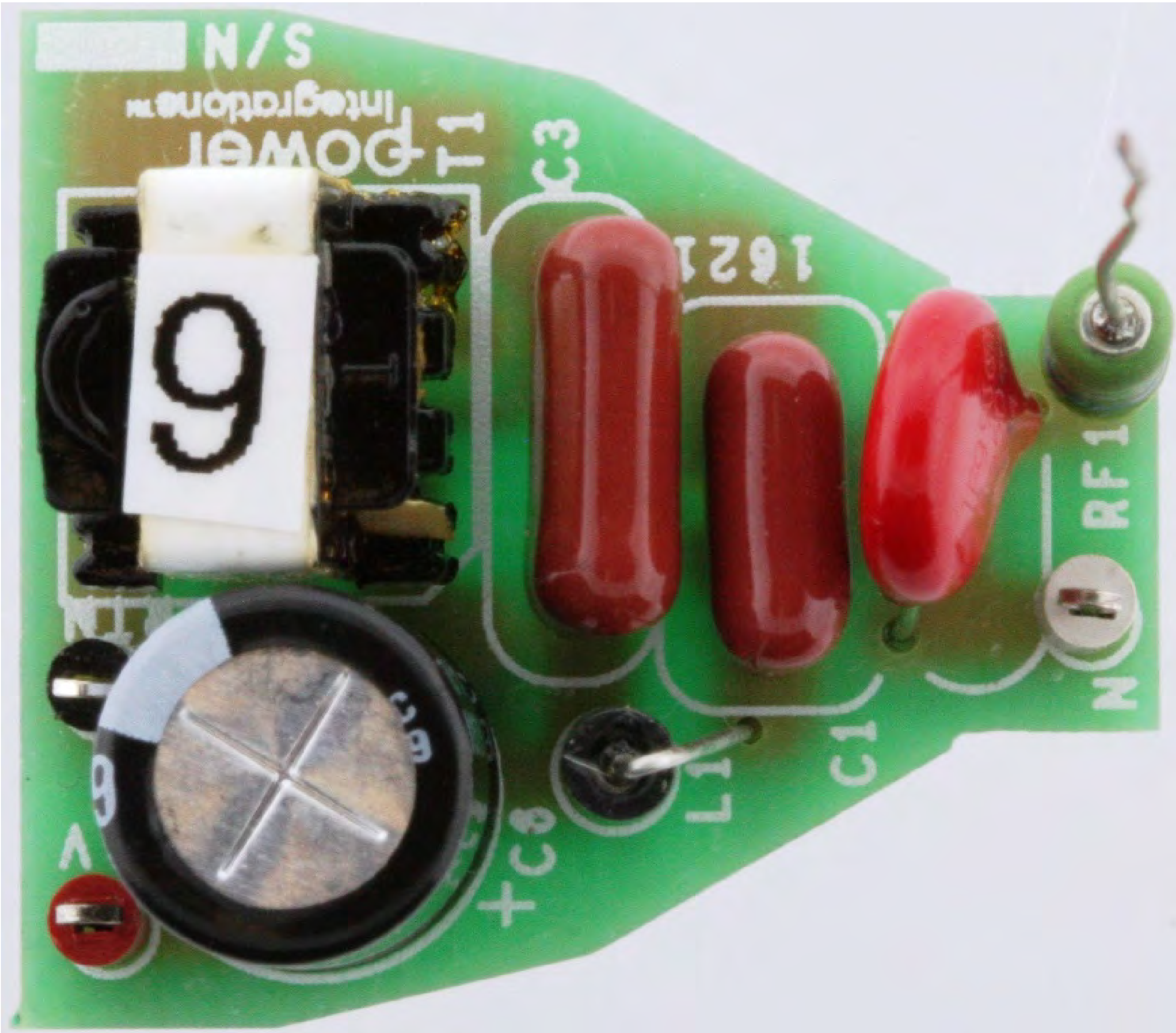

Figure 2 – Populated Circuit Board, Top View.

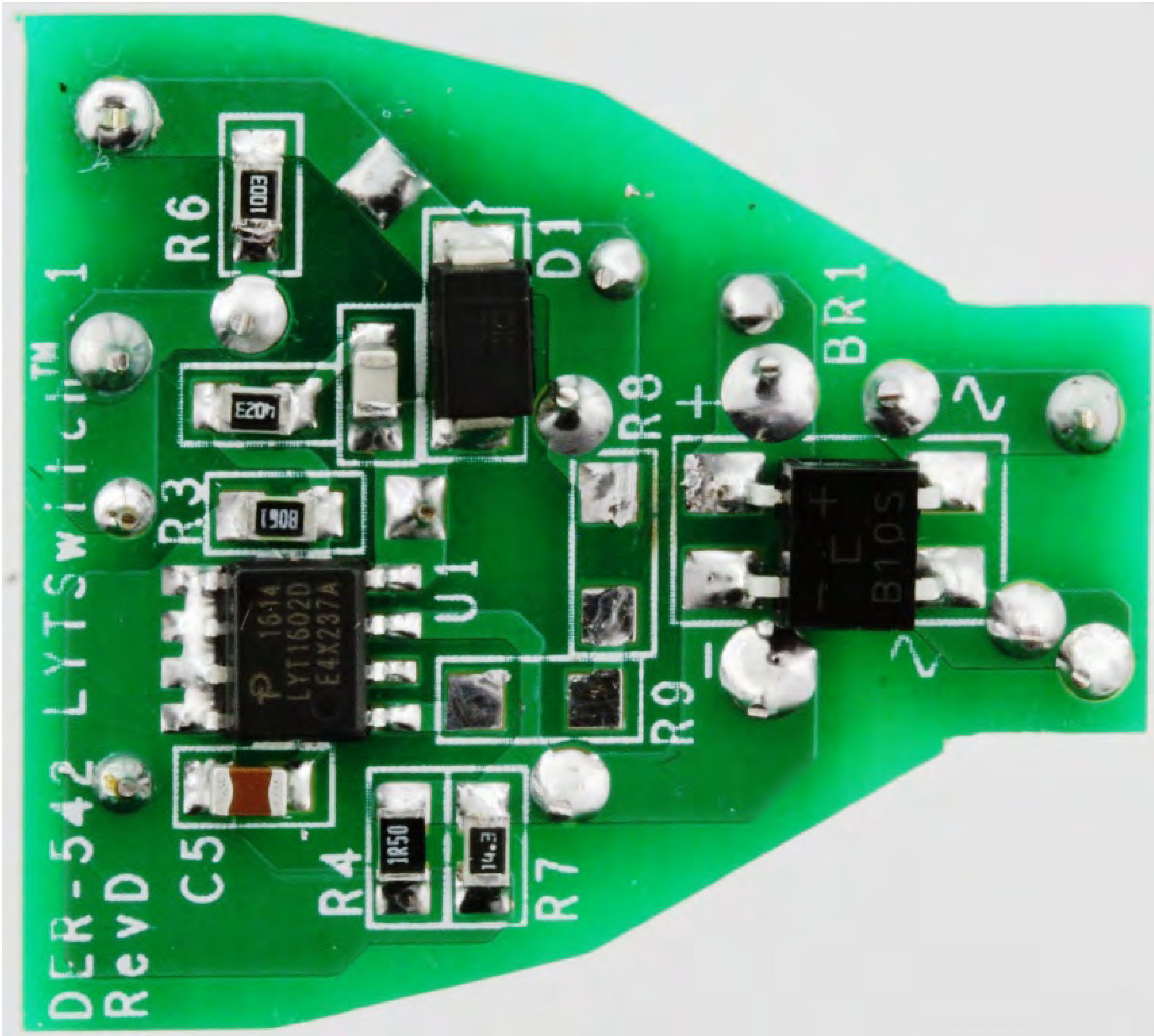

Figure 3 – Populated Circuit Board, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	185	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50		Hz	
Output						
Output Voltage	V_{OUT}		90		V	
Output Current	I_{OUT}		52		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		4.68		W	
Efficiency						
Full Load	η		89		%	230 V / 50 Hz at 25 ºC.
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Isolated				
Ring Wave (100 kHz)			2.5		kV	
Differential Mode (L1-L2)			1.0		kV	
Power Factor			0.9			Measured at230 VAC / 50 Hz.
Ambient Temperature	T_{AMB}		85		ºC	Free Convection, Sea Level.

3 Schematic

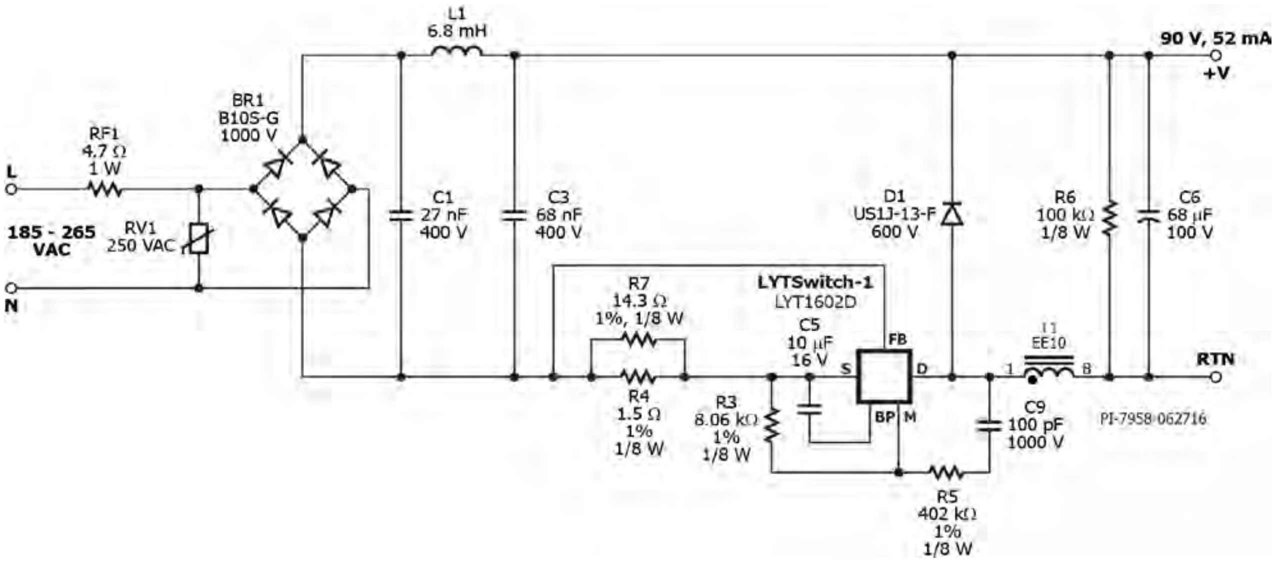

Figure 4 – Schematic.

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4 Circuit Description

The LYTSwitch-1 device (U1-LYT1602D) combines a high-voltage power FET and variable frequency / variable on-time, critical conduction mode controller in a single SO-8 package. The LYT1602D IC is configured to drive a 90 V output non-isolated buck LED driver with 52 mA constant current output. The LYT1602D device was selected from the power table based on maximum output power (10 W for high line) in the data sheet.

4.1 Input Stage

The input fuse RF1 provides safety protection. Varistor RV1 acts as a voltage clamp that limits the voltage spike on the primary during line transient voltage surge events. A 250 V rated part was selected, being slightly above the nominal specified operating input voltage (230 V). The AC input voltage is full wave rectified by BR1 to achieve good power factor and low THD. For higher surge requirement such as >1 kV, C2 and L1 can be placed before the bridge rectifier BR1, but a safety X-capacitor is required for C2.

4.2 EMI Filters

Inductor L1 serves as differential choke. Inductor L1, C1 and C3 capacitors form as an EMI pi filter which works to filter differential and common mode noise. LYTSwitch-1's variable frequency / on-time states and critical conduction code control engine limit RFI emission to significant level which enables design to use simple EMI pi filter even for high power bulb and tube applications.

4.3 LYTSwitch-1 Control Circuit

The LED driver circuit topology is a low side buck configuration, where the FET of U1 and the inductor L1 are connected to the ground rail. During the FET on-time, current ramps through the inductor winding storing energy in the form of magnetic field which is then delivered to the output load via flywheel diode D1 during the FET off-time.

The output capacitor C6 provides output voltage ripple filtering to minimize the output ripple current. To avoid long ghosting effect of light output after power off, resistor R6 preload discharges the output capacitor voltage below the LED voltage.

Capacitor C5 provides local decoupling for the BYPASS (BP) pin of U1, which provides power to the IC during the switch on time. The IC internal regulator draws power from high voltage DRAIN (D) pin and charge the bypass capacitor C5 during the power switch off time. The typical BP pin voltage is 5.22 V. To keep the IC operating normally especially during the dead zone, where $V_{IN} < V_{OUT}$, the value of capacitor should be large enough to keep the BP pin voltage above the $V_{BP(RESET)}$ value of 4.5 V. Recommended minimum value for the BP pin capacitor is 4.7 μF.

Constant output current regulation is achieved through the FEEDBACK (FB) pin directly sensing the drain current during the FET on-time using external current sense resistors

(R_{FB}) R4 and R7 and comparing the voltage drop to a fixed internal reference voltage (V_{FB_REF}) of absolute value 280 mV typical.

$$R_{FB} = V_{FB\_REF} / k \times I_{OUT}$$

Where: k is the ratio between I_{PK} and $I_{OUT;}$ such that k = 3 for LYT14xx, and k = 3.6 for LYT16xx.

Trimming R_{FB} may be necessary to center I_{OUT} at the nominal input voltage.

The MULTIFUNCTION (M) pin monitors the line for any line overvoltage event. When the internal MOSFET is in on-state, the M pin is shorted internally to SOURCE (S) pin in order to detect the rectified input line voltage derived for the voltage across the inductor, i.e. (V_{IN}-V_{OUT}) and current flowing out of the M pin is defined by resistor R5, thus line overvoltage detection is calculated as; where R5 is assumed to be 402 kΩ ±1%.

$$V_{LINE\_OVP} = I_{IOV} \times R5 + V_{OUT}$$

Once the measured current exceeds the input overvoltage threshold (I_{IOV}) of 1 mA typical, the IC will inhibit switching instantaneously and initiate auto-restart to protect the internal MOSFET of the IC.

The M pin also monitors the output for any overvoltage and undervoltage event. When the internal MOSFET is in off-state, the output voltage is monitored through a coupling capacitor C9 and divider resistors R5 and R3. When an output open-load condition occurs, the voltage at the M pin will rise abruptly and when it exceeds the threshold of 2.4 V, the IC will inhibit switching instantaneously and initiate auto-restart to limit the output voltage from further rising. The overvoltage cut-off is typically 120% of the output voltage, which is equivalent to 2 V at the M pin (V_{OUT_OVP} = V_{OUT} x 2.4 V / 2 V). Resistor R5 is set to a fixed value of 402 kΩ ±1% and R5 will determine the output overvoltage limit. Any output short-circuit at the output will be detected once the M pin voltage falls below the undervoltage threshold (V_{OUV}) of 1 V typical, then the IC will inhibit switching instantaneously and initiate auto-restart to limit the average input less than 1 W, preventing any components from overheating.

R3 can be calculated as follows:

$R3 = 2\ V \times R5 / (V_{OUT} - 2\ V)$; this is applicable only to low-side configuration buck.

Another function of the M pin is for zero current detection (ZCD). This is to ensure operation in critical conduction mode. The inductor demagnetization is sensed when the voltage across the inductor begins to collapse towards zero as flywheel diode D1 conduction expires.

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5 PCB Layout

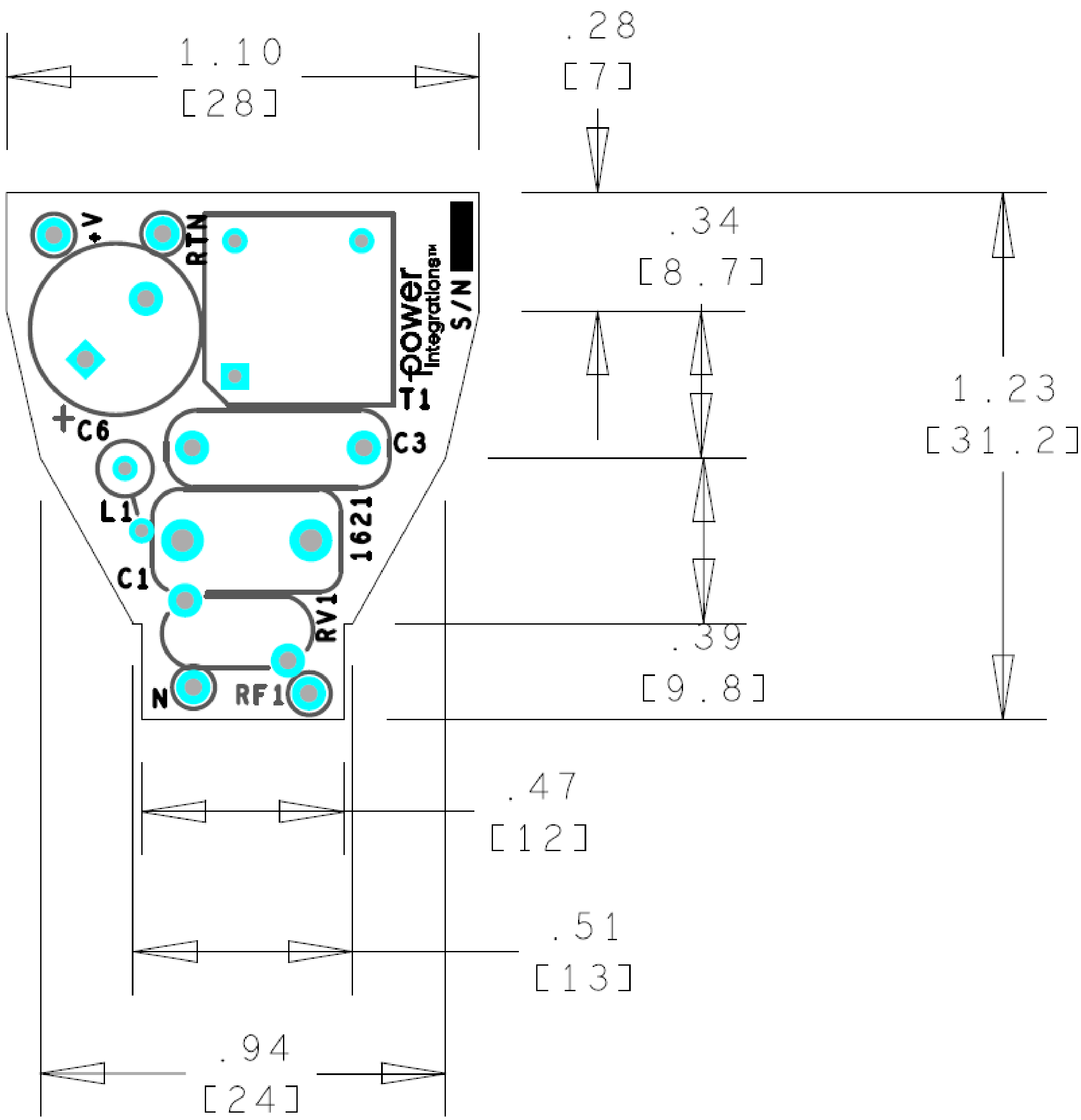

Figure 5 – Top Side.

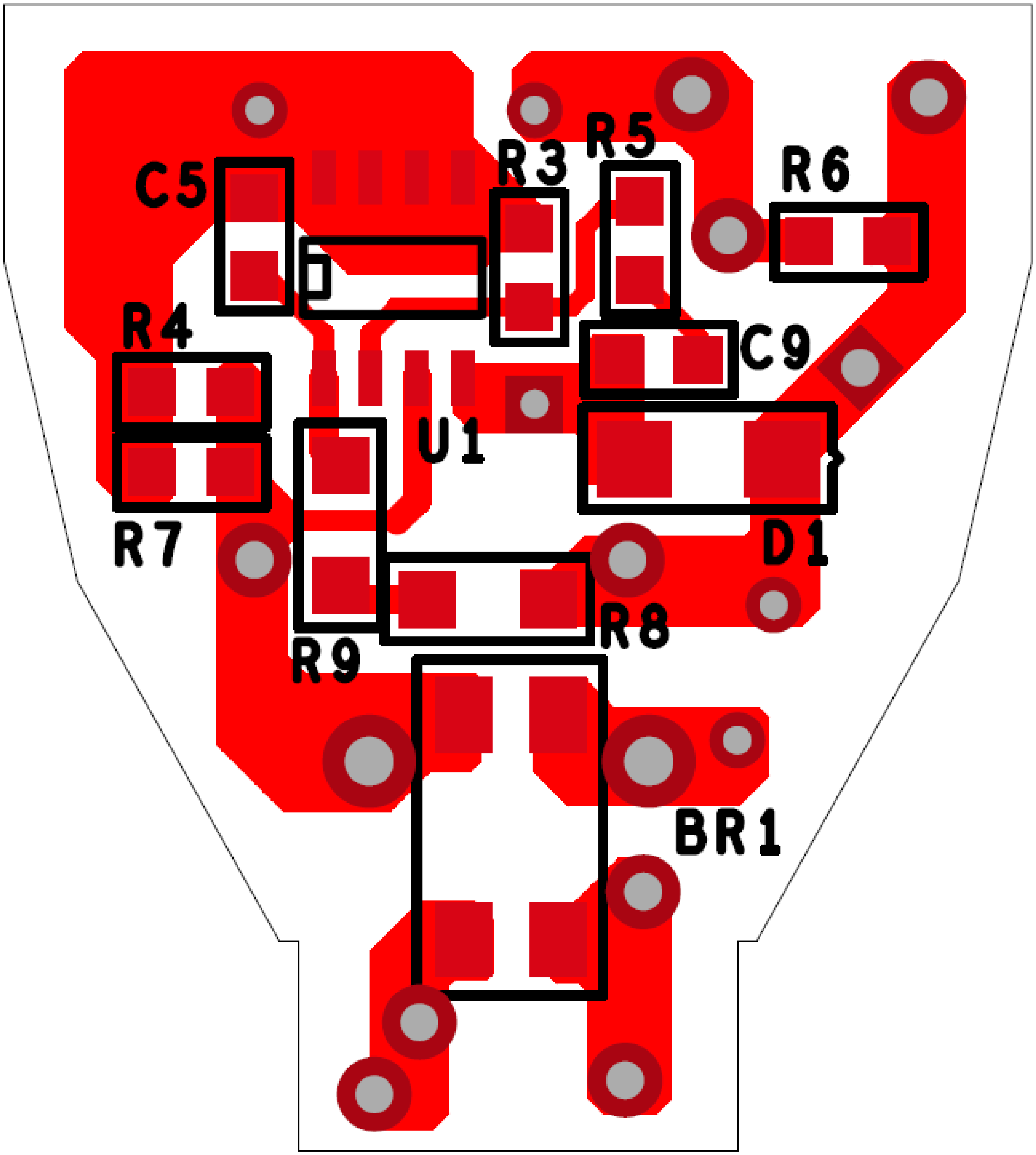

Figure 6 – Bottom Side.

Note: R8 and R9 were unstuffed (not populated).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	27 nF, 400 V, Film	ECQ-E4273KF	Panasonic
3	1	C3	68 nF, 400 V, Film	ECQ-E4683KF	Panasonic
4	1	C5	10µF, ±10%, 16V, X7R, Ceramic Capacitor	CL21B106KOQNNNG	Samsung
5	1	C6	68 µF,100 V, Electrolytic, (10 x 12.5)	UVY2A680MPD	Nichicon
6	1	C9	100 pF, 1000 V, Ceramic, NPO, 0805	C0805C101MDGACTU	Kemet
7	1	D1	Diode Ultrafast, SW 600 V, 1 A, SMA	US1J-13-F	Diodes, Inc.
8	1	L1	FIXED IND, 6.8 mH, 59 mA, 60 Ω, TH	AIAP-01-682K-T	Abracon
9	1	R3	RES, 8.06 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8061V	Panasonic
10	1	R4	RES, 1.5 Ω, 1%, 1/8 W, Thick Film, 0805	MCR10ERTFL1R50	Rohm Semi
11	1	R5	RES, 402 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4023V	Panasonic
12	1	R6	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
13	1	R7	RES, 14.3 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF14R3V	Panasonic
14	1	RF1	RES, 4.7 Ω, 1 W, Fusible/Flame Proof Wire Wound	FKN1WSJR-52-4R7	Yago
15	1	RV1	250 V, 21 J, 7 mm, RADIAL LA	V250LA4P	Littlefuse
16	1	T1	Bobbin, EE10, Vertical, 8 pins (10.2 mm W x 10.4 mm L x 9.7 mm H)	EE-1016	Yulongxin
17	1	U1	LYTSwitch-1, Wide Range, 4W, 45V-65V, SO-8	LYT1602D	Power Integrations

7 Inductor Specification

7.1 Electrical Diagram

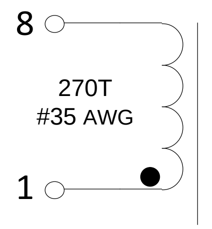

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 8, with all other windings open.	3300 μH
Tolerance	Tolerance of Primary Inductance.	±10%

7.3 Material List

Item	Description
[1]	Core: EE10.
[2]	Bobbin, EE10, Vertical, 8 pins, Part no. 25-01068-00.
[3]	Magnet Wire: #35 AWG.
[4]	Polyester tape: 7 mm.
[5]	Transformer tape: 4 mm.

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7.4 Inductor Build Diagram

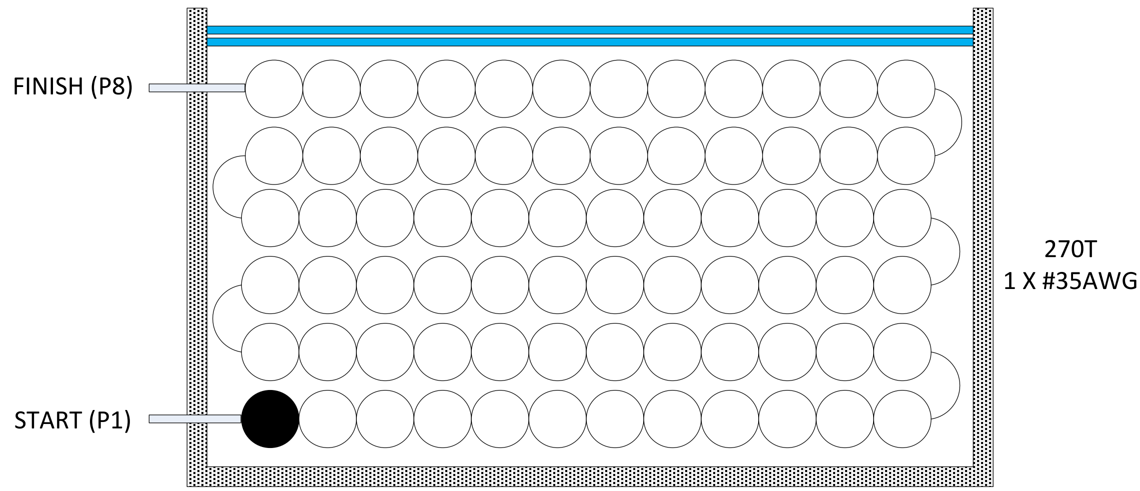
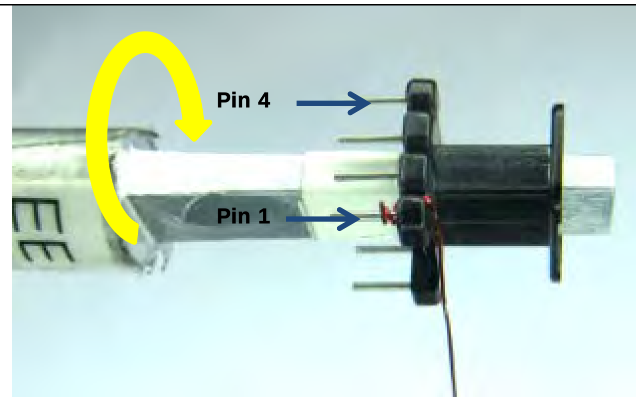
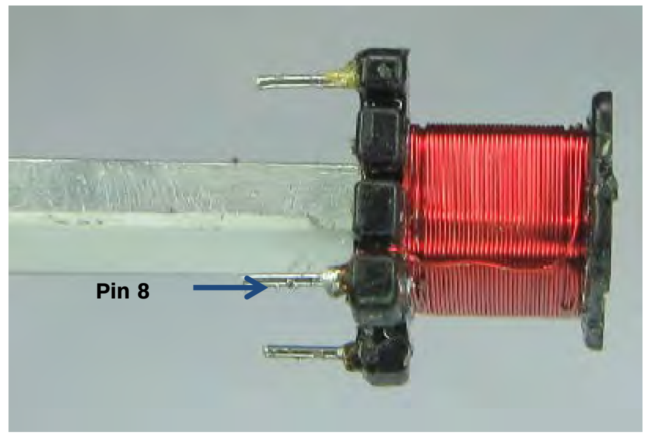
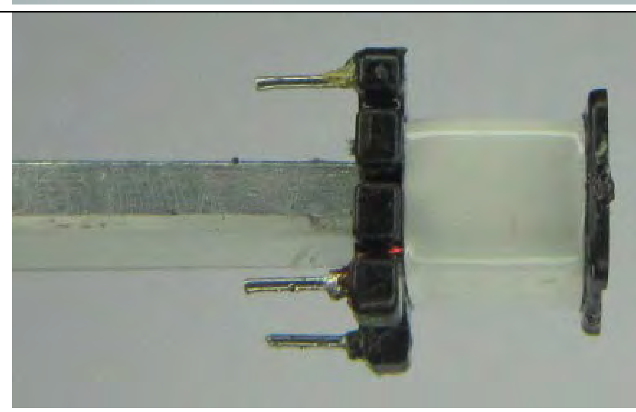


Figure 8 – Transformer Build Diagram.

7.5 Inductor Construction

Winding Directions	Bobbin is oriented on winder jig such that terminal pin 1-4 is in the left side. The winding direction is clockwise as shown in the figure.
Winding 1	Use wire item [3], start at pin 1 and wind 270 turns, then finish the winding on pin 8.
Insulation	Add 2 layer of tape, item [4], for insulation.
Terminal Pins	Pull out terminal pins 2-4 and pin 6-7.
Core Grinding	Grind the center leg of one core until it meets the nominal inductance of 3300 μH.
Core Assembly	Assemble the 2 cores on the bobbin with the ungapped core place on the terminal pin side as shown in the figure. Wrap the 2 cores with polyester tape item (5).
Finish	Dip the transformer assembly in 2:1 thinner and varnish solution.

7.6 Winding Illustrations

Winding Directions Bobbin is oriented on winder jig such that terminal pin 1-4 is in the left side. The winding direction is clockwise as shown in the figure.	
Winding 1 Use wire item [3], start at pin 1 and wind 270 turns, then finish the winding on pin 8.	
Insulation Add 2 layer of tape, item [4], for insulation.	

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Terminal Pins

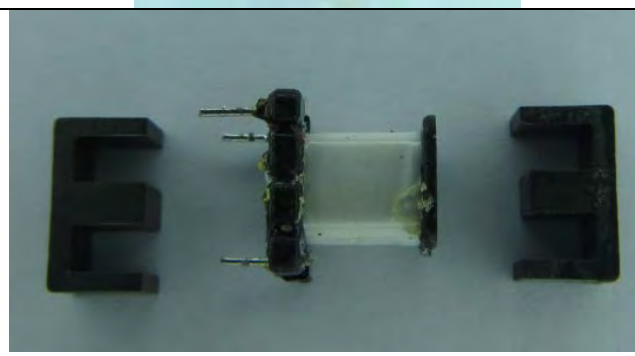
Pull out terminal pins 2-4 and pin 6-7.

Core Grinding

Grind the center leg of one core until it meets the nominal inductance of 3300 μH.

Core Assembly

Assemble the 2 cores on the bobbin with the ungapped core place on the terminal pin side as shown in the figure.



Wrap the 2 cores with polyester tape item (5).

Finish

Dip the transformer assembly in 2:1 thinner and varnish solution.

8 Inductor Design Spreadsheet

ACDC_LYTSwitch1_ Buck_031816; Rev.0.1; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-1 Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			High Line		AC line voltage range
VACMIN	185		185	V	Minimum AC line voltage
VACTYP	230		230	V	Typical AC line voltage
VACMAX	265		265	V	Maximum AC line voltage
FL	50		50	Hz	AC mains frequency
VO	90		90	V	Output Voltage
IO	52		52	mA	Average output current specification
EFFICIENCY			0.90		Efficiency estimate
PO			4.68	W	Continuous output power
VD			0.70	V	Output diode forward voltage drop
OPTIMIZATION PARAMETER	THD		THD		BOM selects IC with lowest peak current. THD selects IC for lowest THD.
ENTER LYTSWITCH-1 VARIABLES					
DEVICE BREAKDOWN VOLTAGE			725	V	This Spreadsheet supports 725V device only
DEVICE	LYT1602D		LYT1602D		Actual LYTSwitch-1 device
ILIMITMIN			0.59	A	Minimum Current Limit
ILIMITTYP			0.65	A	Typical Current Limit
ILIMITMAX			0.70	A	Maximum Current Limit
TON			2	us	On-time during the fixed on-time region at VACTYP
FSW			105	kHz	Maximum switching frequency in the fixed current limit region at VACTYP
DMAX			0.64		Maximum duty cycle possible in the fixed on-time region
DEVICE BREAKDOWN VOLTAGE			725	V	This Spreadsheet supports 725V device only
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
CORE	EE10		EE10		Enter Transformer Core
CUSTOM CORE NAME					If custom core is used - Enter part number here
AE			12.10	mm^2	Core effective cross cectional area
LE			26.10	mm	Core effective path length
AL			850.00	nH/turn^2	Core ungapped effective inductance
AW			11.88	mm^2	Window Area of the bobbin
BW			6.60	mm	Bobbin physical winding width
LAYERS			8.0		Number of Layers
INDUCTOR DESIGN PARAMETERS					
LP_MIN			1486	uH	Absolute minimum design inductance
LP_TYP	3300		3300	uH	Typical design inductance
LP_TOLERANCE			10	%	Tolerance of the design inductance
LP_MAX			29997	uH	Absolue maximum design inductance
TURNS	270		270	Turns	Number of inductor turns
ALG			45.27	nH/turn^2	Inductance per turns squared
BMAX			2496	Gauss	Actual saturation flux density in the fixed peak current region
BAC			1850	Gauss	AC flux density in the fixed peak current region
LG			0.318	mm	Core air gap
BWE			52.80	mm	Effective bobbin width
OD			0.20	mm	Outer diameter of the wire with insulation
INS			0.04	mm	Wire insulation
DIA			0.15	mm	Outer diameter of the wire without insulation
AWG			35		AWG of the bare wire.

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CM			32	Cmils	Bare wire circular mils
CMA			479	Cmils/A	Bare wire circular mils per ampere
CURRENT DENSITY			2.2	A/mm^2	Bare wire current density
BOBBIN FILL FACTOR			86.91%		Area of the bobbin occupied by wire
CURRENT WAVEFORM SHAPE PARAMETERS					
IAVERAGE_INDUCTOR			0.04	A	Average inductor current at VACTYP obtained from half-line cycle emulation
IPEAK_MOSFET			0.19	A	MOSFET peak current at VACTYP when operating in the current limit region
IRMS_MOSFET			0.04	A	MOSFET RMS current at VACTYP obtained from half-line cycle emulation
IRMS_DIODE			0.06	A	Diode RMS current at VACTYP obtained from half-line cycle emulation
IRMS_INDUCTOR			0.07	A	Inductor RMS current at VACTYP obtained from half-line cycle emulation
LYTSWITCH EXTERNAL COMPONENTS					
FB Pin Resistor					
RFB_T			1.496	Ohms	Theoretical calculation of the feedback pin sense resistor
RFB			1.500	Ohms	Standard 1% value of the feedback pin sense resistor
M Pin Components					
BUCK_CONFIG	Low Side Buck				Buck Topology Switch Configuration
RUPPER			402.00	kOhms	Upper resistor on the M-pin divider network (E96 / 1%)
RLOWER	8.06		8.06	kOhms	Lower resistor on the M-pin divider network (E96 /1%)
VO_OVP		Info1	121.4	V	!!Info1. The VO_OVP is 1.35 * VO.
Line_OVP			492	V	Line overvoltage threshold
CC			100	pF	Coupling Capacitor for Low Side Buck Configuration
RPRELOAD			90	kOhms	Minimum Output Preload Resistor
VOLTAGE STRESS PARAMETERS					
VDRAIN			375	V	Estimated worst case drain voltage
PIVD			375	V	Output Rectifier Maximum Peak Inverse Voltage

9 Performance Data

All measurements were performed at room temperature using an LED load string. A 1-minute soak time was applied for each input voltage before measurement.

9.1 Efficiency

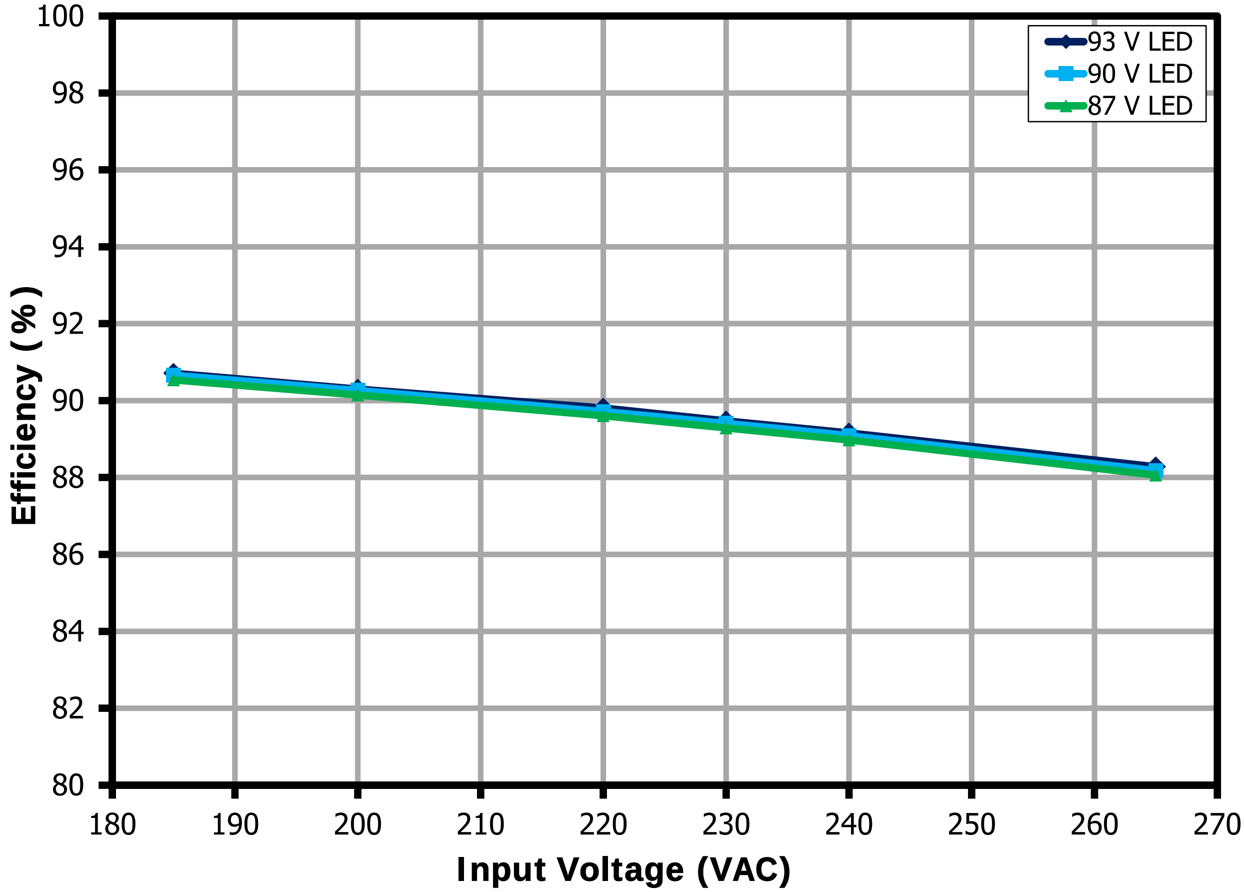

Figure 9 – Efficiency vs. Line and LED Load.

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9.2 Line Regulation

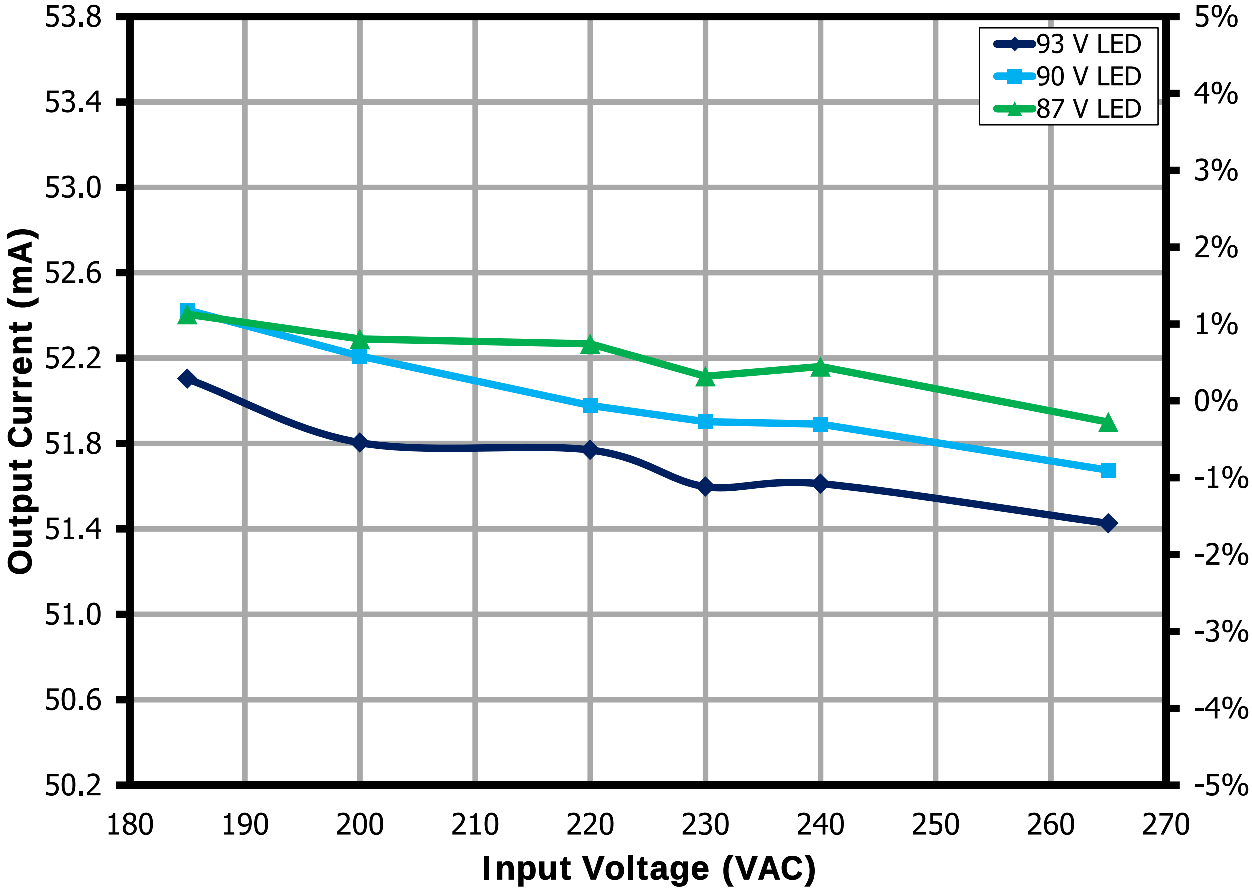

Figure 10 – Regulation vs. Line and LED Load.

9.3 Power Factor

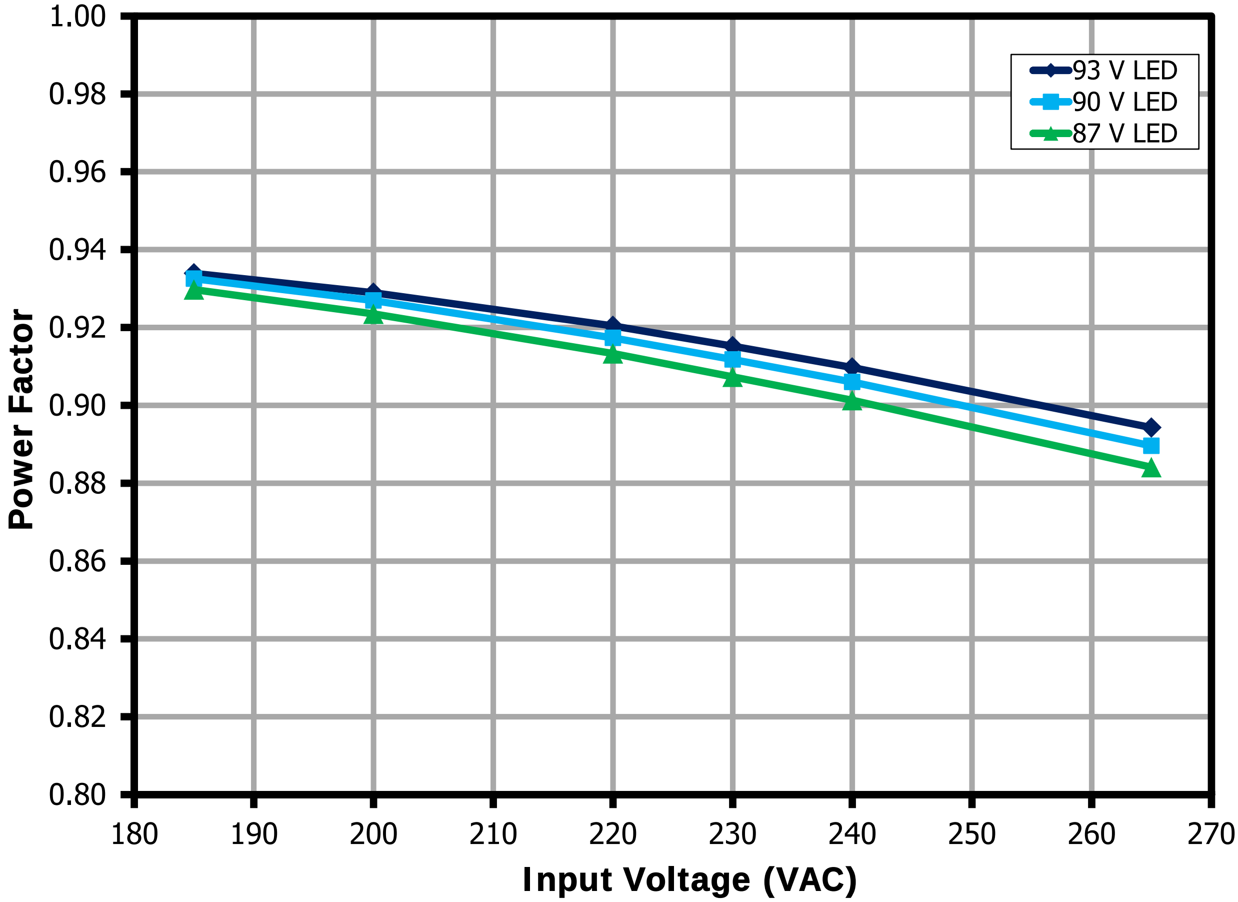

Figure 11 – Power Factor vs. Line and LED Load.

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9.4 %ATHD

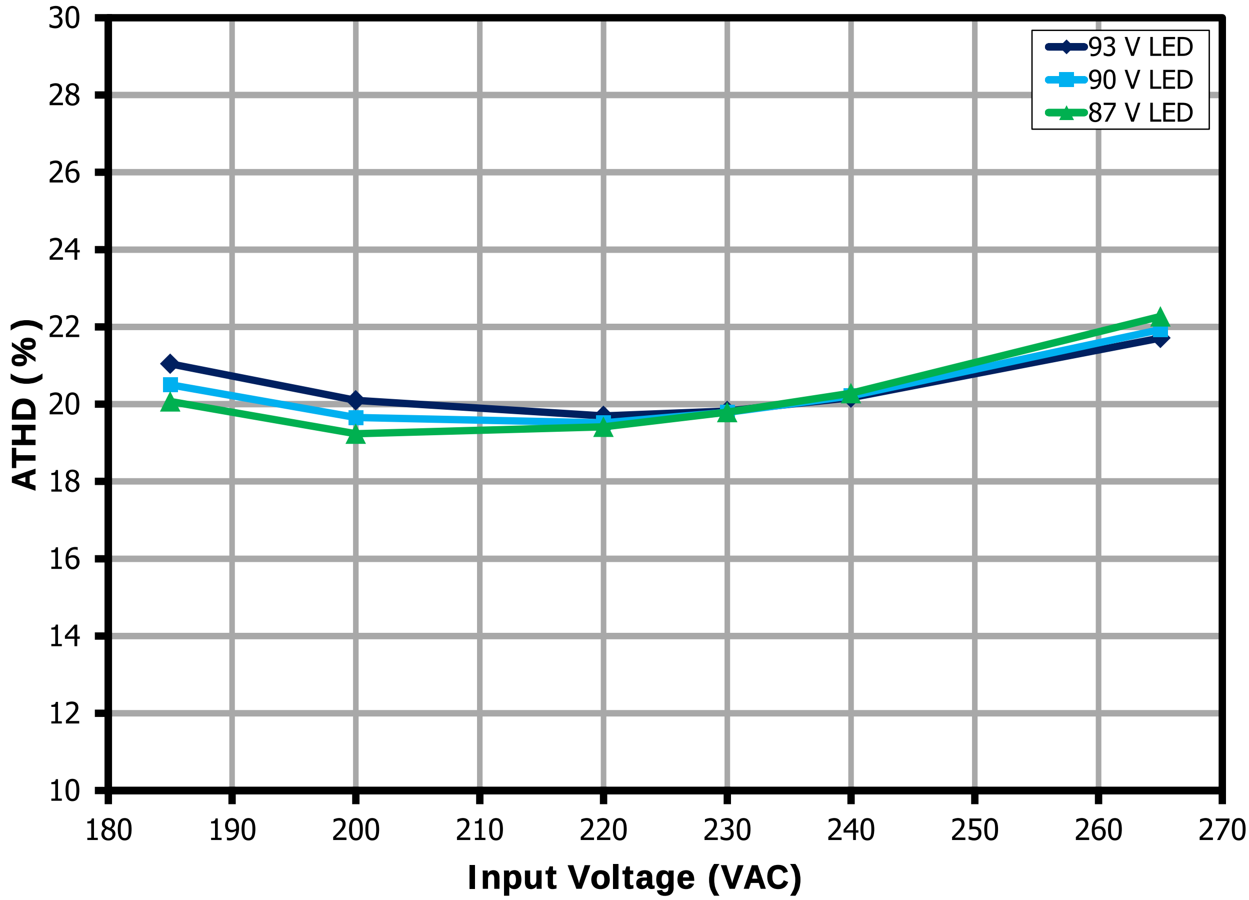

Figure 12 – %ATHD vs. Line and LED Load.

9.5 Individual Harmonic Content

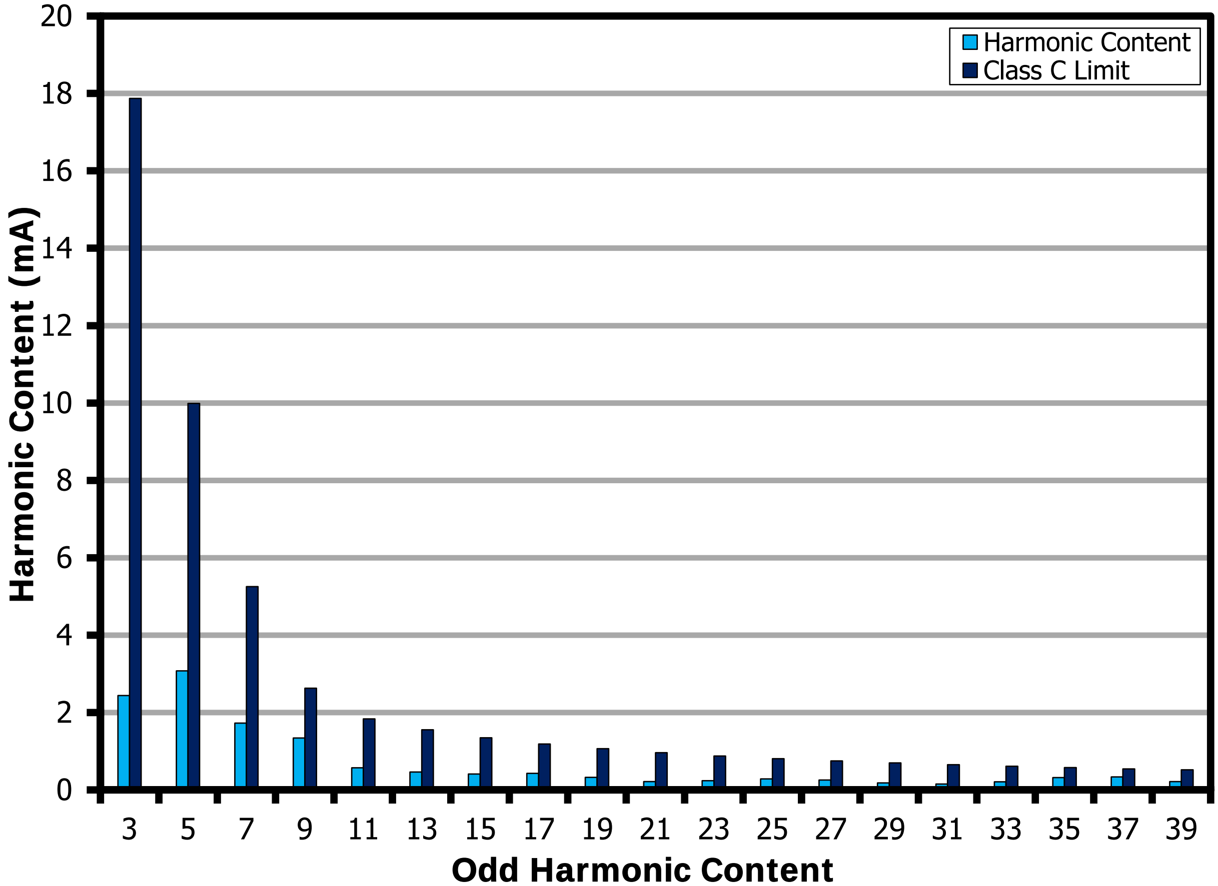

Figure 13 – 90 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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10 Test Data

10.1 Test Data – 93 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
185	50	184.94	31.07	5.37	0.934	21.04	93.28	52.10	4.87	90.71
200	50	199.93	28.83	5.35	0.929	20.10	93.19	51.80	4.83	90.30
220	50	219.96	26.57	5.38	0.920	19.69	93.17	51.77	4.83	89.81
230	50	229.98	25.55	5.38	0.915	19.82	93.13	51.60	4.81	89.47
240	50	240.00	24.72	5.40	0.910	20.17	93.11	51.61	4.81	89.16
265	50	265.02	22.91	5.43	0.894	21.71	93.08	51.43	4.79	88.28

10.2 Test Data – 90 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
185	50	184.94	30.43	5.25	0.933	20.50	90.62	52.43	4.76	90.66
200	50	199.92	28.30	5.24	0.927	19.65	90.52	52.21	4.73	90.26
220	50	219.96	26.01	5.25	0.917	19.52	90.47	51.98	4.71	89.71
230	50	229.98	25.07	5.26	0.912	19.79	90.43	51.90	4.70	89.41
240	50	240.00	24.25	5.27	0.906	20.21	90.40	51.89	4.70	89.09
265	50	265.01	22.49	5.30	0.890	21.93	90.36	51.68	4.68	88.18

10.3 Test Data – 87 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
185	50	184.95	29.54	5.08	0.930	20.07	87.59	52.41	4.60	90.54
200	50	199.93	27.55	5.09	0.924	19.24	87.54	52.29	4.58	90.15
220	50	219.96	25.45	5.11	0.913	19.41	87.53	52.27	4.58	89.61
230	50	229.98	24.51	5.12	0.907	19.79	87.50	52.12	4.57	89.29
240	50	240.00	23.75	5.14	0.901	20.28	87.50	52.16	4.57	88.98
265	50	265.02	22.03	5.16	0.884	22.27	87.47	51.90	4.55	88.06

10.4 Test Data, Harmonic Content at 230 VAC with 90 V LED Load

V_{IN} (V_{RMS})	Freq	I_{IN} (mA_{RMS})	P_{IN} (W)	%THD
230	50	98.09	21.430	19.107
nth Order	**mA Content**	**% Content**	**mA Limit <25 W**	**Remarks**
1	23.32			
2	0.02	0.08%		
3	2.44	10.45%	17.87	Pass
5	3.08	13.21%	9.99	Pass
7	1.73	7.40%	5.26	Pass
9	1.34	5.76%	2.63	Pass
11	0.57	2.45%	1.84	Pass
13	0.47	2.00%	1.56	Pass
15	0.41	1.76%	1.35	Pass
17	0.43	1.85%	1.19	Pass
19	0.33	1.41%	1.07	Pass
21	0.22	0.93%	0.96	Pass
23	0.24	1.04%	0.88	Pass
25	0.29	1.22%	0.81	Pass
27	0.26	1.11%	0.75	Pass
29	0.18	0.78%	0.70	Pass
31	0.15	0.65%	0.65	Pass
33	0.21	0.91%	0.61	Pass
35	0.32	1.37%	0.58	Pass
37	0.34	1.45%	0.55	Pass
39	0.22	0.94%	0.52	Pass

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11 Thermal Performance

11.1 Thermal Performance Scan – Open Frame Unit

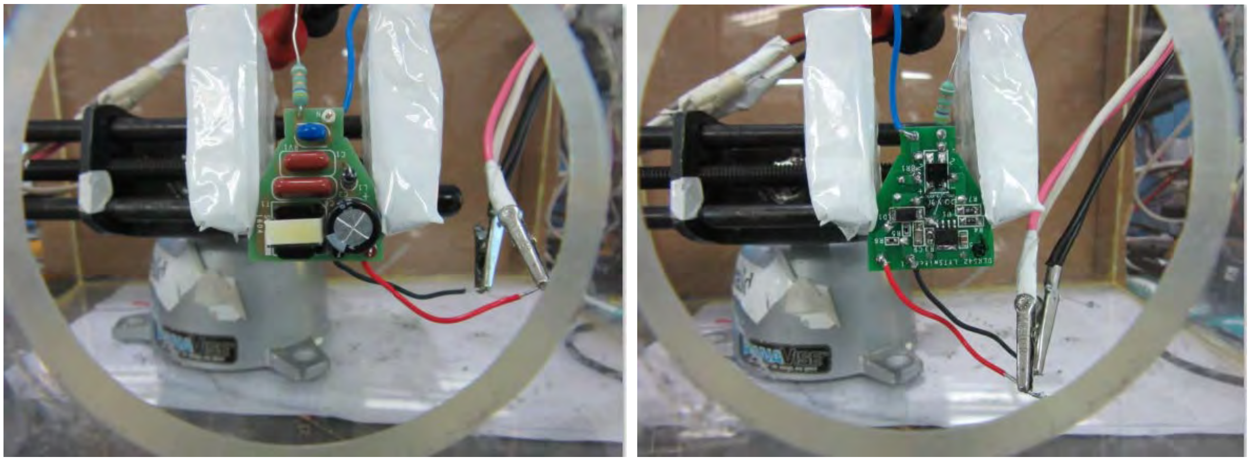

Figure 14 – Test Set-up Picture - Open Frame.

Unit in open frame was placed inside the acrylic enclosure to prevent airflow that might affect the thermal measurements. Temperature was measured using an FLIR thermal camera.

11.1.1 Thermal Scan

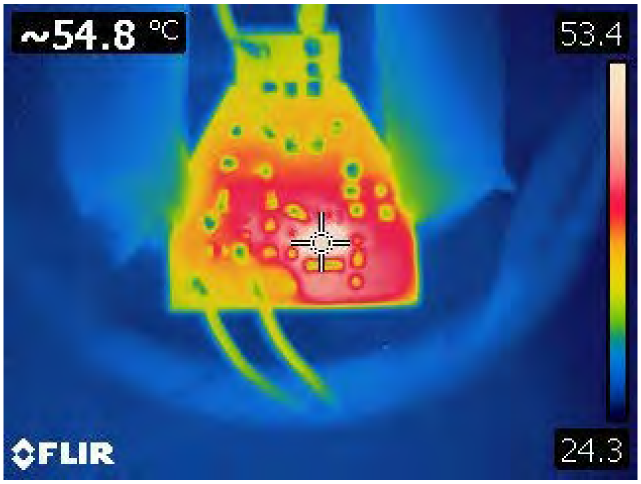

Figure 15 – 230 VAC, 90 V LED Load.
Spot 1: LYT1602D (U1): 54.8 ºC.

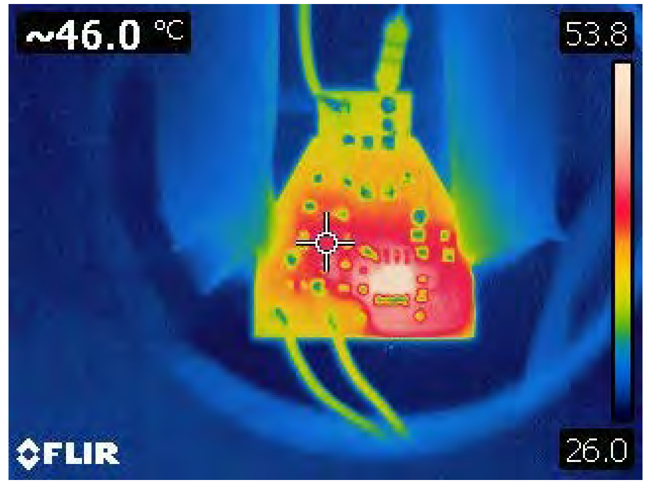

Figure 16 – 230 VAC, 90 V LED Load.
Spot 1: Output Diode (D1): 46 ºC.

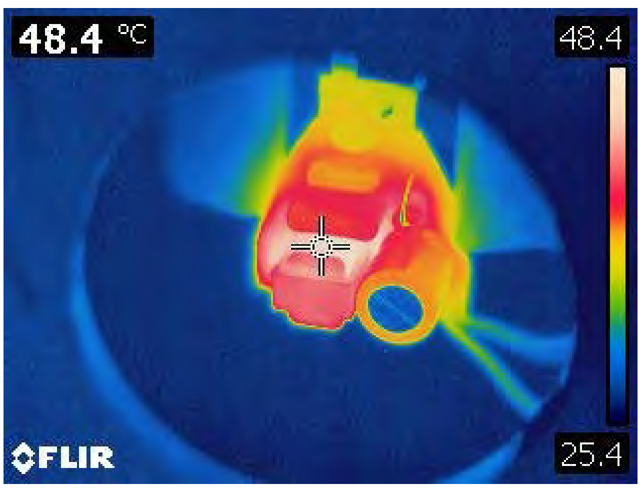

Figure 17 – 230 VAC, 90 V LED Load.
Spot 1: Inductor (T1): 48.4 ºC.

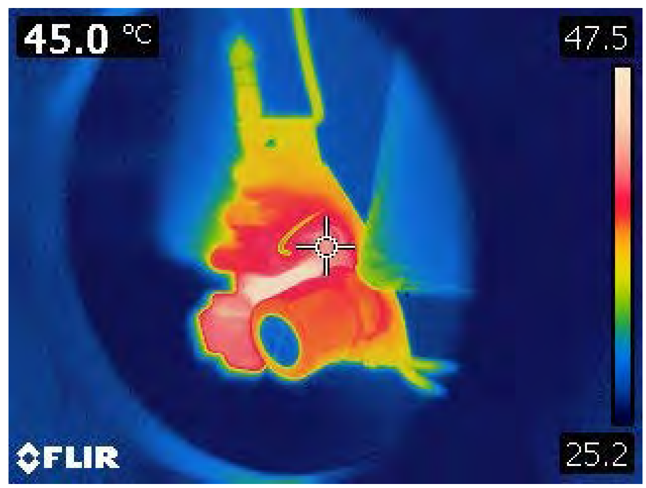

Figure 18 – 230 VAC, 90 V LED Load.
Spot 1: Differential Choke (L1): 45 ºC.

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11.2 Thermal Performance at 85 °C Ambient

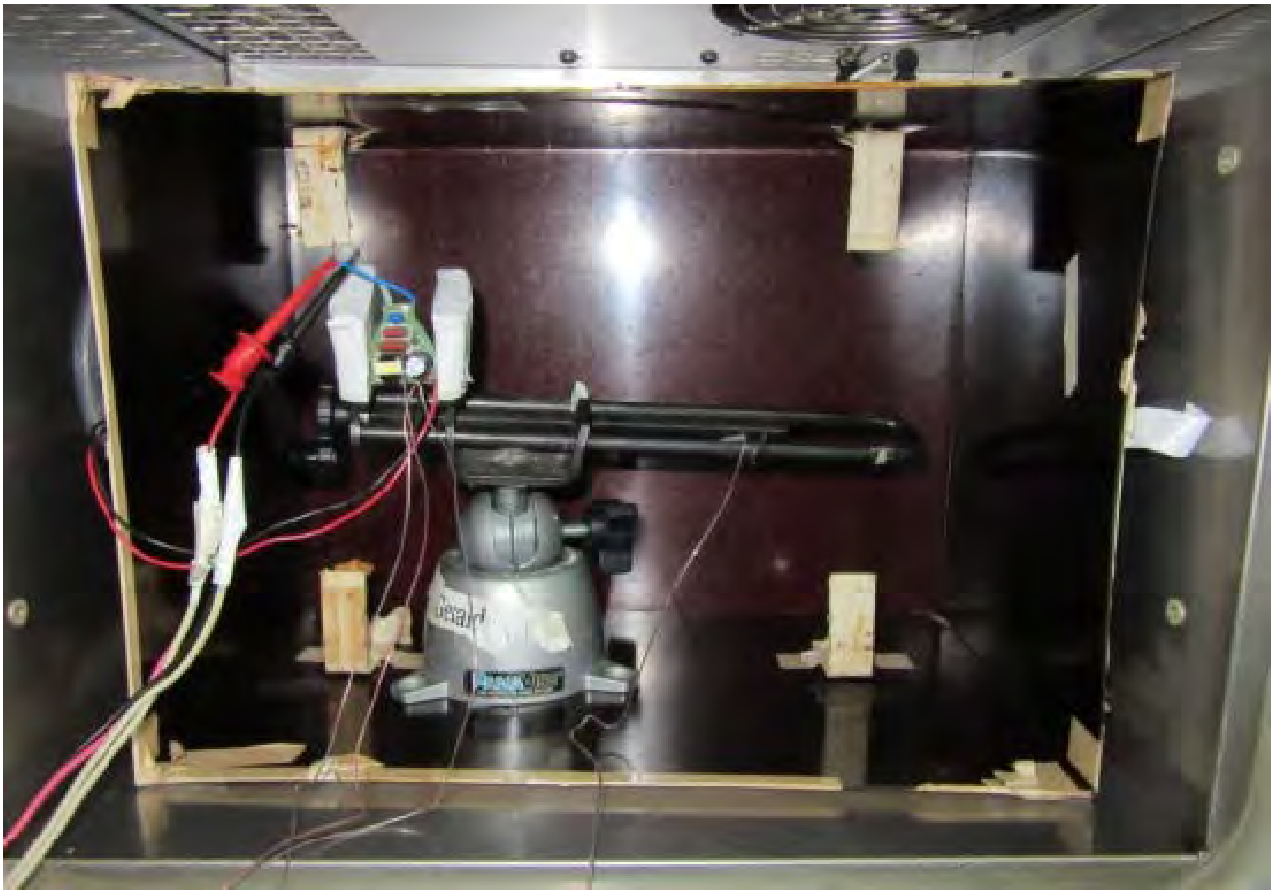

Figure 19 – Test Set-up Picture Thermal at 85 ºC Ambient- Open Frame.

Unit in open frame was placed inside the enclosure to prevent airflow that might affect the thermal measurements. Ambient temperature inside enclosure is 85 ºC. Temperature was measured using Type-T thermocouple.

11.2.1 Thermal Performance at 185 VAC with a 90 V LED Load

Measurement	Ambient	LYTSwitch-1	D1	T1
Maximum (°C)	85.1	101.8	97.2	94.8
Final (°C)	85.0	101.8	97.2	94.8

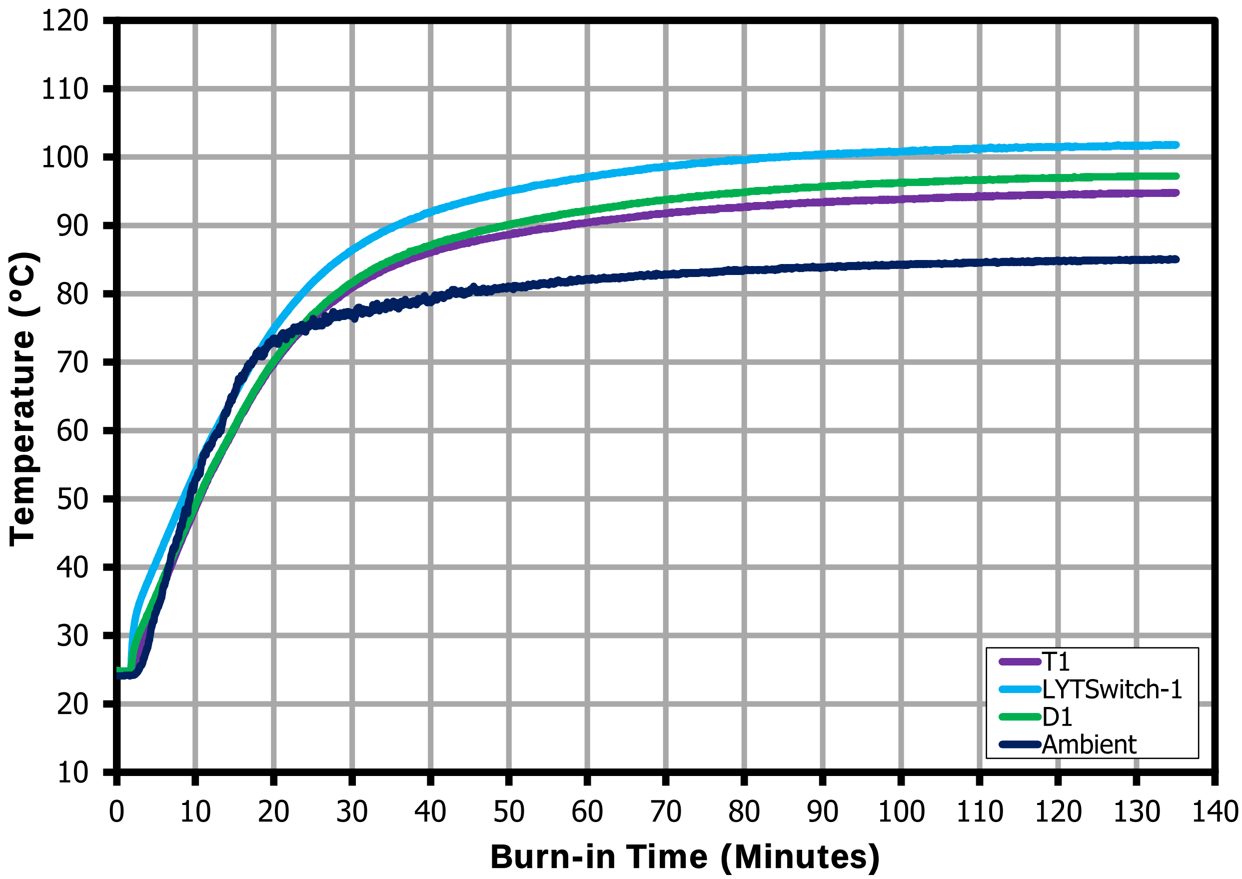

Figure 20 – Component Temperature at 185 VAC, 90 V LED Load, 85 ºC Ambient.

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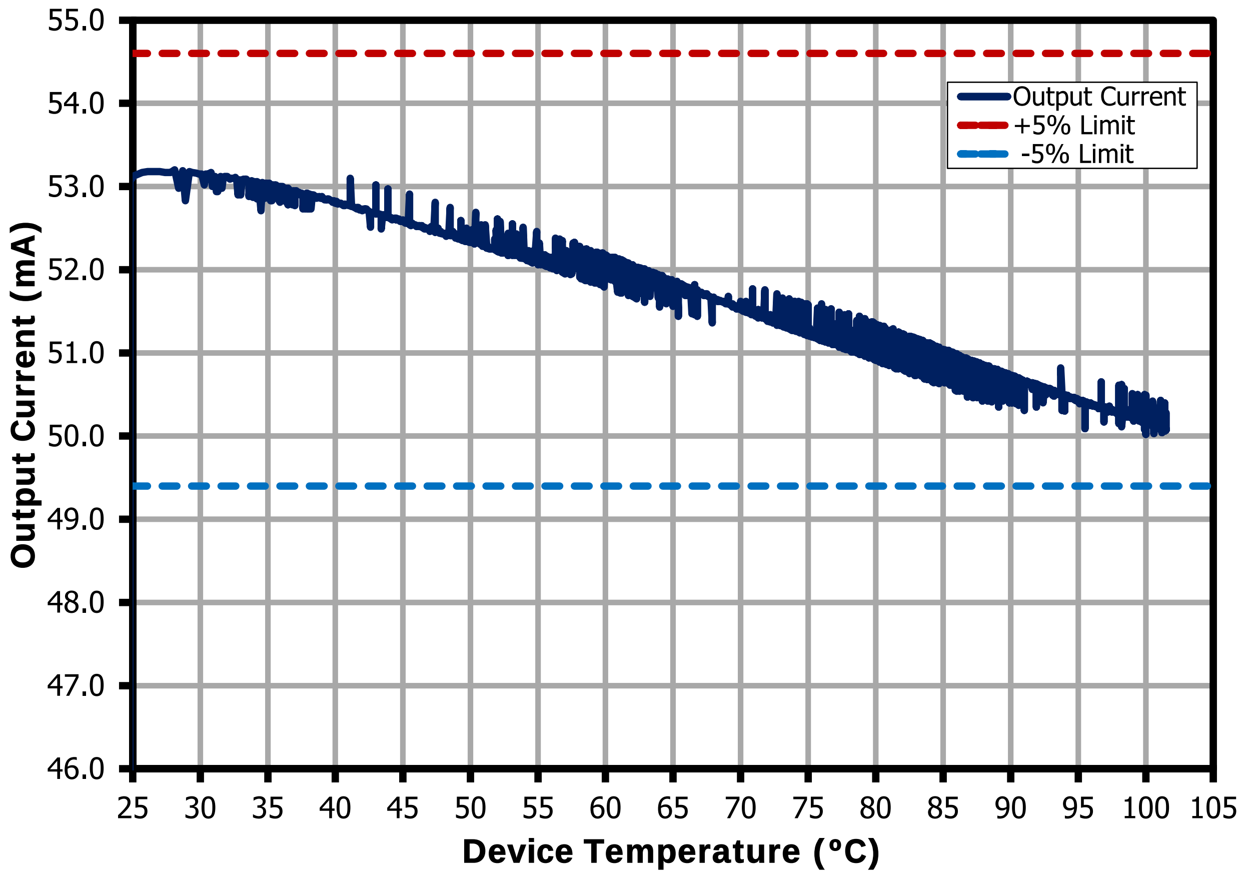

Figure 21 – Output Current vs. Device Temperature at 185 VAC, 90 V LED Load, 85 ºC Ambient.

11.2.2 Thermal Performance at 230 VAC with a 90 V LED Load

Measurement	Ambient	LYTSwitch-1	D1	T1
Maximum (°C)	85.6	106.0	99.9	96.9
Final (°C)	85.5	105.9	99.9	96.9

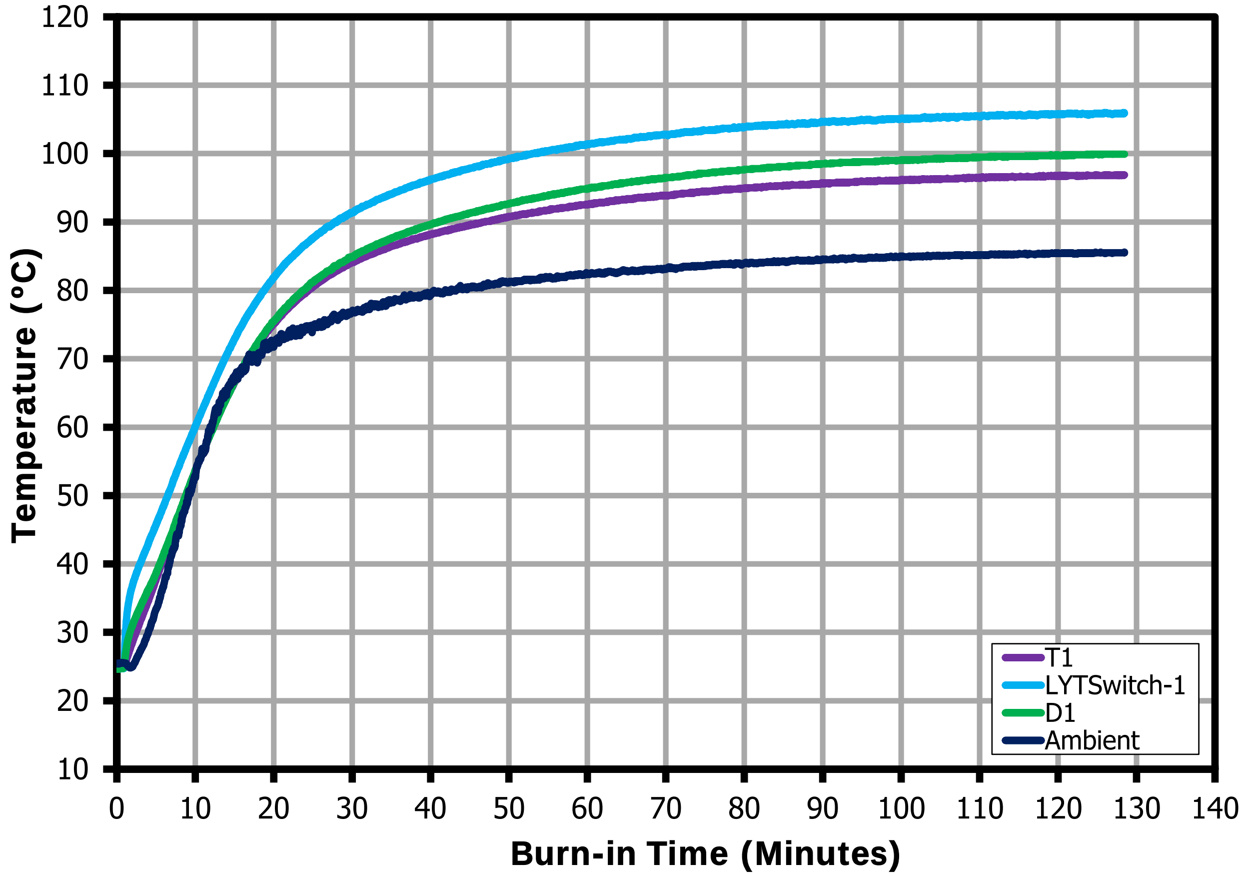

Figure 22 – Component Temperature at 230 VAC, 90 V LED Load, 85 °C Ambient.

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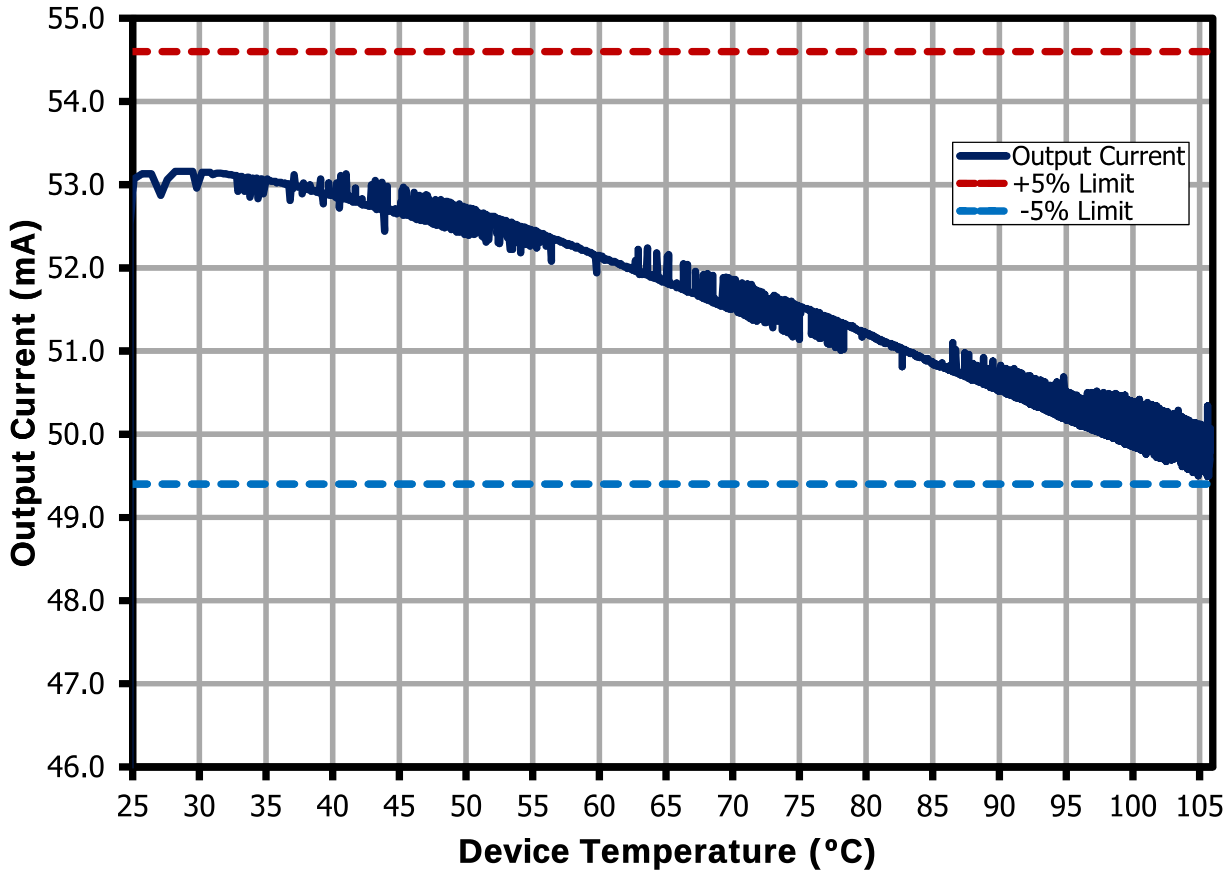

Figure 23 – Output Current vs. Device Temperature at 230 VAC, 90 V LED Load, 85 ºC Ambient.

11.2.3 Thermal Performance at 265 VAC with a 90 V LED Load

Measurement	Ambient	LYTSwitch-1	D1	T1
Maximum (°C)	85.5	109.1	101.4	98.2
Final (°C)	85.5	109.0	101.4	98.2

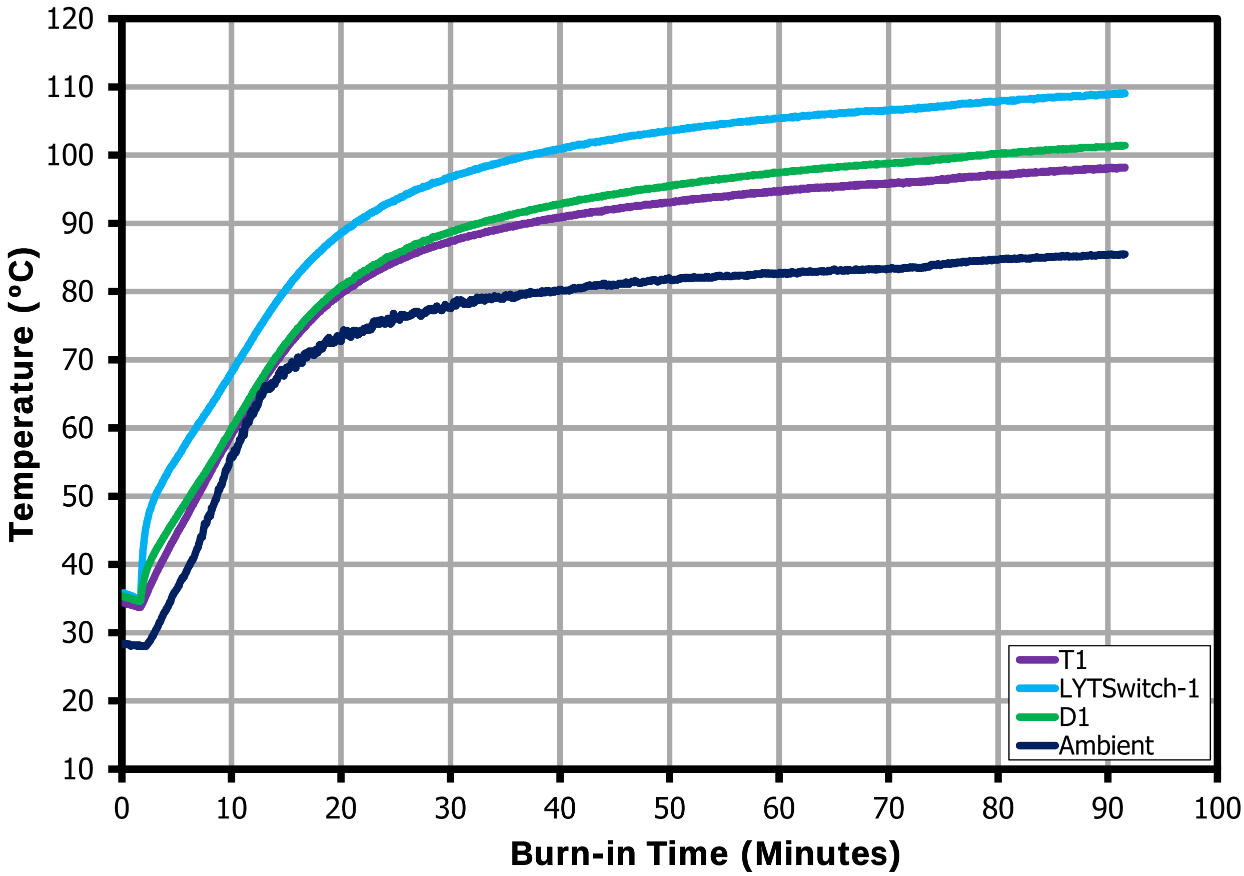

Figure 24 – Component Temperature at 265 VAC, 90 V LED Load, 85 °C Ambient.

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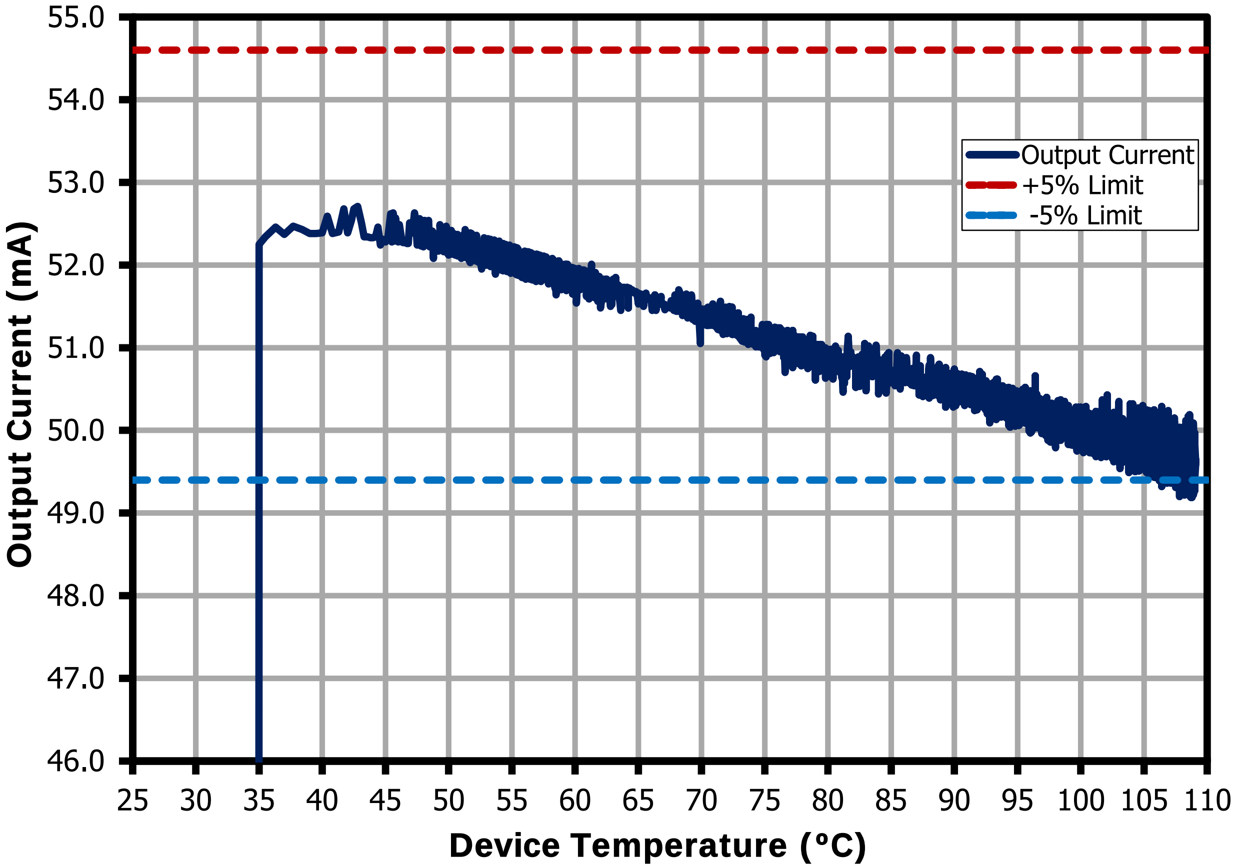

Figure 25 – Output Current vs. Device Temperature at 230 VAC, 90 V LED Load, 85 ºC Ambient.

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12 Waveforms

12.1 Input Voltage and Input Current Waveforms

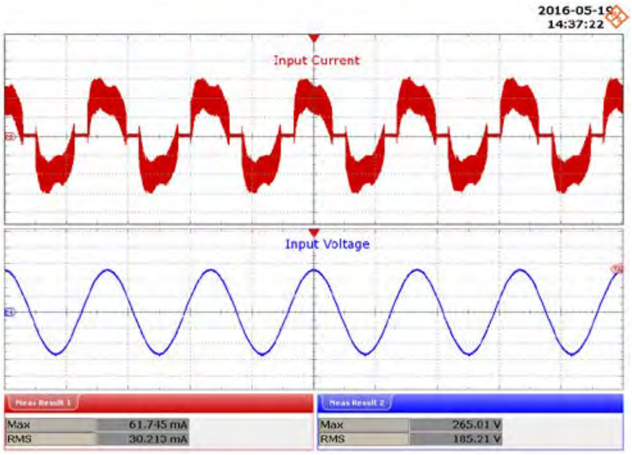

Figure 26 – 185 VAC, 90 V LED Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V / div., 10 ms / div.

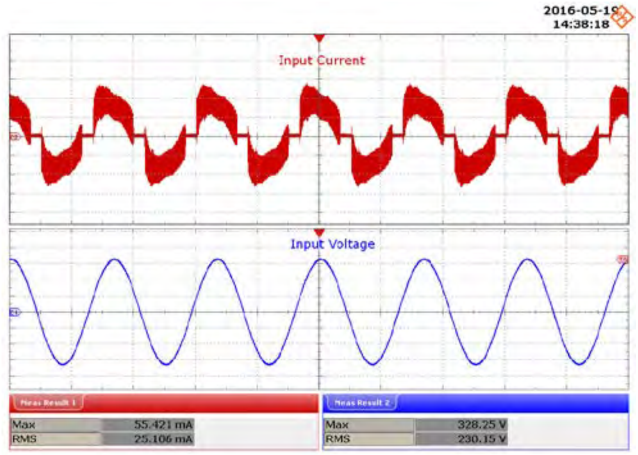

Figure 27 – 230 VAC, 90 V LED Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V / div., 10 ms / div.

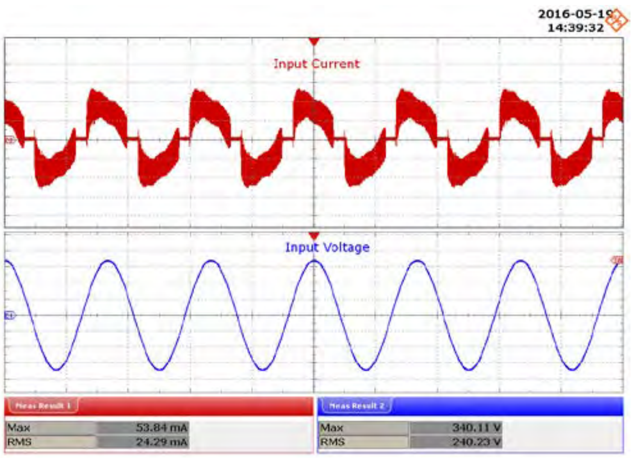

Figure 28 – 240 VAC, 90 V LED Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V / div., 10 ms / div.

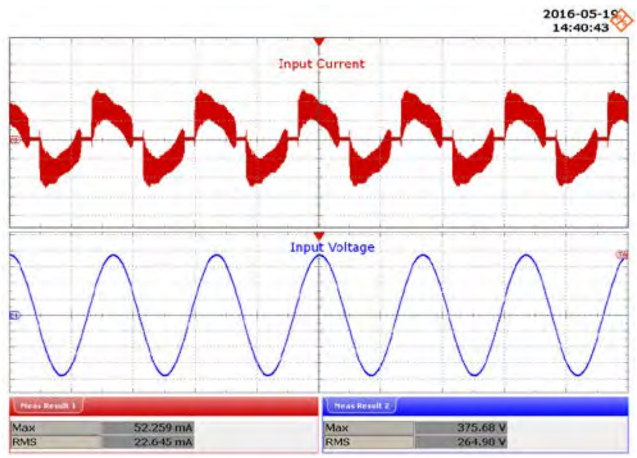

Figure 29 – 265 VAC, 90 V LED Load.
Upper: I_{IN}, 100 mA / div.
Lower: V_{IN}, 100 V / div., 10 ms / div.

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12.2 Start-up Profile

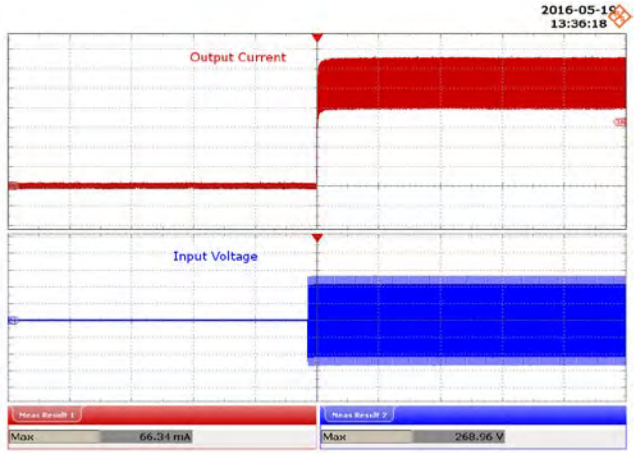

Figure 30 – 185 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

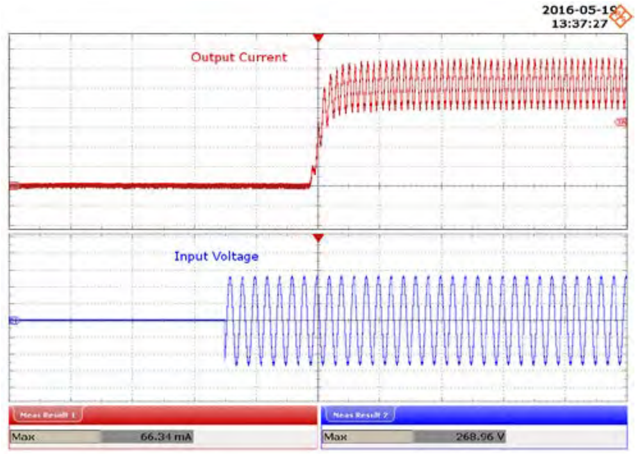

Figure 31 – 185 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

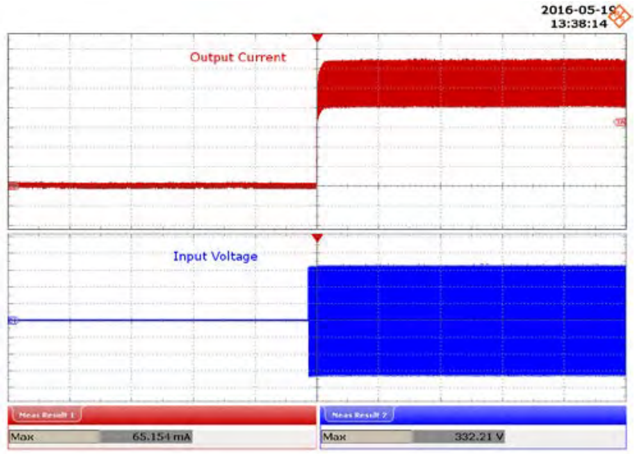

Figure 32 – 230 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

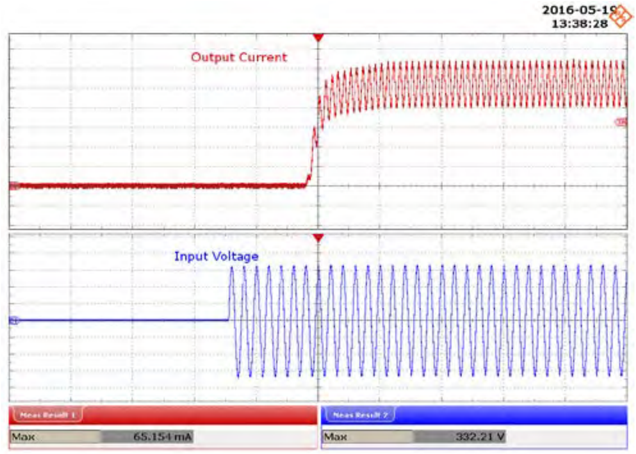

Figure 33 – 230 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

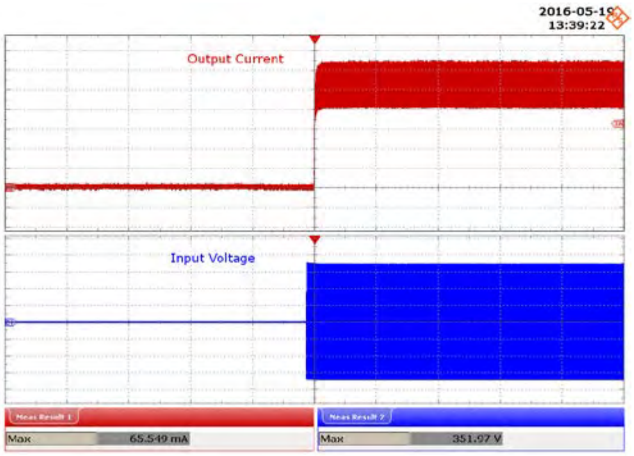

Figure 34 – 240 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

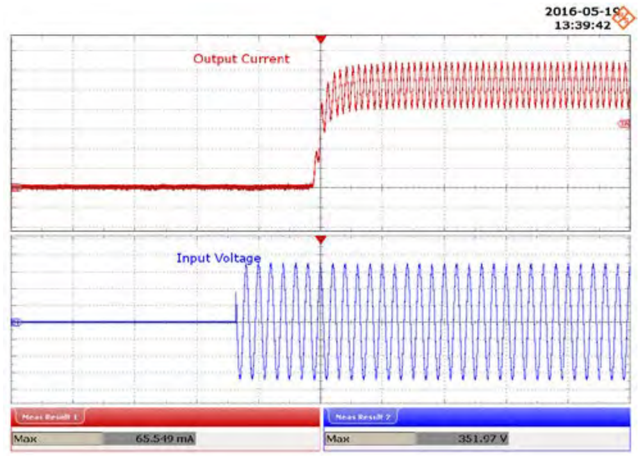

Figure 35 – 240 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

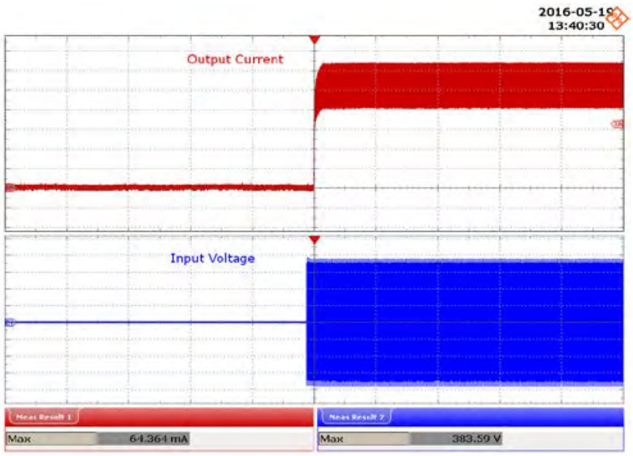

Figure 36 – 265 VAC, 90 V LED, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

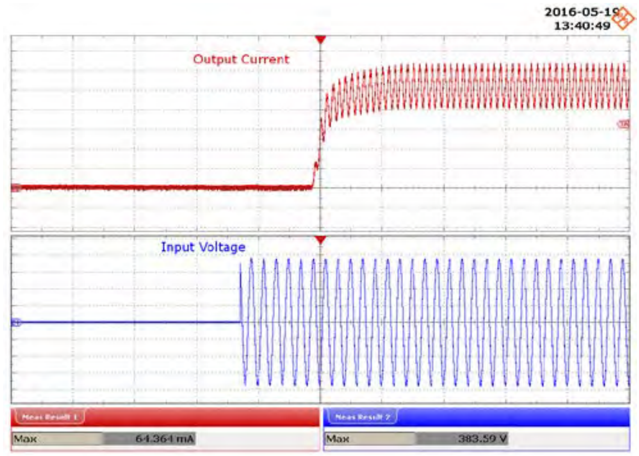

Figure 37 – 265 VAC, 90 V LED Load, Output Rise.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

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12.3 Output Current Fall

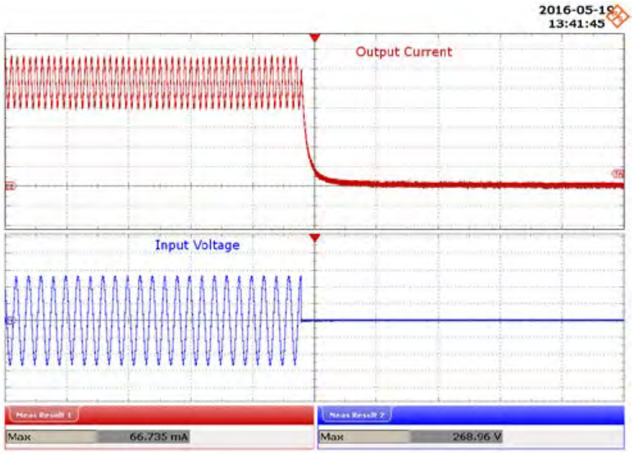

Figure 38 – 185 VAC, 90 V LED, Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

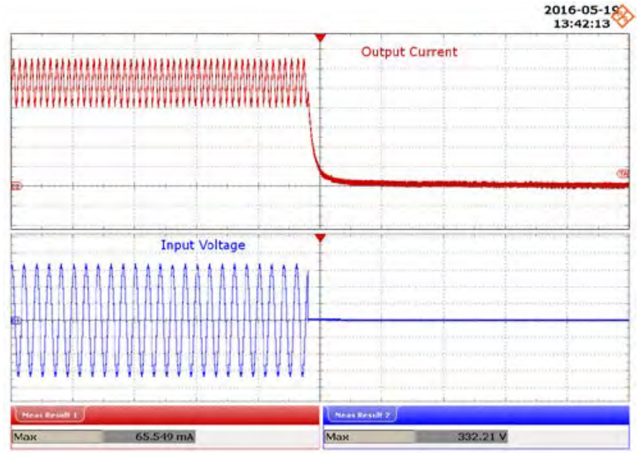

Figure 39 – 230 VAC, 90 V LED, Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

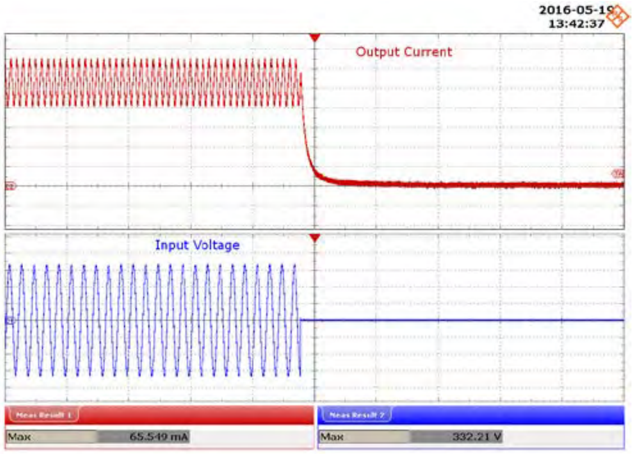

Figure 40 – 240 VAC, 90 V LED, Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

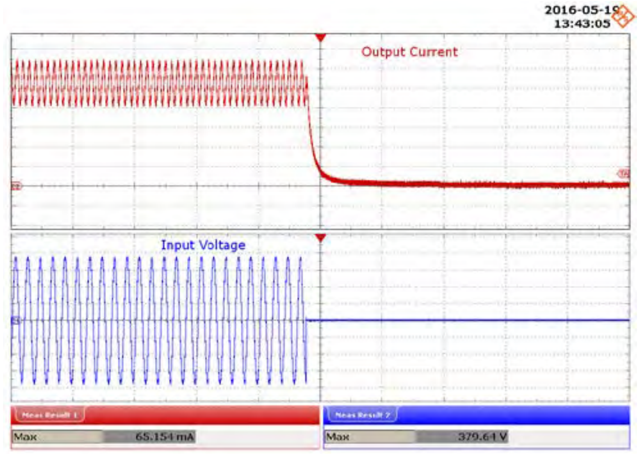

Figure 41 – 265 VAC, 90 V LED, Output Fall.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

12.4 Drain Voltage and Current in Normal Operation

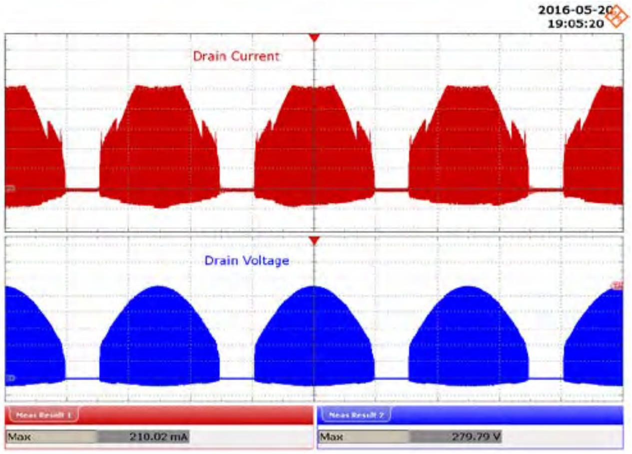

Figure 42 – 185 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 4 ms / div.

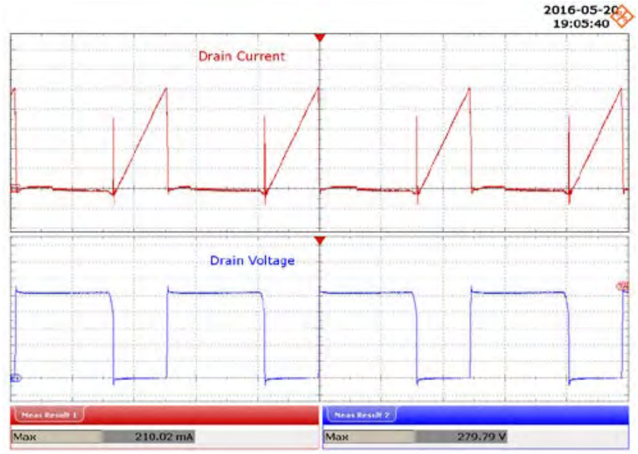

Figure 43 – 185 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 5 µs / div.

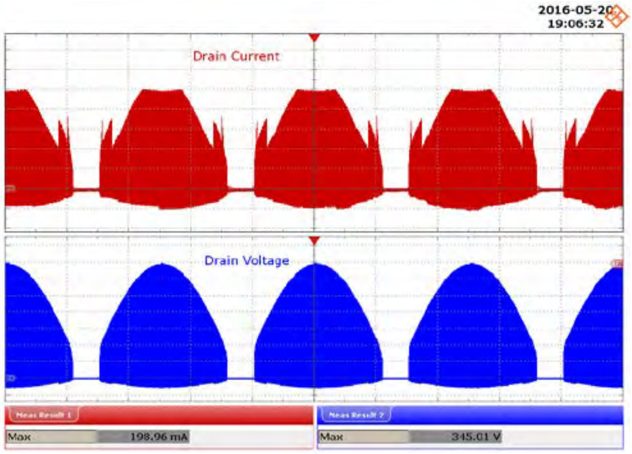

Figure 44 – 230 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 4 ms / div.

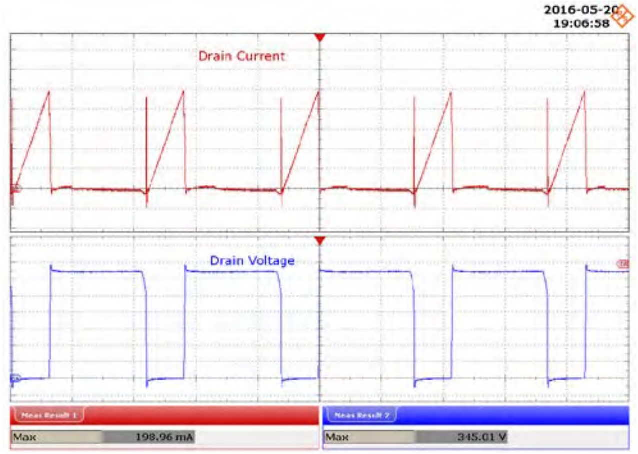

Figure 45 – 230 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 5 µs / div.

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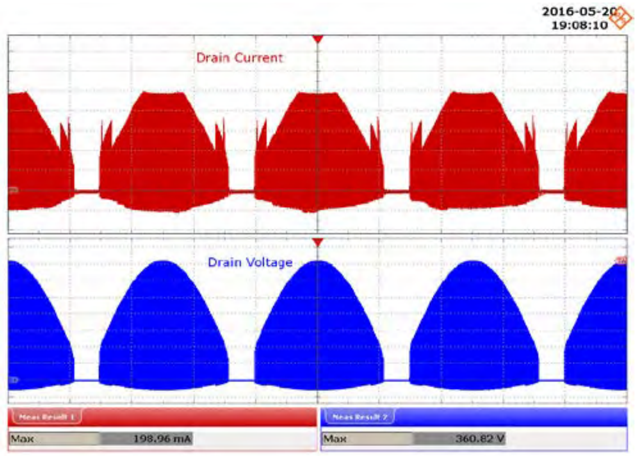

Figure 46 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 4 ms / div.

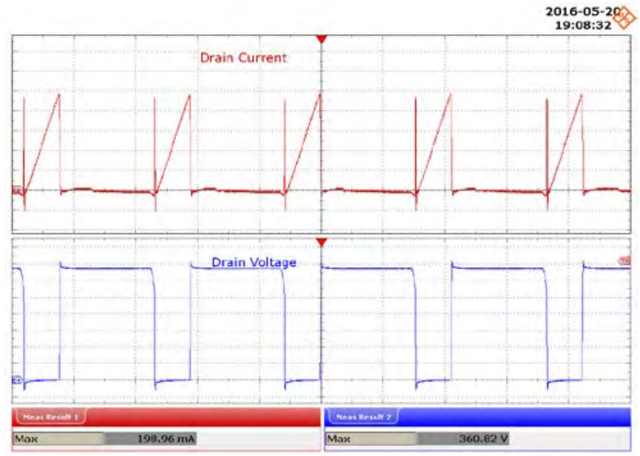

Figure 47 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 5 μs / div.

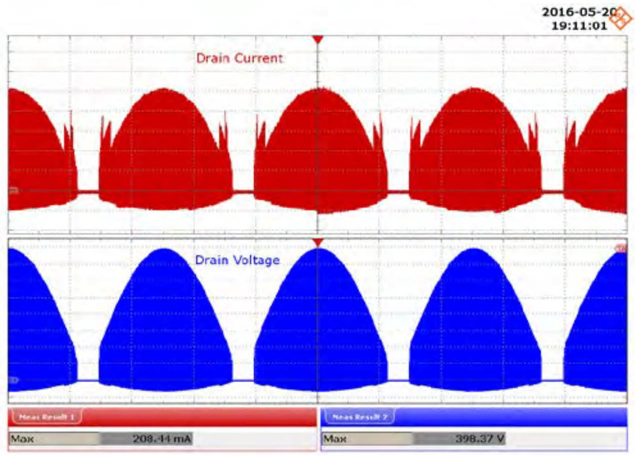

Figure 48 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 4 ms / div.

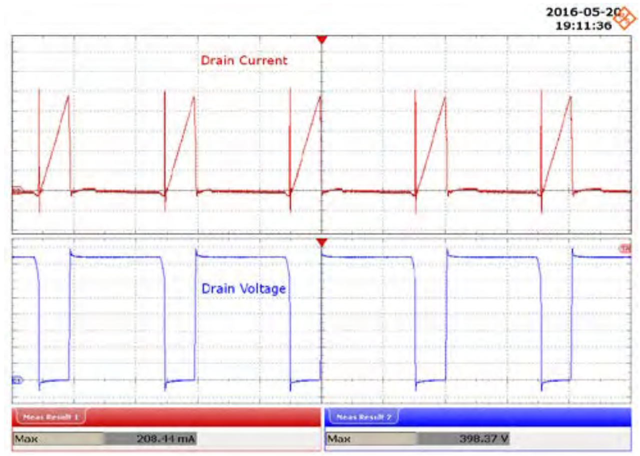

Figure 49 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 40 mA / div.
Lower: V_{DRAIN}, 50 V / div., 5 μs / div.

12.5 Drain Voltage and Current Start-up Profile

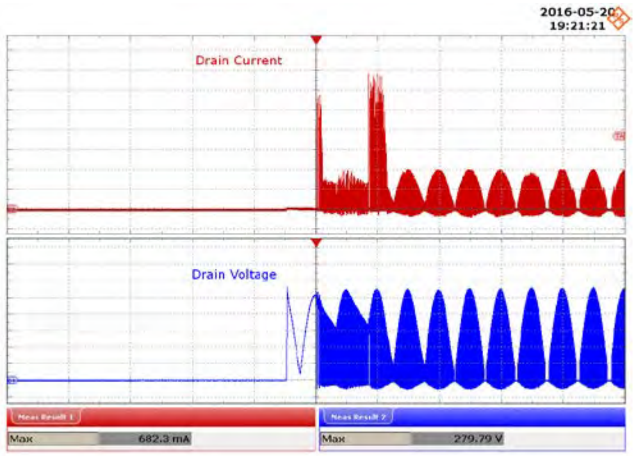

Figure 50 – 185 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 20 ms / div.

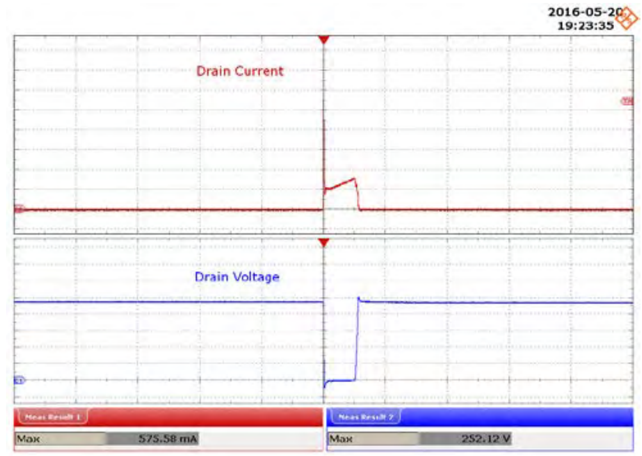

Figure 51 – 185 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 1 μs / div.

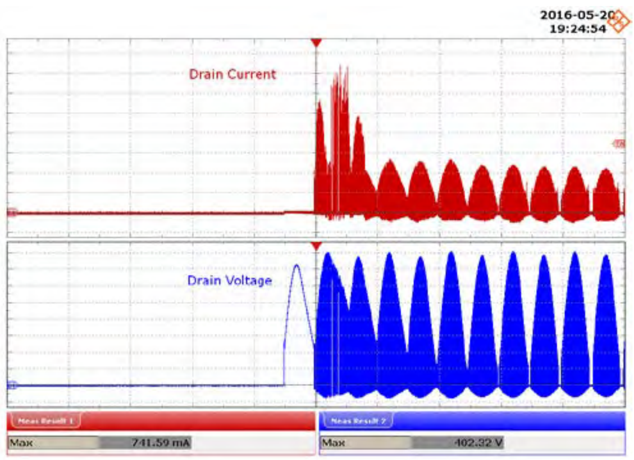

Figure 52 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 20 ms / div.

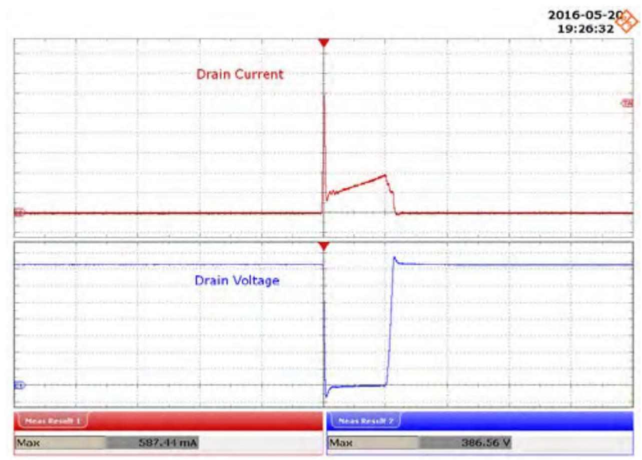

Figure 53 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 1 μs / div.

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12.6 Drain Voltage and Current at Output Short-Circuit

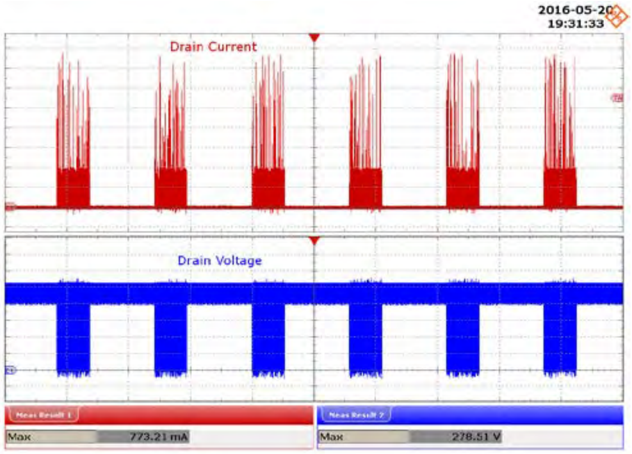

Figure 54 – 185 VAC, Output Short Circuit.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 1 s / div.

Figure 55 – 195 VAC, Output Short Circuit.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 1 µs / div.

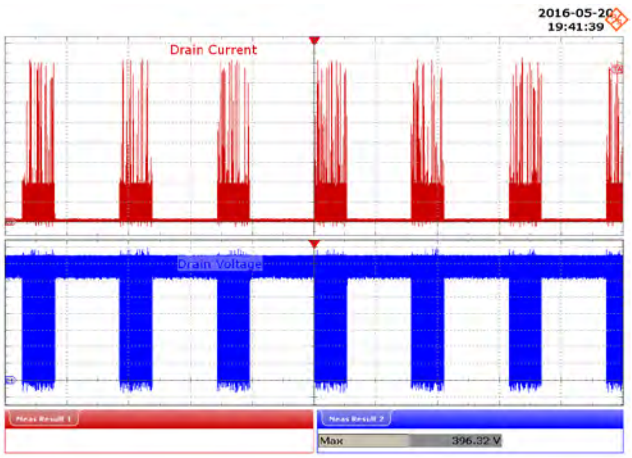

Figure 56 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 20 ms / div.

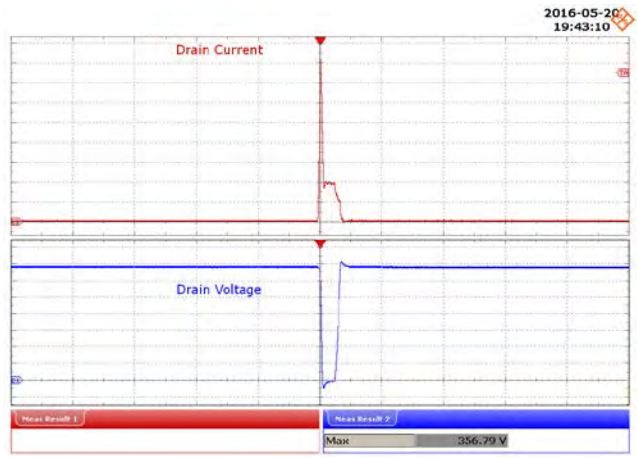

Figure 57 – 265 VAC, 90 V LED Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V / div., 1 µs / div.

12.7 Output Diode Voltage and Current in Normal Operation

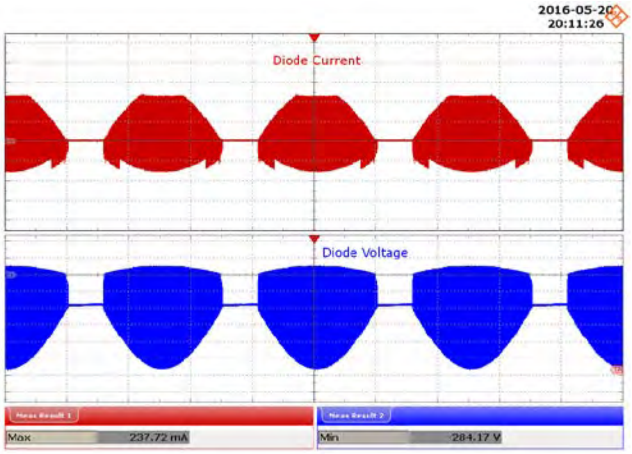

Figure 58 – 185 VAC, 90 V LED Load.
Upper: I_{D1}, 100 mA / div.
Lower: V_{D1}, 50 V / div., 4 ms / div.

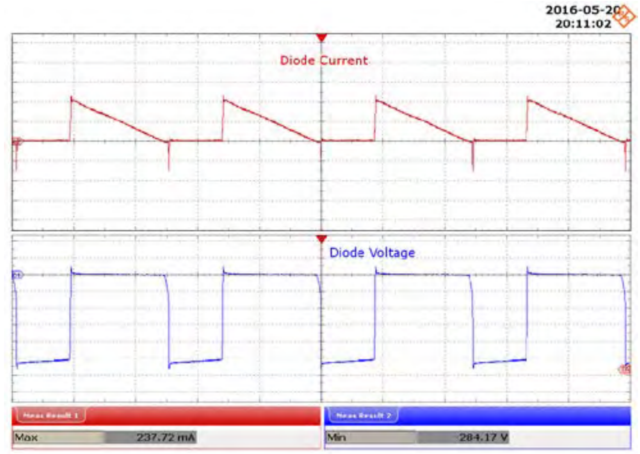

Figure 59 – 185 VAC, 90 V LED Load.
Upper: I_{D1}, 100 mA / div.
Lower: V_{D1}, 50 V / div., 5 µs / div.

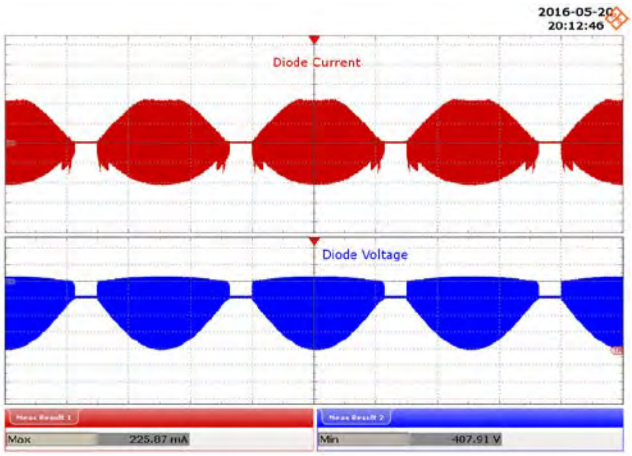

Figure 60 – 265 VAC, 90 V LED Load.
Upper: I_{D1}, 100 mA / div.
Lower: V_{D1}, 100 V / div., 4 ms / div.

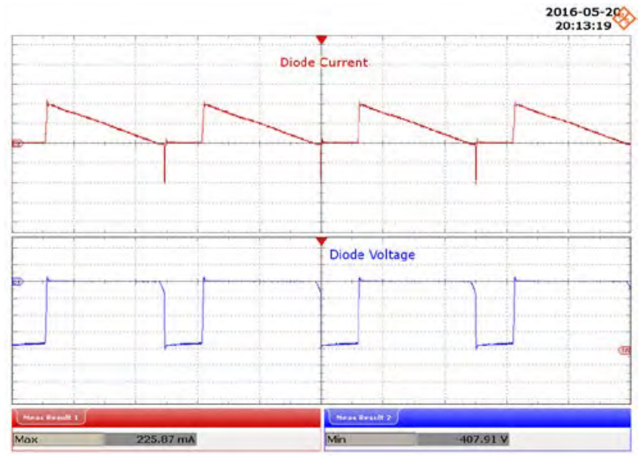

Figure 61 – 265 VAC, 90 V LED Load.
Upper: I_{D1}, 100 mA / div.
Lower: V_{D1}, 100 V / div., 4 µs / div.

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12.8 Output Voltage and Current – Open Output LED Load

Maximum measured no load output voltage is below the surge voltage rating of the output capacitor.

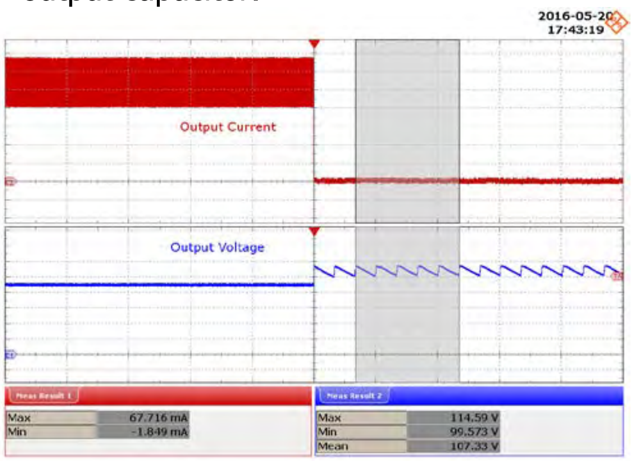

Figure 62 – 185 VAC, 90 V LED Load,
Running Open Load.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V / div., 4 s / div.

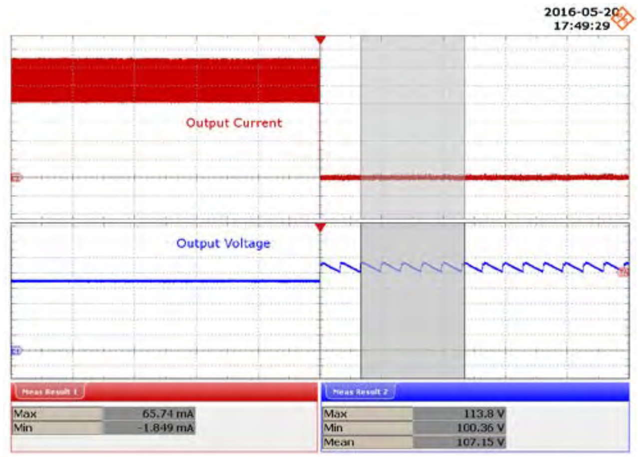

Figure 63 – 265 VAC, 90 V LED Load,
Running Open Load.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V / div., 4 s / div.

12.9 Output Voltage and Current – Start-up at Open Output Load

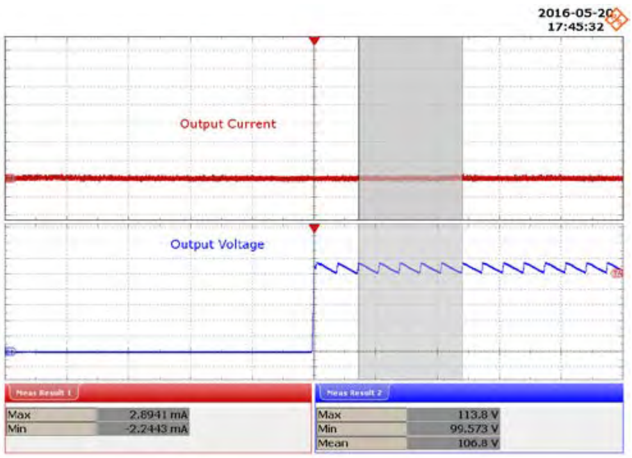

Figure 64 – 185 VAC, Open Load,
Open Load Start-up.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V / div., 4 s / div.

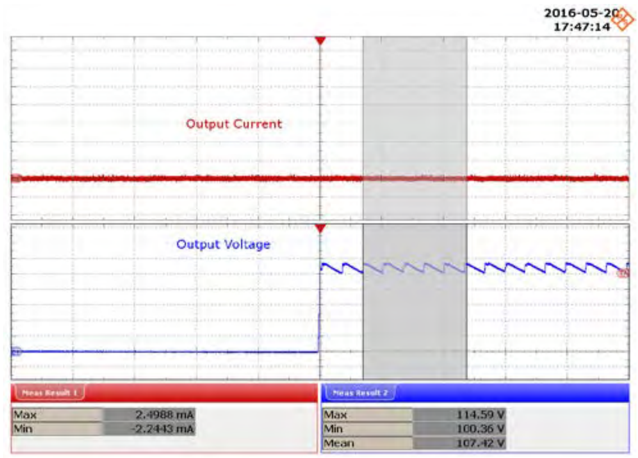

Figure 65 – 265 VAC, Open Load,
Open Load Start-up.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{OUT}, 20 V / div., 4 s / div.

12.10 Output Ripple Current

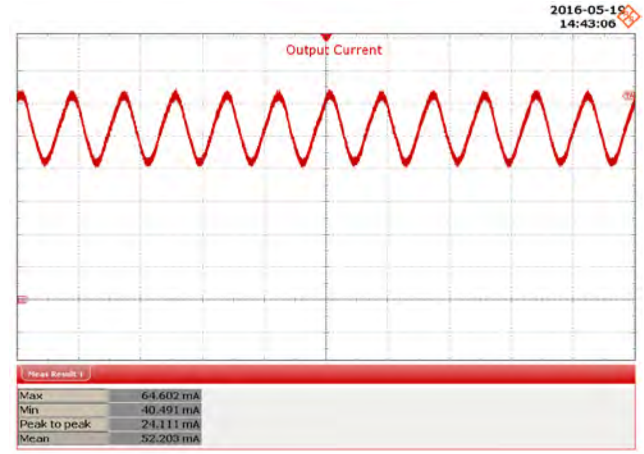

Figure 66 – 185 VAC, 50 Hz, 90 V LED Load.
Upper: I_{OUT}, 10 mA / div., 10 ms / div.

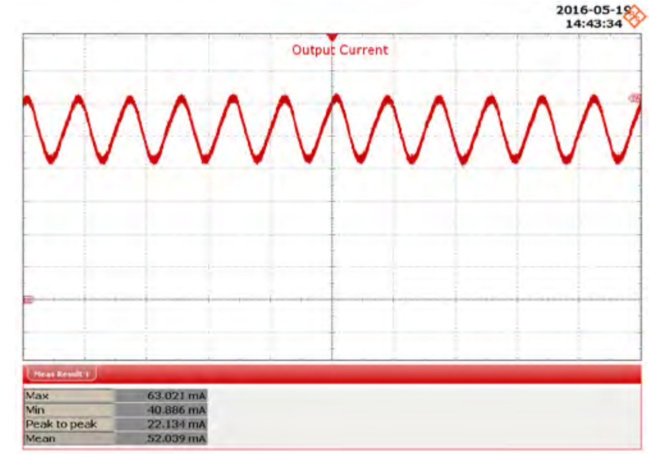

Figure 67 – 230 VAC, 60 Hz, 90 V LED Load.
Upper: I_{OUT}, 10 mA / div., 10 ms / div.

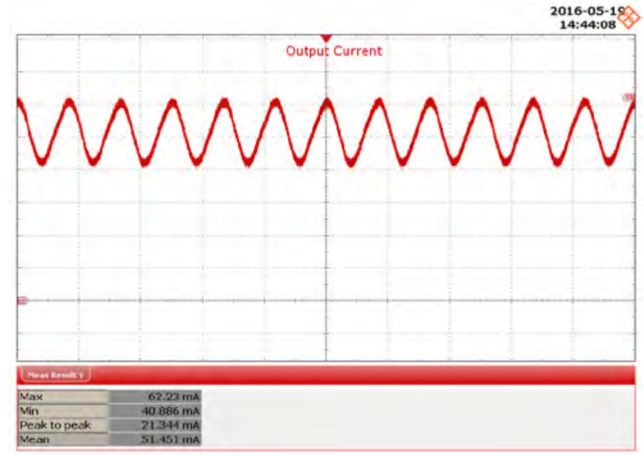

Figure 68 – 265 VAC, 60 Hz, 90 V LED Load.
Upper: I_{OUT}, 10 mA / div., 10 ms / div.

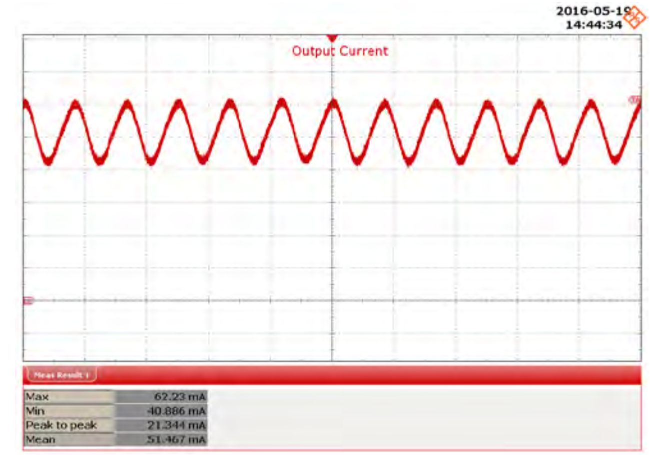

Figure 69 – 265 VAC, 60 Hz, 90 V LED Load.
Upper: I_{OUT}, 10 mA / div., 10 ms / div.

V_{IN} (VAC)	$I_{O(MAX)}$ (mA)	$I_{O(MIN)}$ (mA)	I_{MEAN}	Ripple Ratio (I_{RP-P} / I_{MEAN})	% Flicker 100 x (I_{RP-P} / $I_{O(MAX)}$ + $I_{O(MIN)}$)
185	64.02	40.49	52.2	0.45	22.51
230	63	40.89	52.04	0.42	21.28
240	62.23	40.89	51.45	0.41	20.69
265	62.23	40.89	51.47	0.41	20.69

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13 AC Cycling Test

No output current overshoot was observed during on - off cycling.

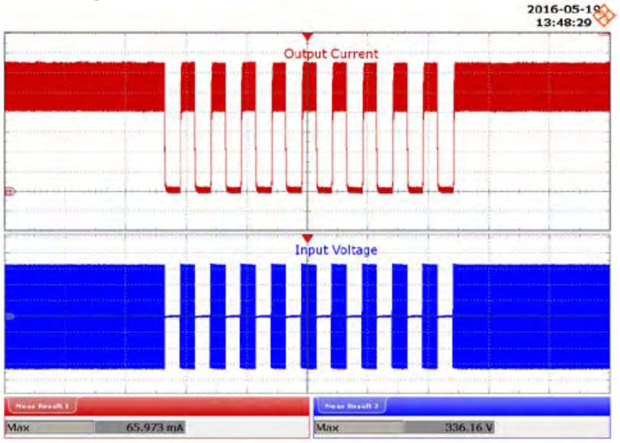

Figure 70 – 230 VAC, 90 V LED Load.
1 s On – 1 s Off.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 4 s / div.

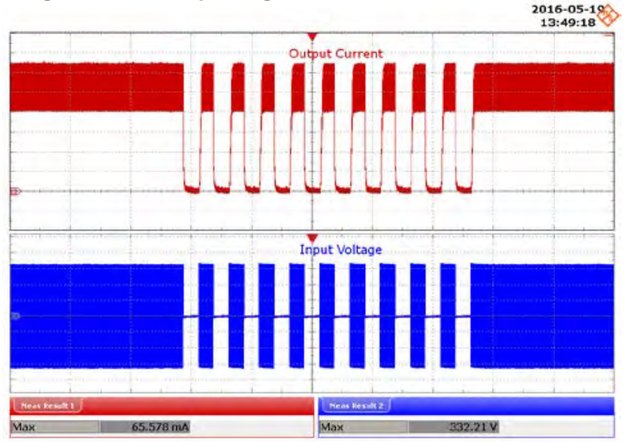

Figure 71 – 230 VAC, 90 V LED Load.
0.5 s On – 0.5 s Off.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 2 s / div.

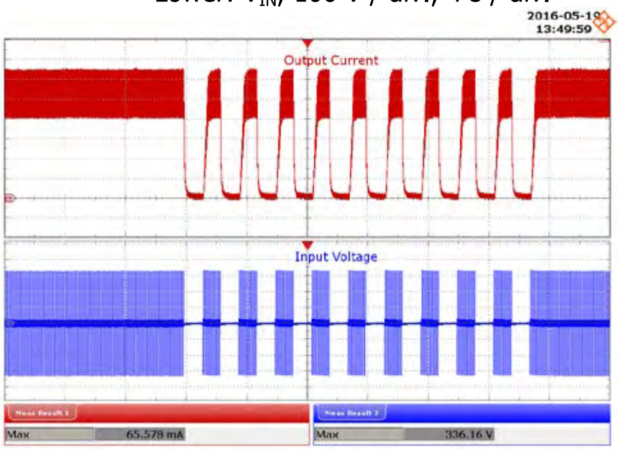

Figure 72 – 230 VAC, 90 V LED Load.
300 ms On – 300 ms Off.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

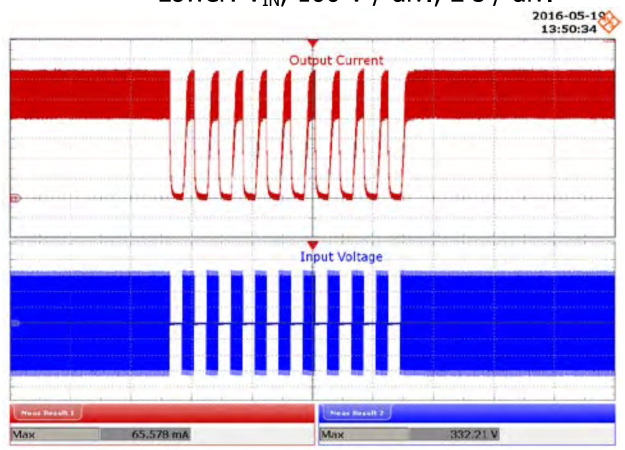

Figure 73 – 230 VAC, 90 V LED Load.
200 ms On – 200 ms Off.
Upper: I_{OUT}, 10 mA / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

14 Conducted EMI

14.1 Test Set-up

14.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. 90 V LED load with input voltage set at 230 VAC.

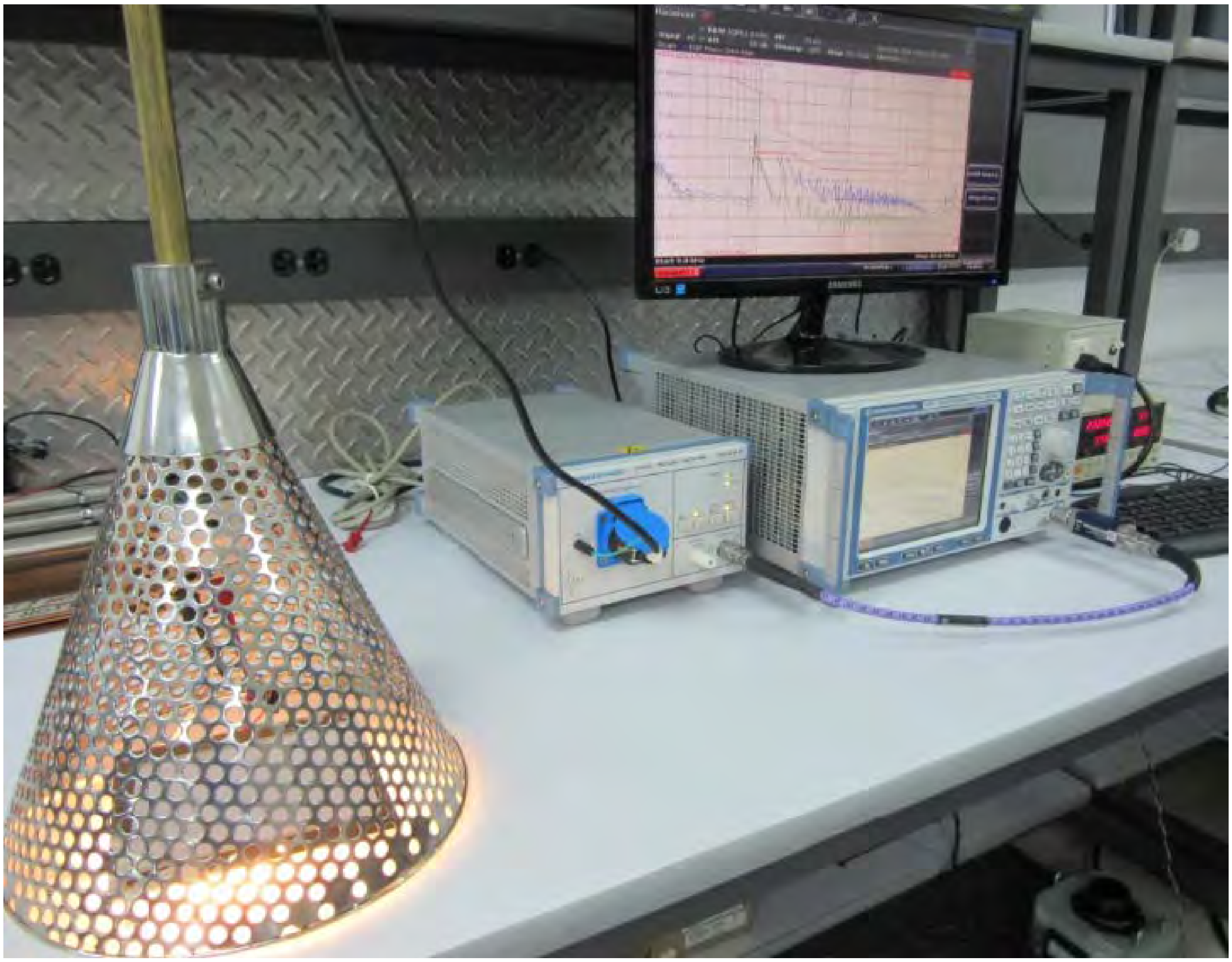

Figure 74 – Conducted EMI Test Set-up.

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14.2 EMI Test Result

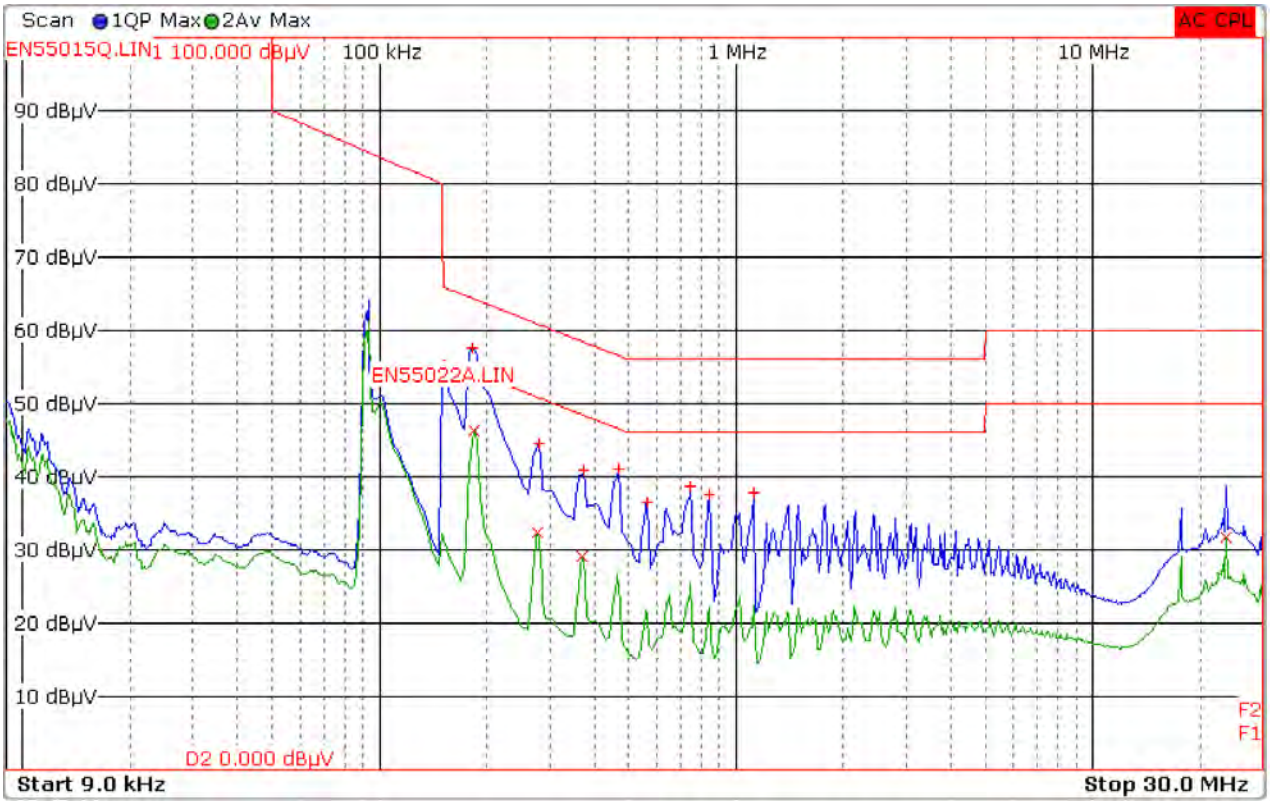

Figure 75 – Conducted EMI QP Scan at 90 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	181.5000 kHz	57.59 N	-6.83 dB
2 Average	183.7500 kHz	46.40 L1	-7.91 dB
1 Quasi Peak	150.0000 kHz	54.81 N	-11.19 dB
1 Quasi Peak	467.2500 kHz	41.07 N	-15.49 dB
1 Quasi Peak	280.5000 kHz	44.65 N	-16.15 dB
1 Quasi Peak	746.2500 kHz	38.62 L1	-17.38 dB
1 Quasi Peak	372.7500 kHz	40.77 L1	-17.67 dB
2 Average	23.6760 MHz	31.81 N	-18.19 dB
1 Quasi Peak	1.1243 MHz	37.75 N	-18.25 dB
2 Average	278.2500 kHz	32.42 L1	-18.45 dB
1 Quasi Peak	843.0000 kHz	37.51 N	-18.49 dB
2 Average	370.5000 kHz	29.07 L1	-19.42 dB
1 Quasi Peak	561.7500 kHz	36.57 N	-19.43 dB

Figure 76 – Conducted EMI Data at 230 VAC, 90 V LED Load.

15 Line Surge

The unit was subjected to ±2500 V, 100 kHz ring wave and ±1000 V differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

15.1 Differential Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

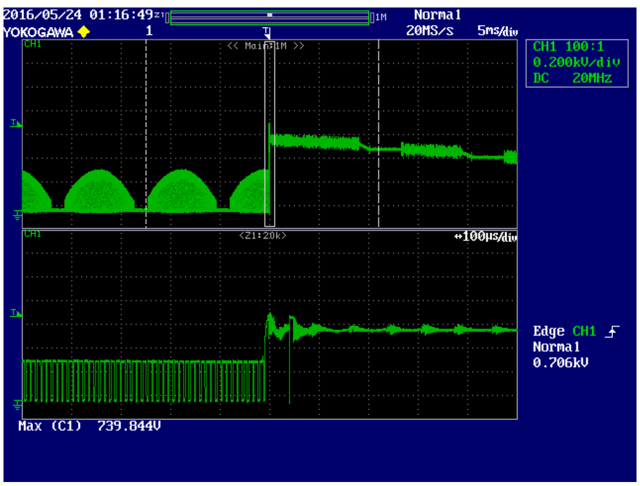

Figure 77 – +1 kV Differential Surge, 90º Phase Angle. Lower: V_{DRAIN}, 200 V / div., 5 ms /div. Peak V_{DRAIN}: 740 V.

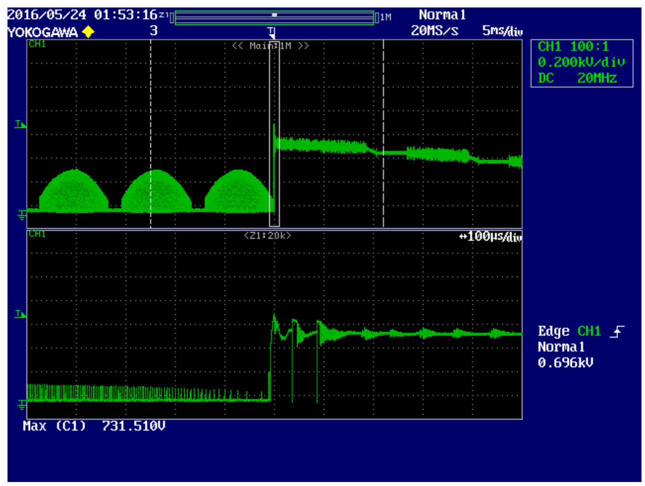

Figure 78 – +1 kV Differential Surge, 0º Phase Angle. Lower: V_{DRAIN}, 200 V / div., 5 ms /div. Peak V_{DRAIN}: 732 V.

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15.2 Ring Wave Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass

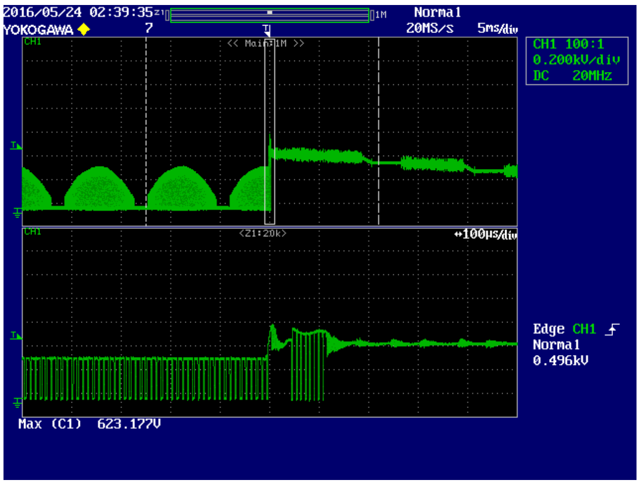

Figure 79 – +2.5 kV Ringwave Surge,
90º Phase Angle.
Lower: V_{DRAIN}, 200 V / div., 5 ms /div.
Peak V_{DRAIN}: 623 V.

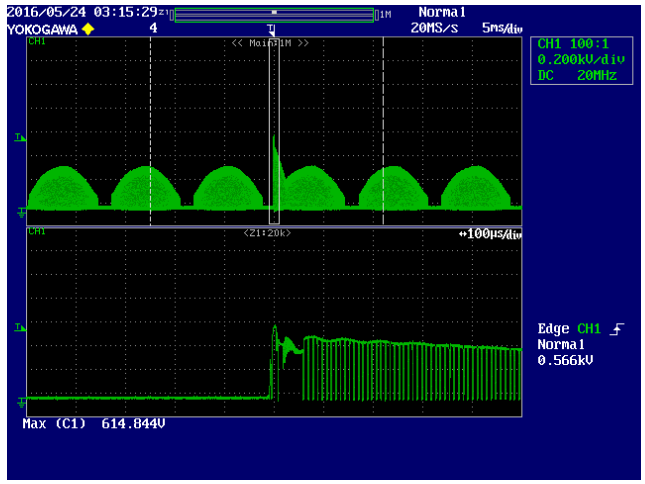

Figure 80 – +2.5 kV Ringwave Surge,
0 º Phase Angle.
Lower: V_{DRAIN}, 200 V / div., 5 ms /div.
Peak V_{DRAIN}: 615 V.

16 Brown-in / Brown-out Test

No component failure and overheating were observed.

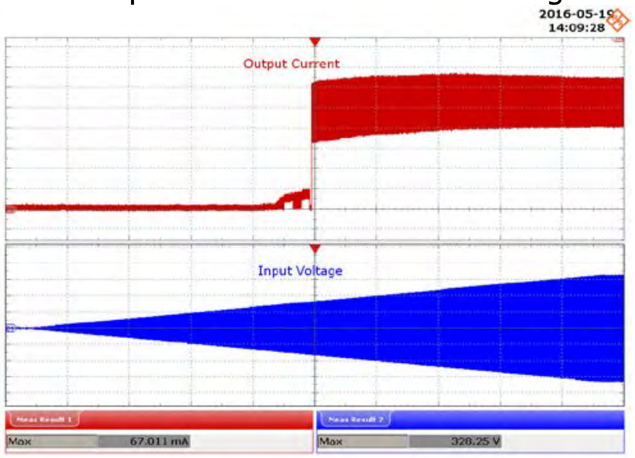

Figure 81 – Brown-in Test at 0.5 V / s.
Ch1: I_{OUT}, 10 mA / div.
Ch2: V_{IN}, 100 V / div.
Time Scale: 50 s / div.

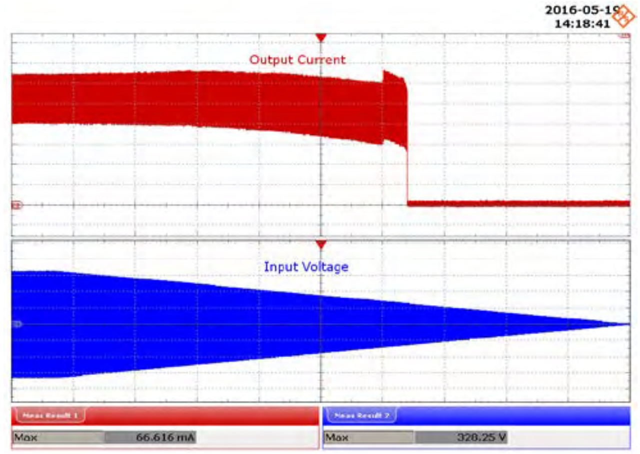

Figure 82 – Brown-out Test at 0.5 V / s
Ch1: I_{OUT}, 10 mA / div.
Ch2: V_{IN}, 100 V / div.
Time Scale: 50 s / div.

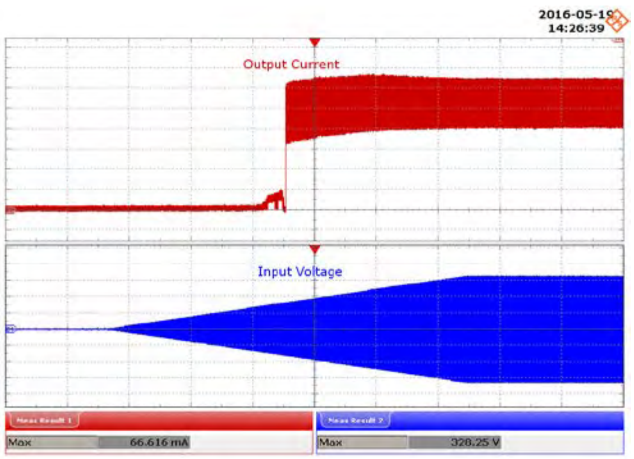

Figure 83 – Brown-in Test at 1 V / s.
Ch1: I_{OUT}, 10 mA / div.
Ch2: V_{IN}, 100 V / div.
Time Scale: 40 s / div.

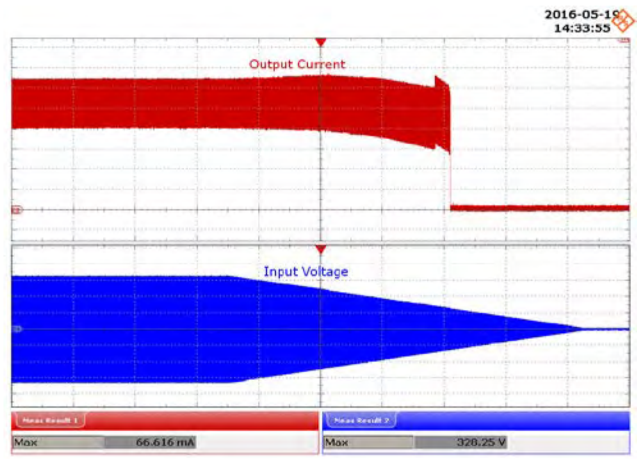

Figure 84 – Brown-out Test at 1 V / s.
Ch1: I_{OUT}, 10 mA / div.
Ch2: V_{IN}, 100 V / div.
Time Scale: 40 s / div.

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17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
22-Jun-16	MGM	1.0	Initial release	Apps & Mktg

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Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

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