Design Example Report

Title	***20 W USB PD Power Supply Using Cypress CCG2 CYPD2134 and InnoSwitch™-CP INN2215K***
Specification	85 VAC – 264 VAC Input; 5 V 3 A; 9 V, 2.2 A Outputs
Application	Mobile Phone Charger
Author	Applications Engineering Department
Document Number	DER-533
Date	June 28, 2016
Revision	1.3

Summary and Features

- InnoSwitch-CP industry first AC/DC IC with isolated, safety rated integrated feedback
- USB-PD compliance via single secondary side IC (CCG2 CYPD2134)
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Built in synchronous rectification for high efficiency
- Meets DOE6 and CoC V5 2016
- <30 mW no-load input power integrated thermal protection
- Primary sensed overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 5 V / 3.0 A or 9 V / 2.2 A output USB Type-C and USB-PD charger using the InnoSwitch-CP and Cypress CCG2 USB Type-C USB-PD Controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch-CP controller providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data

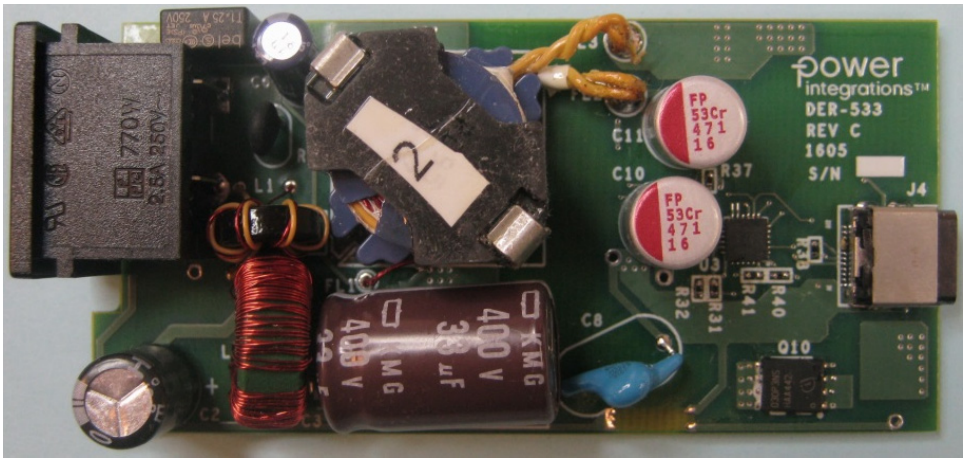

Figure 1 – Populated Circuit Board Photograph, Top.

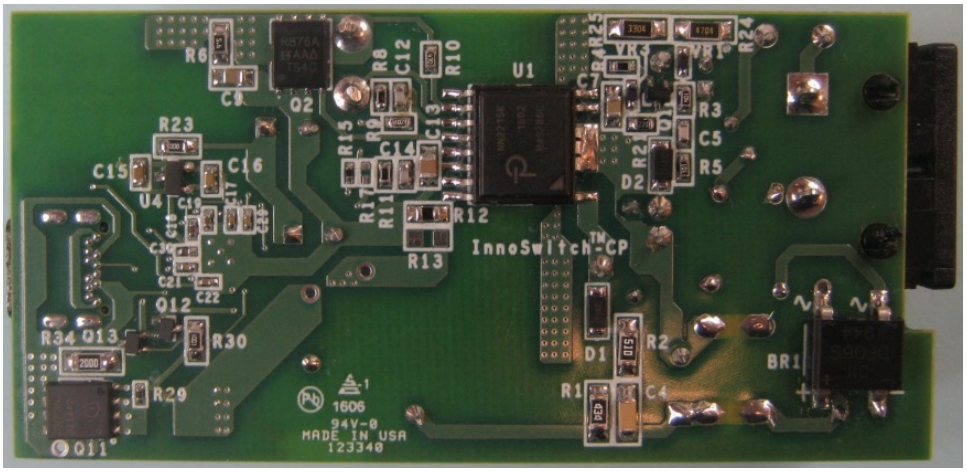

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		264	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)			25	28	mW	Measured at 230 VAC.
5 V Output						
Output Voltage	V_{OUT1}		5		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At the end of cable. Cable needs to have a resistance of 100mΩ.
Output Current	I_{OUT1}	3.0		3.3	A	20 MHz bandwidth.
9 V Output						
Output Voltage	V_{OUT1}		9		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At the end of cable. Cable needs to have a resistance of 100 mΩ.
Output Current	I_{OUT1}				A	At the end of cable. Cable needs to have a resistance of 100 mΩ.
Continuous Output Power	P_{OUT}			20	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

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3 **Schematic**

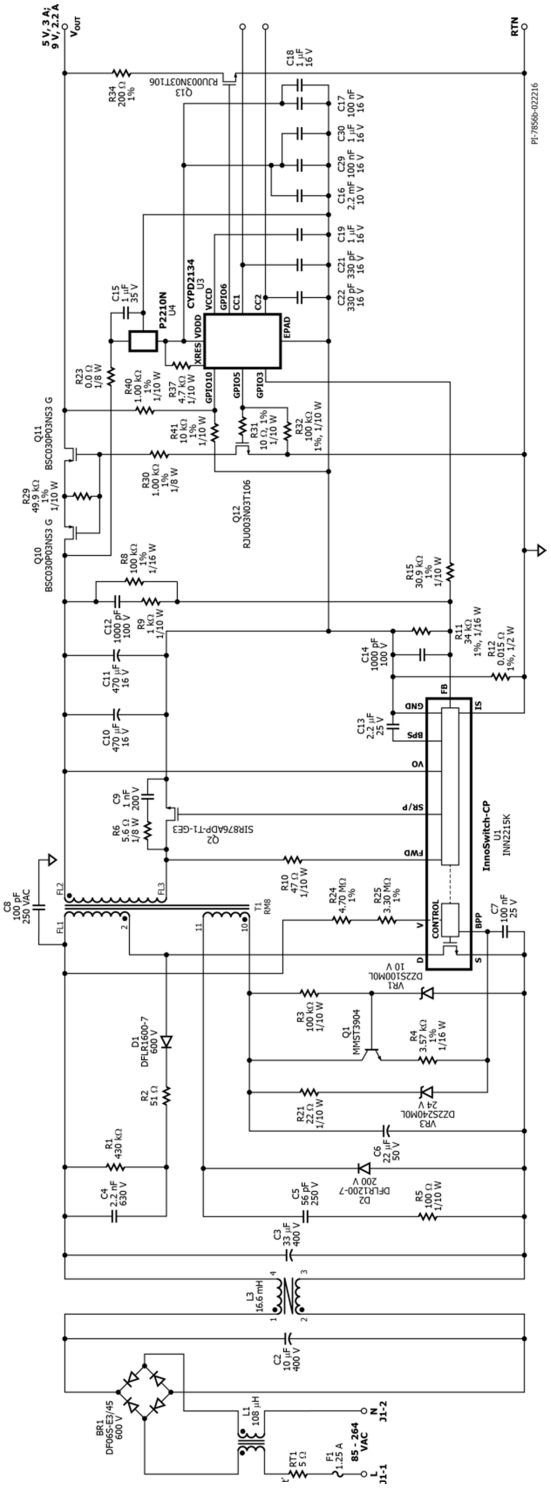

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 with capacitor C8 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C2, L3, and C3. The inductor L3 and capacitors C2, C3 form a pi-filter. This filter provides differential and common mode noise filtering. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

4.2 InnoSwitch-CP IC Primary

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the InnoSwitch-CP IC (U1).

A low cost RCD clamp formed by diode D1, resistors R1 and R2, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C7) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R4 limits the current being supplied to the BPP pin of the InnoSwitch-CP IC (U1). A linear regulator comprising of resistor R3, BJT Q1 and Zener diode VR1 prevent any change in current through R4. The RC network comprising of resistor R5 and capacitor C5 offer damping to the high frequency ringing in the voltage across diode D2 which reduces radiated EMI.

Output regulation is achieved using On/Off control, the number of enabled switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled, and at light load or no-load most cycled are disabled or skipped. Once a cycle is enabled, the MOSFET will remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arranged such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level.

Zener diode VR3 offers primary sensed output over voltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR3 which then causes a current to flow into the BPP pin of InnoSwitch-CP IC U1. If the current flowing into the BPP pin increases above the I_{SD}

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threshold which has a nominal value of 7.6 mA, the InnoSwitch-CP controller will latch off and prevent any further increase in output voltage.

4.3 **InnoSwitch-CP IC Secondary**

The secondary side of the InnoSwitch-CP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R6 and C9.

The gate of Q2 is turned on by secondary side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 24 mV. Secondary side control of the primary side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch-CP IC U1 provides decoupling for the internal circuitry.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C13 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R12 between the IS and GND pins with a threshold of approximately 50 mV to reduce losses. Once the internal current sense threshold is exceeded the device adjusts the number of switch pulses to maintain a fixed output current.

Below the CC threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve a voltage of 1.2 V on the FB pin. Resistor R9 and capacitor C12 form a phase lead network that ensure stable operation and minimize output voltage overshoot and undershoot during transient load conditions. Capacitor C14 provides noise filtering of the signal at the FB pin.

4.4 **USB Type-C and PD Interface**

In this design, CCG2 CYPD2134-24QXIT (U3) is the USB Type-C and PD controller. Output of the InnoSwitch-CP powers the CCG2 device using a 3.3 V linear regulator U4.

Resistors R8 and R11 forms the feedback divider network to sense the output of Innoswitch. Output voltage is changed to 9 V when sink requests for the same. To change the output to 9V, pin-14 of IC U3 goes low and adds resistor R15 in parallel to the bottom resistor of the feedback divider network.

USB-PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which type-C plug is connected.

P-MOSFETS Q10 and Q11 make the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. VBUS_OUT is discharged via resistor R34 by turning on the MOSFET Q13.

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5 PCB Layout

PCB copper thickness is 2.0 oz.

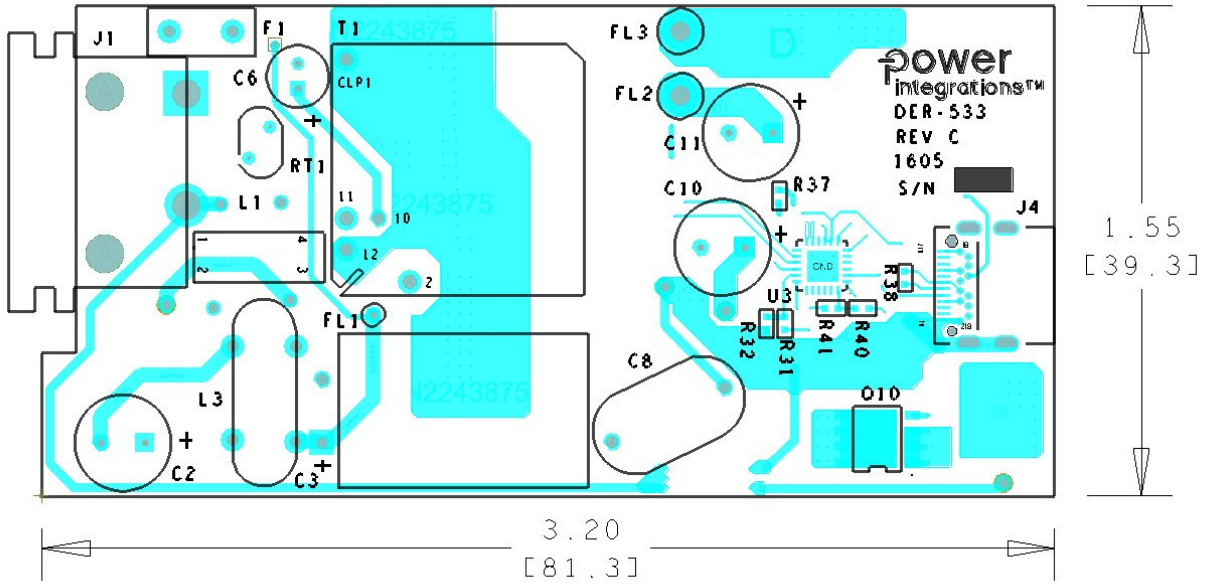

Figure 4 – Printed Circuit Layout, Top.

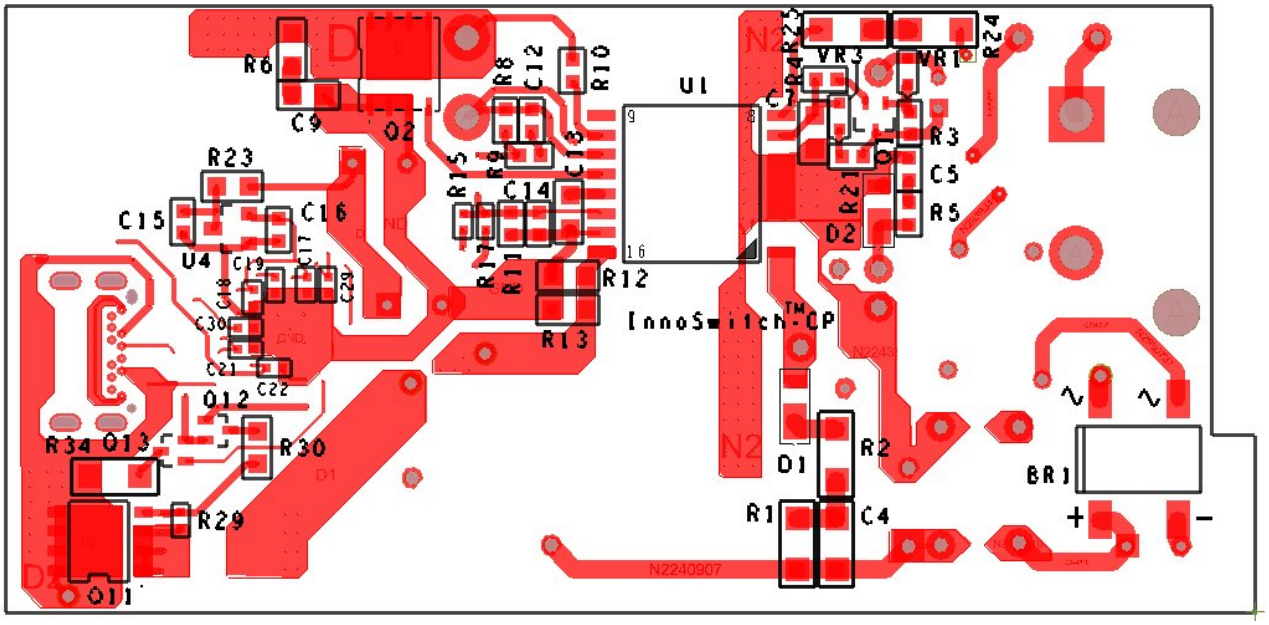

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, SMD, DFS	DF06S-E3/45	Vishay
2	1	C2	10 µF, 400 V, Electrolytic, (8 x 12)	ERK2GM100F12OT	Aishi
3	1	C3	33 µF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
4	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
5	1	C5	56 pF, 250 V, Ceramic, NPO, 0603	GQM1875C2E560JB12D	Murata
6	1	C6	22 uF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
7	1	C7	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
8	1	C8	100 pF, 250 VAC, Film, X1Y1	DE1B3KX101KB4BN01F	TDK
9	1	C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
10	2	C10 C11	470 µF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
11	2	C12 C14	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
12	1	C13	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
13	1	C15	1 µf 35 V, Ceramic, X7R, 0603	C1608X7R1V105M	TDK
14	1	C16	2.2 µF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
15	2	C17 C29	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
16	3	C18 C19 C30	1 µF 16 V, Ceramic, X5R, 0402	C1005X5R1C105M	TDK
17	2	C21 C22	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
18	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
19	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
20	1	F1	FUSE, 1.25A 250VAC, Slow, 8.35 mm x 4.0 mm x 7.7 mm	RST 1.25-BULK	Bel Fuse
21	1	FL1	Flying Lead, Hole size 30 mils	N/A	N/A
22	2	FL2 FL3	Flying Lead, Hole size 70 mils	N/A	N/A
23	1	J1	CONN, AC Recept Panel, R/A, PCB pins	770W-X2/10	Qualtek
24	1	J4	Connector, USB TYPE C, R/A, Receptacle	DX07S024XJ1R1100	JAE Electronics
25	1	L1	Custom, 108 µH, constructed on Core 35T0375-10H	TSD-3761	Premier Magnetics
26	1	L3	16.6 mH, xA, Ferite Toroid, 4 Pin, Output	TSD-3760	Premier Magnetics
27	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
28	1	Q2	100 V, 40 A, N-Channel, PowerPAK SO-8	SIR876ADP-T1-GE3	Vishay
29	2	Q10 Q11	30 V, 100 A, P-Channel, TDSON-8	BSC030P03NS3 G	Infineon
30	2	Q12 Q13	MOSFET, N-CH, 30V, 300MA, SOT-323	RJU003N03T106	Rohm Semi
31	1	R1	RES, 430 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ434V	Panasonic
32	1	R2	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
33	1	R3	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
34	1	R4	RES, 3.57 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3571V	Panasonic
35	1	R5	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
36	1	R6	RES, 5.6 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R6V	Panasonic
37	1	R8	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
38	1	R9	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
39	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
40	1	R11	RES, 34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
41	1	R12	RES, 0.015 Ω, 0.5 W, 1%, 0805	ERJ-6BWFR015V	Panasonic
42	1	R15	RES, 30.9 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3092X	Panasonic
43	1	R21	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
44	1	R23	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
45	1	R24	RES, 4.70 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF4704	Rohm Semi
46	1	R25	RES, 3.30 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3304	Rohm Semi
47	1	R29	RES, 49.9 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4992X	Panasonic
48	1	R30	RES, 1.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
49	1	R31	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic

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50	2	R32 R40	RES, 100.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1003X	Panasonic
51	1	R34	RES, 200 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2000V	Panasonic
52	1	R37	RES, 4.7 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ472X	Panasonic
53	1	R38	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
54	1	R41	RES, 10.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1002X	Panasonic
55	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
56	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer	RM8/12/1 POL-INN015	Schwartzpunkt Premier Magnetics
57	1	U1	InnoSwitch-CP, Off-Line CV/CC Flyback Switcher, ReSOP-16B	INN2215K	Power Integrations
58	1	U3	IC, USB Type-C Port Controller	CYPD2134-24LQXIT	Cypress Semi
59	1	U4	IC, REG, LDO, 3.3V, 0.3A, SOT23-3	P2210N-3.3TRG1	Diodes, Inc.
60	1	VR1	10 V, 5%, 150 mW, SSMINI-2	DZ2S100M0L	Panasonic
61	1	VR3	24 V, 5%, 150 mW, SSMINI-2	DZ2S240M0L	Panasonic

7 Transformer Specification

7.1 Electrical Diagram

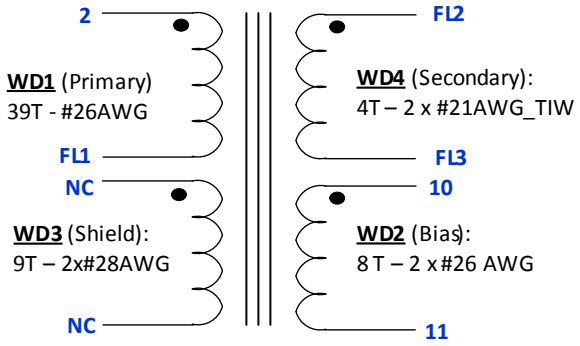

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 2, 10, 12, and FL4 to FL1/FL2.	3000 VAC
Primary Inductance	Pin 2 – FL3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	612 µH, ±5%
Resonant Frequency	Pin 2 – FL3, all other windings open.	1100 kHz (Min.)
Primary Leakage Inductance	Pin 2 – FL3, with pins FL1/FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	16 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: TDK PC95 RM08-Z ,PI # 99-00022-00, or equivalent, gapped for ALG of 392 nH/t^2.
[2]	Bobbin: RM8-12pins(6/6), Ferroxcube-CSV-RM8-1S-12P-G, PI#: 25-01022-00; or equivalent.
[3]	Clip: RM8, Allstar Magnetic, CLI/P-RM8/I.
[4]	Magnet Wire: #26 AWG, solderable double coated.
[5]	Magnet Wire: #28 AWG, solderable double coated.
[6]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[7]	Tape: Polyester Film, 3M 1350-1, 9.0 mm wide.
[8]	Varnish.

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7.4 Transformer Build Diagram

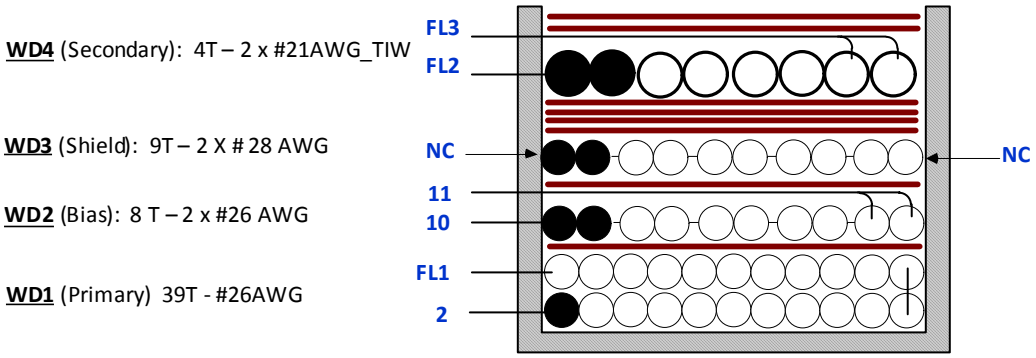
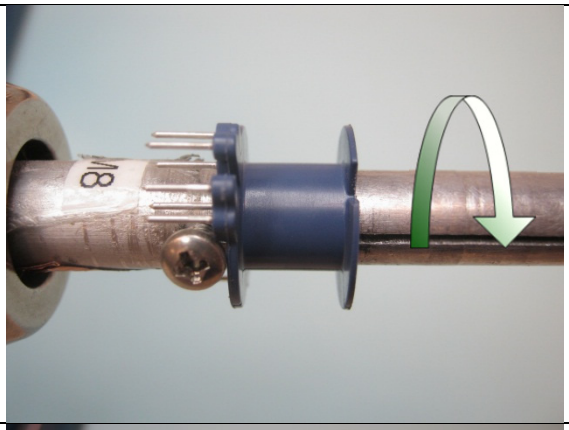
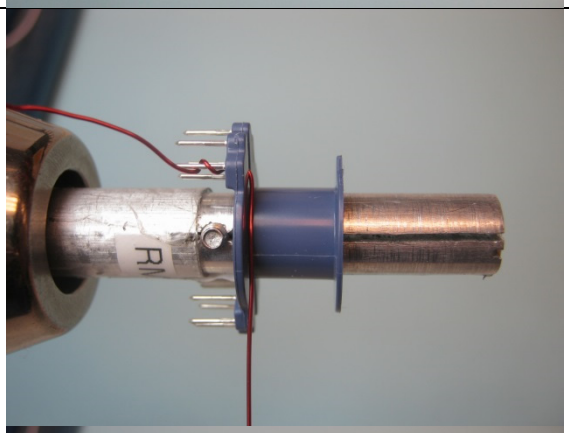
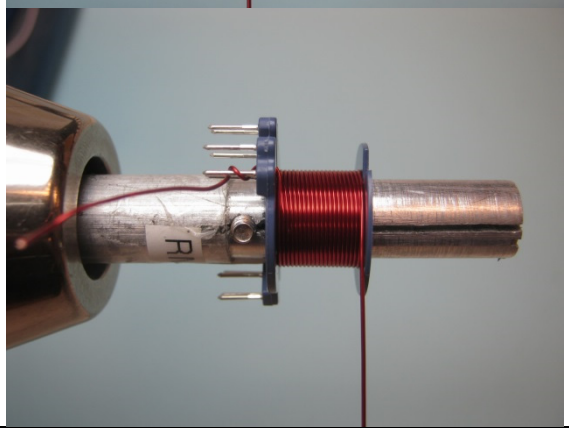


Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary Winding	Start at pin 2. Wind 39 turns of item [4] in approximately 2 layers. Finish as marked FL1.
Insulation	Use 1 layer of item [7] for insulation.
WD2 Bias Winding	Starting at pin 10, wind 8 bifilar turns of item [5]. Spread turns evenly across bobbin. Finish at pin 11.
Insulation	Use 1 layer of item [7] for insulation.
WD3 Shield	Temporarily hang wire item [5] on pin 1 or 2, for start lead, wind 9 bifilar turns of item [5], and spread turns evenly across bobbin. At the last turn cut wire for no-connect, and also cut start lead for no-connect.
Insulation	Use 4 layers of item [7] for insulation.
WD4 Secondary Winding	Take two parallel strands of item [6]. Mark start end as FL2, wind 4 turns of item [6], and finish as FL3.
Insulation	Use 2 layers of item [7] to secure the windings.
Final Assembly	Insert cores, gapped for inductance specified. Secure core halves using clips item [3]. Cut short pins: 1, 3, 4, 5, 6, 7, 8, and 9. Dip varnish item [8].

7.6 **Winding Illustrations**

Bobbin Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary winding**	 	Start at pin 2. Wind 39 turns of item [4] with tight tension in 2 layers. Finish as marked FL1.

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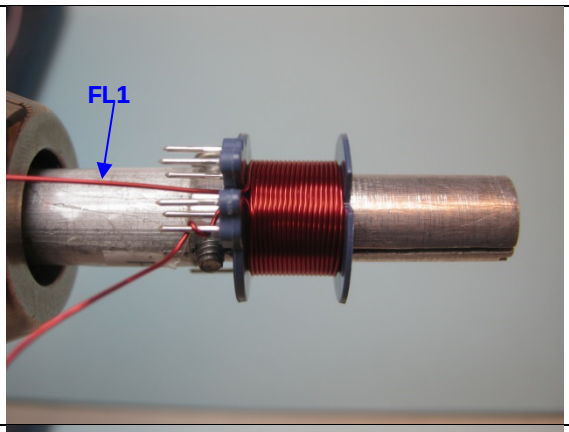
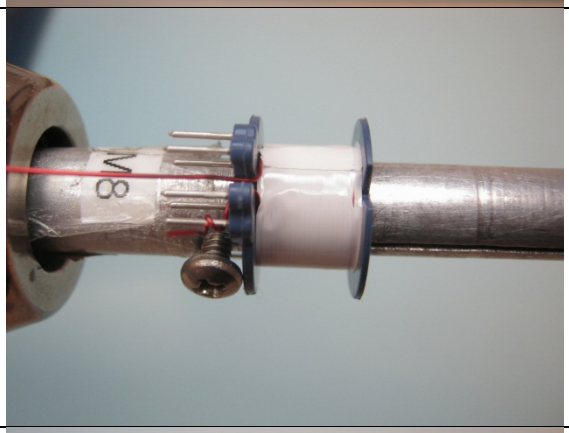
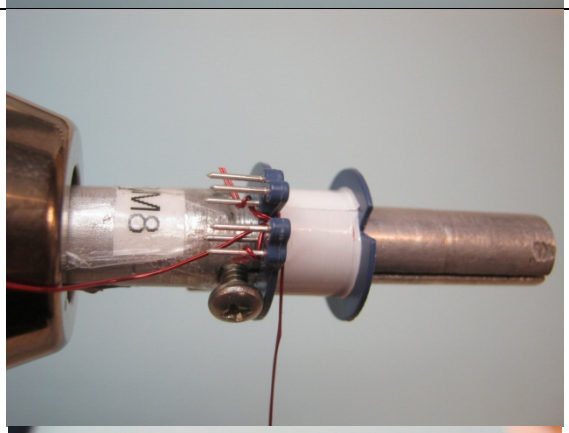
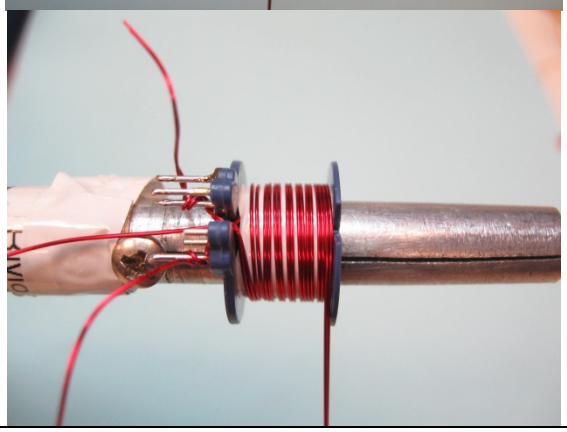
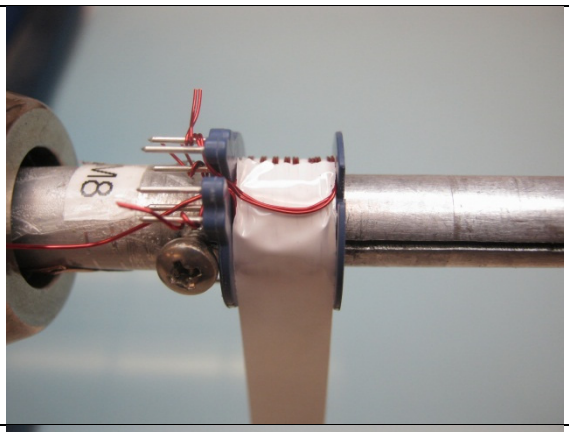
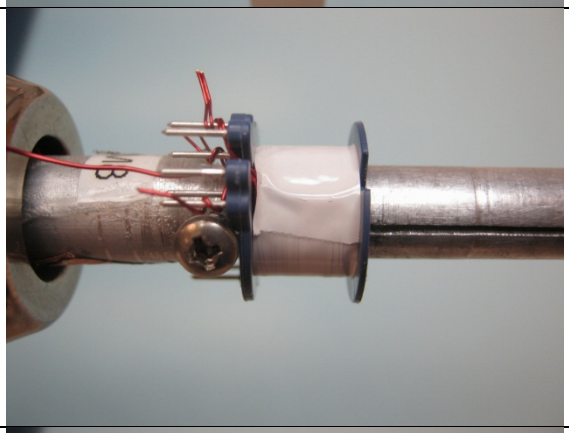
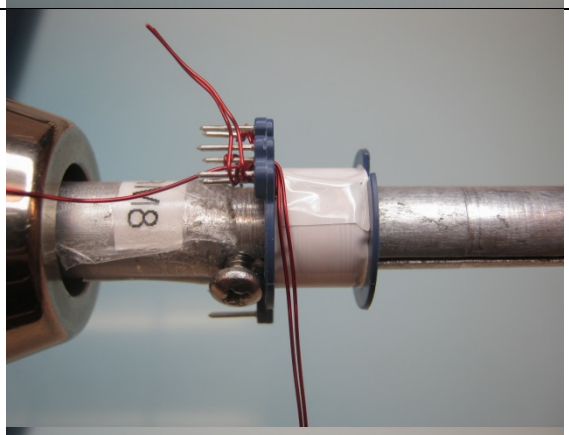
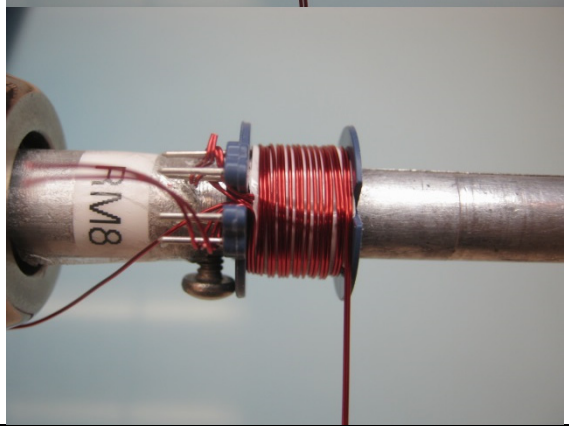
		
Insulation		Use 1 layer of item [7] for insulation.
WD2 **Bias winding**	 	Starting at pin 10, wind 8 bifilar turns of item [4]. Spread turns evenly across bobbin. Finish at pin 11.

		
Insulation		Use 1 layer of item [7] for insulation.
WD3 **Shield**	 	Temporarily hang wire item [5] on pin 1 or 2, for start lead, wind 9 bifilar turns of item [5], and spread turns evenly across bobbin.

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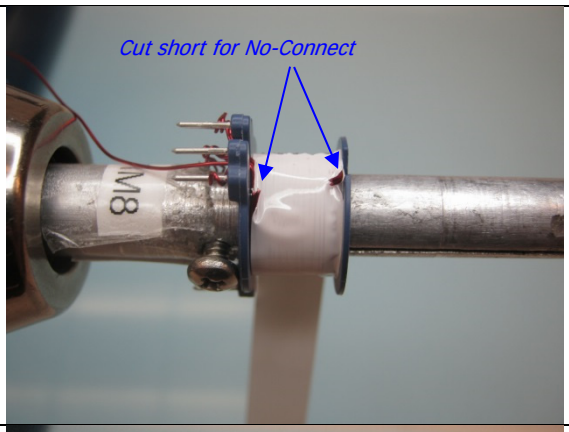
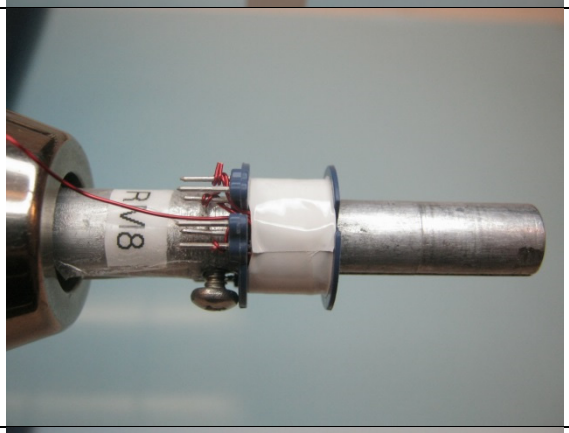
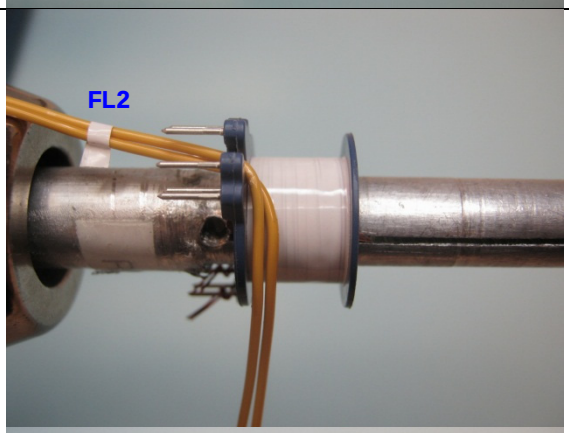
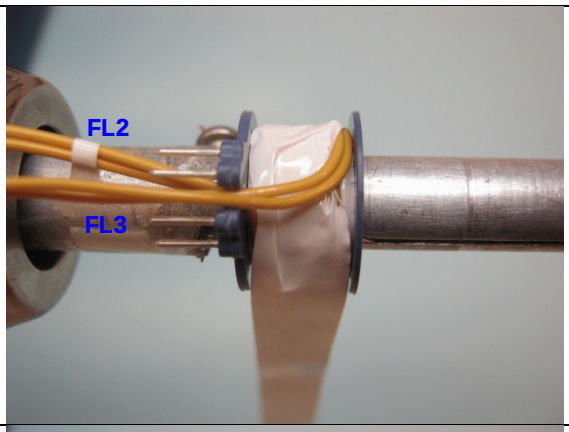
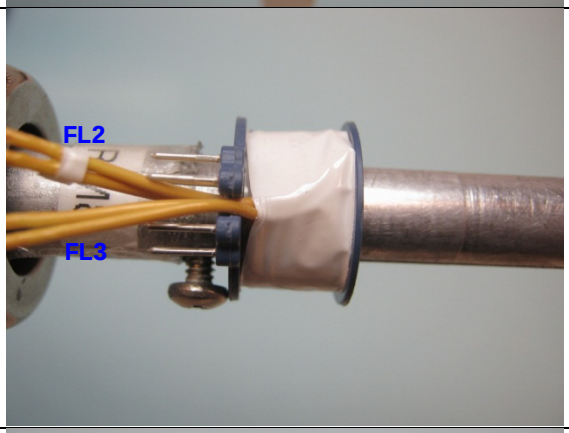
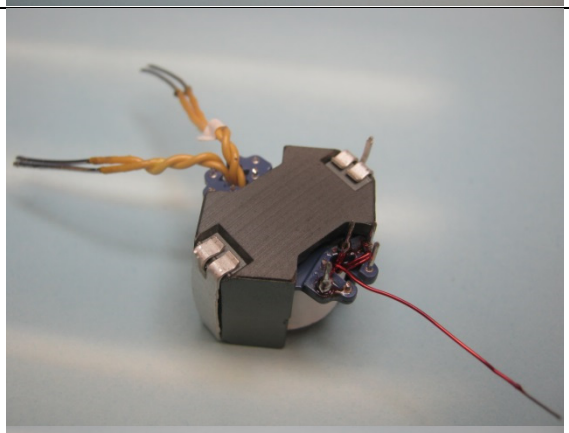
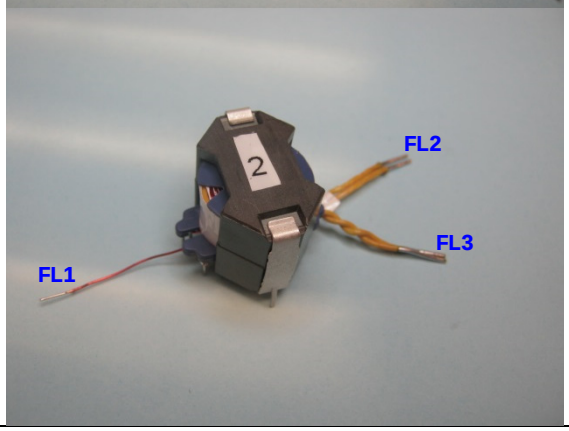
		At the last turn cut wire for no-connect, and also cut start lead for no-connect.
Insulation		Use 4 layers of item [7] for insulation.
WD4 **Secondary winding**	 	Take two parallel strands of item [6]. Mark start end as FL2, wind 4 turns of item [6], and finish as FL3.

		
Insulation		Use 2 layers of item [7] to secure the windings.
Final Assembly	 	Insert cores, gapped for inductance specified. Secure core halves using clips item [3]. Cut short pins: 1, 3, 4, 5, 6, 7, 8, and 9. Dip varnish item [8].

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8 Common Mode Choke Specifications

8.1 *90 µH Common Mode Choke (L1)*

8.1.1 Electrical Diagram

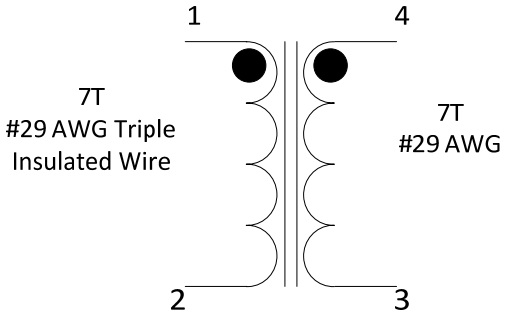


Figure 8 –Inductor Electrical Diagram.

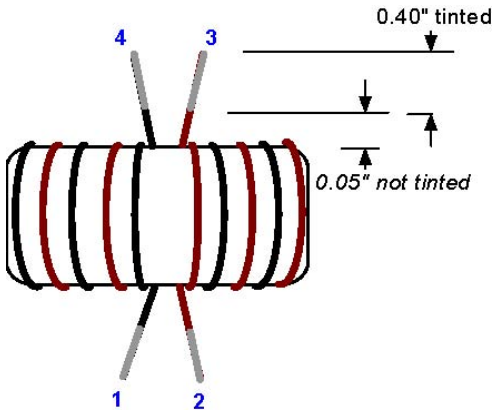
8.1.2 Electrical Specifications

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	108 µH ±20%
Primary Leakage Inductance	Pins 1-2, with 3-4 shorted.	0.5 µH

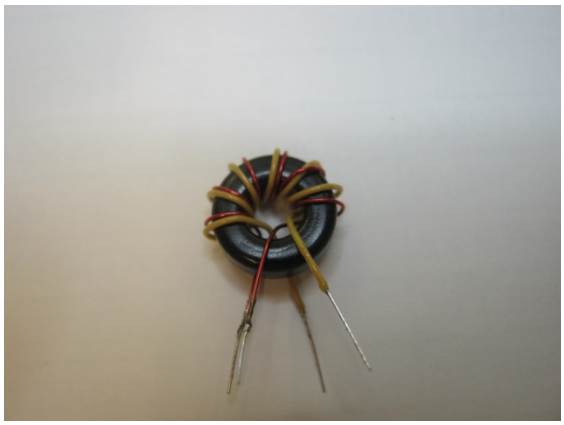
8.1.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID .415" O.D.;Mfg Part number: 35T0375-10H. Dim: 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L.
[2]	Magnet Wire: #29 AWG.
[3]	Triple Insulated Wire #29 AWG.

8.1.4 Illustrations



Top View



Front View

8.2 **10 mH Common Mode Choke (L3)**

8.2.1 Electrical Diagram

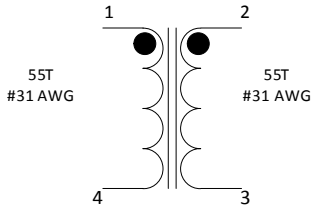


Figure 9 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	16.6 mH ±25%
Core effective Inductance		5500 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	80 µH

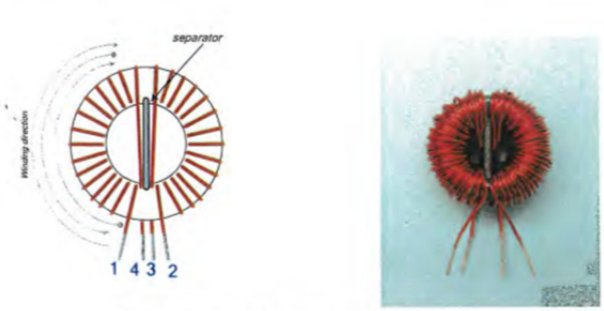
8.2.3 Materials List

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID T14 x 8 x 5.5. PI Part number: #32-00286-00.
	Divider -- Fish paper, insulating cotton rag, 0.010” thick, PI #: 66-00042-00. Cut to size 8 mm x 5.5 mm.
[2]	Magnet Wire: #31 AWG Heavy Nyleze

8.2.4 Winding Instructions

- Use 4 ft of item [2], start at pin 1 wind 55 turns end at pin 4.
- Do the same for another half of Toroid, start at pin 2 and end at pin 3.

8.2.5 Illustrations



Side View

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch-CP_021616; Rev.1.1; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	InnoSwitch-CP Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage. Universal=85VAC to 155VAC. High-Line=185VAC to 215VAC
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC line frequency
VO_1	9.00		9.39	V	Desired output voltage at the end of cable for configuration 1
IO_1	2.14		2.14	A	Output current for configuration 1
Power_1		Info	20.08	W	Specified output power exceeds the device's capability. Increase device size or verify performance on bench
n_1	0.85		0.85		Efficiency Estimate at output terminals for configuration 1. Use 0.8 if no better data available
Z_1	0.50		0.50		Ratio of secondary side losses to the total losses in the power supply for configuration 1. Use 0.5 if no better data available
VO_2	5.00		5.30	V	Desired output voltage at the end of cable for configuration 2
IO_2	3.00		3.00	A	Power Supply Output Current (corresponding to peak power) for configuration 2
Power_2			15.90	W	Continuous Output Power, including cable drop compensation for configuration 2
n_2	0.80		0.80		Efficiency Estimate at output terminals for configuration 2. Use 0.8 if no better data available
Z_2	0.50		0.50		Ratio of secondary side losses to the total losses in the power supply for configuration 2. Use 0.5 if no better data available
VO_3			0.00	V	Configuration 3 is turned off
IO_3			0.00	A	Configuration 3 is turned off
Power_3			0.00	W	Configuration 3 is turned off
n_3	0.80		0.80		Configuration 3 is turned off
Z_3	0.50		0.50		Configuration 3 is turned off
VO_4			0.00	V	Configuration 4 is turned off
IO_4			0.00	A	Configuration 4 is turned off
Power_4			0.00	W	Configuration 4 is turned off
n_4	0.80		0.80		Configuration 4 is turned off
Z_4	0.50		0.50		Configuration 4 is turned off
tC	3.00		3.00	mS	Bridge Rectifier Conduction Time Estimate
CIN	43.00		43.00	uF	Input capacitor
Enclosure	Adapter		Adapter		Select between Adapter and Open Frame
Cable compensation type	Potential Divider		Potential Divider		The output voltage is varied by varying the lower feedback resistor
ENTER InnoSwitch-RC VARIABLES					
InnoSwitch-RC	**Auto**		**INN2215**		Recommended InnoSwitch-CP
Cable drop compensation	**6%**		**6%**		Select Cable Drop Compensation option.
Complete Part Number			**INN2215K**		Final part number including package
Chose Configuration	**STD**		**Standard Current Limit**		Enter "RED" for reduced current limit, "STD" for standard current limit or "INC" for increased current limit
ILIMITMIN			0.893	A	Minimum Current Limit
ILIMITTYP			0.950	A	Typical Current Limit
ILIMITMAX			1.007	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency

I^2fmin			78.52	A^2kHz	Worst case I2f for power delivery
VOR	88		88	V	Reflected output voltage assigned to configuration 1
VDS	5.00		5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.435		Minimum Value of KP given all configurations and i2f conditions
KP_TRANSIENT			0.289		Minimum Value of KP_TRANSIENT given all configurations and i2f conditions
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Minimum bias winding voltage. Bias voltage will be higher for higher output voltages. Verify performance on the bench.
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			8.00	V	Minimum bias winding number of turns to ensure the minimum bias winding voltage.
PIVB			119.63	V	Minimum PIV rating of the bias diode given all configurations and i2f conditions.
ENTER TRANSFORMER CORE VARIABLES					
Core Type	**RM8**		**RM8**		Enter Transformer Core
Core			PC47RM8Z-12		Enter core part number, if necessary
Bobbin			BRM8-718CPFR		Enter bobbin part number, if necessary
AE			0.64	cm^2	Core Effective Cross Sectional Area
LE			3.80	cm	Core Effective Path Length
AL			1950	nH/T^2	Ungapped Core Effective Inductance
BW			9.05	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
LAYERS_PRIMARY			2		Number of Primary Layers
NS	4		4		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			79	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
PRIMARY CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.543		Maximum value of DMAX given all configurations and i2f conditions
IP_AVG			0.294	A	Maximum value of the average primary current given all configurations and i2f conditions
IP_PEAK			1.014	A	Maximum value of the peak primary current given all configurations and i2f conditions
IP_RMS			0.532	A	Maximum value of the primary RMS current given all configurations and i2f conditions
IP_RIPPLE			0.745	A	Maximum value of the primary ripple current given all configurations and i2f conditions
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			612	uHenry	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 532 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			39		Primary Winding Number of Turns
ALG			402	nH/T^2	Gapped Core Effective Inductance
BM			2610	Gauss	Maximum operating flux density given all configurations and i2f conditions
BAC			867	Gauss	Maximum AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) given all configurations and i2f conditions
ur			921		Relative Permeability of Ungapped Core
LG			0.16	mm	Gap Length (Lg > 0.1 mm)
BWE			18.1	mm	Effective Bobbin Width
OD			0.46	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.40	mm	Bare conductor diameter

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AWGP			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CMP			203	Cmils	Bare conductor effective area in circular mils
CMAP			382	Cmils/Amp	Primary wire circular mils per amp
CDP			5.2	A/mm^2	Primary wire current density
SECONDARY CURRENT WAVEFORM SHAPE PARAMETERS					
IS_PEAK			9.818	A	Maximum value of the peak secondary current, given all configurations and i2f conditions
IS_RMS			6.007	A	Maximum value of the secondary RMS current, given all configurations and i2f conditions
IS_RIPPLE			5.204	A	Maximum value of the output capacitor RMS ripple current, given all configurations and i2f conditions
TRANSFORMER SECONDARY DESIGN PARAMETERS					
NS			4		Number of secondary turns
CMS			1201	Cmils	Secondary Bare Conductor minimum circular mils
CMAS			200	Cmils/Amp	Worst-case cecondary wire circular mils per amp given all configurations and i2f conditions
CDS			9.2	A/mm^2	Worst-case secondary wire current density given all configurations and i2f conditions
AWGS			19	AWG	Worst-case secondary wire gauge (Rounded up to next larger standard AWG value) given all configurations and i2f conditions
DIAS			0.91	mm	Minimum Bare Conductor Diameter
ODS			2.26	mm	Maximum Outside Diameter for Triple Insulated Wire
SECONDARY SR FET DESIGN PARAMETERS					
SRFET	**Auto**		Si7456		Recommended SR FET for the design
RDSON_HOT			0.0420	Ohms	RDSon at 100C
PIV_rated			100	V	Rated voltage of selected SR FET
VD			0.098	V	Output Synchronous Rectification FET Forward Voltage Drop
PD			1.545	W	Output Synchronous Rectification FET Power Dissipation
VOLTAGE STRESS PARAMETERS					
VDRAIN			570	V	Maximum Drain Voltage Estimate
PIVS			63	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
DESIGN CONFIGURATION PARAMETERS					
Configuration	**1**		1		Select the configuration number
VO			9.00	V	Output voltage at the end of the cable for the selected configuration
IO			2.14	A	Output current for the selected configuration
PO			20.08	W	Output power at the end of the cable for the selected configuration
n			0.85		Efficiency for the selected configuration
Z			0.50		Loss allocation factor for the selected configuration
DMAX			0.543		DMAX for the selected configuration
VOR			87.8	V	VOR for the desired configuration
KP			0.733		KP for the selected configuration
KP_transient			0.520		KP_transient for the selected configuration
IPP			1.01	A	Primary switch peak current given all i2f conditions
IPRMS			0.53	A	Primary switch RMS current given all i2f conditions
IPRIPPLE			0.74	A	Primary switch current ripple given all i2f conditions
ISP			9.82	A	Secondary switch peak current given all i2f conditions
ISRMS			4.77	A	Secondary switch RMS current given all i2f conditions
ISRIPPLE			4.26	A	Secondary switch curent ripple given all i2f conditions

10 **Performance Data**

Note: Connector mechanical tolerances in the USB Type-C connectors from certain manufactures have been found to have a loose fit which either does not allow the connector on the cable to mate with the connector on the board or causes intermittent connections. Full Load Efficiency vs. Line (at the end of 100 mΩ Resistor)

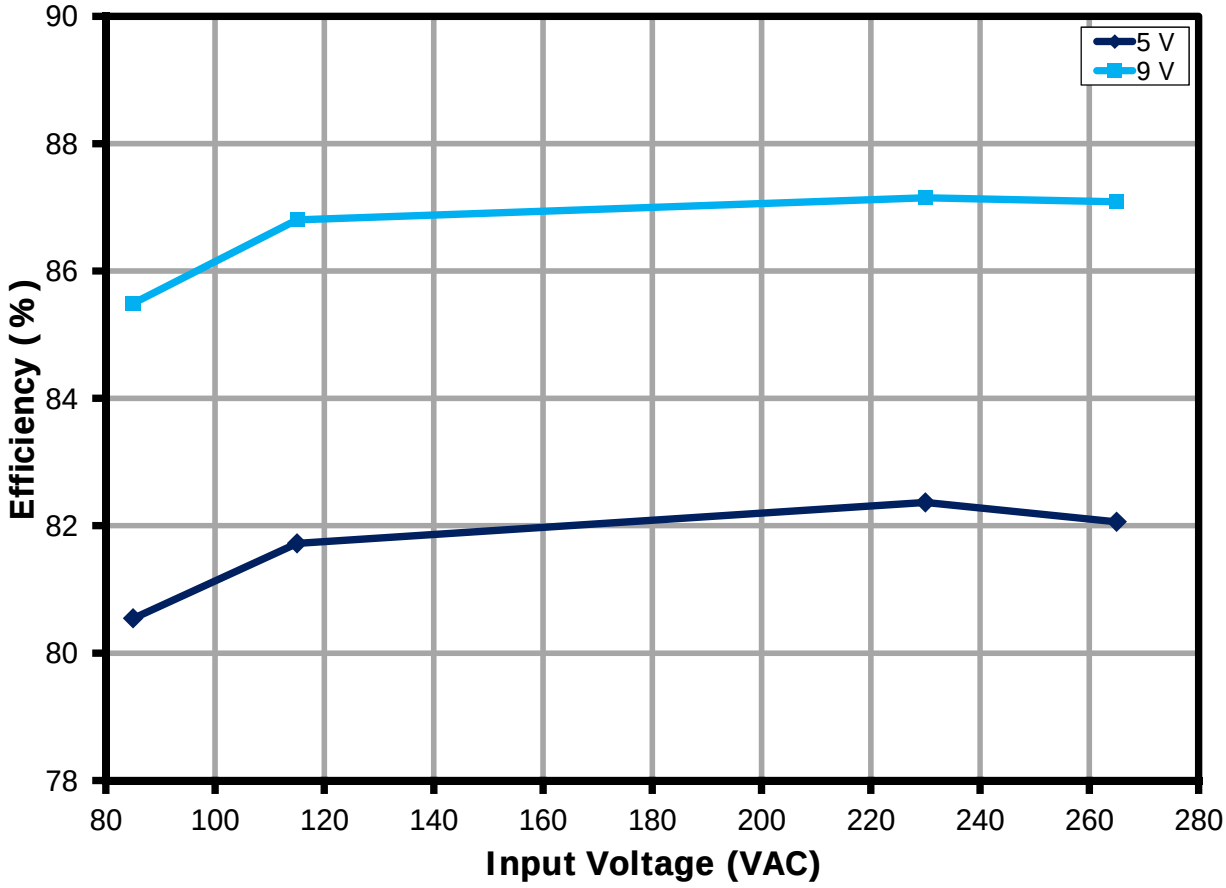

Figure 10 – Efficiency vs. Line Voltage, Room Temperature.

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10.1 Efficiency vs. Load (at the End of 100 mΩ Resistor)

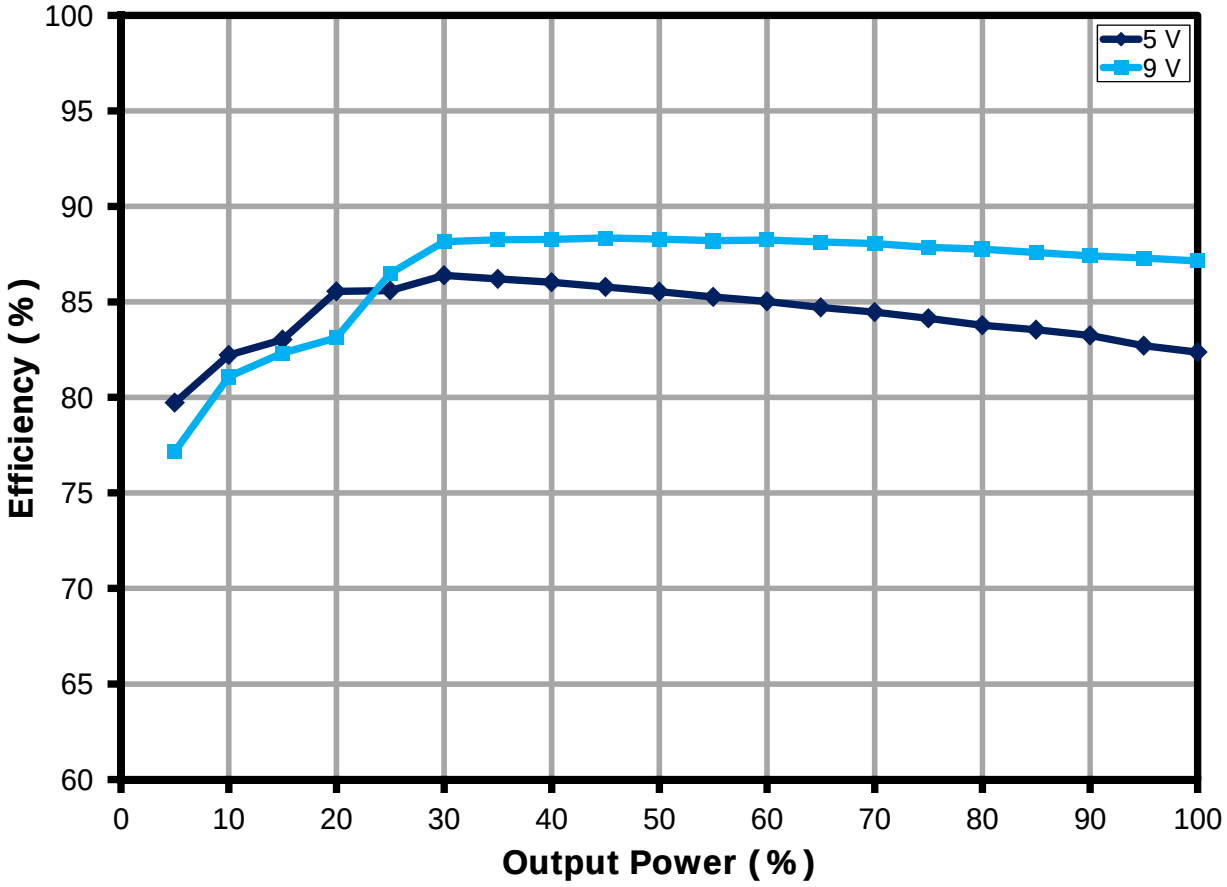

Figure 11 – Efficiency vs. Load, Room Ambient. 115 VAC.

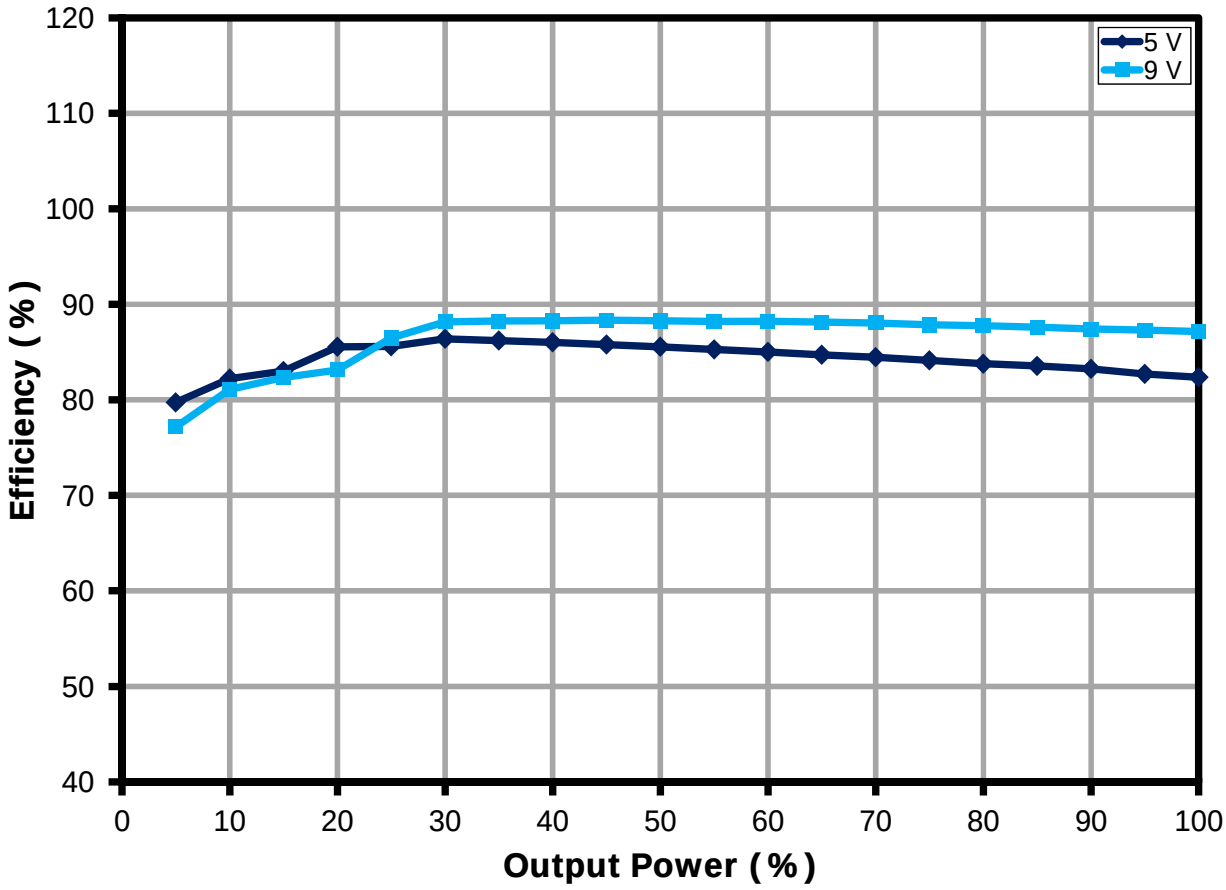

Figure 12 – Efficiency vs. Load, Room Ambient. 230 VAC.

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10.2 No-Load Input Power at 5 V_{OUT}

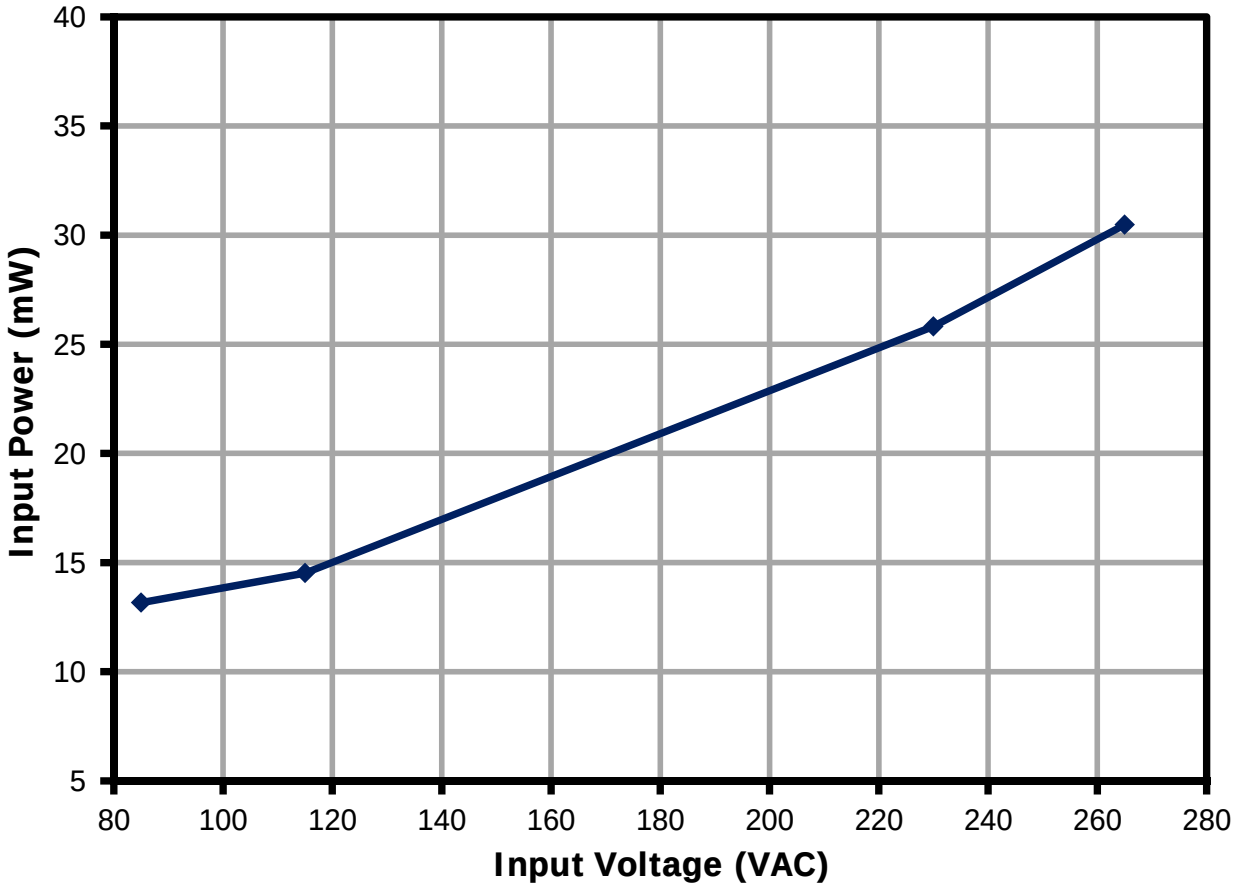

Figure 13 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.3 **Average Efficiency (at the End of 100 mΩ Resistor)**

10.3.1 Average Efficiency Requirements

Test	Average	Average	10% Load
Model	>6 V Voltage	>6 V Voltage	>6 V Voltage
Regulation	**New IESA2007**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
Required Efficiency	**85.5%**	**86.0%**	**76.0%**

Test	Average	Average	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage
Regulation	**New IESA2007**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
Required Efficiency	**81.4%**	**81.8%**	**72.5%**

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10.4 Average Efficiency and 10 % Load at 115 VAC Input

10.4.1 5.0 V Out

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	14.71	81.72	
75%	11.18	83.98	
50%	7.48	85.61	
25%	3.75	86.62	84.48
10%	1.5	84.94	

10.4.2 9.0 V Out

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	20.26	86.8	
75%	15.17	87.69	
50%	10.11	88.36	
25%	5.03	88.11	87.74
10%	1.75	83.00	

10.5 Average Efficiency at 230 VAC Input and 10 % Load

10.5.1 5.0 V Out

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	14.76	82.36	
75%	11.20	84.14	
50%	7.50	85.54	
25%	3.75	85.599	84.41
10%	1.93	83.79	

10.5.2 9.0 V Out

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	20.34	87.14	
75%	15.26	87.85	
50%	10.12	88.28	
25%	5.03	86.48	87.44
10%	1.75	81.14	

10.6 **Line and Load Regulation**

10.6.1 Line Regulation (at USB Socket)

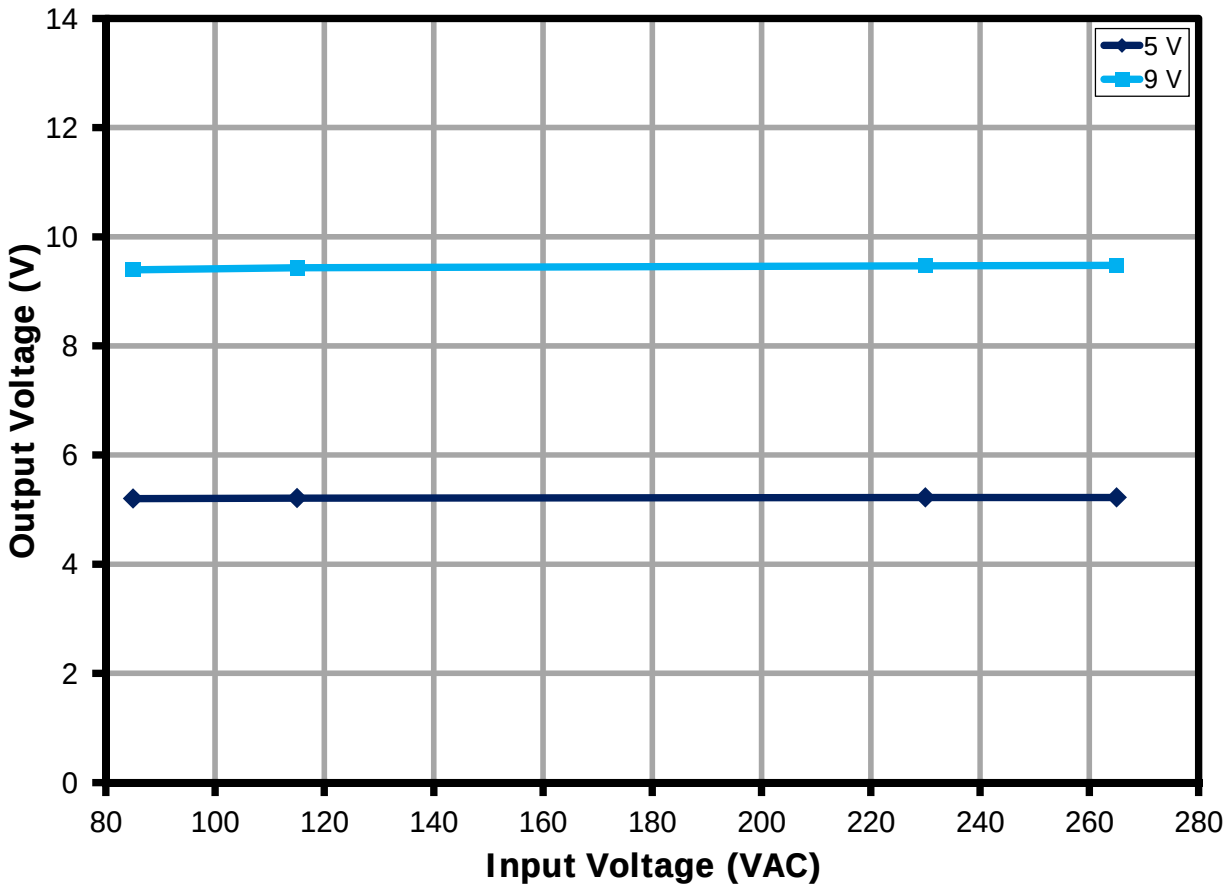

Figure 14 – Output Voltage vs. Input Line Voltage, Room Temperature.

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10.6.2 Load Regulation (at USB Socket)

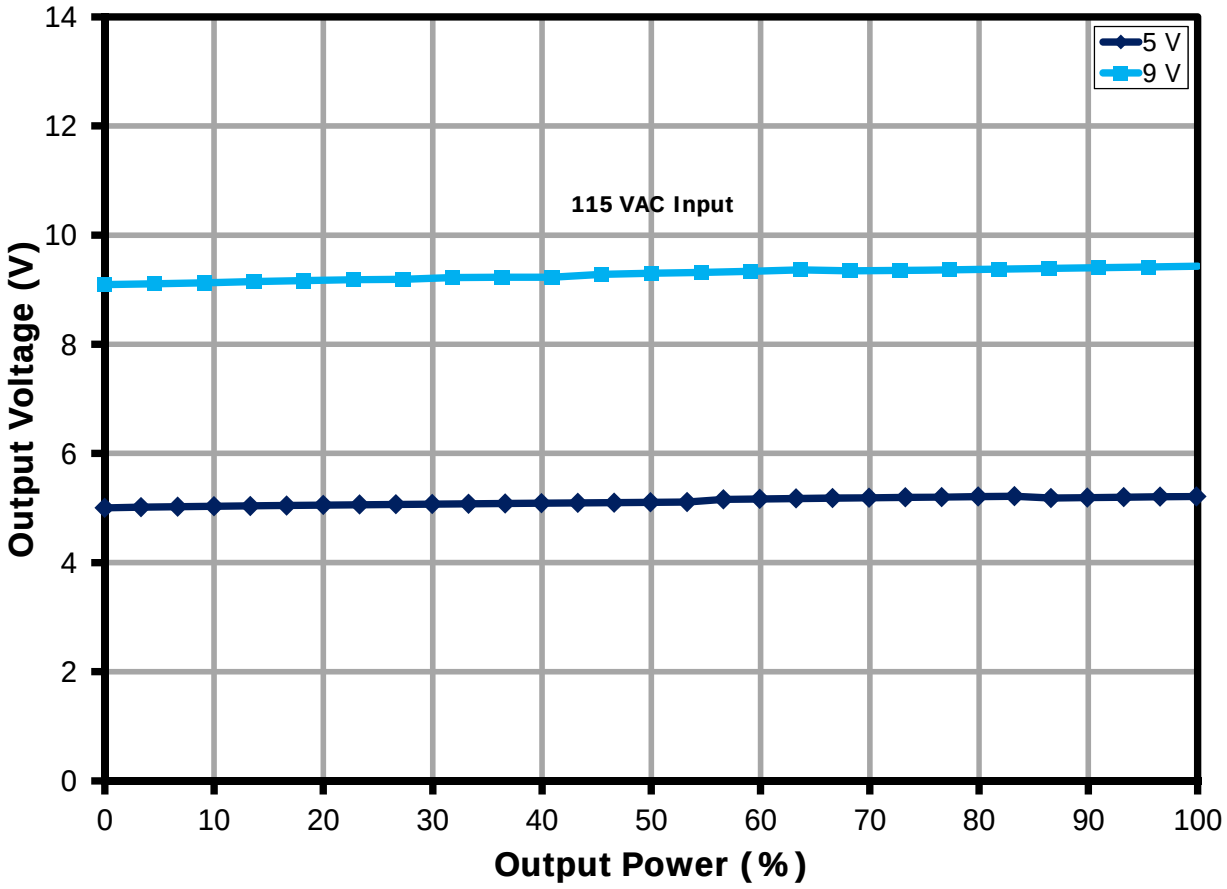

Figure 15 – Output Voltage vs. Output Load, Room Temperature. 115 VAC.

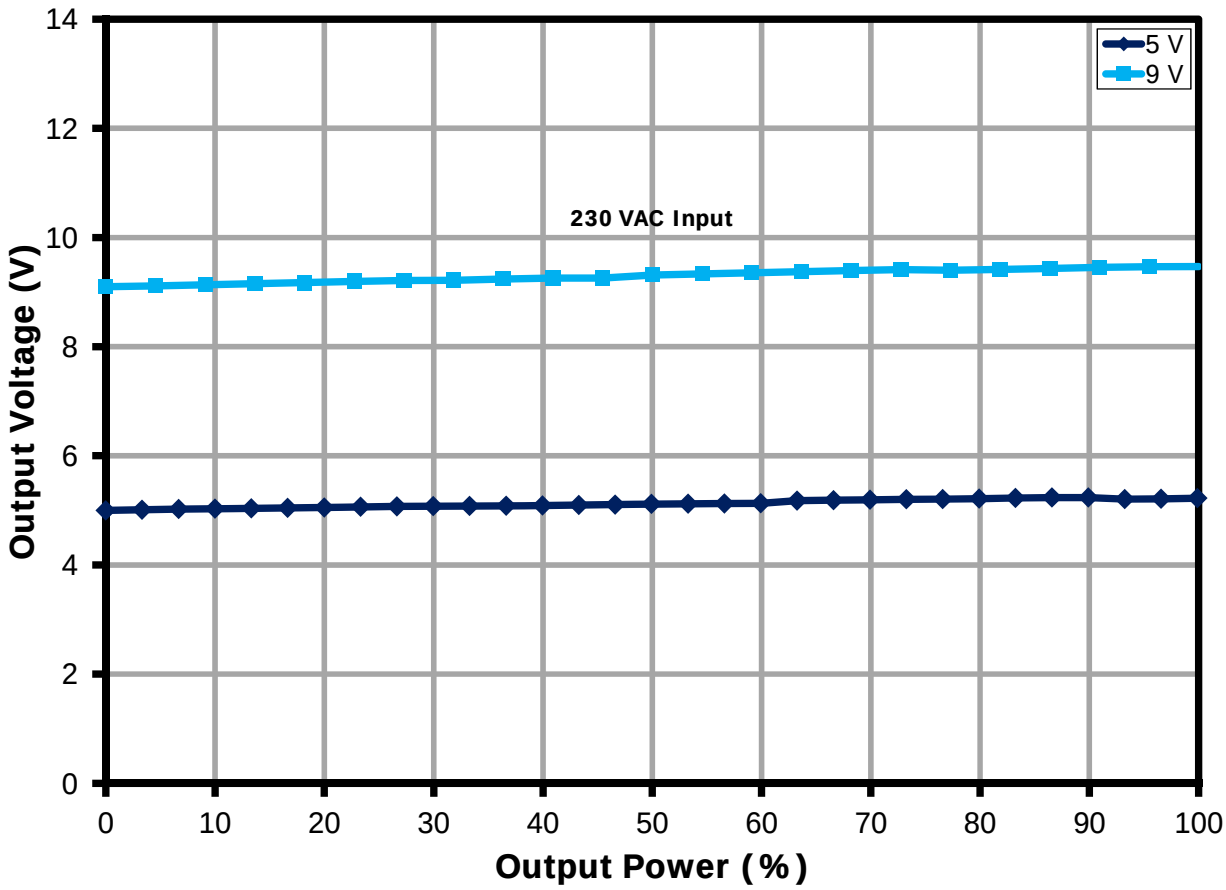

Figure 16 – Output Voltage vs. Output Load, Room Temperature. 230 VAC.

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10.7 CV/CC vs. Line (at the USB Socket)

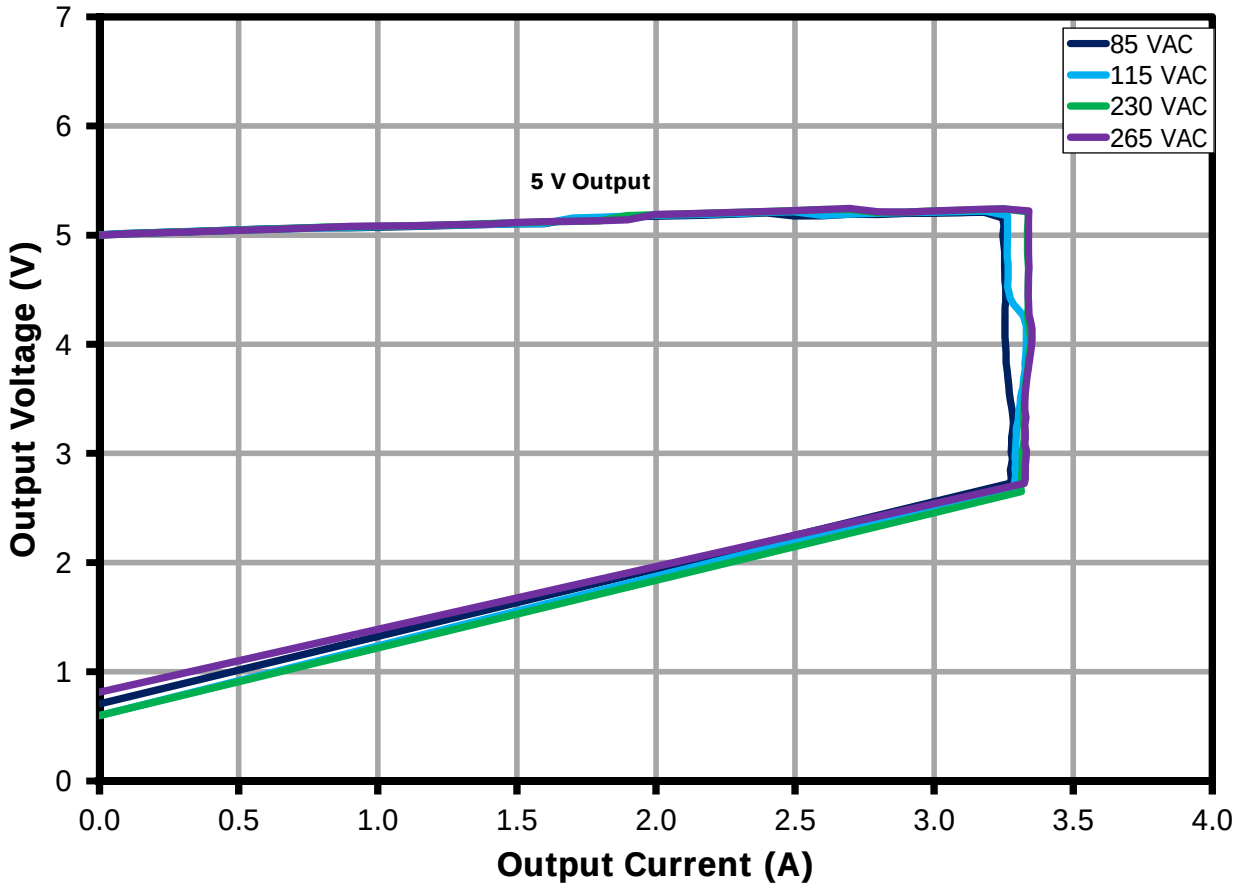

Figure 17 – Output Voltage vs. Output Current, Room Temperature. 5 V Output.

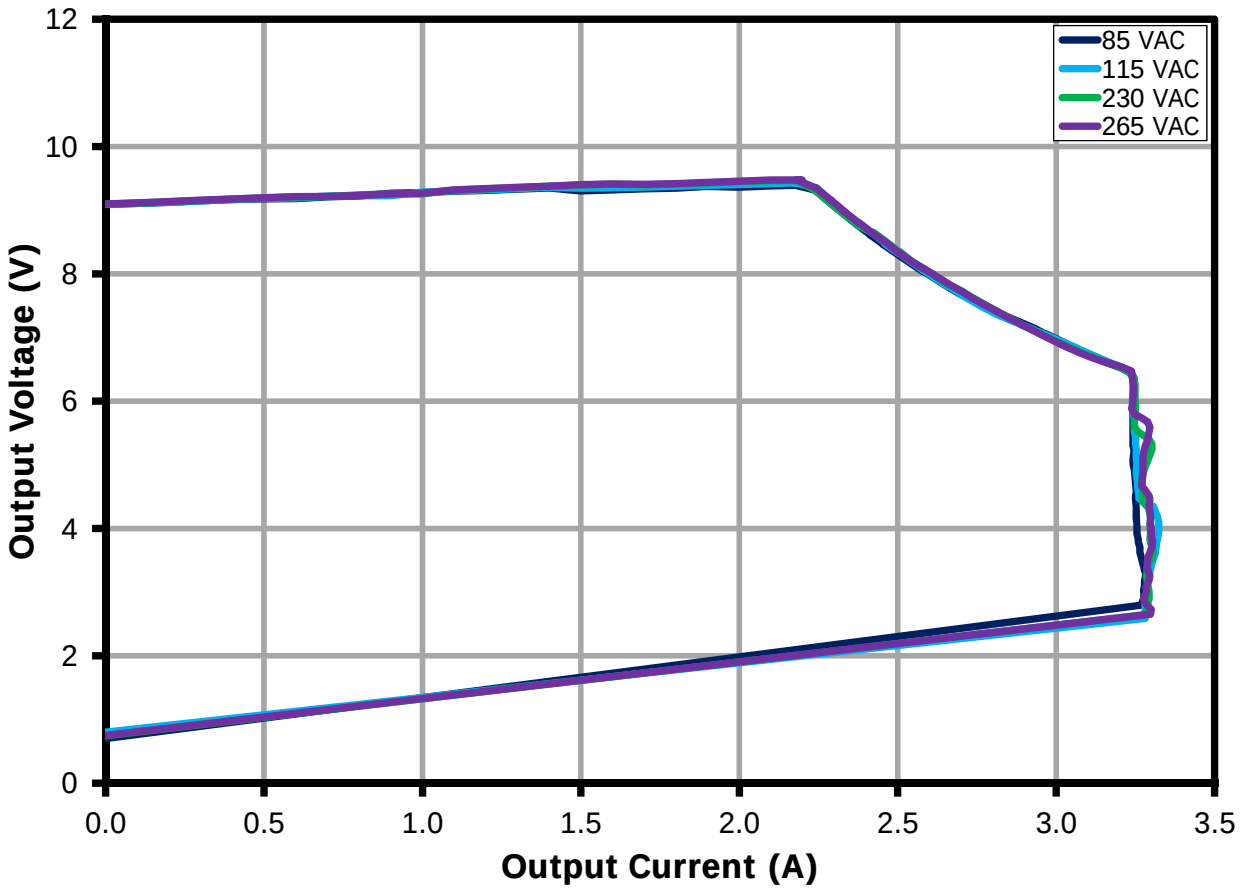

Figure 18 – Output Voltage vs. Output Current, Room Temperature. 9 V Output.

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11 Thermal Performance in Open Case at 9 V / 2.2 A Output

11.1 85 VAC Input

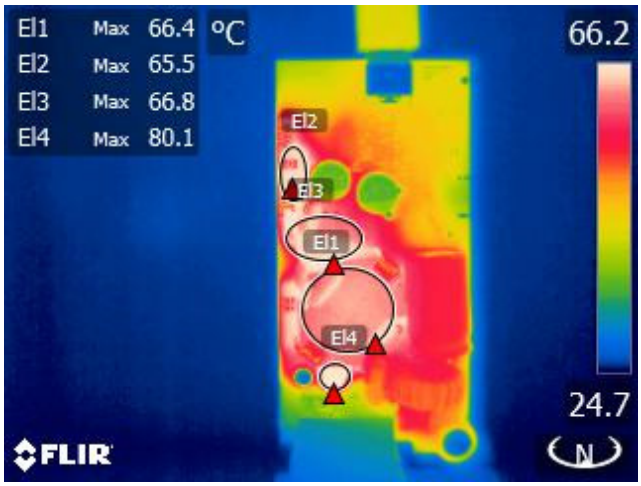

Figure 19 – Transformer Side.
Ambient = 26.2 ºC.
Transformer, T1 = 66.4 ºC.
SR-FET Top, Q2 = 65.5 ºC.
Thermistor, RT1 = 80.1 ºC.

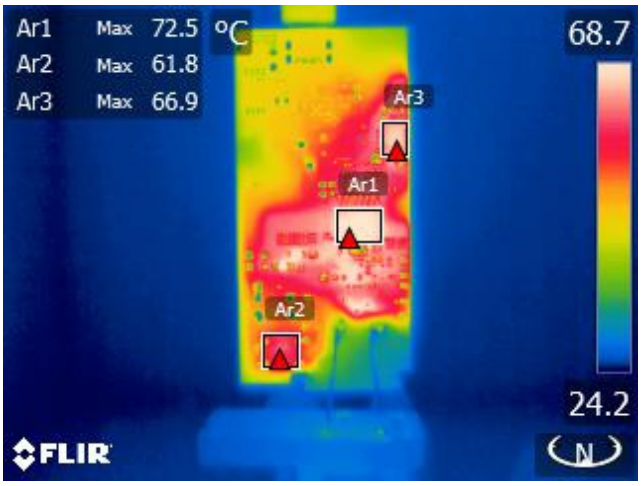

Figure 20 – InnoSwitch-CP Side.
Ambient = 26.2 ºC.
InnoSwitch-CP, U1 = 72.5 ºC.
SR FET, Q2 = 66.9 ºC.
Bridge Rectifier, BR1 = 61.8 ºC.

11.2 115 VAC Input

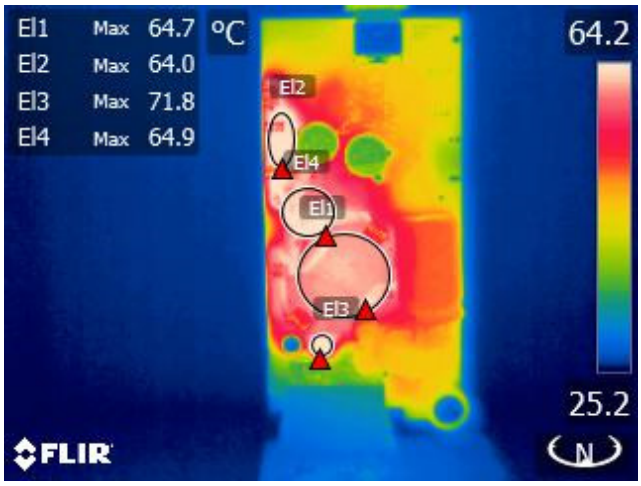

Figure 21 – Transformer Side.
Ambient = 26.2 ºC.
Transformer, T1 = 64.7 ºC.
SR-FET Top, Q2 = 64.0 ºC.
Thermistor, RT1 = 71.8 ºC.

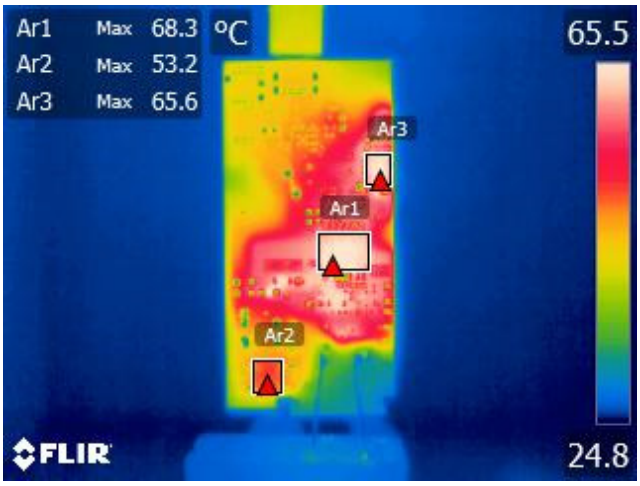

Figure 22 – InnoSwitch-CP Side.
Ambient = 26.2 ºC.
InnoSwitch-CP, U1 = 68.3 ºC.
SR FET, Q2 = 65.6 ºC.
Bridge Rectifier, BR1 = 53.2 ºC.

11.3 **230 VAC Input**

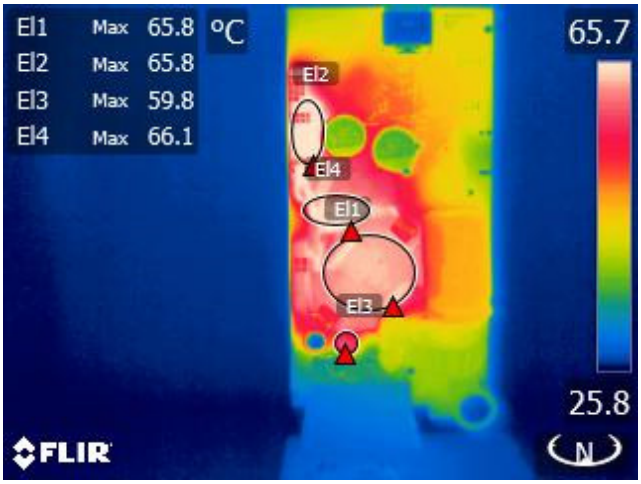

Figure 23 – Transformer Side.
Ambient = 26.2 ºC.
Transformer, T1 = 65.8 ºC.
SR-FET Top, Q2 = 65.8 ºC.
Thermistor, RT1 = 59.8 ºC.

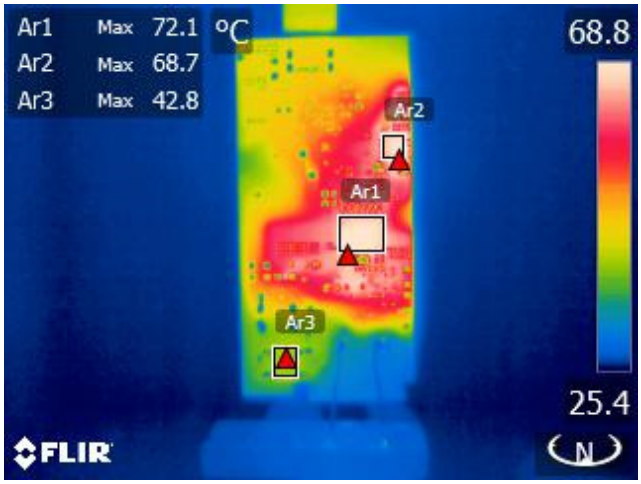

Figure 24 – InnoSwitch-CP Side.
Ambient = 26.2 ºC.
InnoSwitch-CP, U1 = 72.1 ºC.
SR FET, Q2 = 68.7 ºC.
Bridge Rectifier, BR1 = 42.8 ºC.

11.4 **265 VAC Input**

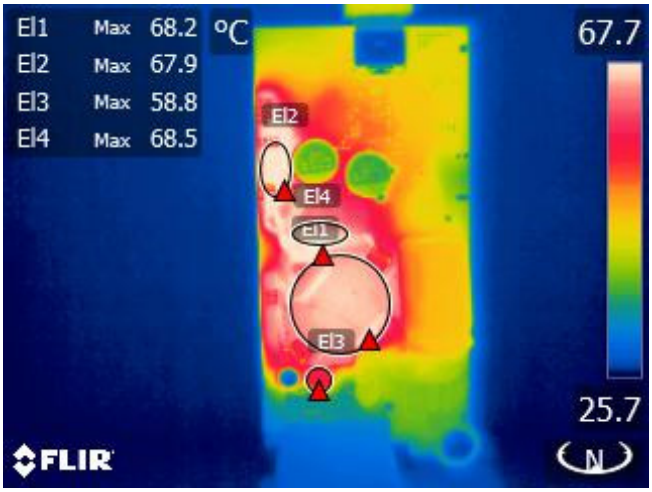

Figure 25 – Transformer Side.
Ambient = 26.2 ºC.
Transformer, T1 = 68.2 ºC.
SR-FET Top, Q2 = 67.9 ºC.
Thermistor, RT1 = 58.8 ºC.

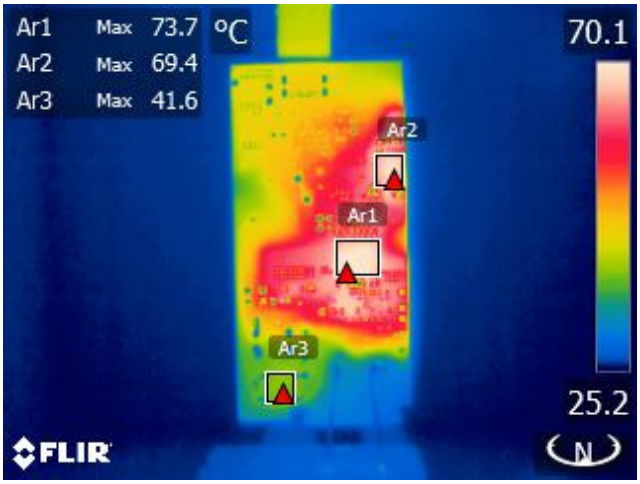

Figure 26 – InnoSwitch-CP Side.
Ambient = 26.2 ºC.
InnoSwitch-CP, U1 = 73.7 ºC.
SR FET, Q2 = 69.4 ºC.
Bridge Rectifier BR1 = 41.6 ºC.

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12 Waveforms

12.1 Load Transient Response (at the End of the Cable)

Note: This test demonstrates change of output voltage from 5 V to 9 V and from 9 V to 5 V with a load of 2.2 A connected at the output of the charger. A USB-PD host board from Cypress Semiconductor [CY4504 Rev 05] was used for the test

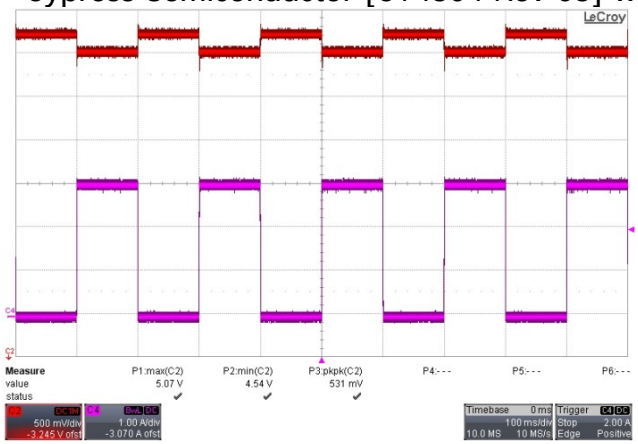

Figure 27 – Transient Response.
85 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN} 4.54 V, V_{MAX}: 5.07 V.
Upper: V_{OUT}, 0.5 V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

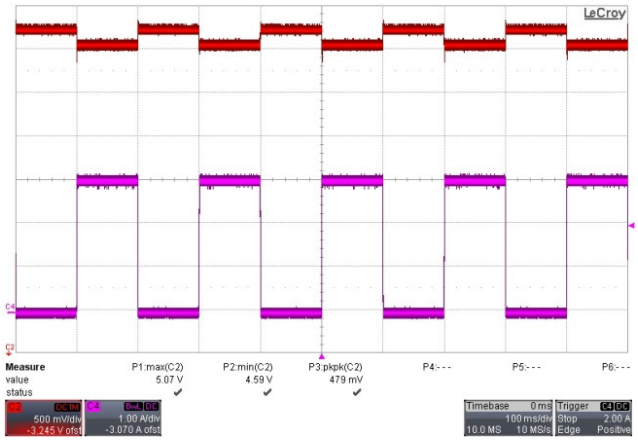

Figure 28 – Transient Response.
265 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN} 4.59 V, V_{MAX}: 5.07 V.
Upper: V_{OUT}, 0.5 V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

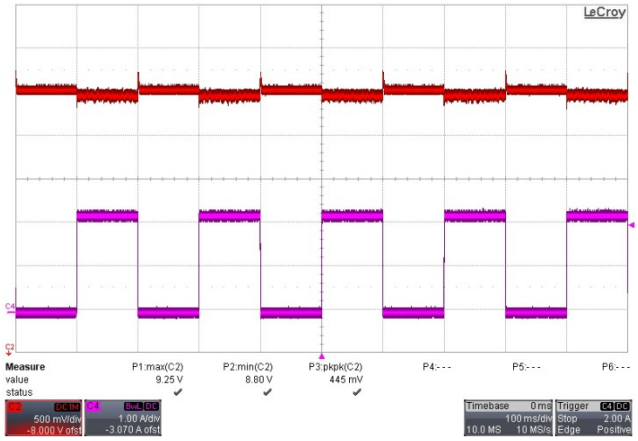

Figure 29 – Transient Response.
85 VAC, 9 V, 0 – 2.2 A Load Step.
V_{MIN}: 8.80 V, V_{MAX}: 9.25 V.
Upper: V_{OUT}, .5 V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

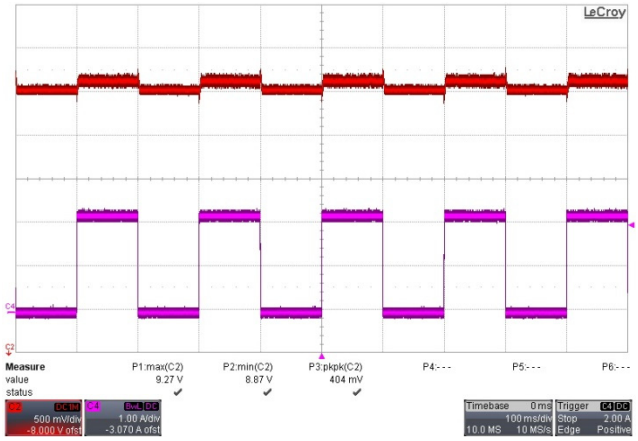

Figure 30 – Transient Response.
265 VAC, 9 V, 0 – 2.2 A Load Step.
V_{MIN}: 8.87 V, V_{MAX}: 9.27 V.
Upper: V_{OUT}, .5 V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

12.2 **Switching Waveforms**

12.2.1 Drain Voltage and Current

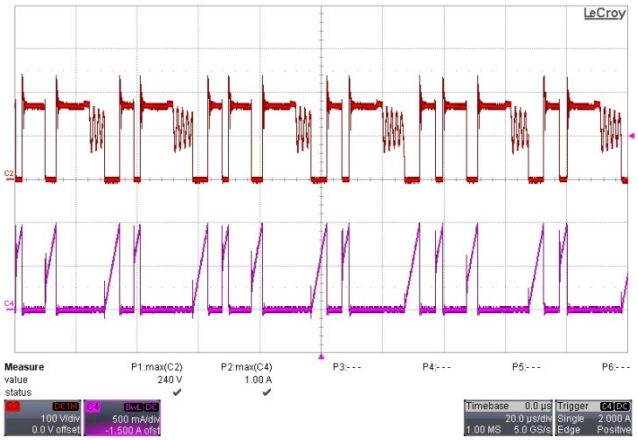

Figure 31 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3 A Load, (240 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

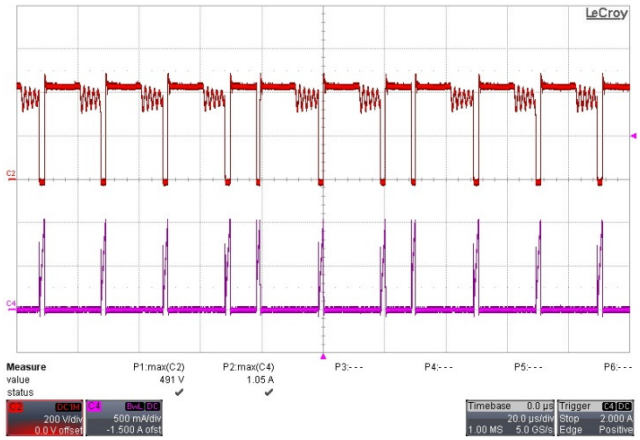

Figure 32 – Drain Voltage and Current Waveforms.
265 VAC, 5 V, 3 A Load, (491 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

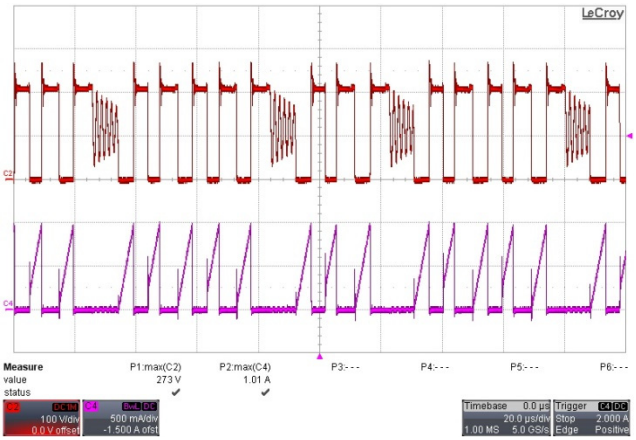

Figure 33 – Drain Voltage and Current Waveforms.
85 VAC, 9.0 V, 2.2 A Load, (273 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

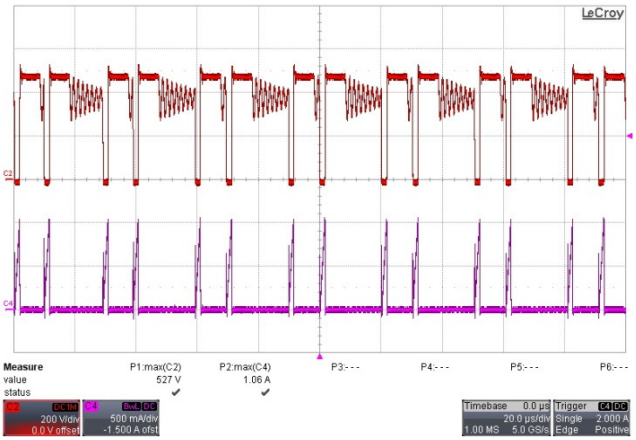

Figure 34 – Drain Voltage and Current Waveforms.
265 VAC, 9 V, 2.2 A Load, (527 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

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12.2.2 Drain Voltage and Current Start-up

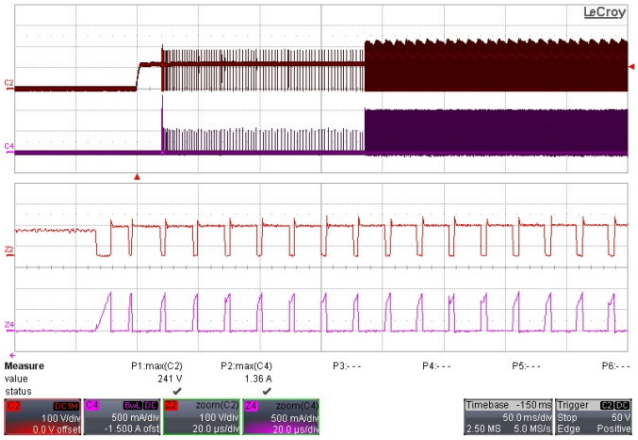

Figure 35 – Drain Voltage and Current Waveforms.
85 VAC, 5 V, 3 A Load, (241 V_{MAX})
Upper: V_{DRAIN}, 100 V, 50 ms, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

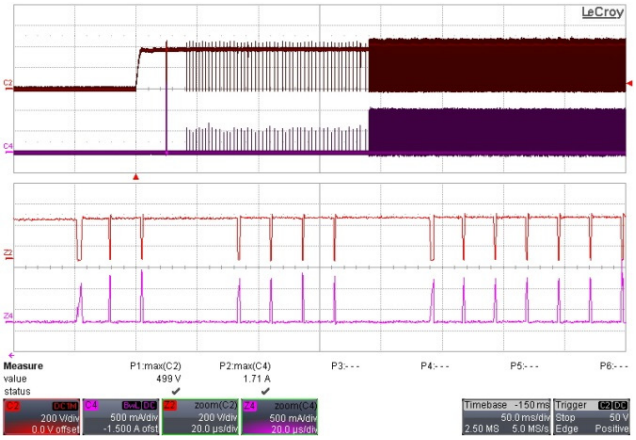

Figure 36 – Drain Voltage and Current Waveforms.
265 VAC, 5 V, 3 A Load, (499 V_{MAX})
Upper: V_{DRAIN}, 200 V, 50 ms, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

12.2.3 SR FET Voltage

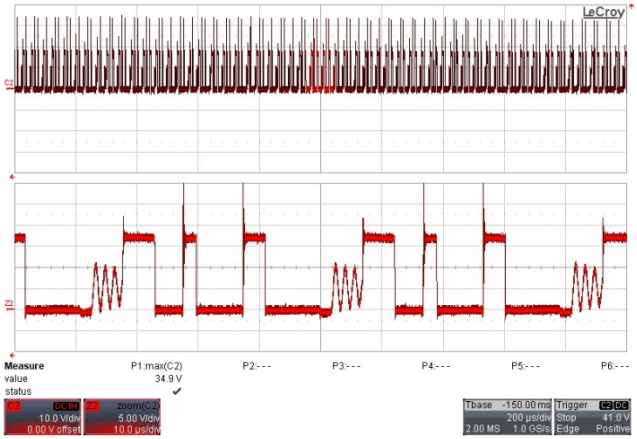

Figure 37 – SR FET Voltage Waveforms.
85 VAC, 5 V, 3 A Load, (34.9 V_{MAX}).
V_{DRAIN}, 10 V, 200 µs, 10 µs / div.

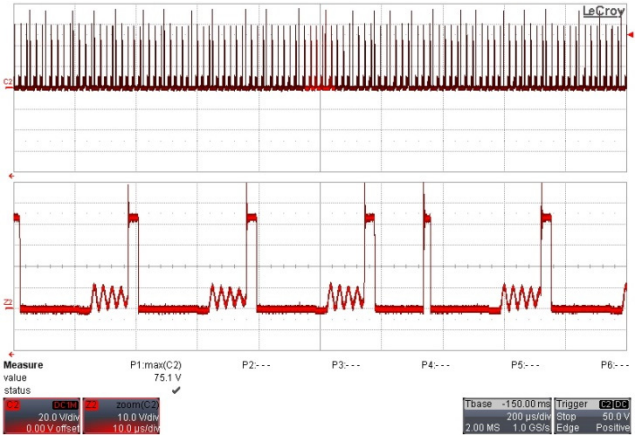

Figure 38 – SR FET Voltage Waveforms.
265 VAC, 5 V, 3 A Load, (75.1 V_{MAX}).
V_{DRAIN}, 20 V, 200 µs, 10 µs / div.

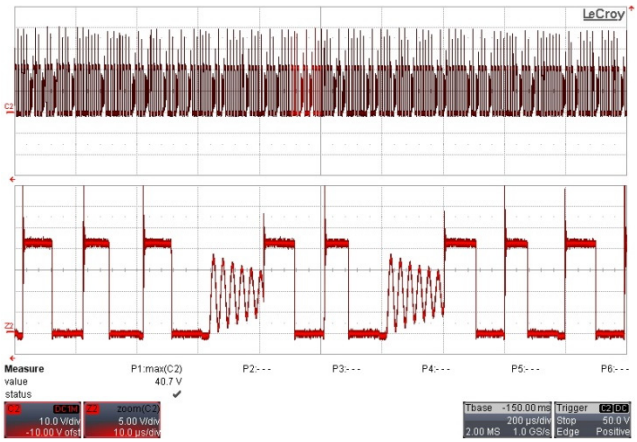

Figure 39 – SR FET Voltage Waveforms.
85 VAC, 9 V, 2.2 A Load, (40.7 V_{MAX}).
V_{DRAIN}, 10 V, 200 µs, 10 µs / div.

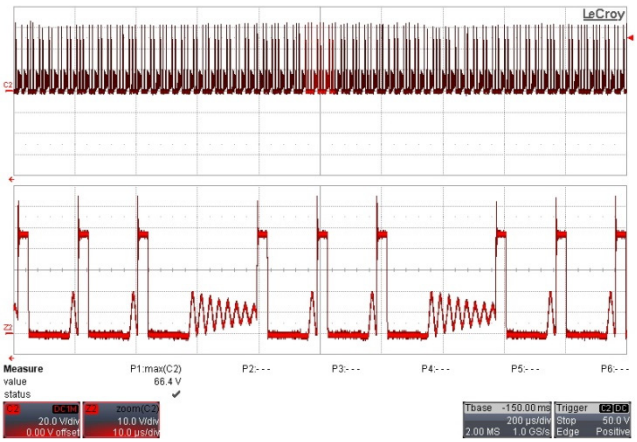

Figure 40 – SR FET Voltage Waveforms.
265 VAC, 9 V, 2.2 A Load, (66.4 V_{MAX}).
V_{DRAIN}, 20 V, 200 µs, 10 µs / div.

12.2.4 Output Voltage and Current Start-up (at End of the Cable)

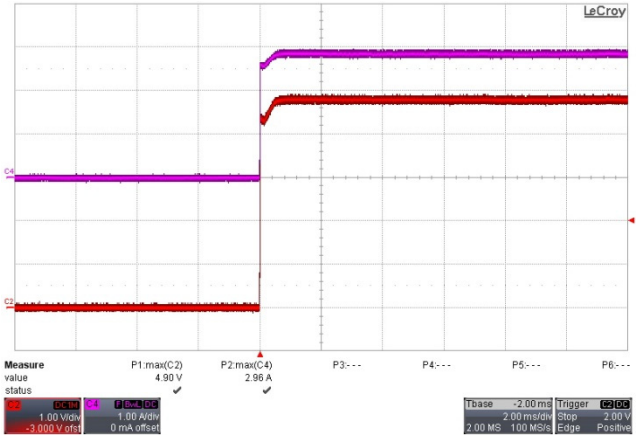

Figure 41 – Output Voltage and Current Waveforms.
85 VAC Input, 1.66 Ω Load .
Upper: I_{OUT}, 1 A, 2 ms / div.
Lower: V_{OUT}, 1 V / div.

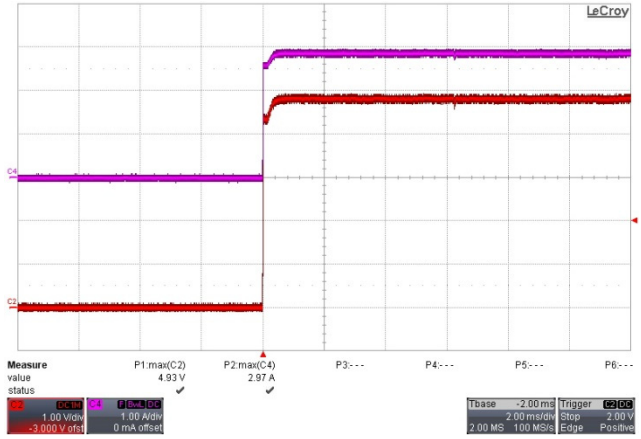

Figure 42 – Output Voltage and Current Waveforms.
265 VAC Input, 1.66 Ω Load.
Upper: I_{OUT}, 1 A, 2 ms / div.
Lower: V_{OUT}, 1 V / div.

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12.3 **Output Voltage Change (Measured at the End of the Cable)**

12.3.1 Output Voltage Change (USB-PD)

12.3.1.1 2.2 A Load

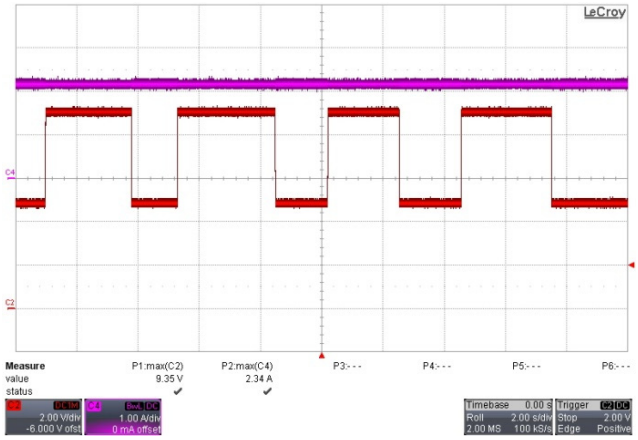

Figure 43 – Output Voltage and Current Waveforms.
85 VAC Input, 2.2 A Load.
Upper: I_{OUT}, 1 A, 2 s / div.
Lower: V_{OUT}, 2 V / div.

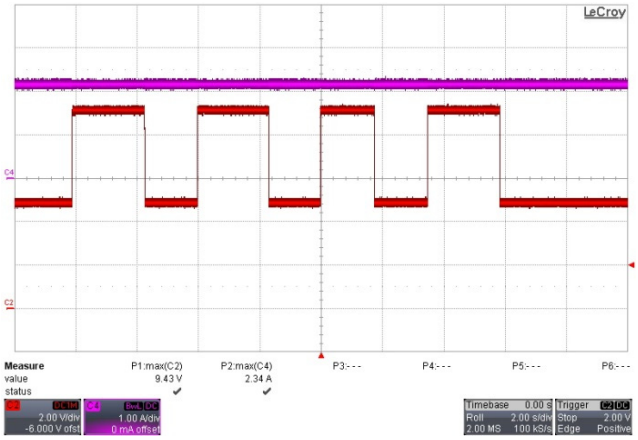

Figure 44 – Output Voltage and Current Waveforms.
265 VAC Input, 2.2 A Load.
Upper: I_{OUT}, 1 A, 2 s / div.
Lower: V_{OUT}, 2 V / div.

12.4 *Output Ripple Measurements*

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

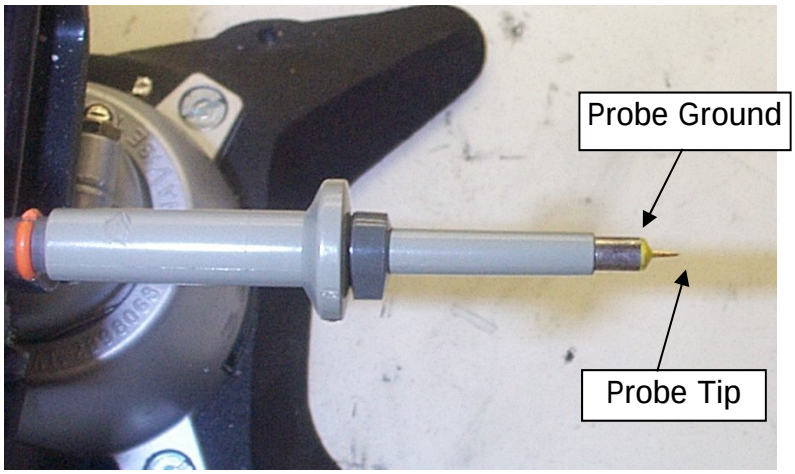

Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

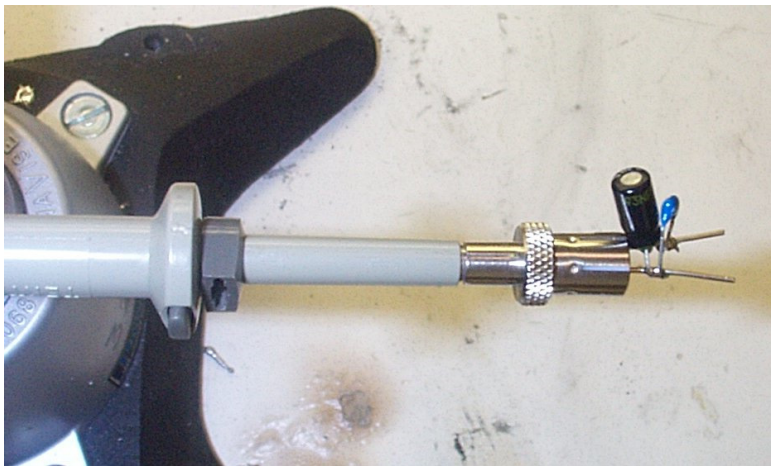

Figure 46 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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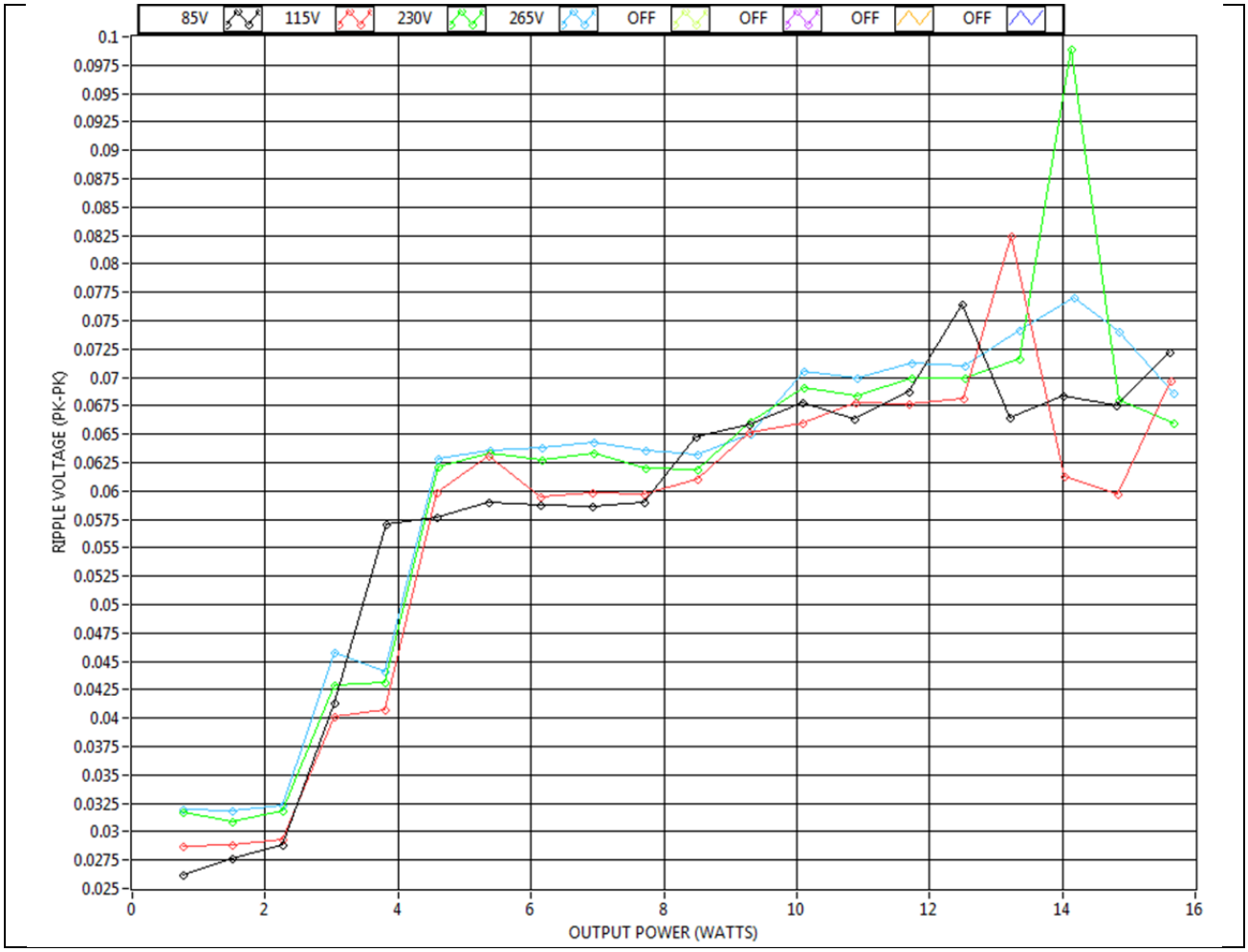
12.4.2 Ripple Amplitude vs. Line

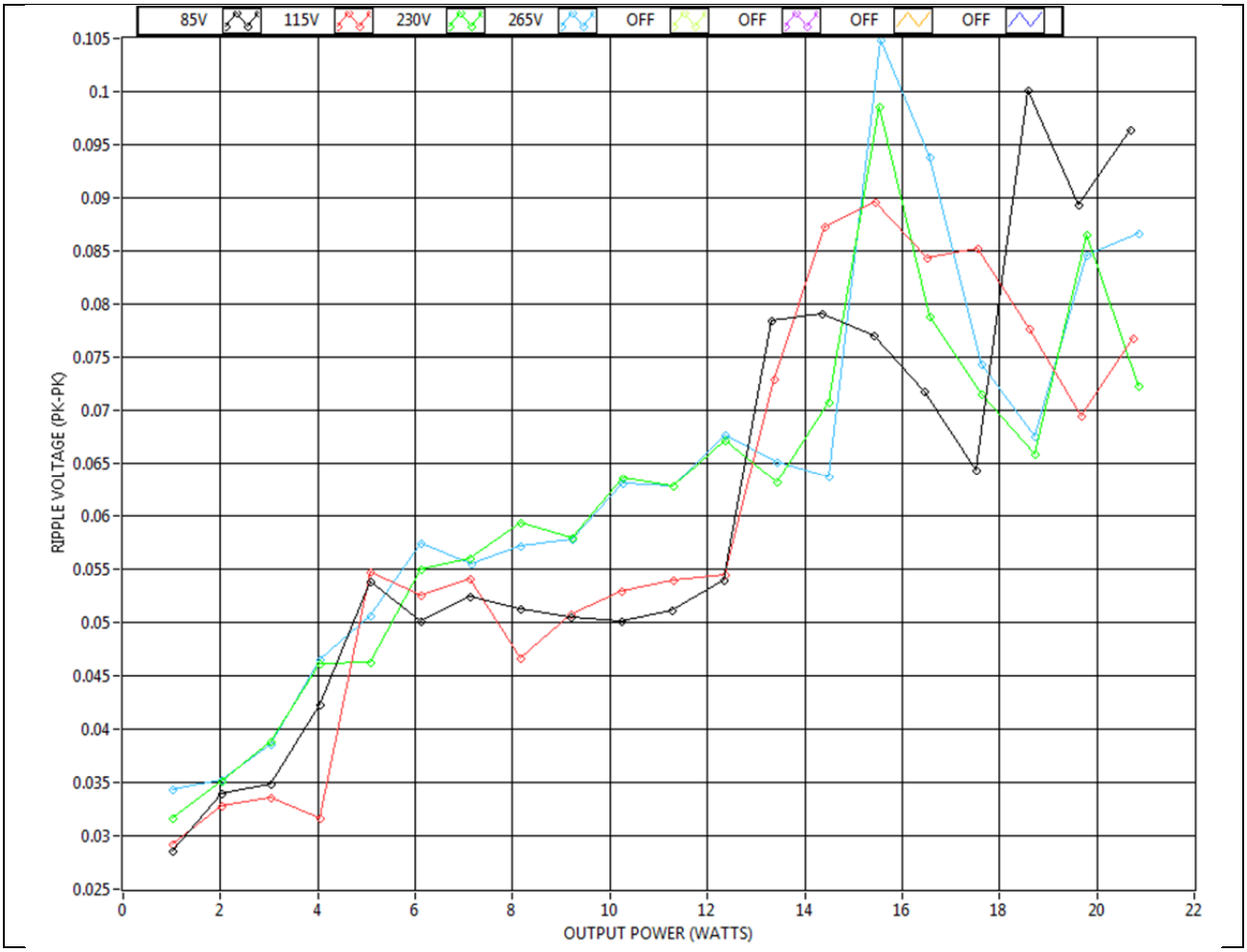
12.4.2.1 5.0 V



Input	85 VAC	115 VAC	230 VAC	265 VAC
Max Ripple (mV)	76.5	82.4	98.9	77

Figure 47 – Ripple Amplitude vs. Output Power 5 V.

12.4.2.2 9.0 V



Input	85 VAC	115 VAC	230 VAC	265 VAC
Max Ripple (mV)	100.1	89.6	98.6	104.9

Figure 48 – Ripple Amplitude vs. Output Power 9.0 V.

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12.4.2.3 5 V

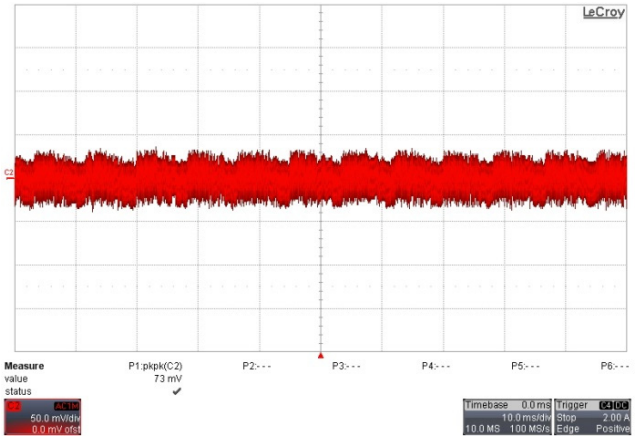


Figure 49 – Output Ripple.
85 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

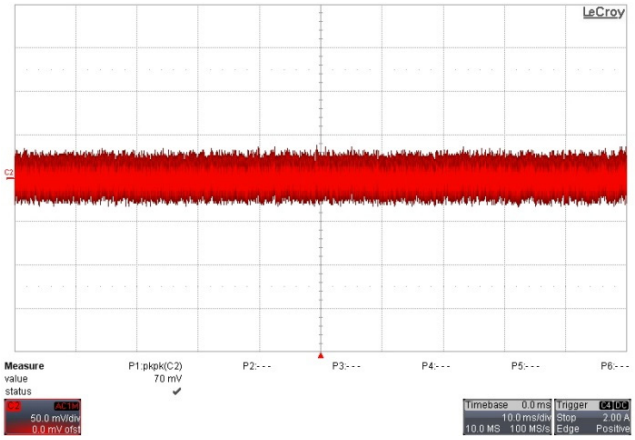


Figure 50 – Output Ripple.
265 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

12.4.2.4 9 V

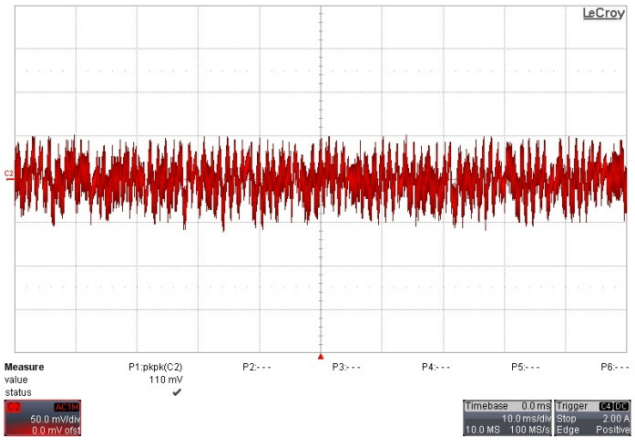


Figure 51 – Output Ripple.
85 VAC Input, 9.0 V, 2.2 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

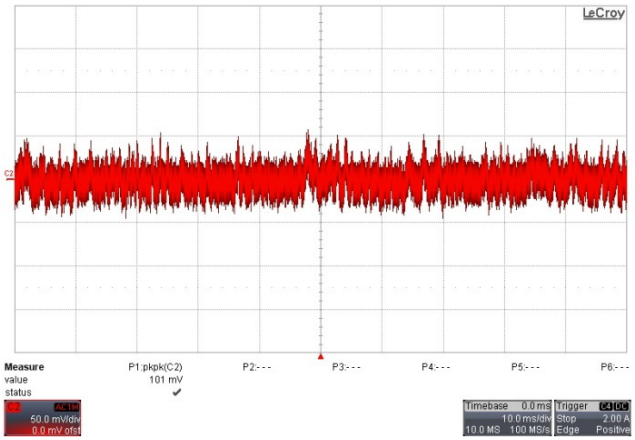
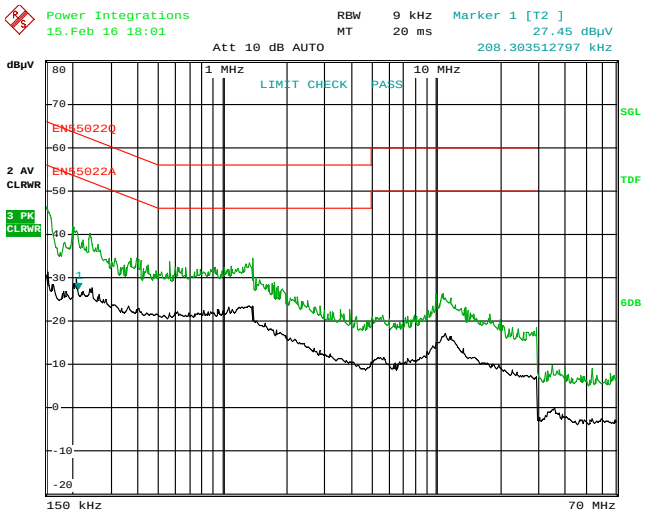


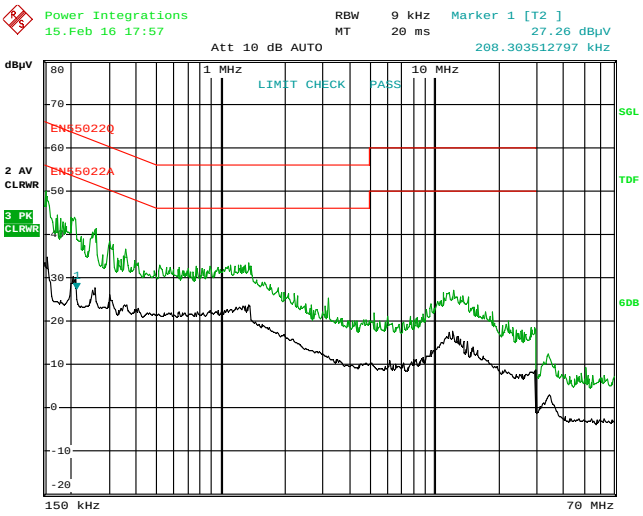
Figure 52 – Output Ripple.
265 VAC Input 9.0 V, 2.2 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

13 Conducted EMI

13.1 Floating Output (PK / AV)

13.1.1 5 V, 3 A





115 VAC Input 230 VAC Input

Figure 53 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].

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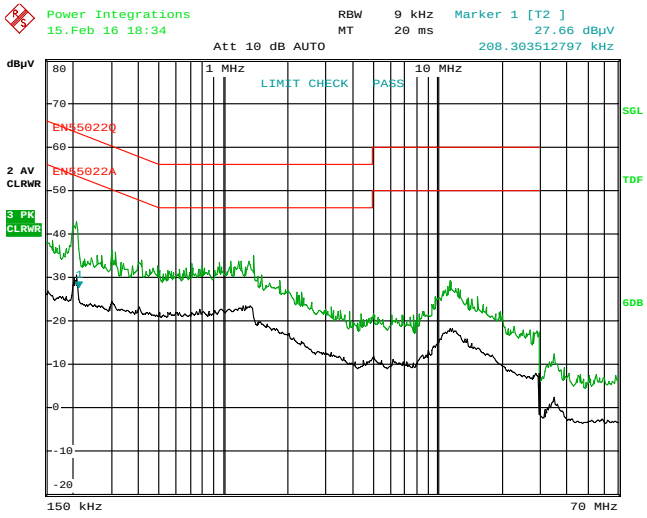
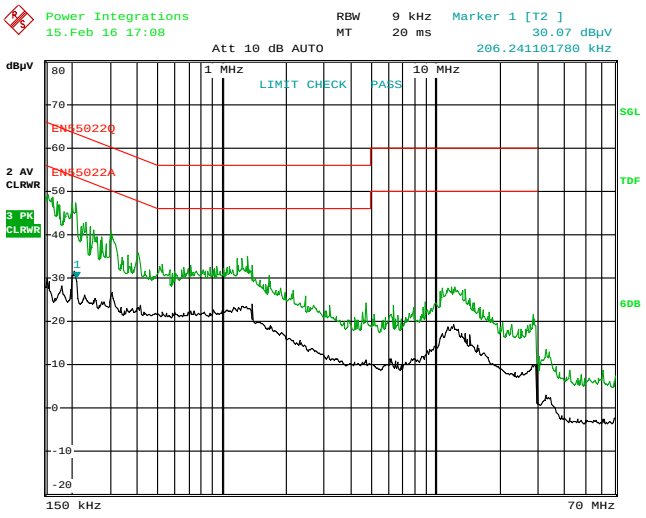
13.1.2 9 V, 2.2 A



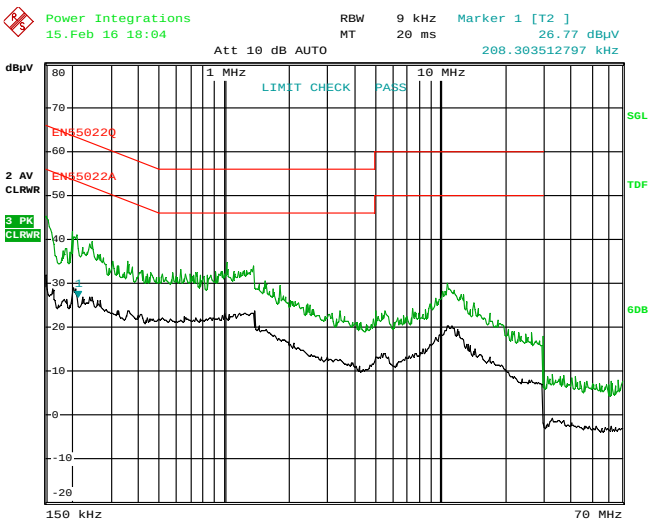


115 VAC Input 230 VAC Input

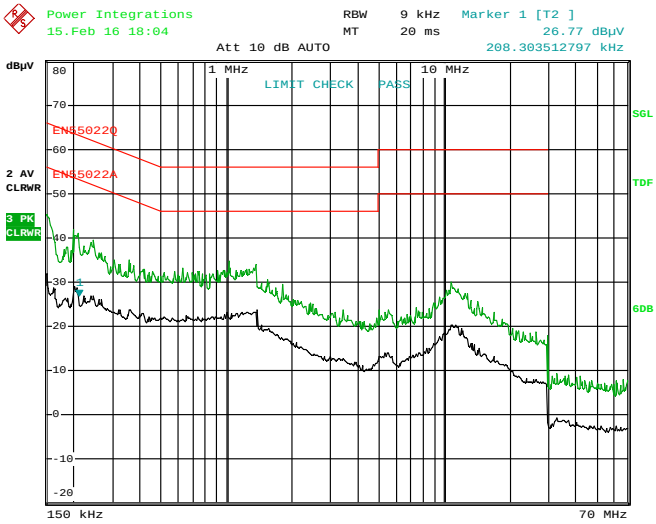
Figure 54 – Floating Ground EMI, 9 V / 2.2 A Load [Line Scan].

13.2 **Artificial Hand Ground (PK / AV)**

13.2.1 5 V, 3 A



115 VAC Input



230 VAC Input

Figure 55 – Artificial Hand Ground EMI, 5 V / 3 A Load [Line Scan].

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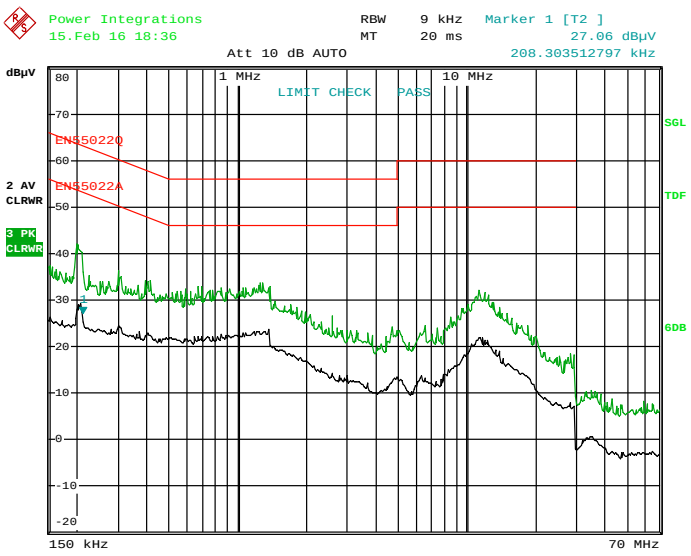
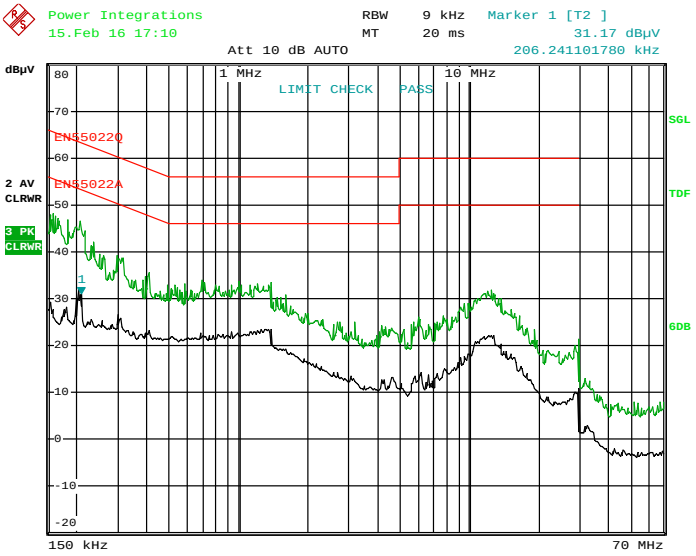
13.2.2 9 V, 2.2 A



DAK85_115_NHAND_NOYCAP_NOFUSE
Date: 15.FEB.2016 18:36:01



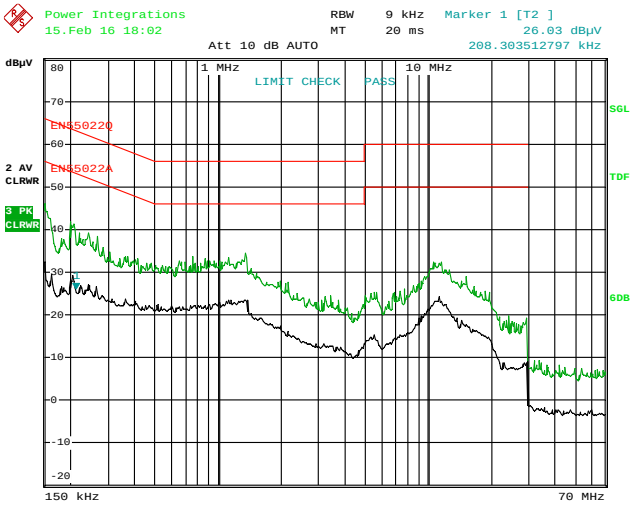
DAK85_115_NHAND_NOYCAP_NOFUSE
Date: 15.FEB.2016 17:10:37

115 VAC Input 230 VAC Input

Figure 56 – Artificial Hand Ground EMI, 9 V / 2.2 A Load [Line Scan].

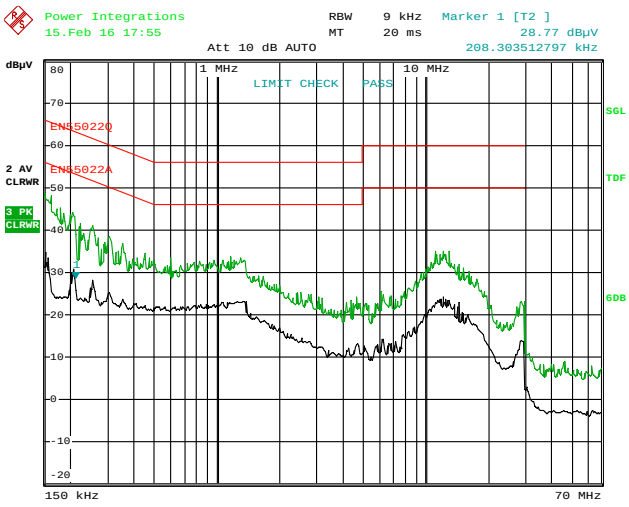
13.3 **Earth Ground (PK / AV)**

13.3.1 5 V, 3 A



DAK85_115_NHAND_NOYCAP_NOFUSE
Date: 15.FEB.2016 18:02:32

115 VAC Input



DAK85_115_NHAND_NOYCAP_NOFUSE
Date: 15.FEB.2016 17:55:56

230 VAC Input

Figure 57 – Earth Ground EMI, 5 V / 3 A Load [Line Scan].

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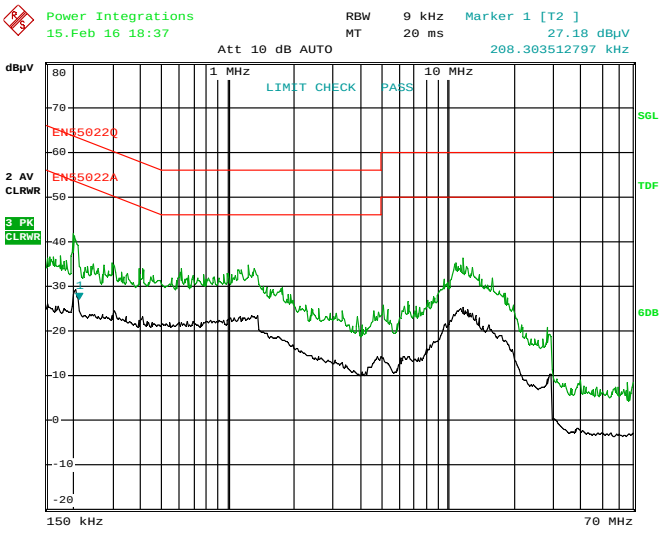
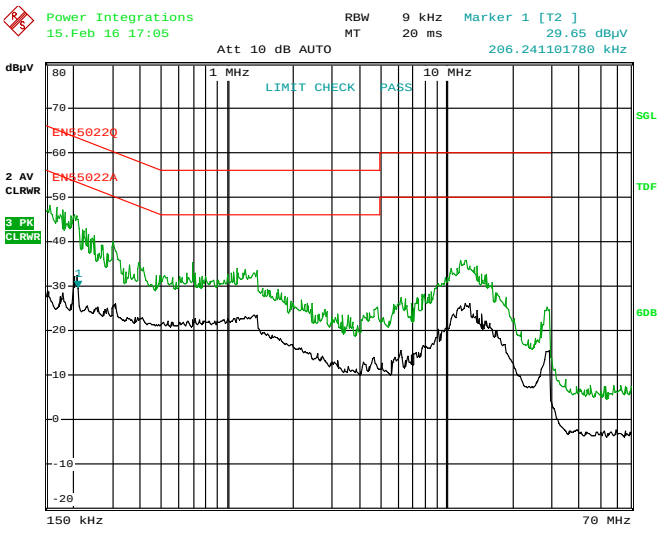
13.3.2 9 V, 2.2 A



115 VAC Input



230 VAC Input

Figure 58 – Earth Ground EMI, 9 V / 2.2 A Load [Line Scan].

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
18-Feb-16	AK	1.0	Initial Release	
19-Feb-16	RJ	1.1	Minor Edits	
23-Feb-16	RJ	1.2	Minor Edits	
28-Jun-16	KM	1.3	Added Magnetics Supplier.	

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