Design Example Report

Title	***High Efficiency 20 W Power Supply Using InnoSwitch™-CH INN2005K***
Specification	85 VAC – 264 VAC Input; 5.1 V, 4 A Output
Application	USB Adapter
Author	Applications Engineering Department
Document Number	DER-451
Date	May 22, 2015
Revision	1.4

Summary and Features

- InnoSwitch-CH - industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built in synchronous rectification for high efficiency
- >90% average efficiency
- >83% efficiency at 10% load
- Meet DOE6 and CoC V5 2016
- All the benefits of secondary side control with the simplicity of primary side regulation
  - 3% output voltage regulation over line and load variation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
  - Smaller, lower cost output capacitors
  - <15 mW no-load input power
- Primary sensed output over voltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown.

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 4 A, 5.1 V adapter utilizing a device from the InnoSwitch-CH family of ICs. This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

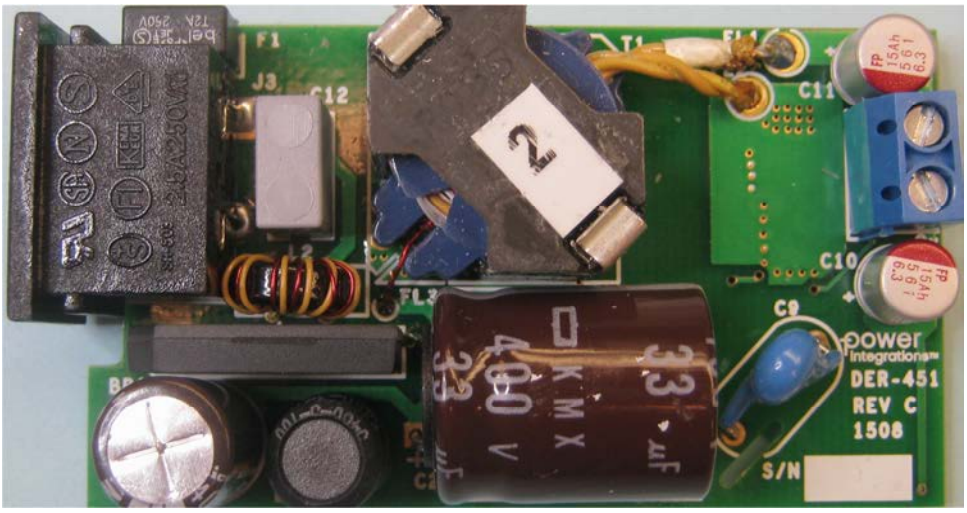

Figure 1 – Populated Circuit Board Photograph, Top.

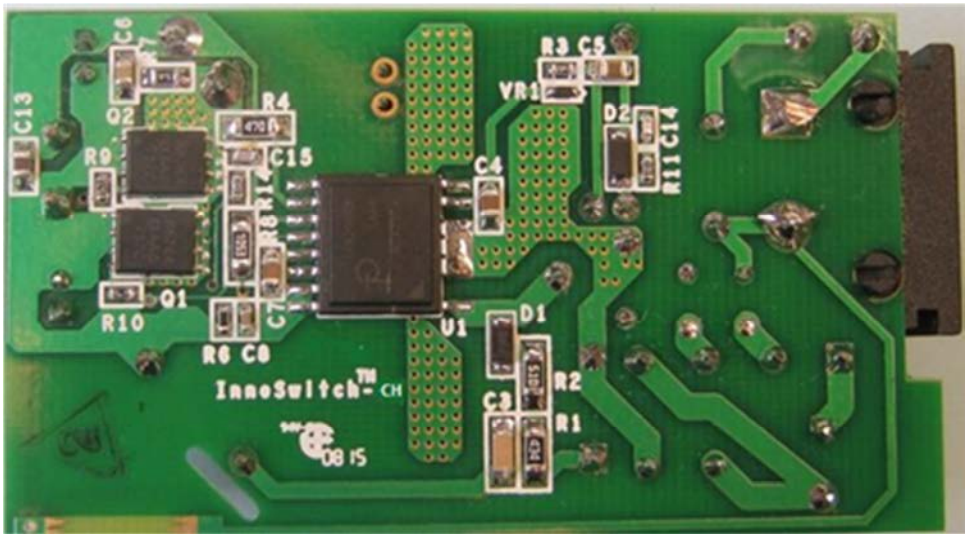

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		264	VAC	2 Wire – No P.E.
Frequency	f_{LINE}	50	50/60	64	Hz	
No-load Input Power				15	mW	230 VAC
Output						
Output Voltage	V_{OUT}	4.95	5.1	5.25	V	
Output Current				4	A	
Transient Output Voltage	$V_{OUT(T)}$	4.5		5.5	V	0 A - 4 A - 0 A Load Step at the End of #22 AWG, 1 m Cable, 11 mΩ
Output Ripple Voltage	V_{RIPPLE}			150	mV	At the End of 1 m #22 AWG Cable
Turn on Rise Time	t_R			20	ms	
Rated Output Power	P_{OUT}	20			W	
Efficiency at 115 VAC / 230 VAC						
Full load		89.5	90	90.5	%	Measured at Output Terminal
Average Efficiency 25%, 50%, 75%, and 100% Load	η	89			%	Measured at Output Terminal
10% Load	$\eta_{10\%}$	83			%	Measured at Output Terminal
Environmental						
Conducted EMI		CISPR22B / EN55022B Floating or Grounded Load				Resistive Load, 6 dB Margin
Safety		IEC950 / UL1950 Class II				Designed to Meet
Audible Noise				25	dB	Measured at 3 cm Distance
Line Surge						
Common Mode (L1/L2-PE)				6	kV	Ring Wave, Common Mode: 12 Ω
Differential Mode				1	kV	1.2 μs / 50 μs Surge Mode, 2 Ω
ESD						
Contact		±8			kV	No Degradation in Performance
Air Discharge		±15			kV	No Degradation in Performance
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure

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3 **Schematic**

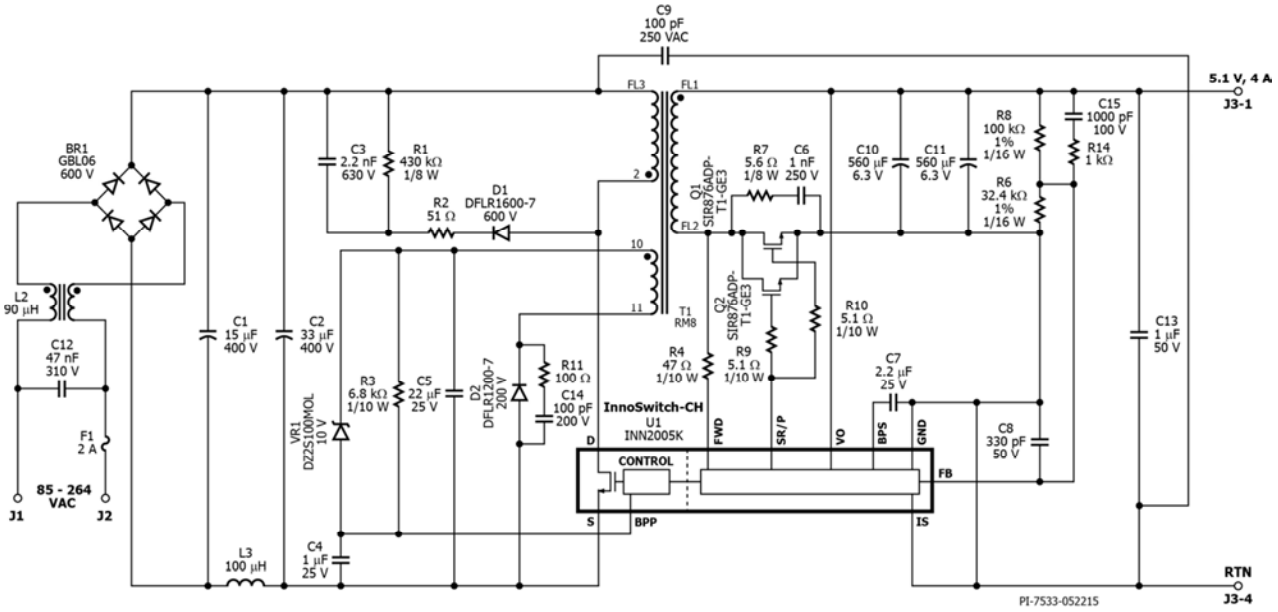

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and the common mode choke L2 with capacitors, C9 and C12, provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1, L3, and C2. The inductor L3 and capacitors C1 and C2 form a pi-filter. This filter, with capacitor C12 provides differential noise filtering.

4.2 *InnoSwitch-CH IC Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 650 V power MOSFET inside the InnoSwitch-CH IC (U1).

A low cost RCD clamp formed by D1, R1, R2, and C3 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C5, and fed in the BPP pin via a current limiting resistor R3. Radiated EMI caused by resonant ringing across diode D2 is reduced via snubber components R11 and C14. The primary side overvoltage protection is obtained using Zener diode VR1. In the event of overvoltage at output, the increased voltage at the output of the bias winding causes Zener diode VR1 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch-CH IC.

4.3 *InnoSwitch-CH IC Secondary*

The secondary side of the InnoSwitch-CH provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by synchronous FETs (SR FETS), Q1 and Q2, and filtered by capacitors C10, C11, and C13. High frequency ringing during switching transients that would otherwise create high-voltage across SR FETs and radiated EMI is reduced via snubber components R7 and C6.

The gate of Q1 and Q2 is turned on based on the winding voltage sensed via R4 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

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The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C7 via R4 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

The output voltage is sensed via resistor divider R8 and R6. The output voltage is sampled through the divider network comprising of resistors R8 and R6 and the divided voltage is equal to the internal reference. The InnoSwitch-CH IC has an internal reference of 1.265 V. Feedback compensation network comprising capacitor C15 and resistor R14, reduces the output ripple voltage capacitor C8 provides decoupling from high frequency noise affecting power supply operation.

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

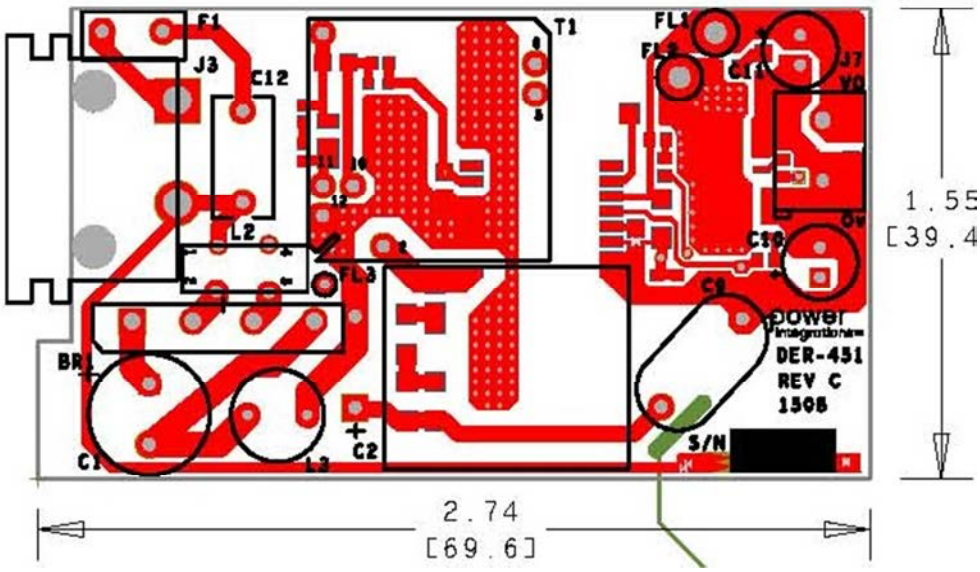

Figure 4 – Printed Circuit Layout, Top.

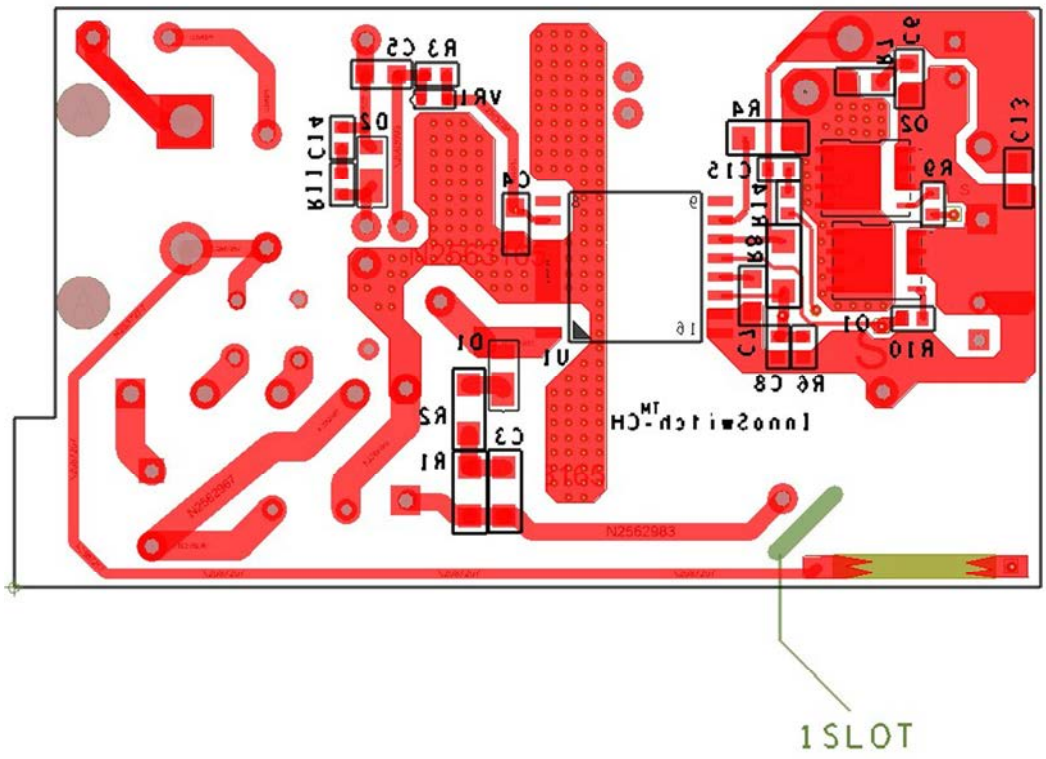

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Diode Bridge 600 V 4 A GB	GBL06	Genesic Semi
2	1	C1	15 µF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
3	1	C2	33 µF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	EKMX401ELL330ML20S	Nippon Chemi-Con
4	1	C3	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
5	1	C4	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
6	1	C5	22 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E226M125AC	TDK
7	1	C6	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
8	1	C7	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
9	1	C8	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C9	100 pF, 250 VAC, Film, X1Y1	CD70-B2GA101KYNS	TDK
11	2	C10 C11	560 µF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
12	1	C12	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
13	1	C13	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
14	1	C14	100 pF 200 V, Ceramic, NPO, 0603	C0603C101J2GAC7867	Kemet
15	1	C15	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
16	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
17	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
18	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
19	1	J3	AC Input Receptacle	S-01-02A	Sunfair
20	1	J7	CONN TERM BLOCK, 2 POS, 5 mm, PCB	ED500/2DS	On Shore Technology
21	1	L2	Custom, 90 µH, constructed on Core 35T0375-10H from PI# 30-00275-00		Power Integrations
22	1	L3	100 µH, 1.0 A, 20%	RL-5480-3-100	Renco
23	2	Q1 Q2	100 V, 40 A, N-Channel, PowerPAK SO-8	SIR876ADP-T1-GE3	Vishay
24	1	R1	430 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ434V	Panasonic
25	1	R2	51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
26	1	R3	6.8 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ682V	Panasonic
27	1	R4	47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
28	1	R6	32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
29	1	R7	5.6 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R6V	Panasonic
30	1	R8	100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
31	2	R9 R10	5.1 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ5R1V	Panasonic
32	1	R11	100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
33	1	R14	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
34	1	T1	Bobbin, RM8, Vertical, 12 pins	RM8/12/1	Schwartzpunkt
35	1	U1	InnoSwitch-CH, Off-Line CV/CC Flyback Switcher, ReSOP-16B	INN2005K	Power Integrations
36	1	VR1	10 V, 5%, 150 mW, SSMINI-2	DZ2S100M0L	Panasonic-SSG

7 Transformer Specification

7.1 *Electrical Diagram*

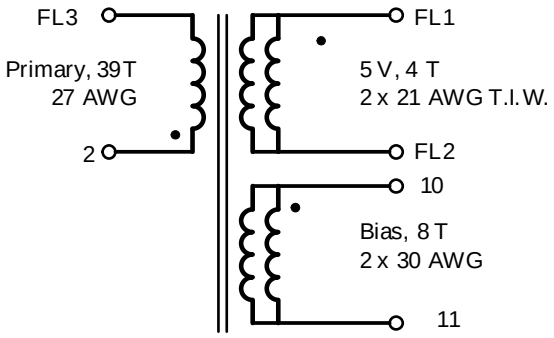

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Primary Inductance	Pin 2 - FL3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	597 µH ±5%
Resonant Frequency	Pin2 - FL3, all other windings open.	1100 kHz (Min.)
Primary Leakage Inductance	Pin2 - FL3, with FL1 and FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	15 µH (Max.)

7.3 *Materials*

Item	Description
[1]	Core: TDK PC95 RM08-Z or equivalent PI # 99-00022-00, gapped for ALG of 392 nH/t^2.
[2]	Bobbin: RM8-12pins(6/6), Ferroxcube-CSV-RM8-1S-12P-G, PI#: 25-01022-00; or equivalent.
[3]	Clip: RM8, Allstar Magnetic, CLI/P-RM8/I.
[4]	Magnet Wire: #27 AWG, solderable double coated.
[5]	Magnet Wire: #30 AWG, solderable double coated.
[6]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[7]	Tape: Polyester Film, 3M 1350-1, 9.0 mm wide.
[8]	Tape: Polyester Film, 3M 1350-1, 20 mm x 12.0 mm, with corner cuts.
[9]	Varnish.

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7.4 *Transformer Build Diagram*

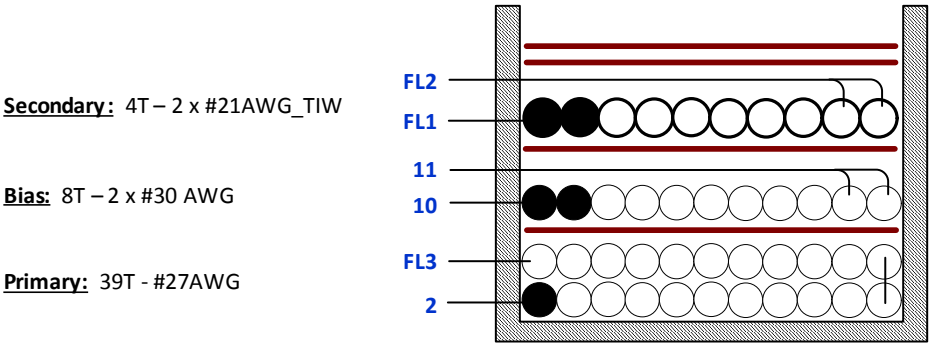
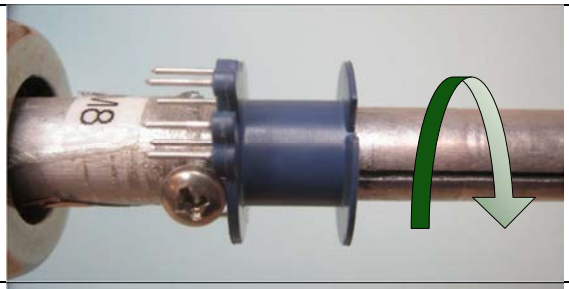
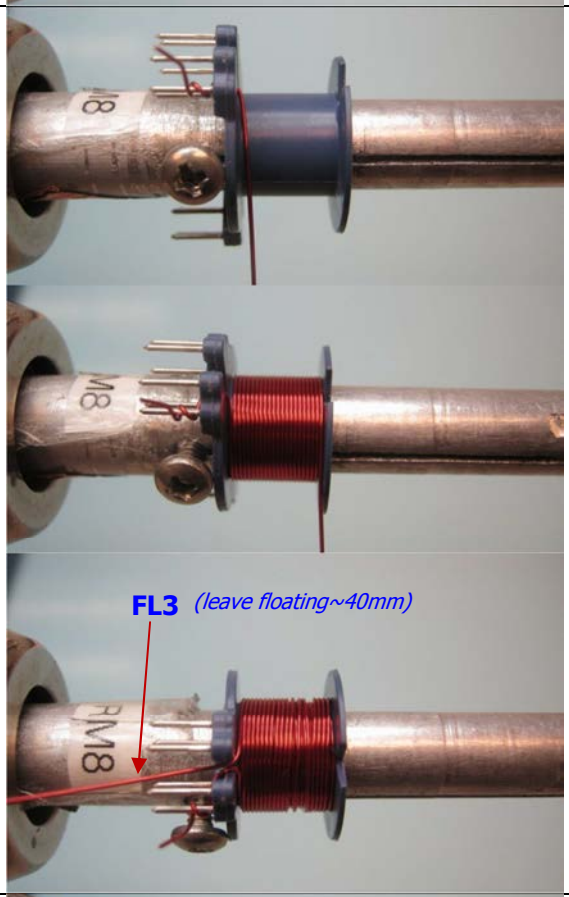


Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
Primary Winding	Start at pin 2. Wind 39 turns of item [4] in approximately 2 layers. Finish as marked FL3.
Insulation	Use 1 layer of item [7] for insulation.
Bias winding	Starting at pin10, wind 8 bifilar turns of item [5]. Spread turns evenly across bobbin. Finish at pin 11.
Insulation	Use 1 layer of item [7] for insulation.
Secondary winding	Take two parallel strands of item [6]. Mark start end as FL1, wind 4 turns of item [6], and finish as FL2.
Insulation	Use 2 layers of item [7] to secure the windings.
Final Assembly	Insert cores, gapped for inductance specified. Secure core halves using clips item [3]. Cut short pins: 1, 3, 4, 7, 8, and 9. Dip varnish item [8].

7.6 *Transformer Illustrations*

Bobbin Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
Primary Winding		Start at pin 2. Wind 39 turns of item [4] in approximately 2 layers. Finish as marked FL3.
Insulation		Use 1 layer of item [7] for insulation.

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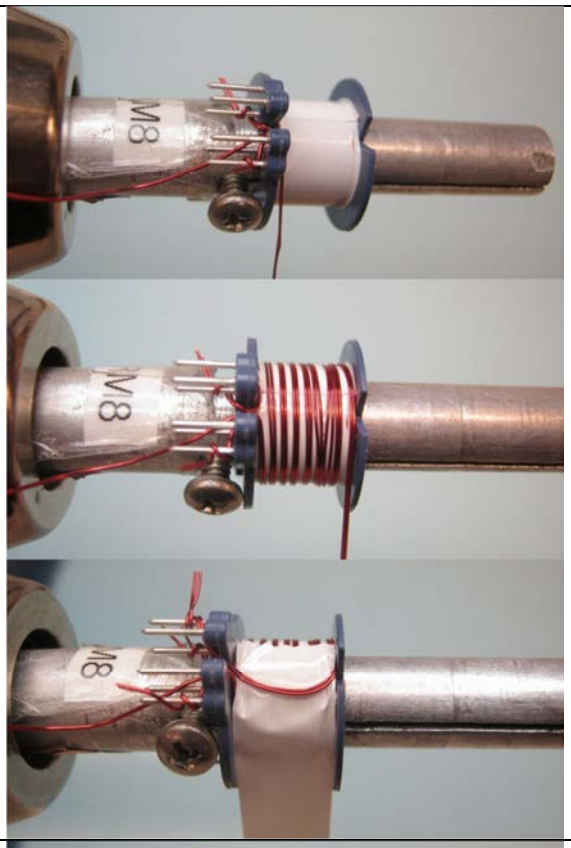
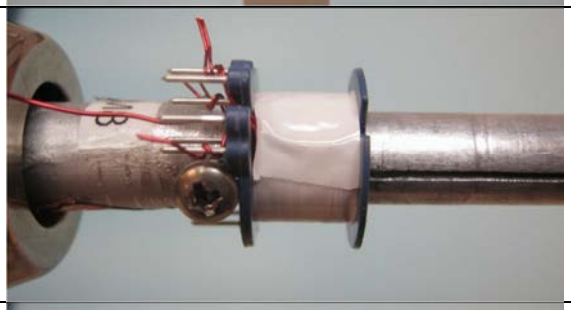
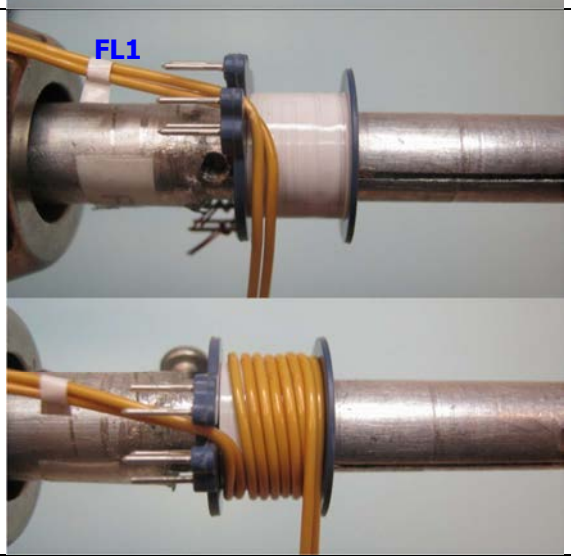
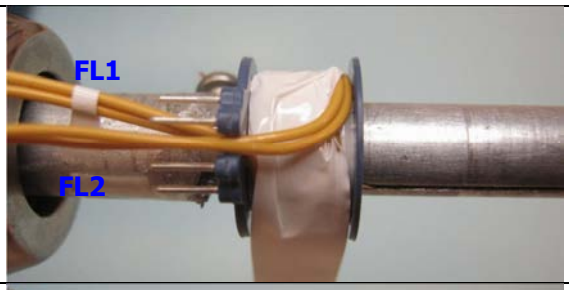
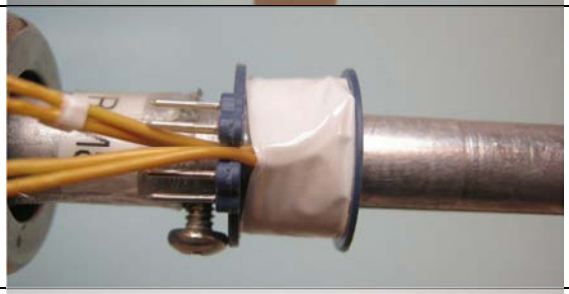
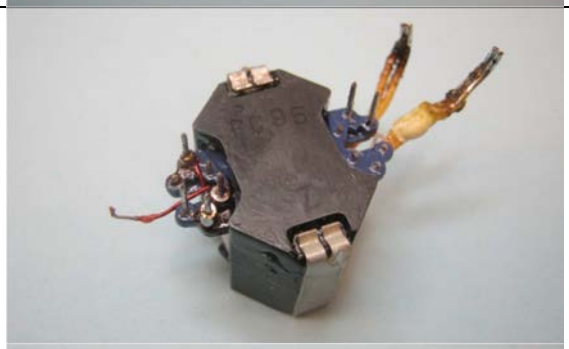
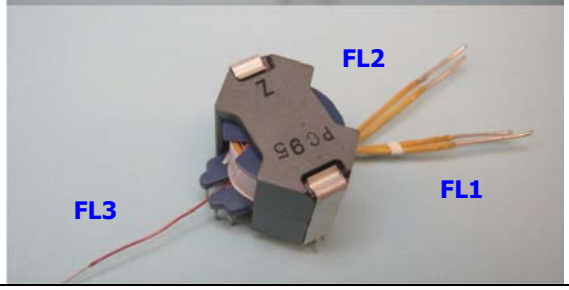
Bias Winding		Starting at pin10, wind 8 bifilar turns of item [5]. Spread turns evenly across bobbin. Finish at pin 11.
Insulation		Use 1 layer of item [7] for insulation.
Secondary Winding		Take two parallel strands of item [6]. Mark start end as FL1, wind 4 turns of item [6], and finish as FL2.

		
Insulation		Use 2 layers of item [7] to secure the windings.
Final Assembly	  	Insert cores, gapped for inductance specified. Secure core halves using clips item [3]. Cut short pins: 1,3 , 4, 7 ,8 , and 9. Place 2 layers of tape item [8]. Dip varnish item [9].

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8 Transformer Design Spreadsheet

ACDC_InnoSwitch-CH_102014; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch-CH_101714_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	5.10		5.10	V	Output Voltage (continuous power at the end of the cable)
IO	4.00		4.00	A	Power Supply Output Current (corresponding to peak power)
Power		**Info**	20.4	W	Specified Output Power exceeds the value specified on the datasheet for universal input adapter. Please verify performance on bench
n	0.90		0.90		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	48.00		48.00	uFarad	Input Capacitance
ENTER InnoSwitch-CH VARIABLES					
InnoSwitch-CH	**Auto**		**INN20x5**		Recommended InnoSwitch-CH
Cable drop compensation	**0%**		**0%**		Select Cable Drop Compensation option
Complete Part Number			**INN2005K**		Final part number including package
Chose Configuration	**INC**		**Increased Current Limit**		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.955	A	Minimum Current Limit
ILIMITTYP			1.050	A	Typical Current Limit
ILIMITMAX			1.145	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			92.61	A^2kHz	Worst case I2F parameter across the temperature range
VOR	51		51	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.58		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.27		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			7.70	V	Bias Winding Number of Turns
PIVB			115.53	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM8**		**RM8**		Enter Transformer Core
Core			PC47RM8Z-12		Enter core part number, if necessary
Bobbin			BRM8-718CPFR		Enter bobbin part number, if necessary
AE			0.640	cm^2	Core Effective Cross Sectional Area
LE			3.80	cm	Core Effective Path Length
AL			1950	nH/T^2	Ungapped Core Effective Inductance
BW			9.05	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to

					Secondary Creepage Distance)
L	2		2		Number of Primary Layers
NS	4		4		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			89	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.38		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.26	A	Average Primary Current
IP			0.955	A	Peak Primary Current assuming ILIMITMIN
IR			0.550	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.43	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			597	uHenry	Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 566 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			39		Primary Winding Number of Turns
ALG			392	nH/T^2	Gapped Core Effective Inductance
BM		**Warning**	3057	Gauss	!!! Warning. Maximum flux density too high, may cause transformer saturation. REDUCE BP<3000. Increase NS , use larger Core or increase VOR
BAC			880	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			921		Relative Permeability of Ungapped Core
LG			0.16	mm	Gap Length (Lg > 0.1 mm)
BWE			18.1	mm	Effective Bobbin Width
OD			0.46	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.40	mm	Bare conductor diameter
AWG			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			203	Cmils	Bare conductor effective area in circular mils
CMA			473	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			9.31	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			5.36	A	Secondary RMS Current
IRIPPLE			3.58	A	Output Capacitor RMS Ripple Current
CMS			1073	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			502	V	Maximum Drain Voltage Estimate
PIVS			59	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.10	V	Main Output Voltage directly after output rectifier
IO1			4.00	A	Output DC Current
PO1			20.40	W	Output Power
VD1			0.10	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			4.00	Turns	Output Winding Number of Turns
ISRMS1			5.36	A	Output Winding RMS Current

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IRIPPLE1			3.58	A	Output Capacitor RMS Ripple Current
PIVS1			59	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			**Si7456**		Recommended SR FET for this output
RDSON_HOT			0.042	Ohm	RDSon at 100C
VRATED			100	V	Rated voltage of selected SR FET
CMS1			1073	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			19	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.91	mm	Minimum Bare Conductor Diameter
ODS1			2.26	mm	Maximum Outside Diameter for Triple Insulated Wire

Note: Warning: The spreadsheet shows a warning .The warning is due to flux density increasing beyond 3000 Gauss (the ferrite core material selected for this project is PC40 which has a saturation flux density spec of 3900 Gauss at 100 °C).

9 Performance Data

9.1 *Full Load Efficiency (at Output Terminal) vs. Line*

9.1.1 Efficiency with Two FETs (Q1 & Q2) in Parallel for Synchronous Rectification

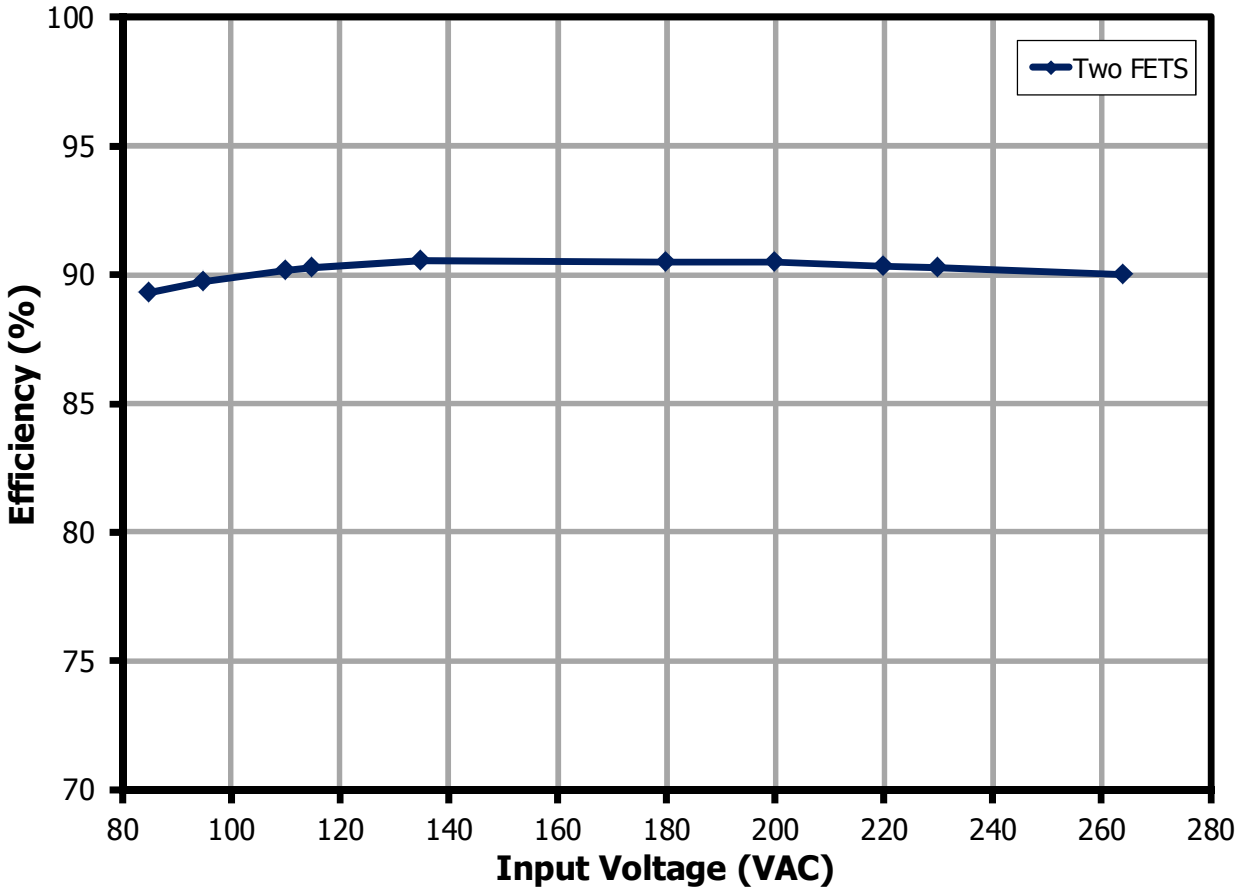

Figure 8 – Efficiency vs. Line Voltage, Room Temperature.

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9.1.2 Efficiency with one FET (Q1 Only) for Synchronous Rectification

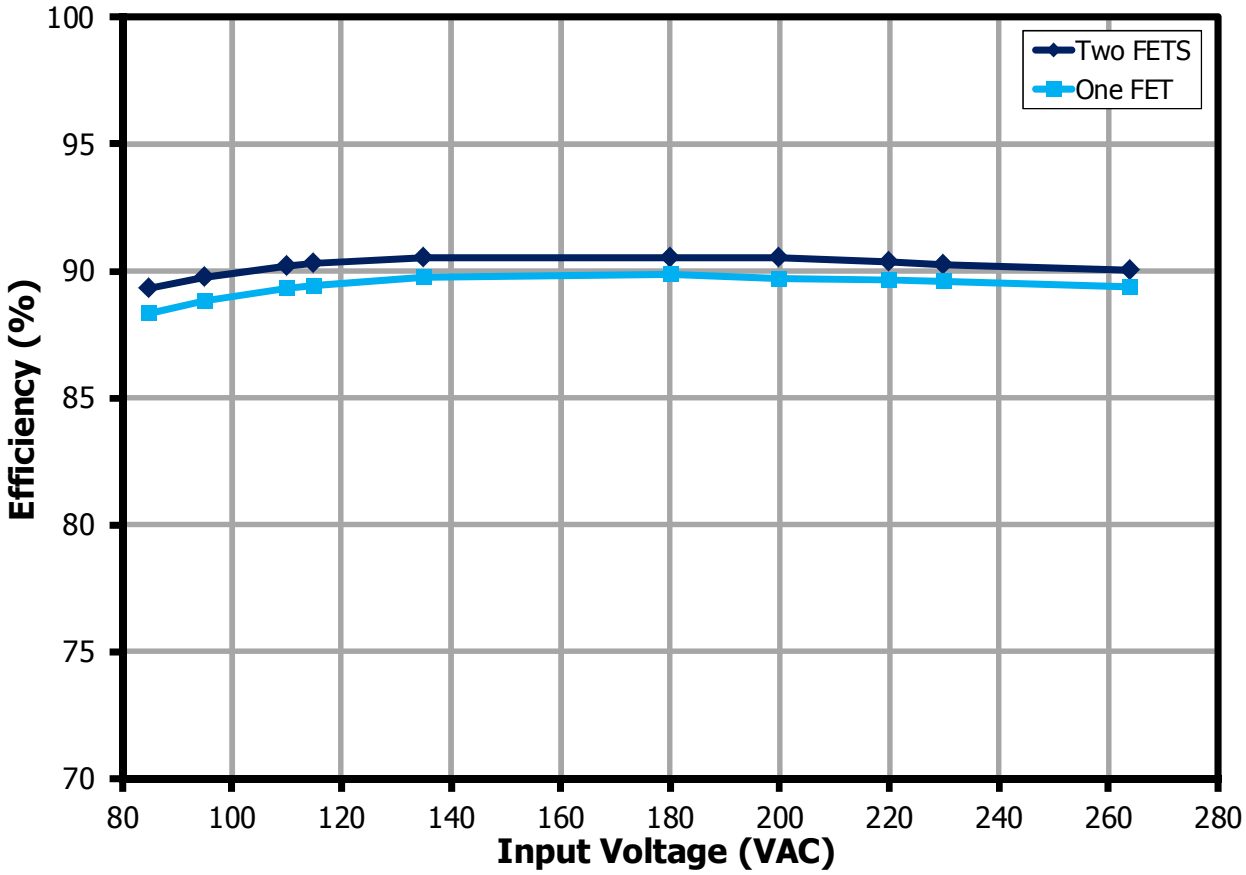

Figure 9 – Efficiency vs. Line Voltage, Room Temperature.

9.2 *Efficiency vs. Load (at Output Terminal)*

9.2.1 Efficiency with Two FETs (Q1 & Q2) in Parallel for Synchronous Rectification

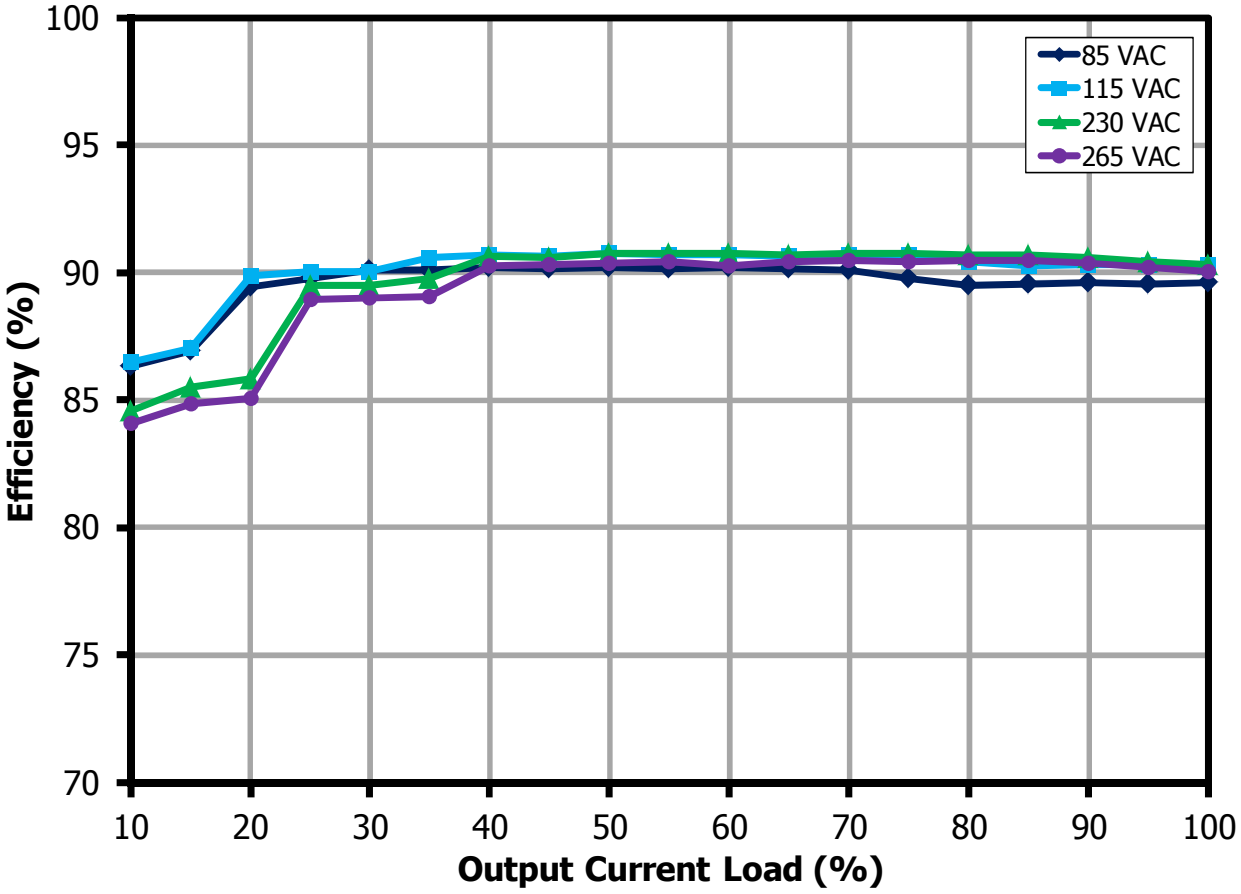

Figure 10 – Efficiency vs. Load, Room Ambient.

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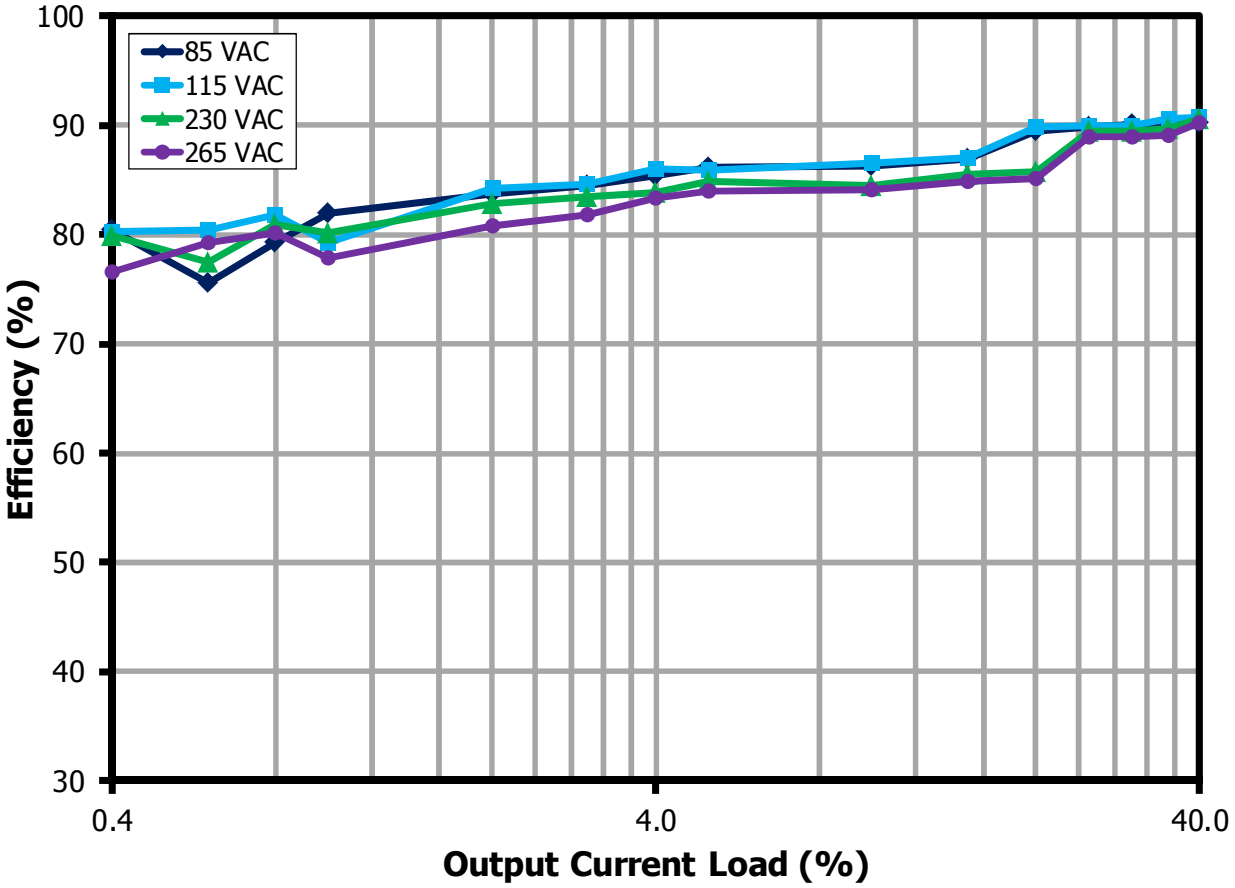

Figure 11 – Efficiency vs. Load (Log Scale to Demonstrate Light Load Performance).

9.2.2 Efficiency with One FET (Q1 Only) for Synchronous Rectification

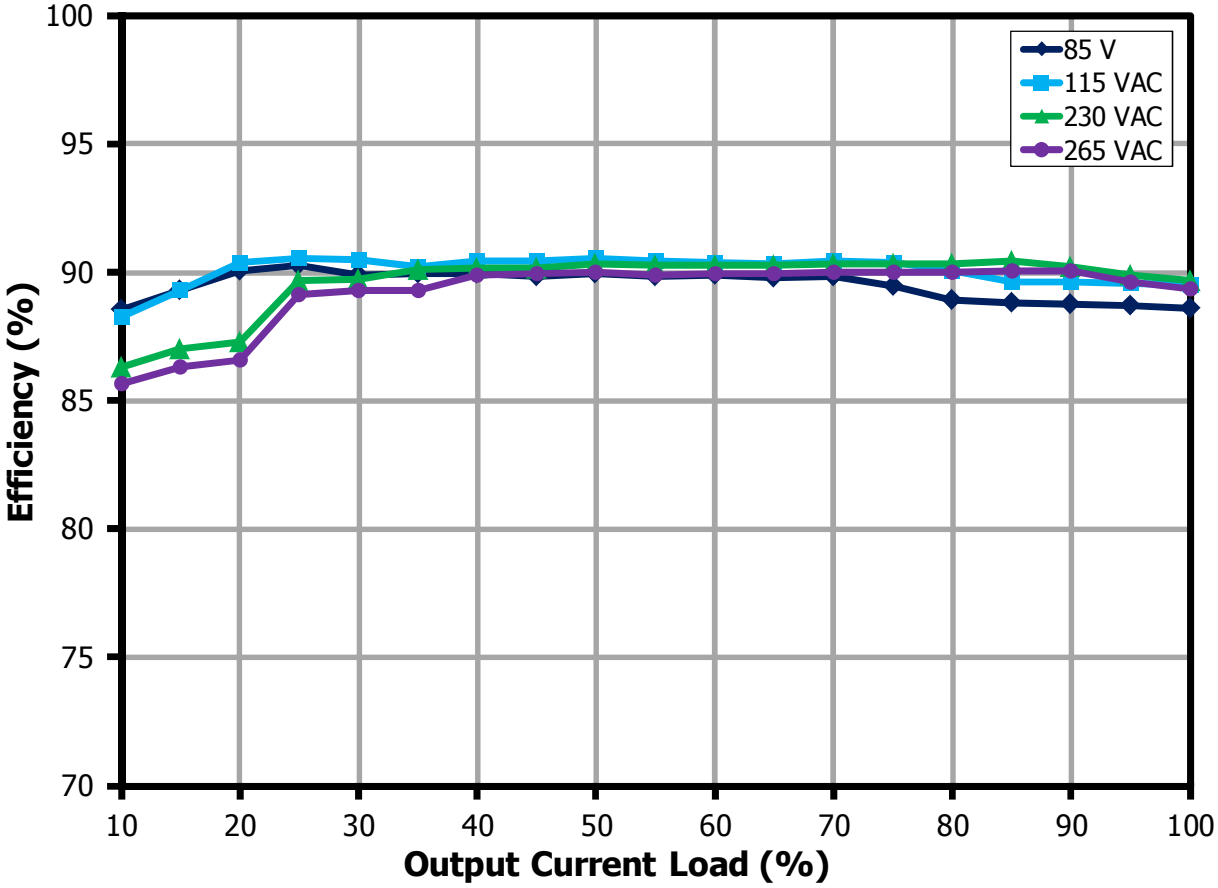

Figure 12 – Efficiency vs. Load, Room Temperature, 60 Hz.

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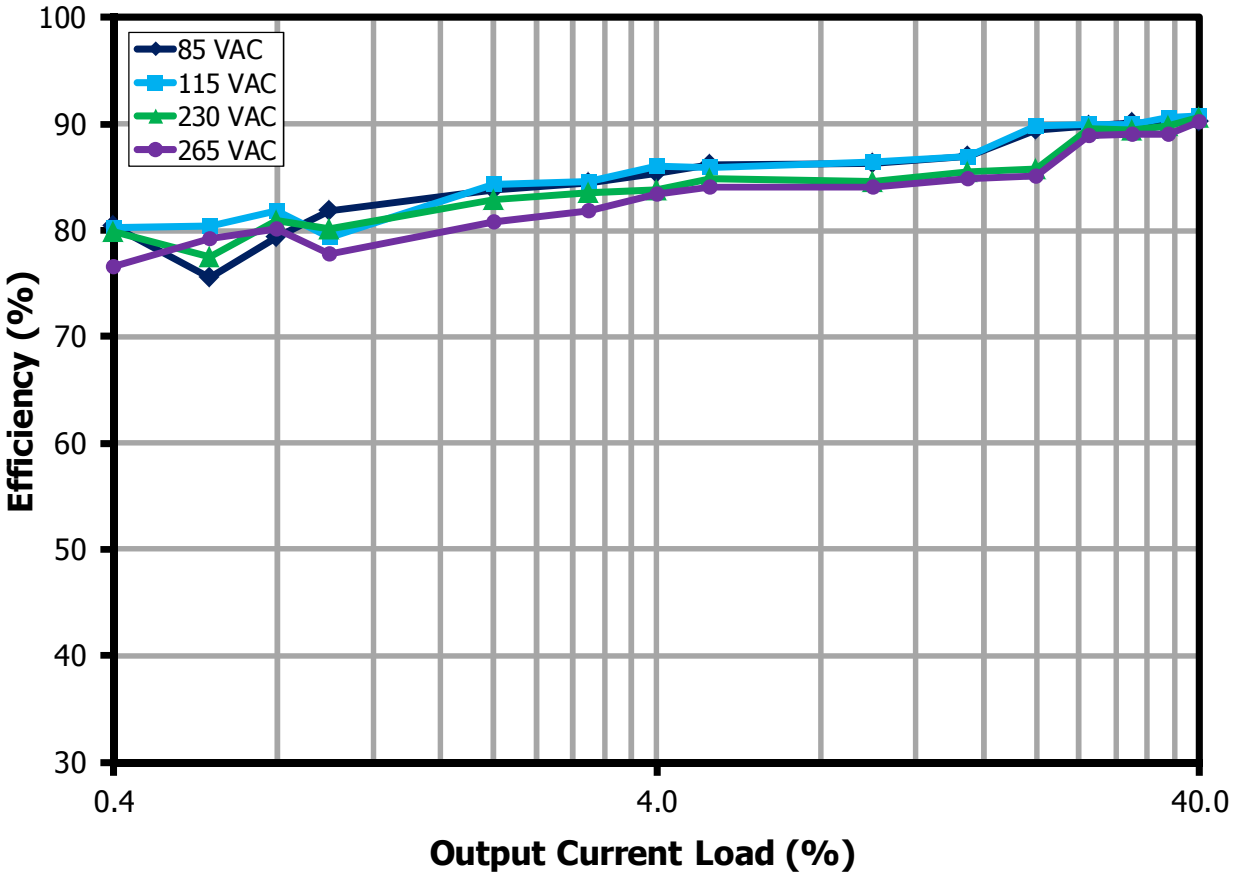

Figure 13 – Efficiency vs. Load (Log Scale to Demonstrate Light Load Performance).

9.3 *No-Load Input Power*

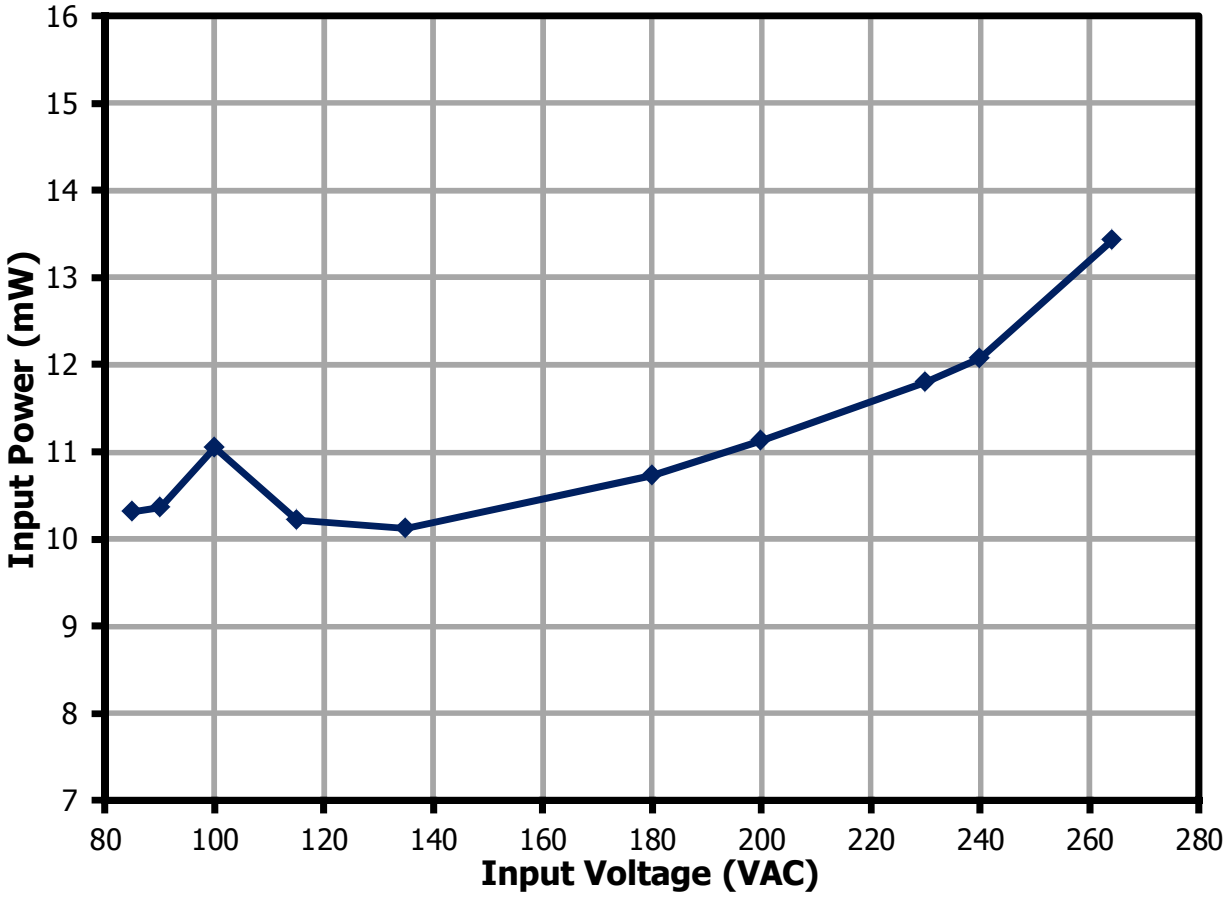

Figure 14 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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9.4 *Average Efficiency (at Output Terminals)*

9.4.1 Efficiency Requirements

Test	Average	Average	Average	Average	10% Load	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
Effective	Now	2016	Now	2016	Now	2016
Regulation	**Energy Star 2**	**New IESA2007**	**CoC v5 Tier 1**	**CoC v5 Tier 2**	**CoC v5 Tier 1**	**CoC v5 Tier 2**
Required Efficiency	**79.4%**	**83.1%**	**81.2%**	**83.7%**	**71.6%**	**74.2%**

9.5 *Average Efficiency at 115 VAC Input*

9.5.1 Efficiency with Two FETs (Q1 & Q2) in Parallel for Synchronous Rectification

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	114.99	0.40	22.64	5.12	3.99	20.44	90.30
75	114.99	0.32	17.16	5.18	3.00	15.56	90.69
50	115.00	0.24	11.46	5.21	2.00	10.40	90.76
25	115.00	0.14	5.72	5.19	0.99	5.15	90.02
10	115.01	0.06	2.33	5.18	0.39	2.02	86.49
					Average Efficiency		90.44

9.5.2 Efficiency with One FET (Q1 Only) for Synchronous Rectification

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	114.99	0.41	22.87	5.13	3.99	20.47	89.52
75	115.00	0.33	17.24	5.19	3.00	15.58	90.38
50	115.00	0.24	11.50	5.21	2.00	10.41	90.52
25	115.00	0.14	5.69	5.20	0.99	5.15	90.53
10	115.01	0.06	2.29	5.19	0.39	2.02	88.29
					Average Efficiency		90.24

9.6 ***Average Efficiency at 230 VAC Input***

9.6.1 Efficiency with Two FETs (Q1 & Q2) in Parallel for Synchronous Rectification

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	230.05	0.27	22.80	5.16	3.99	20.59	90.30
75	230.05	0.22	17.18	5.19	3.00	15.59	90.76
50	230.05	0.16	11.49	5.22	2.00	10.42	90.72
25	230.06	0.09	5.77	5.21	0.99	5.16	89.51
10	230.06	0.04	2.38	5.19	0.39	2.01	84.55
					Average Efficiency		90.32

9.6.2 Efficiency with One FET (Q1 Only) for Synchronous Rectification

Load (%)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	230.05	0.27	22.99	5.16	3.99	20.61	89.66
75	230.05	0.22	17.28	5.20	3.00	15.61	90.33
50	230.05	0.16	11.54	5.22	2.00	10.42	90.34
25	230.05	0.09	5.76	5.21	0.99	5.17	89.69
10	230.06	0.04	2.34	5.19	0.39	2.02	86.33
					Average Efficiency		90.00

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9.7 *Line and Load Regulation (at Output Terminal)*

9.7.1 Line Regulation

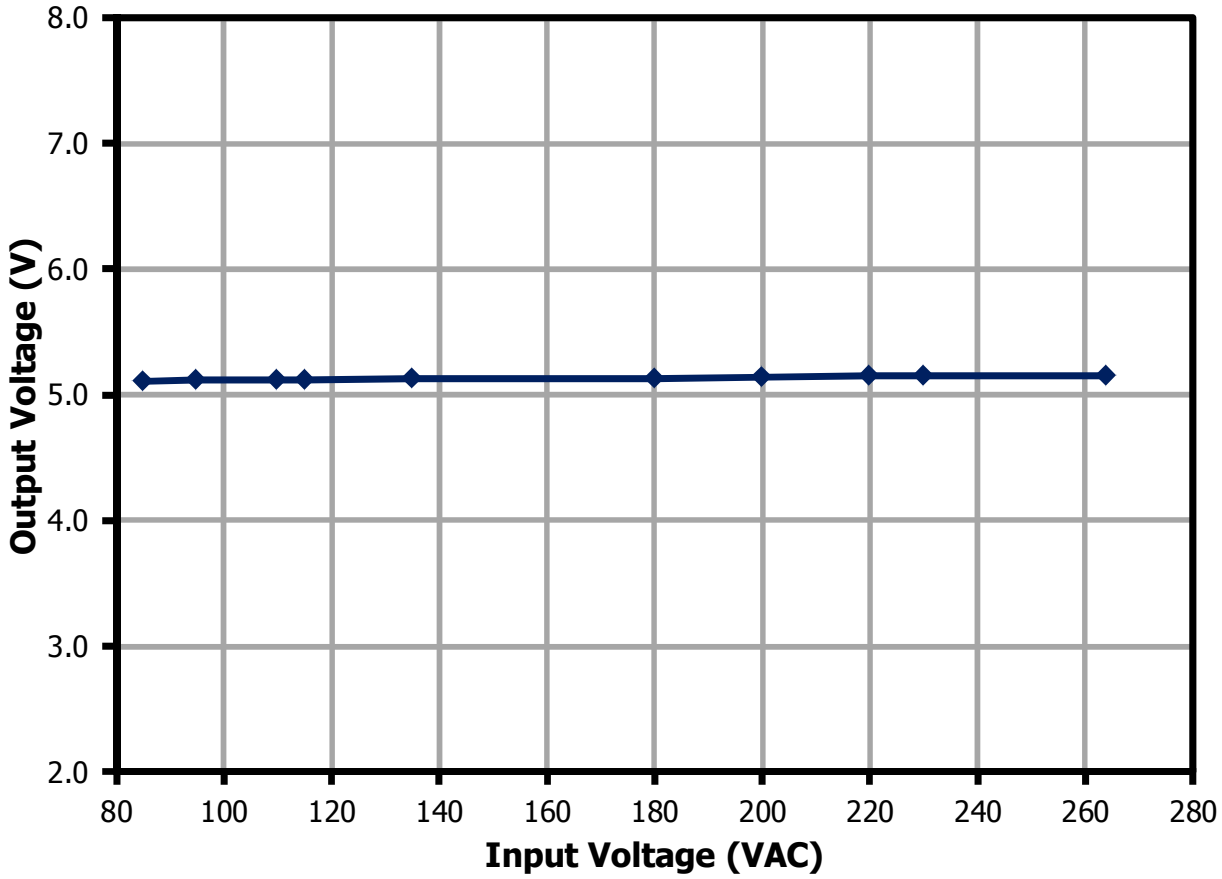

Figure 15 – Output Voltage vs. Input Line Voltage, Room Temperature.

9.7.2 Load Regulation

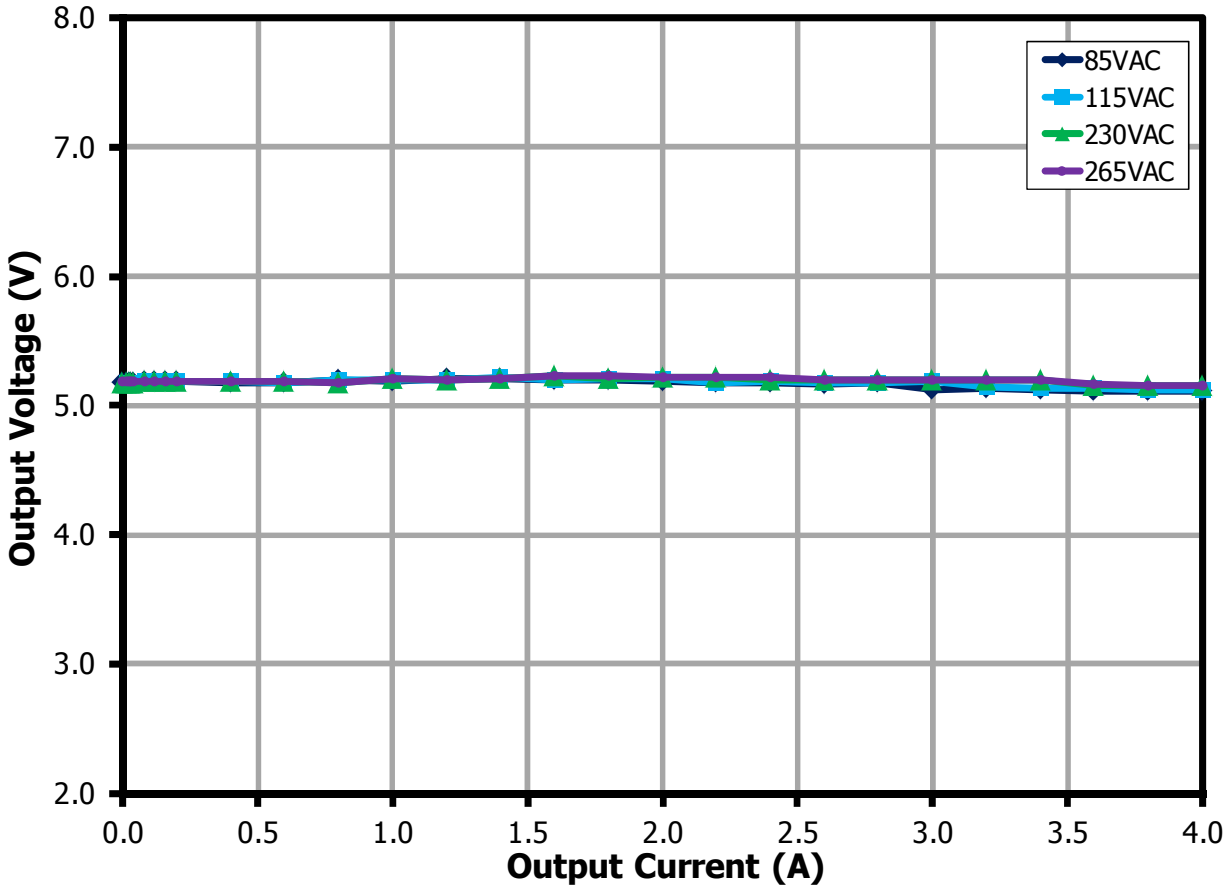

Figure 16 – Output Voltage vs. Output Load, Room Temperature.

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10 Thermal Performance

10.1 *Open Case*

10.1.1 85 VAC

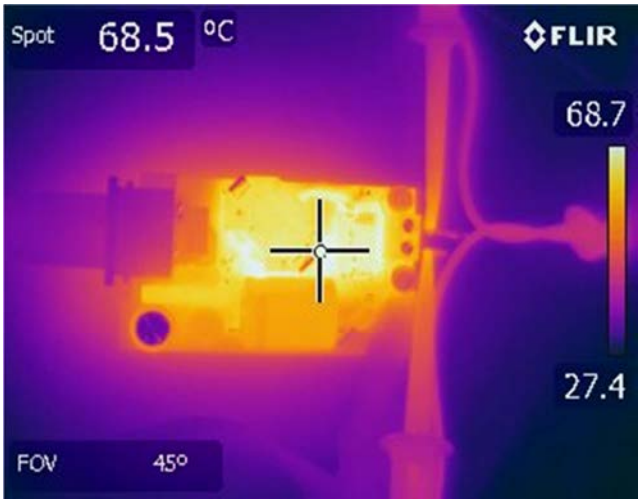

Figure 17 – Transformer Side.
85 VAC, 4 A Load.
Ambient = 27.4 ºC.
Transformer, T1 = 65.4 ºC.
Input Capacitor, C1 = 30.3 ºC.
Input Capacitor, C2 = 53.6 ºC.
Bridge Rectifier, BR1 = 60.2 ºC.
Differential Choke, L3 = 51.1 ºC.

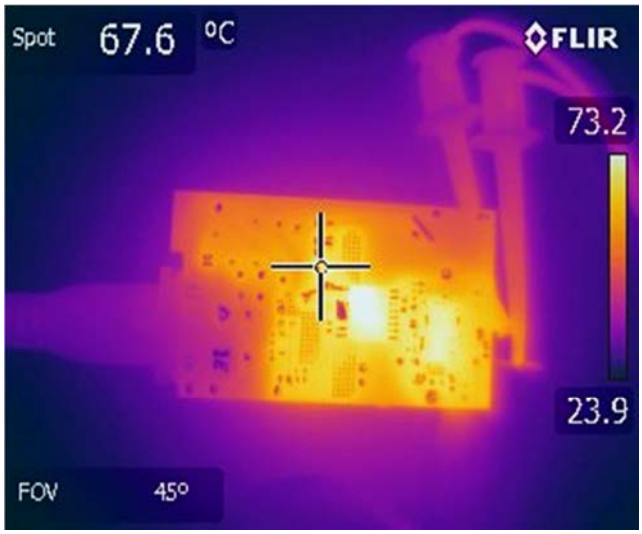

Figure 18 – InnoSwitch-CH Side.
85 VAC, 4 A Load.
Ambient = 24.5 ºC.
InnoSwitch-CH, U1 = 76 ºC.
SR FET, Q1 = 70 ºC.
SR FET, Q2 = 71.4 ºC.
Clamp Resistor, R2 = 68.2 ºC.

10.1.2 110 VAC

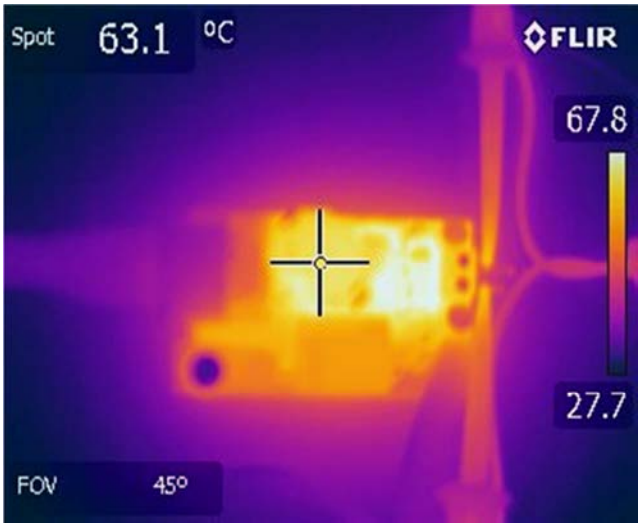

Figure 19 – Transformer Side.
110 VAC, 4 A Load.
Ambient = 27.6 ºC.
Transformer, T1 = 62.6 ºC.
Input Capacitor, C1 = 29.3 ºC.
Input Capacitor, C2 = 50.6 ºC.
Bridge Rectifier, BR1 = 53.3 ºC.
Differential Choke, L3 = 46.6 ºC.

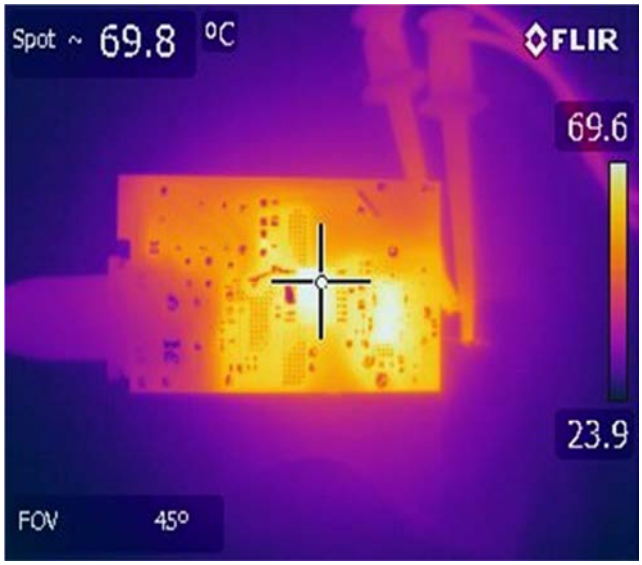

Figure 20 – InnoSwitch-CH Side.
110 VAC, 4 A Load.
Ambient = 25 ºC.
InnoSwitch-CH, U1 = 72.4 ºC.
SR FET, Q1 = 69.4 ºC.
SR FET, Q2 = 70 ºC.
Clamp Resistor, R2 = 65 ºC.

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10.1.3 230 VAC

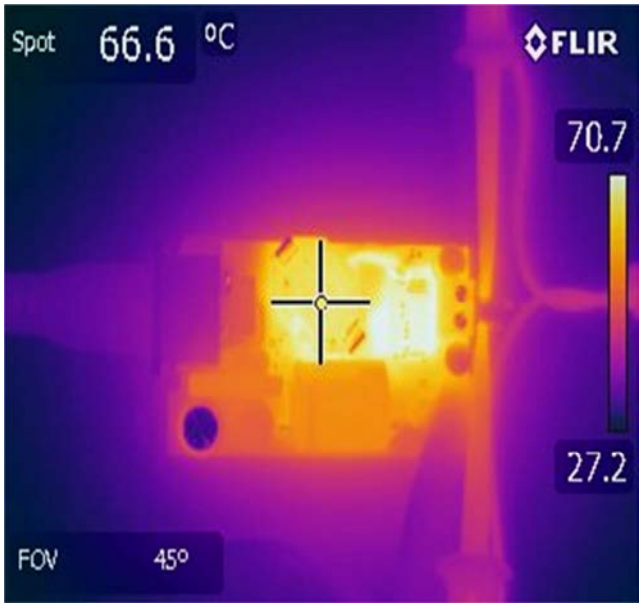

Figure 21 – Transformer Side.
230 VAC, 4 A Load.
Ambient = 27.4 ºC.
Transformer, T1 = 66.3 ºC.
Input Capacitor, C1 = 29 ºC.
Input Capacitor, C2 = 50.5 ºC.
Bridge Rectifier, BR1 = 47.1 ºC.
Differential Choke, L3 = 43.5 ºC.

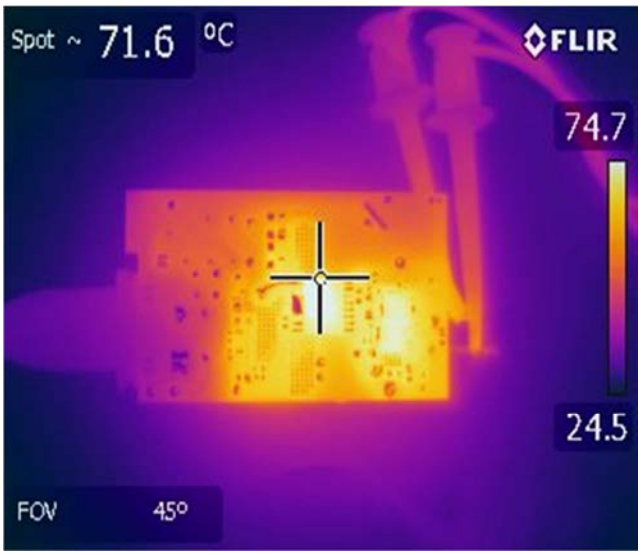

Figure 22 – InnoSwitch-CH Side.
230 VAC, 4 A Load.
Ambient = 25.3 ºC.
InnoSwitch-CH, U1 = 78.2 ºC.
SR FET, Q1 = 73.1 ºC.
SR FET, Q2 = 73.9 ºC.
Clamp Resistor, R2 = 64 ºC.

10.1.4 265 VAC

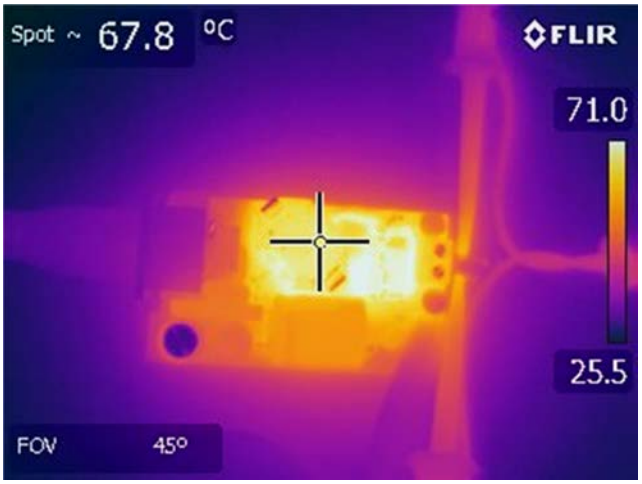

Figure 23 – Transformer Side.
265 VAC, 4 A Load.
Ambient = 27.4 ºC.
Transformer, T1 67.3 ºC.
Input Capacitor, C1 = 28.5 ºC.
Input Capacitor, C2 = 51.5 ºC.
Bridge Rectifier, BR1 = 46.4 ºC.
Differential Choke, L3 = 43 ºC.

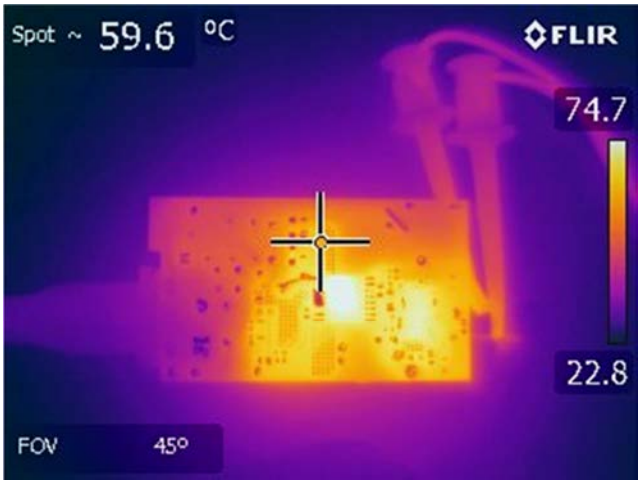

Figure 24 – InnoSwitch-CH Side.
265 VAC, 4 A Load.
Ambient = 23.8 ºC.
InnoSwitch-CH, U1 = 78.8 ºC.
SR FET, Q1 = 71.4 ºC.
SR FET, Q2 = 72.7 ºC.
Clamp Resistor, R2 = 66.1 ºC.

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10.2 ***Thermal Data with the Box Closed***

Measured with #30 AWG thermocouple. Ambient temperature: 25.7 ºC.

Component, Reference Location	Input Voltage (VAC)			
	85	110	230	265
	(ºC)	(ºC)	(ºC)	(ºC)
Transformer, T1	73.4	71.4	74.4	75.9
Input Capacitor, C1	55.9	52.2	48	48.1
Input Capacitor, C2	60	57.8	57.8	58.7
Bridge Rectifier, BR1	66.8	61.4	55.3	55.3
Differential Choke, L3	59.3	55.6	52.3	52.5
InnoSwitch-CH, U1	78.2	74.8	79.1	81.3
SR FET, Q1	72.5	71.5	74.6	75.7
SR FET, Q2	75.3	74.3	77.5	78.8
Clamp Resistor, R2	75.5	71.8	72.2	73.5

11 **Waveforms**

11.1 ***Load Transient Response (End of 1 M Cable)***

Results were measured with 47 µF at end of cable which is the typical specified measurement condition for adapters.

Figure 25 – Transient Response.
85 VAC, 0 - 4 A Load Step.
V_{MIN} 4.66 V, V_{MAX}: 5.34 V.
Upper: I_{LOAD}, 2 A / div.
Lower: V_{OUT}, 1 V, 100 ms / div.

Figure 26 – Transient Response.
110 VAC, 0 - 4 A Load Step.
V_{MIN}: 4.67 V, V_{MAX}: 5.34 V.
Upper: I_{LOAD}, 2 A / div.
Lower: V_{OUT}, 1 V, 100 ms / div.

Figure 27 – Transient Response.
230 VAC, 0-4 A Load Step.
V_{MIN}: 4.74 V, V_{MAX}: 5.34 V.
Upper: I_{LOAD}, 2 A / div.
Lower: V_{OUT}, 1 V, 100 ms / div.

Figure 28 – Transient Response.
265 VAC, 0 - 4 A Load Step.
V_{MIN}: 4.74 V, V_{MAX}: 5.35 V.
Upper: I_{LOAD}, 2 A / div.
Lower: V_{OUT}, 1 V, 100 ms / div.

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11.2 *Switching Waveforms*

11.2.1 InnoSwitch-CH Waveforms

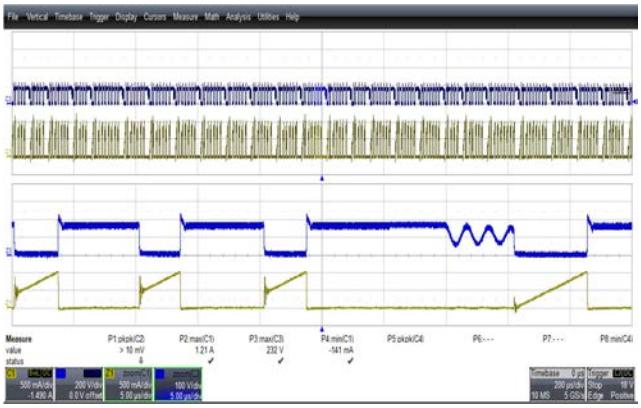

Figure 29 – Drain Voltage and Current Waveforms.
85 VAC, 4 A Load.
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 200 µs, 5 µs / div.

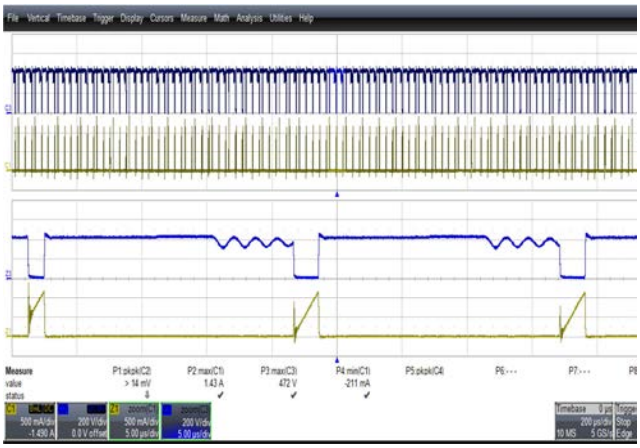

Figure 30 – Drain Voltage and Current Waveforms.
265 VAC, 4 A Load, (472 V_{MAX}).
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 200 µs, 5 µs / div.

11.2.2 Drain Voltage and Current Waveforms During Turn-On

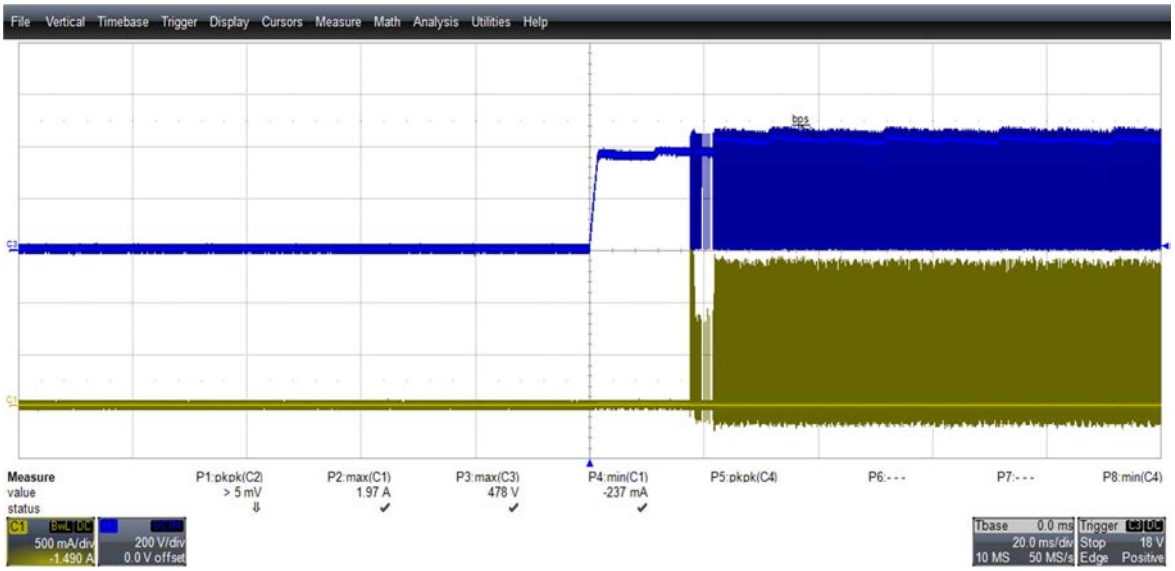

Figure 31 – Drain Voltage and Current Waveforms.
265 VAC, 4 A Load, (478 V_{MAX})
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 20 ms / div.

11.2.3 SR FET Waveforms

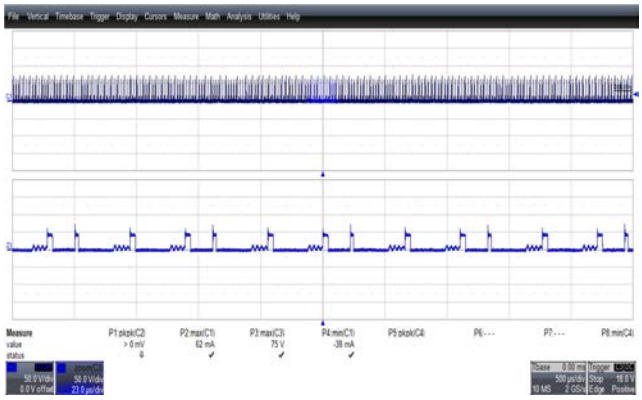

Figure 32 – SR FET Voltage Waveforms.
265 VAC Input, 4 A Load, (75 V_{MAX}).
V_{DRAIN}, 50 V, 500 µs, 23 µs / div.

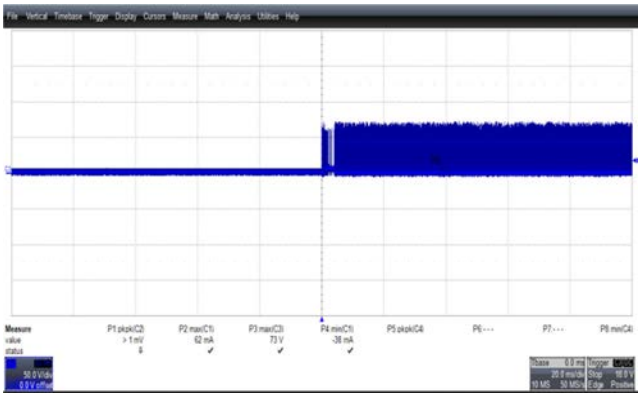

Figure 33 – SR FET Voltage Waveforms During Turn-On.
265 VAC Input, 4 A Load, (73 V_{MAX}).
V_{DRAIN}, 20 V, 20 ms / div.

11.2.4 Output Voltage and Current Waveforms During Turn-On (No-Load)

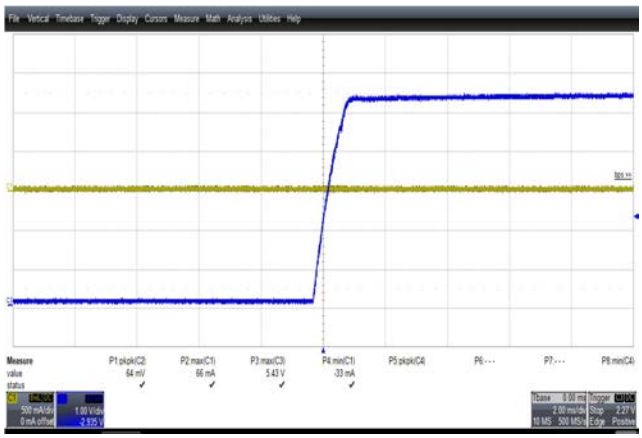

Figure 34 – Output Voltage and Current Waveforms.
85 VAC Input.
Lower: I_{OUT}, 500 mA / div.
Upper: V_{OUT}, 1 V, 2 ms / div.

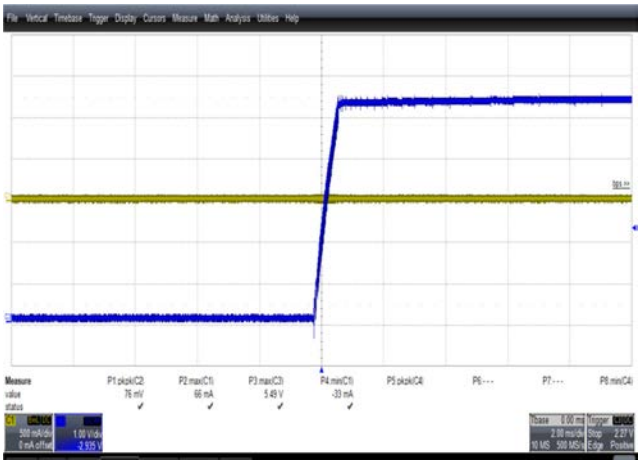

Figure 35 – Output Voltage and Current Waveforms.
265 VAC Input.
Lower: I_{OUT}, 500 mA / div.
Upper: V_{OUT}, 1 V, 2 ms / div.

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11.2.5 Output Voltage and Current Waveforms During Turn-On (4 A Resistive Load)

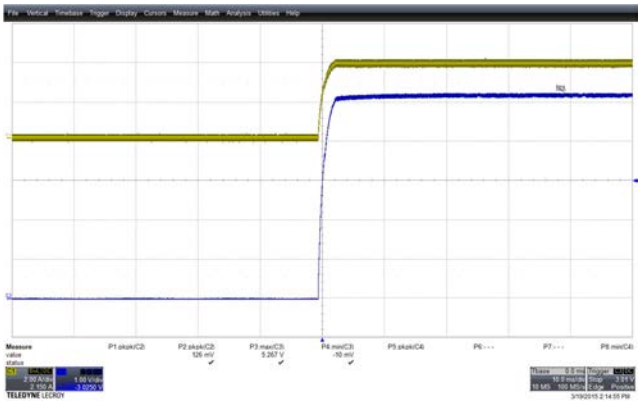

Figure 36 – Output Voltage and Current Waveforms.
85 VAC Input.
Lower: V_{OUT}, 1 V / div.
Upper: I_{OUT}, 2 A, 10 ms / div.

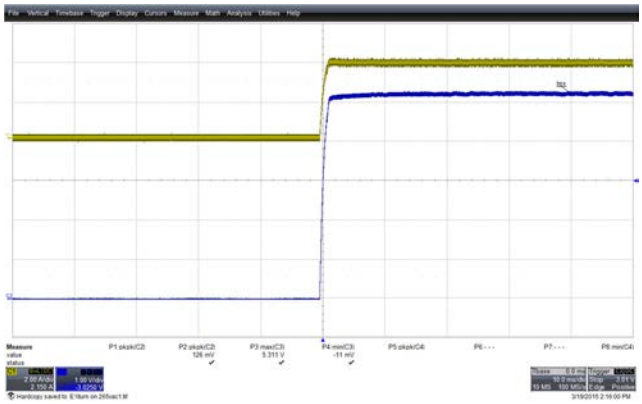

Figure 37 – Output Voltage and Current Waveforms.
265 VAC Input.
Lower: V_{OUT}, 1 V / div.
Upper: I_{OUT}, 2 A, 10 ms / div.

11.2.6 Output Voltage and Current Waveform with Shorted Output

Figure 38 – Output Voltage and Current Waveforms.
85 VAC Input.
Lower: I_{OUT}, 2 A / div.
Upper: V_{OUT}, 2 V, 2 s / div.

Figure 39 – Output Voltage and Current Waveforms.
265 VAC Input.
Lower: I_{OUT}, 5 A / div.
Upper: V_{OUT}, 2 V, 2 s / div.

11.3 *Output Voltage and Current Waveform with Open Feedback Loop*

Latched off for overvoltage protection (Loop opened while power supply was in operation)

Note: For the purpose of this test, output capacitors were replaced with capacitors rated for 16 V as aluminum-Polymer capacitors used in this power supply output are sensitive and could be rendered defective after conducting this test as they generally cannot withstand higher voltage)

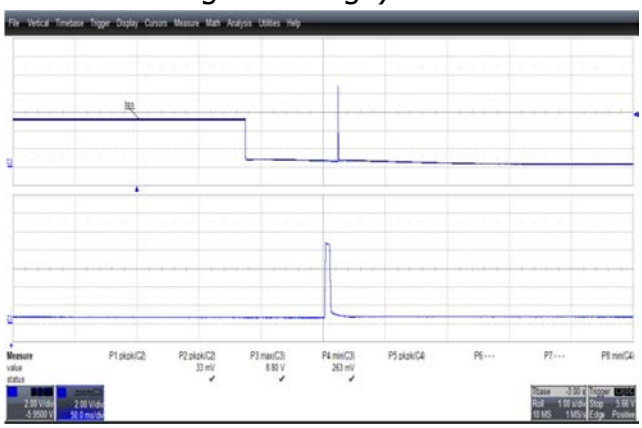

Figure 40 – Output Voltage Waveform.
85 VAC Input.
V_{OUT}, 2 V, 1 s, 50 ms / div.

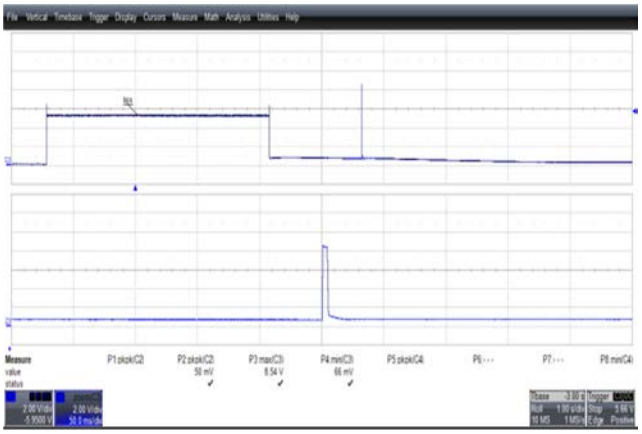

Figure 41 – Output Voltage Waveform.
265 VAC Input.
V_{OUT}, 2 V, 1 s, 50 ms / div.

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11.4 ***Output Ripple Measurements***

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF/50 V ceramic type and one (1) 47 µF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

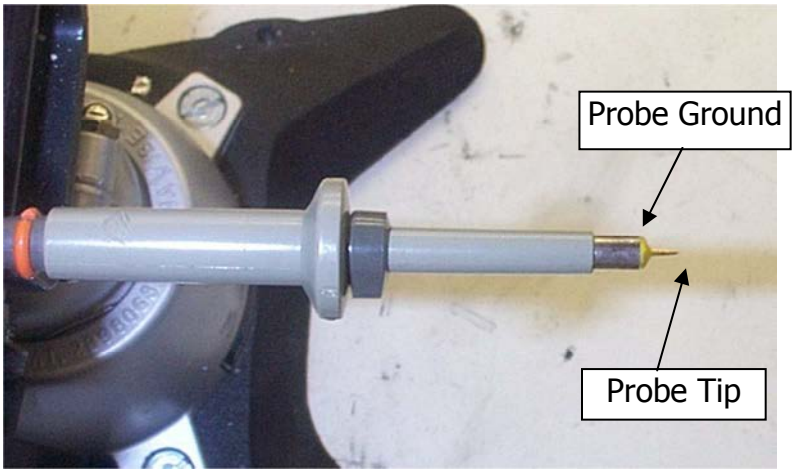

Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

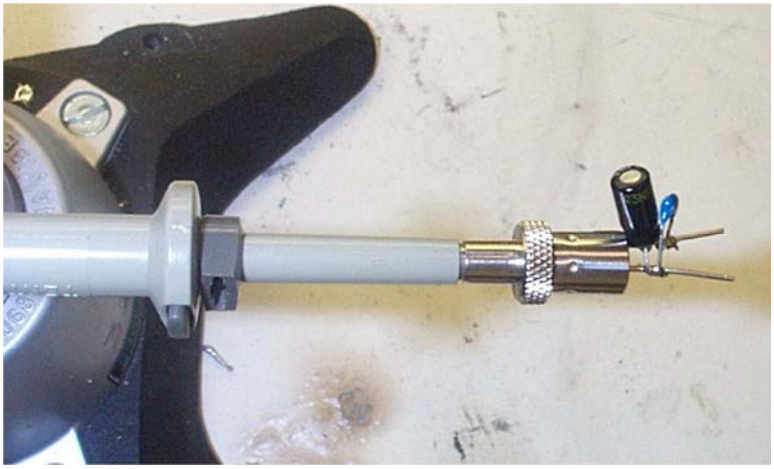

Figure 43 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.4.2 Measurement Results

Measured at the end of 1 m cable.

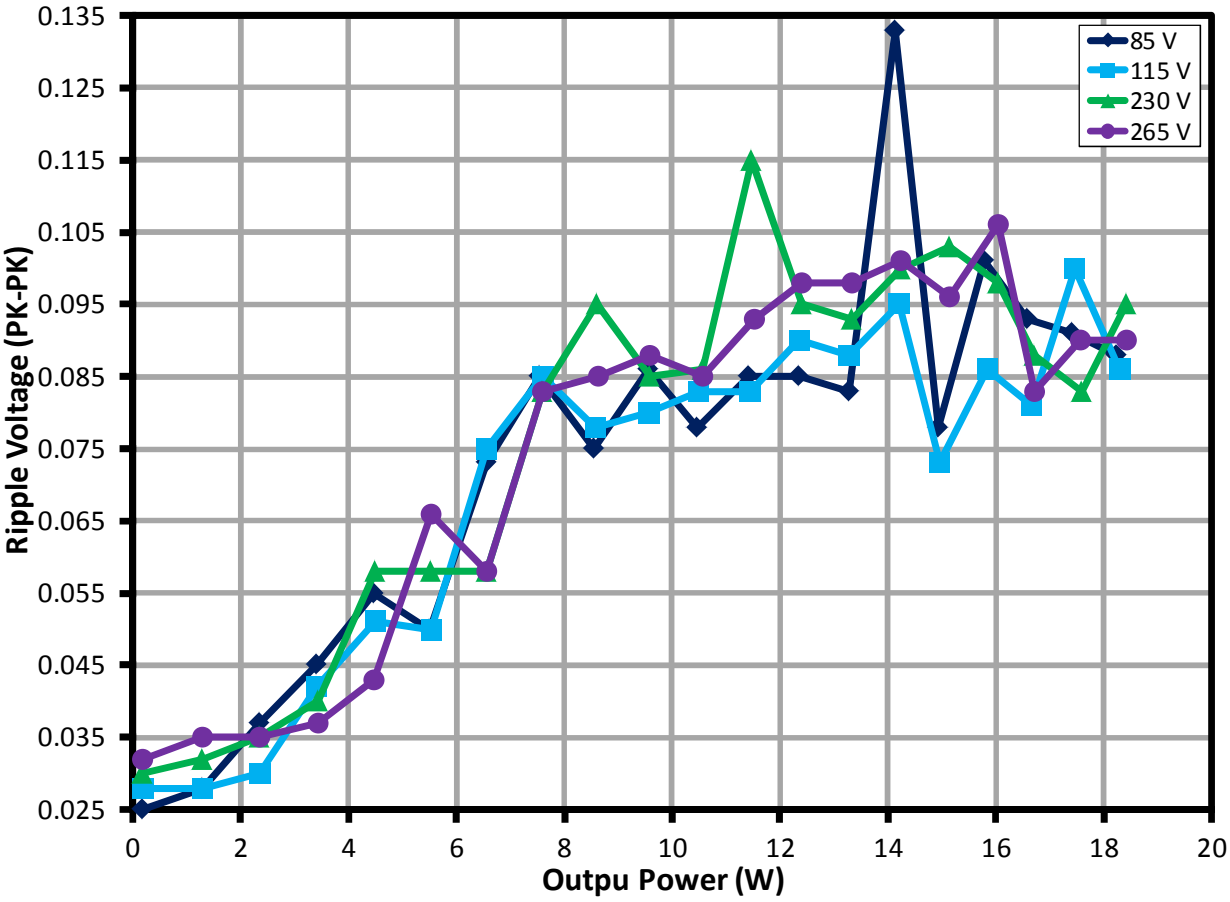

Figure 44 – Output Ripple Voltage.

85 V RIPPLE (V_{PK-PK})	115 V RIPPLE (V_{PK-PK})	230 V RIPPLE (mV_{PK-PK})	265 V RIPPLE (V_{PK-PK})
0.133	0.100	0.115	0.106

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11.4.3 Ripple Voltage Waveforms

Figure 45 – Output Voltage and Current Waveforms.
85 VAC Input
V_{RIPPLE}, 50 mV / div., 20 ms, 100 µs / div.

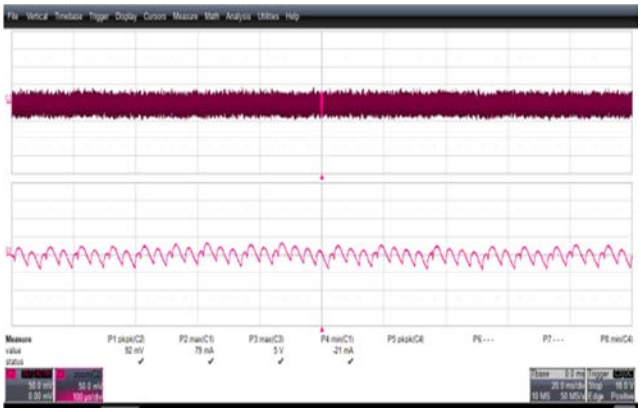
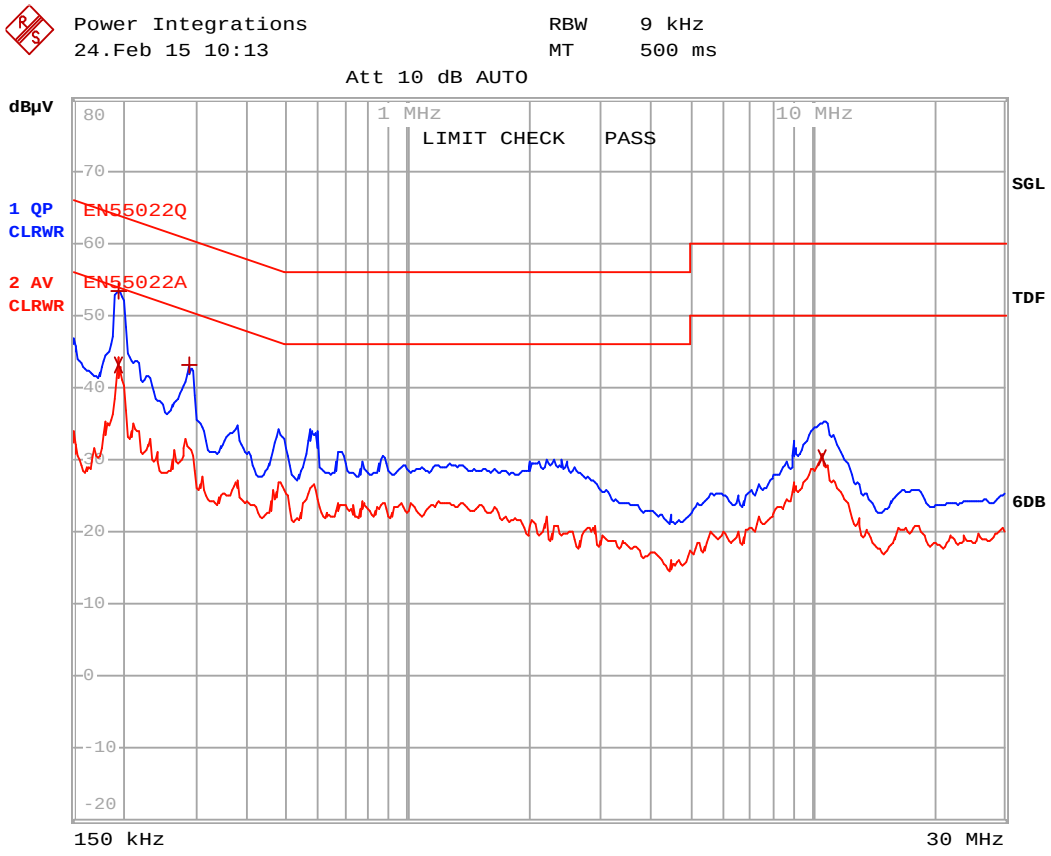


Figure 46 – Output Voltage and Current Waveforms.
265 VAC Input.
V_{RIPPLE}, 50 mV / div., 20 ms, 100 µs / div.

12 Conducted EMI

12.1 *4 A Resistive Load, Floating Output (QP / AV)*

12.1.1 115 VAC



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	194.040994568 kHz	53.36	L1 gnd	-10.49
2	Average	194.040994568 kHz	43.11	N gnd	-10.74
1	Quasi Peak	288.334710591 kHz	43.19	L1 gnd	-17.38
2	Average	10.5956642433 MHz	30.30	N gnd	-19.69

Figure 47 – Floating Ground EMI at 115 VAC.

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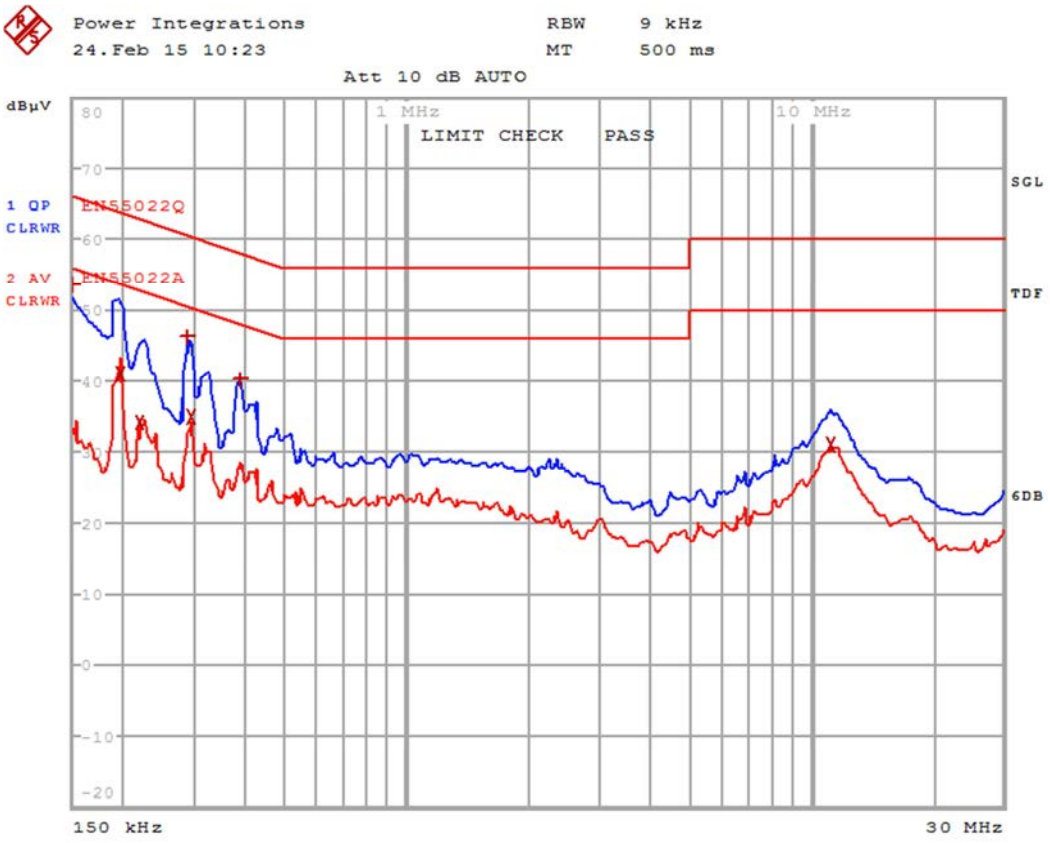
12.1.2 230 VAC



EDIT PEAK LIST (Final Measurement Results)

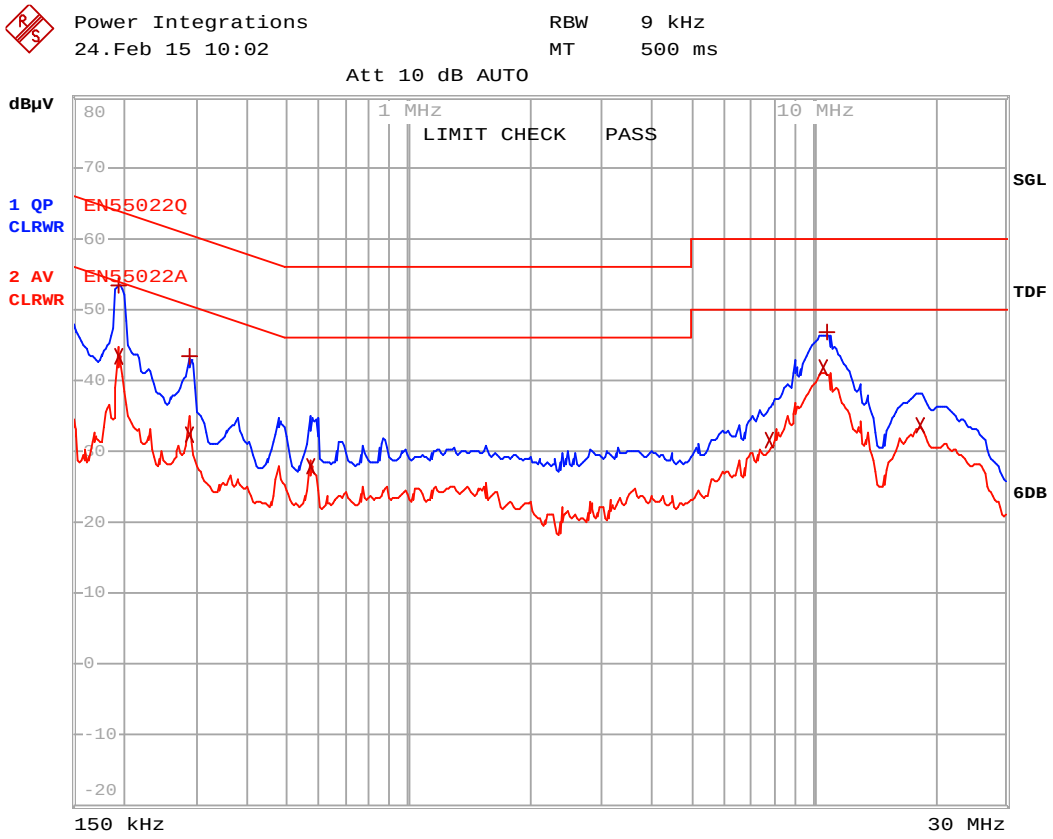
Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	53.64	L1 gnd	-12.35
2	Average	197.921814459 kHz	41.02	N gnd	-12.66
2	Average	218.521675879 kHz	34.09	N gnd	-18.77
1	Quasi Peak	288.334710591 kHz	46.33	L1 gnd	-14.23
2	Average	294.101404803 kHz	35.04	N gnd	-15.36
1	Quasi Peak	388.060557825 kHz	40.11	L1 gnd	-17.98
2	Average	11.2442036603 MHz	30.97	N gnd	-19.02

Figure 48 – Floating Ground at 230 VAC.

12.2 *4 A Resistive Load, Artificial Hand Ground (QP / AV)*

12.2.1 115 VAC



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	194.040994568 kHz	53.47	L1 gnd	-10.38
2	Average	194.040994568 kHz	43.31	N gnd	-10.55
1	Quasi Peak	288.334710591 kHz	43.47	L1 gnd	-17.09
2	Average	288.334710591 kHz	32.35	N gnd	-18.21
2	Average	576.637575382 kHz	27.89	N gnd	-18.10
2	Average	7.87273460681 MHz	31.67	L1 gnd	-18.32
2	Average	10.5956642433 MHz	41.87	L1 gnd	-8.12
1	Quasi Peak	10.8075775282 MHz	46.74	L1 gnd	-13.25
2	Average	18.4473079281 MHz	33.59	L1 gnd	-16.40

Figure 49 – Artificial Ground at 115 VAC.

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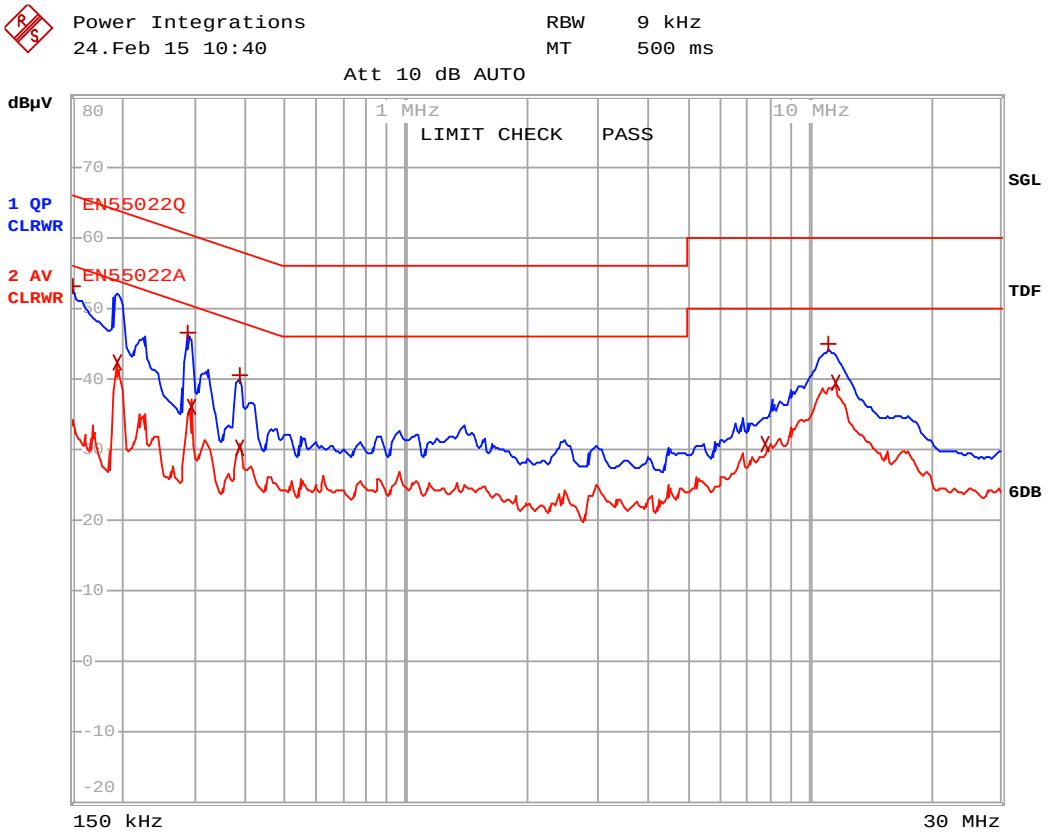
12.2.2 230 VAC



EDIT PEAK LIST (Final Measurement Results)

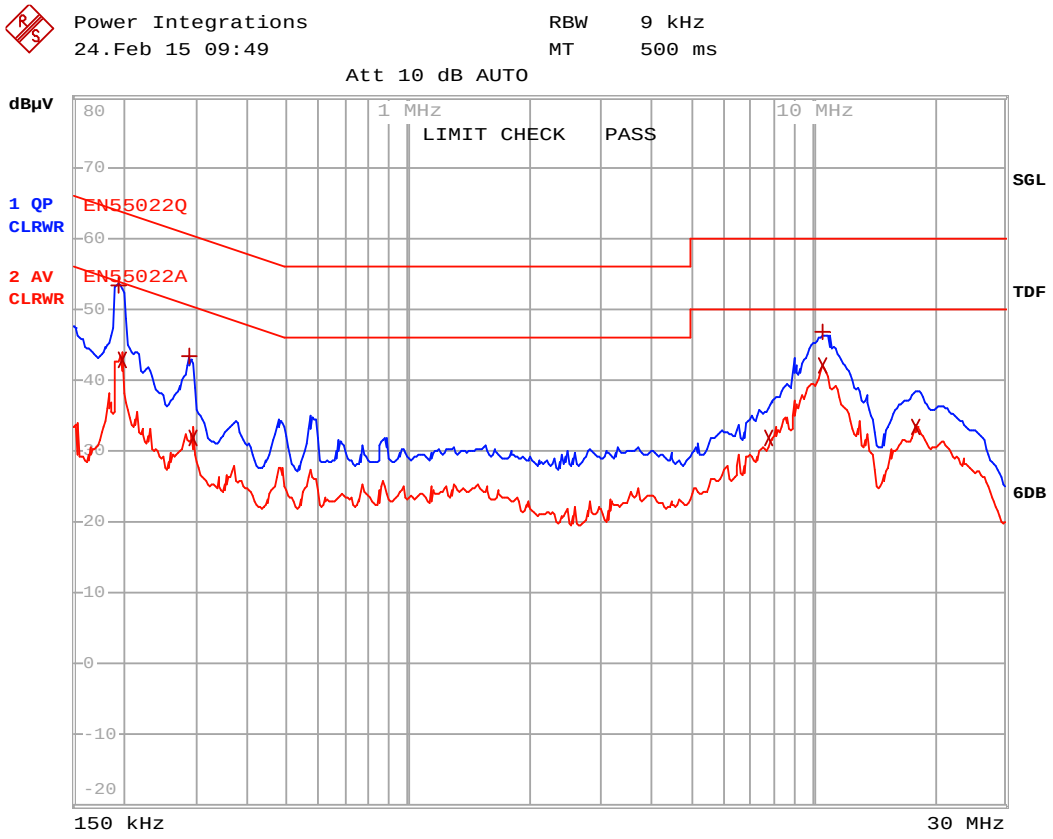
Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	52.97	L1 gnd	-13.02
2	Average	194.040994568 kHz	42.23	N gnd	-11.62
1	Quasi Peak	288.334710591 kHz	46.59	L1 gnd	-13.97
2	Average	294.101404803 kHz	36.06	N gnd	-14.34
1	Quasi Peak	388.060557825 kHz	40.59	L1 gnd	-17.51
2	Average	388.060557825 kHz	30.38	N gnd	-17.71
2	Average	7.87273460681 MHz	30.91	L1 gnd	-19.09
1	Quasi Peak	11.2442036603 MHz	45.08	L1 gnd	-14.91
2	Average	11.6984694882 MHz	39.45	L1 gnd	-10.54

Figure 50 – Artificial Ground at 230 VAC.

12.3 *4 A Resistive Load, Earth Ground (QP / AV)*

12.3.1 115 VAC



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	194.040994568 kHz	53.47	L1 gnd	-10.38
2	Average	197.921814459 kHz	42.81	N gnd	-10.87
1	Quasi Peak	288.334710591 kHz	43.42	L1 gnd	-17.15
2	Average	294.101404803 kHz	31.83	N gnd	-18.57
2	Average	7.87273460681 MHz	31.70	L1 gnd	-18.29
1	Quasi Peak	10.5956642433 MHz	46.78	L1 gnd	-13.21
2	Average	10.5956642433 MHz	42.05	L1 gnd	-7.94
2	Average	18.085596008 MHz	33.37	L1 gnd	-16.62

Figure 51 – Earth Ground at 115 VAC.

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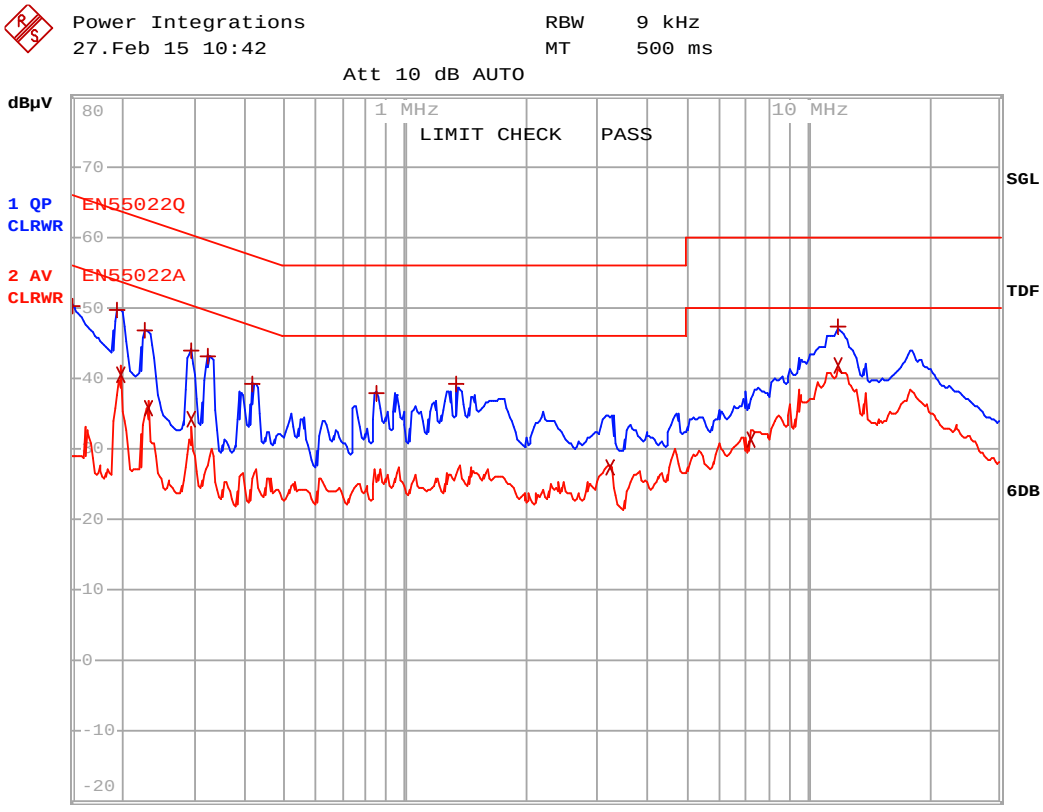
12.3.2 230 VAC



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

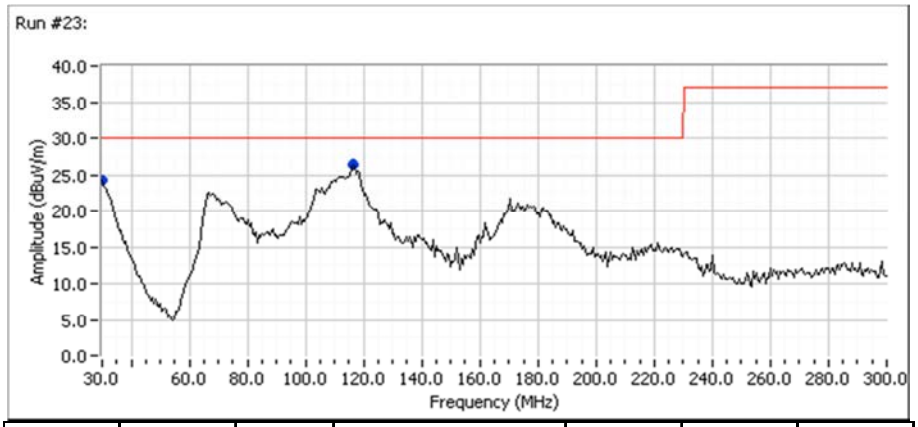
	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	50.18	N gnd	-15.82
1	Quasi Peak	194.040994568 kHz	49.69	N gnd	-14.16
2	Average	197.921814459 kHz	40.57	L1 gnd	-13.12
1	Quasi Peak	227.349951585 kHz	46.89	N gnd	-15.65
2	Average	231.896950616 kHz	35.68	L1 gnd	-16.70
1	Quasi Peak	294.101404803 kHz	43.99	N gnd	-16.41
2	Average	294.101404803 kHz	34.18	L1 gnd	-16.22
1	Quasi Peak	324.711715237 kHz	43.21	N gnd	-16.37
1	Quasi Peak	420.049227817 kHz	39.28	N gnd	-18.16
1	Quasi Peak	856.853103562 kHz	37.95	N gnd	-18.05
1	Quasi Peak	1.35117102853 MHz	39.07	N gnd	-16.92
2	Average	3.22937056272 MHz	27.47	N gnd	-18.52
2	Average	7.27318985682 MHz	31.29	N gnd	-18.71
1	Quasi Peak	11.932438878 MHz	47.30	L1 gnd	-12.69
2	Average	11.932438878 MHz	41.73	L1 gnd	-8.26

Figure 52 – Earth Ground at 230 VAC**.**

12.4 ***Radiated EMI, 5 V 4 A Resistive Load Without Output Cable***

12.4.1 115 VAC Input

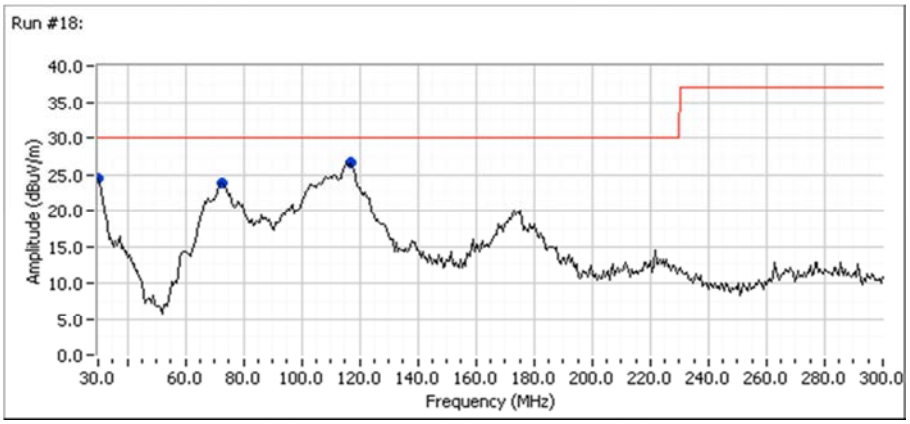
12.4.1.1 Floating Ground



Frequency	Level	Pol	EN 55022 Class B		Detector	Azimuth	Height
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
116.102	22.9	V	30.0	-7.1	QP	291	1.0
30.163	20.5	V	30.0	-9.5	QP	331	1.5

Figure 53 – Radiation at 115 VAC Floating Ground.

12.4.1.2 Earth Ground



Frequency	Level	Pol	EN 55022 Class B		Detector	Azimuth	Height
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
116.985	24.0	V	30.0	-6.0	QP	244	1.0
116.985	23.9	V	30.0	-6.1	QP	245	1.0
72.465	20.8	V	30.0	-9.2	QP	150	1.5

Figure 54 – Radiation at 115 VAC Earth Ground.

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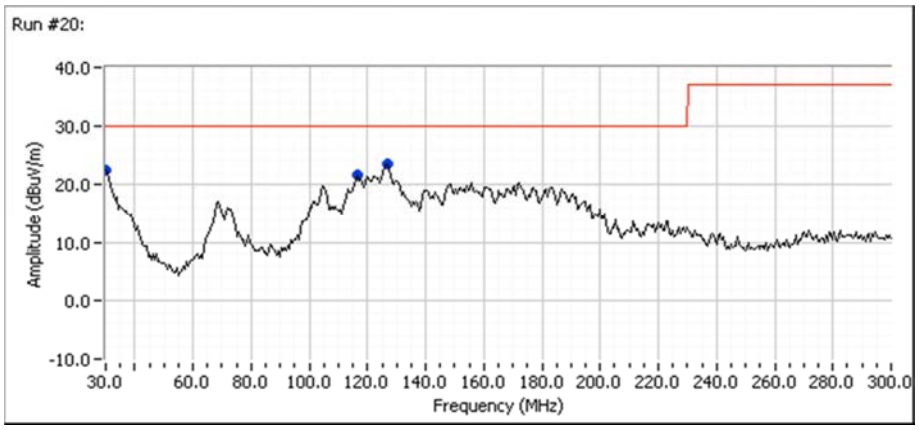
12.4.2 230 VAC Input

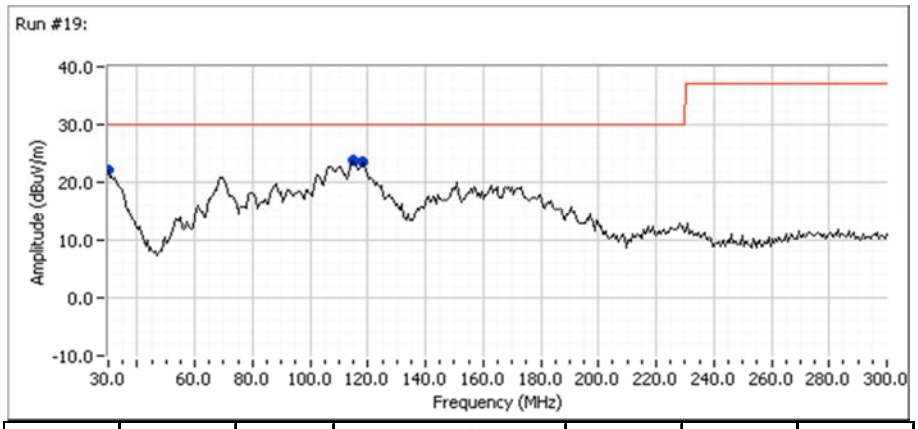
12.4.2.1 Floating Ground



Frequency	Level	Pol	EN 55022 Class B		Detector	Azimuth	Height
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
126.485	22.2	V	30.0	-7.8	QP	285	1.5
116.654	19.6	V	30.0	-10.4	QP	314	1.0
30.531	18.1	V	30.0	-11.9	QP	360	1.5

Figure 55 – Radiation at 230 VAC Floating Ground.

12.4.2.2 Earth Ground



Frequency	Level	Pol	EN 55022 Class B		Detector	Azimuth	Height
MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
114.927	21.2	V	30.0	-8.8	QP	293	1.0
118.444	18.9	V	30.0	-11.1	QP	222	1.0
30.159	17.2	V	30.0	-12.8	QP	91	1.5

Figure 56 – Radiation at 230 VAC Earth Ground.

13 **Audible Noise**

Test performed inside the plastic case with microphone placed 3 cm from case surface on long side of case, transformer facing towards microphone.

Figure 57 – Plastic Case Used for Test.

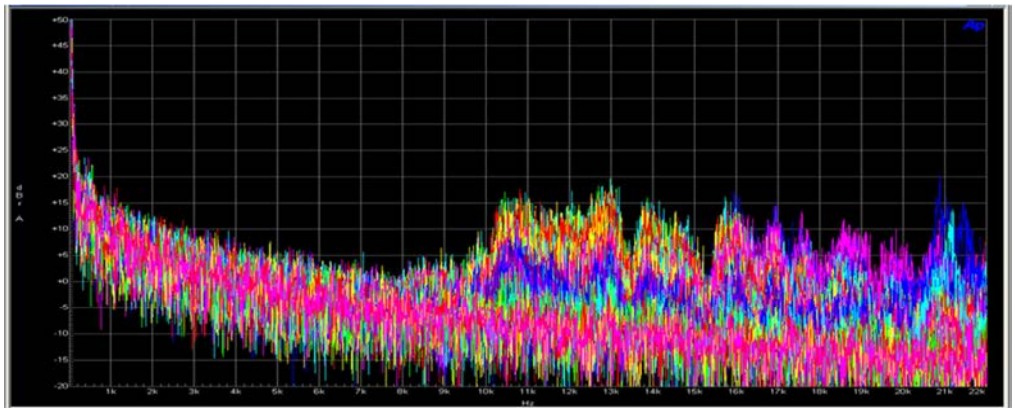


Figure 58 – Audible Noise Spectrum: 85 VAC, I_{OUT} Swept from 0 A to 4.0 A

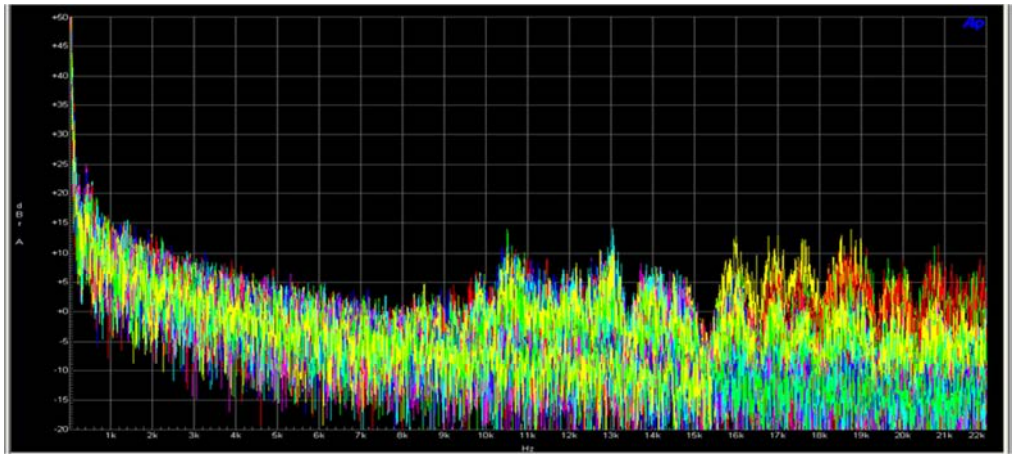


Figure 59 – Audible Noise Spectrum: 110 VAC, I_{OUT} Swept from 0 A to 4.0 A.

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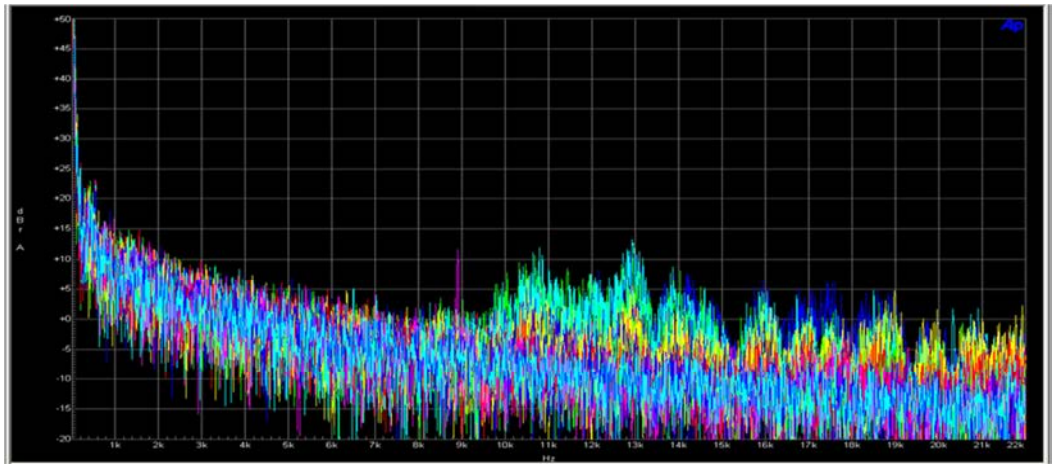

Figure 60 – Audible Noise Spectrum: 230 VAC, I_{OUT} Swept from 0 A to 4.0 A.

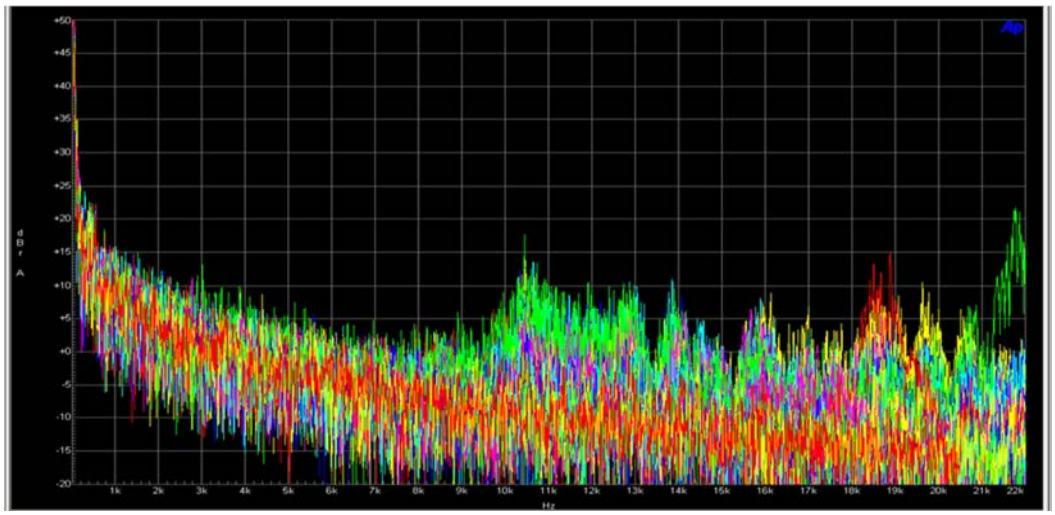

Figure 61 – Audible Noise Spectrum: 265 VAC, I_{OUT} Swept from 0 A to 4.0 A.

14 Lighting Surge and ESD Test

14.1 *Differential Mode Test*

Passed ±1 kV, 500 A surge test,

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
1	90	2	10	PASS
1	270	2	10	PASS

14.2 *Common Mode Test*

Passed ±6 kV, 500 A ring wave test

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
6	90	12	10	PASS
-6	90	12	10	PASS
6	270	12	10	PASS
-6	270	12	10	PASS

14.3 *ESD Test*

Passed ±15 kV Air Discharge, ±8 kV Contact Discharge Test Level (kV)	Input Voltage (VAC)	Discharge	Number of Discharges	Test Result
8	230	Contact	10	PASS
15	230	Air	10	PASS
-8	230	Contact	10	PASS
-15	230	Air	10	PASS

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15 **Revision History**

Date	Author	Revision	Description & Changes	Reviewed
22-May-15	RJ	1.4	Initial Release	Mktg & Apps

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