Design Example Report

Title	*12 W 24 V CV/CC, Isolated Flyback LED Driver Using LYTSwitch™-2 LYT2005E*
Specification	90 VAC – 265 VAC Input; 24 V, 500 mA Output
Application	External Ballast Constant Voltage LED Driver
Author	Applications Engineering Department
Document Number	DER-440
Date	September 29, 2015
Revision	1.0

Summary and Features

- Accurate (primary-side control) constant voltage
    - Accurate CV/CC, less than ±2% variation over load (1% to 100%) and line (90 VAC to 265 VAC)
- Average efficiency >85% at 230 VAC
- Power factor >0.7 full load at all line conditions.
- Low-cost, low component count (35), small PCB
- Fast start-up time (<100 ms) – no perceptible delay
- No-load consumption <30 mW at 115 VAC or 230 VAC
- Integrated protection and reliability features
    - Output short-circuit protected with auto-recovery
    - 130% maximum CC overcurrent protection
    - Auto-recovering thermal shutdown with large hysteresis
    - No damage during brown-out conditions, 1 kV differential surge and 2.5 kV ring wave
    - Easily meets EN55015 and CISPR-22 Class B EMI standards

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Table of Contents

Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a universal input, 24 V constant voltage, 500 mA LED driver. This power supply utilizes the LYT2005E device from the Power Integrations LYTSwitch-2 family.

This document contains the power supply and transformer specifications, schematics, bill of materials, and typical performance characteristics pertaining to this power supply.

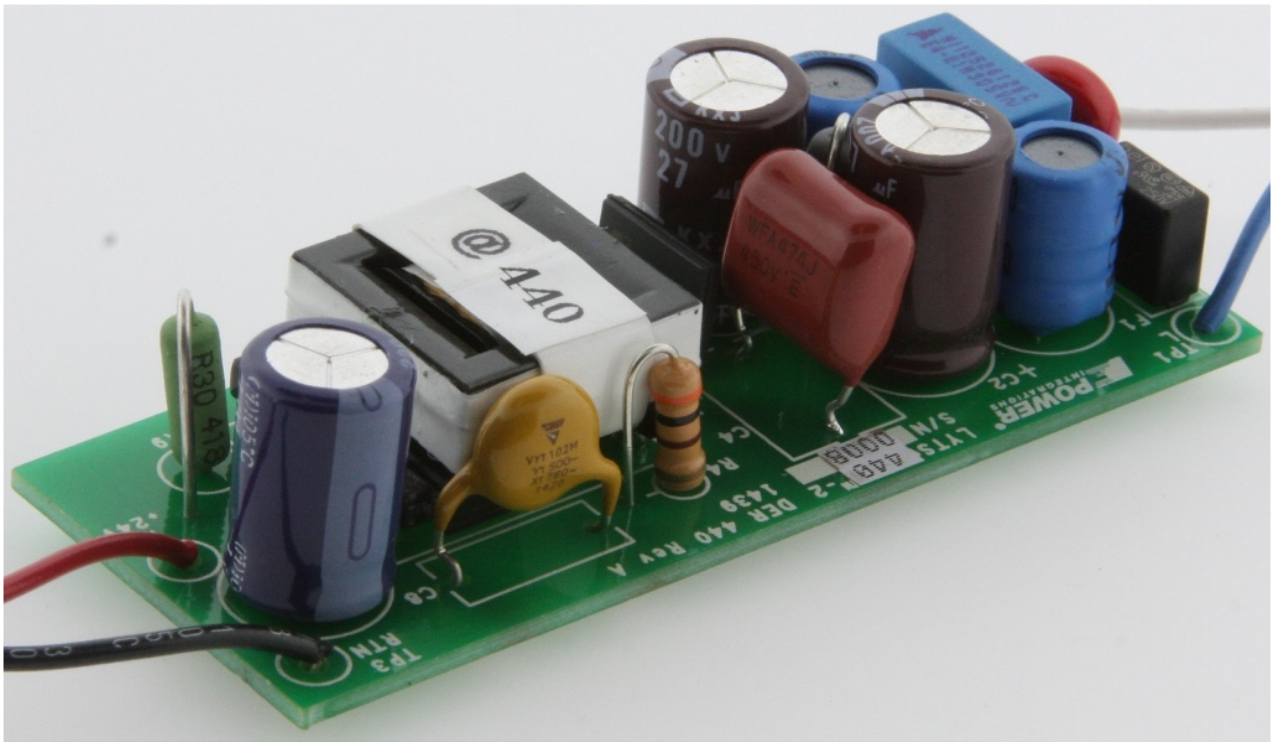

Figure 1 – Populated Circuit Board, Angle View.

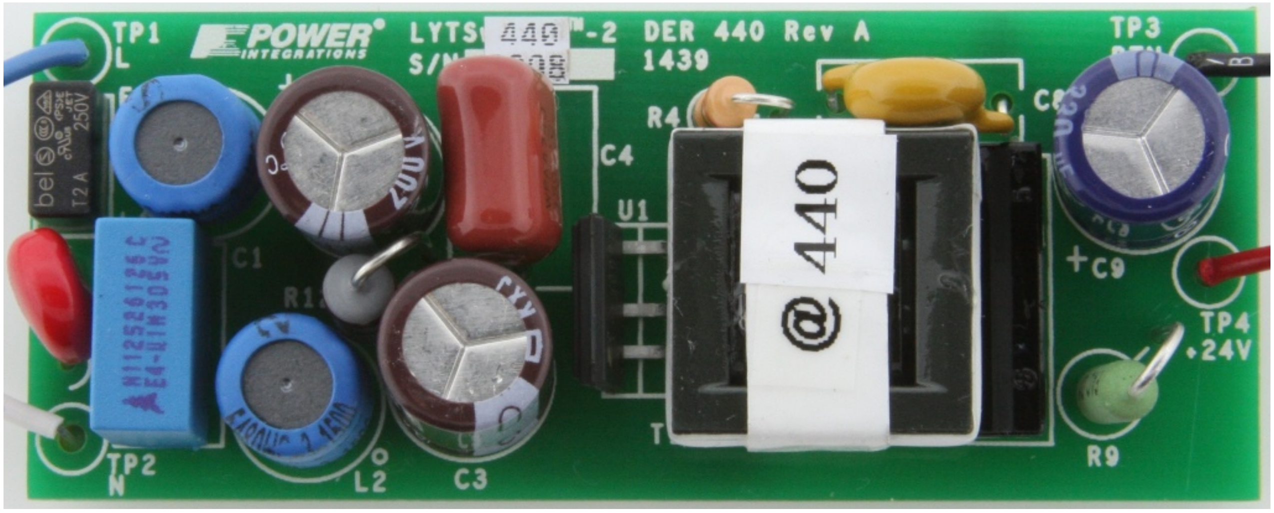

Figure 2 – Populated Circuit Board, Top View.

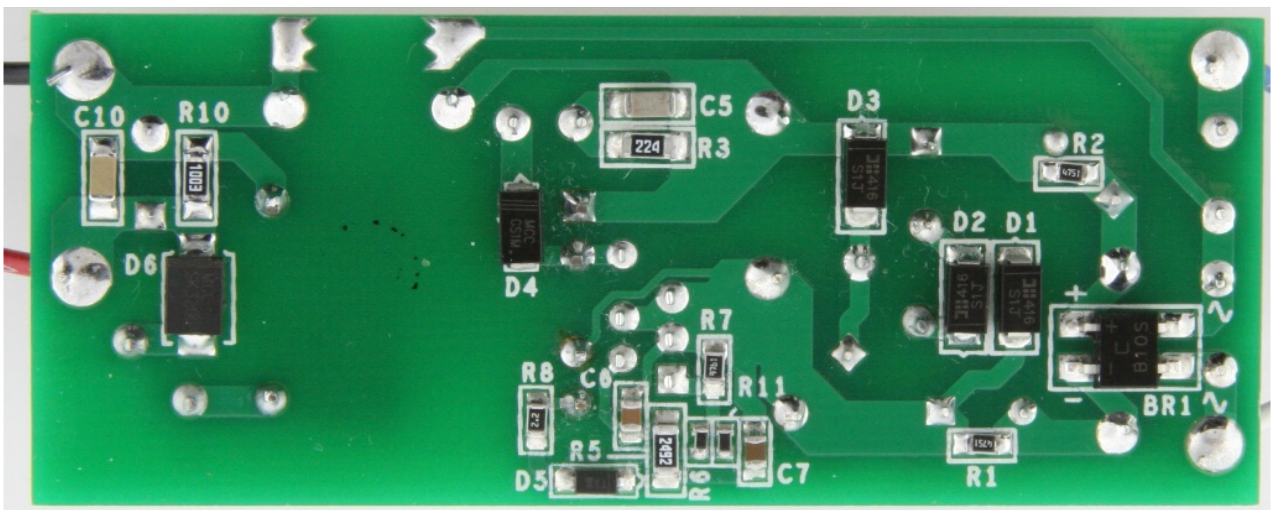

Figure 3 – Populated Circuit Board, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
No-load Input Power	P_{NL}		28		mW	Measure at V_{IN} = 230 VAC
Output						
Output Voltage	V_{OUT}	23.5	24	24.5	V	
Output Current	I_{OUT}			500	mA	25 ºC
Total Output Power						
Continuous Output Power	P_{OUT}	0		12	W	
Efficiency						
Full Load	η		86		%	Measured at P_{OUT} 25 ºC, 230 VAC
Ripple						
Output Voltage	V_{RIPPLE}			1000	mV_{PK-PK}	
Output Current	I_{RIPPLE}			100	mA_{PK-PK}	
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: 2 Ω
Differential Surge			1000		V	
ESD						
Contact Discharge		-8		+8	kV	IEC 61000-4-2
Air Discharge		-15		+15	kV	
Ambient Temperature	T_{AMB}		40		°C	

3 Schematic Diagram

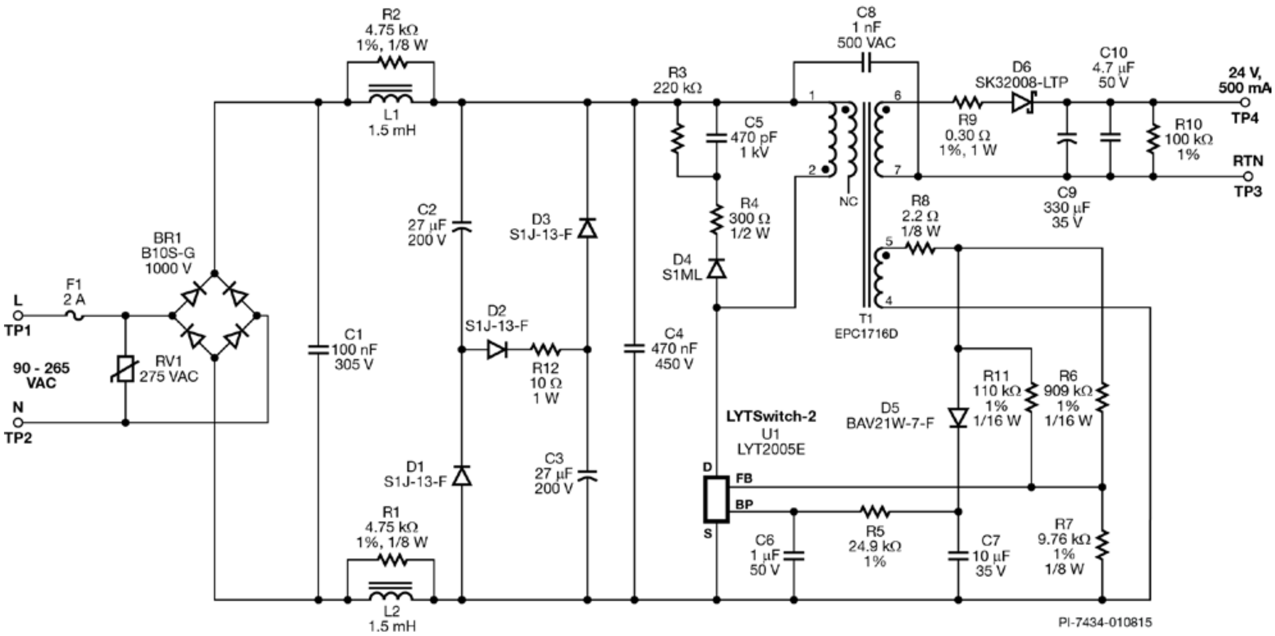

Figure 4 – Schematic.

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4 Circuit Description

4.1 Input Circuit

The power supply unit is protected with 2 A slow blow fuse F1. Varistor RV1 clamps surge voltages to safe levels. AC input power is rectified by bridge BR1 to bulk voltage for DC-DC conversion.

The circuit does not need a thermistor in series with the AC line input. This can be added to reduce in-rush current.

4.2 EMI Filter

Inductors L1, L2, with capacitors C1 and C4, form pi (π) filters to attenuate conducted differential-mode noise. This configuration along with a balanced transformer design, grounded core, belly band, and the Y capacitor C8 allows this circuit to meet EMI EN55022 class B with good margin. Resistors R1 and R2 damp the self-resonance of the inductors L1 and L2 to avoid noise peaking in the conducted EMI plot at their resonant frequency. The capacitance of C1 and C4 is minimized for best power factor.

4.3 Valley-Fill Circuit

Capacitor C2, C3, R12, D1, D2 and D3 form a cost effective valley-fill PFC stage. This allows sufficient input capacitance for hold-up near the zero crossing. Diode D2 and R12 provide a charging path for C2 and C3 during peak voltage without creating an in-rush current when D1 and D3 are the discharge path for the valley-fill.

4.4 LYTSwitch-2 Primary

The LYTSwitch-2 (U1) incorporates the power switching device, oscillator, CV/CC control engine, start-up and protection functions in one IC. The integrated 725 V power MOSFET allows sufficient voltage margin for universal input AC conditions, including extended line swells.

The valley-filled rectified voltage is applied to one end of the primary winding of transformer (T1). The other end of the transformer's primary winding is driven by the internal power MOSFET of U1. An RCD-R clamp consisting of R3, C5, D4 and R4 limits drain voltage spikes caused by leakage inductance. The clamp circuit is optimized in order to prevent any excessive ringing on the drain voltage waveform which may affect regulation.

The external bias supply, D5, R5, and C7 improves efficiency and reduces no-load input power to less than 30 mW at nominal input voltage. A high value for resistor R5 is used to reduce dissipation whilst still sourcing sufficient IC supply current. Capacitor C6 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller.

4.5 Output Rectification

The transformer's secondary output is rectified by D6 and filtered by C9 and C10. The output capacitor is selected to provide <5% output voltage peak-to-peak ripple for a 24 V, 500 mA load. Resistor R9 enables accurate regulation and stability preventing flicker. Resistor R10 is a pre-load needed for voltage regulation during a no-load condition.

4.6 Regulation

The LYTSwitch-2 device regulates the output using ON/OFF control for CV regulation and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The 1% feedback resistors (R6//R11 and R7) were selected using standard values to center voltage regulation and set the output constant current range between 110% to 130% of the nominal value as overcurrent protection.

Resistor R8 provides filtering of the feedback signals which keeps the output voltage stable at no-load. The value must be kept low to prevent output voltage creeping up.

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5 PCB Layout

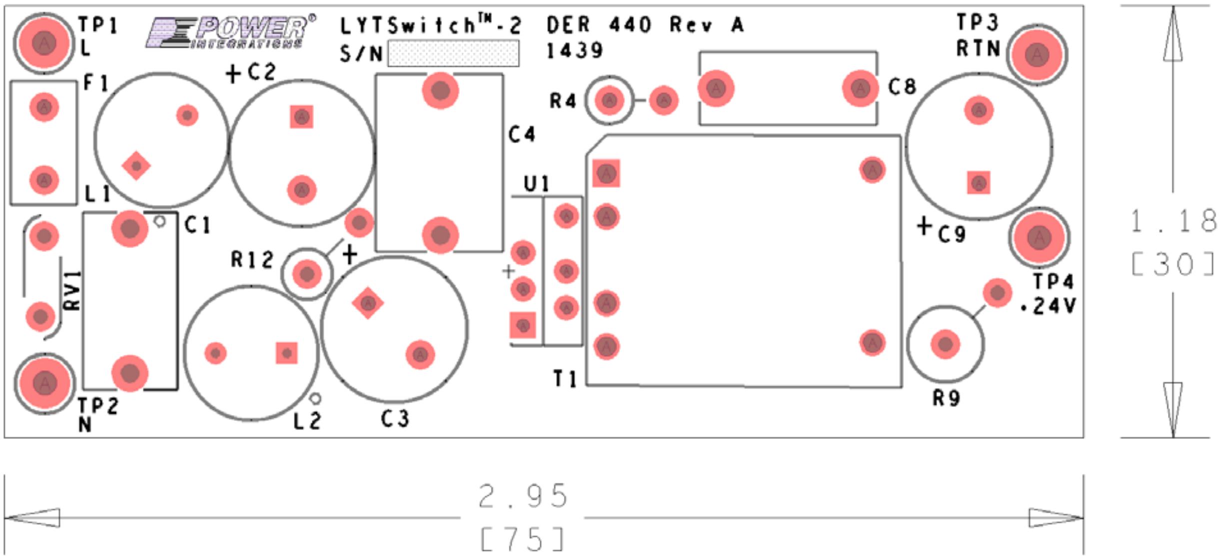

Figure 5 – Printed Circuit Board Layout, Top Side.

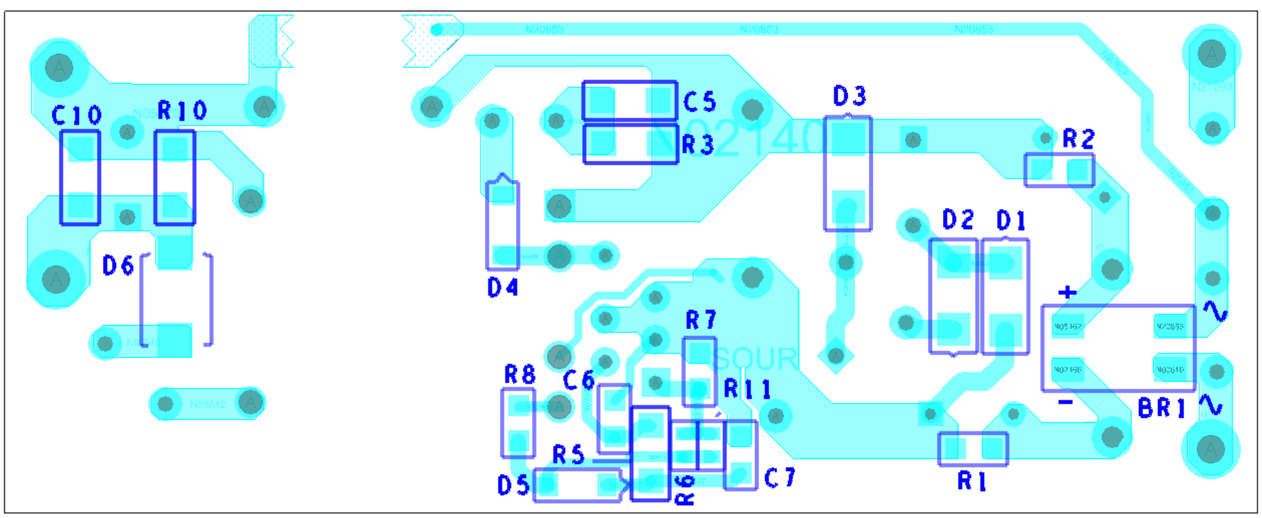

Figure 6 – Printed Circuit Board Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Tech
2	1	C1	100 nF, 305 VAC, Film, X2	B32921C3104M	Epcos
3	2	C2 C3	27 μF, 200 V, Electrolytic, (10 x 16),	EKXJ201ELL270MJ16S	Nippon Chemi-Con
4	1	C4	470 nF, 450 V, METALPOLYPRO	ECW-F2W474JAQ	Panasonic
5	1	C5	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay
6	1	C6	1 μF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
7	1	C7	10 μF, 35 V, Ceramic, X5R, 0805	C2012X5R1V106K085AC	TDK
8	1	C8	1 nF, 500 VAC, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
9	1	C9	330 μF, 35 V, Electrolytic, Low ESR, 68 mΩ, (10 x 16)	ELXZ350ELL331MJ16S	Nippon Chemi-Con
10	1	C10	4.7 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB472	Yageo
11	3	D1 D2 D3	600 V, 1 A, Standard Recovery, SMA	S1J-13-F	Diodes, Inc.
12	1	D4	1K V, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
13	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-123	BAV21W-7-F	Diodes, Inc.
14	1	D6	200 V, 3 A, DIODE SCHOTTKY 1A 200V, SMB	SK3200B-LTP	Micro Commercial
15	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
16	2	L1 L2	1.5 mH, 0.250 A, 10%	RL-5480HC-3-1500	Renco
17	2	R1 R2	4.75 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4751V	Panasonic
18	1	R3	220 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ224V	Panasonic
19	1	R4	300 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-300R	Yageo
20	1	R5	24.9 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2492V	Panasonic
21	1	R6	909 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9093V	Panasonic
22	1	R7	9.76 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9761V	Panasonic
23	1	R8	2.2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
24	1	R9	0.30 Ω, 1%, 1 W	2306 327 53007	Phoenix
25	1	R10	100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
26	1	R11	110 Ωk, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1103V	Panasonic
27	1	R12	10 R, 5%, 1 W, Metal Oxide	RSF100JB-10R	Yageo
28	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
29	1	T1	Bobbin, EPC1716D, Horizontal,7 pins (5primary,2secondary) Transformer	EPC1716D SNX-R1777-X1	SunTech Santronics
30	1	TP1, L	WIRE, AWG#24 3inch, BLUE	C2003L-100-ND	Gen Cable
31	1	TP2, N	WIRE, AWG#24 3inch, WHITE	C2003W-100-ND	Gen Cable
32	1	TP3, RTN	WIRE, AWG#24 3inch, BLACK	C2003B-100-ND	Gen Cable
33	1	TP4, +24V	WIRE, AWG#24 3inch, RED	C2003R-100-ND	Gen Cable
34	1	U1	LYTSwitch-2, CV/CC, eSIP	LYT2005E	Power Integrations

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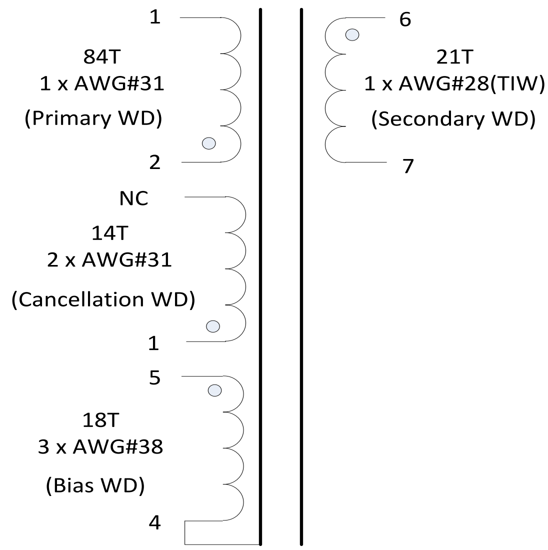
7 Transformer Specification

7.1 Electrical Diagram



(Core is grounded through pin 4. Dot signifies phase orientation, not mechanical winding start)

Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 4, 5 to 6, 7.	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1.10 mH ±7%
Primary Leakage Inductance	Pins 1-2, all other windings shorted, measured at 100 kHz, 0.4 V_{RMS}.	40 μH max

7.3 Material List

Item	Description
[1]	Core: EPC1716D.
[2]	Bobbin: EPC1716D Horizontal, 7 pins. SunTech P/N: EPC1716D. (PI P/N: 25-01026-00).
[3]	Magnet wire: #31 AWG - Double coated.
[4]	Magnet wire: #38 AWG - Double coated.
[5]	Triple Insulated: #28 AWG (0.32 mm).
[6]	Tape: 3M 1298 Polyester Film, 8.2 mm wide, 2.0 mils thick, or equivalent.
[7]	Tape: 3M 1298 Polyester Film, 6.0 mm wide, 2.0 mils thick, or equivalent.
[8]	Non-insulated wire: #31 AWG.
[9]	Copper Tape: 3M 6 mm wide, or equivalent
[10]	Varnish: Dolph BC-359 or equivalent.

7.4 Transformer Build Diagram

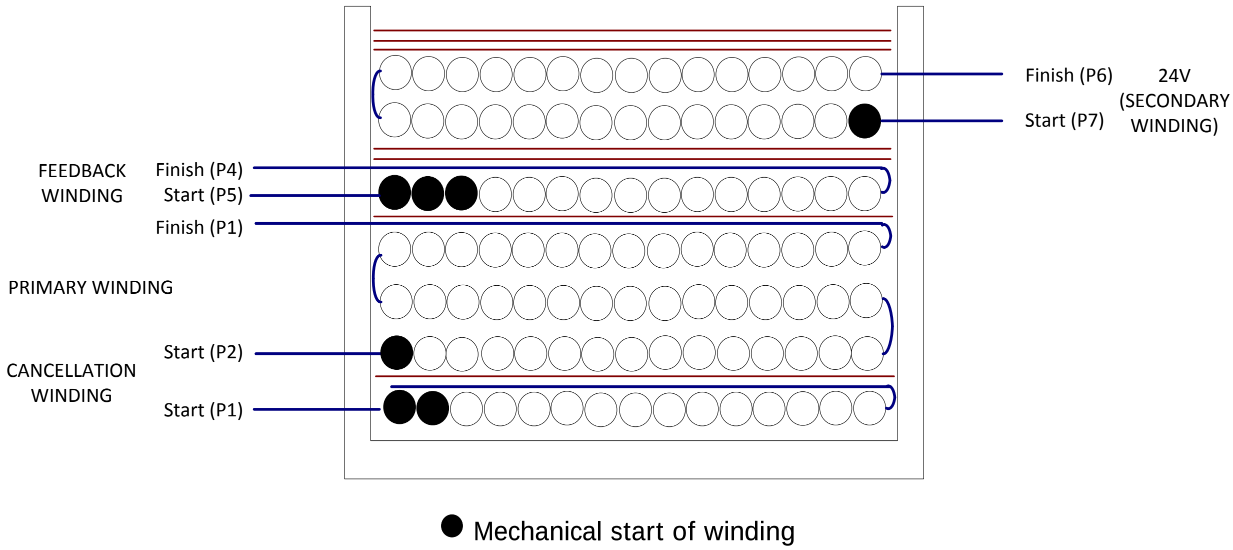


Figure 8 – Transformer Build Diagram.

7.5 Winding Construction

Winding Preparation	Item [1]. Remove pin 3. Place the bobbin on the mandrel with pins 1-4 on the right side. Winding direction is clockwise.
WD1 Cancellation	Item [3]. 2 x AWG #31. Start at pin 1, wind 14T covering bobbin width. End of winding floating. Insulate with 1layer of tape item [6]. See details in section 7.6 winding illustration.
WD2 Primary	Item [3]: Start at pin 2, wind 84T of wire in 3 layers and finish at pin 1. Insulate with 1layer of tape item [6].
WD3 Bias	Item [4]. 3 x AWG #38. Start 18T at pin 5 and finish at pin 4. Insulate with 1layer of tape item [6]. See details in section 7.6 winding illustration.
WD4 Secondary	Bobbin inverted, pin 6-7 on the right side. Item [5]. Start 21T at pin 7 and finish at pin 6. Distribute equally second layer of winding throughout the bobbin width. Insulate with 2layers of tape item [6]. See details in section 7.6 winding illustration.
Core	Grind core item [1] halves to get 1.10mH inductance. Cut 80mm of item [8], terminate to pin 4 and loop around the core. Fix the core and wire with 3layers of tape item [7]. See details in section 7.6 winding illustration.
Belly Band	Insulate 65mm of item [9]. Loop around the transformer connecting both ends. Secure the belly band with 2 layers of tape item [6]. See details in section 7.6 winding illustration.
Finish	Vanish with item [10].

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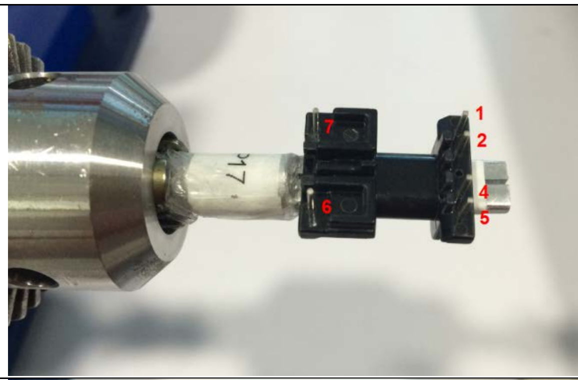
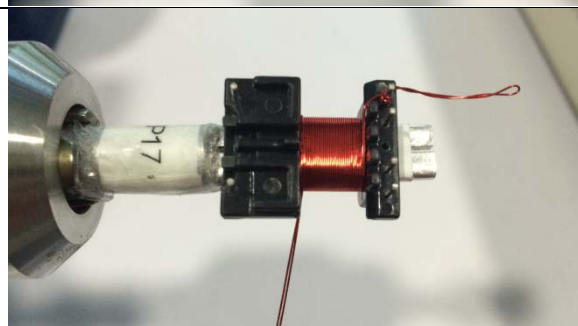
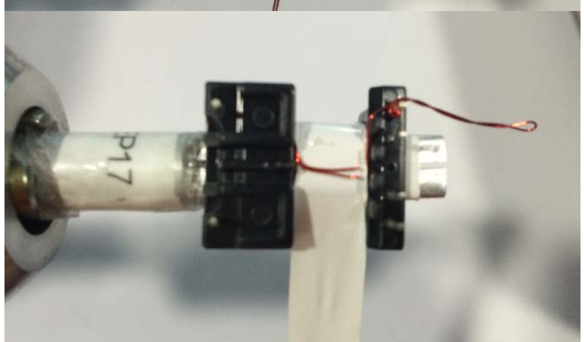
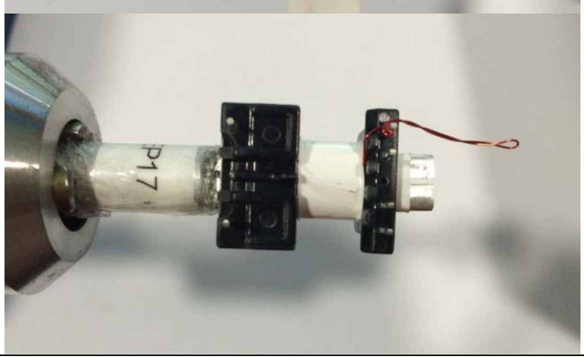
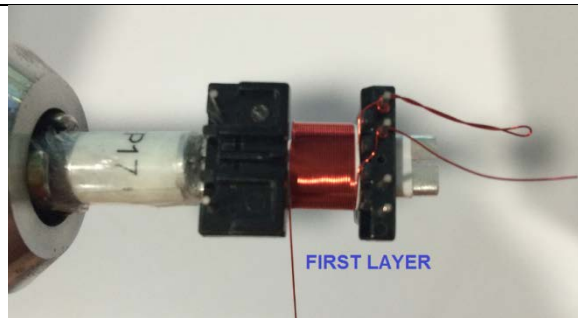
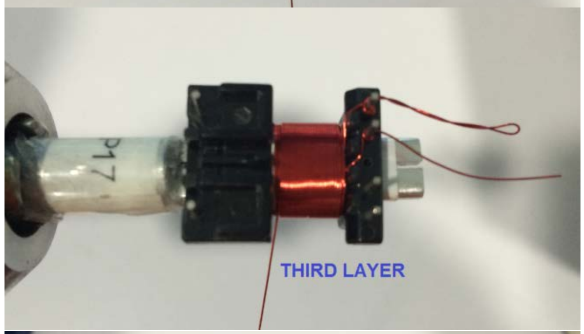
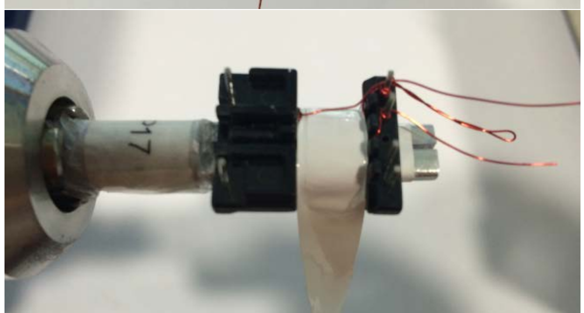
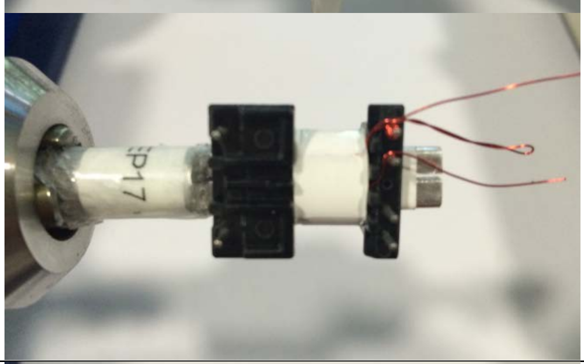
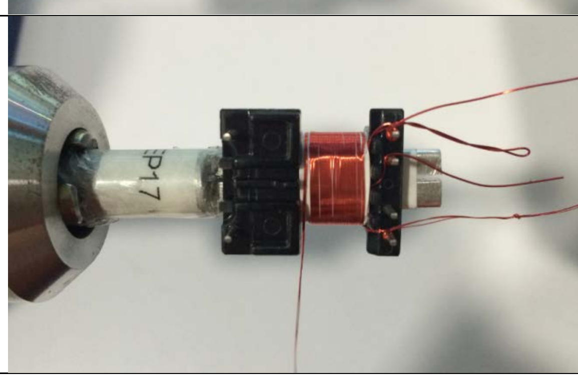
7.6 Winding Illustration

Winding Preparation		Place the bobbin item [2] on the mandrel with pins 1-5 on right side. Pull pin 3. Winding direction is clockwise.
WD1 Cancellation Winding	  	Start at pin 1, wind 14 turns of wire item [3], 2 x #31 AWG. In single layer covering the bobbin width. See pictures for sequential winding procedures.

<table>
<tr>
<td>WD2
Primary
Winding</td>
<td>






</td>
<td>Start at pin 2, wind 84 turns of wire item [3], 1 x #31 AWG in 3 layers and finish at pin 1. Put tape item [6] to secure the primary winding and to cover the crossing of winding from left to right for termination. See pictures for sequential winding procedure.</td>
</tr>
<tr>
<td>WD3
Bias
Winding</td>
<td>

</td>
<td>Item [4], 18 turns of 3 x #38 AWG. Start at pin 5, evenly spread winding and finish at pin 4 crossing from left to right. Insulate one layer of tape.</td>
</tr>
</table>

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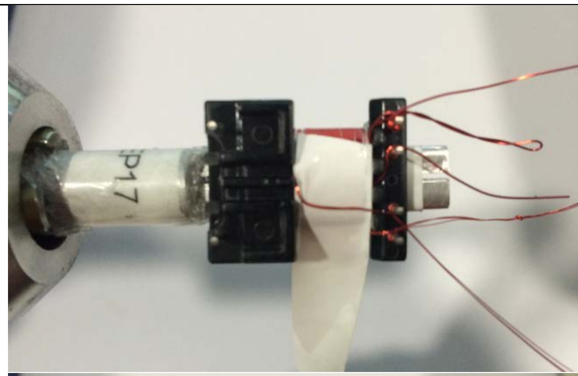
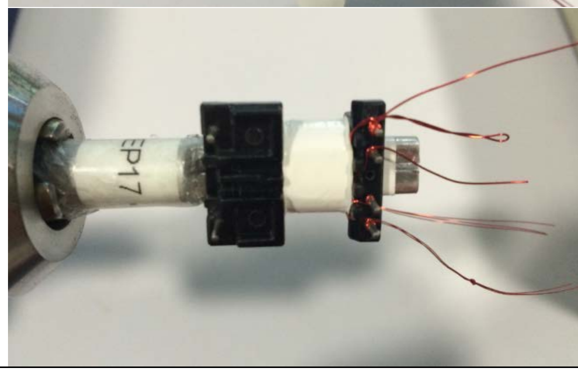
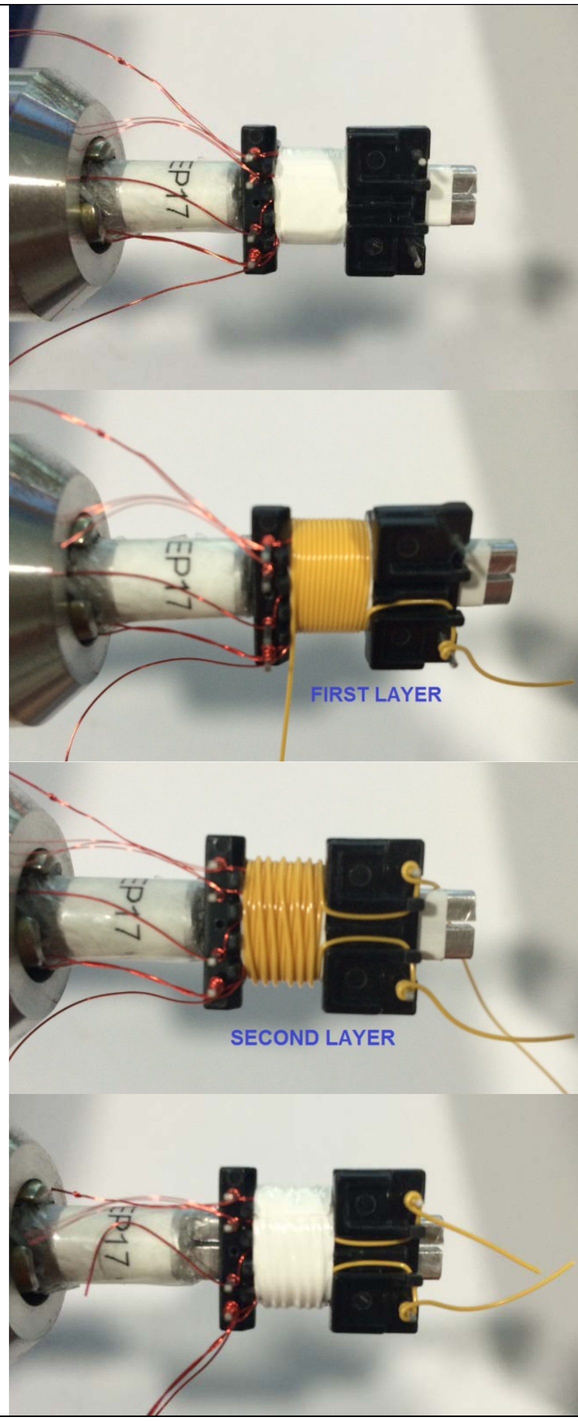

EP17


EP17

WD4 Secondary Winding		Invert bobbin orientation. Using 1 x #28 AWG (TIW) item [5], start at pin 7 and finish at pin 6 with 21T. Fill full width with first layer and evenly distribute the second layer. Insulate with two layers of tape.

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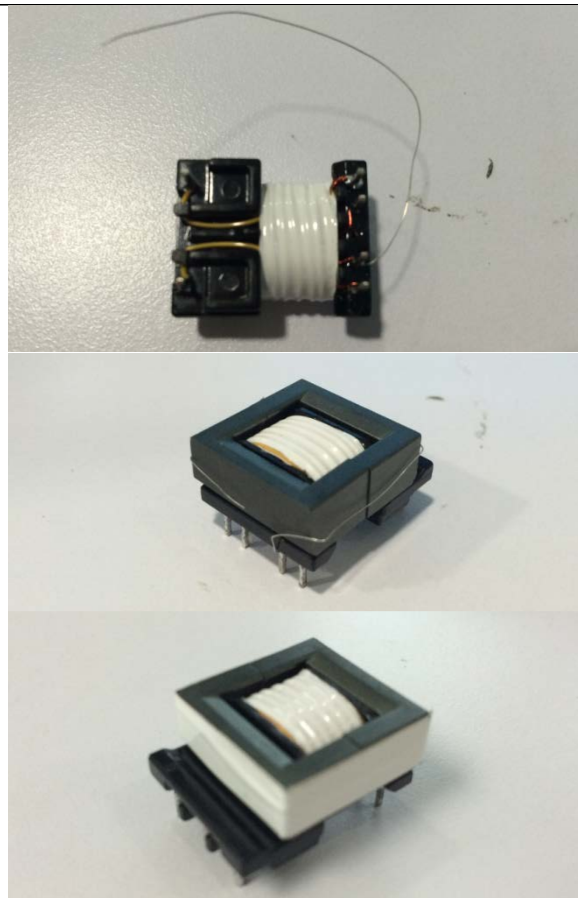
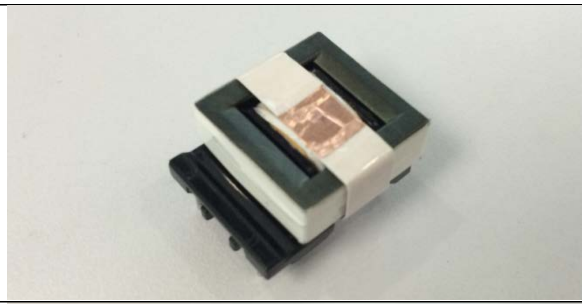
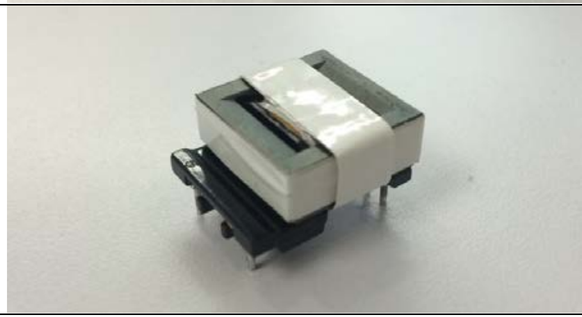
Core Grounding		Properly terminate and solder windings to its pin. Grind the core to meet 1.10 mH primary inductance. Terminate to pin 4 80 mm of item [8] then loop around the core. Secure the core and insulated wire around it with 3 layers of tape item [7]. See pictures for sequential procedure.
Belly Band		Prepare 65 mm of belly band item [9] as shown. Loop around the transformer and secure with 2 layers of tape item [6].

		
Finish		Varnish with item [10].

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8 Transformer Design Spreadsheet

ACDC_LYTSwitch-2_081114; Rev.2.1; Copyright Power Integrations 2014	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**ACDC_LYTSwitch-2_080814_Rev2-1; Discontinuous Flyback Transformer Design Spreadsheet**
ENTER APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC Input Voltage
fL	50		50	Hz	AC Mains Frequency
Application Type	Ballast-CC		Ballast-CC		Choose application type
VO	24.00		24.00	V	Output Voltage. This value is recommended to be 10% higher than the maximum LED Voltage
IO	0.55		0.55	A	Power Supply Output Current (corresponding to peak power)
Power		Info	13.20	W	!!! Continuous output power may be too high. Verify thermal performance
n	0.88		0.88		Efficiency Estimate at output terminals
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	27.00		27.00	uF	Input Capacitance
ENTER LYTSwitch-2 VARIABLES					
Chosen Device	LYT2005K/E		LYT2005K/E		Chosen LYTSwitch-2 device
ILIMITMIN			0.53	A	Minimum Current Limit
ILIMITTYP			0.58	A	Typical Current Limit
ILIMITMAX			0.62	A	Maximum Current Limit
FS	78.00	Info	78.00	kHz	Choose a frequency between 63.23kHz and 73.23kHz to achieve best output tolerance
VOR			98.00	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP		Warning	0.77		Kp is too low. Increase Cin, decrease DCON or use larger LYTSwitch-2 device, or use external bias supply
FEEDBACK WINDING PARAMETERS					
NFB	18.00		18.00		Feedback winding turns
VFLY			21.00	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			19.67	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
BIAS	Ext. bias		Ext. bias		Select between self bias or external bias to supply the IC.
VB			N/A	V	Feedback Winding Voltage (VFLY) is greater than 20 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.
NB	.		N/A		Bias Winding number of turns
REXT			4.60	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON	5.50	Warning	5.50	us	!!! Warning. Diode conduction time outside acceptable limits. 4.6us <= DCON <= 9 us
DCON_FINAL		Warning	5.49	us	Final output conduction diode, assuming integer values for NP and NS
TON			5.86	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		Info	92.80	k-ohm	Upper resistor in Feedback resistor divider.

					Once the initial prototype is running, it may be necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER			9.45	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	Custom		EPC1716D		Enter Transformer Core.
Custom_Core	EPC1716D				Enter Core name if selection on drop down menu is "Custom"
Bobbin					#N/A
AE	28.75		28.75	mm^2	Core Effective Cross Sectional Area
LE	36.85		36.85	mm	Core Effective Path Length
AL	2160.00		2160.00	nH/turn^2	Ungapped Core Effective Inductance
BW	8.00		8.00	mm	Bobbin Physical Winding Width
M	0.00		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3.00		Number of Primary Layers
NS			21.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			91.77	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX		Warning	0.58		!!! Warning. Maximum duty cycle exceeded. Increase Cin, VACMIN, or select larger LYTSwitch-2
IAVG			0.18	A	Input Average current
IP			0.53	A	Peak primary current
IR			0.53	A	Primary ripple current
IRMS			0.27	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1016.96	uH	Minimum Primary Inductance
LPTYP			1093.50	uH	Typical Primary inductance
LP_TOLERANCE	7.00		7.00	%	Tolerance in primary inductance
NP			84.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			154.97	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET			2600.00	Gauss	Target Flux Density
BM		Info	2603.57	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2600 is recommended
BP			3008.69	Gauss	!!! Warning. Peak Flux density exceeds 3100 Gauss and is not recommended. Reduce BP by increasing NS
BAC			1301.79	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			220.31		Relative Permeability of Ungapped Core
LG			0.23	mm	Gap Length (LG > 0.1 mm)
BWE			24.00	mm	Effective Bobbin Width
OD			0.29	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.23	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			80.63	Cmils	Bare conductor effective area in circular mils
CMA			295.09	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)

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TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			2.12	A	Peak Secondary Current
ISRMS			1.06	A	Secondary RMS Current
IRIPPLE			0.90	A	Output Capacitor RMS Ripple Current
CMS			211.55	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			26.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			600.57	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS			117.69	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL	98.12		98.12	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL	9.76		9.76	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)	23.90		23.90	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)	0.65		0.65	Amps	Measured Output current from first prototype
RUPPER_FINE			83.35	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 82.5 k-ohms
RLOWER_FINE			8.25	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 8.25 k-ohms

*** Power supply intentionally designed to operate on continuous conduction mode at low line and discontinuous conduction mode at high line so it can deliver full 12 W power at universal input.

9 Performance Data

All measurements were taken with the board configured as open frame in a 25 ºC ambient.

9.1 Efficiency

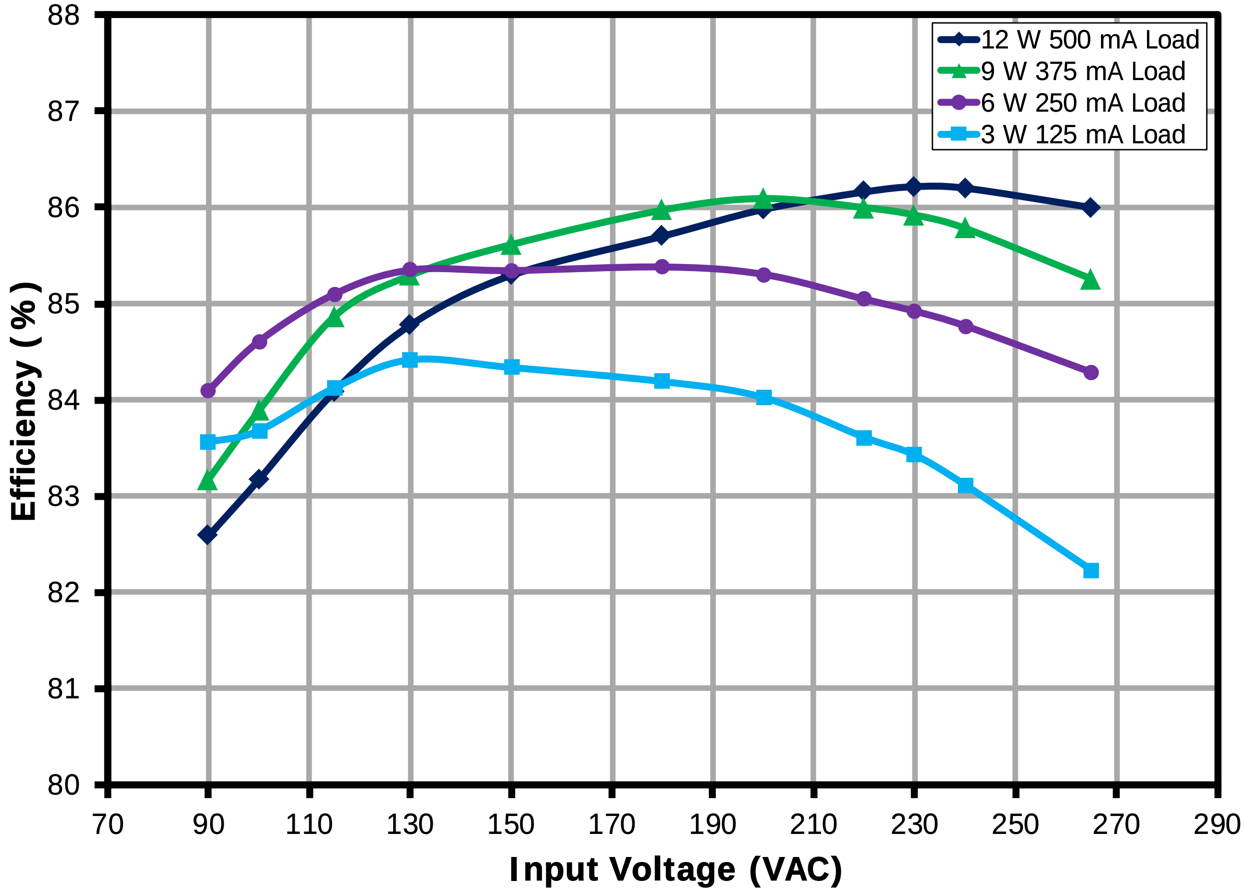

Figure 9 – Efficiency with Line and Load Variations.

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9.2 Average Efficiency

9.2.1 90 VAC

		Input Measurement					Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	500	89.84	185.45	14.59	0.875	44.48	24.10	499.81	12.05	82.58
75	375	89.87	143.21	10.93	0.849	48.81	24.26	374.72	9.09	83.17
50	250	89.90	97.60	7.20	0.820	53.28	24.21	249.97	6.05	84.10
25	125	89.92	52.31	3.60	0.766	58.27	24.07	124.99	3.01	83.56
							AVERAGE EFFICIENCY			83.35

9.2.2 115 VAC

		Input Measurement					Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	500	114.95	149.31	14.37	0.837	49.97	24.18	499.79	12.09	84.09
75	375	114.99	112.87	10.68	0.823	52.81	24.19	374.72	9.06	84.87
50	250	115.01	78.61	7.10	0.786	57.45	24.19	249.97	6.05	85.10
25	125	115.03	43.45	3.58	0.716	62.54	24.10	124.99	3.01	84.13
							AVERAGE EFFICIENCY			84.55

9.2.3 230 VAC

		Input Measurement					Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	500	229.96	82.08	14.01	0.742	61.87	24.17	499.70	12.08	86.22
75	375	230.00	65.40	10.53	0.700	64.17	24.16	374.65	9.05	85.92
50	250	230.01	46.42	7.11	0.666	64.82	24.15	249.97	6.04	84.92
25	125	230.01	26.91	3.62	0.584	65.20	24.13	124.99	3.02	83.43
							AVERAGE EFFICIENCY			85.12

9.2.4 265 VAC

		Input Measurement					Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	500	265.00	75.04	14.04	0.706	64.42	24.16	499.69	12.08	86.00
75	375	265.04	59.58	10.62	0.672	65.67	24.16	374.64	9.05	85.26
50	250	265.05	41.72	7.16	0.647	64.18	24.14	249.95	6.03	84.29
25	125	265.06	24.73	3.66	0.559	70.87	24.10	125.00	3.01	82.23
							AVERAGE EFFICIENCY			84.44

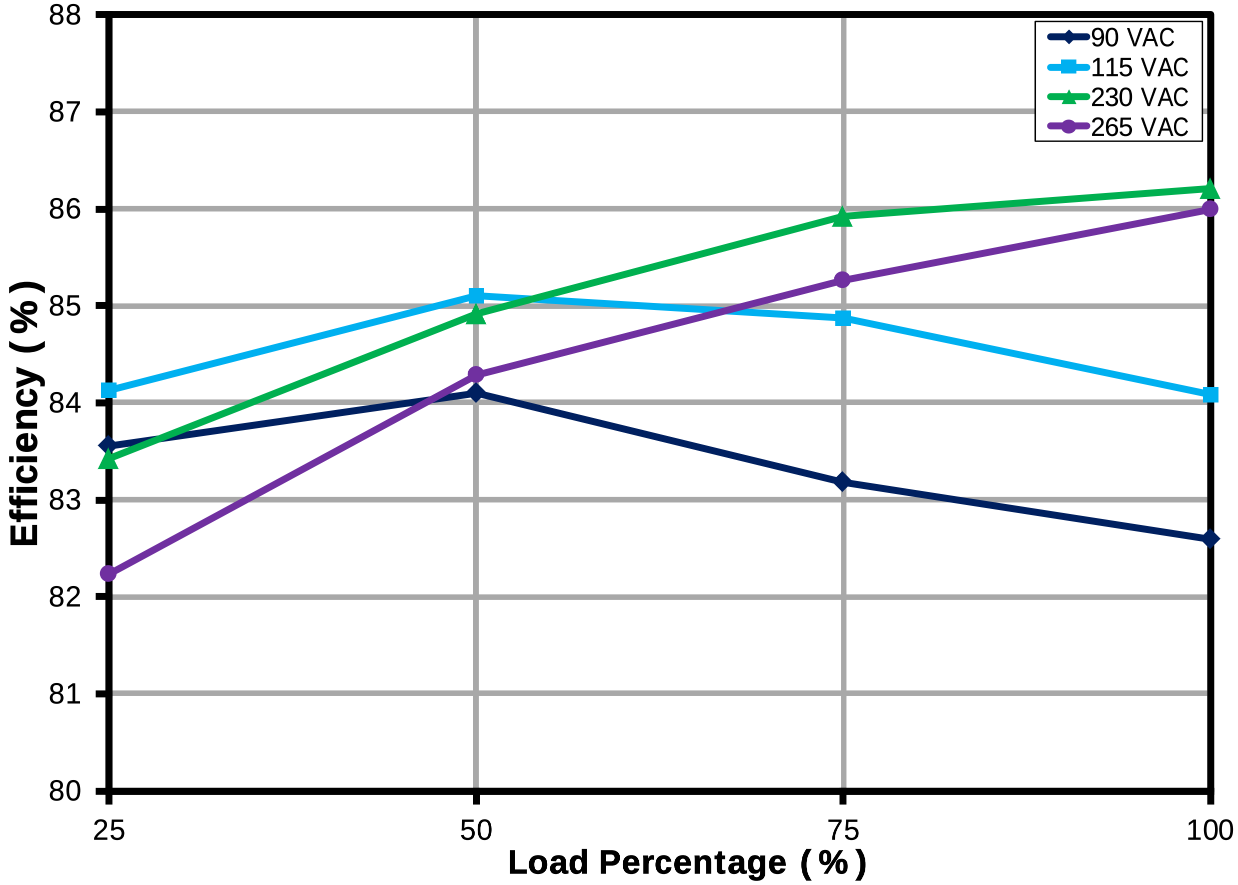

Figure 10 – Average Efficiency Graph.

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9.3 Line and Load Regulation

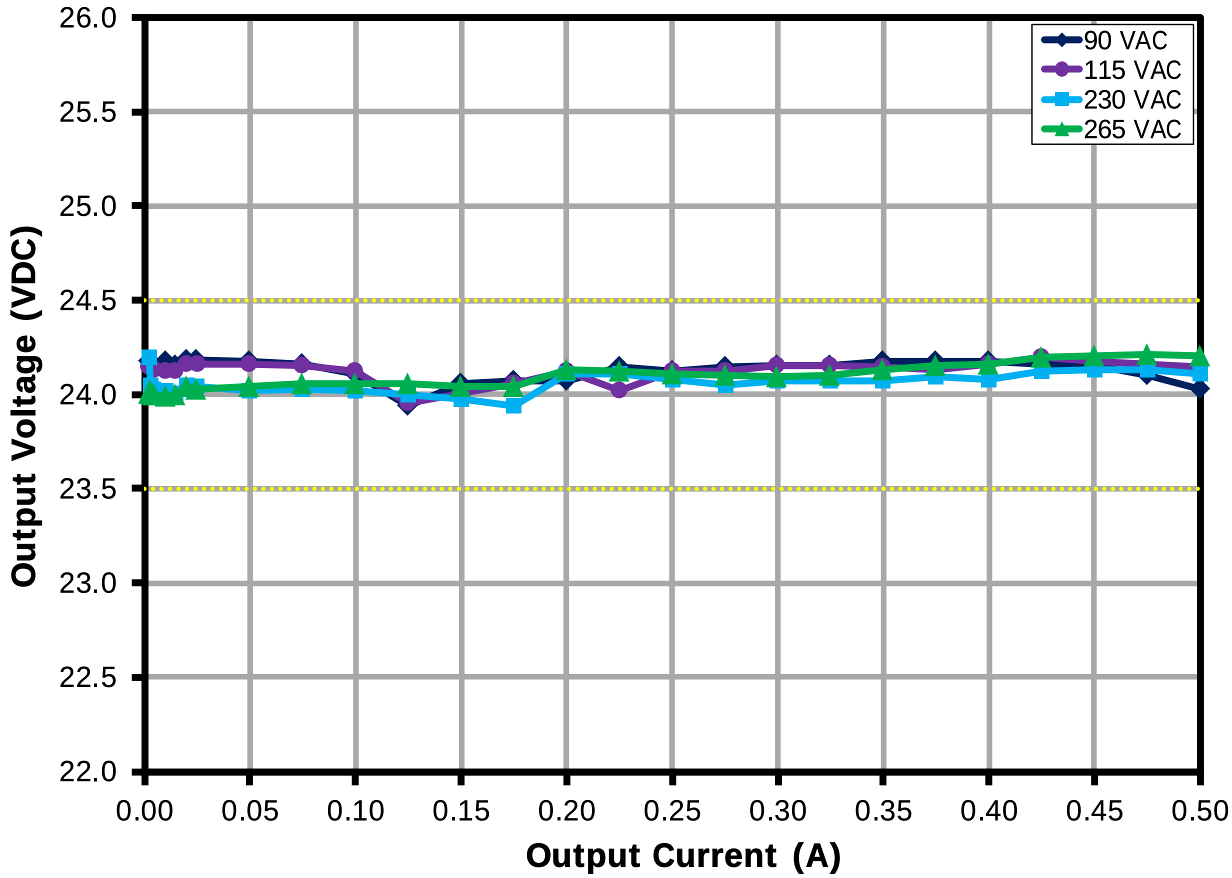

Figure 11 – Regulation vs. Line and Load.

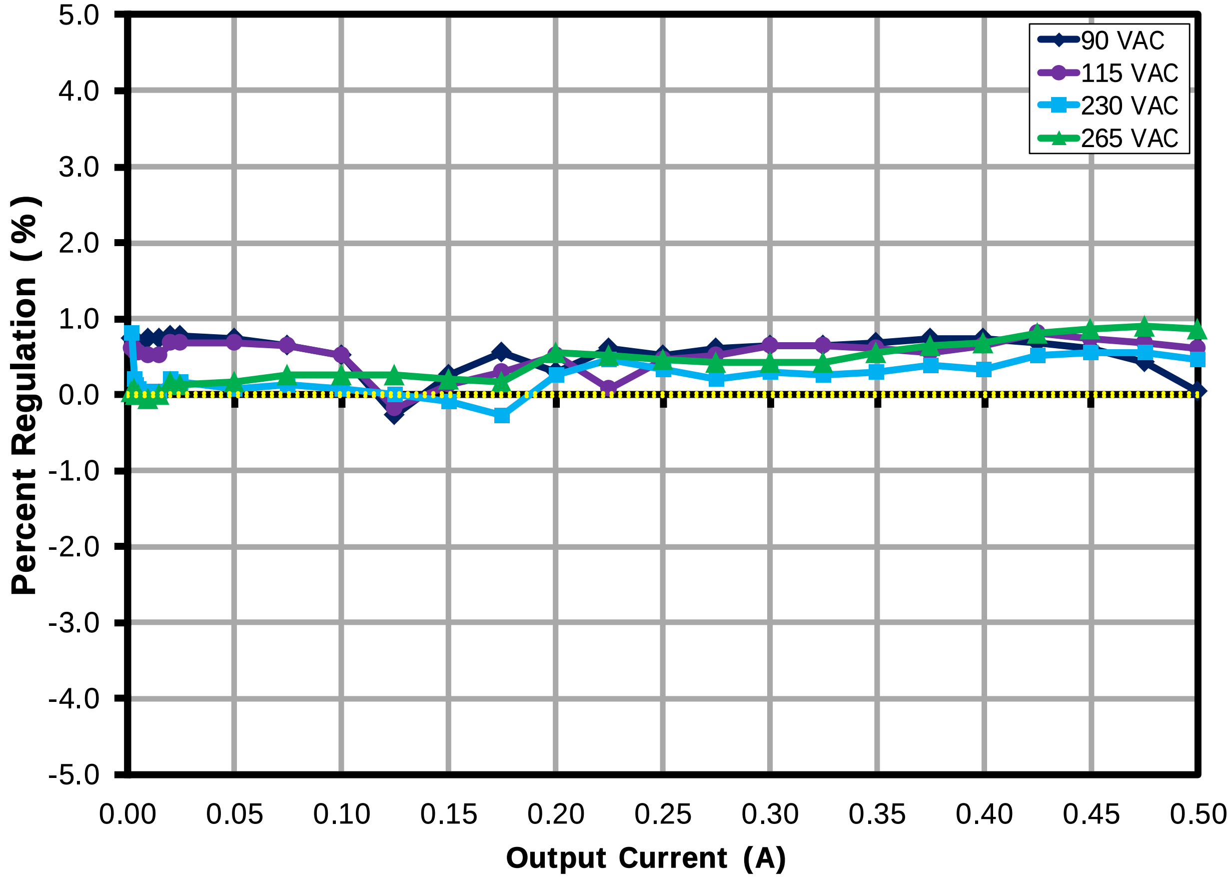

Figure 12 – % Regulation vs. Line and Load.

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9.4 Overcurrent Protection Limits

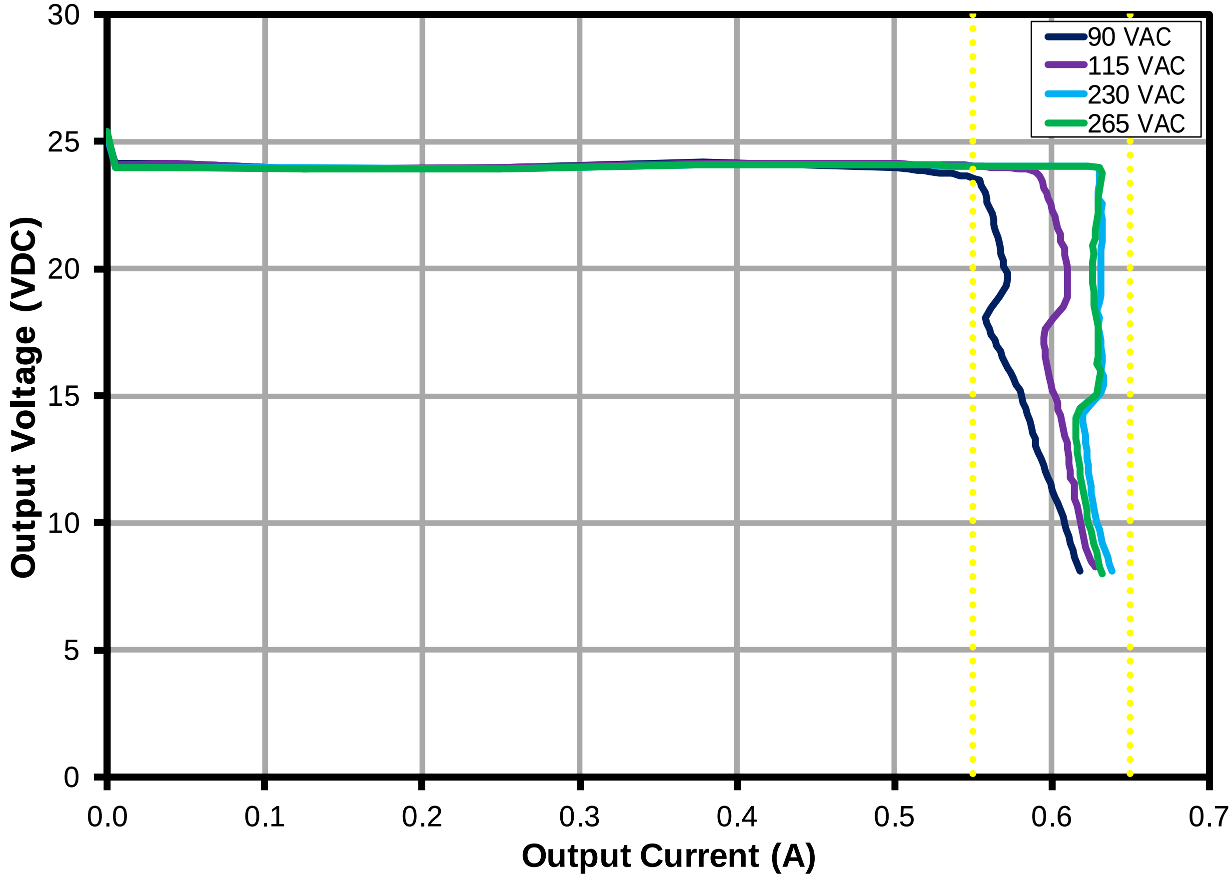

Figure 13 – OCP Limits.

9.5 No-Load Input Power

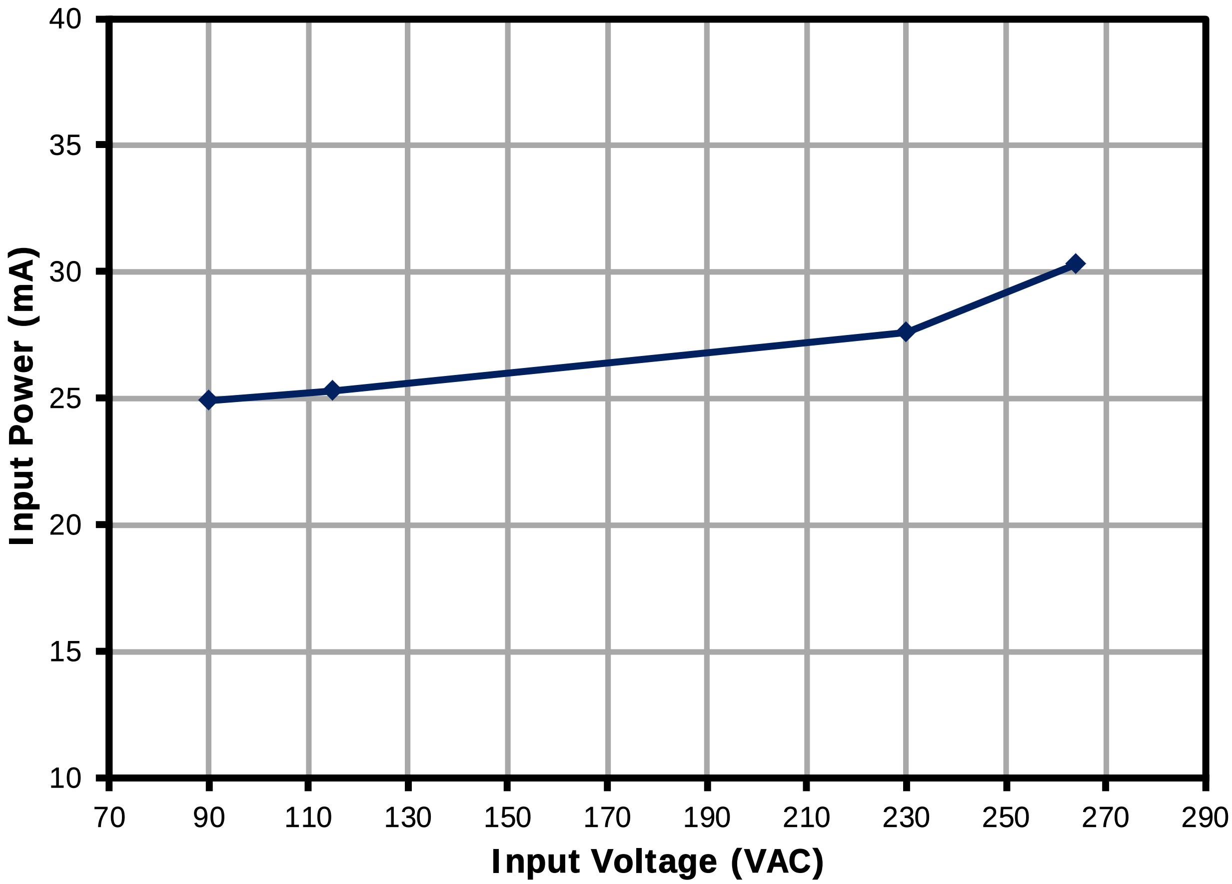

Figure 14 – No-Load Input Power.

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9.6 Power Factor

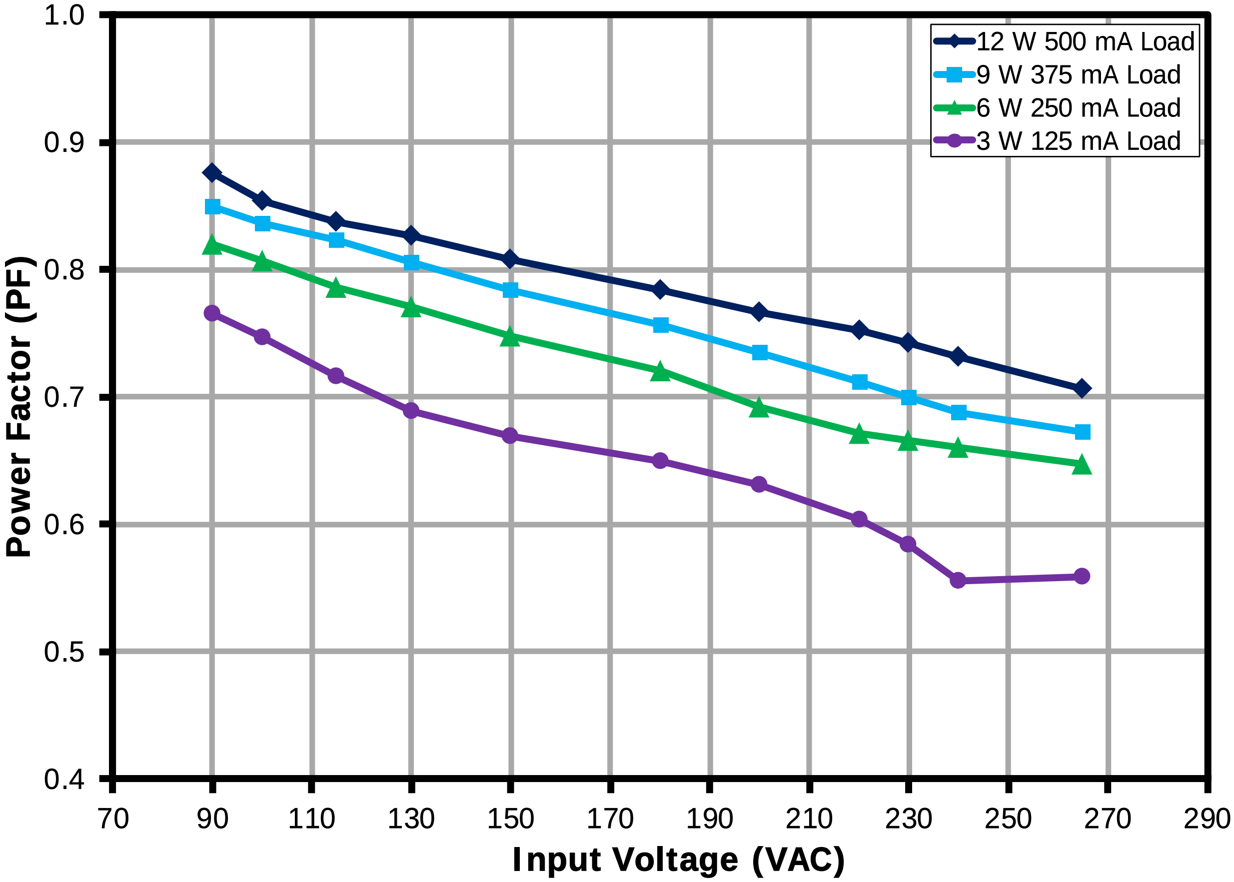

Figure 15 – Power Factor.

10 Thermal Performance

Images captured after running for >30 minutes in an enclosed compartment (~30 °C ambient).

Figure 16 – 90 VAC, Thermal, Top Side.
SPOT1 (U1): 89.0 °C.
SPOT2 (T1): 58.9 °C.

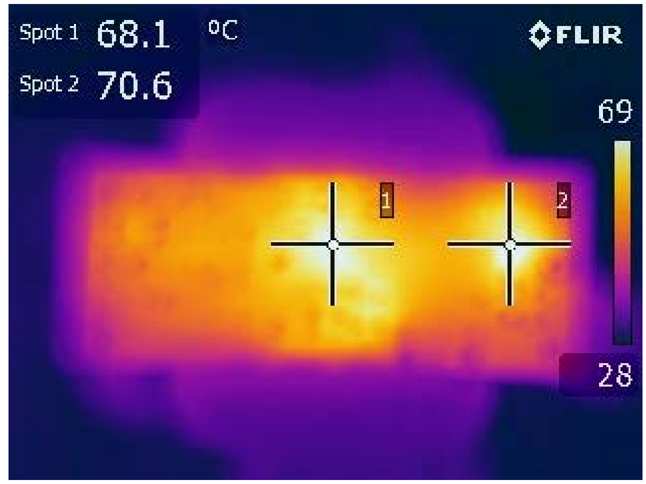

Figure 17 – 90 VAC, Thermal, Bottom Side.
SPOT1 (U1 PCB Bottom): 68.1 °C.
SPOT2 (D6): 70.6°C.

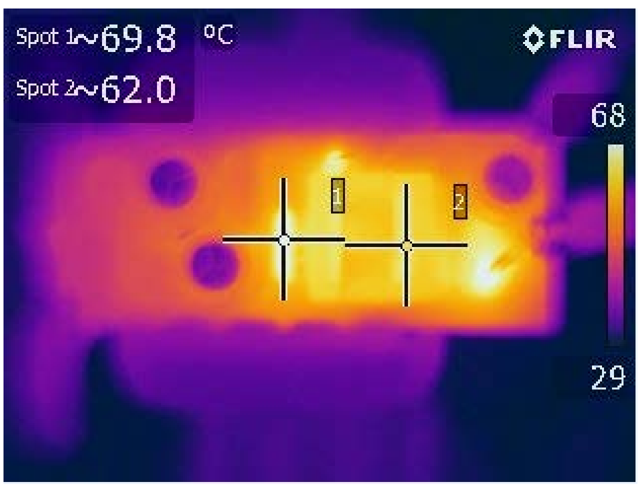

Figure 18 – 265 VAC, Thermal, Top Side.
SPOT1 (U1): 69.8 °C.
SPOT2 (T1): 62.0 °C.

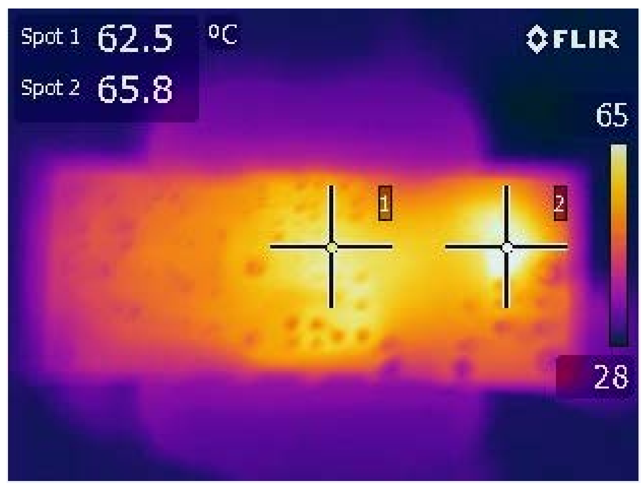

Figure 19 – 265 VAC, Thermal, Bottom Side.
SPOT1 (U1 PCB Bottom): 62.5 °C.
SPOT2 (D6): 65.8 °C.

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11 Waveforms

11.1 Input Voltage and Input Current Waveforms

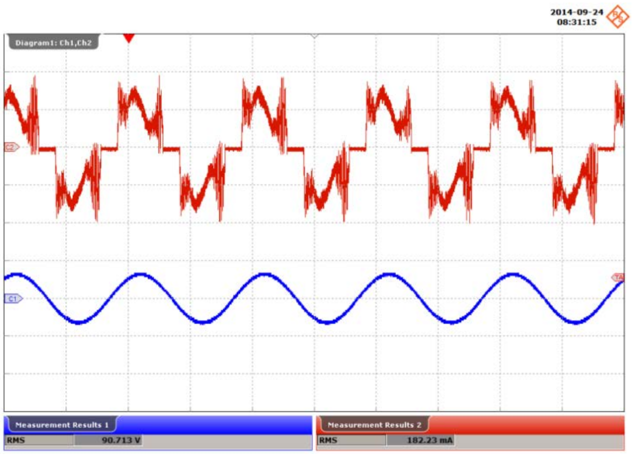

Figure 20 – 90 VAC, 50Hz Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

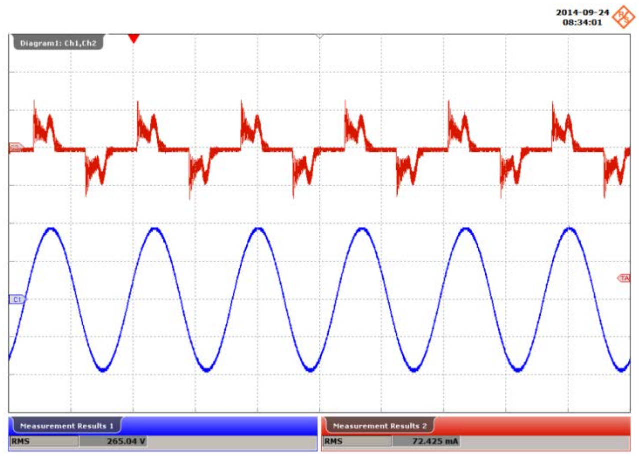

Figure 21 – 265 VAC, 60Hz Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

11.2 Output Current and Output Voltage at Normal Operation

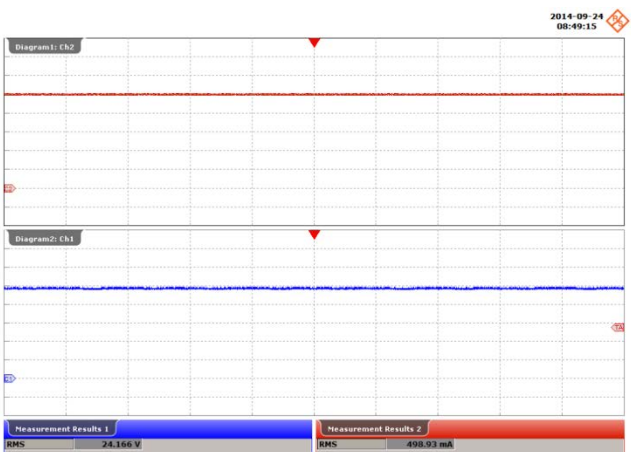

Figure 22 – 115 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 5 V, 10 ms / div.

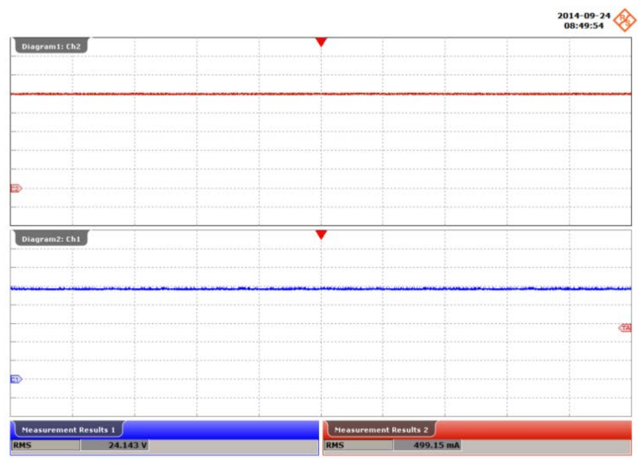

Figure 23 – 230 VAC, 60 Hz Full Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 5 V, 10 ms / div.

11.3 Output Voltage / Current Rise and Fall

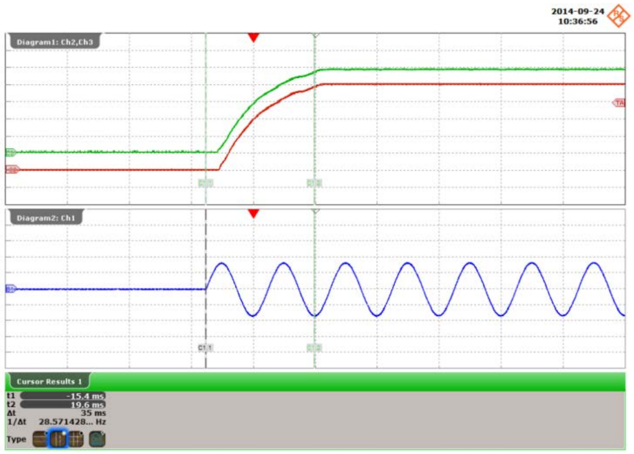

Figure 24 – 115 VAC, 50 Hz, Output Rise.
Upper: V_{OUT}, 5 V / div.
Middle: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
Start-up Time: 35 ms.

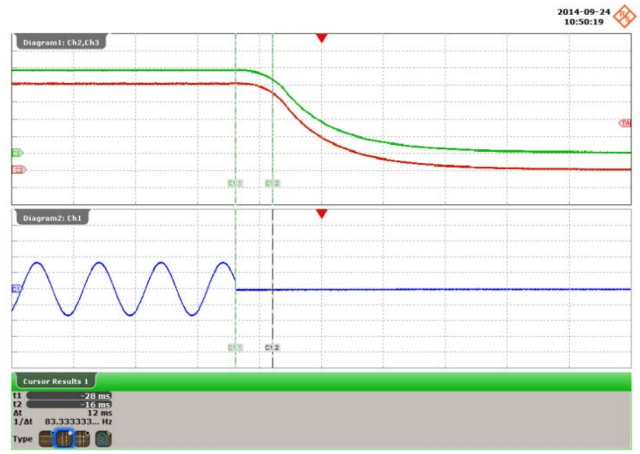

Figure 25 – 115 VAC, 50 Hz, Output Fall.
Upper: V_{OUT}, 5 V / div.
Middle: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
Hold-up Time: 12 ms.

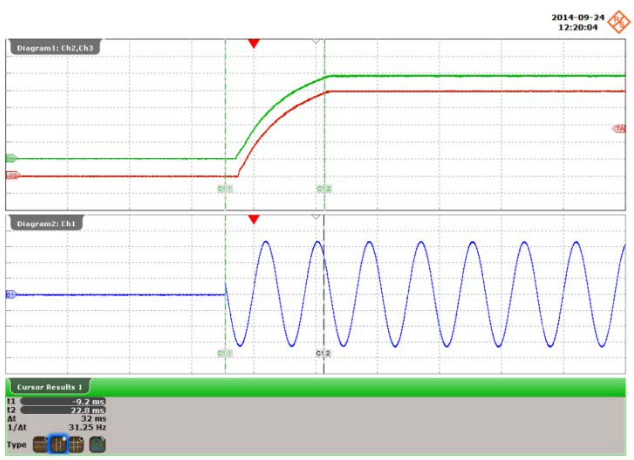

Figure 26 – 230 VAC, 60 Hz, Output Rise.
Upper: V_{OUT}, 5 V / div.
Middle: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
Start-up Time: 32 ms.

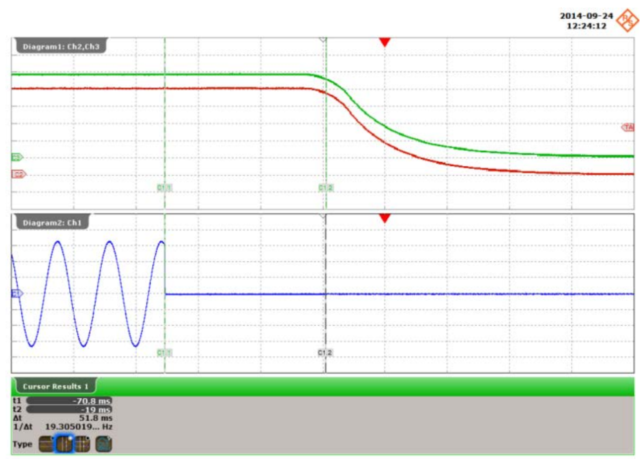

Figure 27 – 230 VAC, 60 Hz, Output Fall.
Upper: V_{OUT}, 5 V / div.
Middle: I_{OUT}, 100 mA / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
Hold-up Time: 51.8 ms.

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11.4 Output Voltage and Current Ripple

11.4.1 Load: 125 mA, 3 W, 25% Power

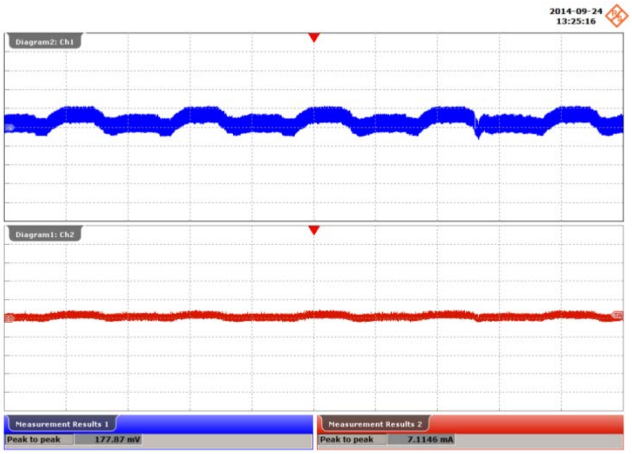

Figure 28 – 90 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

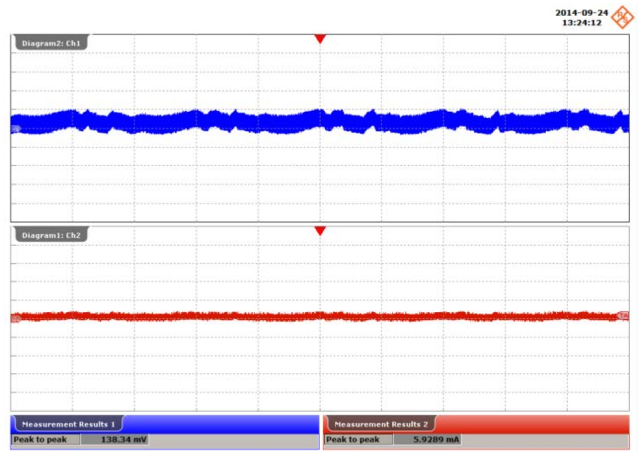

Figure 29 – 115 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

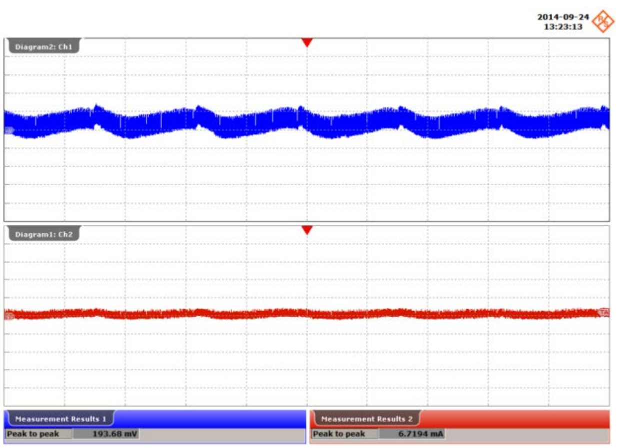

Figure 30 – 230 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

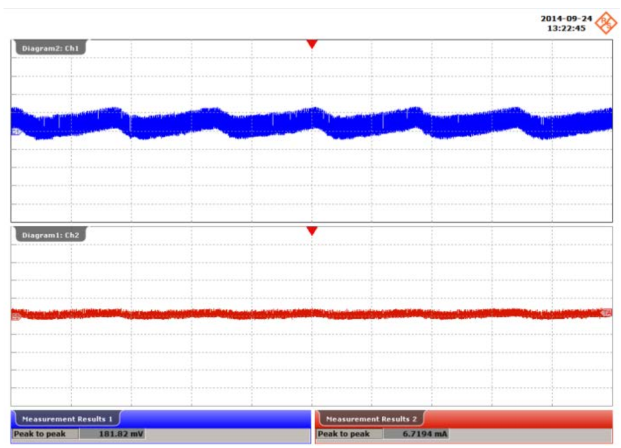

Figure 31 – 265 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

11.4.2 Load: 250 mA, 6 W, 50% Power

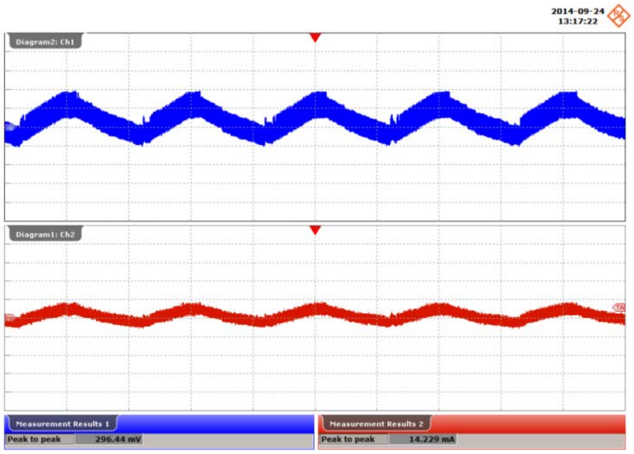

Figure 32 – 90 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

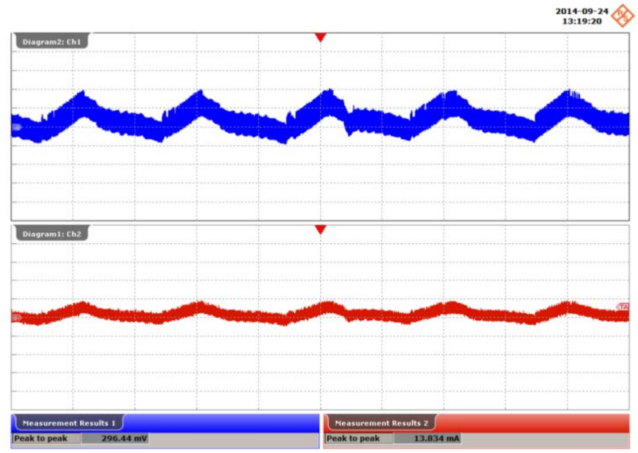

Figure 33 – 115 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

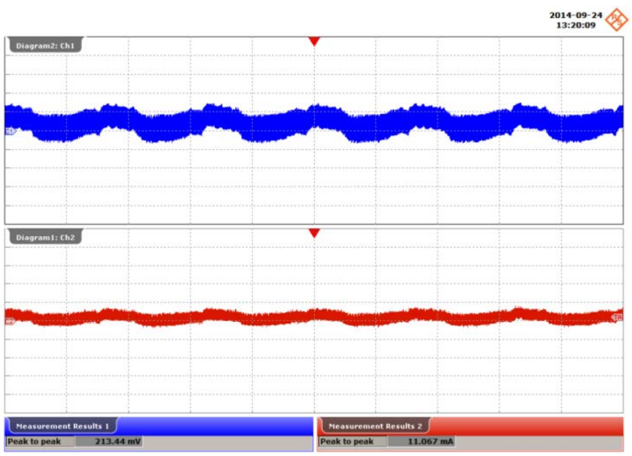

Figure 34 – 230 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

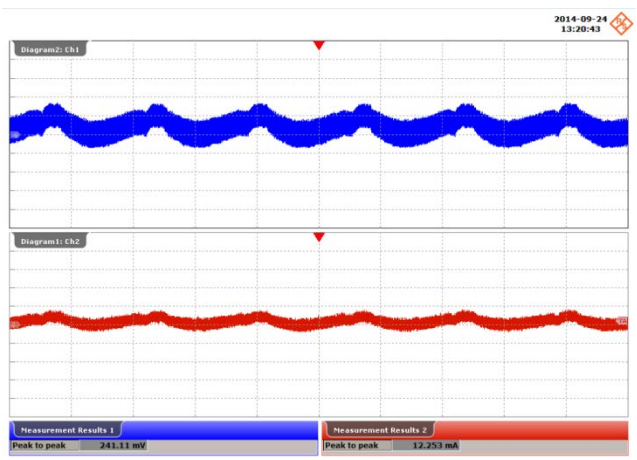

Figure 35 – 265 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

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11.4.3 Load: 375 mA, 9 W, 75% Power

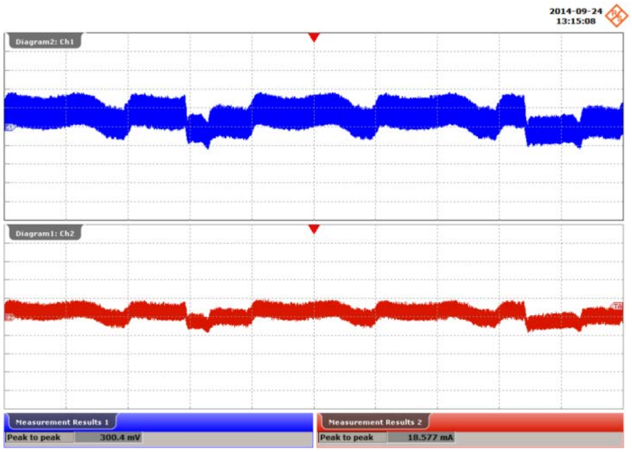

Figure 36 – 90 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

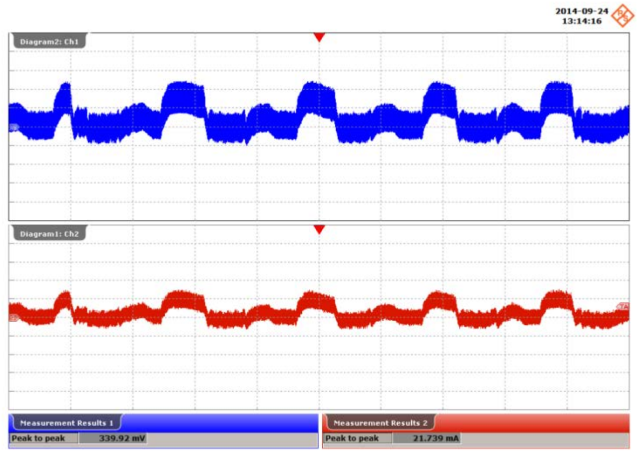

Figure 37 – 115 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

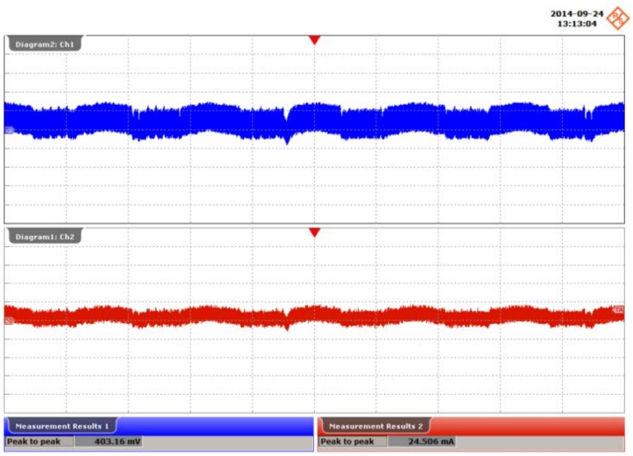

Figure 38 – 230 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

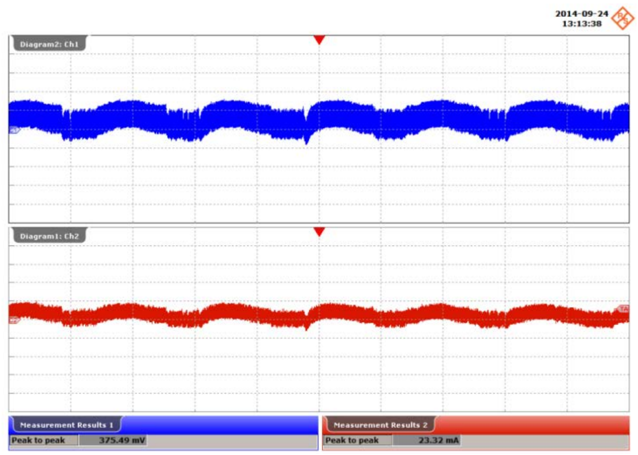

Figure 39 – 265 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

11.4.4 Load: 500 mA, 12 W, 100% Power

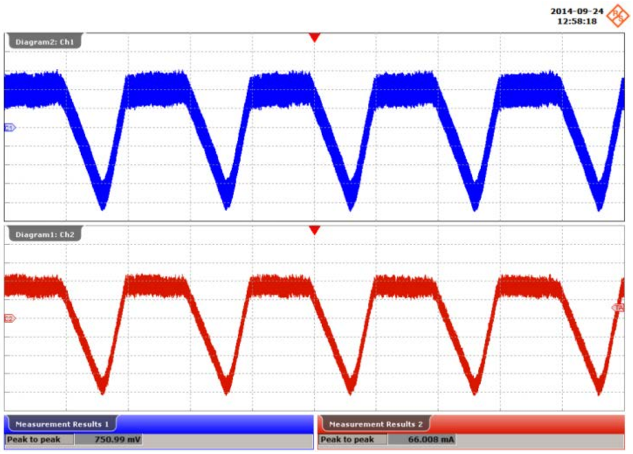

Figure 40 – 90 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

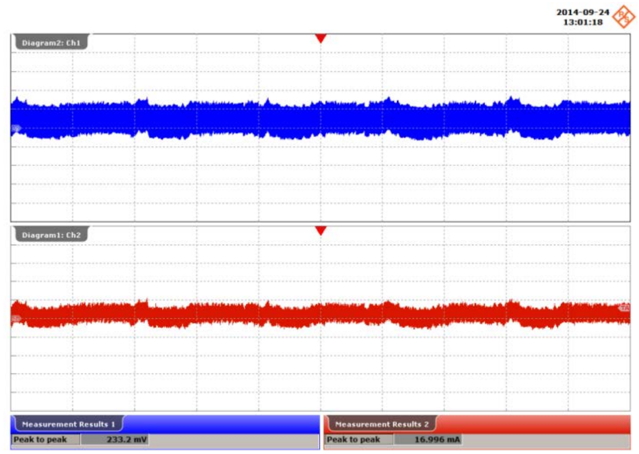

Figure 41 – 115 VAC, 50 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

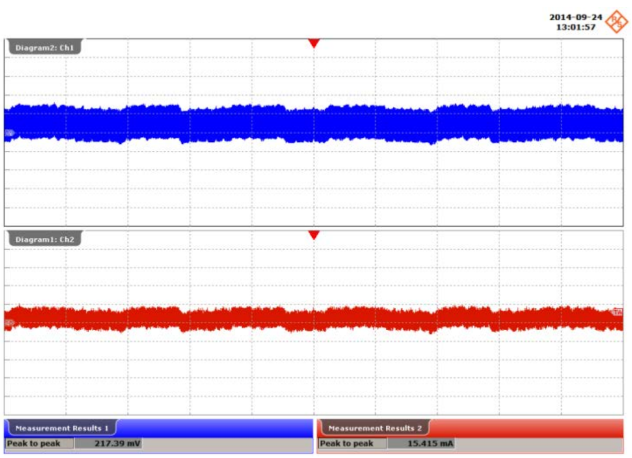

Figure 42 – 230 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

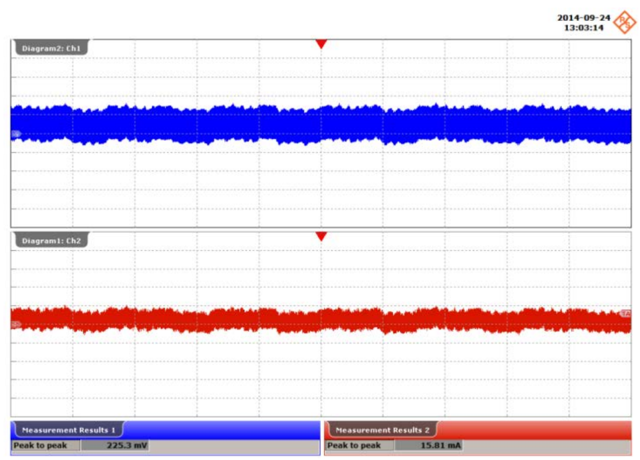

Figure 43 – 265 VAC, 60 Hz.
Upper: $V_{OUT(RIPPLE)}$, 100 mV / div.
Lower: $I_{OUT(RIPPLE)}$, 10 mA, 5 ms / div.

*** No flicker observed using 7 LED in series and resistor for varying load.
*** Possible flicker might occur when using 8 LED in series. Not enough headroom to conduct total LED Vf.

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11.5 Drain Voltage and Current at Normal Operation

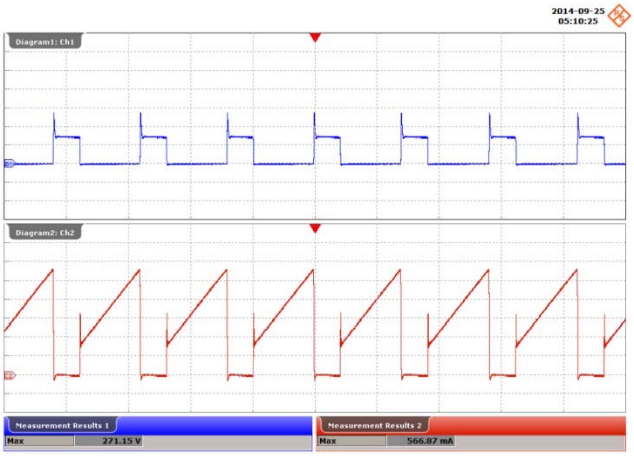

Figure 44 – 90 VAC, 50 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 10 µs / div.

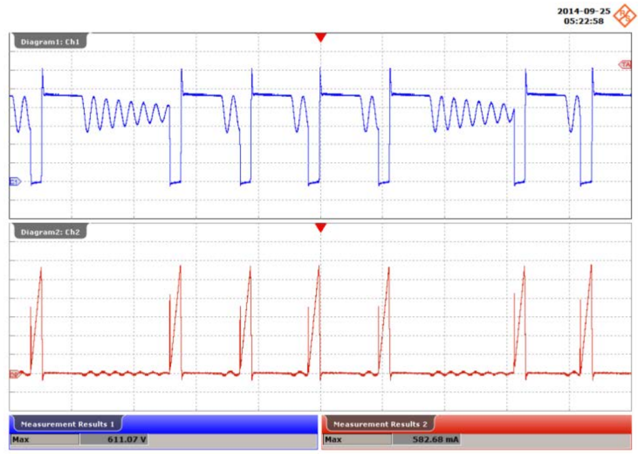

Figure 45 – 265 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 10 µs / div.

11.6 Start-up Drain Voltage and Current

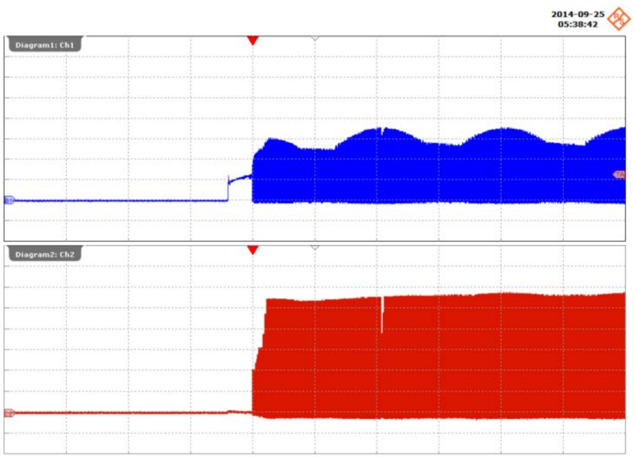

Figure 46 – 90 VAC, 50 Hz Start-up.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 5 ms / div.

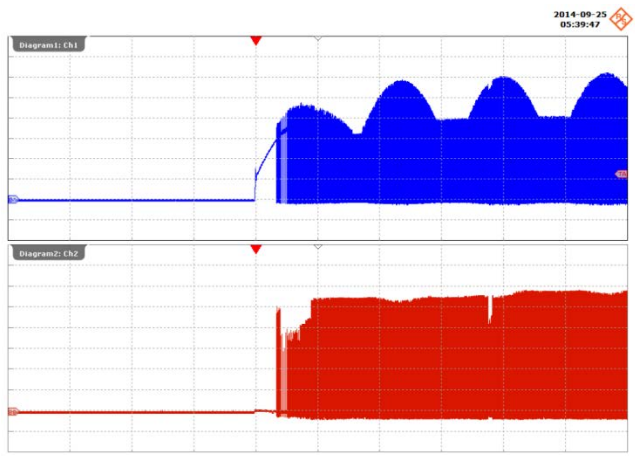

Figure 47 – 265 VAC, 60 Hz Start-up.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 5 ms / div.

11.7 Drain Current and Drain Voltage during Output Short Condition

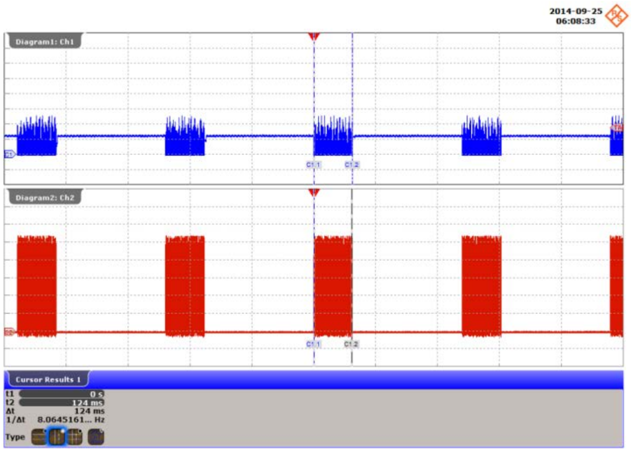

Figure 48 – 90 VAC, 50 Hz Output Short.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto Restart ON-Time: 124 ms.

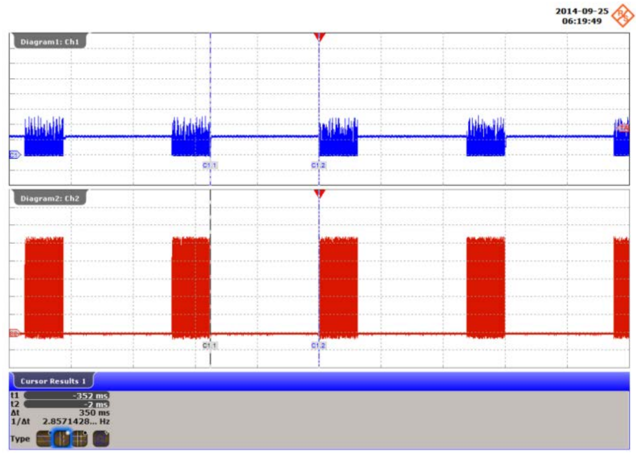

Figure 49 – 90 VAC, 50 Hz Output Short.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto Restart OFF-Time: 350 ms.

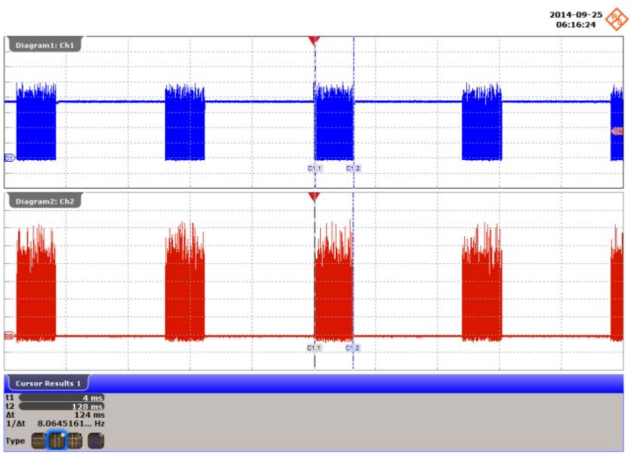

Figure 50 – 265 VAC, 60 Hz Output Short.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto Restart ON-Time: 124 ms.

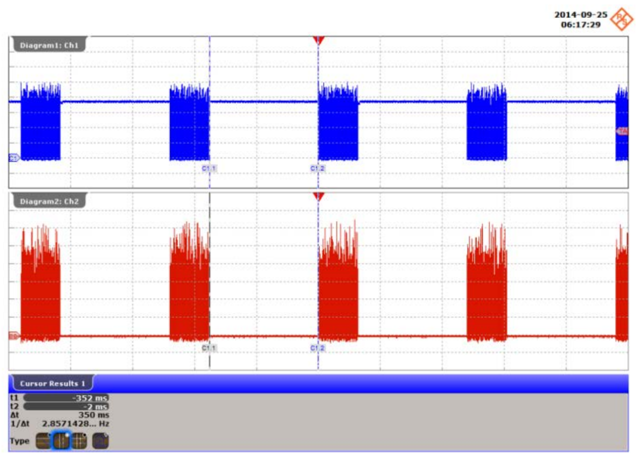

Figure 51 – 265 VAC, 60 Hz Output Short.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto Restart OFF-Time: 350 ms.

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11.8 Drain Current and Drain Voltage during Open-Loop Condition (R8 is Open)

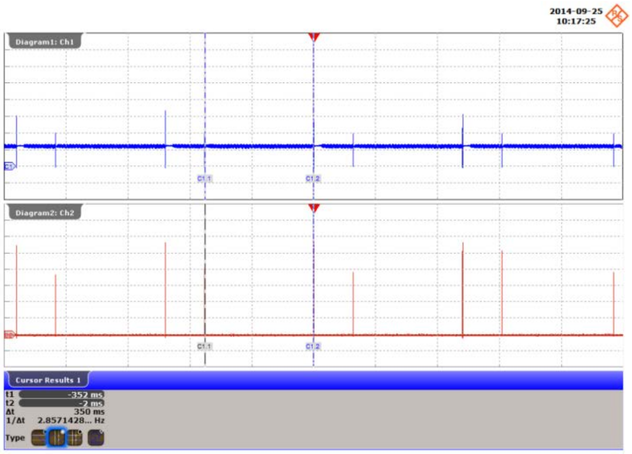

Figure 52 – 90 VAC, 50 Hz Open-loop Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto-Restart OFF-Time: 350 ms.

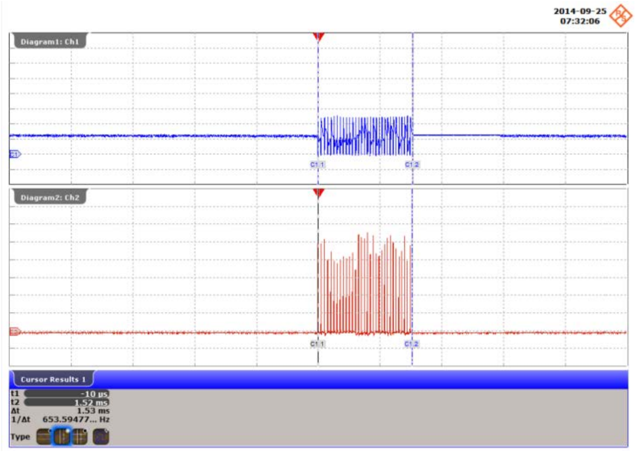

Figure 53 – 90 VAC, 50 Hz Open-loop Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 1 ms / div.
Auto-Restart ON-Time: 1.53 ms.

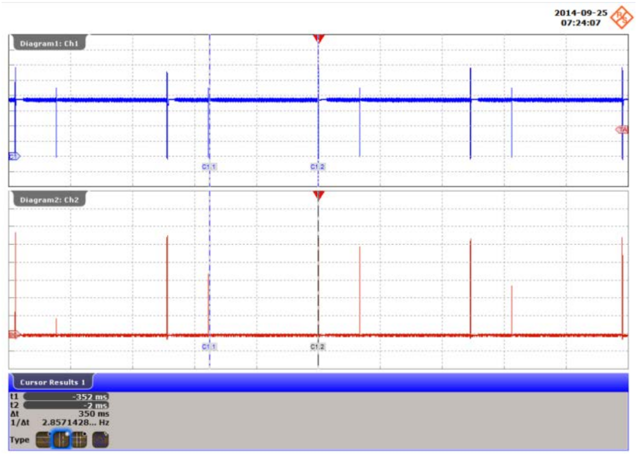

Figure 54 – 265 VAC, 60 Hz Open-loop Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 200 ms / div.
Auto-Restart OFF-Time: 350 ms.

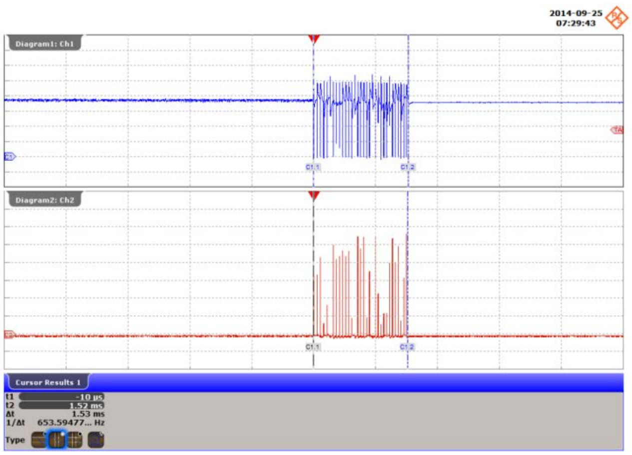

Figure 55 – 265 VAC, 60 Hz Open-loop Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 1 ms / div.
Auto-Restart ON-Time: 1.53 ms.

11.9 Output Diode Current and Voltage Waveforms Normal Operation

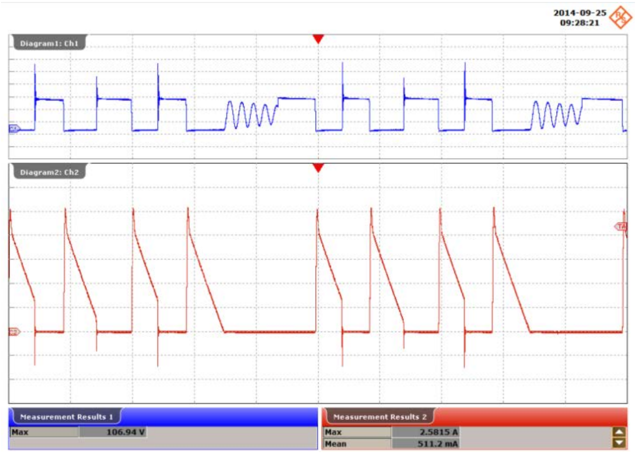

Figure 56 – 90 VAC, 50 Hz.
Upper: V_{D6}, 20 V / div.
Lower: I_{D6}, 500 mA, 10 μs / div.

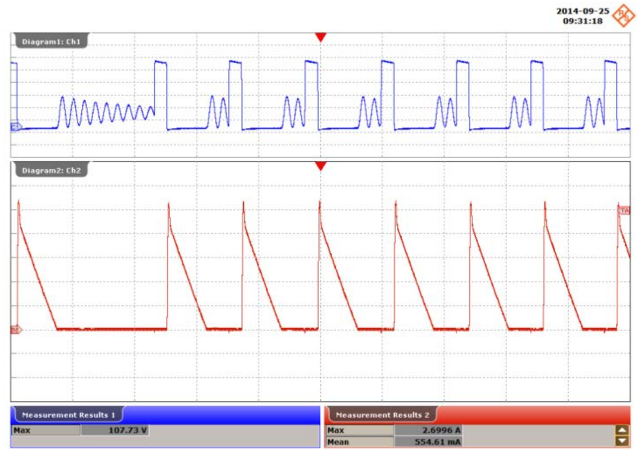

Figure 57 – 265 VAC, 60 Hz.
Upper: V_{D6}, 20 V / div.
Lower: I_{D6}, 500 mA, 10 μs / div.

11.10 Output Diode Current and Voltage Short-Circuit Waveforms

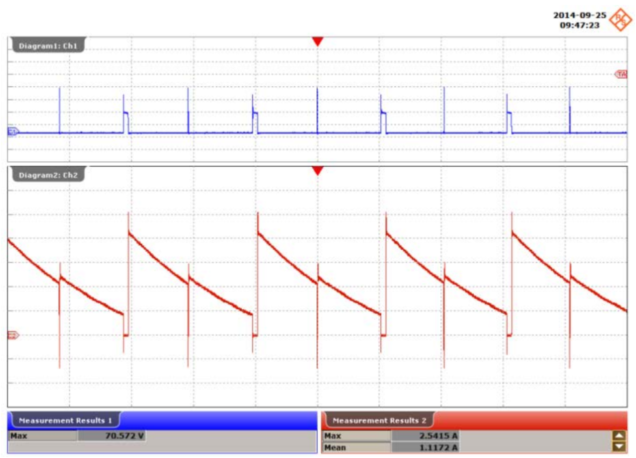

Figure 58 – 90 VAC, 50 Hz.
Upper: V_{D6}, 20 V / div.
Lower: I_{D6}, 500 mA, 50 μs / div.

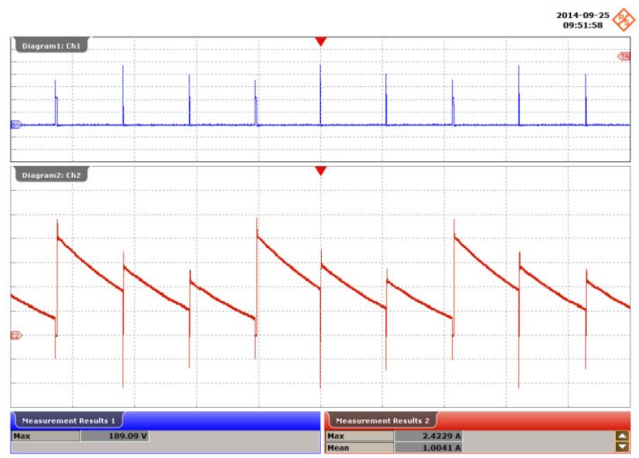

Figure 59 – 265 VAC, 60 Hz.
Upper: V_{D6}, 40 V / div.
Lower: I_{D6}, 500 mA, 50 μs / div.

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11.11 Brown-out / Brown-in

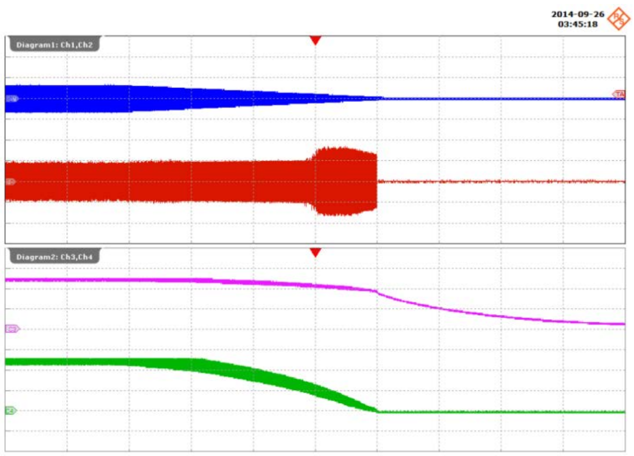

Figure 60 – 90 VAC, Brown-out (1 V / s Decay Rate).
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{IN}, 400 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 20 s / div.

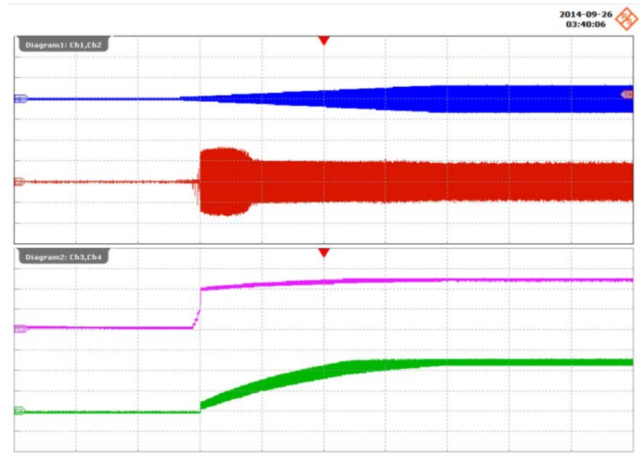

Figure 61 – 90 VAC, Brown-in (1 V / s Ramp Rate).
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{IN}, 400 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 20 s / div.

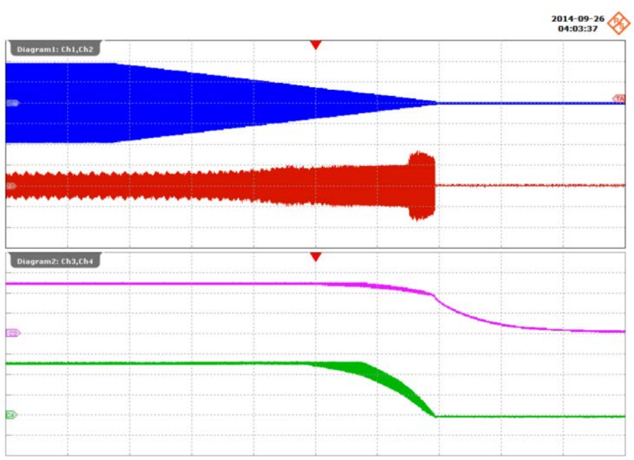

Figure 62 – 265 VAC, Brown-out (1 V / s Decay Rate).
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{IN}, 400 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 50 s / div.

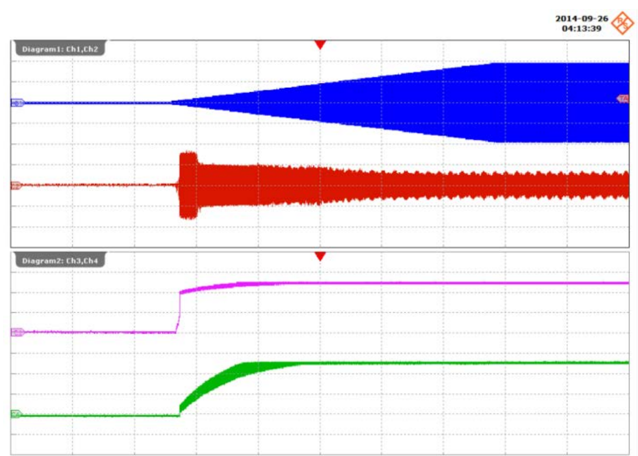

Figure 63 – 265 VAC, Brown-in (1 V / s Ramp Rate).
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{IN}, 400 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 50 s / div.

11.12 Line Transient

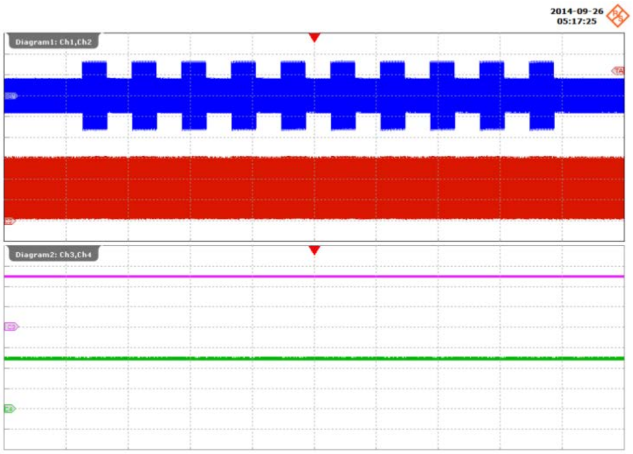

Figure 64 – 115 VAC to 230 VAC Line Transient.
CH1: V_{IN}, 200 V / div.
CH2: I_{DRAIN}, 200 mA / div.
CH3: V_{OUT}, 10 V / div.
CH4: I_{OUT}, 200 mA, 1 s / div.

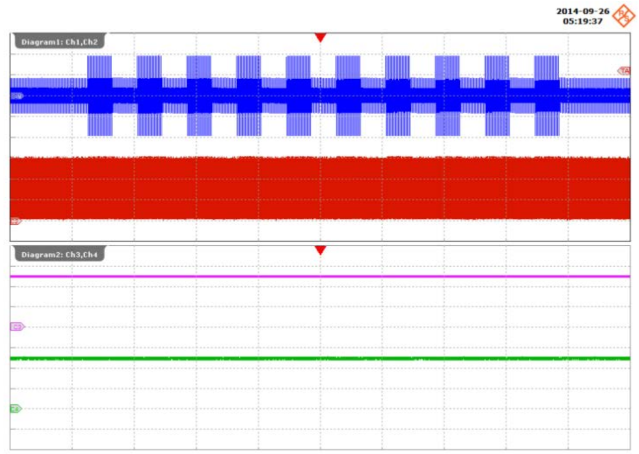

Figure 65 – 115 VAC to 265 VAC Line Transient.
CH1: V_{IN}, 200 V / div.
CH2: I_{DRAIN}, 200 mA / div.
CH3: V_{OUT}, 10 V / div.
CH4: I_{OUT}, 200 mA, 1 s / div.

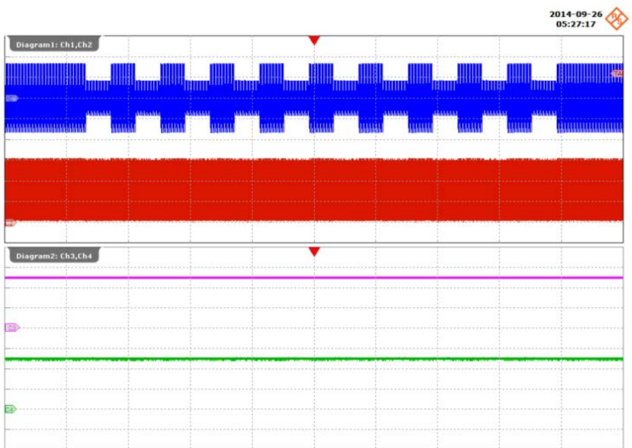

Figure 66 – 230 VAC to 115 VAC Line Transient.
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 1 s / div.

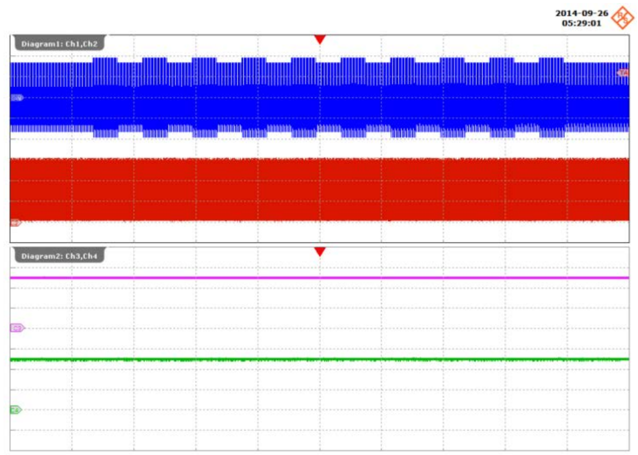

Figure 67 – 230 VAC to 265 VAC Line Transient.
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 1 s / div.

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11.13 400 ms ON, 400 ms OFF AC Cycling

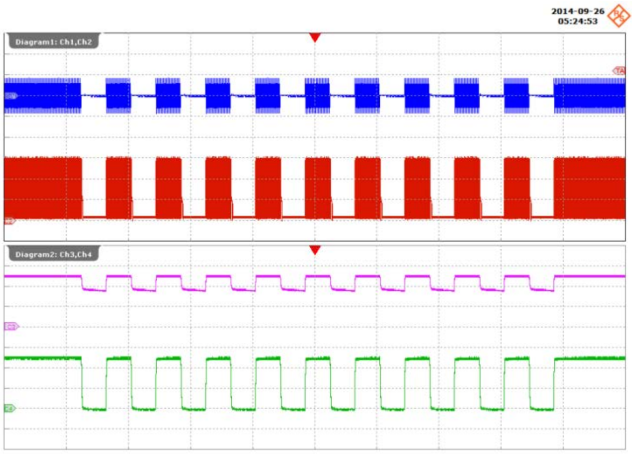

Figure 68 – 115 VAC, ON-OFF Cycling.
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 1 s / div.

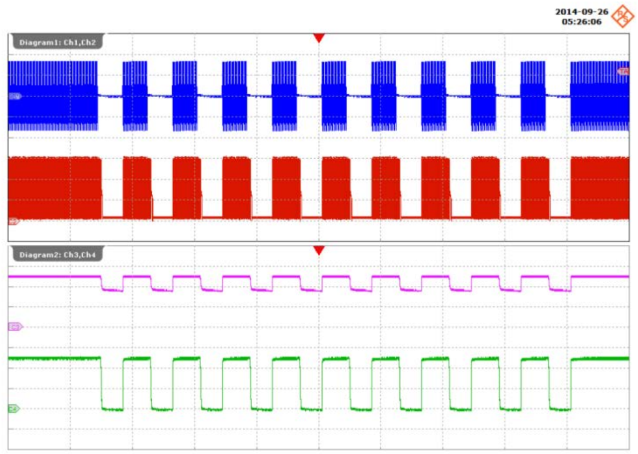

Figure 69 – 230 VAC, ON-OFF Cycling.
Upper: V_{IN}, 200 V / div.
Upper Middle: I_{DRAIN}, 200 mA / div.
Lower Middle: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA, 1 s / div.

12 Conducted EMI

The unit was tested using series of 7 LEDs and a 7.5 Ω resistor (24 V, 500 mA).

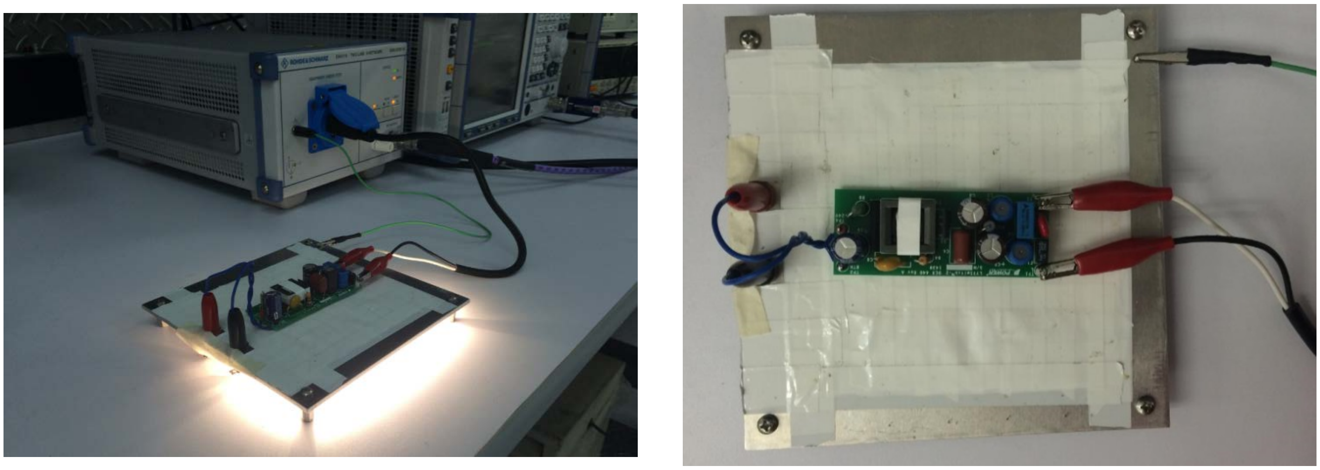

Figure 70 – Conducted EMI Set-up.

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12.1 Conducted EMI Ground Plane with Connection to Earth

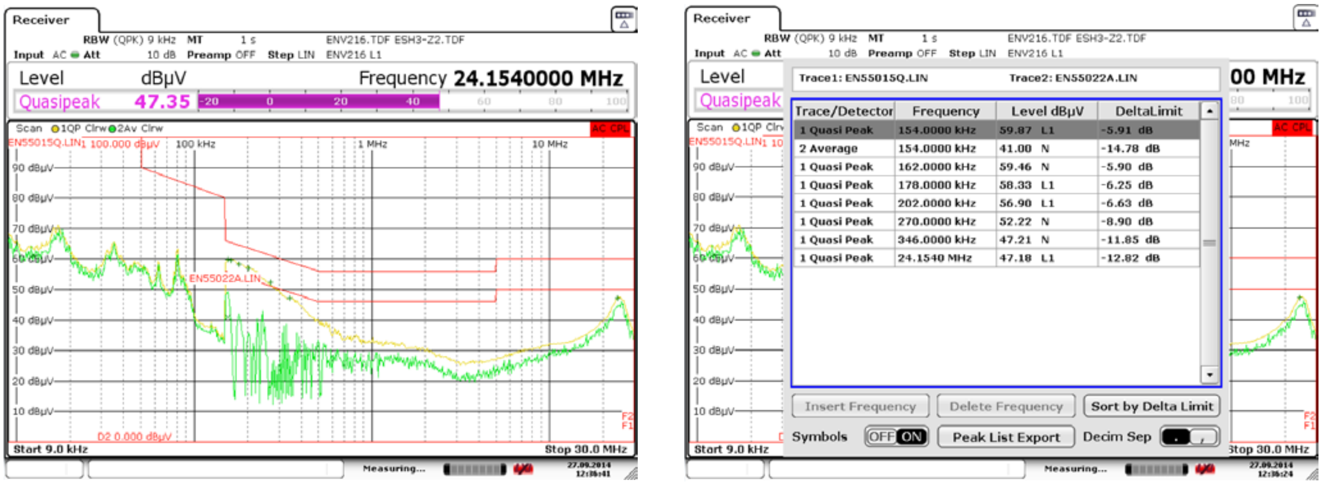

Figure 71 – 115 VAC, 60 Hz, EN55015 B Limits (Quasi-Peak Scan).

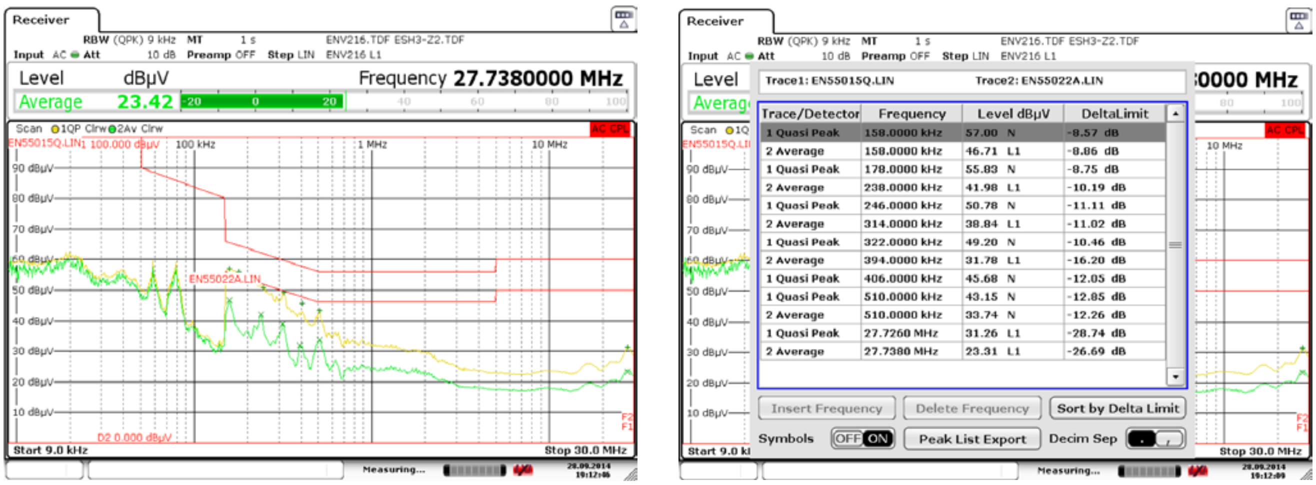

Figure 72 – 230 VAC, 60 Hz, EN55015 B Limits (Quasi-Peak Scan).

12.2 Conducted EMI Ground Plane without Connection to Earth

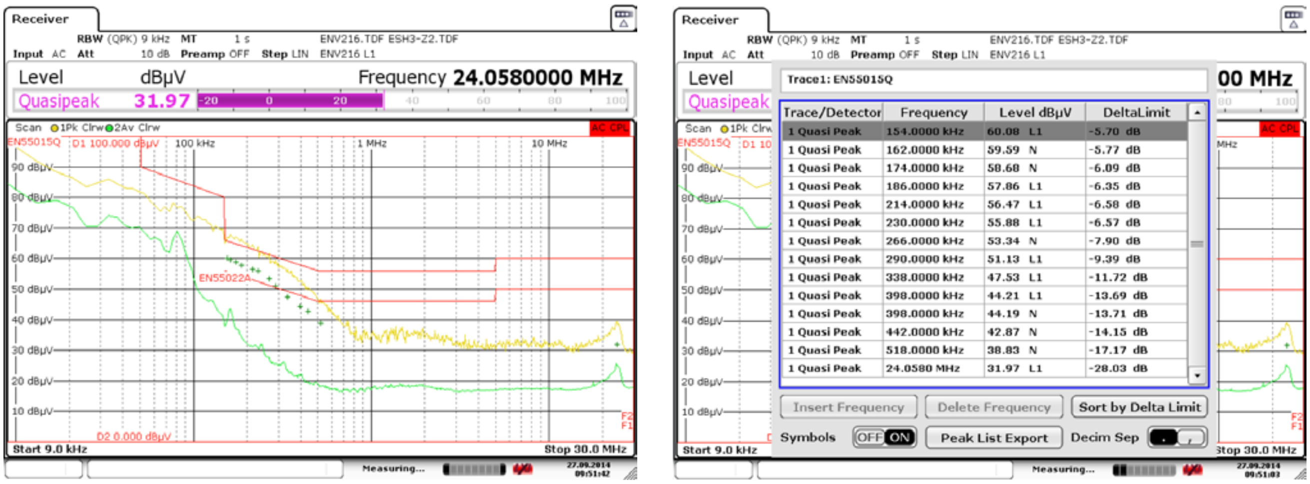

Figure 73 – 115 VAC, 60 Hz, EN55015 B Limits (Peak Scan).

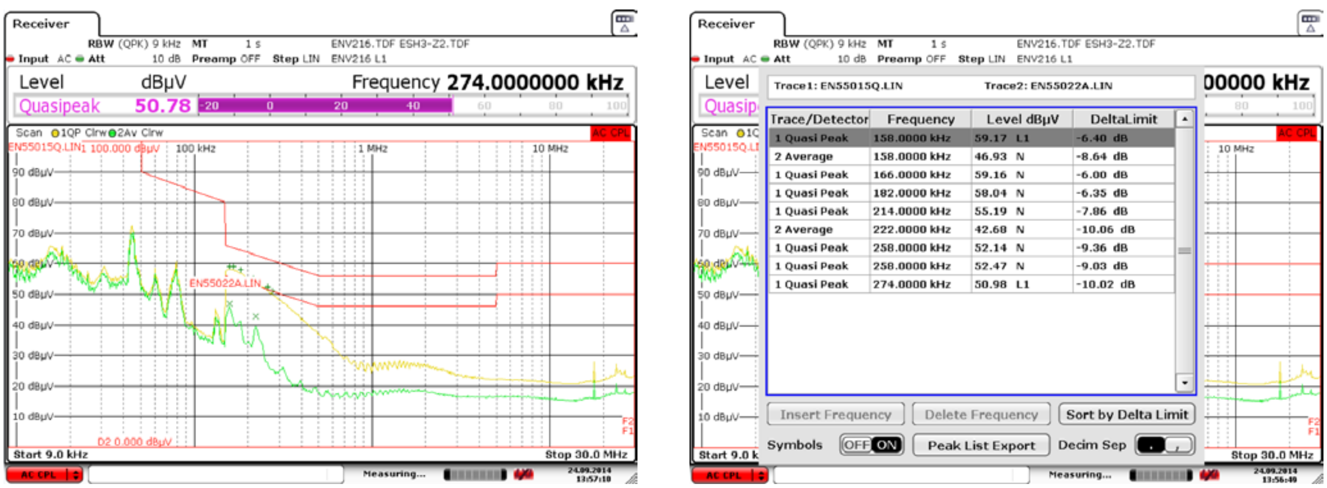

Figure 74 – 230 VAC, 60 Hz, EN55015 B Limits (Quasi-Peak Scan).

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13 Line Surge Test

The unit was subjected to ±2500 V, 100 kHz ring wave and ±1000 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+1000	230	L1, L2	0	Surge (2Ω)	Pass
-1000	230	L1, L2	90	Surge (2Ω)	Pass
+1000	230	L1, L2	0	Surge (2Ω)	Pass
-1000	230	L1, L2	90	Surge (2Ω)	Pass

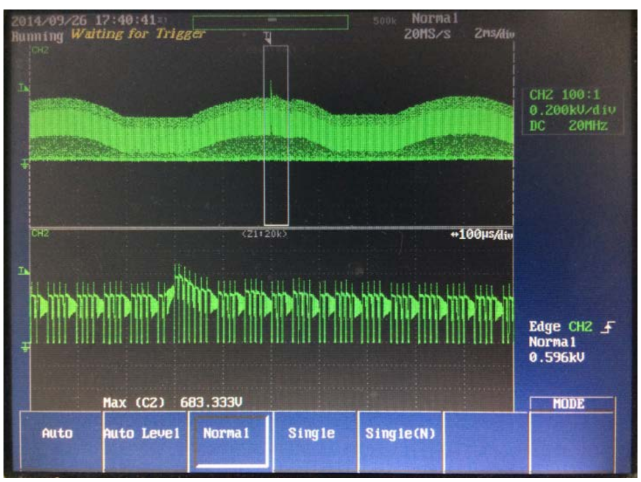

Figure 75 – (+) 1000 V Differential Surge, 90º.
Upper: V_{DRAIN}, 200 V / div., 20 ms / div.
Lower: V_{DRAIN} (zoomed-in), 200 V / div., 2 ms / div.

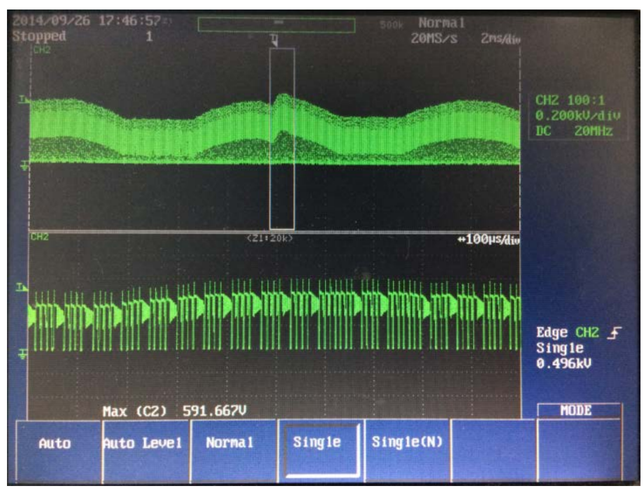

Figure 76 – (+) 2500 V Ring Wave, 90º.
Upper: V_{DRAIN}, 200 V / div., 20 ms / div.
Lower: V_{DRAIN} (zoomed-in), 200 V / div., 2 ms / div.

14 Electrostatic Discharge (ESD)

The unit was subjected to +8 kV, contact discharge and ±15 kV, air discharge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharges	Test Result (Pass/Fail)
+8000	230	Contact	10	Pass
+15000	230	Air	10	Pass

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
29-Sep-15	AP	1.0	Initial Release	Apps & Mktg

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Patent Information

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