



Design Example Report

Title	<i>8 W Power Factor Corrected (Valley Fill) Non-Dimmable Isolated Flyback, Constant Voltage LED Driver Using LYTSwitch™-2 LYT2005E</i>
Specification	Input: 190 VAC – 265 VAC (47 – 63 Hz) Output: 24 V, 330 mA
Application	Ballast Type LED Driver
Author	Applications Engineering Department
Document Number	DER-422
Date	July 24, 2014
Revision	1.1

Summary and Features

- No-load consumption <60 mW at 230 VAC
- >80% full load efficiency
- Accurate I²f combined parameter (–10%, +12%) reduces system cost
 - Increases MOSFET and magnetics power delivery
 - Reduces overload power, lowering output diode and capacitor costs
- Integrated LYTSwitch-2 Safety/Reliability features:
 - Accurate auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
 - Auto-restart protects against output short circuit and open loop fault conditions
 - >3.2 mm package creepage enables reliable operation in high humidity and high pollution environments
- Meets EN550022, EN55015 and CISPR-22 Class B conducted EMI
- Accurate load and line regulation easily meets ±5% CC
- EcoSmart™ – Meets all existing and proposed harmonized energy efficiency standards for external adapters including: CECP (China), CEC, EPA, AGO, European Commission

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing 8 W power supply utilizing a LYTSwitch-2 LYT2005E. This power supply was designed for LED ballast application and may be used also as a general evaluation platform for other applications. The power supply has a constant voltage (CV) and constant current (CC) characteristic, making it ideal for configurable load or application.

The LYTSwitch-2 provides a sophisticated range of protection features including auto-restart for control loop component open/short circuit, over voltage protection and output short-circuit conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and the PCB), which even in high humidity environment help prevents arcing which increases reliability.

The EE16 transformer bobbin in this design includes extended creepage distance to meet safety spacing requirements.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

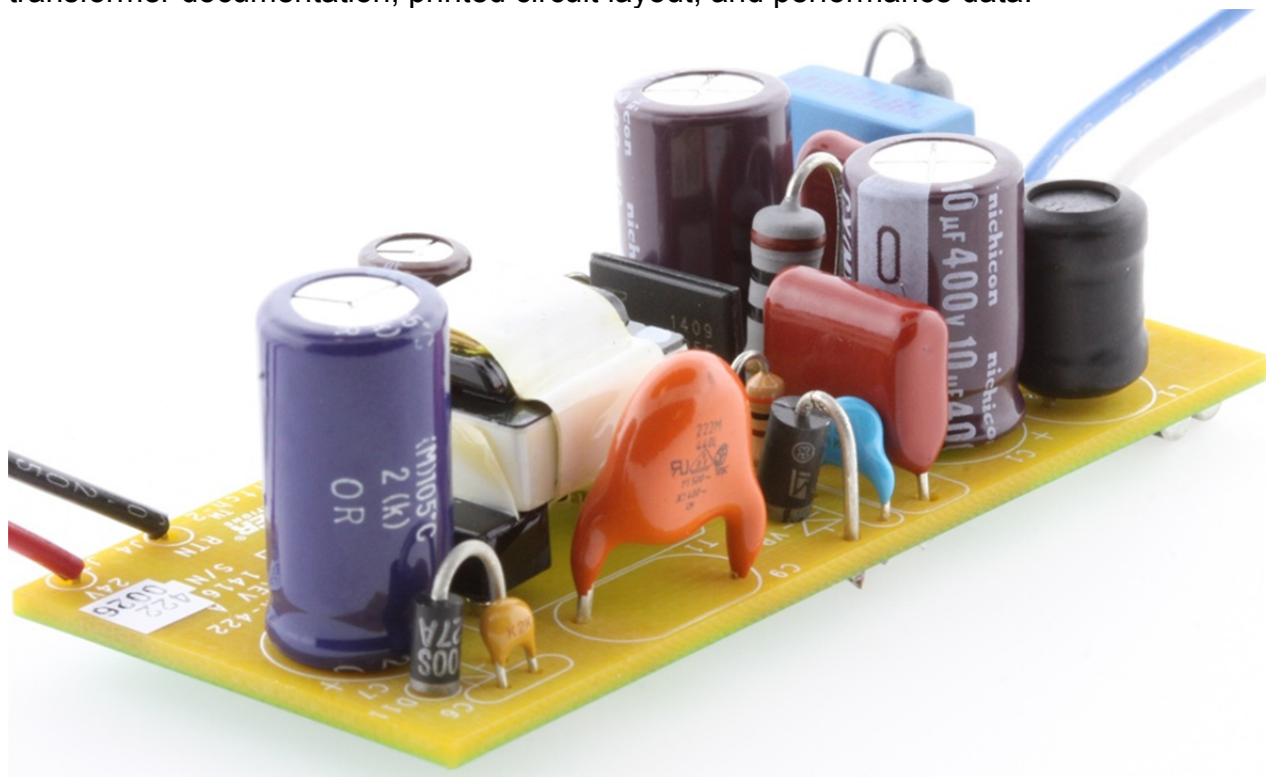


Figure 1 – Populated Circuit Board Photograph.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power (230 VAC)				0.1	W	
In-rush current (Cold start)	I_{RUSH}					269 V; 50 Hz – No damage will occur to the PSU nor should the fuse open
Output						
Output Voltage	V_{OUT}	23	24	25	V	$\pm 5\%$
Output Ripple Voltage	V_{RIPPLE}			1	V	Peak to peak, 20 MHz bandwidth-measured with 0.1 μF and 1 μF Ceramic Capacitor
Total Output Power						
Continuous Output Power	P_{OUT}			8	W	
Peak Output Power	P_{OUT_PEAK}			10	W	
Efficiency						
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{AVE}	80			%	Per Energy Star test method
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B/FCC Part 15				6 dBuV margin with Grounded and Ungrounded chassis
Safety		Designed to meet IEC950 / UL1950 Class II				
Leakage Current	I_{LEAK}	0.25 mA				Measured at 265 V_{RMS} , 50/60 Hz
Line Surge						
Differential Mode (L1-L2)				1	kV	IEC 61000-4-5/EN5504, 500 A short-circuit Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Common mode (L1/L2-PE)				2.5	kV	
Ring Wave (100 kHz)						
Differential Mode (L1-L2)				2.5	kV	
Common mode (L1/L2-PE)					kV	
Ambient Temperature	T_{AMB}	0		40	$^{\circ}C$	Free convection, sea level



Figure 2 – Schematic.

4 Circuit Description

This cost effective cost converter is configured as an isolated flyback. The converter provides 330 mA at 24 V output and an input voltage range of 190 VAC to 265 VAC designed to drive LEDs in a constant voltage, constant current (CV/CC) operation for LED driver applications.

4.1 Input Stage

Fusible resistor FR1 provides protection against component failure. The resistance of the fusible resistor also helps reduce stress on the integrated power MOSFET during a line surge.

The passive damping resistance and the total effective input capacitance are sufficient to suppress differential mode line surges of 1 kV differential mode and 2.5 kV ring-wave. A MOV (located after FR1) is required to withstand surges of >1 kV.

The AC input is full-wave rectified by BR1.

Capacitor C12, C10, C11 and differential choke L1 form the EMI filter. This together with the frequency jittering feature of LYTSwitch-2 ensures compliance with EN 55055 Class B emission limits. Resistor R1 damps the resonance of the EMI filter, preventing peaks in the EMI spectrum. Inductor L1 is positioned after the bridge to avoid an imbalance in EMI between line and neutral. This positioning also permits the use of small high-voltage ceramic capacitors in the input filter.

A valley-fill circuit comprising C1, C2 and D5, D6, and D7 ensures a power factor greater than 0.7. The same circuit also absorbs energy during a line disturbance allowing the circuit to meet IEC 61000-4-5/EN5504.

4.2 LYTSwitch-2 Primary

The LYTSwitch-2 device (U1) is an integrated IC, which includes a power MOSFET, an oscillator, controller block, start-up circuit and protection functions. It is a low part-count design, optimized for ballast lighting applications. The power supply features very accurate regulation of the output voltage and current without the use of an optocoupler. The integrated 700 V switching MOSFET and ON/OFF control function achieve both high efficiency (under all load conditions), and very low no-load energy consumption. Any design using the LYTSwitch-2 family of easily meets all current and proposed international energy efficiency standards.

A clamp circuit (D9, VR1, R4 and C3) limits the voltage that can appear on the drain of U1 each time the power MOSFET turns off. This clamp design also maximizes efficiency at light load as it returns some of the energy stored in C3 back to the input.

The output of the bias/auxiliary winding is rectified by diode D10 and filtered by R10 and capacitor C5. The bias winding is used to supply current to the LYT2005E BYPASS (BP) pin during steady state operation. The value of resistor R7 is selected to deliver the



correct IC supply current to the BP pin in order to achieve low input power consumption under light load and no-load conditions.

4.3 Output Rectification

Schottky diode D11 provides output rectification, and capacitor C7 is the main output filter capacitor. A secondary RC snubber is used across D11 to reduce common-mode EMI.

Resistor R9 is an output pre-load and is necessary to prevent the output voltage from rising if the load is disconnected.

4.4 Output Feedback

The IC regulates by using ON/OFF control for CV regulation and frequency control for CC regulation. The feedback resistors (R5 and R6) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation points.

4.5 Open-loop and Output Short Protection

In the event of a fault condition the LYTSwitch-2 enters into a protection mode. If the FEEDBACK pin voltage falls below 0.7 V during the flyback period ($t_{AR(ON)}$) the converter enters auto-restart. In addition, if the FEEDBACK pin current during the forward period of the conduction cycle falls below $\sim 120 \mu A$, the converter infers an open-loop condition. The data sheet provides information on auto-restart and open-loop-protection.



5 PCB Layout

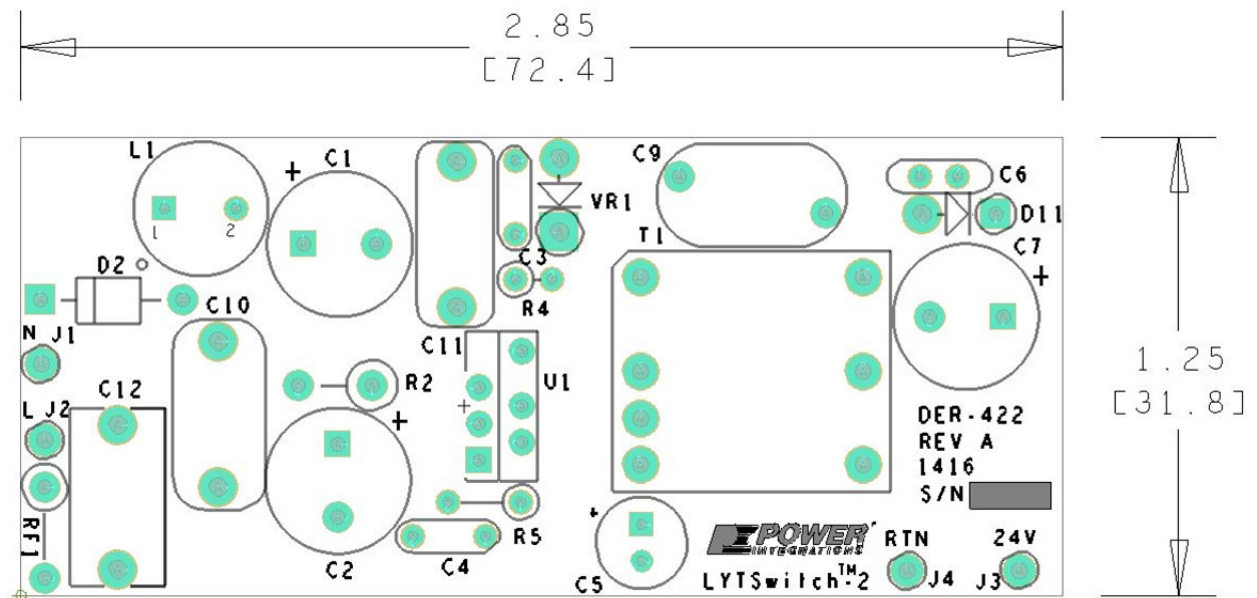


Figure 3 – Top Printed Circuit Layout.

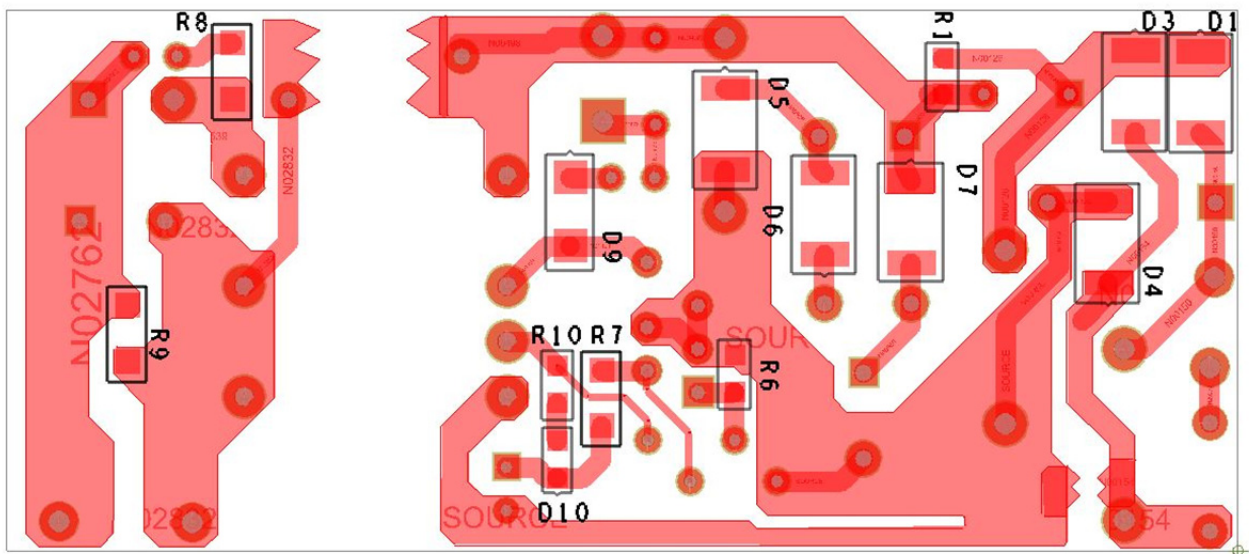


Figure 4 – Bottom Layout.



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7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg P/N	Manufacturer
1	2	C1 C2	10 μ F, 400 V, Electrolytic, (10 x 16)	UCY2G100MPD	Nichicon
2	1	C3	1 nF, 1 kV, Disc Ceramic	DEBE33A102ZC1B	Murata
3	1	C4	1.0 μ F, 50 V, Ceramic, X7R	FK20X7R1H105K	TDK
4	1	C5	10 μ F, 100 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG101ELL100MF11D	Nippon Chemi-Con
5	1	C6	1000 pF, 200 V, Ceramic, X7R	C315C102K2R5TA	Kemet
6	1	C7	470 μ F, 35 V, Electrolytic, Low ESR, 52 m Ω , (10 x 20)	ELXZ350ELL471MJ20S	Nippon Chemi-Con
7	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
8	1	C10	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
9	1	C11	220 nF, 450 V, Film	MEXXF32204JJ	Duratech
10	1	C12	100 nF, 305 VAC, Film, X2	B32921C3104M	Epcos
11	6	D1 D3 D4 D5 D6 D7	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
12	1	D2	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
13	1	D9	600 V, 1 A, Standard Recovery, SMA	S1J-13-F	Diodes, Inc.
14	1	D10	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
15	1	D11	Diode, Schottky, 200 V, 2 A, DO204AL	VSB2200S-M3/54	Vishay
16	1	L1	10 mH, 0.076 A, 20%	RL-5480-3-10000	Renco
17	1	R1	10 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
18	1	R2	10 Ω , 5%, 1 W, Metal Oxide	RSF100JB-10R	Yageo
19	1	R4	300 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-300R	Yageo
20	1	R5	60.4 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-60K4	Yageo
21	1	R6	5.62 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5621V	Panasonic
22	1	R7	7.5 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ752V	Panasonic
23	1	R8	33 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ330V	Panasonic
24	1	R9	330 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ334V	Panasonic
25	1	R10	2.2 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
26	1	RF1	10 Ω , 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 10R	Vitrohm
27	1	T1	Bobbin, EE16 Extended Creepage, Horizontal, 10 pins; Custom Transformer	Custom SNX-R1745-X1	Taiwan Shulin Santronics
28	1	U1	LYTSwitch-2, CV/CC, eSIP	LYT2005E	Power Integrations
29	1	VR1	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	Littlefuse
Mechanical BOM					
1	1	J2; L (WIRE #24 AWG INS)	Wire, UL1007, #24 AWG, Blu, PVC, 4"	1007-24/7-6	Anixter
2	1	J1; N (WIRE #24 AWG INS)	Wire, UL1007, #24 AWG, Wht, PVC, 4"	1007-24/7-9	Anixter
3	1	J3; V+ (WIRE #24 AWG INS)	Wire, UL1007, #24 AWG, Red, PVC, 4"	1007-24/7-2	Anixter
4	1	J4; RTN (WIRE #24 AWG INS)	Wire, UL1007, #24 AWG, Blk, PVC, 4"	1007-24/7-0	Anixter
5	1	PCB	PCB, 0.062X 1.25 X 4 in; 2oz Cu	-	-



8 Transformer Specification

8.1 Electrical Diagram

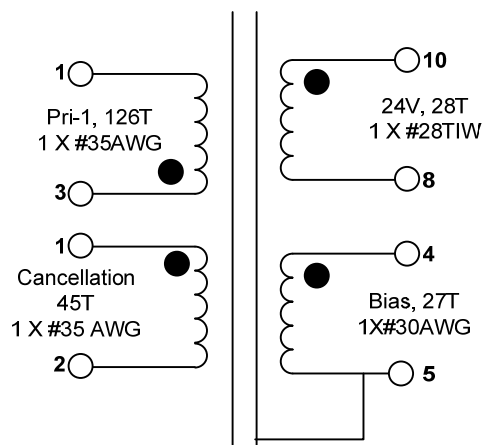


Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 8-9.	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	1100 μ H $\pm$ 10%
Resonant Frequency	Pins 1-3 all other windings open.	635 kHz $\pm$ 20 kHz
Primary Leakage Inductance	Pins 1-3, with pins 5-9 shorted, measured at 100 kHz, 0.4 V _{RMS} .	35 μ H (Max.)

8.3 Materials

Item	Description
[1]	Core: EE16, P4 (Acme) or Equivalent, gapped for ALG of 69.25 nH/T ² .
[2]	Bobbin: EE16 (5-5 pins) Horizontal, High Creepage.
[3]	Tape Polyester film [2 mil (25 μ m) base thickness], 8.3 mm wide.
[4]	Varnish; BC346 or BC359 (Dolphins).
[5]	Magnet Wire: AWG #35.
[6]	Tripple Insulated Wire: AWG #28.
[7]	Magnet Wire: AWG #30.
[8]	Copper tape; 2 mil thick; 7.5 mm width.
[9]	Tape Polyester film [2 mil (25 μ m) base thickness], 5.00 mm wide.



8.4 Transformer Build Diagram

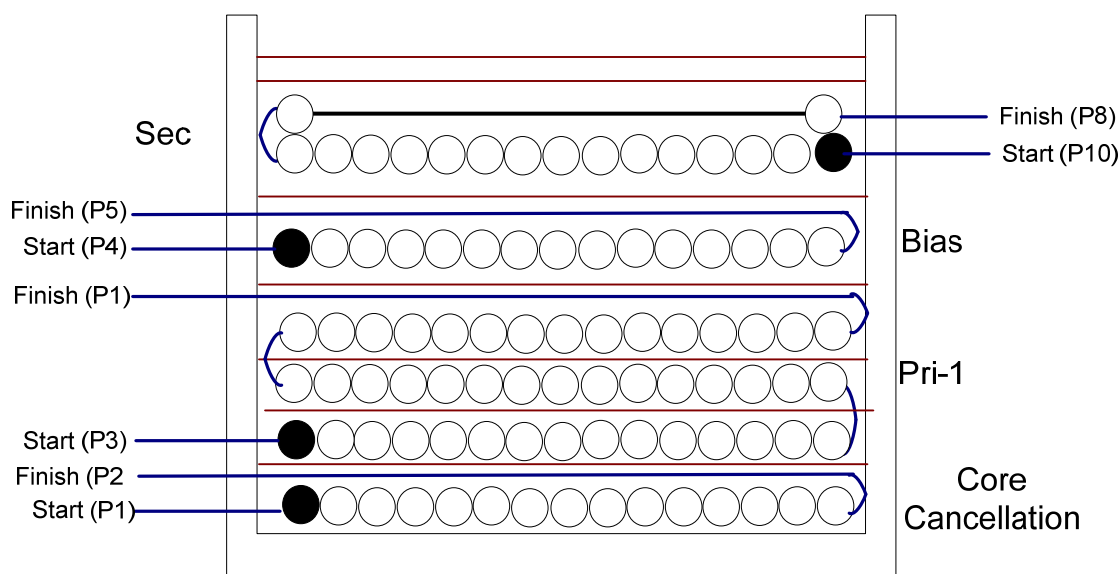


Figure 8 – Transformer Build Diagram.

8.5 Transformer Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise. Follow the pin number assignment in the specification. Cut pin number 2, 7 and pin 9.
WDG1; Core Cancellation	Start on pin(s) 1 and wind 45 turns (x1 filar) of item [5] from left to right. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2.
Insulation	Add 1 layer of tape, item [3], for insulation.
WDG2; Pri-1	Start on pin(s) 3 and wind 42 turns (x1 filar) of item [5]. in 2 layer(s) from left to right. Add 1 layer of tape, item [3], for insulation. At the end of 1st layer, continue to wind the next layer from right to left. Add 1 layer of tape, item [3], for insulation. At the end of 2nd layer, continue to wind the next layer from left to right. Finish this winding on pin(s) 1.
Insulation	Add 1 layer of tape, item [3], for insulation.
WDG3; Bias	Start on pin(s) 4 and wind 27 turns (x1 filar) of item [7]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5.
Insulation	Add 1 layer of tape, item [3], for insulation.
WDG3; Sec	Start on pin(s) 10 and wind 28 turns (x1 filar) in two layer of item [6]. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 8.
Insulation	Add 3 layers of tape, item [3], for insulation.
Core Preparation	Grind E core to get the desired inductance. Wrap bottom of one E core with 2 layers of tape to secure the core
Shield	Add the copper shield perpendicular to the core leg then terminate to pin 5 with item 5.
Varnish	Dip the transformer to the varnish [4] then dry.

9 Transformer Design Spreadsheet

ACDC_LYTSwitch-2_051614; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LYTSwitch-2_051614_Rev2-0; Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC Input Voltage
fL	50		50	Hz	AC Mains Frequency
Application Type	Ballast-CV	Info	Ballast-CV		For CV ballast applications, the calculations use a current that is 1.2*IO to guarantee that the part never goes into CC mode
VO	24.00		24.00	V	Output Voltage
IO	0.33		0.33	A	Power Supply Output Current
Power			7.92	W	Continuous Output Power
n	0.80		0.80		Efficiency Estimate at output terminals
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	16.00		16.00	uF	Input Capacitance
ENTER LYTSwitch-2 VARIABLES					
Chosen Device	LYT2005K/E		LYT2005K/E		Chosen LYTSwitch-2 device
ILIMITMIN			0.53	A	Minimum Current Limit
ILIMITTYP			0.58	A	Typical Current Limit
ILIMITMAX			0.62	A	Maximum Current Limit
FS	61.00		61.00	kHz	Typical Device Switching Frequency at maximum power
VOR			114.33	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			1.33		KP assuming minimum LP, VMIN, and average switching frequency. Ensure that this value is above 1.30 for optimal operation
FEEDBACK WINDING PARAMETERS					
NFB	27.00		27.00		Feedback winding turns
VFLY			24.50	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			16.33	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
BIAS	Ext. bias		Ext. bias		Select between self bias or external bias to supply the IC.
VB			N/A	V	Feedback Winding Voltage (VFLY) is greater than 10 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.
NB			N/A		Bias Winding number of turns
REXT			38.00	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON	4.65		4.65	us	Desired output diode conduction time



DCON_FINAL			4.70	us	Final output conduction diode, assuming integer values for NP and NS
TON			7.06	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		Info	60.01	k-ohm	Upper resistor in Feedback resistor divider. Once the initial prototype is running, it may be necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER			5.16	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	EE16		EE16		Enter Transformer Core.
Custom_Core					Enter Core name if selection on drop down menu is "Custom"
Bobbin			BE-16-116CP		Bobbin part number
AE			19.20	mm^2	Core Effective Cross Sectional Area
LE			35.00	mm	Core Effective Path Length
AL			1140.00	nH/tur n^2	Ungapped Core Effective Inductance
BW			8.50	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3.00		Number of Primary Layers
NS			27.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			76.19	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.53		Maximum duty cycle measured at VMIN
Iavg			0.18	A	Input Average current
IP			0.53	A	Peak primary current
IR			0.53	A	Primary ripple current
IRMS			0.26	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1016.63	uH	Minimum Primary Inductance
LPTYP			1093.16	uH	Typical Primary inductance
LP_TOLERANCE			7.00	%	Tolerance in primary inductance
NP			126.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			68.86	nH/tur n^2	Gapped Core Effective Inductance
BM_TARGET			2600.00	Gauss	Target Flux Density
BM			2598.23	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2600 is recommended
BP			3002.52	Gauss	!!! Warning. Peak Flux density exceeds 3100 Gauss and is not recommended. Reduce BP by increasing NS
BAC			1299.12	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			165.37		Relative Permeability of Ungapped Core
LG			0.36	mm	Gap Length (LG > 0.1 mm)
BWE			25.50	mm	Effective Bobbin Width
OD			0.20	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)



DIA			0.16	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32.00	Cmils	Bare conductor effective area in circular mils
CMA		<i>Warning</i>	122.53	Cmils/ A	!!! Warning. CMA is less than 200 and may cause overheating of the primary winding. Increase primary winding layers or use larger transformer
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			2.47	A	Peak Secondary Current
ISRMS			0.99	A	Secondary RMS Current
IRIPPLE			0.91	A	Output Capacitor RMS Ripple Current
CMS			198.97	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			27.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			634.87	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS			104.31	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL	59.00		59.00	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL	5.23		5.23	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measured) Output Voltage (VDC)	25.19		25.19	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)	0.37		0.37	Amps	Measured Output current from first prototype
RUPPER_FINE			60.17	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 60.4 k-ohms
RLOWER_FINE			5.61	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 5.62 k-ohms

Note: CMA <200 is used in the design to evenly distribute the primary winding in 3 layers.



10 Performance Data

All measurements performed at room temperature unless otherwise specified.

10.1 Efficiency

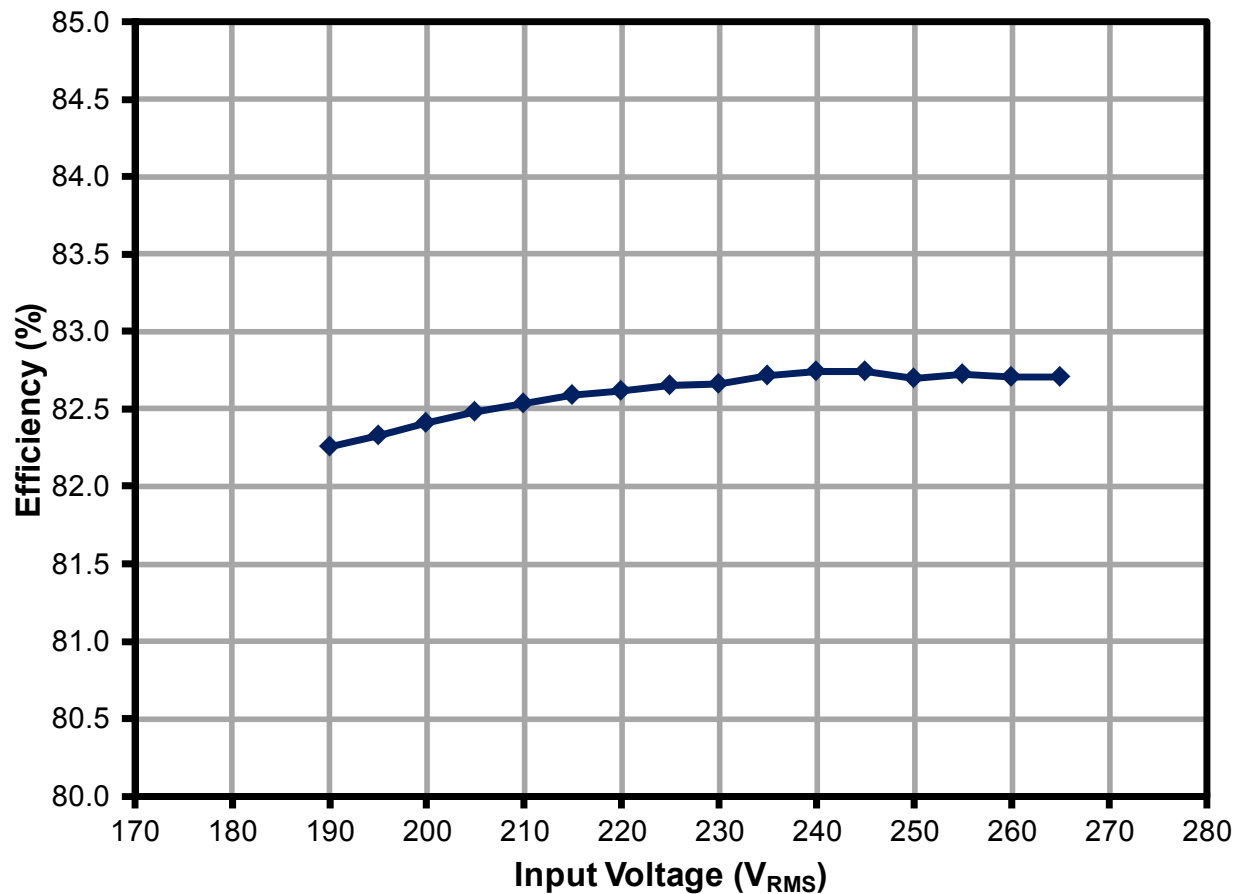


Figure 9 – Efficiency vs. Input Voltage, 50 Hz.

Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	PF	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	
180	50	179.9	0.07	9.59	0.79	23.78	0.33	7.8	82.0
185	50	184.9	0.07	9.51	0.79	23.78	0.33	7.8	82.1
190	50	189.9	0.06	9.50	0.78	23.79	0.33	7.8	82.2
195	50	194.9	0.06	9.49	0.78	23.78	0.33	7.8	82.3
200	50	199.9	0.06	9.48	0.77	23.78	0.33	7.8	82.4
205	50	204.9	0.06	9.47	0.77	23.78	0.33	7.8	82.4
210	50	209.9	0.06	9.46	0.76	23.79	0.33	7.8	82.5
215	50	214.9	0.06	9.46	0.76	23.78	0.33	7.8	82.5
220	50	219.9	0.06	9.45	0.75	23.78	0.33	7.8	82.6
225	50	224.9	0.06	9.45	0.75	23.78	0.33	7.8	82.6
230	50	229.9	0.06	9.44	0.74	23.78	0.33	7.8	82.6
235	50	234.9	0.05	9.44	0.74	23.78	0.33	7.8	82.7
240	50	239.9	0.05	9.44	0.73	23.78	0.33	7.8	82.7
245	50	244.9	0.05	9.44	0.72	23.78	0.33	7.8	82.7
250	50	249.9	0.05	9.44	0.72	23.77	0.33	7.8	82.7
255	50	254.9	0.05	9.44	0.71	23.78	0.33	7.8	82.7
260	50	259.9	0.05	9.44	0.71	23.77	0.33	7.8	82.7
265	50	265.0	0.05	9.44	0.70	23.77	0.33	7.8	82.7

Table 1 – Data for Figure 9.



10.2 Active Mode Efficiency

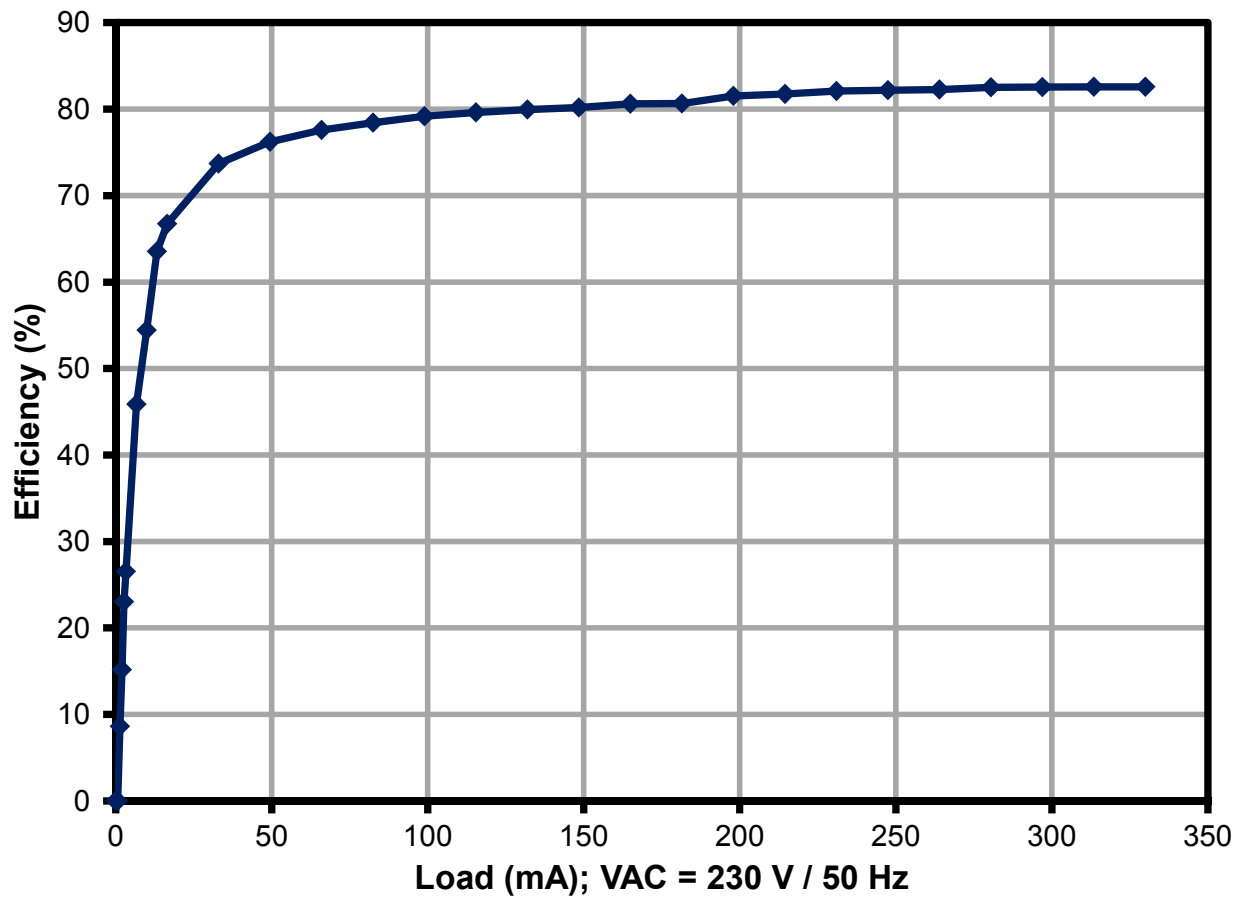


Figure 10 – Load Efficiency at 230 V_{RMS} / 50 Hz line



Load Setting		Input Measurement				Load Measurement			Efficiency (%)
Load (%)	Load (A)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	PF	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	
100%	330.00	229.93	0.06	9.46	0.74	23.78	0.33	7.81	82.58
95%	313.50	229.93	0.05	8.99	0.74	23.79	0.31	7.42	82.58
90%	297.00	229.93	0.05	8.52	0.73	23.81	0.29	7.03	82.55
85%	280.50	229.93	0.05	8.05	0.72	23.82	0.28	6.64	82.52
80%	264.00	229.93	0.05	7.57	0.69	23.74	0.26	6.23	82.27
75%	247.50	229.93	0.05	7.08	0.68	23.66	0.25	5.82	82.20
70%	231.00	229.93	0.04	6.60	0.67	23.62	0.23	5.42	82.07
65%	214.50	229.94	0.04	6.14	0.64	23.58	0.21	5.02	81.75
60%	198.00	229.94	0.04	5.68	0.64	23.55	0.20	4.63	81.52
55%	181.50	229.94	0.04	5.24	0.64	23.47	0.18	4.22	80.63
50%	165.00	229.94	0.03	4.76	0.59	23.50	0.16	3.84	80.63
45%	148.50	229.94	0.03	4.29	0.61	23.43	0.15	3.44	80.17
40%	132.00	229.94	0.03	3.82	0.59	23.41	0.13	3.05	79.96
35%	115.50	229.94	0.03	3.35	0.58	23.43	0.11	2.67	79.62
30%	99.00	229.94	0.02	2.88	0.54	23.39	0.10	2.28	79.17
25%	82.50	229.94	0.02	2.41	0.49	23.39	0.08	1.89	78.43
20%	66.00	229.94	0.02	1.94	0.44	23.38	0.06	1.51	77.59
15%	49.50	229.94	0.02	1.47	0.38	23.34	0.05	1.12	76.22
10%	33.00	229.94	0.01	0.99	0.32	23.34	0.03	0.73	73.70
5%	16.50	229.94	0.01	0.52	0.19	23.10	0.01	0.35	66.72
4%	13.20	229.94	0.01	0.42	0.15	23.38	0.01	0.27	63.55
3%	9.90	229.94	0.01	0.34	0.15	22.79	0.01	0.19	54.44
2%	6.60	229.94	0.01	0.24	0.11	22.84	0.00	0.11	45.87
1%	3.30	229.94	0.01	0.15	0.07	23.02	0.00	0.04	26.51
0.80%	2.64	229.94	0.01	0.13	0.06	23.09	0.00	0.03	23.03
0.60%	1.98	229.94	0.01	0.11	0.05	23.17	0.00	0.02	15.19
0.40%	1.32	229.94	0.01	0.10	0.05	23.20	0.00	0.01	8.61
0.20%	0.66	229.94	0.01	0.09	0.04	23.33	0.00	0.00	0.00
0.10%	0.33	229.94	0.01	0.08	0.04	23.39	0.00	0.00	0.00
0.00%	0.00	229.94	0.01	0.06	0.03	24.91	0.00	0.00	0.00
						Average % Efficiency			80.96

Table 2 – Data for Figure 10.



Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only, the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EP_SupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green-Room:

<http://www.powerint.com/greenroom/regulations.htm>

10.2.1 USA Energy Independence and Security Act 2007

This legislation mandates that all single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no-load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

$\ln$ = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes legislation from individual US States (for example CEC in California).



10.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

$\ln$ = natural logarithm

Active Mode Efficiency Low Voltage Models ($V_O < 6$ V and $I_O \geq 550$ mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

$\ln$ = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W



10.3 No-Load Input Power

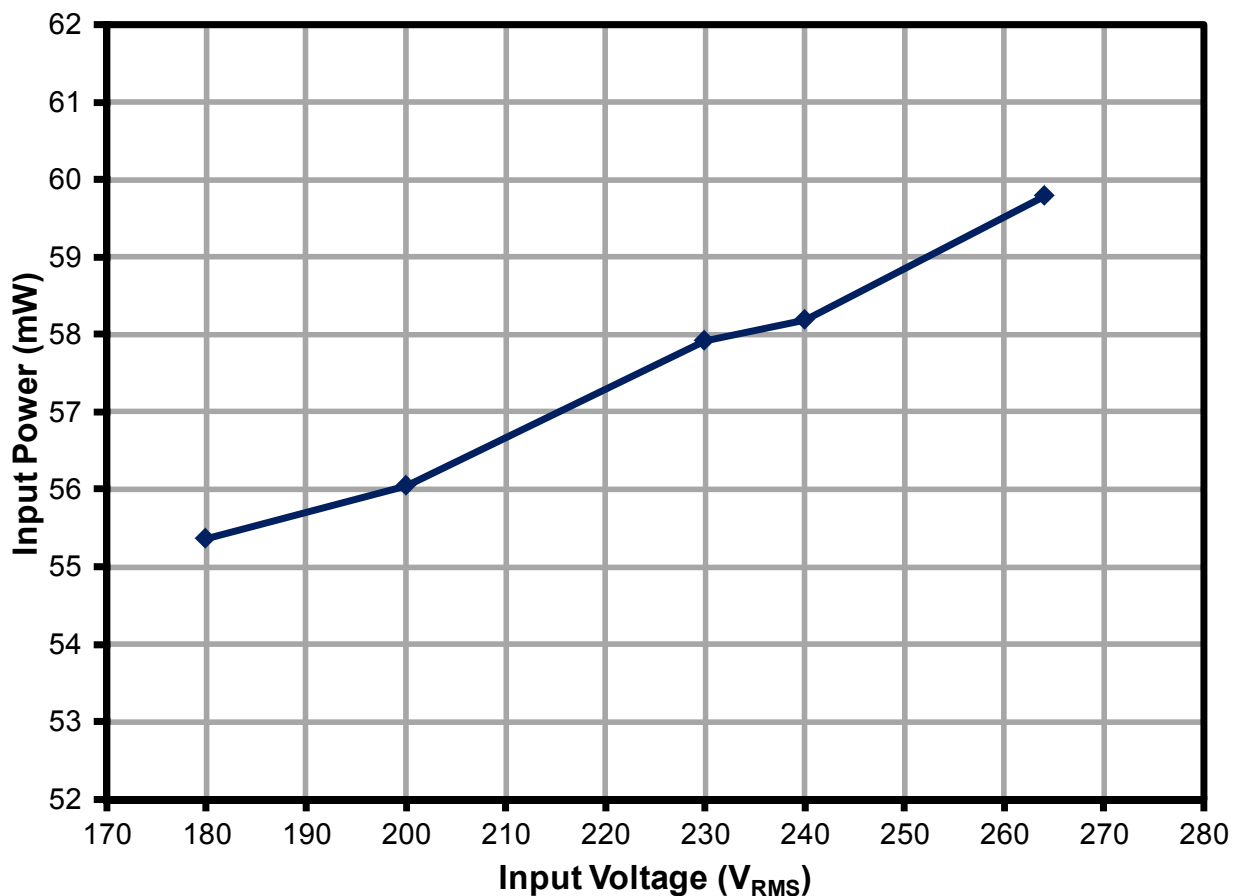


Figure 11 – Zero Load Input Power vs. Input Line Voltage, 50 Hz.

Input		Input Measurement		Input Measurement (Integration)			
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (mW)	P_{IN} (mW)	I_{IN} (mA_{RMS})	V_{OUT} (V_{DC})
180	50	179.96	8.20	55.6	55.36	8.19	25.39
200	50	199.94	8.46	55.4	56.05	8.46	25.33
230	50	229.95	8.95	58.0	57.91	8.94	25.26
240	50	239.97	9.12	57.9	58.18	9.12	25.22
264	50	264.00	9.53	59.3	59.79	9.53	25.13

Table 3 – Data for Figure 11.



10.4 Regulation

10.4.1 Load

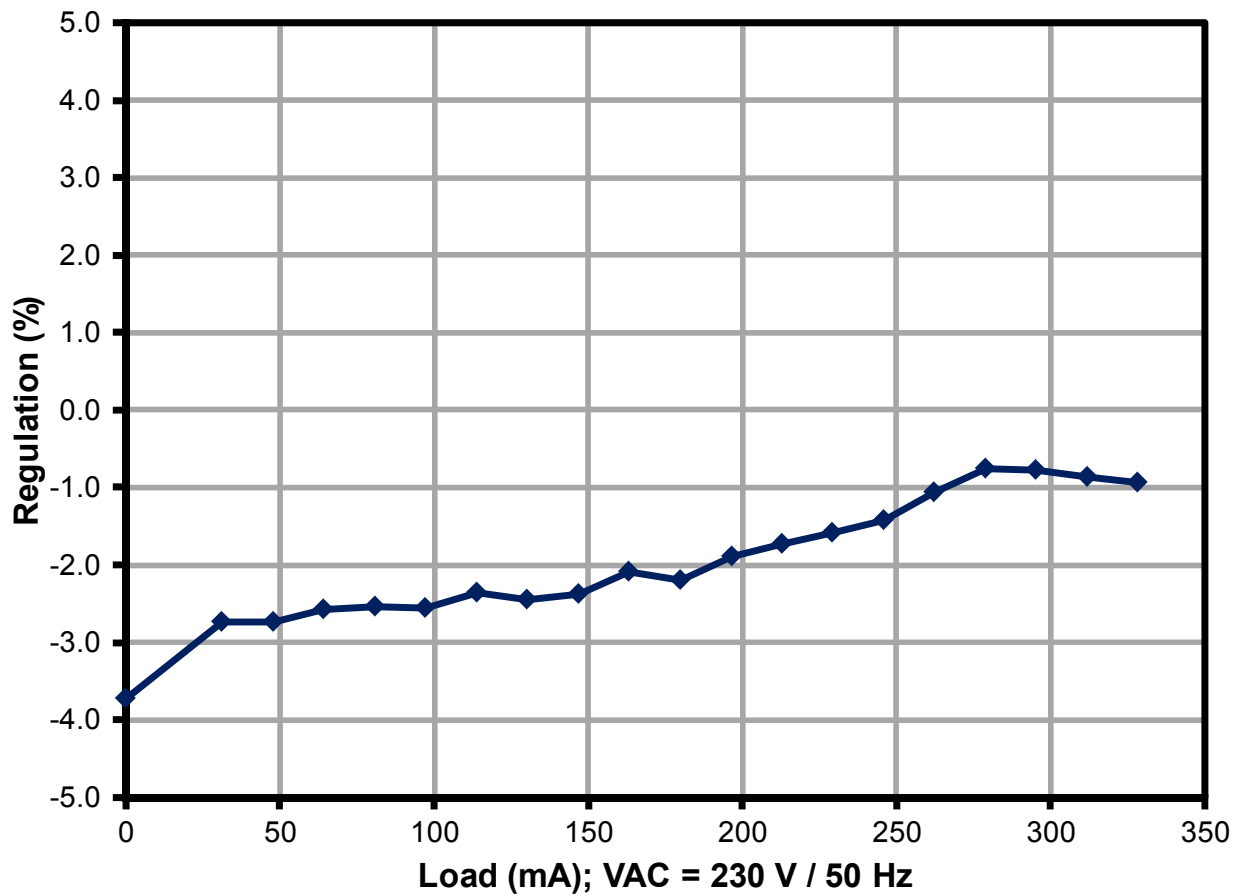
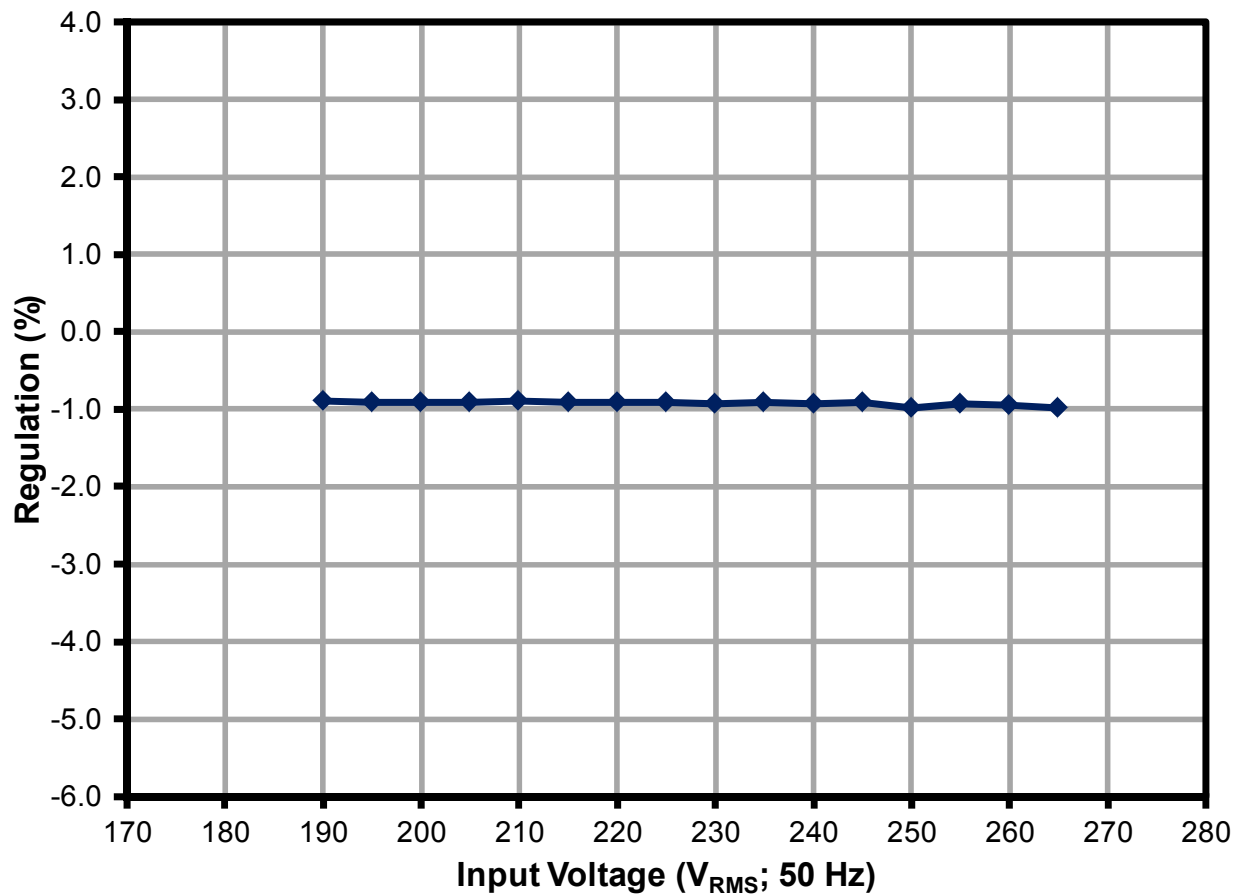


Figure 12 – Load Regulation, CV



10.4.2 Line

**Figure 13** – Line Regulation, CV, Full Load.

10.4.3 Power Factor (PF)

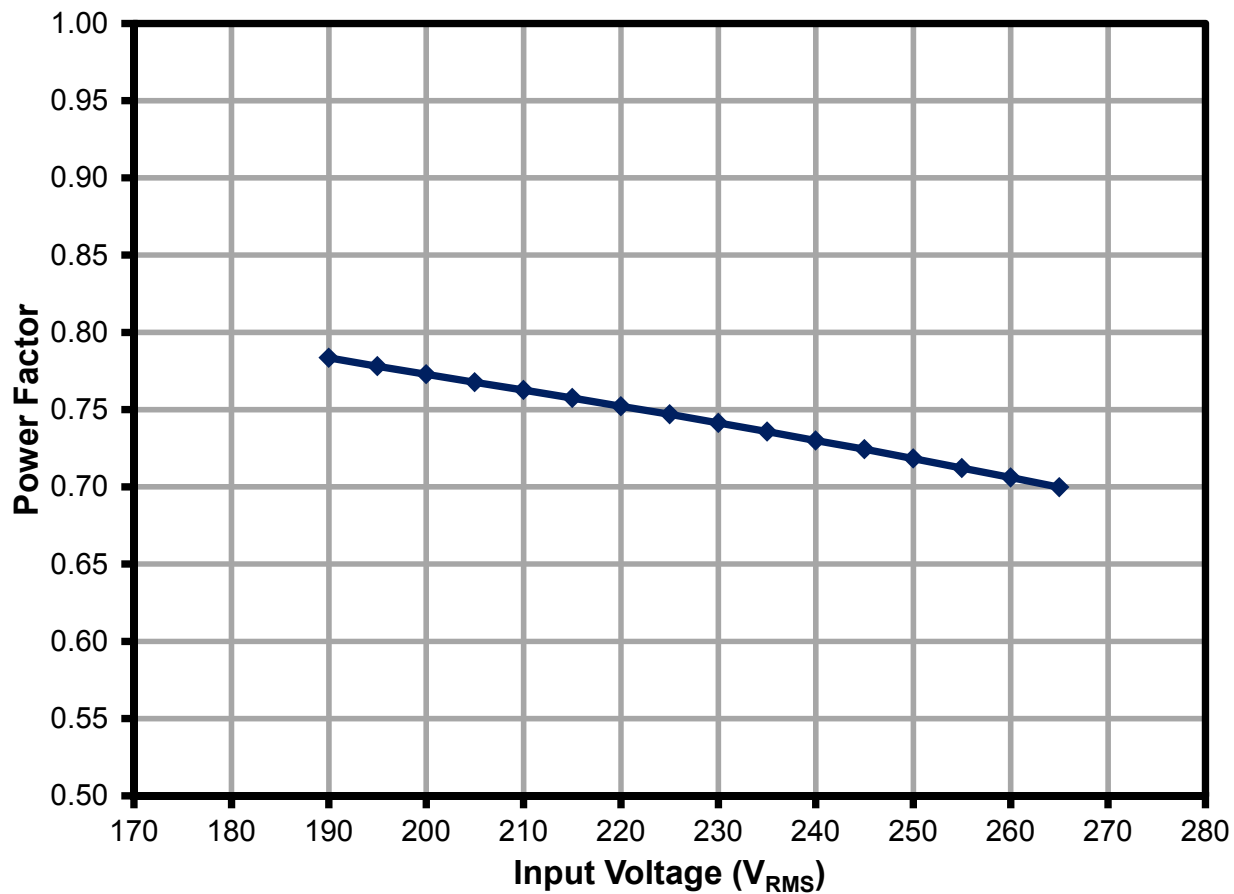


Figure 14 – Power Factor, Full Load.



10.4.4 CV/CC

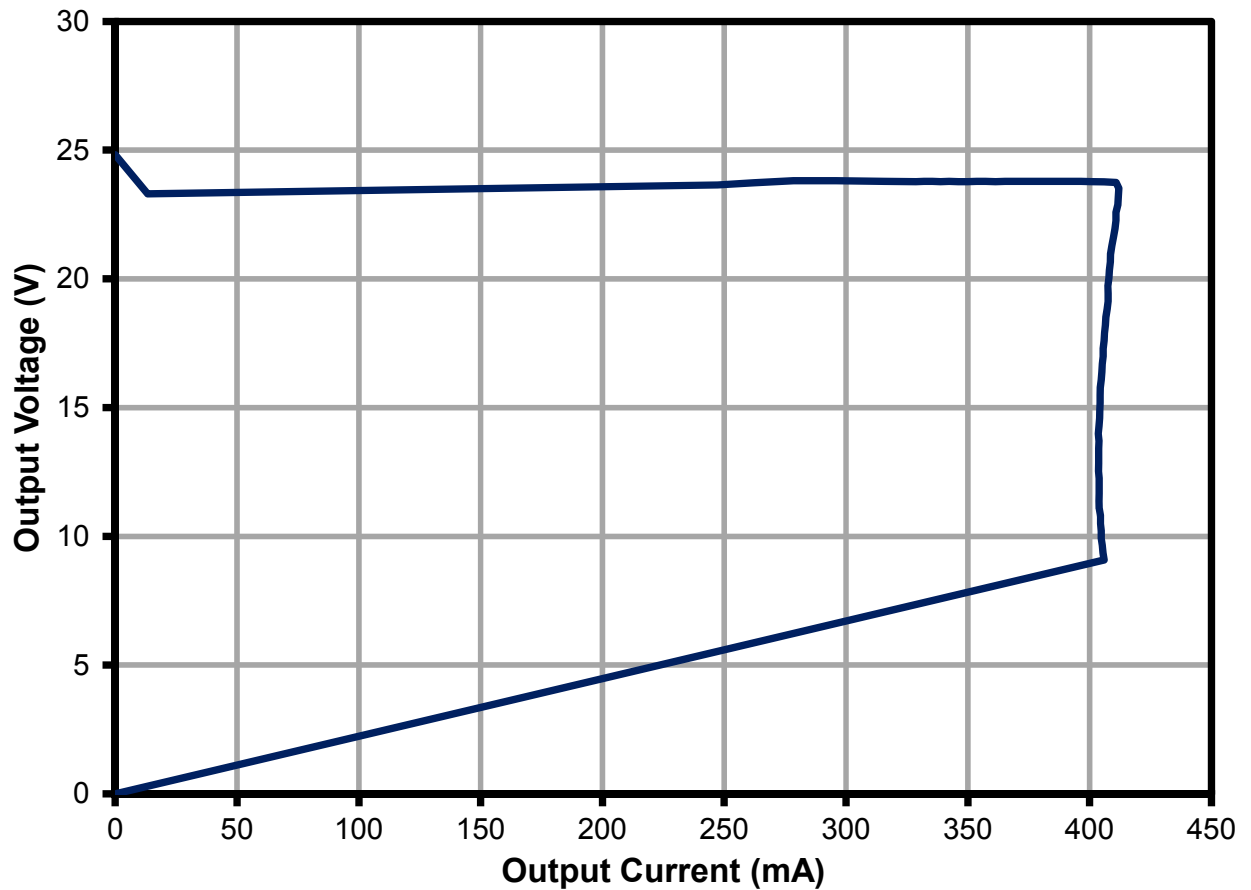
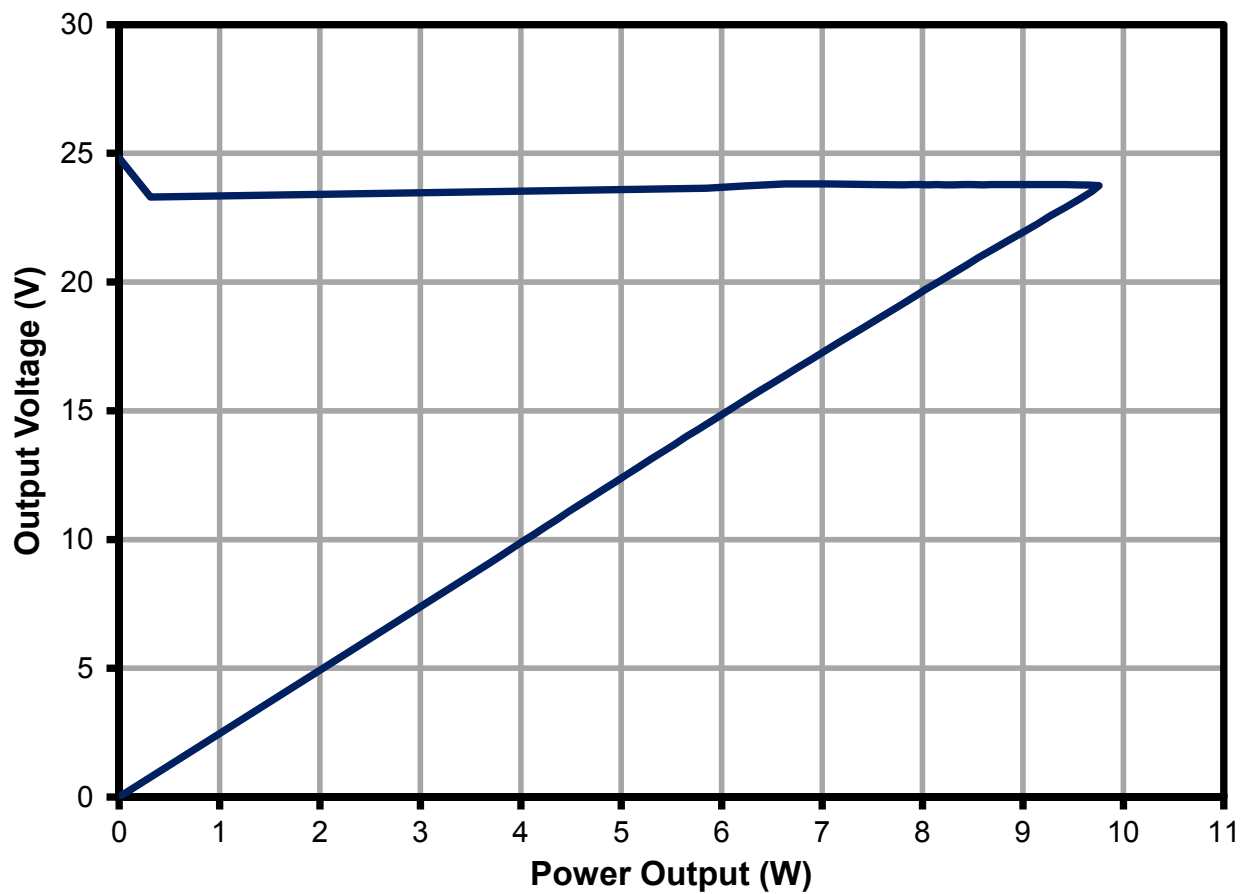


Figure 15 – CV/CC at 230 V / 50 Hz Line Input



10.4.5 Power Curve

**Figure 16** – Power Curve at 230 V / 50 Hz Line Input

11 Thermal Performance

11.1 Thermal Images

Unit was measured open frame (no enclosure). Temperatures were allowed to stabilize prior to making measurements (~30 minutes).

11.1.1 Component Temperatures (190 VAC, 50 Hz, 25 °C)

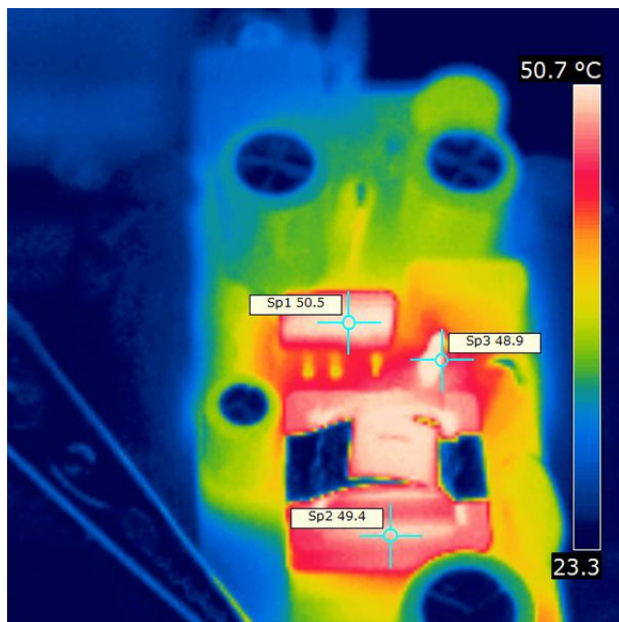


Figure 17 – SP1 – LYT2005E (U1).
SP2 – Series Snubber Resistor (R4).
SP3 – Transformer (T1)

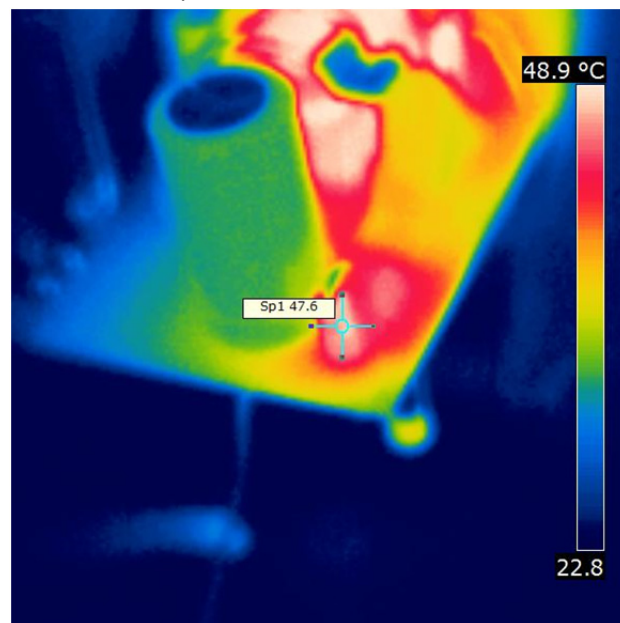


Figure 18 – SP1 – Output Diode (D11).

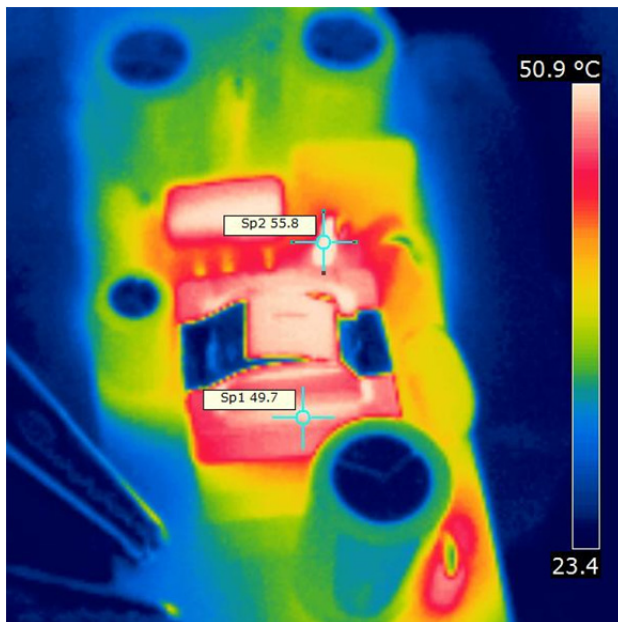


Figure 19 – SP1 – Transformer (T1).
SP2 – Series Snubber Resistor (R4).

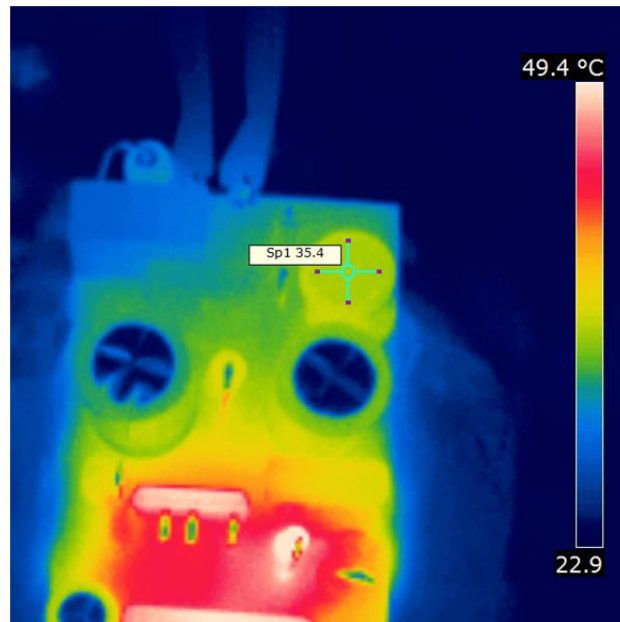


Figure 20 – SP1 – Common Mode Choke (L1).

11.1.2 Component Temperatures (265 VAC, 50 Hz, 25 °C)

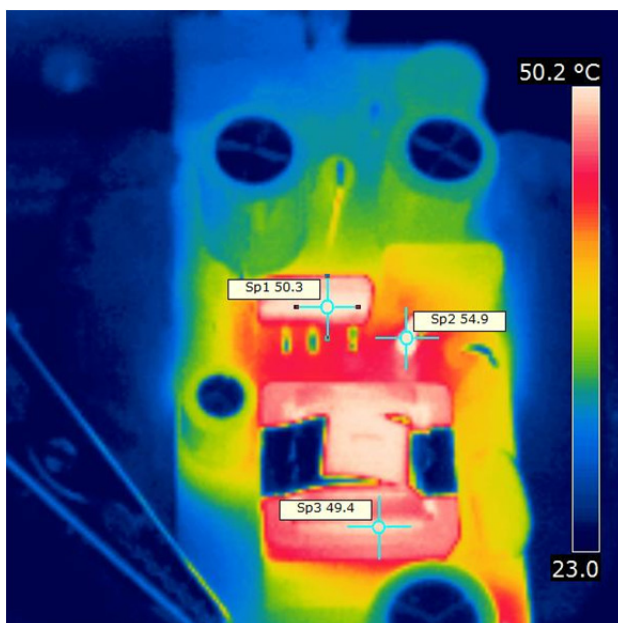


Figure 21 – SP1 – LYT2005E (U1).
SP2 – Series Snubber Resistor (R4).
SP3 – Transformer (T1).

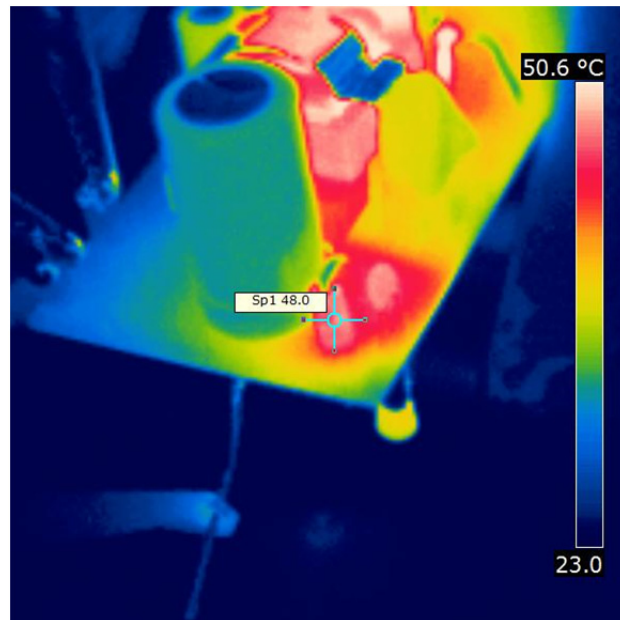


Figure 22 – SP1 – Output Diode (D11).

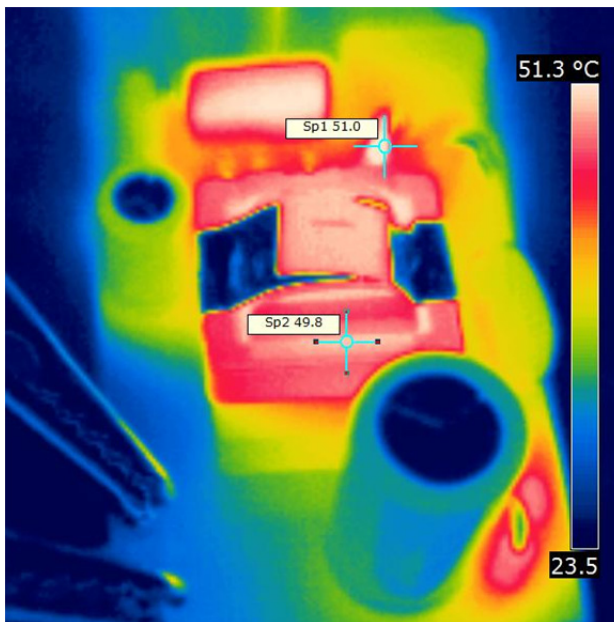


Figure 23 – SP1 – Transformer (T1).
SP2 – Series Snubber Resistor (R4).

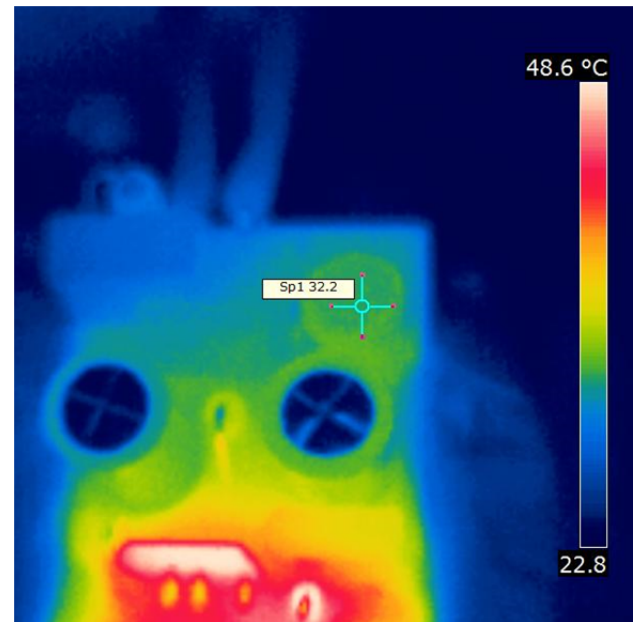


Figure 24 – SP1 – Common Mode Choke (L1).

12 Waveforms

12.1 Input Voltage and Current, Normal Operation

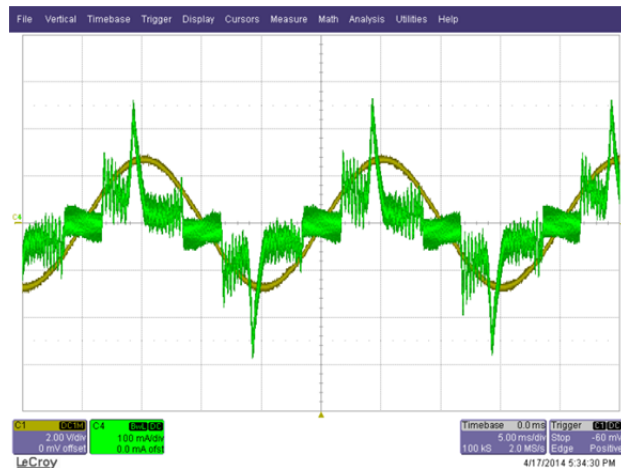


Figure 25 – 190 VAC, Full Load.
Green: I_{IN} , 0.1 A / div.
Yellow: V_{DIN} , 200 V, 5 ms / div.

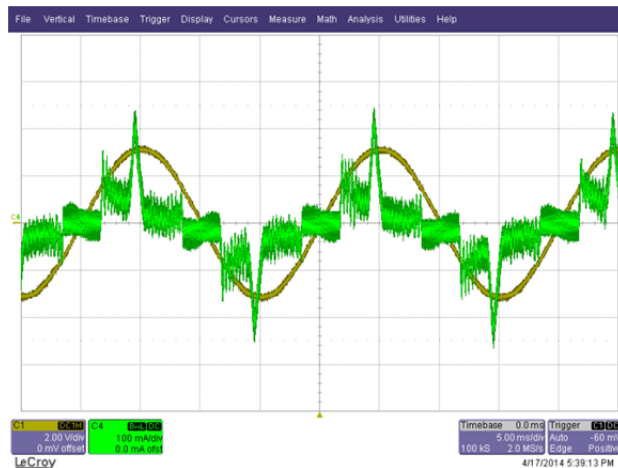


Figure 26 – 220 VAC, Full Load.
Green: I_{IN} , 0.1 A / div.
Yellow: V_{DIN} , 100 V, 5 ms / div.

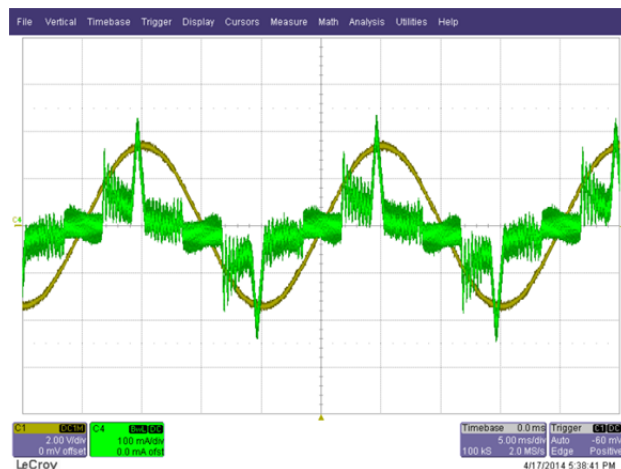


Figure 27 – 240 VAC, Full Load.
Green: I_{IN} , 0.1 A / div.
Yellow: V_{DIN} , 100 V, 5 ms / div.

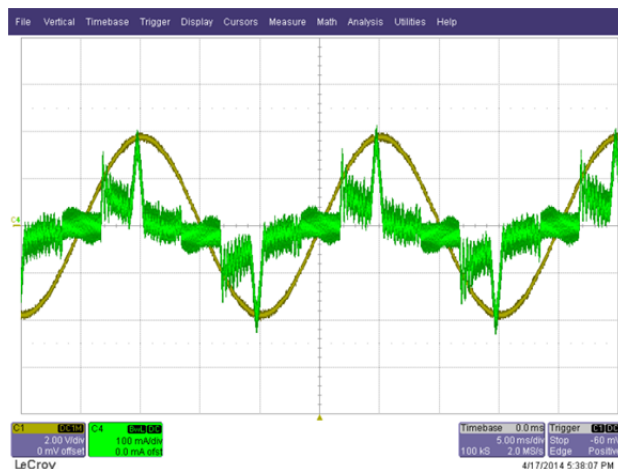


Figure 28 – 265 VAC, Full Load.
Green: I_{IN} , 0.1 A / div.
Yellow: V_{DIN} , 100 V, 5 ms / div.

12.2 Drain Voltage and Current, Normal Operation

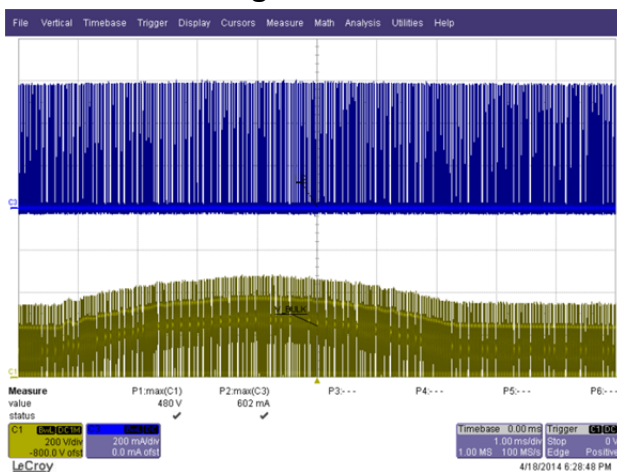


Figure 29 – 190 VAC, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V, 1 ms / div.

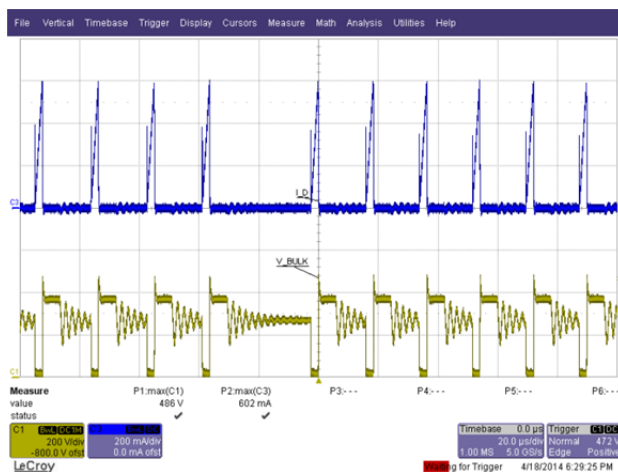


Figure 30 – 190 VAC, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 20 μs / div.

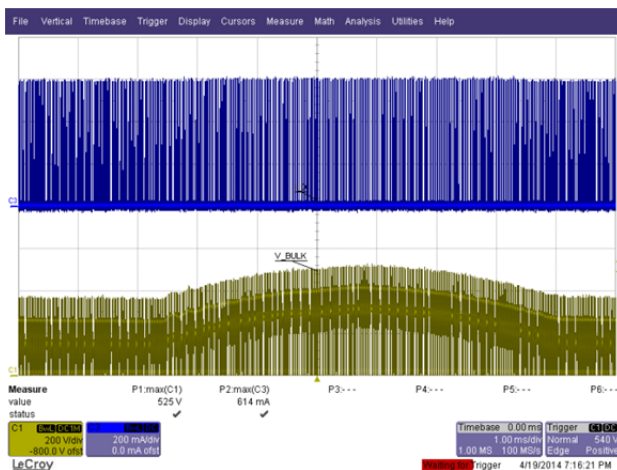


Figure 31 – 220 VAC, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V, 1 ms / div.

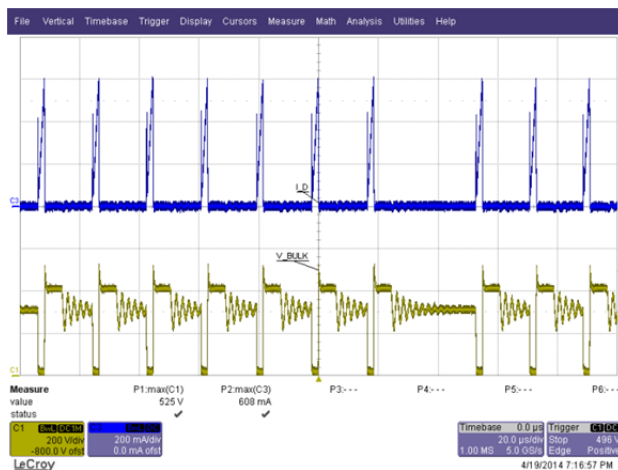


Figure 32 – 220 VAC, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 20 μs / div.

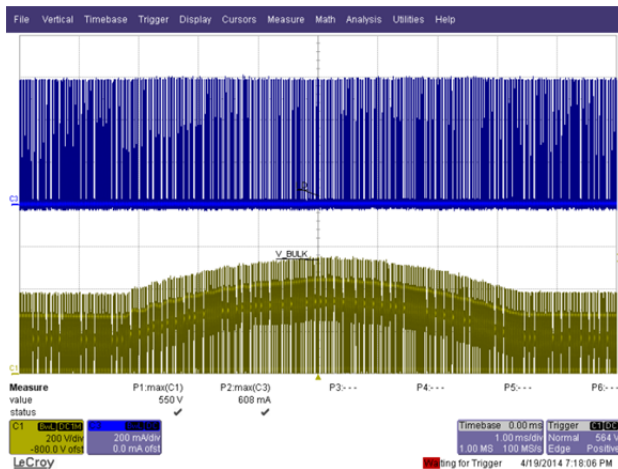


Figure 33 – 240 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.

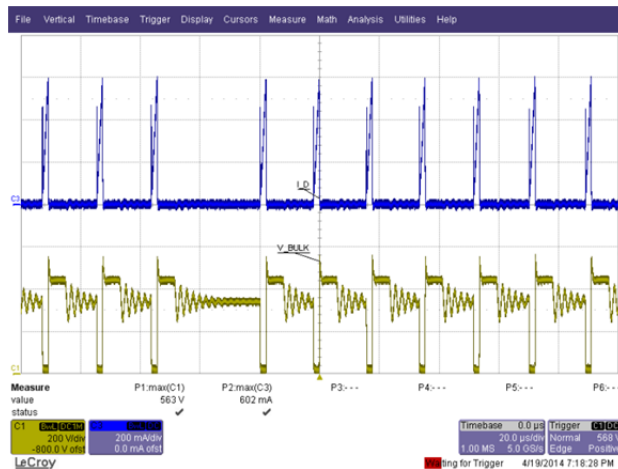


Figure 34 – 240 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 20 μ s / div.

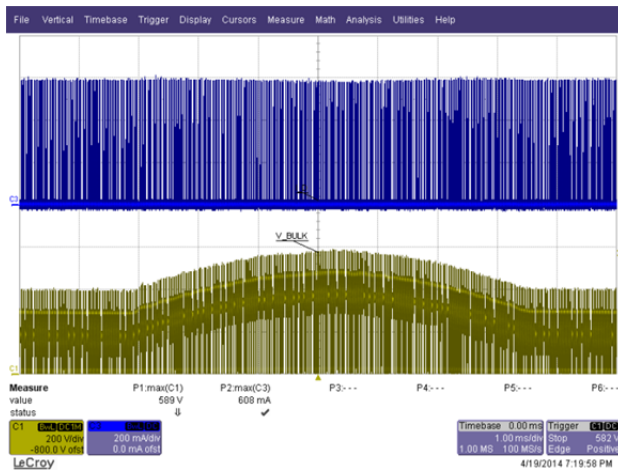


Figure 35 – 265 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.

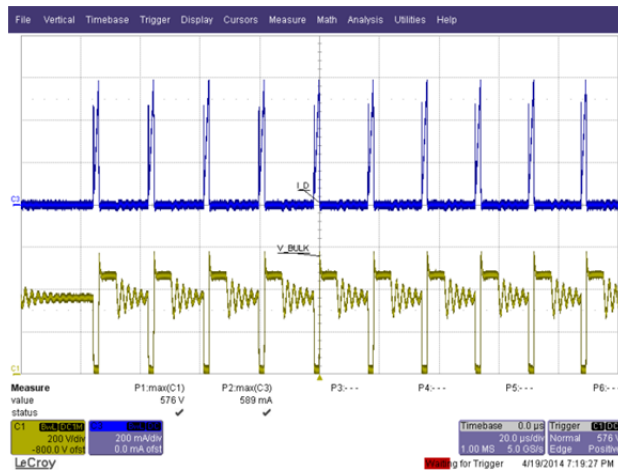


Figure 36 – 265 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 20 μ s / div.

12.3 Drain Voltage and Current Start-up Profile

No indication of saturation or any possible cause of failure was noted in the waveforms.

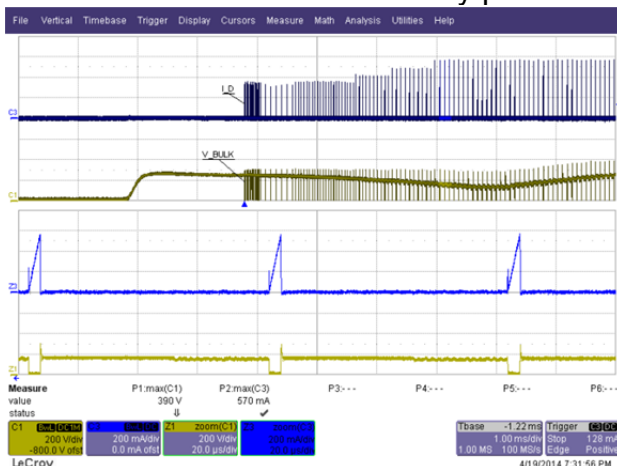


Figure 37 – 190 VAC Input and Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 1 ms / div.
Zoom Time Scale: 20 μ s / div

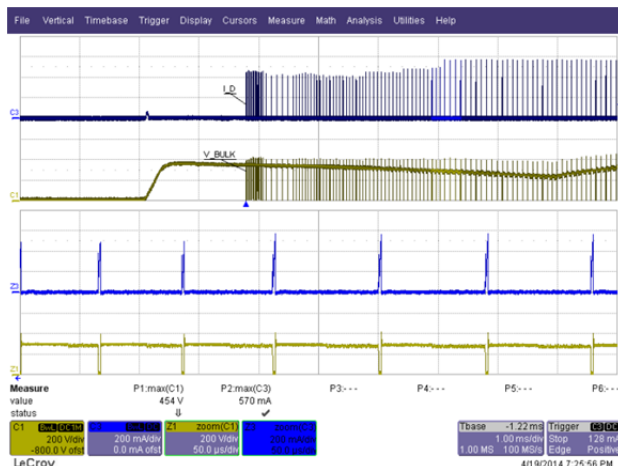


Figure 38 – 265 VAC Input and Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 1 ms / div.
Zoom Time Scale: 50 μ s / div.

12.4 Drain Voltage and Current Start-up Short Waveform

No indication of saturation or any possible cause of failure was noted in the waveforms.

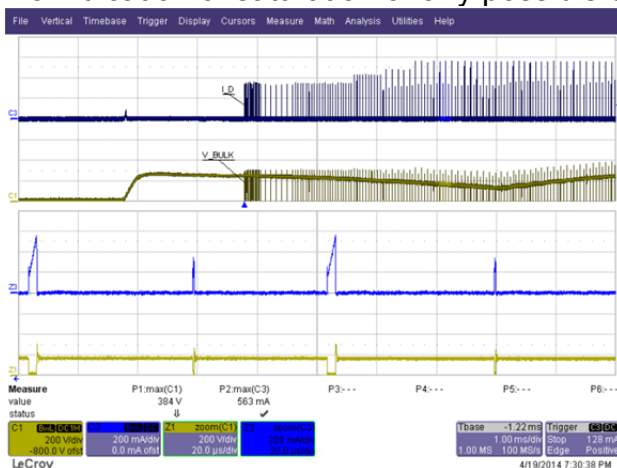


Figure 39 – 190 VAC Input and Shorted Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 1 ms / div.
Zoom Time Scale: 20 μ s / div.

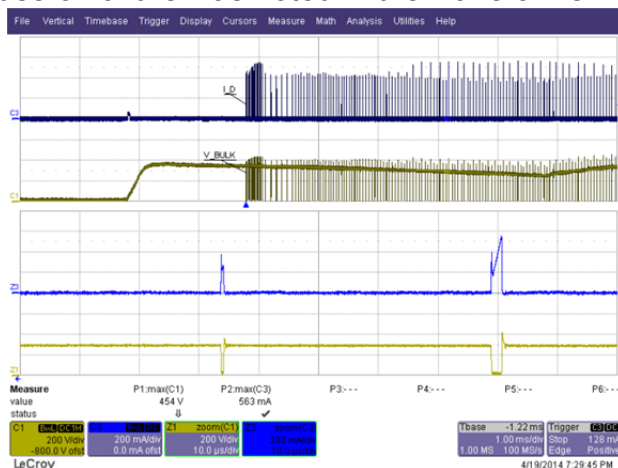


Figure 40 – 265 VAC Input and Shorted Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 1 ms / div.
Zoom Time Scale: 10 μ s / div.



12.5 Drain Voltage and Current Normal Running; Output Shorted Waveform

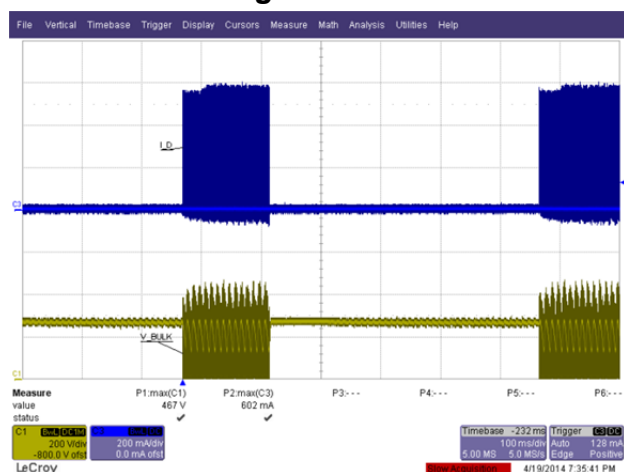


Figure 41 – 190 VAC Input, Full Load then Short.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 100 ms / div.

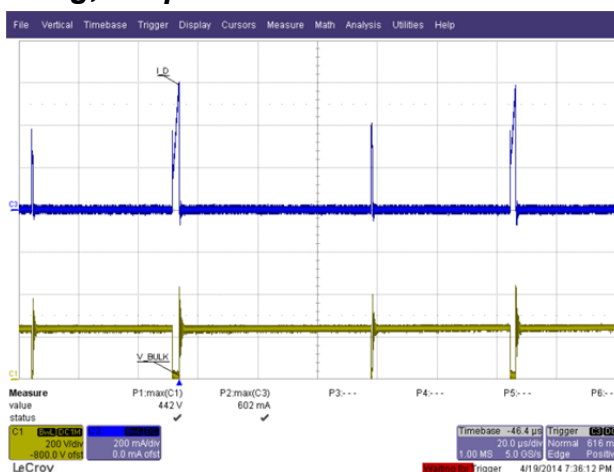


Figure 42 – 190 VAC Input, Full Load then Short.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 20 μ s / div.

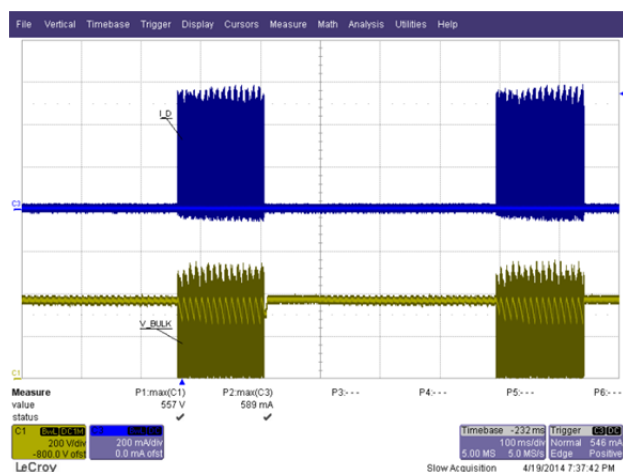


Figure 43 – 265 VAC Input and Full Load then Short.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 100 ms / div.

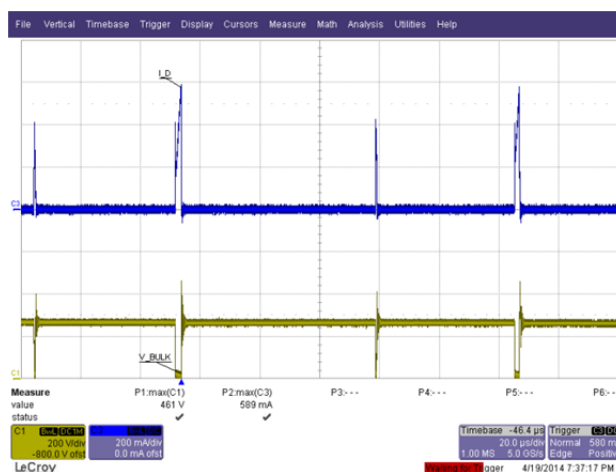


Figure 44 – 265 VAC Input and Full Load then Short.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 200 V / div.
Time Scale: 20 μ s / div.

12.6 Output Diode Waveform in Normal Operation



Figure 45 – 190 VAC Input and Full Load.
Upper: V_{DIODE} , 0.2 A / div.
Lower, Zoom: V_{DIODE} , 20 V / div.
Time Scale: 2 ms / div.
Zoom Time Scale: 5 μ s / div.

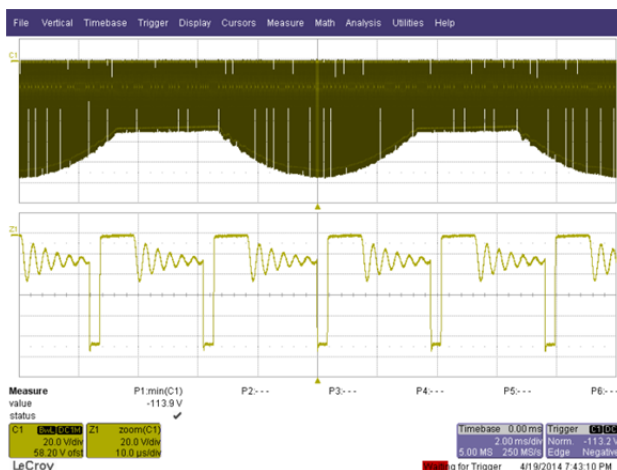


Figure 46 – 265 VAC Input and Full Load.
Upper: V_{DIODE} , 0.2 A / div.
Lower, Zoom: V_{DIODE} , 20 V / div.
Time Scale: 2 ms / div.
Zoom Time Scale: 5 μ s / div.

12.7 Output Voltage Start-up Profile

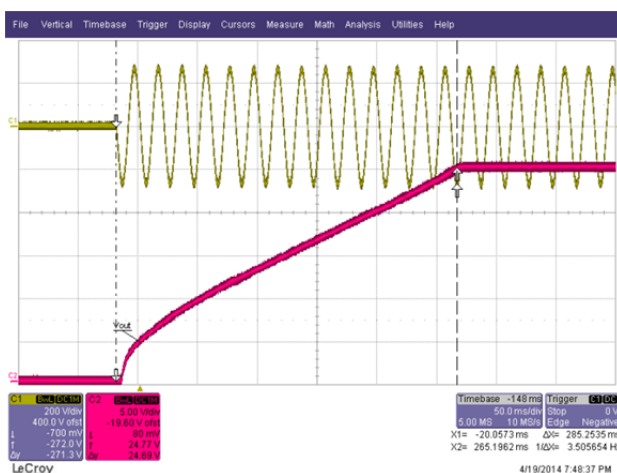


Figure 47 – Start-up Profile, 190 VAC.
Upper: V_{IN} , 200 V / div.
Lower: V_{OUT} , 5 V / div.
Time Scale: 50 ms / div.

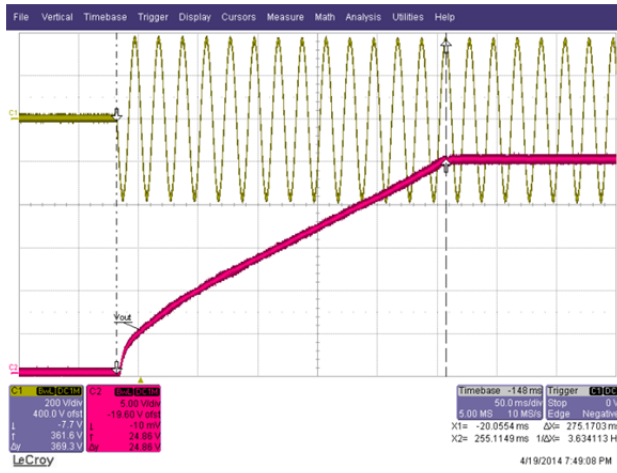


Figure 48 – Start-up Profile, 265 VAC.
Upper: V_{IN} , 200 V / div.
Lower: V_{OUT} , 5 V / div.
Time Scale: 50 ms / div.

12.8 Load Transient Response (0% to 100% Load Step)

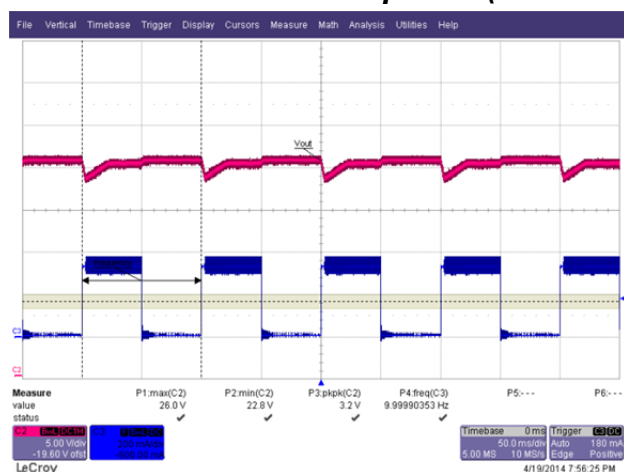


Figure 49 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 10 Hz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 50 ms / div.

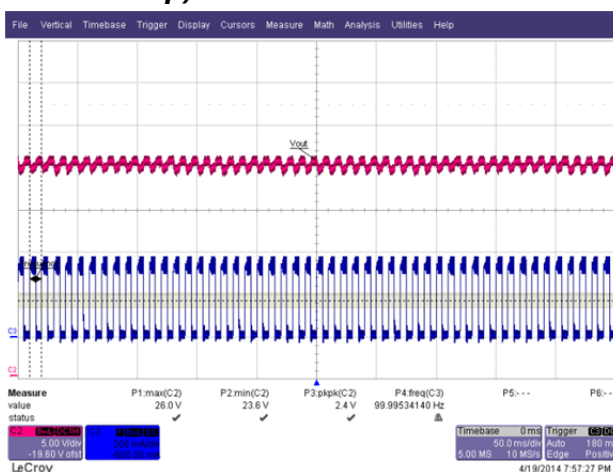


Figure 50 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 100 Hz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 50 ms / div.

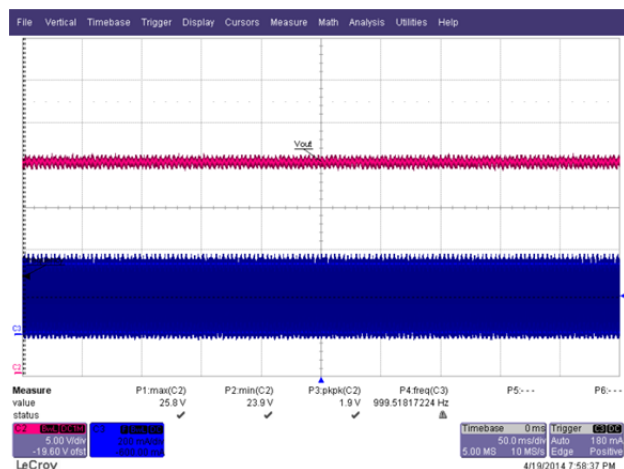


Figure 51 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 50 ms / div.

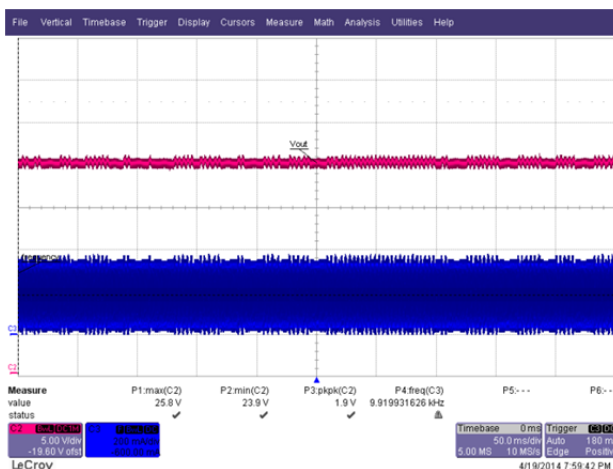


Figure 52 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 10 kHz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 50 ms / div.



12.9 Brown-out Test

No component failure was observed.

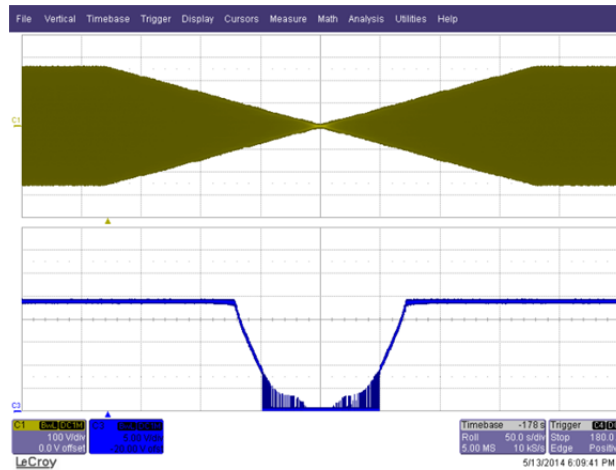


Figure 53 – Brown-out at 1 V / div.
Upper: V_{IN} , 100 V / div.
Lower: V_{OUT} , 5 V / div.
Time Scale: 50 s / div.

12.10 Output Ripple Measurements

12.10.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF /50 V ceramic type and one (1) 1.0 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

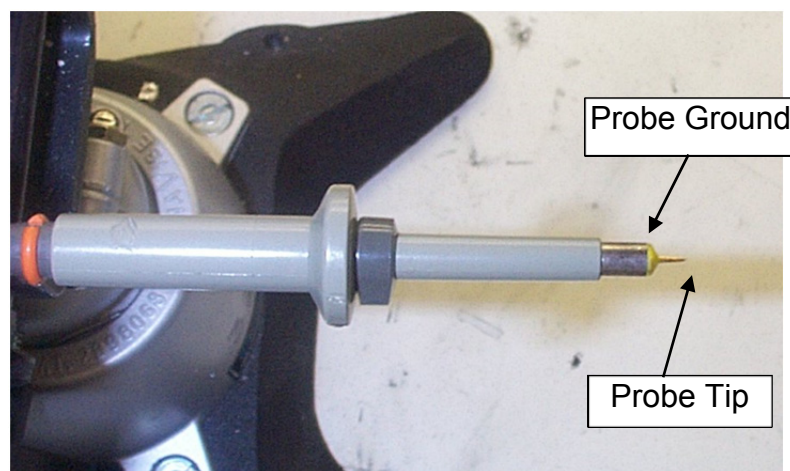


Figure 54 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

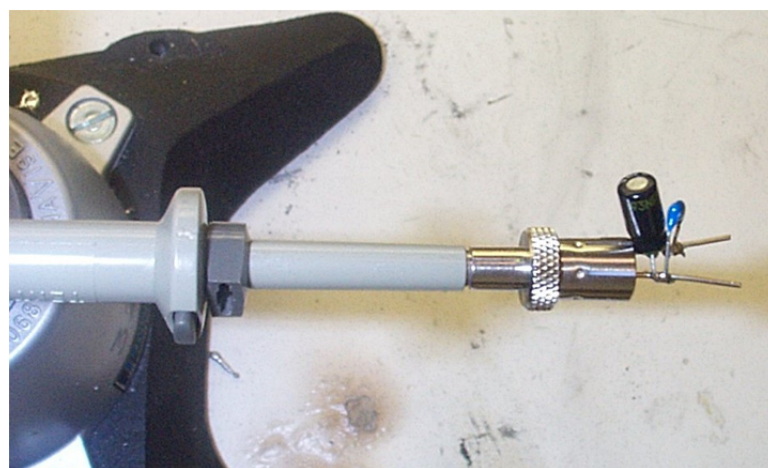


Figure 55 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.10.2 Measurement Results

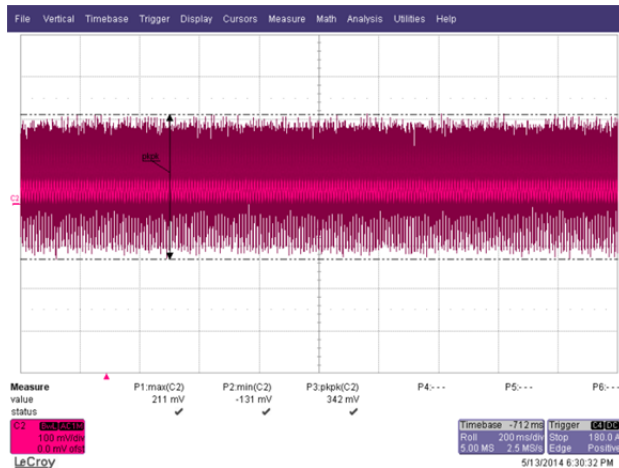


Figure 56 – Ripple, 230 VAC, Full Load.
 $V_{OUT} = 100 \text{ mV} / \text{div.}$
 Time Scale: 200 ms.

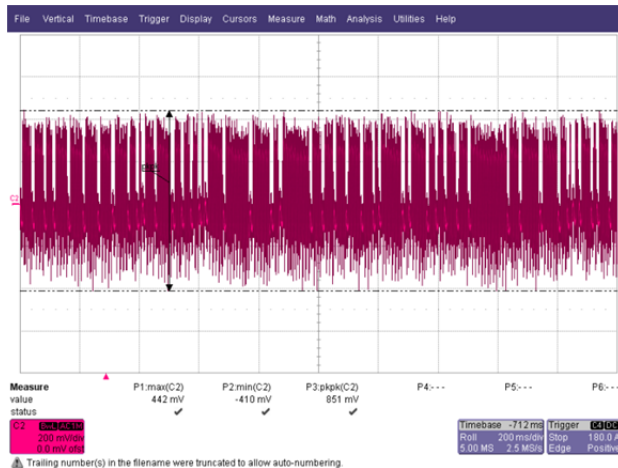


Figure 57 – Ripple, 230 VAC, Half Load.
 $V_{OUT} = 200 \text{ mV} / \text{div.}$
 Time Scale: 200 ms.

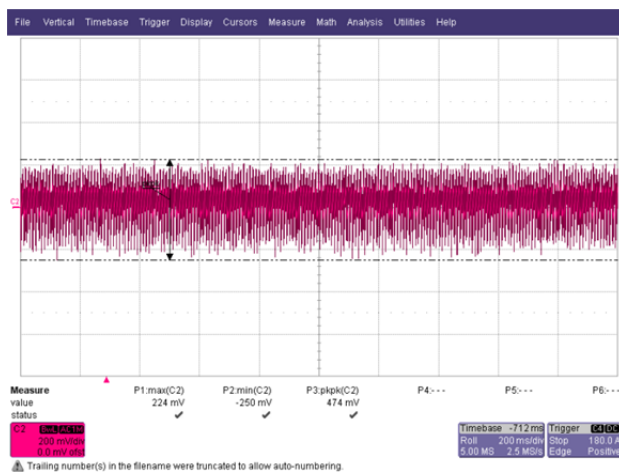


Figure 58 – Ripple, 230 VAC, Quarter Load.
 $V_{OUT} = 200 \text{ mV} / \text{div.}$
 Time Scale: 200 ms.

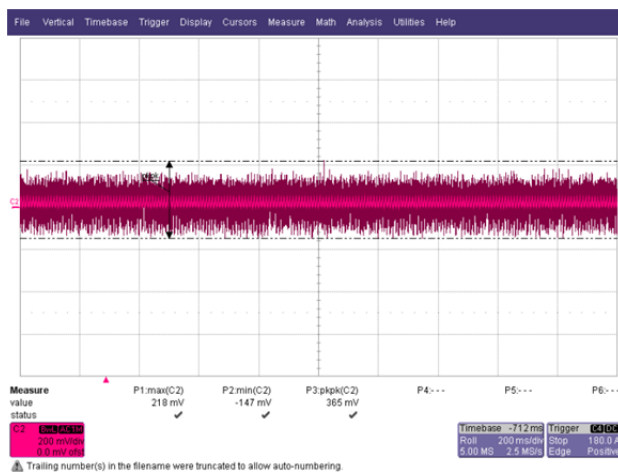


Figure 59 – Ripple, 230 VAC, Eighth Load.
 $V_{OUT} = 200 \text{ mV} / \text{div.}$
 Time Scale: 200 ms.

13 Line Surge

Differential input line 1.2/50 μ s surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+250	230	L to N	90	Pass
-250	230	L to N	90	Pass
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass
+750	230	L to N	90	Pass
-750	230	L to N	90	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

Unit passes under all test conditions.

Differential ring input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	90	Pass
-25000	230	L to N	90	Pass
+2500	230	L to N	0	Pass
-25000	230	L to N	0	Pass

Unit passes under all test conditions.



13.1 Surge Waveforms

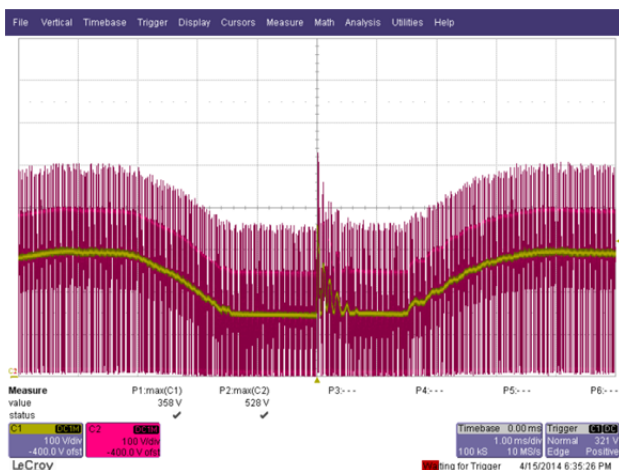


Figure 60 – Ring Surge of 2.5 kV, 230 VAC at 0°. Yellow: V_{BULK} , 100 V / div. Red: V_{DS} , 100 V / div. Time Scale: 1 ms / div.

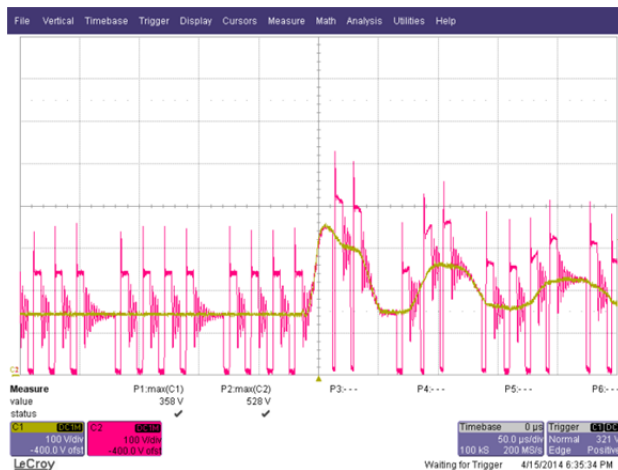


Figure 61 – Ring Surge of 2.5 kV, 230 VAC at 0°. Yellow: V_{BULK} , 100 V / div. Red: V_{DS} , 100 V / div. Time Scale: 50 μs / div.

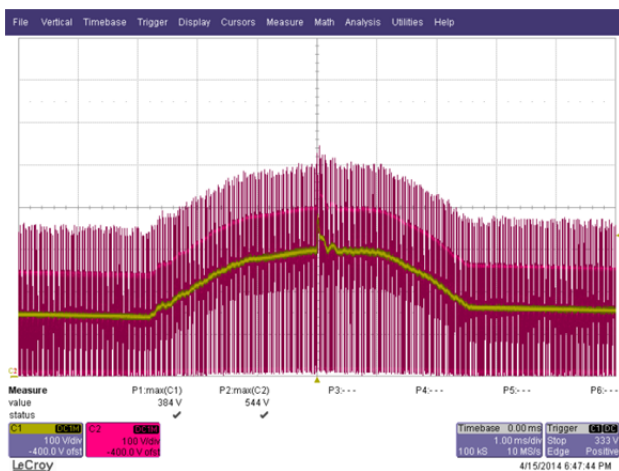


Figure 62 – Ring Surge of 2.5 kV, 230 VAC at 90°. Yellow: V_{BULK} , 100 V / div. Red: V_{DS} , 100 V / div. Time Scale: 1 ms / div.

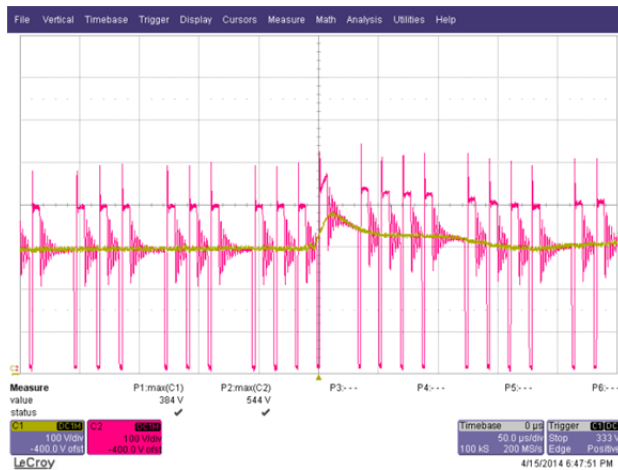


Figure 63 – Ring Surge of 2.5 kV, 230 VAC at 90°. Yellow: V_{BULK} , 100 V / div. Red: V_{DS} , 100 V / div. Time Scale: 50 μs / div.

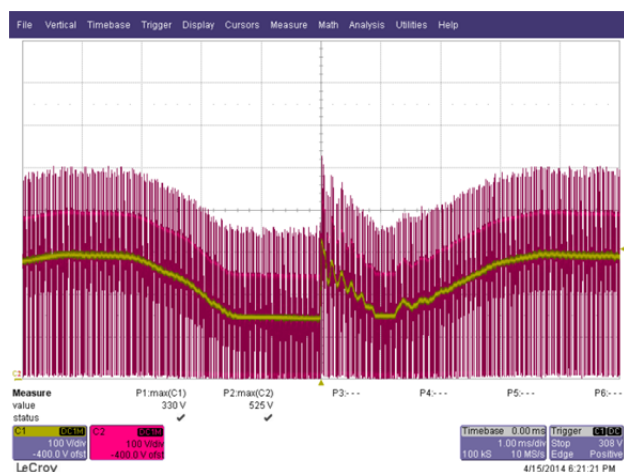


Figure 64 – Differential Surge of 2.5 kV, 230 VAC at 0°.
 Yellow: V_{BULK} , 100 V / div.
 Red: V_{DS} , 100 V / div.
 Time Scale: 1 ms / div.

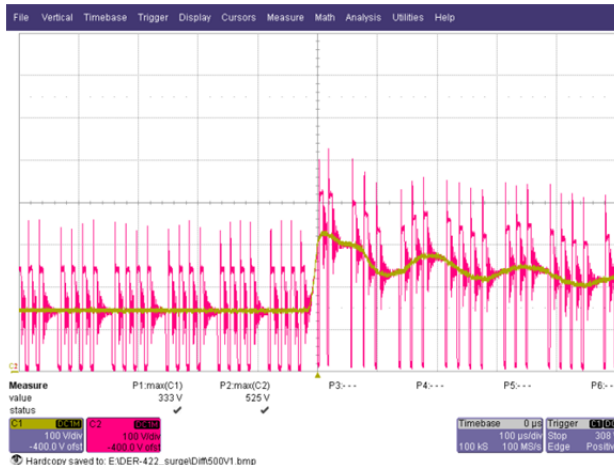


Figure 65 – Differential Surge of 2.5 kV, 230 VAC at 0°.
 Yellow: V_{BULK} , 100 V / div.
 Red: V_{DS} , 100 V / div.
 Time Scale: 1 ms / div.

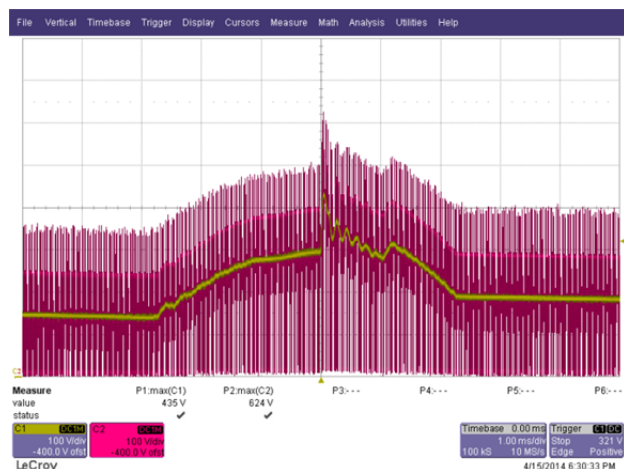


Figure 66 – Differential Surge of 2.5 kV, 230 VAC at 90°.
 Yellow: V_{BULK} , 100 V / div.
 Red: V_{DS} , 100 V / div.
 Time Scale: 1 ms / div.



Figure 67 – Differential Surge of 2.5 kV, 230 VAC at 90°.
 Yellow: V_{BULK} , 100 V / div.
 Red: V_{DS} , 100 V / div.
 Time Scale: 1 ms / div.

14 Conducted EMI



Power Integrations
17.Apr 14 16:39

RBW 9 kHz
MT 500 ms

Att 10 dB AUTO

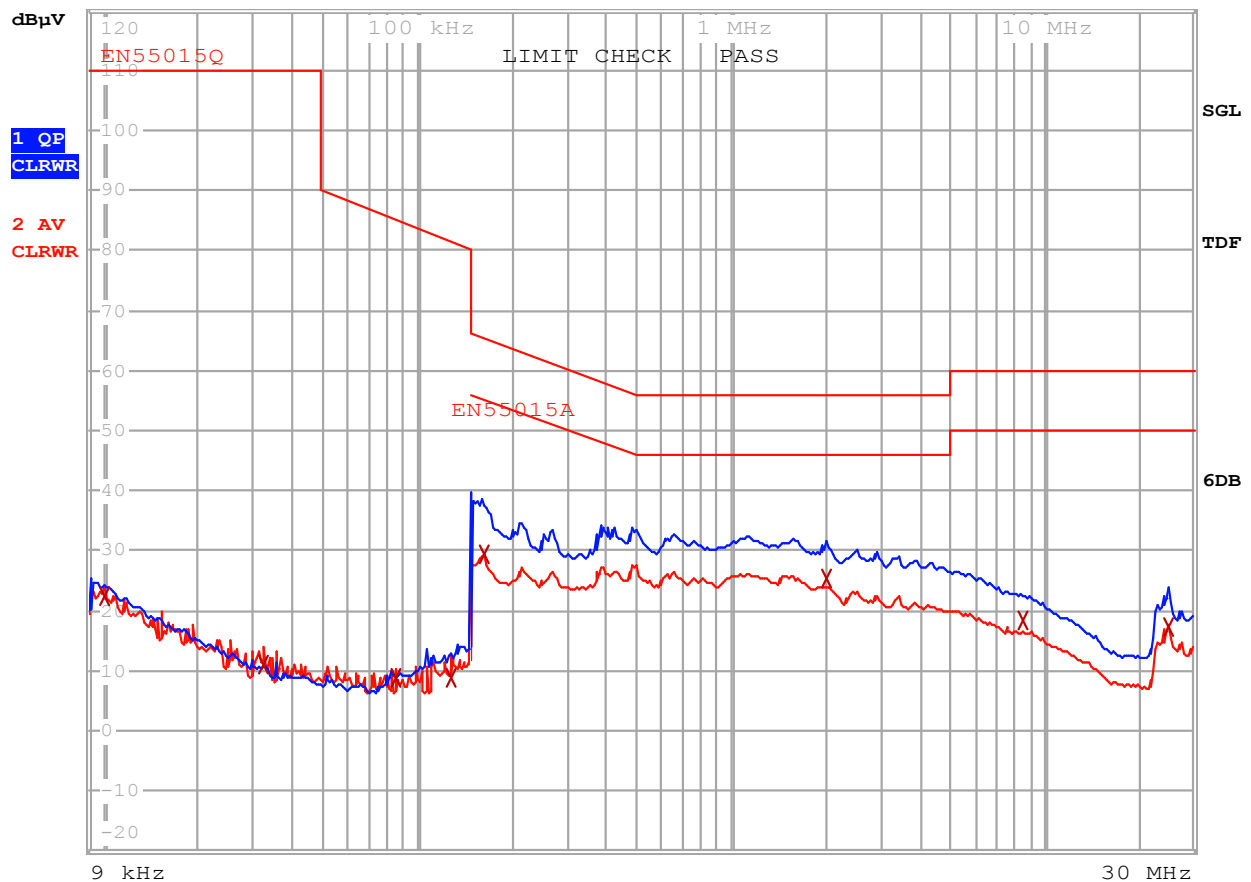


Figure 27 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane.



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q

Trace2: EN55015A

Trace3: ---

	TRACE	FREQUENCY	LEVEL	dB μ V		DELTA LIMIT	dB
2	Average	9.9415991287 kHz	22.52	L1 gnd			
2	Average	31.8461531877 kHz	10.96	L1 gnd			
2	Average	84.4406583237 kHz	8.67	N gnd			
2	Average	126.977840157 kHz	8.72	N gnd			
2	Average	162.428505844 kHz	29.46	N gnd		-25.87	
2	Average	2.03372014292 MHz	25.31	N gnd		-20.68	
2	Average	8.52253934396 MHz	18.25	N gnd		-31.74	
2	Average	24.9618853035 MHz	17.43	L1 gnd		-32.56	

Table 4 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane.





Figure 27 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane that is Connected to Earth.



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q

Trace2: EN55015A

Trace3: ---

	TRACE	FREQUENCY	LEVEL dBμV	DELTA LIMIT dB
2	Average	9.1809 kHz	23.46 N gnd	
2	Average	22.2580710126 kHz	13.06 L1 gnd	
2	Average	35.5297450746 kHz	11.69 L1 gnd	
2	Average	145.957752913 kHz	13.99 N gnd	
2	Average	160.820302816 kHz	36.23 N gnd	-19.18
1	Quasi Peak	221.118376275 kHz	47.03 N gnd	-15.73
1	Quasi Peak	267.135089486 kHz	47.38 N gnd	-13.82
2	Average	267.135089486 kHz	38.63 N gnd	-12.57
1	Quasi Peak	401.705024172 kHz	49.10 N gnd	-8.71
2	Average	500.008614528 kHz	40.76 N gnd	-5.23
1	Quasi Peak	2.03372014292 MHz	46.35 N gnd	-9.64
2	Average	2.03372014292 MHz	37.32 N gnd	-8.67
2	Average	8.95727450287 MHz	32.27 N gnd	-17.73
2	Average	29.8580960942 MHz	15.21 N gnd	-34.79

Table 5 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane that is Connected to Earth.



15 Revision History

Date	Author	Revision	Description & changes	Reviewed
14-May-14	JdC	1.0	Initial Release	Apps & Mktg
24-Jul-14	KM	1.1	Updated pictures and graphs.	Apps & Mktg



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