Design Example Report

Title	***92% Efficiency 24 W T10, Non-Isolated, Buck-Boost Topology, Power Factor Corrected, LED Driver Using LinkSwitch™-PH LNK419EG***
Specification	90 VAC – 265 VAC Input; 134 V, 180 mA Output
Application	T10 Tube Lamp LED Driver
Author	Applications Engineering Department
Document Number	DER-356
Date	December 6, 2012
Revision	1.0

Summary and Features

- Dramatically simplifies off-line, power factor corrected, LED driver design
  - Single-stage combined, power factor correction and constant current output, non-isolated LED driver
  - Compact with extremely low component count
  - Eliminates all control loop compensation
  - No output current sensing required
  - High efficiency >92% at 230 VAC
  - High PF >0.95 across line and load
  - Low THD, <25% at 230 VAC
  - IEC61000-3-2 CLASS C compliant
- Advanced performance features
  - Compensates for inductance tolerance
  - Compensates for input voltage variations
  - Compensates for output voltage variations
  - Frequency jittering greatly reduces EMI filter costs
- Advanced protection and safety features
  - Auto-restart protection for short-circuit
  - Hysteretic thermal shutdown

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document describes a non-isolated, power factor corrected, low THD, high-efficiency LED driver designed to drive a ~134 V LED string at 180 mA from an input voltage range of 90 VAC to 265 VAC.

The LinkSwitch-PH has been developed to cost effectively implement a single-stage power factor corrected LED driver combined with a primary-side constant-current control. The LinkSwitch-PH controller is optimized for LED driver applications and requires minimal external parts. It provides control of the output current through the LED load without the use of an optocoupler.

The LinkSwitch-PH monolithically combines the 725 V power MOSFET and controller. The controller consists of an oscillator, PWM, 6 V regulator, over-temperature protection, frequency jittering, cycle-by-cycle current limit and other protection features plus a charge controller for output CC (constant current) control.

The LinkSwitch-PH provides a sophisticated range of additional protection features including auto-restart for control loop open/short faults and output short-circuit conditions. The accurate hysteretic thermal shutdown ensures safe PCB temperatures under all conditions.

The non-isolated power factor corrected buck-boost design presented in this report shows how LinkSwitch-PH dramatically simplifies off-line, high-efficiency, power factor corrected LED driver design with very low parts count and enables an EN 61000-3-2 Class C harmonic current compliant implementation of a very high efficiency, high output voltage design

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, conducted EMI measurements, thermal measurements, inductor documentation and typical performance characteristics.

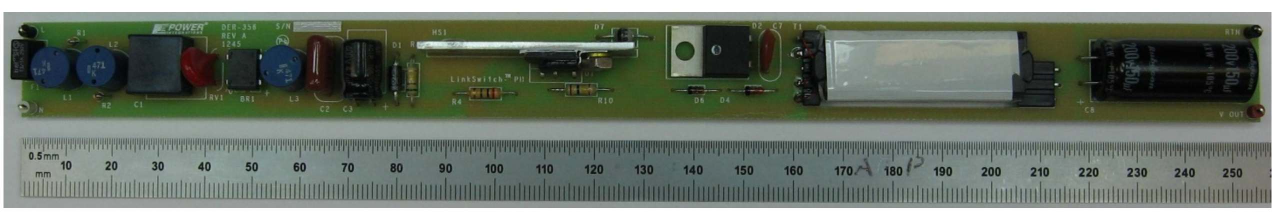

Figure 1 – Populated Circuit Board Photograph.
(L: 10” [254 mm] x W: 0.78” [19.8 mm].
Heat Sink Highest Component: 0.36” [9.14 mm]

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
Output						
LED Voltage	V_{OUT}		134		V	
LED Current			180		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		24		W	
Environmental						
Conducted EMI		Meets EN55015B				
Safety		Non-isolated				
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	
Differential Surge (1.2/50 μs)			500		V	
Efficiency			92		%	Measured at 230 VAC, 25 °C
Harmonic Currents		EN 61000-3-2 Class C				
Power Factor			0.97			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Ambient Temperature	T_{AMB}		40		°C	

3 Schematic

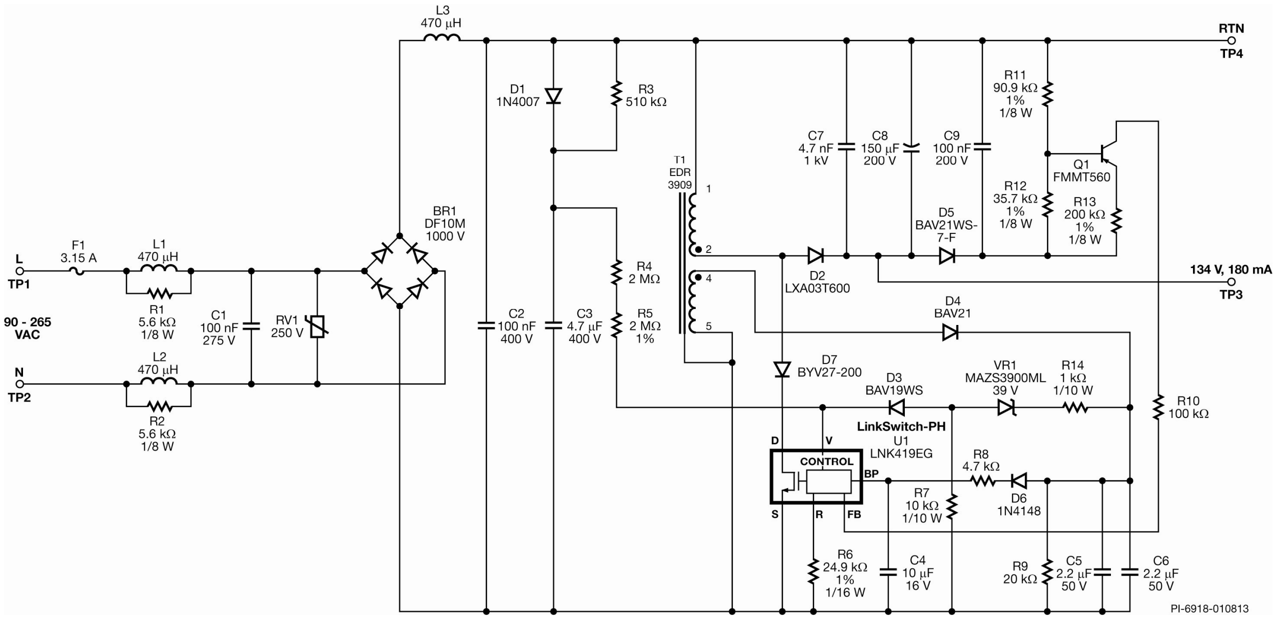

Figure 2 – Schematic.

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4 Circuit Description

The LinkSwitch-PH (U1) is a highly integrated primary-side controller intended for use in LED driver applications. The LinkSwitch-PH provides high power factor in a single-stage conversion topology while regulating the output current across the range of input and output voltage conditions expected in a typical LED driver environment. All of the control circuitry responsible for these functions plus the high-voltage power MOSFET is incorporated into the device.

Capacitor C1, C2, differential chokes L1, L2, and L3 perform EMI filtering and are sized to maintain a high-power factor. Resistor R1 and R2 are used to damp the Q of L1 and L2 to prevent a resonant peak in the EMI spectrum.

The buck-boost power circuit with floating output is composed of U1 (power switch + control), output diode D2, output capacitor C7 and C8, and output inductor T1. Inductor T1 has a second winding configured in flyback configuration to provide a bias supply to U1. Diode D7 was used to prevent negative voltage appearing across drain-source of U1 near the zero-crossing of the input voltage. Diode D1 and C3 detect the peak AC line voltage. The voltage across C3 along with R4 and R5 sets the input current fed into the VOLTAGE MONITOR (V) pin. This current is used by U1 to control line undervoltage (UV), overvoltage (OV), and feed-forward current which in conjunction with the FEEDBACK (FB) pin current provides a constant current to the LED load.

The FB pin current used by U1 for output current regulation is provided by the voltage to current converter network formed by R10, R11, R12, R13, Q1, C9, and D5. Output voltage is related to feedback current by the following equation:

$$I_{FB} \approx I_{R13} = \frac{V_{OUT} \times \frac{R12}{R11 + R12} - V_{BE}}{R13}$$

Voltage across R12 was chosen to eliminate or minimize the effect of temperature and V_{CE} dependence of the V_{BE} voltage of Q1.

Capacitor C4 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C4 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN (D) pin of U1. Capacitor C4 was chosen to be 10 μF to enable the device to operate in full mode. External bias supply was employed (via D6 and R8) to give the lowest device dissipation and provide sufficient supply to U1 during deep dimming condition. Output over-voltage (open load) protection is provided through the V pin and VR1, R14, and D3. Once the voltage across capacitor C6 of the bias supply exceeded VR1 threshold due to open load condition, current will flow to V pin until it reaches Line Overvoltage Threshold (I_{OV}) then the IC will terminate switching immediately thereby preventing the output voltage from rising further.

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5 PCB Layout

Copper: 2 oz. / 70 μm thickness used.

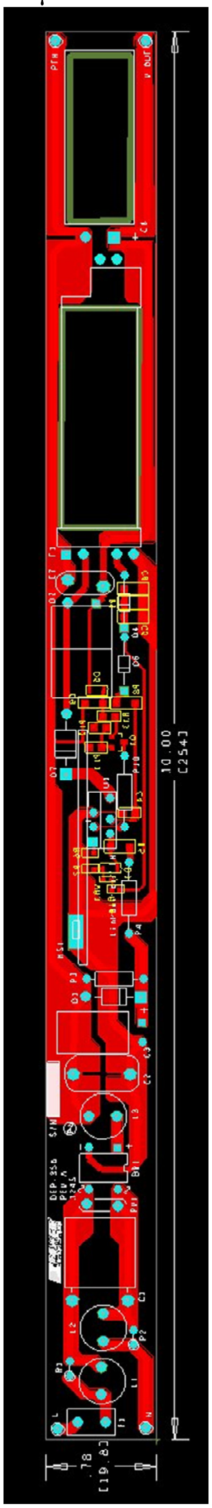

Figure 3 – Printed Circuit Layout, Top and Bottom.

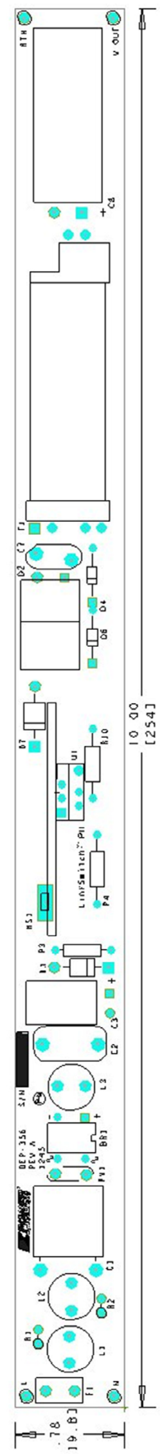

Figure 4 – Printed Circuit Layout, Top.

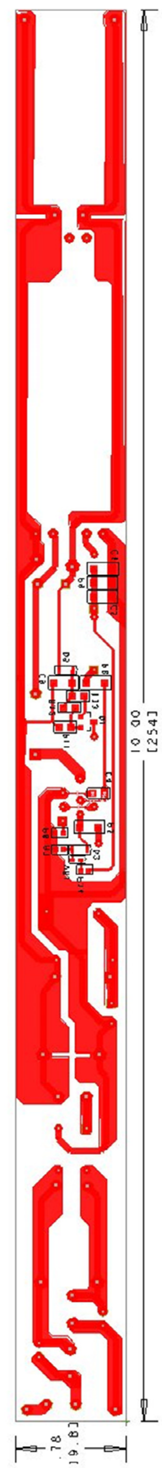

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Electrical BOM

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 1 A, Bridge Rectifier, DF-M, Glass Passivated, 4-EDIP	DF10M	Diodes, Inc.
2	1	C1	100 nF, 275 VAC, Film, X2	LE104-M	OKAYA
3	1	C2	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
4	1	C3	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	SHD400WV 4.7uF	Sam Young
5	1	C4	10 μF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
6	2	C5 C6	2.2 μF, 50 V, Ceramic, Y5V, 1206	GRM31MF51H225ZA01L	Murata
7	1	C7	4.7 nF, 1 kV, Thru Hole, Disc Ceramic	562R5GAD47	Vishay
8	1	C8	150 μF, 200 V, Electrolytic, (12.5 x 30)	200KXW150MEFC12.5X30	Rubycon
9	1	C9	100 nF, 200 V, Ceramic, X7R, 1206	VJ1206Y104KXCAT	Vishay
10	1	D1	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
11	1	D2	600 V, 3 A, TO-220AC	LXA03T600	Power Integrations
12	1	D3	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
13	1	D4	250 V, 250 mA, Fast Switching, DO-35	BAV21	Vishay
14	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
15	1	D6	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
16	1	D7	200 V, 2 A, Ultrafast Recovery, 25 ns, SOD57	BYV27-200-TR	Vishay
17	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
18	1	HS1	Heat Sink, Custom, Al, 3003, 0.062" Thk		Custom
19	3	L1 L2 L3	470 μH, 0.38 A, Radial	TSL0808RA-471KR38-PF	TDK
20	1	Q1	PNP, Small Signal BJT, 500 V, 0.15 A, SOT23	FMMT560TA	Zetex
21	2	R1 R2	5.6 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-5K6	Yageo
22	1	R3	510 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-510K	Yageo
23	1	R4	2.0 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2M0	Yageo
24	1	R5	2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
25	1	R6	24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
26	1	R7	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
27	1	R8	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
28	1	R9	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
29	1	R10	100 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-100K	Yageo
30	1	R11	90.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9092V	Panasonic
31	1	R12	35.7 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3572V	Panasonic
32	1	R13	200 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2003V	Panasonic
33	1	R14	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
34	1	RV1	250 V, 21 J, 7 mm, RADIAL LA	V250LA4P	Littlefuse
35	1	T1	Bobbin, EDR-3909, Horizontal, 8 pins Transformer	 SNX-R1681	SBEF Santronics USA
36	1	U1	LinkSwitch-PH, eSIP	LNK419EG	Power Integrations
37	1	VR1	39 V, 5%, 150 mW, SSMINI-2	MAZS39000L	Panasonic

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7 T1 Transformer Specification

7.1 Electrical Diagram

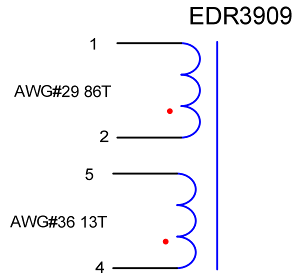

Figure 6 – Electrical Diagram.

7.2 Electrical Specification

Primary Inductance	Pins 1-2, all other windings open, measured at 66 kHz, 0.4 V_{RMS}.	2.8 mH ±2%
Resonant Frequency	Pins 1-2, all other windings open.	1 MHz (Min.)

7.3 Materials

Item	Description
[1]	Core: EDR3909.
[2]	Bobbin: EDR3909, Horizontal, 8 pins, 5/3.
[3]	Magnet Wire: #29 AWG.
[4]	Magnet Wire: #36 AWG.
[5]	Tape: 3M 1298 Polyester Film, 4.5 mm wide.
[6]	Copper Tape: 0.125” wide, 2 mil thick.

7.4 Transformer Build Diagram

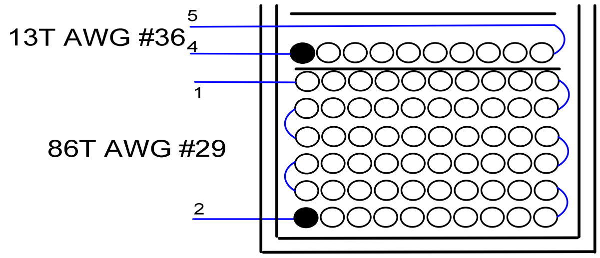

Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Pull-out pin number 3 and 6.
General Note	For the purpose of these instructions, Bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is clockwise.
WDG1 Primary 1	Start at pin 2; wind with firm tension 86 turns of item [3] in 7 layers from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1
Insulation	1 layer of tape [5] for insulation.
WDG2 Bias	Start on pin(s) 4 and wind 13 turns of item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5.
Insulation	2 layers of tape [5] for insulation.
Assemble Core	Assemble and secure the cores.
Flux Band	Construct a flux band by wrapping a single shorted turn of item [6] around the outside of windings and core halves with tight tension. Make an electrical connection to pin(s) 5 using wire. Add 3 layers of tape, item [4], for insulation.
Finish	Varnish transformer assembly.

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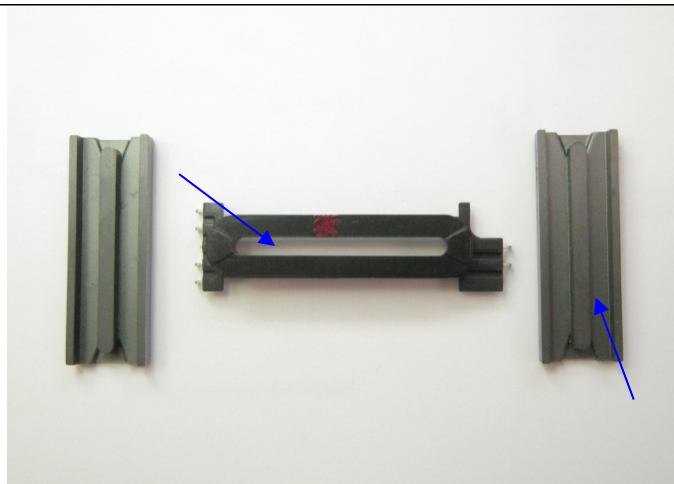
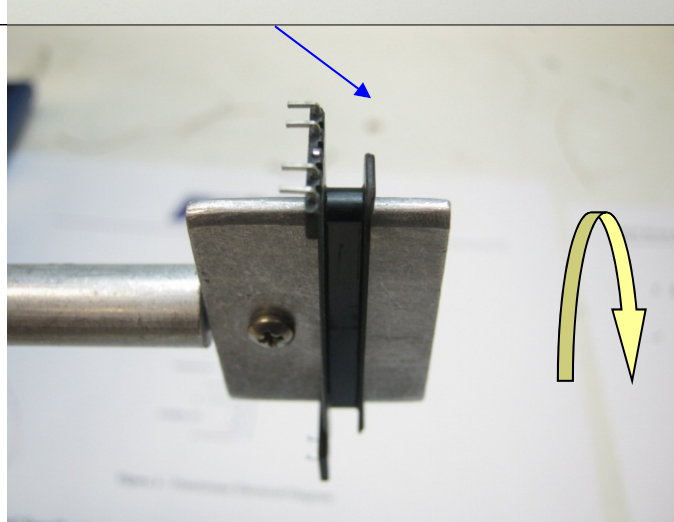
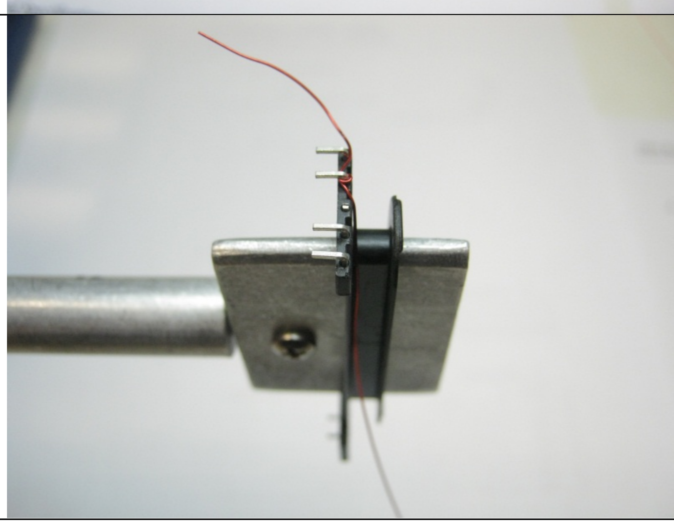
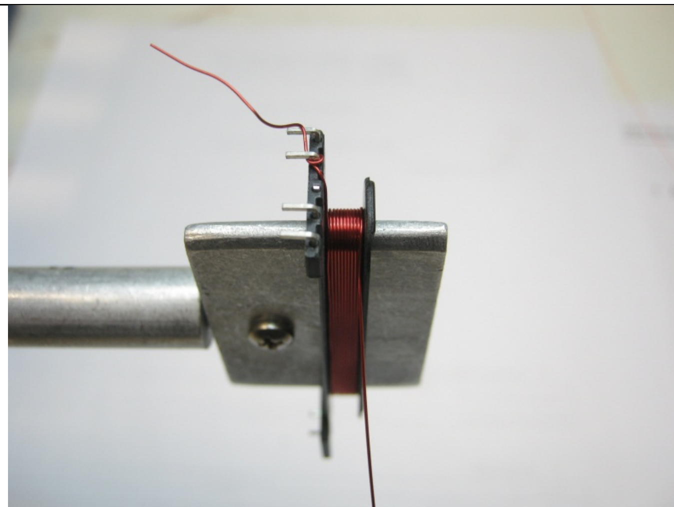
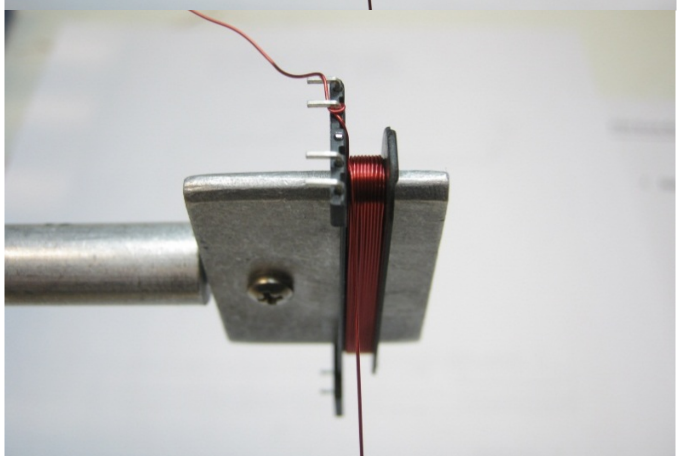
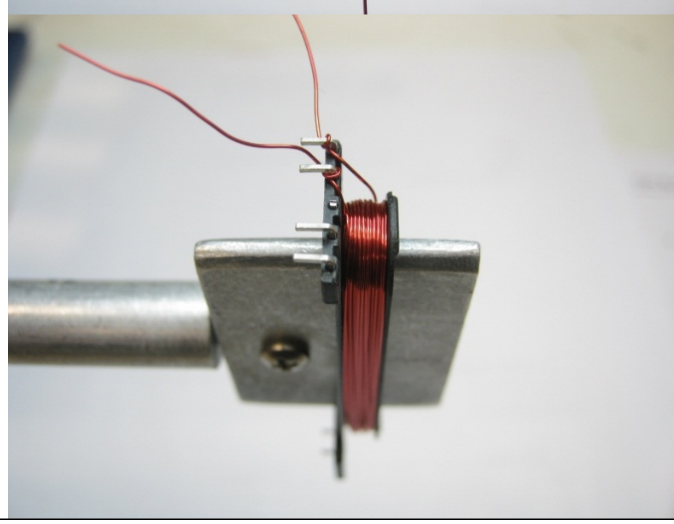
7.6 Transformer Winding Illustrations

Bobbin Preparation		Pull-out pin number 3 and 6.
General Note		For the purpose of these instructions, Bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is clockwise.
WDG1 Primary 1		Start at pin 2; wind with firm tension 86 turns of item [3] in 7 layers from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1

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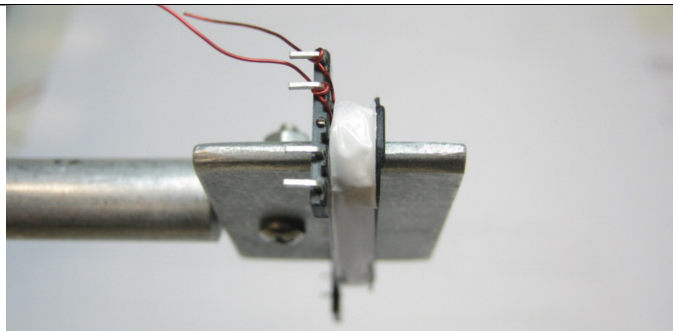
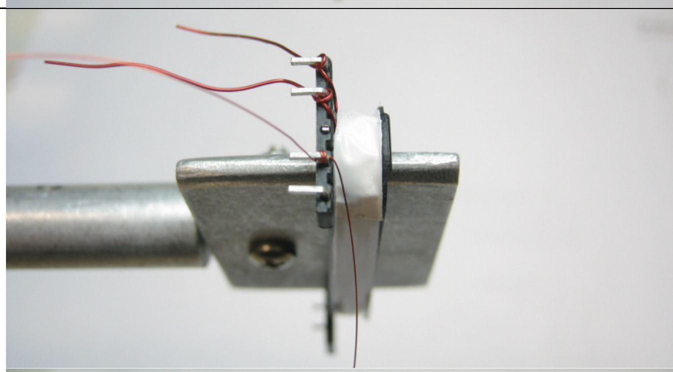
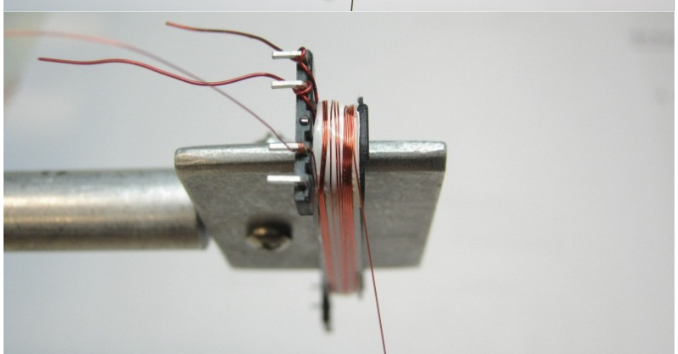
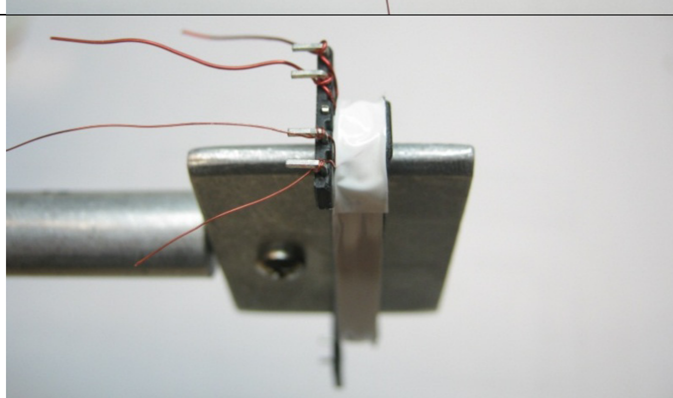
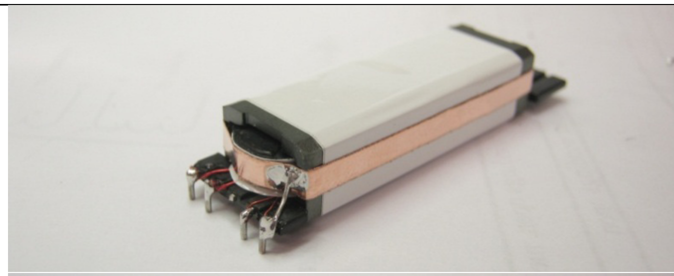
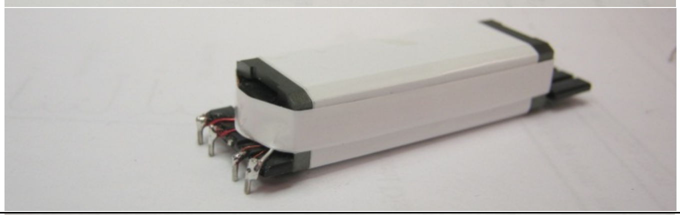
Insulation		1 layer of tape [5] for insulation.
WDG2 Bias	 	Start on pin(s) 4 and wind 13 turns of item [4]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5.
Insulation		1 layer of tape [5] for insulation.
Assemble Core		Assemble and secure the cores.

Flux Band	 	Construct a flux band by wrapping a single shorted turn of item [6] around the outside of windings and core halves with tight tension. Make an electrical connection to pin(s) 5 using wire. Add 3 layers of tape, item [4], for insulation.
Finish		Varnish transformer assembly.

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8 Inductor Design Spreadsheet

Buck-boost inductor parameters can be calculated using LinkSwitch-PH PIXls spreadsheet using VO ≡ VOR.

ACDC_LinkSwitch-PH_071112; Rev.1.8; Copyright Power Integrations 2012	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_071112: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**NO**		**NO**		Select 'YES' option if dimming is required. Otherwise select 'NO'.
VACMIN			90	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	140.00		140	V	Typical output voltage of LED string at full load
VO_MAX			154.00	V	Maximum expected LED string Voltage.
VO_MIN			126.00	V	Minimum expected LED string Voltage.
V_OVP			169.40	V	Over-voltage protection setpoint
IO	0.18		0.18	A	Typical full load LED current
PO			25.2	W	Output Power
n	0.90		0.9		
VB	20		20	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK419**		**LNK419**	Universal	115 Doubled/230V
Chosen Device		LNK419			
Current Limit Mode	**RED**		**RED**		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			2.35	A	Minimum current limit
ILIMITMAX			2.73	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			38.7	uA	V pin current
RV			3.909	M-ohms	Upper V pin resistor
RV2			1.402	M-ohms	Lower V pin resistor
IFB			155.8	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			109.1	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	0.46		0.46		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			2820	uH	Primary Inductance
VOR	135.00		135	V	Reflected Output Voltage.
Expected IO (average)			0.18	A	Expected Average Output Current
KP_VACMAX			0.76		Expected ripple current ratio at VACMAX
TON_MIN			4.01	us	Minimum on time at maximum AC input voltage
PCLAMP			0.29	W	Estimated dissipation in primary clamp
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Custom**		**EDR 3909**		Transformer core
Custom Core	**EDR 3909**				If using a custom core - Enter part number here
AE	1.0400		1.04	cm^2	Core Effective Cross Sectional Area
LE	2.0000		2	cm	Core Effective Path Length

AL	5000.0		5000	nH/T^2	Ungapped Core Effective Inductance
BW	3.7		3.7	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	7.00		7		Number of Primary Layers
NS	90		90		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			127	V	Peak input voltage at VACMIN
VMAX			375	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.54		Minimum duty cycle at peak of VACMIN
IAVG			0.29	A	Average Primary Current
IP			0.97	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.42	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2820	uH	Primary Inductance
NP			86		Primary Winding Number of Turns
NB			13		Bias Winding Number of Turns
ALG			377	nH/T^2	Gapped Core Effective Inductance
BM			3032	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3669	Gauss	Peak Flux Density (BP<3700)
BAC			697	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			765		Relative Permeability of Ungapped Core
LG			0.32	mm	Gap Length (Lg > 0.1 mm)
BWE			25.9	mm	Effective Bobbin Width
OD			0.30	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.25	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			191	Cmils/Amp	!!! INCREASE (200 < CMA < 600) Increase L(primary layers),decrease NS,larger Core
LP_TOL			10		Tolerance of primary inductance
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			0.93	A	Peak Secondary Current
ISRMS			0.36	A	Secondary RMS Current
IRIPPLE			0.31	A	Output Capacitor RMS Ripple Current
CMS			72	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			31	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.23	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.04	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN			647	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			559	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			82	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage

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					inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			3.91	M-ohms	Upper V Pin Resistor Value
RV2			1.40	M-ohms	Lower V Pin Resistor Value
VAC1			115.0	V	Test Input Voltage Condition1
VAC2			230.0	V	Test Input Voltage Condition2
IO_VAC1			0.18	A	Measured Output Current at VAC1
IO_VAC2			0.18	A	Measured Output Current at VAC2
RV1 (new)			3.91	M-ohms	New RV1
RV2 (new)			1.40	M-ohms	New RV2
V_OV			318.3	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			70.8	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			109	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+012	k-ohms	Lower FB Pin Resistor Value
VB1			17.9	V	Test Bias Voltage Condition1
VB2			22.1	V	Test Bias Voltage Condition2
IO1			0.18	A	Measured Output Current at Vb1
IO2			0.18	A	Measured Output Current at Vb2
RFB1 (new)			109.1	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2
Input Current Harmonic Analysis					
Harmonic			% of Fund	Limit(%)	
1st Harmonic					
3rd Harmonic			17.14	27.00	PASS. %age of 3rd Harmonic is lower than the limit
5th Harmonic			6.3	10.00	PASS. %age of 5th Harmonic is lower than the limit
7th Harmonic			3.2	7.00	PASS. %age of 7th Harmonic is lower than the limit
9th Harmonic			1.92	5.00	PASS. %age of 9th Harmonic is lower than the limit
11th Harmonic			1.34	3.00	PASS. %age of 11th Harmonic is lower than the limit
13th Harmonic			1.02	3.00	PASS. %age of 13th Harmonic is lower than the limit
15th Harmonic			0.82	3.00	PASS. %age of 15th Harmonic is lower than the limit
THD			18.4	%	Estimated total Harmonic Distortion (THD)

9 U1 Heat Sink Assembly

9.1 Heat Sink Fabrication Drawing

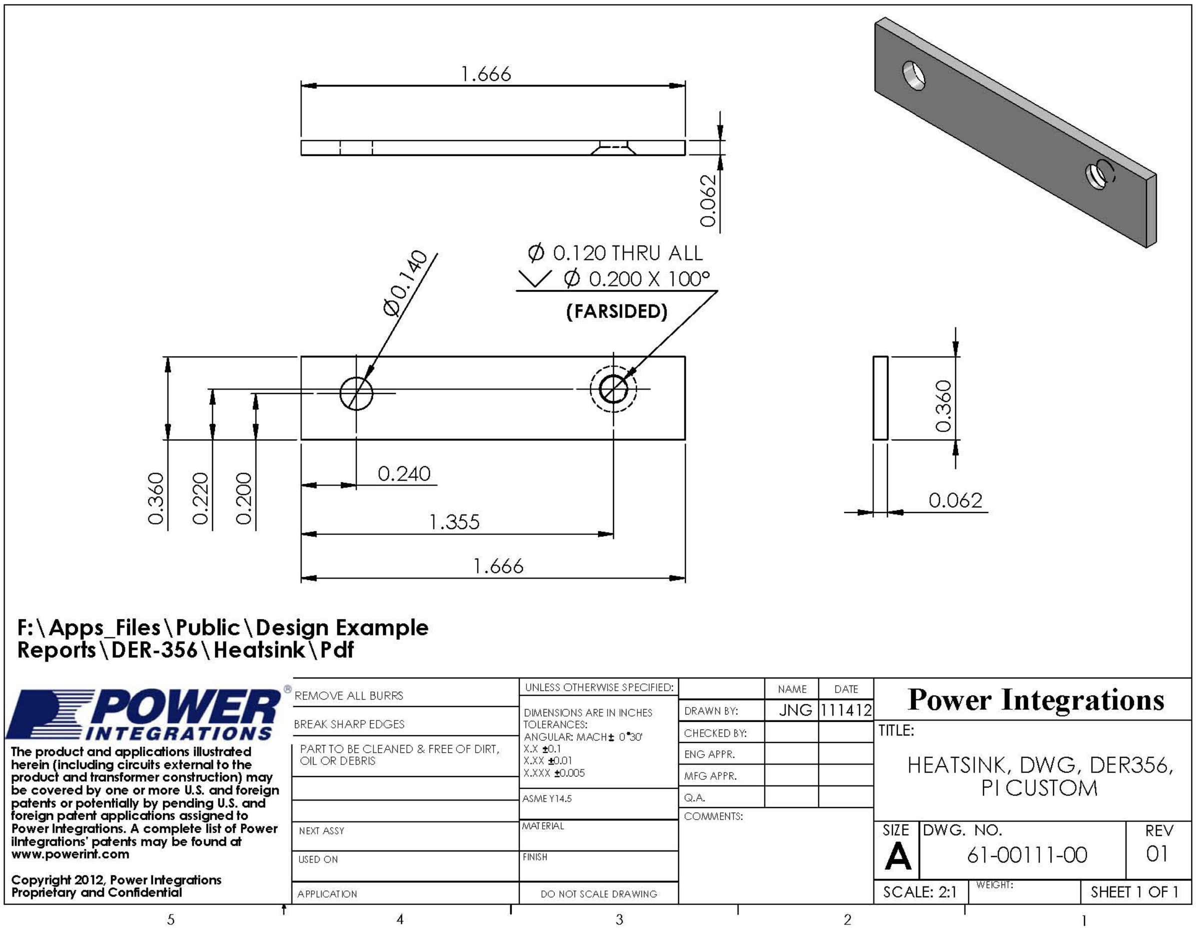

Figure 8 – U1 Heat Sink Dimensions.

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9.2 Heat Sink Assembly Drawing

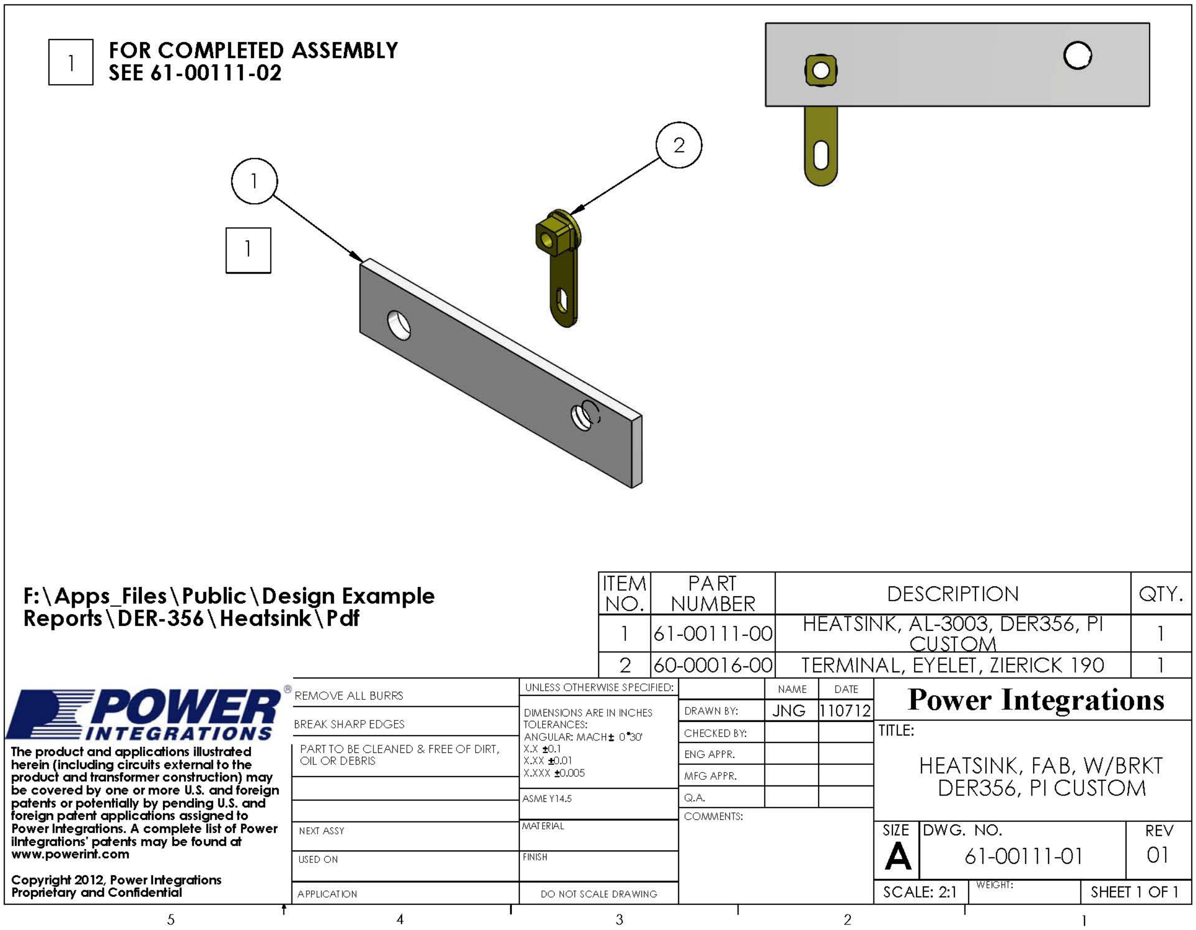
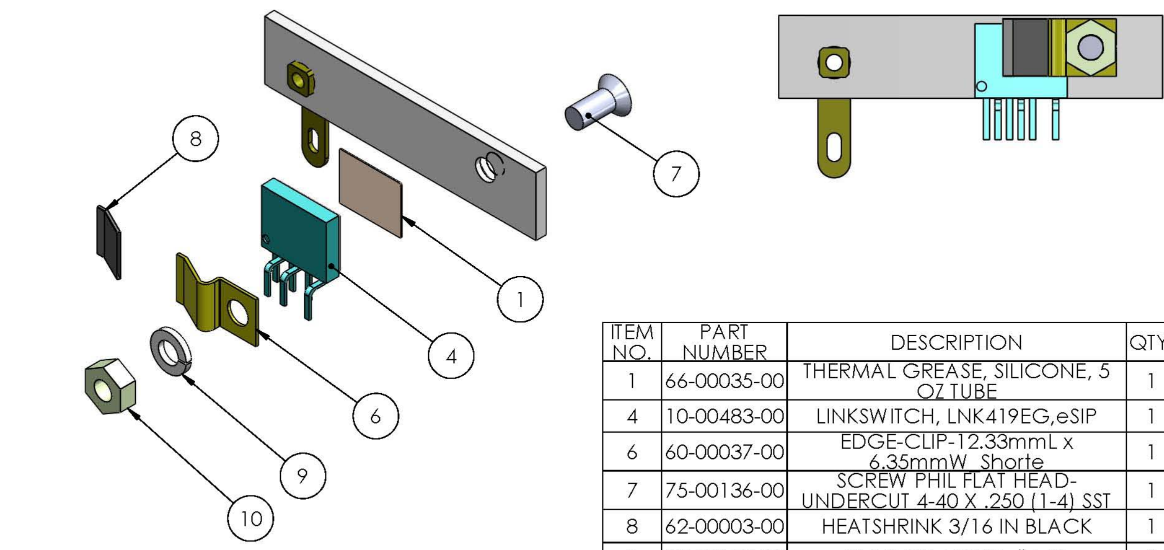


Figure 9 – U1 Heat Sink Fabrication Drawing.

9.3 Heat Sink and U1 Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	66-00035-00	THERMAL GREASE, SILICONE, 5 OZ TUBE	1
4	10-00483-00	LINKSWITCH, LNK419EG,eSIP	1
6	60-00037-00	EDGE-CLIP-12.33mmL x 6.35mmW_Shorte	1
7	75-00136-00	SCREW PHIL FLAT HEAD-UNDERCUT 4-40 X .250 (1-4) SST	1
8	62-00003-00	HEATSHRINK 3/16 IN BLACK	1
9	75-00153-00	WASHER, LOCK, #4 SS	1
10	75-00024-00	NUT,HEX 4-40, SS	1
11	61-00111-00	HEATSINK, CUSTOM, AL 3003, 0.062" THK	1

F:\Apps_Files\Public\Design Example Reports\DER-356\Heatsink\Pdf

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REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	110712
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

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TITLE: HEATSKINK, ASSY, eSIP, W/BRKT, DER356, PI CUSTOM

SIZE A | DWG. NO. 61-00111-02 | REV 01

SCALE: 1:1 | WEIGHT: | SHEET 1 OF 1

5 4 3 2 1

Figure 10 – U1 Heat Sink Assembly Drawing.

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10 Performance Data

The following data was compiled using 3 sets of load (121 V, 134 V, and 142 V LED strings). All measurements were performed at room temperature.

10.1 Efficiency

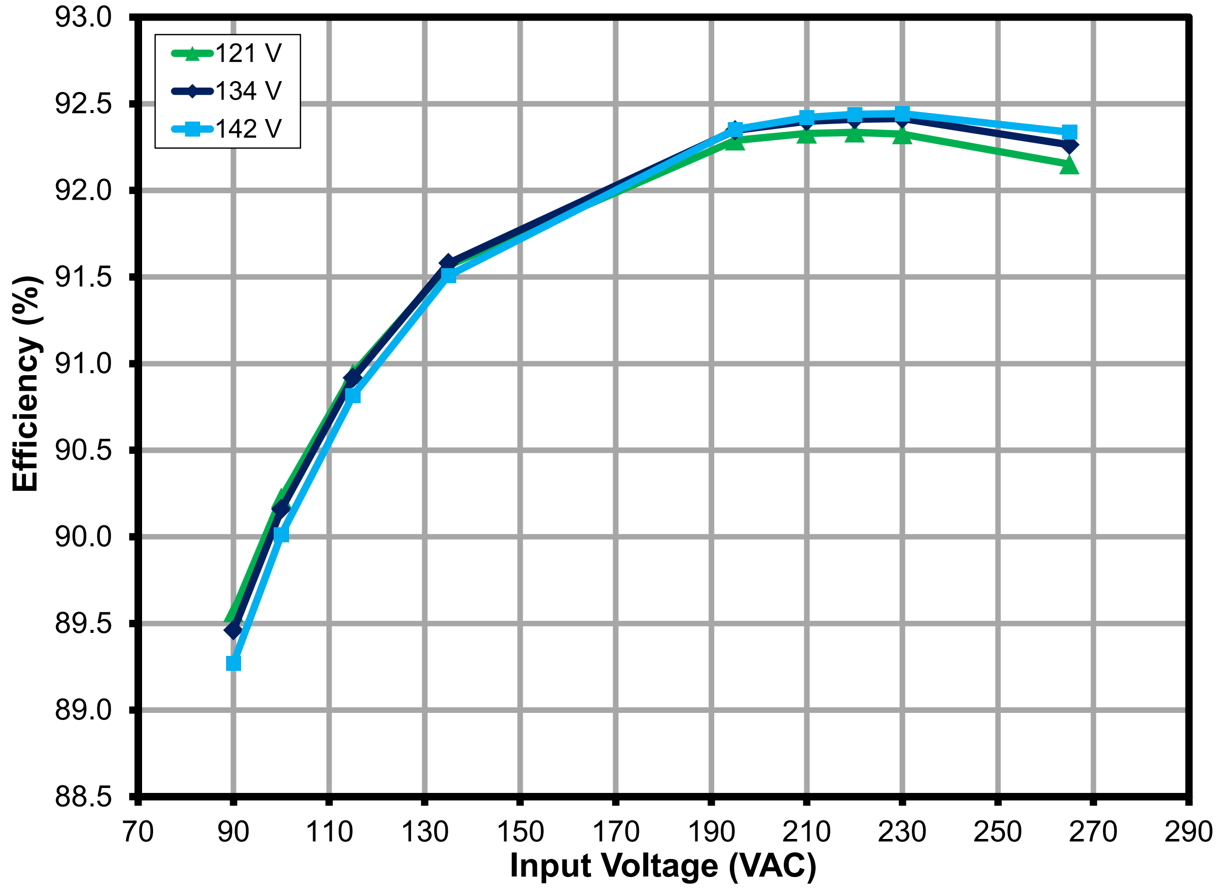

Figure 11 – Efficiency vs. Line and Load.

10.2 Line and Load Regulation

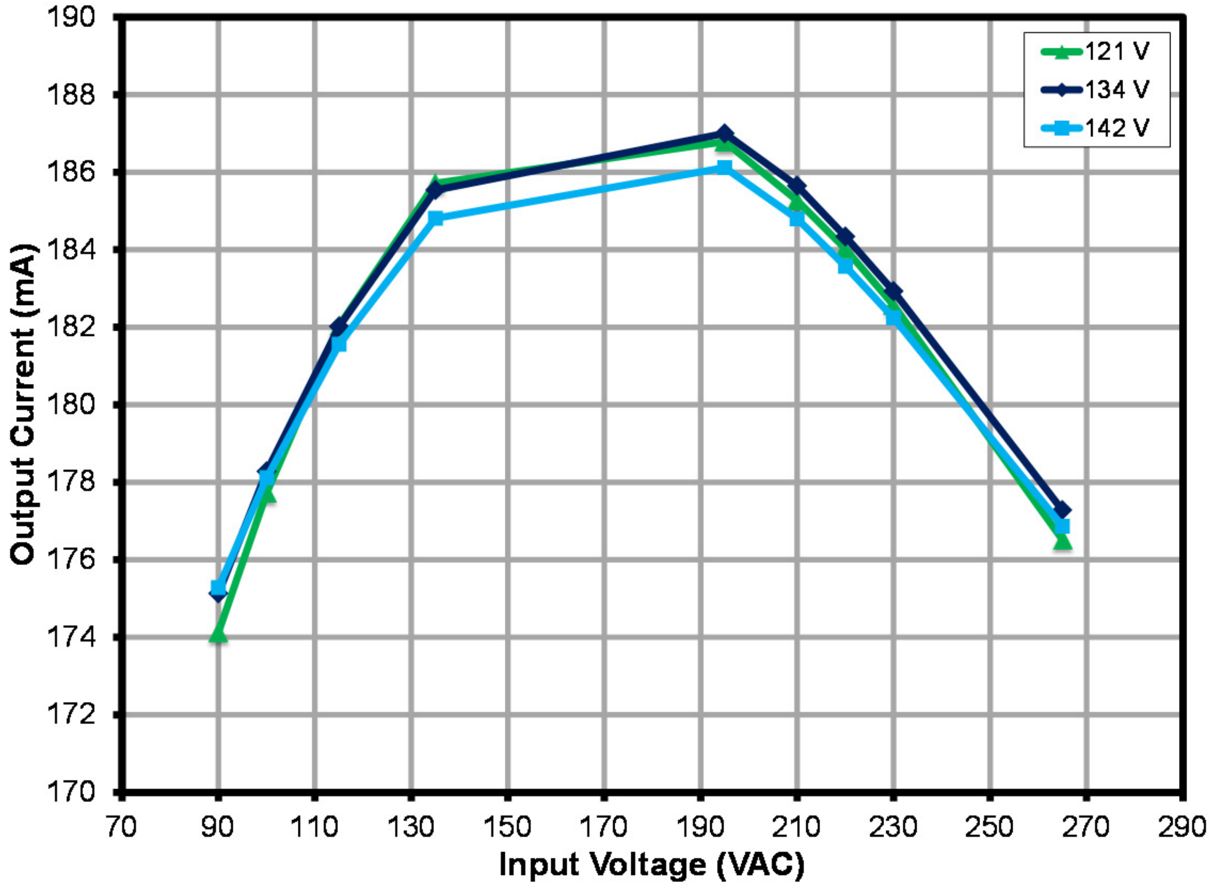

Figure 12 – Regulation vs. Line and Load.

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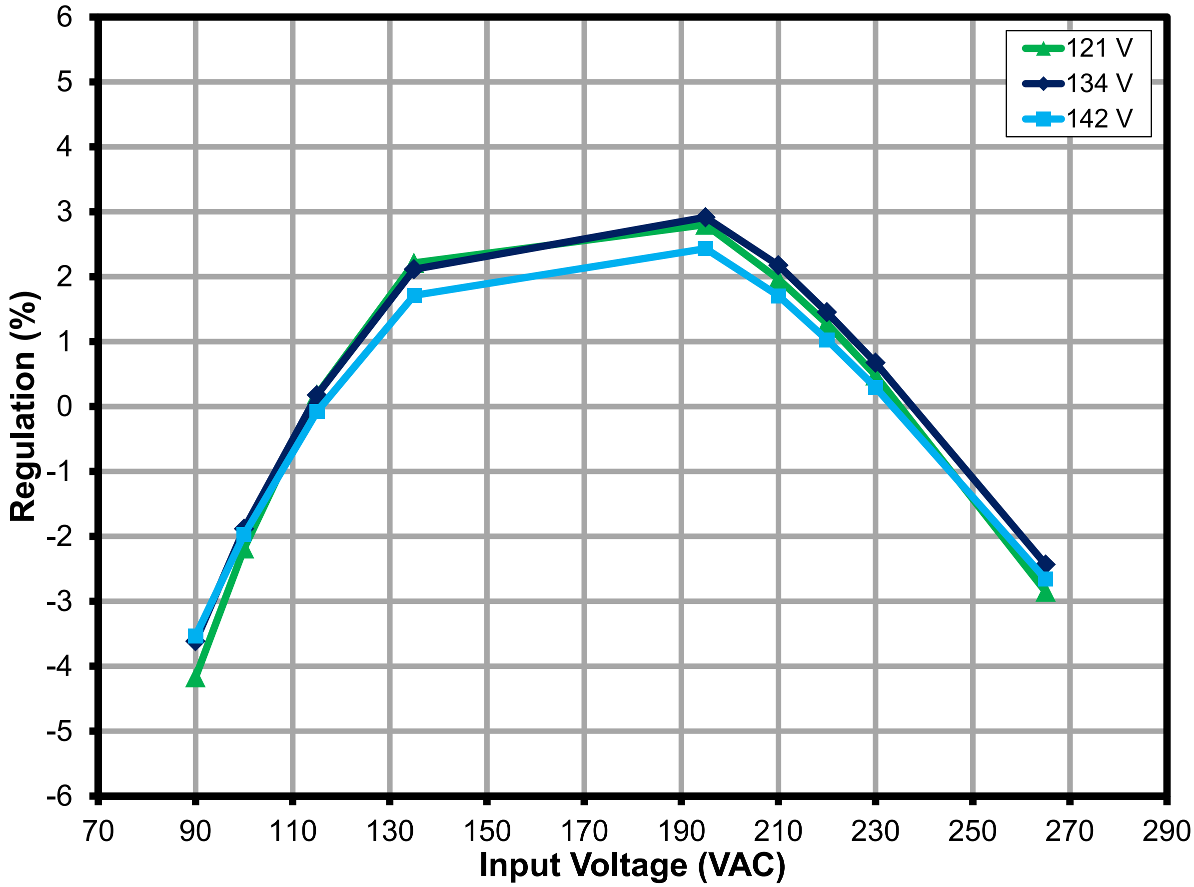

Figure 13 – Percent Line/Load Regulation.

10.3 Power Factor

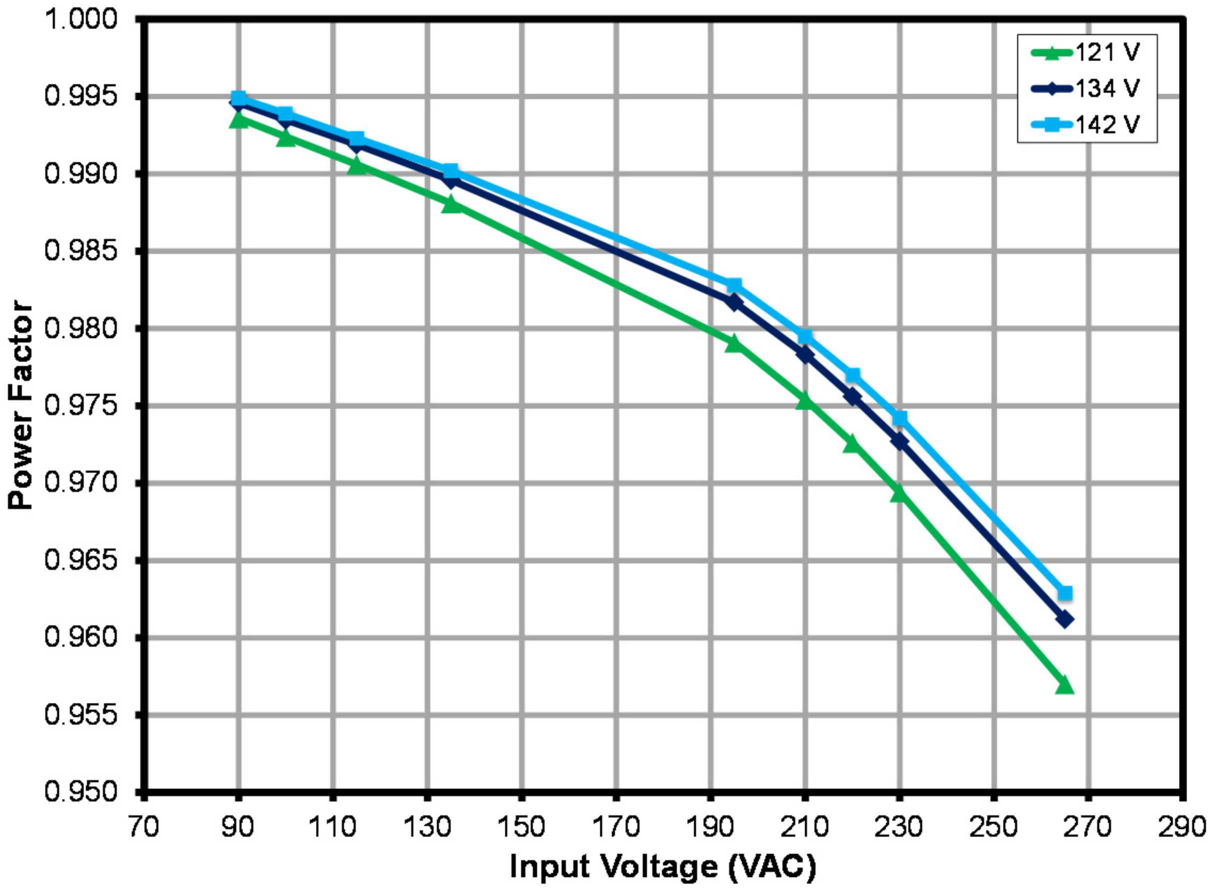

Figure 14 – Power Factor vs. Line and Load.

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10.4 A-THD

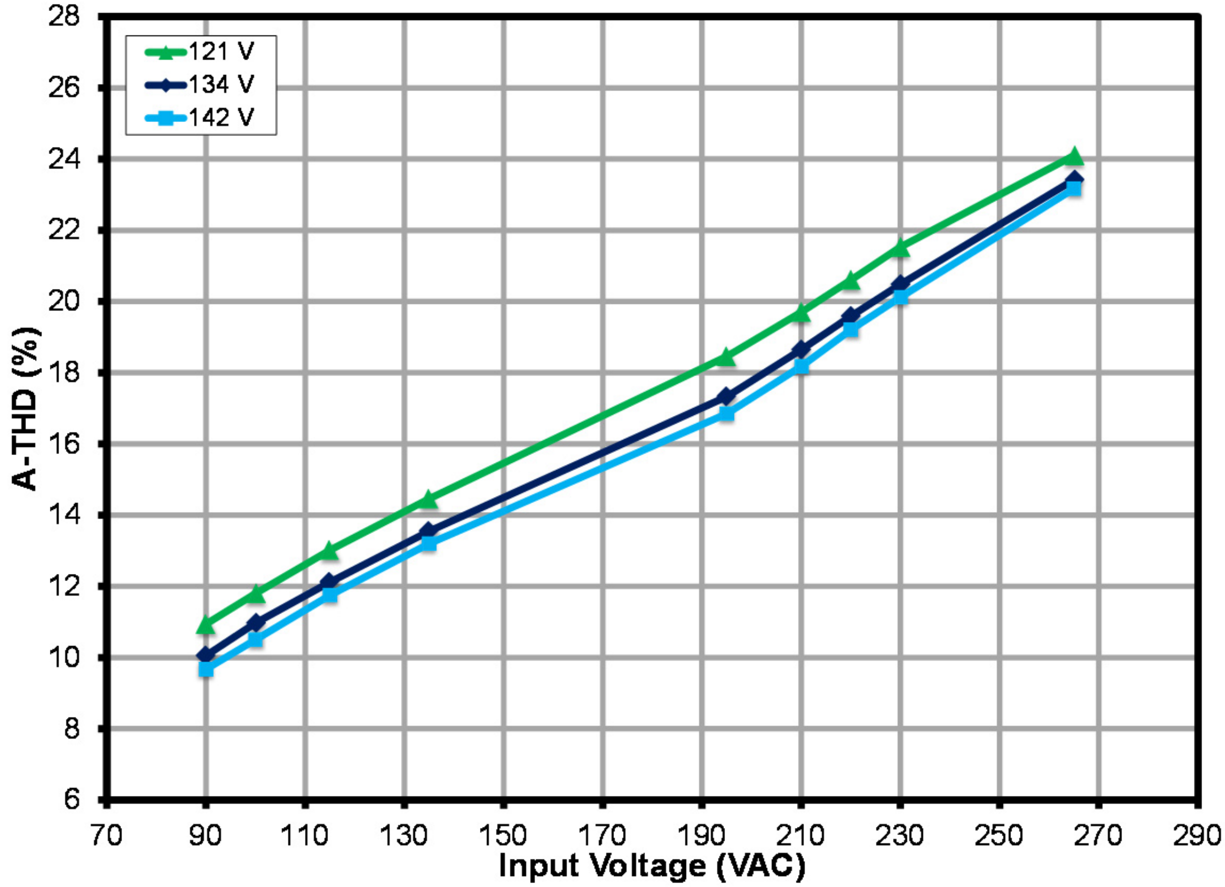

Figure 15 – A-THD vs. Line and Load.

10.5 Harmonics

The design met the IEC61000-3-2 Limits for Class C equipment (section 7.3-a) for an Active input power of > 25 W, which states that the harmonic currents shall not exceed the related limits given in Table 2 - Limits for Class C equipment.

10.5.1 134 V LED Load at 115 V, 60 Hz Input

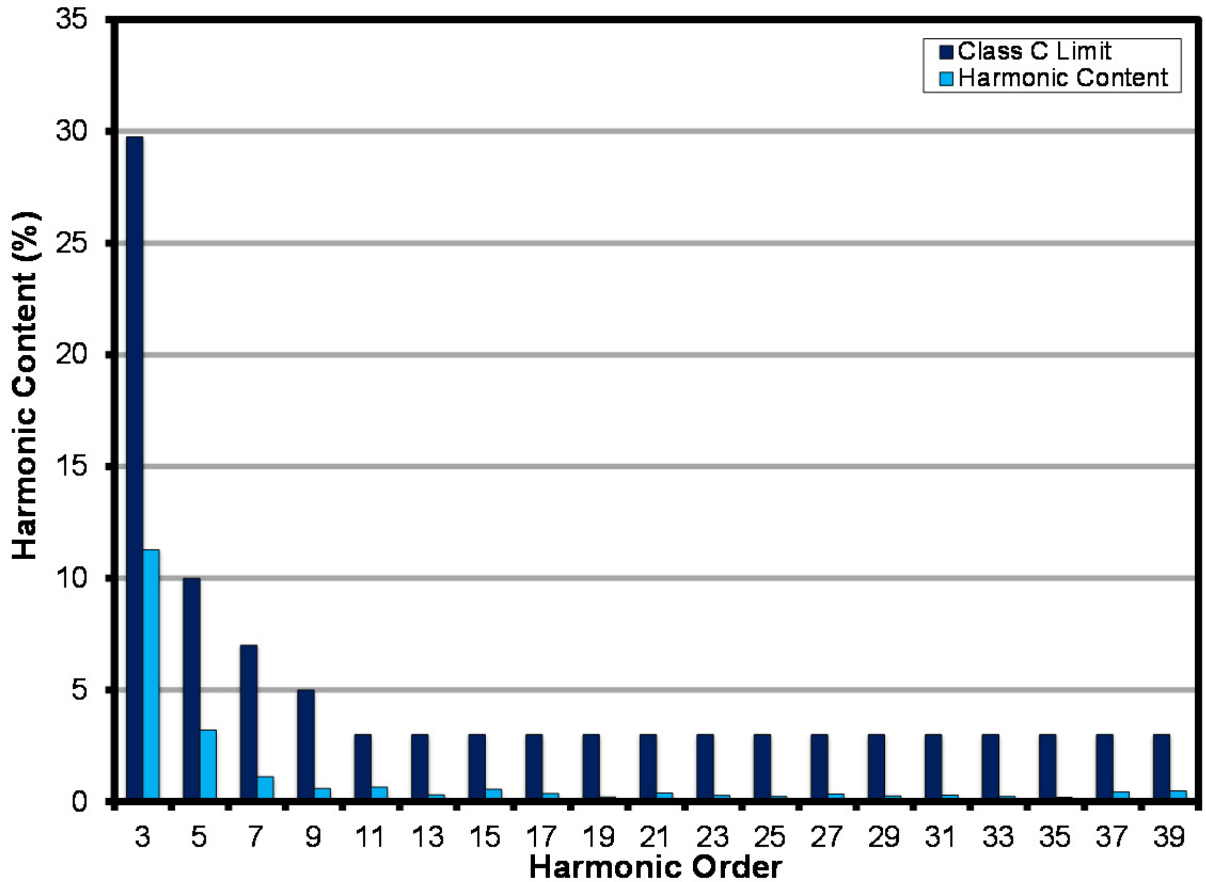

Figure 16 – 134 V LED Load Input Current Harmonics at 115 VAC, 60 Hz.

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10.5.3 134 V LED Load at 230 V, 50 Hz Input

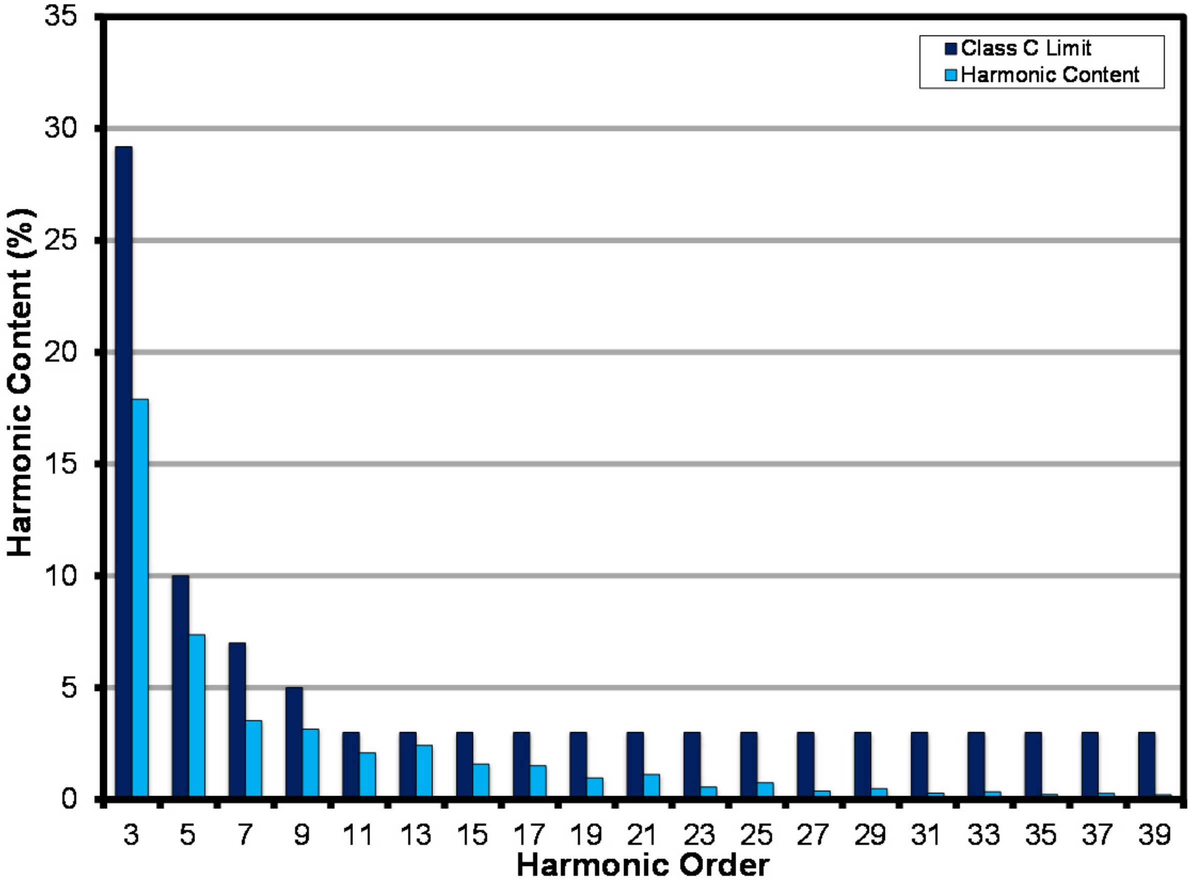

Figure 17 – 134 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

10.6 Test Data

All measurements were taken with the board in open frame configuration, and 25 °C ambient.

10.6.1 Test Data, 121 V LED Load

Input		Input Measurement					Load Measurement			Calculation			
V_{RMS} (VAC)	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)	% Reg
90	60	89.91	264.01	23.584	0.994	10.94	121.0700	174.130	21.123	21.08	89.56	2.46	4.17
100	60	99.95	241.02	23.907	0.992	11.8	121.1200	177.730	21.570	21.53	90.22	2.34	2.18
115	60	114.97	213.43	24.308	0.991	13.02	121.2000	182.040	22.106	22.06	90.94	2.20	0.19
135	60	134.96	184.78	24.642	0.988	14.46	121.2600	185.720	22.564	22.52	91.57	2.08	2.21
195	50	195.00	128.85	24.601	0.979	18.46	121.2500	186.790	22.704	22.65	92.29	1.90	2.80
210	50	209.94	119.04	24.377	0.975	19.7	121.1900	185.270	22.507	22.45	92.33	1.87	1.96
220	50	219.98	113.11	24.200	0.973	20.61	121.1500	184.020	22.345	22.29	92.33	1.86	1.28
230	50	230.02	107.62	23.999	0.969	21.53	121.0900	182.570	22.157	22.11	92.32	1.84	0.48
265	50	265.04	91.53	23.215	0.957	24.1	120.9500	176.520	21.393	21.35	92.15	1.82	-2.85

10.6.2 Test Data, 134 V LED Load

Input		Input Measurement					Load Measurement			Calculation			
V_{RMS} (VAC)	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)	% Reg
90	60	89.90	294.78	26.358	0.995	10.05	134.4100	175.130	23.580	23.54	89.46	2.78	-3.62
100	60	99.94	268.15	26.626	0.994	10.97	134.4200	178.280	24.006	23.96	90.16	2.62	-1.88
115	60	114.96	236.46	26.964	0.992	12.12	134.4500	182.020	24.515	24.47	90.92	2.45	0.18
135	60	134.96	204.35	27.292	0.990	13.55	134.4800	185.540	24.994	24.95	91.58	2.30	2.11
195	50	194.99	142.53	27.282	0.982	17.33	134.4400	187.000	25.194	25.14	92.35	2.09	2.92
210	50	209.93	131.71	27.051	0.978	18.65	134.3500	185.650	24.995	24.94	92.40	2.06	2.17
220	50	219.98	125.06	26.839	0.976	19.59	134.2700	184.340	24.802	24.75	92.41	2.04	1.45
230	50	230.02	118.96	26.616	0.973	20.48	134.1900	182.930	24.597	24.55	92.41	2.02	0.68
265	50	265.04	101.26	25.797	0.961	23.42	134.0200	177.280	23.801	23.76	92.26	2.00	-2.43

10.6.3 Test Data, 142 V LED Load

Input		Input Measurement					Load Measurement			Calculation			
V_{RMS} (VAC)	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)	% Reg
90	60	89.90	312.51	27.951	0.995	9.67	142.1300	175.280	24.952	24.91	89.27	3.00	-3.53
100	60	99.94	283.66	28.177	0.994	10.5	142.1700	178.120	25.363	25.32	90.01	2.81	-1.97
115	60	114.97	249.48	28.462	0.992	11.75	142.1400	181.560	25.848	25.81	90.82	2.61	-0.08
135	60	134.96	215.32	28.774	0.990	13.2	142.2700	184.810	26.331	26.29	91.51	2.44	1.71
195	50	195.00	149.83	28.713	0.983	16.85	142.2000	186.120	26.517	26.47	92.35	2.20	2.43
210	50	209.94	138.39	28.459	0.980	18.18	142.0600	184.800	26.302	26.25	92.42	2.16	1.71
220	50	219.98	131.44	28.249	0.977	19.21	141.9900	183.570	26.113	26.07	92.44	2.14	1.03
230	50	230.02	125.08	28.028	0.974	20.12	141.9200	182.240	25.910	25.86	92.44	2.12	0.30
265	50	265.04	106.55	27.194	0.963	23.17	141.7500	176.870	25.110	25.07	92.34	2.08	-2.66

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10.6.4 134 V LED Load Harmonics Data at 115 VAC, 60 Hz Input

V	Freq	I (mA)	P	PF	%THD
115	60.00	236.46	26.9640	0.9919	12.12
	nth Order	mA Content	% Content	Class C Limit	Remarks
	1	234.47			
	2	0.18	0.08%	2.00%	
	3	26.43	11.27%	29.76%	PASS
	5	7.53	3.21%	10.00%	PASS
	7	2.61	1.11%	7.00%	PASS
	9	1.38	0.59%	5.00%	PASS
	11	1.52	0.65%	3.00%	PASS
	13	0.73	0.31%	3.00%	PASS
	15	1.30	0.55%	3.00%	PASS
	17	0.87	0.37%	3.00%	PASS
	19	0.49	0.21%	3.00%	PASS
	21	0.92	0.39%	3.00%	PASS
	23	0.66	0.28%	3.00%	PASS
	25	0.54	0.23%	3.00%	PASS
	27	0.80	0.34%	3.00%	PASS
	29	0.60	0.26%	3.00%	PASS
	31	0.69	0.29%	3.00%	PASS
	33	0.56	0.24%	3.00%	PASS
	35	0.46	0.20%	3.00%	PASS
	37	1.02	0.44%	3.00%	PASS
	39	1.14	0.49%	3.00%	PASS

10.6.5 134 V LED Load Harmonics Data at 230 VAC, 50 Hz Input

V	Freq	I (mA)	P	PF	%THD
230	50.00	118.96	26.6160	0.9727	20.48
	nth Order	**mA Content**	**% Content**	**Limit >25 W**	**Remarks**
	1	116.30			
	2	0.12	0.10%	2.00%	
	3	20.81	17.89%	29.18%	PASS
	5	8.56	7.36%	10.00%	PASS
	7	4.10	3.53%	7.00%	PASS
	9	3.66	3.15%	5.00%	PASS
	11	2.42	2.08%	3.00%	PASS
	13	2.81	2.42%	3.00%	PASS
	15	1.83	1.57%	3.00%	PASS
	17	1.75	1.50%	3.00%	PASS
	19	1.12	0.96%	3.00%	PASS
	21	1.30	1.12%	3.00%	PASS
	23	0.64	0.55%	3.00%	PASS
	25	0.87	0.75%	3.00%	PASS
	27	0.44	0.38%	3.00%	PASS
	29	0.56	0.48%	3.00%	PASS
	31	0.32	0.28%	3.00%	PASS
	33	0.39	0.34%	3.00%	PASS
	35	0.26	0.22%	3.00%	PASS
	37	0.31	0.27%	3.00%	PASS
	39	0.24	0.21%	3.00%	PASS

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11 Waveforms

11.1 Input Line Current

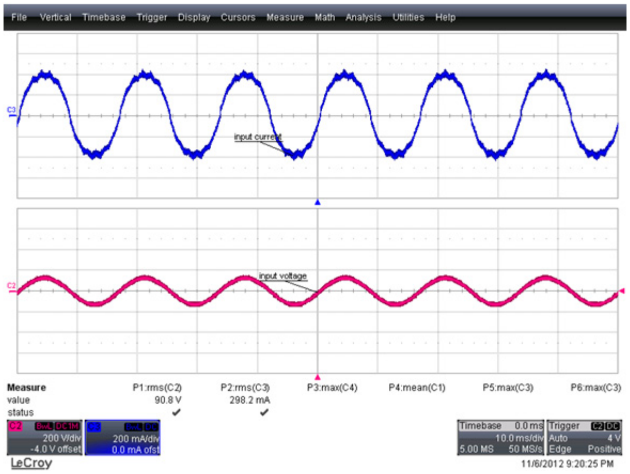

Figure 18 – 90 VAC 60 Hz, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

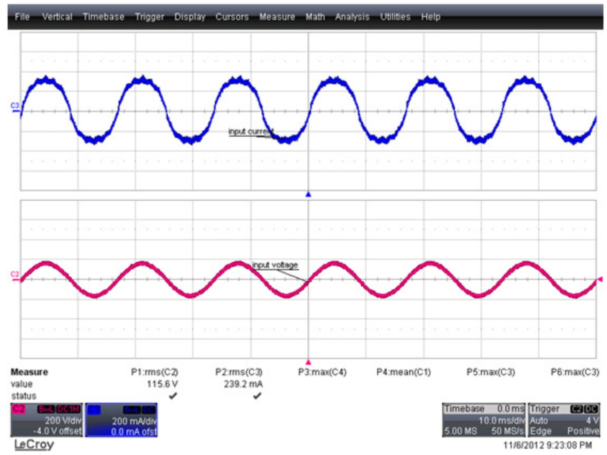

Figure 19 – 115 VAC 60 Hz, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

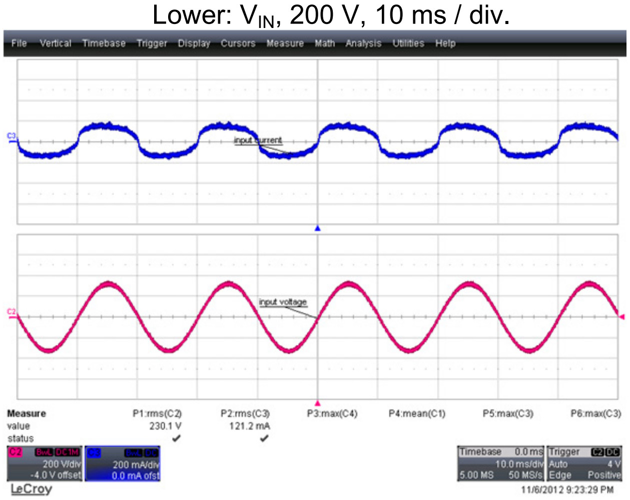

Figure 20 – 230 VAC 50 Hz, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

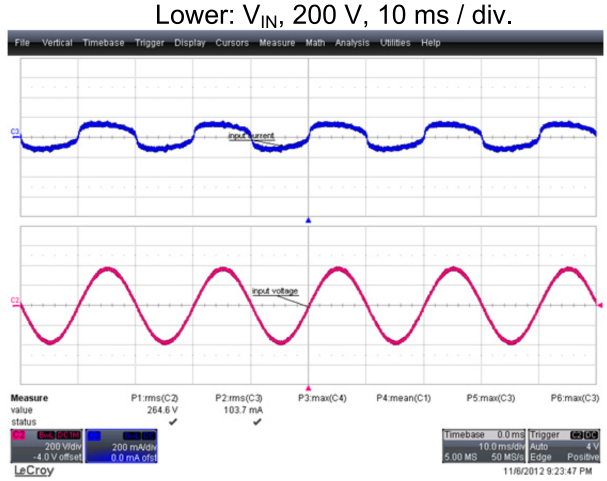

Figure 21 – 265 VAC 50 Hz, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

11.2 Drain Voltage and Current Normal Operation

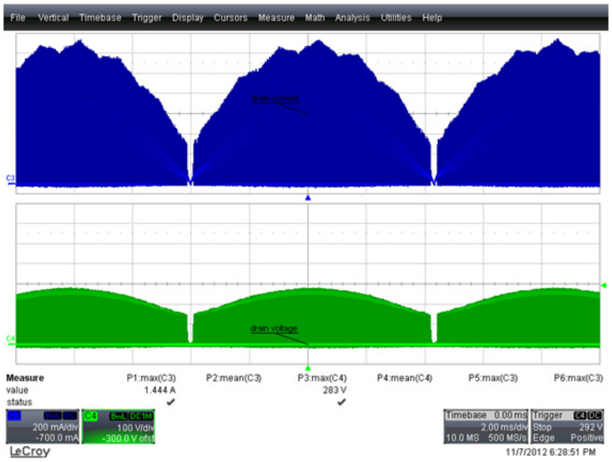

Figure 22 – 90 VAC 60 Hz, Full Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V, 2 ms / div.

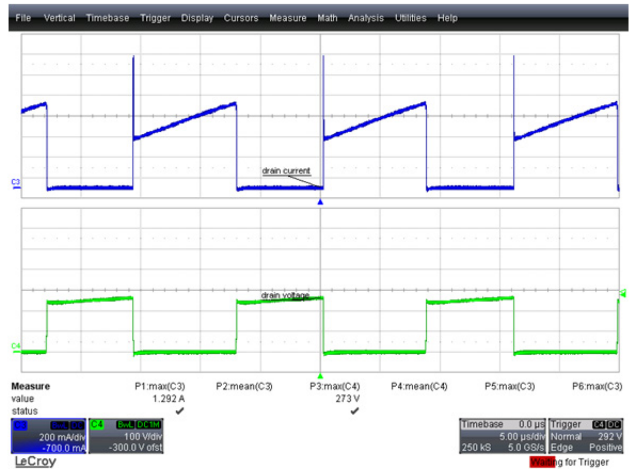

Figure 23 – 90 VAC 60 Hz, Full Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V, 5 μs / div.

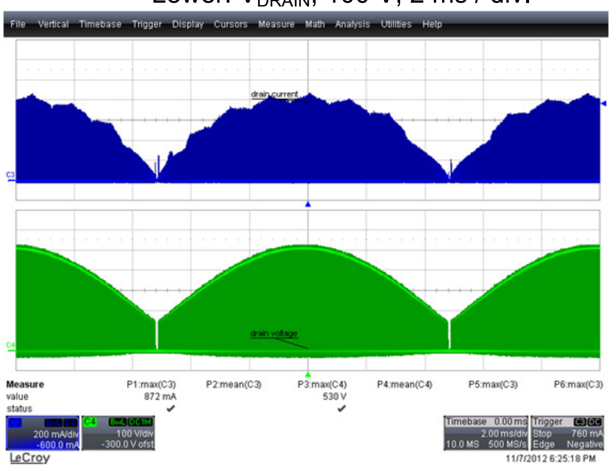

Figure 24 – 265 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V, 2 ms / div.

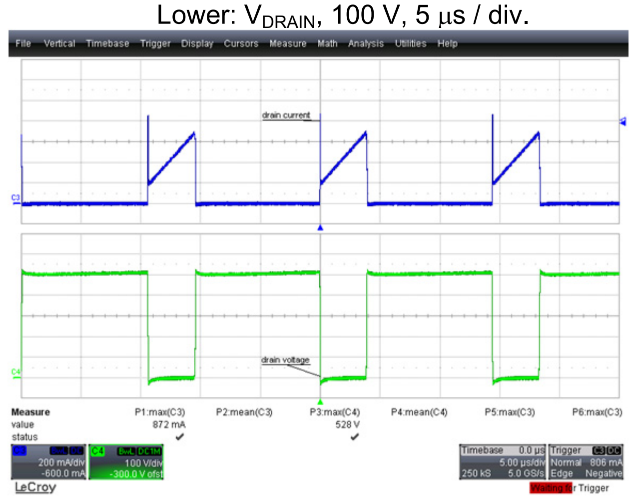

Figure 25 – 265 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 100 V, 5 μs / div.

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11.3 Drain Voltage and Current Start-up Operation

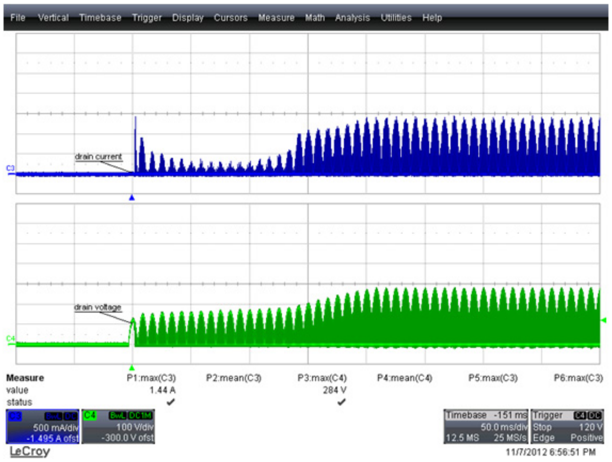

Figure 26 – 90 VAC 60 Hz, Full Load Start-up.
Upper: I_{DRAIN}, 500 mA / div.
Lower: V_{DRAIN}, 100 V, 50 ms / div.

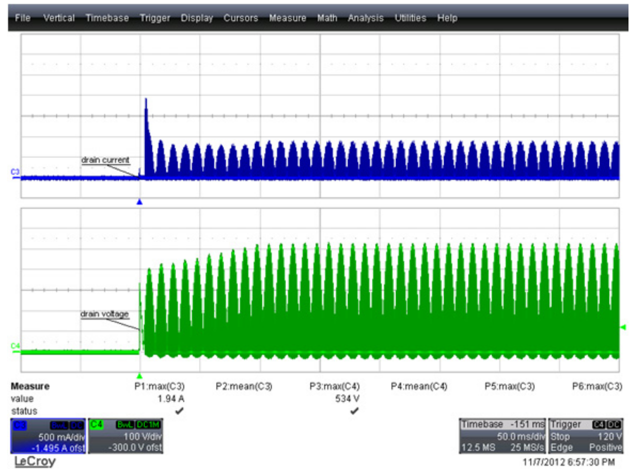

Figure 27 – 265 VAC 50 Hz, Full Load Start-up.
Upper: I_{DRAIN}, 500 mA / div.
Lower: V_{DRAIN}, 100 V, 50 ms / div.

11.4 Output Current and Output Voltage

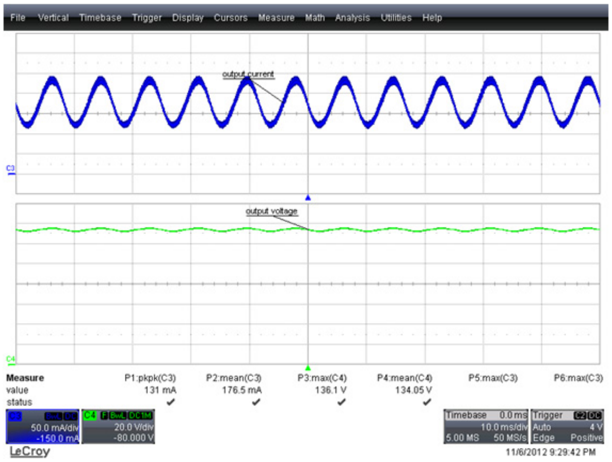

Figure 28 – 90 VAC 60 Hz, Full Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

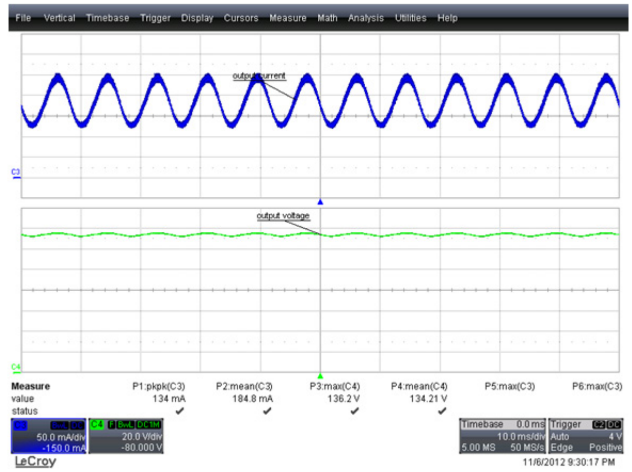

Figure 29 – 115 VAC 60 Hz, Full Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

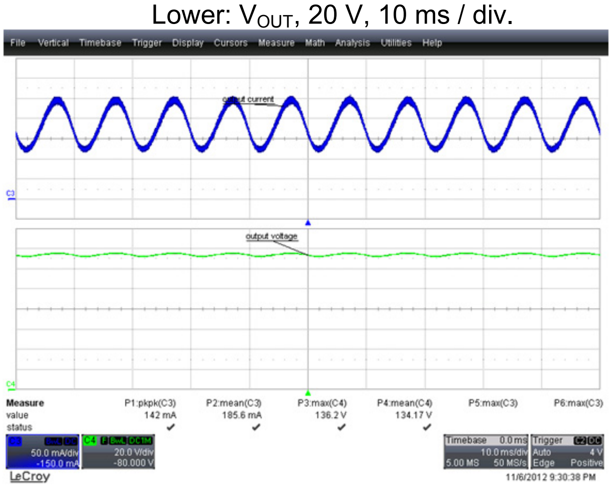

Figure 30 – 230 VAC 50 Hz, Full Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

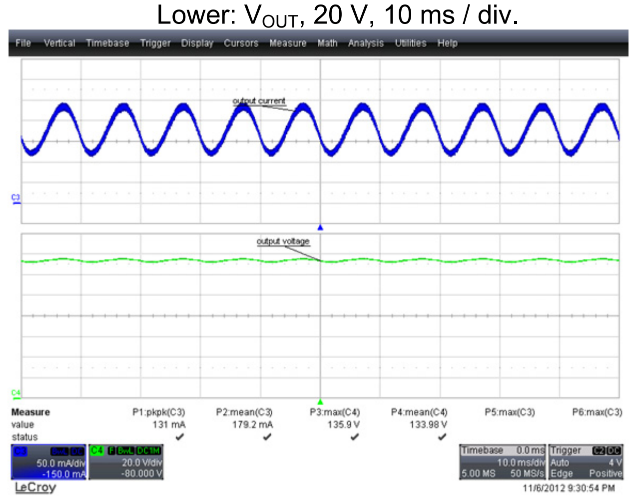

Figure 31 – 265 VAC 50 Hz, Full Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

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11.5 *Output Current and Voltage at Power-up, Power-down*

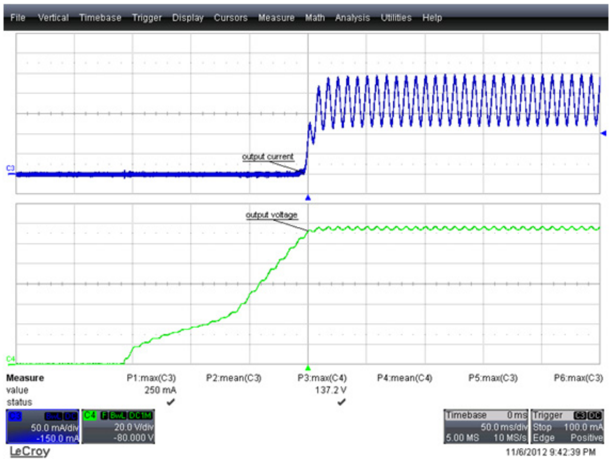

Figure 32 – 115 VAC 60 Hz, Output Rise.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 50 ms / div.

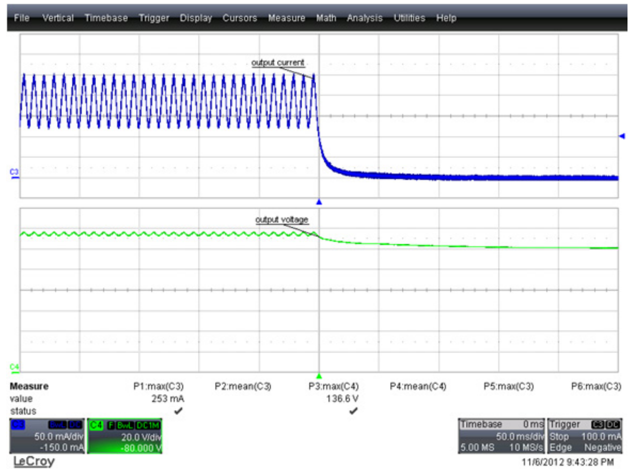

Figure 33 – 115 VAC 60 Hz, Output Fall.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 50 ms / div.

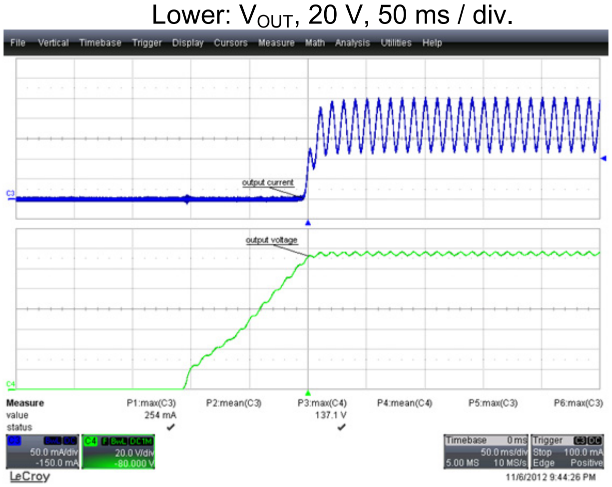

Figure 34 – 230 VAC 50 Hz, Output Rise.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 50 ms / div.

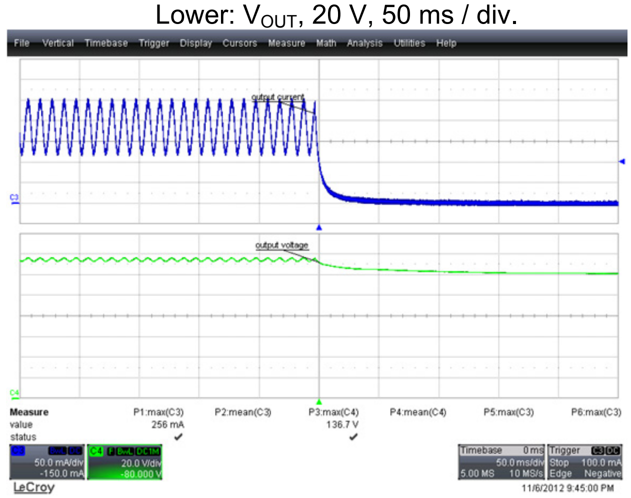

Figure 35 – 230 VAC 50 Hz, Output Fall.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{OUT}, 20 V, 50 ms / div.

11.6 Output Short

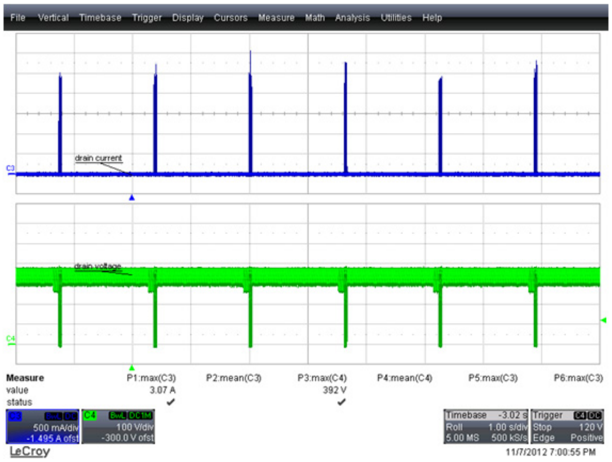

Figure 36 – 265 VAC 50 Hz, Output Short.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 1 s / div.

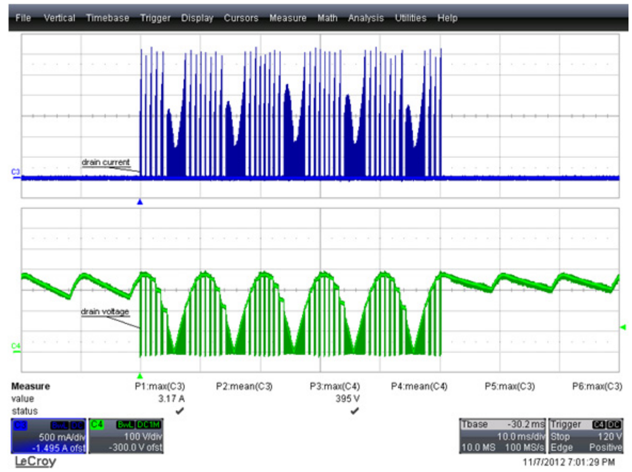

Figure 37 – 265 VAC 50 Hz, Output Short.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 10 ms / div.

11.7 Open Load

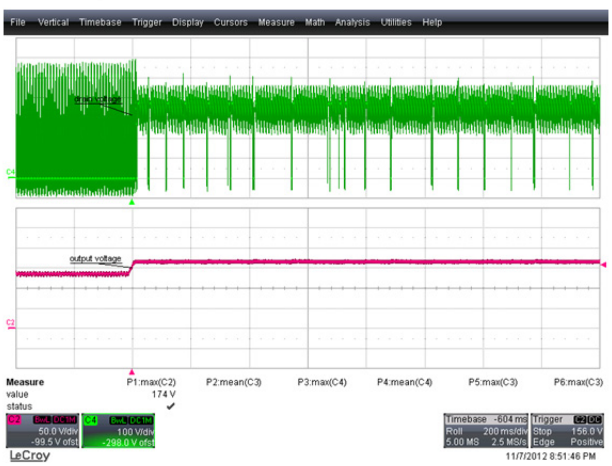

Figure 38 – 265 VAC 50 Hz, Open Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: V_{OUT}, 50 V, 200 ms / div.

Figure 39 – 265 VAC 50 Hz, Open Load Start-up
Upper: V_{DRAIN}, 100 V / div.
Lower: V_{OUT}, 50 V, 200 ms / div.

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12 Thermal Measurements

Thermal measurements were done with the EUT operated at room temperature, 134 V LED Load

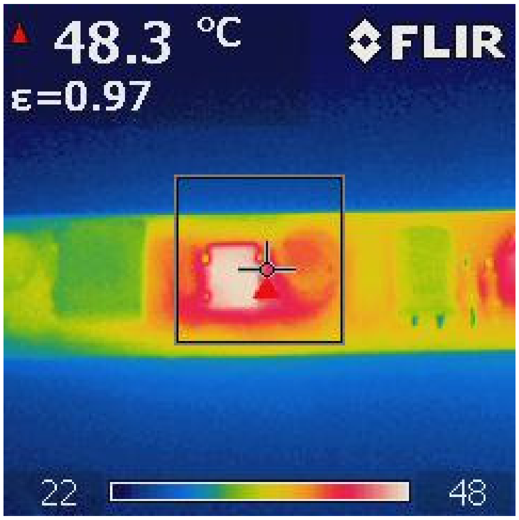


Figure 40 – Input Area, 110 VAC, 60 Hz

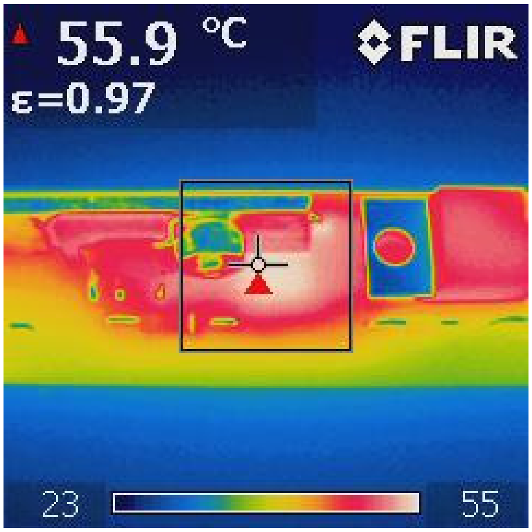


Figure 41 – LNK419EG Area, 110 VAC, 60 Hz

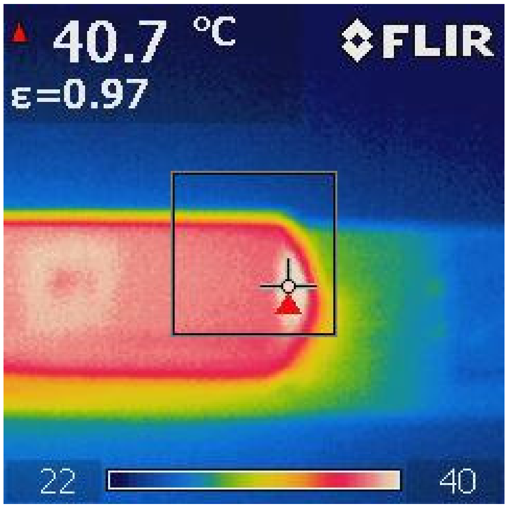
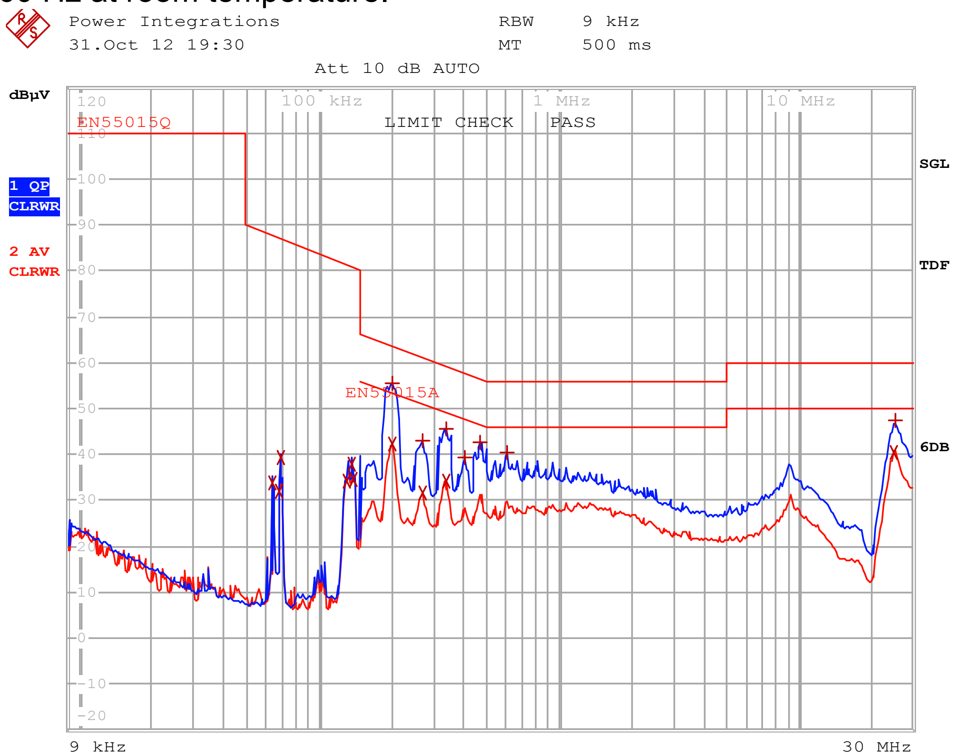


Figure 42 – Output Area, 110 VAC, 60 Hz

13 Conducted EMI Measurements

The unit was tested using ~ 134 V LED strings as load with an input voltage of 230 VAC, 60 Hz at room temperature.



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	63.9076936414 kHz	34.01	L1 gnd	
2	Average	67.1676282959 kHz	31.88	N gnd	
2	Average	68.5176976246 kHz	39.49	L1 gnd	
2	Average	129.530094744 kHz	34.19	N gnd	
2	Average	136.137431366 kHz	37.75	L1 gnd	
2	Average	138.873793737 kHz	34.40	L1 gnd	
1	Quasi Peak	200.175581485 kHz	55.37	L1 gnd	-8.23
2	Average	200.175581485 kHz	42.37	L1 gnd	-11.22
1	Quasi Peak	267.135089486 kHz	43.02	L1 gnd	-18.18
2	Average	267.135089486 kHz	31.62	L1 gnd	-19.58
1	Quasi Peak	335.832355405 kHz	45.66	L1 gnd	-13.64
2	Average	335.832355405 kHz	34.29	L1 gnd	-15.01
1	Quasi Peak	401.705024172 kHz	39.28	L1 gnd	-18.52
1	Quasi Peak	466.367062279 kHz	42.56	N gnd	-14.01
1	Quasi Peak	604.06488251 kHz	40.46	N gnd	-15.53
2	Average	24.9618853035 MHz	40.45	L1 gnd	-9.54
1	Quasi Peak	25.2115041566 MHz	47.61	L1 gnd	-12.38

Figure 43 – Conducted EMI, 134 V LED Load, 115 VAC, 60 Hz, EN55015B Limits.

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EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV			DELTA LIMIT dB
2	Average	68.5176976246 kHz	34.65	L1	gnd	
2	Average	126.977840157 kHz	38.88	L1	gnd	
2	Average	136.137431366 kHz	45.83	L1	gnd	
2	Average	141.665156991 kHz	35.36	N	gnd	
2	Average	167.350252 kHz	31.78	N	gnd	-23.30
1	Quasi Peak	190.46019728 kHz	49.13	L1	gnd	-14.88
2	Average	200.175581485 kHz	38.67	L1	gnd	-14.92
1	Quasi Peak	267.135089486 kHz	46.62	L1	gnd	-14.58
2	Average	267.135089486 kHz	35.71	L1	gnd	-15.49
1	Quasi Peak	335.832355405 kHz	45.10	L1	gnd	-14.19
2	Average	335.832355405 kHz	33.96	L1	gnd	-15.33
1	Quasi Peak	401.705024172 kHz	39.85	N	gnd	-17.96
1	Quasi Peak	536.076911993 kHz	43.86	L1	gnd	-12.13
2	Average	536.076911993 kHz	32.50	L1	gnd	-13.49
1	Quasi Peak	2.18042326152 MHz	36.71	L1	gnd	-19.28
1	Quasi Peak	25.4636191981 MHz	43.61	L1	gnd	-16.38
2	Average	25.4636191981 MHz	37.36	L1	gnd	-12.63

Figure 44 – Conducted EMI, 134 V LED Load, 230 VAC, 60 Hz, EN55015B Limits.

14 Line Surge Test

The unit was subjected to ±2500 V, 100 kHz ring wave and ±500 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

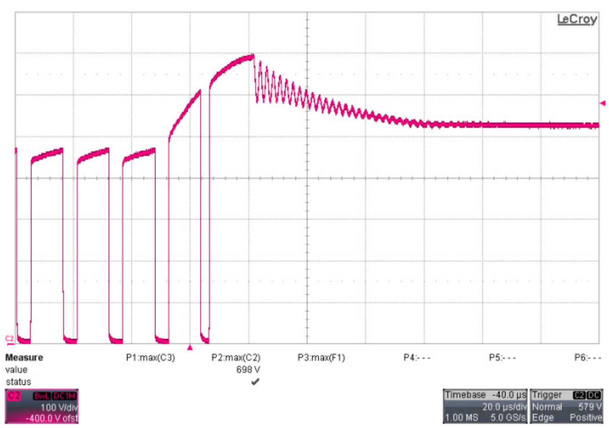

Figure 45 – (+) 500 V Differential Surge, 90°
V_{DRAIN}, 100 V, 20 μs / div.

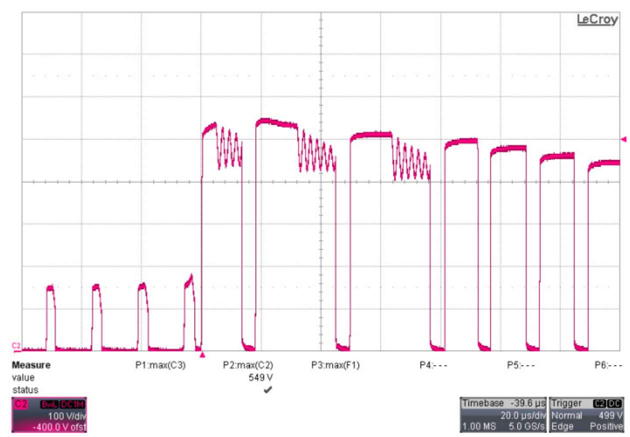

Figure 46 – (+) 500 V Differential Surge, 0°
V_{DRAIN}, 100 V, 20 μs / div.

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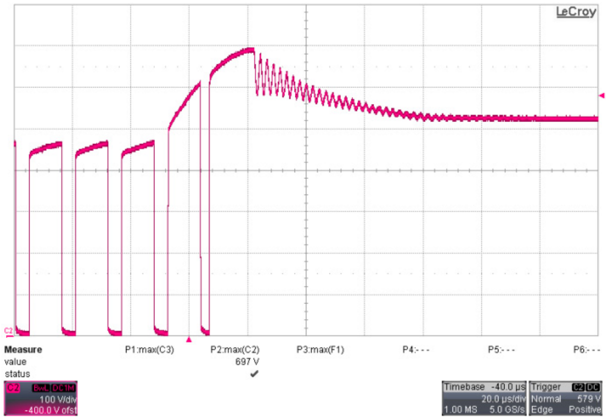

Figure 47 – (-) 500 V Differential Surge, 90°
V_{DRAIN}, 100 V, 20 μs / div.

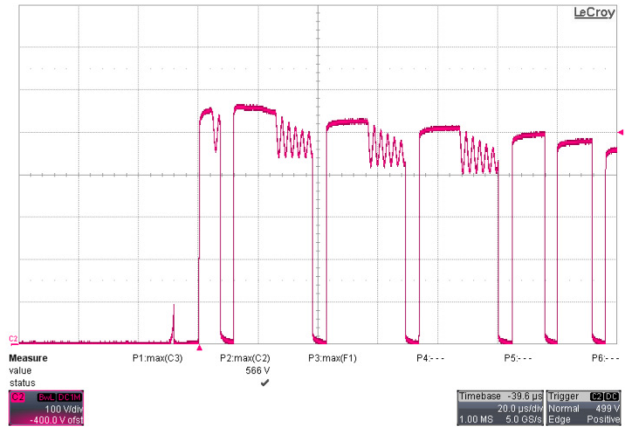

Figure 48 – (-) 500 V Differential Surge, 0°
V_{DRAIN}, 100 V, 20 μs / div.

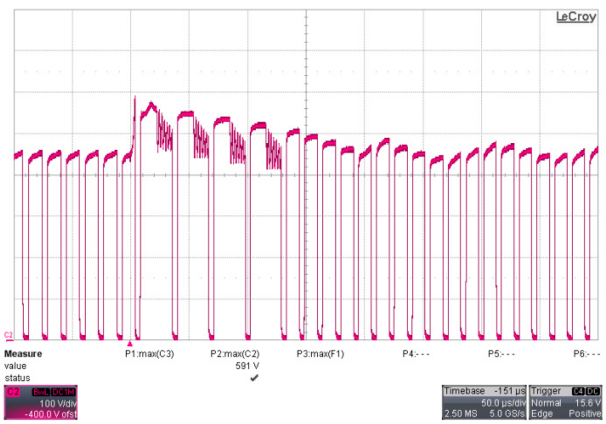

Figure 49 – (+) 2.5 kV Ring Wave, 90°
V_{DRAIN}, 100 V, 50 μs / div.

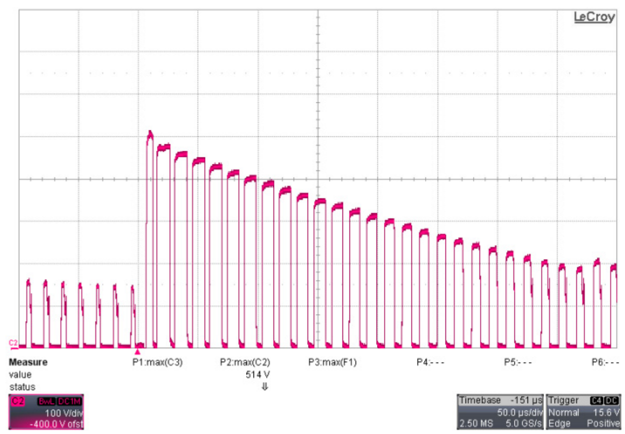

Figure 50 – (+) 2.5 kV Ring Wave, 0°
V_{DRAIN}, 100 V, 50 μs / div.

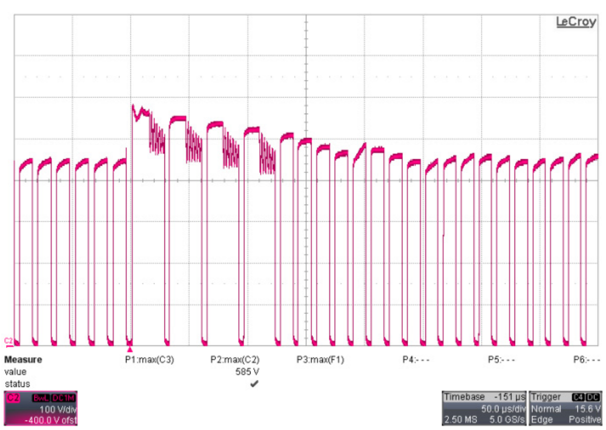

Figure 51 – (-) 2.5 kV Ring Wave, 90°
V_{DRAIN}, 100 V, 50 μs / div.

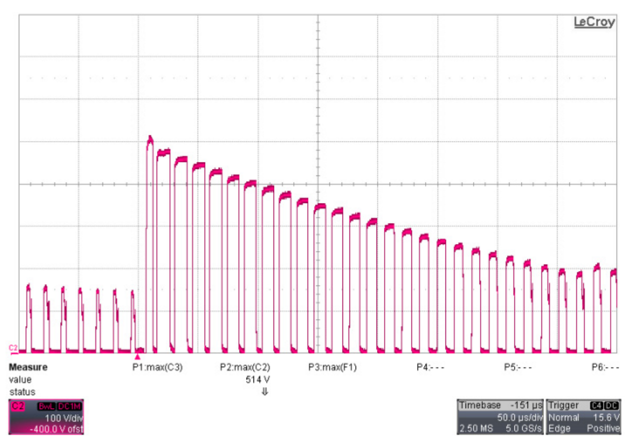

Figure 52 – (-) 2.5 kV Ring Wave, 0°
V_{DRAIN}, 100 V, 50 μs / div.

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
6-Dec-12	DS	1.0	Initial Release	Apps and Mktg

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