Design Example Report

Title	***7 W Power Factor Corrected LED Driver (Non-Isolated Boost) B10 Lamp Replacement Using LinkSwitch^{TM}-PL LNK457DG***
Specification	90 VAC – 132 VAC Input; 230 $V_{TYPICAL}$, 30 mA Output
Application	LED Driver for B10 Lamp Replacement
Author	Applications Engineering Department
Document Number	DER-324
Date	March 14, 2012
Revision	1.0

Summary and Features

- Single-stage power factor corrected and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Highly energy efficient, >90 % at 115 VAC input
- No potting is needed to operate at 75 ºC internal case ambient.
- Fast start-up time (<50 ms) – no perceptible delay
- Integrated protection and reliability features
  - No-load protection / hard short-circuit protected
  - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
  - No damage during line brown-out or brown-in conditions
- PF >0.95 at 115 VAC
- %ATHD <25% at 115 VAC
- Meets IEC 2.5 kV ring wave, 500 V differential line surge and EN55015 conducted EMI

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Table of Contents

Important Note:
Although this board is designed to satisfy safety requirements for non-isolated LED drivers, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK457DG from the LinkSwitch-PL family of devices.

The DER-324 provides a single 7 W constant current output.

The key design goals were high efficiency to maximize efficacy and small size. This allowed the driver to fit into B10 sized lamps and be as close to a production design as possible.

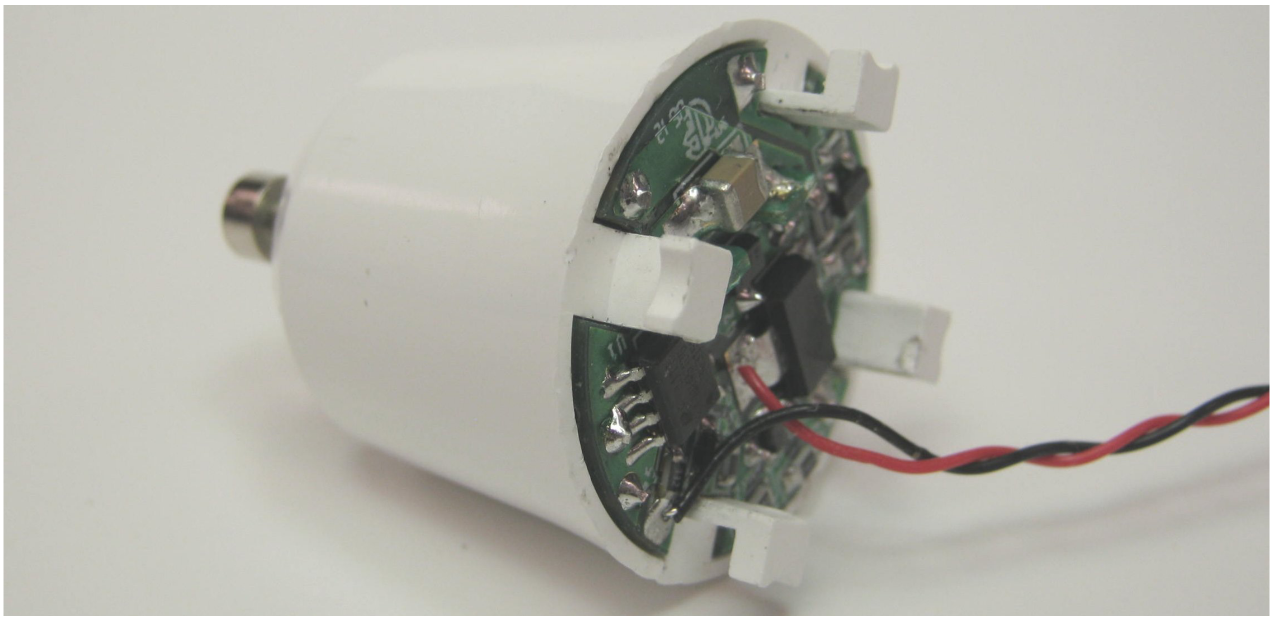

Figure 1 – PCB Assembly Inside B10 Housing.

The board was optimized to operate over the low AC input voltage range (90 VAC to 132 VAC, 47 Hz to 63 Hz). LinkSwitch-PL IC based designs provide a high power factor (>0.95) meeting current international requirements.

The form factor of the board was chosen to meet the requirements for standard B10 LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet and performance data.

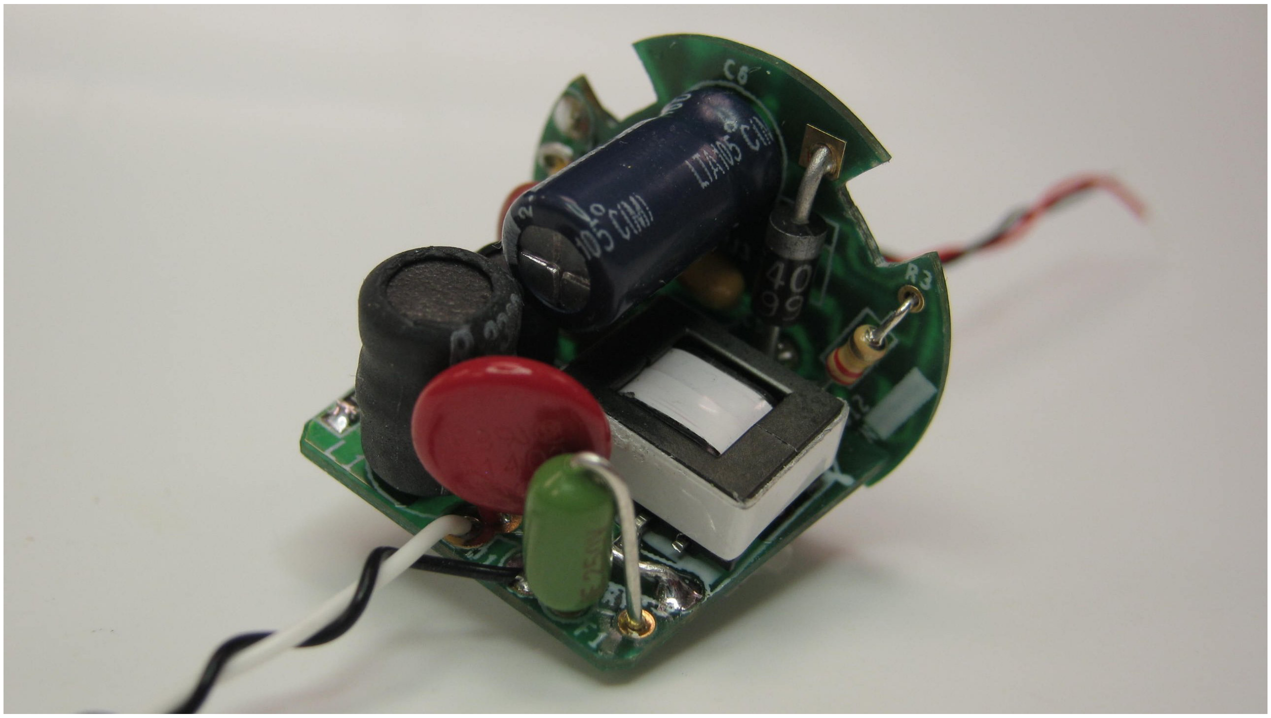

Figure 2 – Populated Circuit Board Assembly.

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2 Power Supply Specifications

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power Factor		0.95				At 115 VAC
%ATHD				25		
Output						
Output Voltage	V_{OUT}	200	230	253	V	
Output Current	I_{OUT}	28	30	32	mA	At 115 VAC
Total Output Power						
Continuous Output Power	P_{OUT}		7		W	
Efficiency						
Nominal	η		90		%	Measured at P_{OUT} 25 °C at 115 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			500		V	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω Short-Circuit Series Impedance

3 Schematic

Schematic is split into two sections representing the two PCBs used.

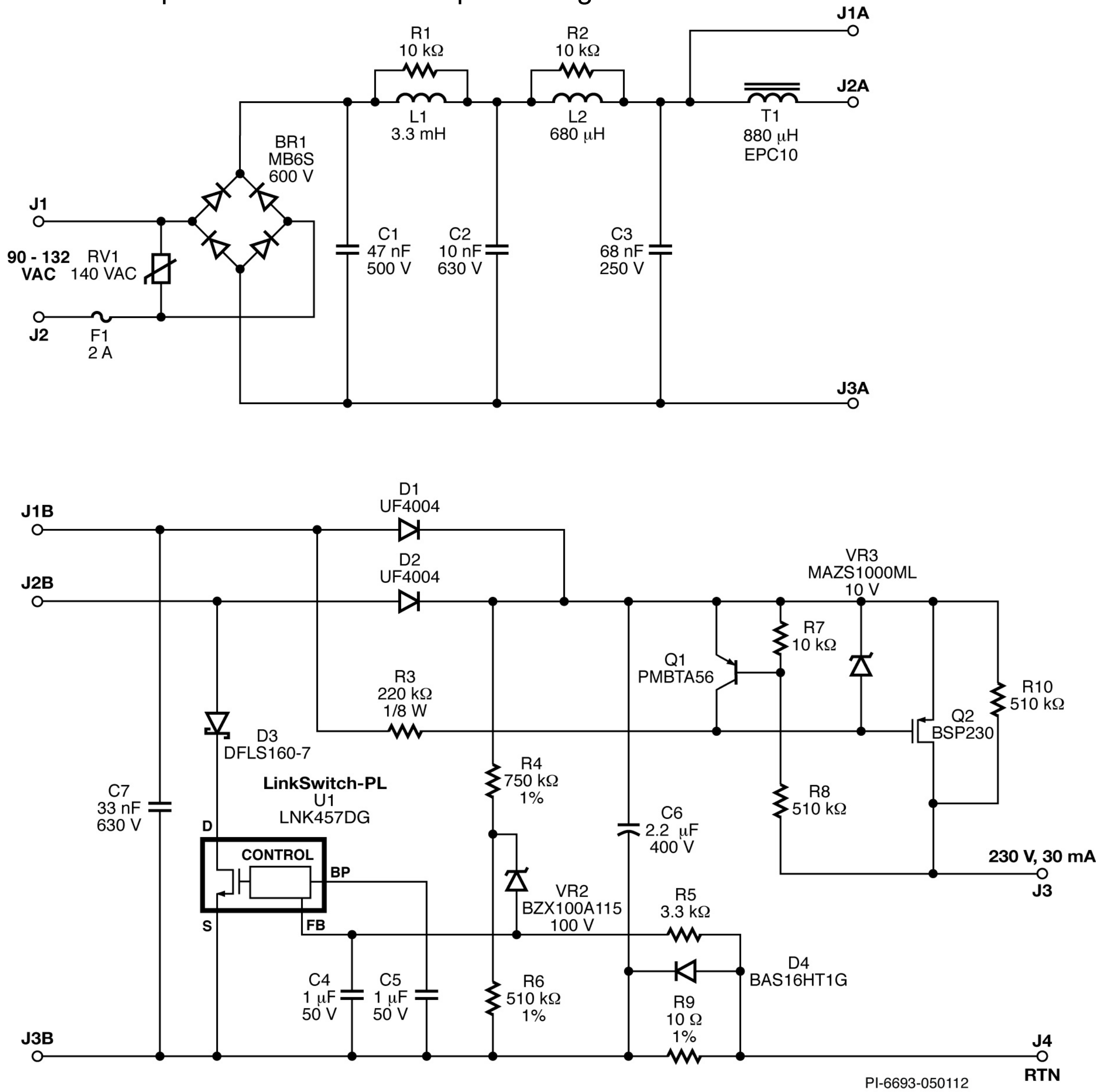

Figure 3 – Schematic for 230 V / 30 mA Replacement Lamp.

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4 Circuit Description

The LinkSwitch-PL (U1) family is highly integrated power ICs intended for use in LED driver applications. They LinkSwitch-PL provides high power factor in a single-stage conversion topology while regulating the output current across a range of input (90 VAC - 132 VAC) and output voltage variations typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus a high-voltage power MOSFET are incorporated into the IC.

4.1 Input Stage

Fuse F1 provides protection against component failure. A relatively high, fast 2 A rating was needed to prevent false opening during line surges. For lower cost at the expense of lower efficiency, the fuse may be replaced with a fusible resistor (2 W, 3.3 Ω).

The maximum input voltage is clamped by RV1 during differential line surges.

The AC input is full wave rectified by BR1 to achieve good power factor and THD.

Capacitor C1, C2, C3 and differential choke L1 and L2 form the EMI filter. Filter capacitance is limited to maintaining high power factor. This input 2-π filter network plus the frequency jittering feature of LinkSwitch-PL allows compliance with Class B emission limits. Resistors R1 and R2 damp the resonance of the EMI filter if needed, preventing peaks in the EMI spectrum when measured in a system (driver plus enclosure). Remove R1 and R2 if radiated EMI spectrum has significant margin in system level application.

- Inductor L1 and L2 are positioned after the bridge to avoid an imbalance in the EMI scan between line and neutral. This also gives sufficient leeway to use small high-voltage ceramic capacitors in the input filter.
- Inductor L2 can be increased from 680 μH to 2.2 mH to achieve more than 10 dBμV conducted EMI margin, at a cost of lower efficiency.

4.2 Boost Topology Using LinkSwitch-PL Devices

The boost power train is composed of U1 (power switch + control), D2 (boost diode), C6 (output capacitor), and T1 (inductor). Diode D3 was used to prevent negative voltage appearing across the drain-source of U1 especially near the zero-crossing of the input voltage. The bypass capacitor C5 provides the internal supply for U1, recharged via the drain during MOSFET off-time.

4.3 Output Feedback

The output current feedback is sensed by the voltage drop across R9 and then filtered by a low pass filter (R5 and C4) to keep the LinkSwitch-PL operating point such that the average FEEDBACK (FB) pin voltage is 290 mV in steady-state operation (30 mA output current).

4.4 Disconnected Load Protection

For this type of LED bulb application, disconnection of the LED load or output short-circuit represents a failure of the product. However, to prevent failure of C6 due to overvoltage R4, R5 and Zener VR2 regulate the output voltage (across C6) at <400 V during either condition. An output short-circuit creates a disconnect load condition due to the action of the short-circuit protection circuit (see following sections).

4.5 Line Surge Load Protection

All LED drivers should be protected from disturbances in the AC input such as line surges and swells. For the boost topology, once the input exceeds the output voltage the output will track the input voltage and output regulation is lost. With an LED load this allows an unregulated output current to flow limited only by the impedance of the LED load and input EMI filter. This uncontrolled current could damage or degrade the LED load.

In this design this was solved by Q2 which isolates the LED load during any event where the instantaneous input voltage is close to LED voltage.

MOSET Q2 is a small (SOT223 package, 17 Ω $R_{DS(ON)}$) P channel device with a gate threshold (V_{GSTH}) of -2.8 V_{TYP}. The source is connected to the 200 V output of the boost stage and the drain to the LED load. The gate is fed via R3 from the DC bus (voltage across C3). During normal operation the DC bus is <V_{OUT}, and the gate to source voltage is -10 V, clamped by VR3. In this condition Q2 is on and the driver delivers current to the LED load.

During a line surge the DC bus voltage rises and approaches V_{OUT}. When the difference between the DC bus and V_{OUT} is less than the V_{GSTH} of Q2 it turns off disconnecting the driver and protecting the LED load.

Once Q2 is off a potential difference appears between the LED driver output and the boost output voltage across C6. This difference causes Q1 to be biased on through R8, pulling the V_{GS} of Q2 to <V_{GSTH} and keeping it off. The line surge energy is stored in the relatively large value of output capacitance (C6), effectively clamping the DC bus voltage and V_{DS} of U1 to an acceptable level.

The high bus voltage also triggers cycle skipping operation of U1 via R4, R6 and VR2. This maintains the boost voltage within the output capacitor (C6) rating.

Once the line surge event ends, R10 discharges C6 through the LED load (at low current). Once the boost voltage return close to normal Q2 turns on and the driver operates normally.

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4.6 Short-Circuit Protection

The traditional boost converter topology is not protected against an output short-circuit. To provide this protection the line surge protection circuit is reutilized. Shorting the LED driver also isolates the boost converter output by turning off Q2. However as this is a latching shutdown the AC must be cycled to return the driver to normal operation.

5 PCB Layout

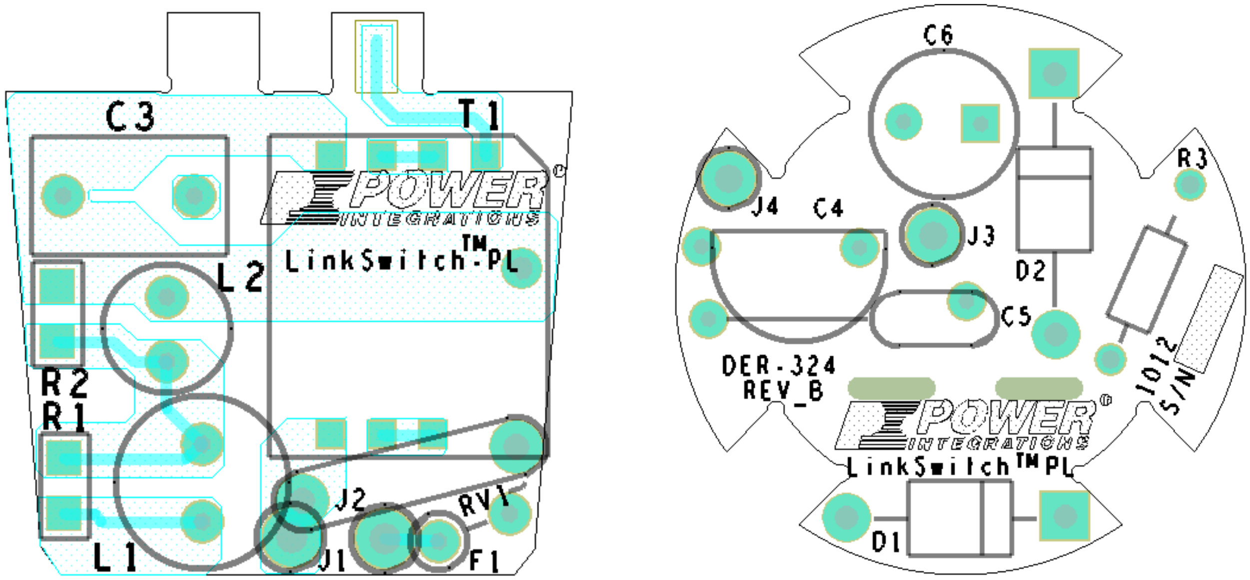

Figure 4 – Top Printed Circuit Layout.

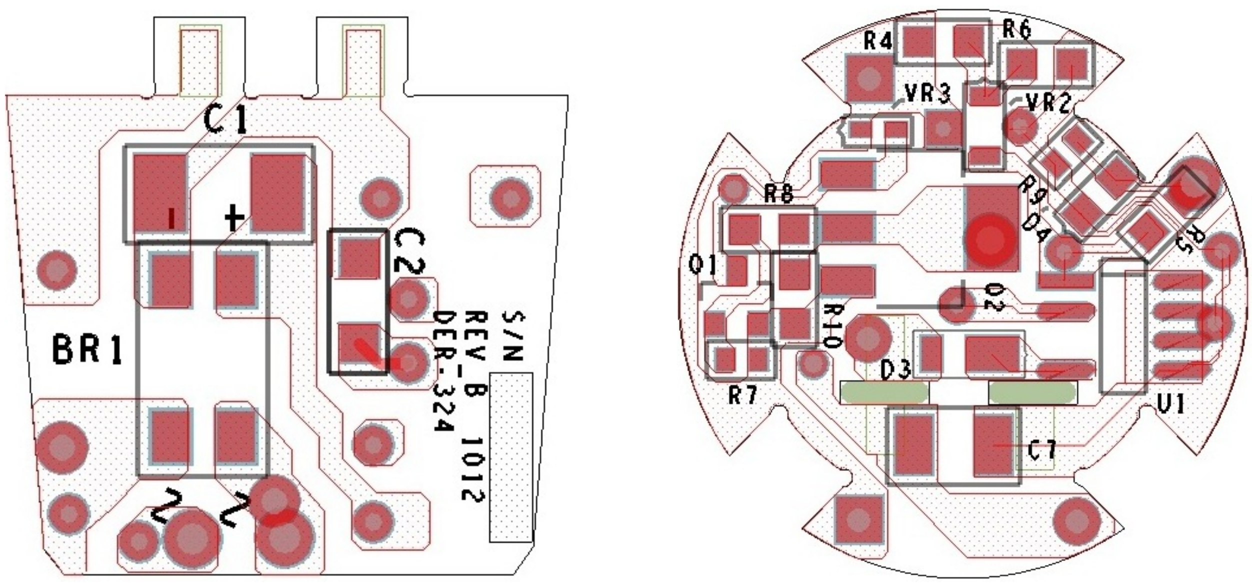

Figure 5 – Bottom Printed Circuit Layout.

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6 PCB Mechanical Outline

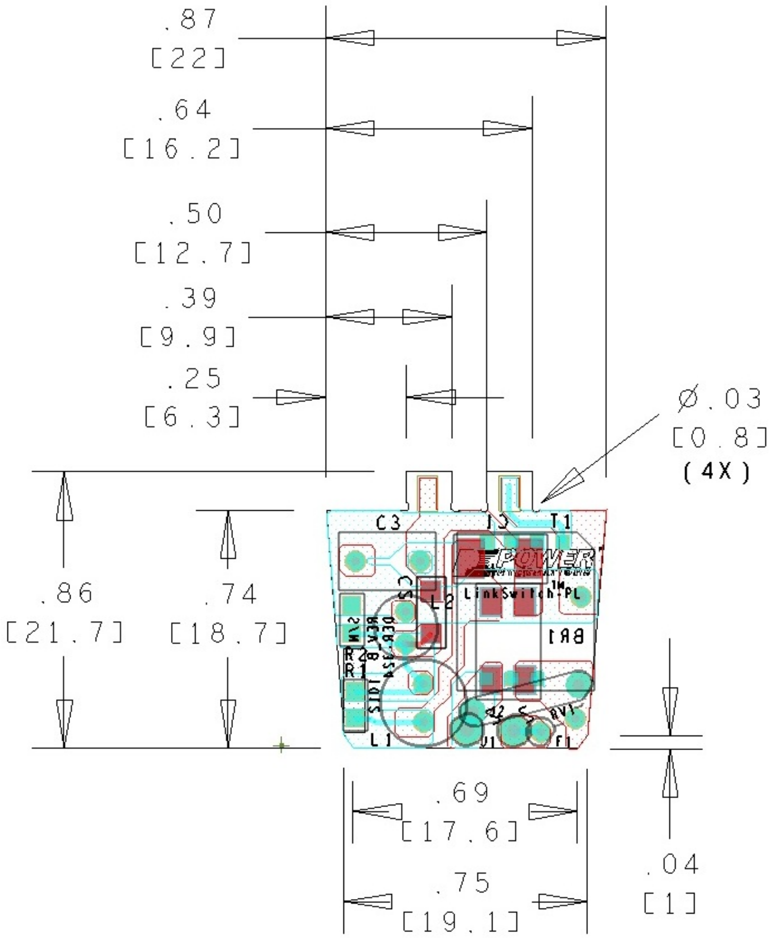

Figure 6 – Board 1 PCB Outline.

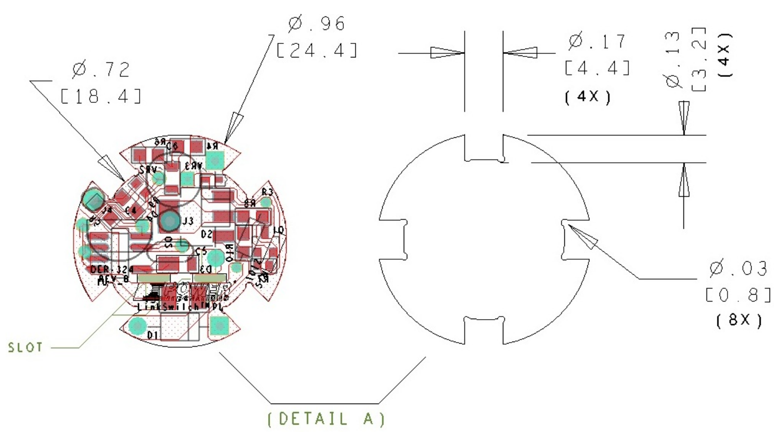

Figure 7 – Board 2 PCB Outline.

7 Populated PCB

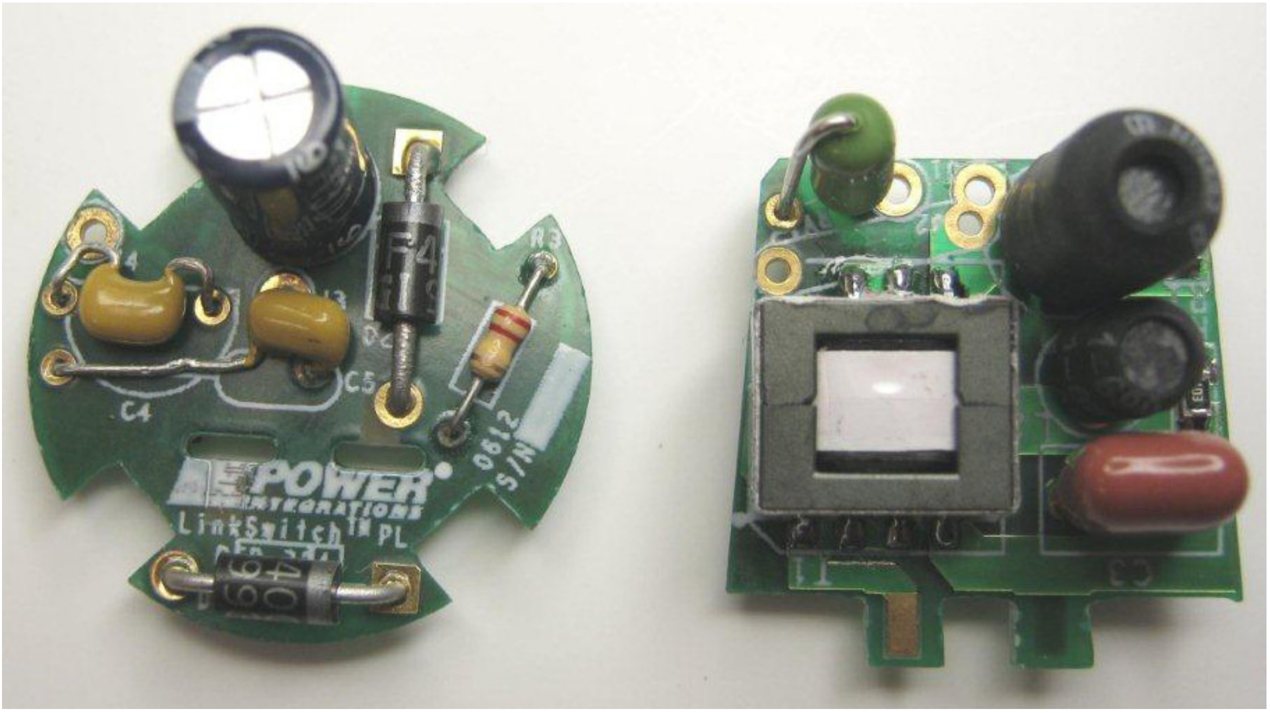

Figure 8 – Populated Circuit Board (top side).

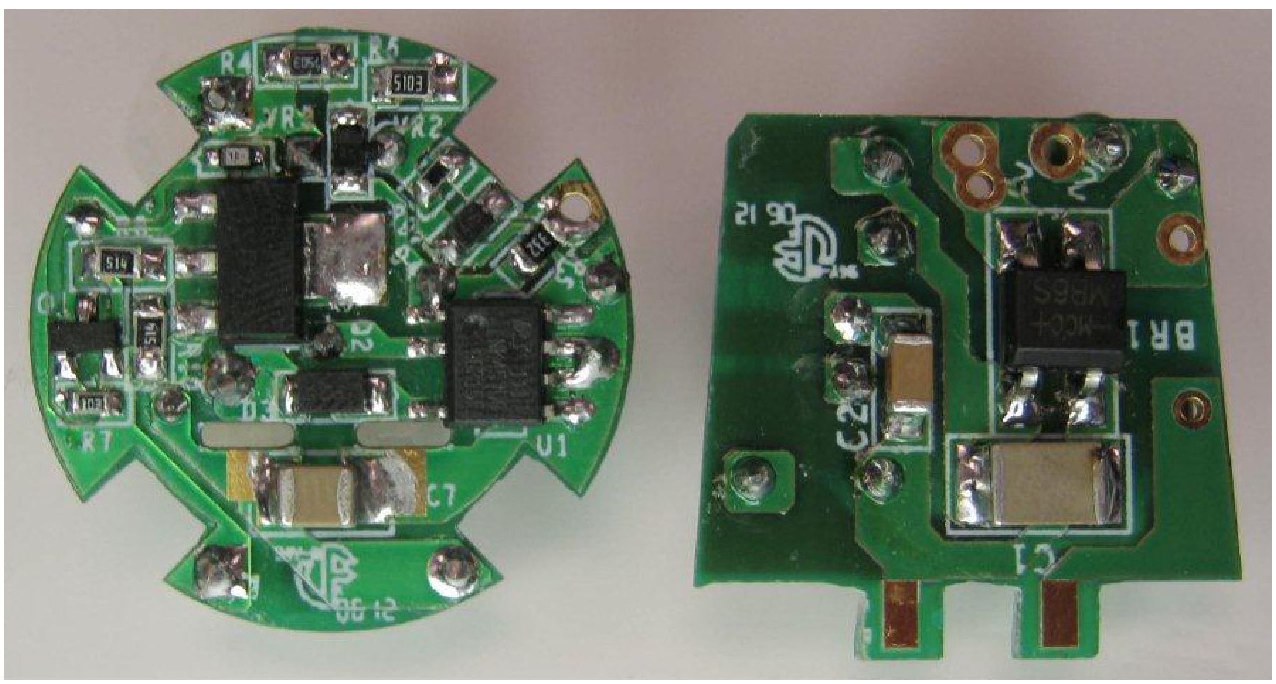

Figure 9 – Populated Circuit Board (bottom side).

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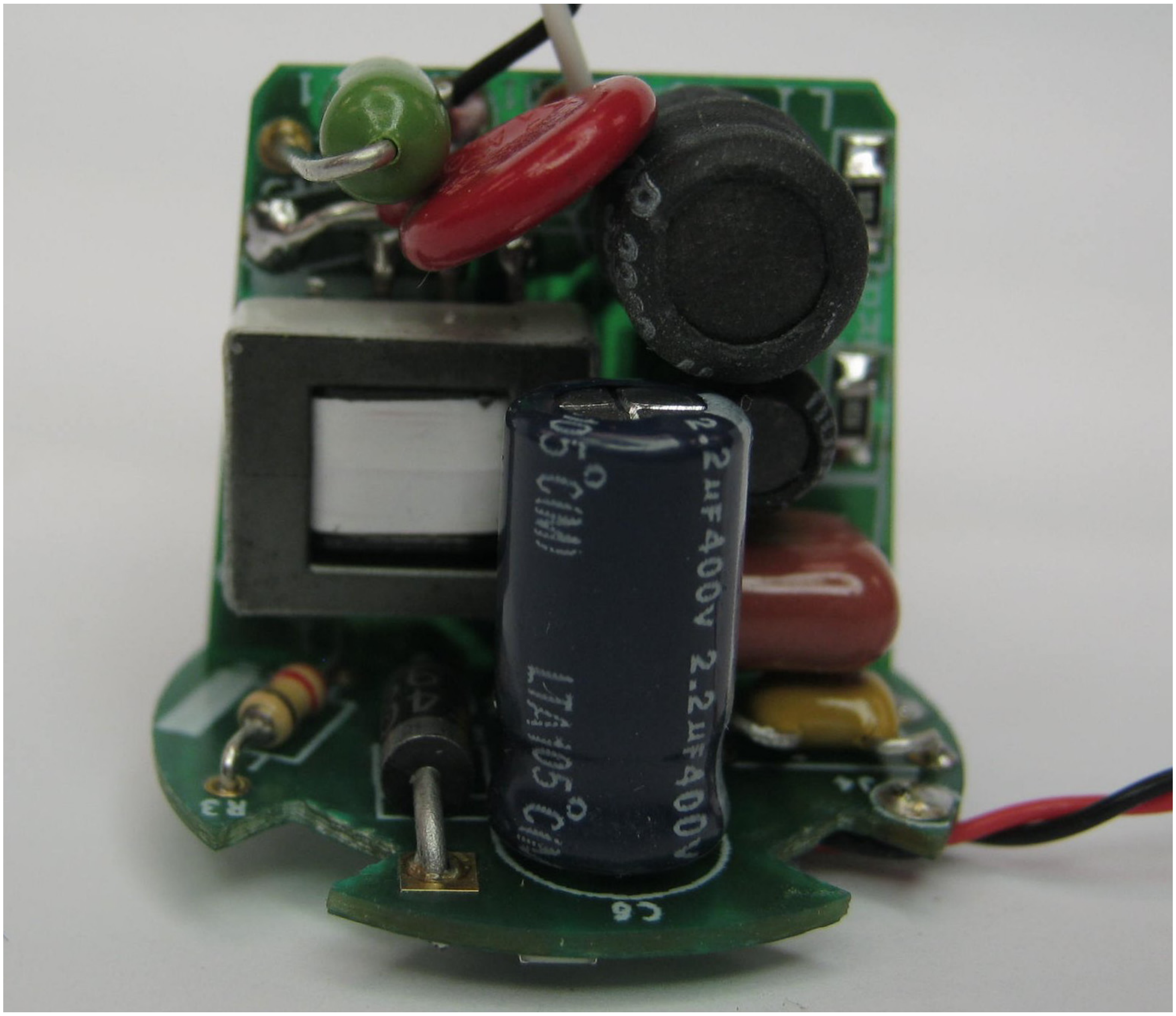

Figure 10 – PCB Assembly, Board 1 and Board 2 Combined.

8 Bill of Materials

The table below is the reference design BOM.

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	47 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y473KXEAT	Vishay
3	1	C2	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
4	1	C3	68 nF, 250 V, Polyester Film	ECQ-E2683KB	Panasonic
5	2	C4 C5	1.0 μF, 50 V, Ceramic, Z5U	B37988G5105M000	Epcos
6	1	C6	2.2 μF, 400 V, Electrolytic, (6.3 x 11)	TAB2GM2R2E110	Ltec
7	1	C7	33 nF, 630 V, Ceramic, X7R, 1210	GRM32DR72J333KW01L	Murata
8	2	D1 D2	400 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4004-E3	Vishay
9	1	D3	60 V, 1 A, Diode Schottky, PWRDI 123	DFLS160-7	Diodes, Inc.
10	1	D4	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	On Semi
11	1	F1	Fuse, Pico, 2 A, 250V,Fast, Axial	0263002.MXL	Littlefuse
12	1	L1	3.3 mH, 0.095 A, 20%	RL-5480-2-3300	Renco
13	1	L2	680 μH, 0.095 A, 20%	RL-5480-1-680	Renco
14	1	Q1	PNP, Small Signal BJT, 80 V, 0.5 A, SOT-23	PMBTA56 T/R	Philips
15	1	Q2	300 V, 210mA, P-Channel, SOT 223	BSP230,135	NXP Semi
16	2	R1 R2	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
17	1	R3	220 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-220K	Yageo
18	1	R4	750 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7503V	Panasonic
19	1	R5	3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
20	1	R6	510 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5103V	Panasonic
21	1	R7	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
22	2	R8 R10	510 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ514V	Panasonic
23	1	R9	10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
24	1	RV1	140 V, 12 J, 7 mm, RADIAL	V140LA2P	Littlefuse
25	1	T1	880 μH; EPC10; Custom made	BEPC-10-118GA	TDK
26	1	U1	LinkSwitch-PL, SO-8C	LNK457DG	Power Integrations
27	1	VR2	100 V, 5%, 310 mW, SOD-323	BZX100A,115	NXP Semi
28	1	VR3	10 V, 5%, 150 mW, SSMINI-2	MAZS1000ML	Panasonic

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9 Inductor Specification

9.1 Electrical Diagram

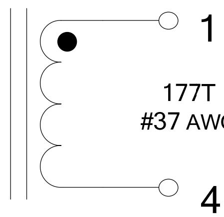

Figure 11 – Transformer Electrical Diagram.

9.2 Electrical Specifications

Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	880 µH ±5%

9.3 Materials

Item	Description
[1]	Core: EPC-10; TDK-PC44EPC10Z or equivalent.
[2]	Bobbin: EPC-10 SMD; 4/4 pin (TDK: BEPC-10-118GA or equivalent).
[3]	Magnet Wire: #37 AWG.
[4]	Tape, Polyester film, 3M 1350F-1 or equivalent, 4 mm wide.
[5]	Loctite Super Glue Control Gel.

9.4 Inductor Build Diagram

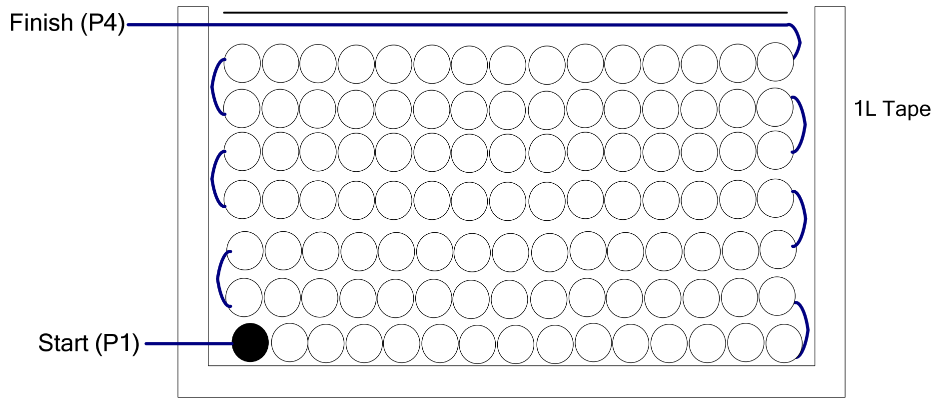

Figure 12 – Inductor Build Diagram.

9.5 Inductor Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise.
WDG 1	Start at pin 1. Wind enough turns of item [3] and terminate at pin 4. Note: 1 layer tape [4] avoids possible insulation break of the winding and ensure guide of termination.
Final Assembly	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pin 8. Apply adhesive item [5] to core and bobbin to prevent core movement.

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10 Performance Data

All measurements performed at 25 ºC room temperature, 60 Hz input frequency unless otherwise specified.

10.1 Active Mode Efficiency

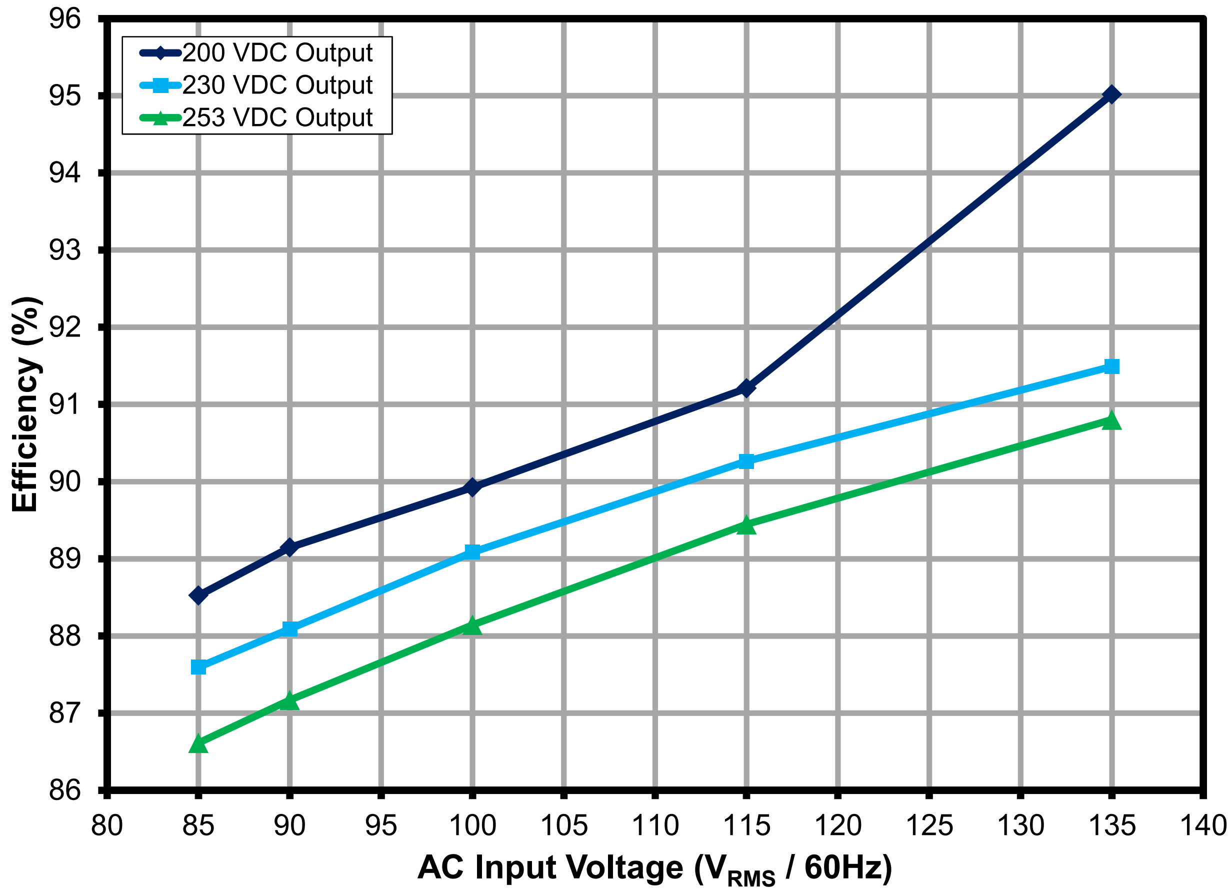

Figure 13 – Efficiency with Respect to AC Input Voltage at 30 mA.

10.2 Line Regulation

The LinkSwitch-PL device regulates the output by controlling the power MOSFET on-time and switching frequency to maintain the average FEEDBACK pin at its 0.29 V threshold. Slight changes in output current may be observed when input or output conditions are changed or after AC cycling due to the device selecting a slightly different operating state (selection of on-time and frequency).

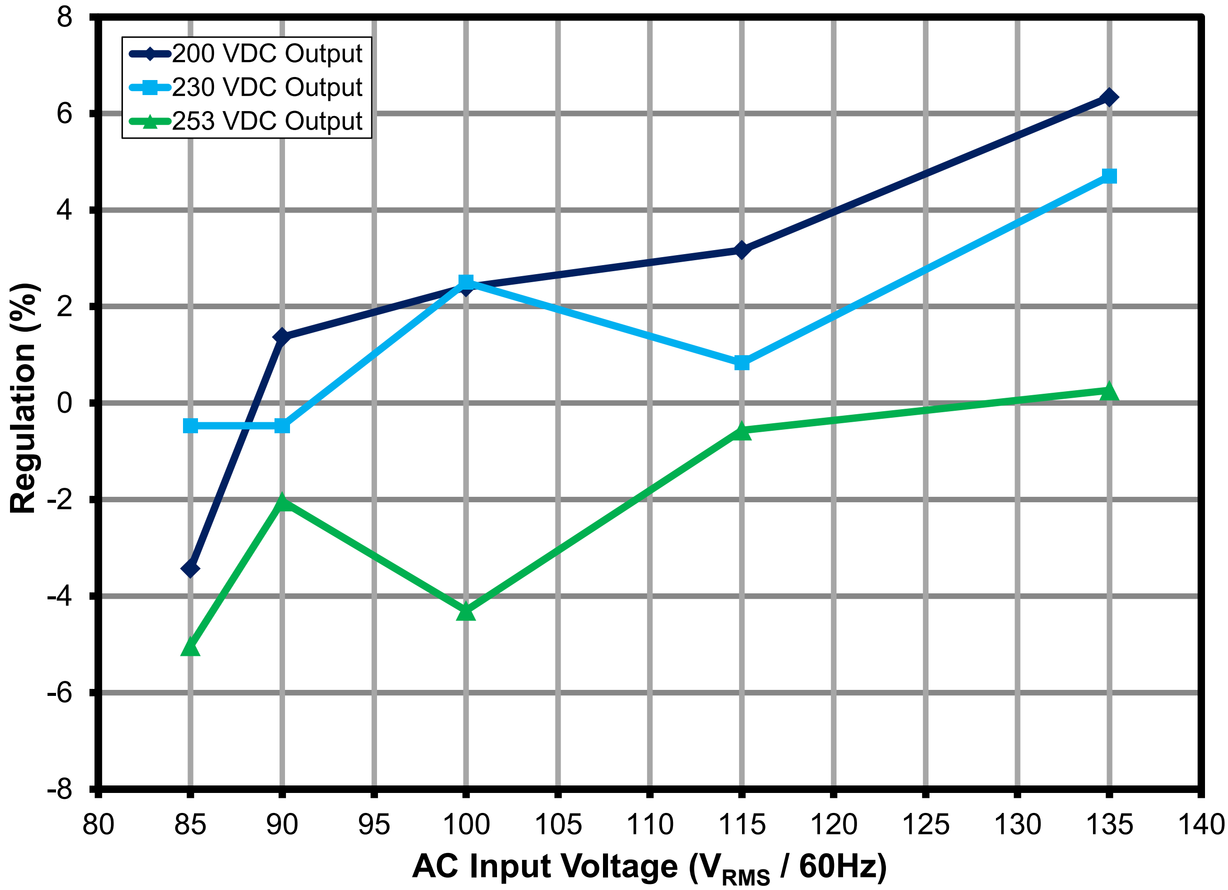

Figure 14 – Line Regulation, Room Temperature.

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10.3 Power Factor

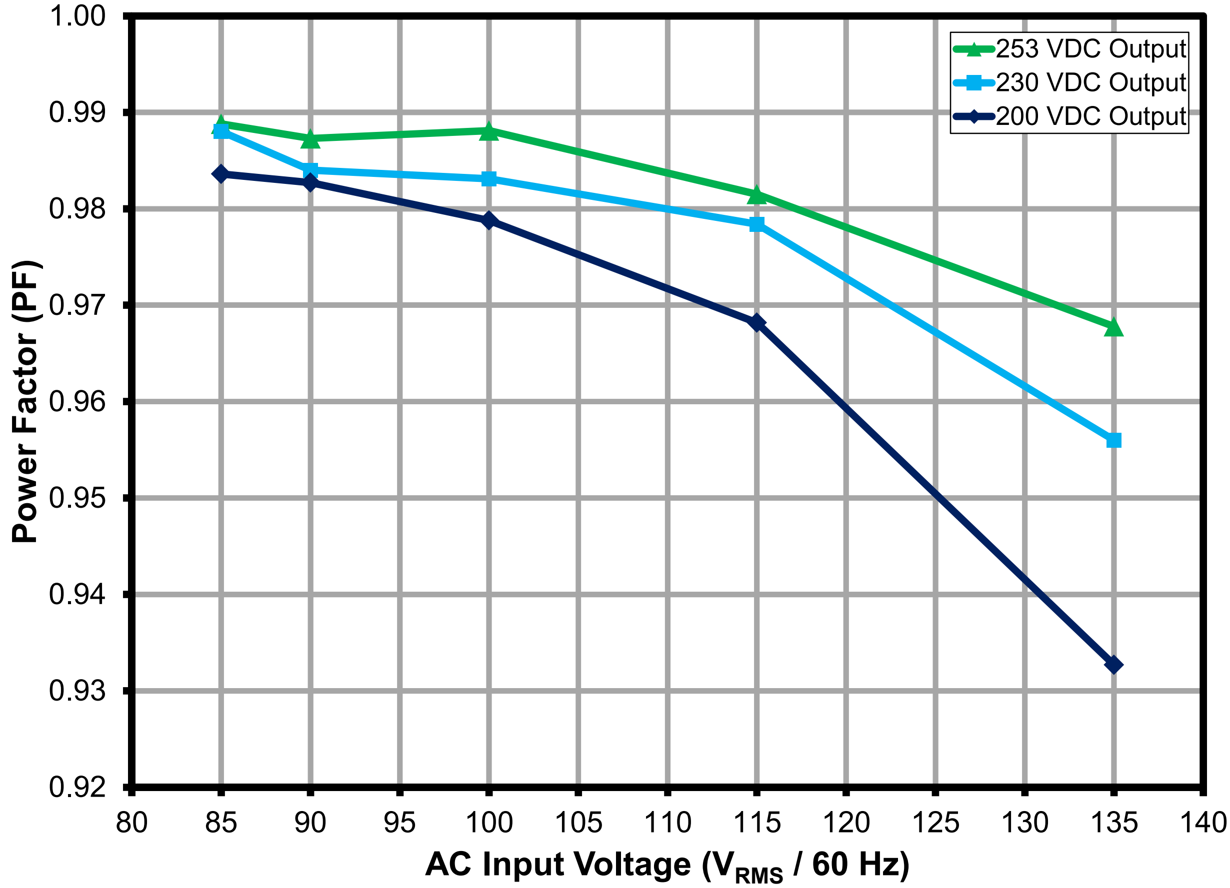

Figure 15 – High Power Factor within the Operating Range for 230 V LED.

10.4 %THD

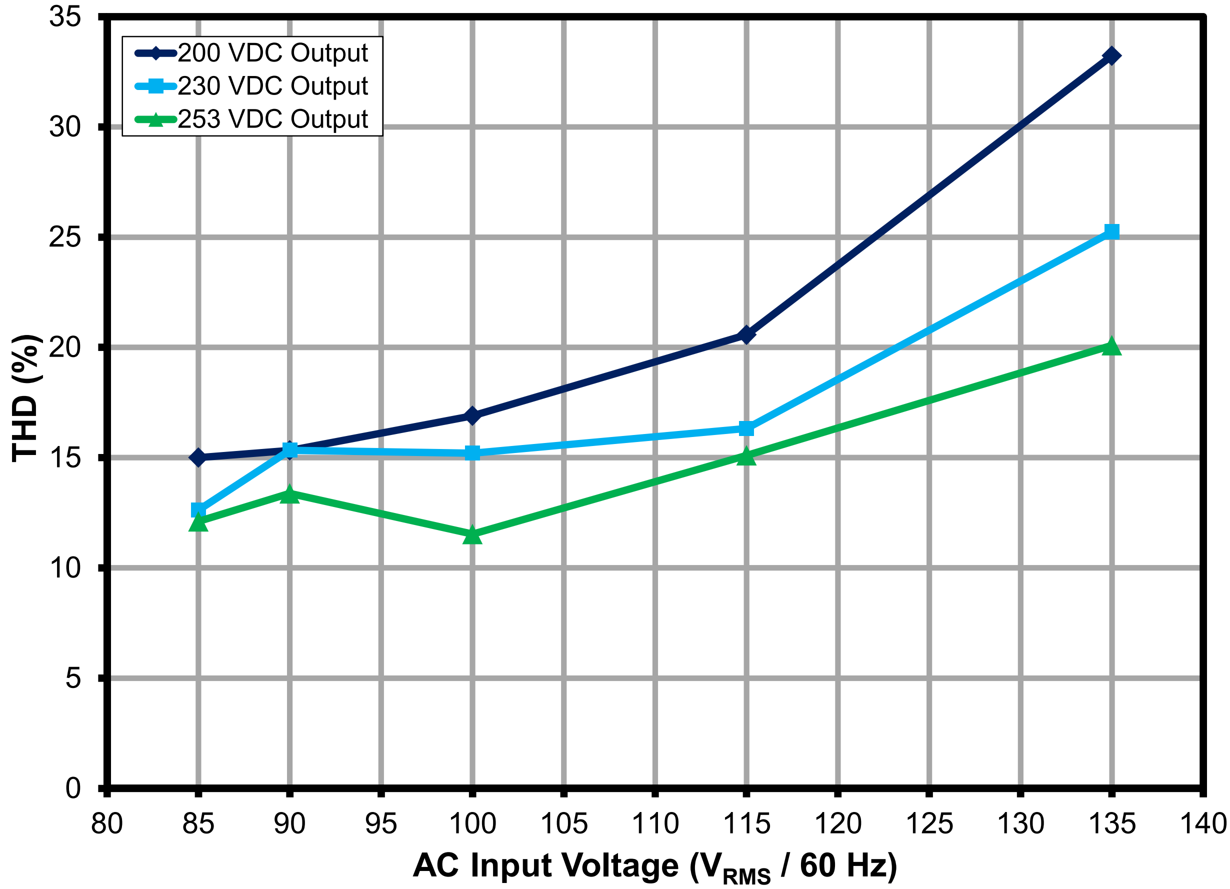

Figure 16 – Very Low %ATHD at 115 VAC.

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10.5 Harmonic Content

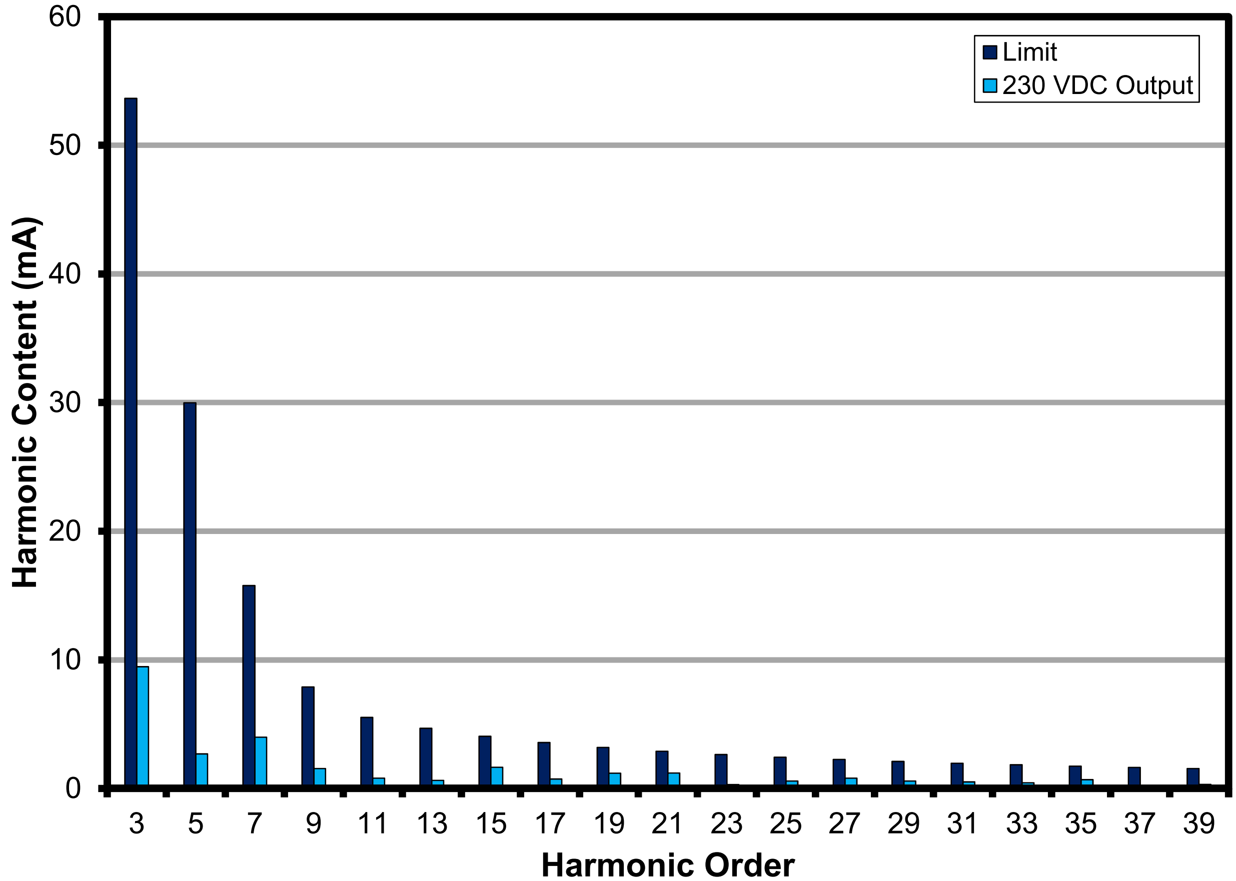

Figure 17 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating for 230 V LED Output.

10.6 Harmonic Measurements

There are no requirement standards for 115 V input harmonic contents but this engineering sample design illustrates how good the input current waveform is.

VAC (V_{RMS})	Freq (Hz)	I (mA)	P	PF
115	**60**	47.90	5.2690	0.9568
nth Order	**mA Content**	**% Content**	**Limit (mA) <25 W**	**Remarks**
1	68.91			
2	0.33	0.48%		
3	9.46	13.73%	53.6384	**Pass**
5	2.69	3.90%	29.9744	**Pass**
7	3.98	5.78%	15.7760	**Pass**
9	1.55	2.25%	7.8880	**Pass**
11	0.81	1.18%	5.5216	**Pass**
13	0.64	0.93%	4.6721	**Pass**
15	1.66	2.41%	4.0492	**Pass**
17	0.73	1.06%	3.5728	**Pass**
19	1.19	1.73%	3.1967	**Pass**
21	1.21	1.76%	2.8923	**Pass**
23	0.30	0.44%	2.6408	**Pass**
25	0.59	0.86%	2.4295	**Pass**
27	0.80	1.16%	2.2495	**Pass**
29	0.58	0.84%	2.0944	**Pass**
31	0.52	0.75%	1.9593	**Pass**
33	0.45	0.65%	1.8405	**Pass**
35	0.68	0.99%	1.7354	**Pass**
37	0.20	0.29%	1.6416	**Pass**
39	0.32	0.46%	1.5574	**Pass**
41	0.34	0.49%		
43	0.18	0.26%		
45	0.34	0.49%		
47	0.11	0.16%		
49	0.13	0.19%		

Table 1 –115 VAC Input Current Harmonic Measurement for 230 V LED.

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10.7 Thermal Scans

The scan is conducted at ambient temperature of 25 ºC, 90 VAC / 47 Hz input.

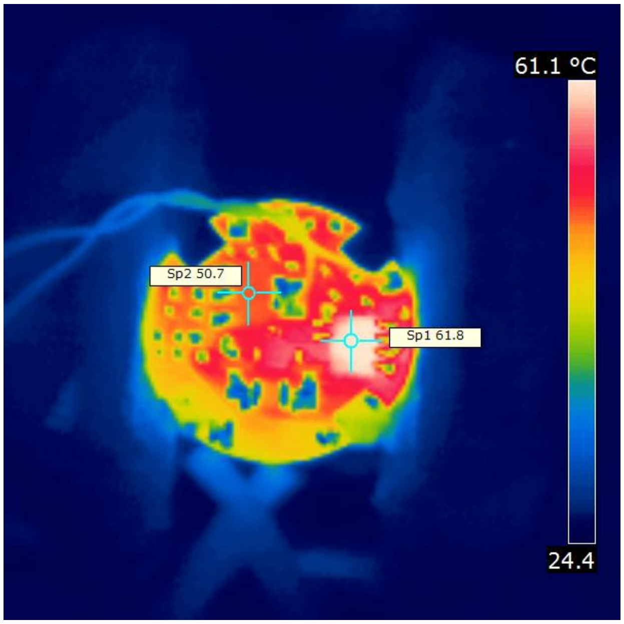

Figure 18 – U1 Case Temperature (Sp1).
Q2 Case Temperature (Sp2).

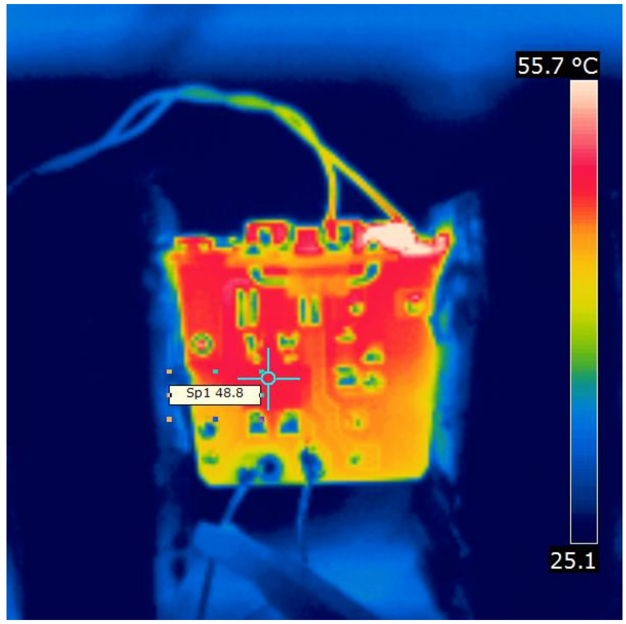

Figure 19 – BR1 Bridge Rectifier (Sp1).

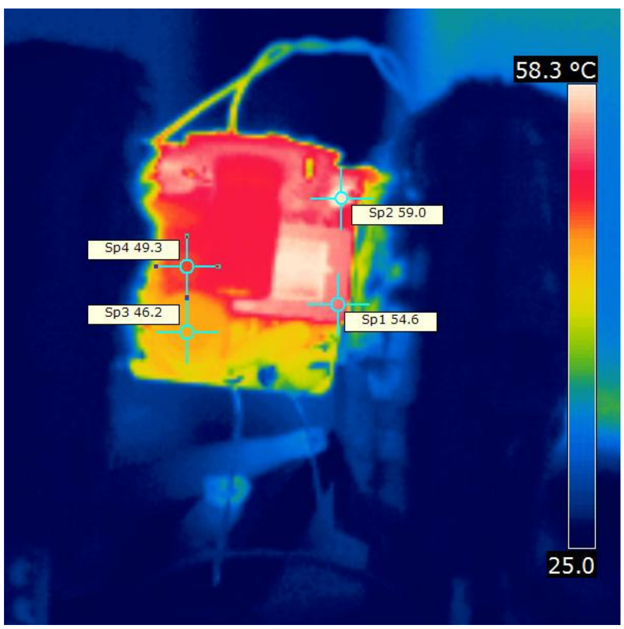

Figure 20 – T1 Core Temperature (Sp1).
D2 Boost Diode (Sp2).
L1 EMI Choke (Sp3).
L2 EMI Choke (Sp4).

11 Thermal Performance

11.1 Equipment Used

Chamber:	Tenney Environmental Chamber Model No: TJR-17 942
AC Source:	Chroma Programmable AC Source Model No: 6415
Wattmeter:	Yokogawa Power Meter Model No: WT2000
Data Logger:	Yokogawa MV2000

Figure 21 – Thermal Chamber Set-up Showing Box Used to Prevent Airflow Over UUT.

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11.2 Thermal Results

11.2.1 Normal Operation

Load: 230 V / 30 mA LED load.
Ambient of 75 °C simulates operation inside sealed LED replacement enclosure. The unit was verified inside a B10 enclosure (LED load was outside the chamber).

Component	Device Temperature (ºC)					
	90 VAC / 50 Hz			132 VAC / 50 Hz		
Case External Ambient	25	50	75	25	50	75
Bridge (BR1)	45.2	74.7	100	45	74	99.1
Boost Diode (D1)	43.3	75	101.1	45.4	76	102
LNK457DG (U1)	48.3	79.1	105.7	48.2	78.9	105.5
Inductor Core (T1)	49.3	81.4	109.4	49.3	81.3	109.2
Output FET (Q2)	39	70.3	96.3	41.7	42	96.5

Table 2 – Thermal Data, No Potting.

11.2.2 Thermal Shutdown and Recovery

LED Load: 230 VDC / 30 mA
The unit was verified inside a B10 enclosure (LED load was outside the chamber). Chamber temperature was ramped at 0.25 ºC/min.

The data showed operation at an external ambient of up to 94.5 °C, with the hottest component the LinkSwitch-PL IC (U1). This indicates excellent thermal margin and demonstrates that U1 provides system level thermal protection.

Normal Operation	Device Temperature (ºC)	
	90 VAC / 50 Hz	
Component	**Thermal Shutdown**	**Thermal Recovery**
Case External Ambient	94.5	48.1
Bridge (BR1)	120.9	65.5
Boost Diode (D1)	123	58.3
LNK457DG (U1)	129.2	59.7
Inductor Core (T1)	131.8	66.5
Output FET (Q2)	119.6	53.1

Table 3 – Key Component Temperatures at Maximum External Operating Case Temperature.

12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

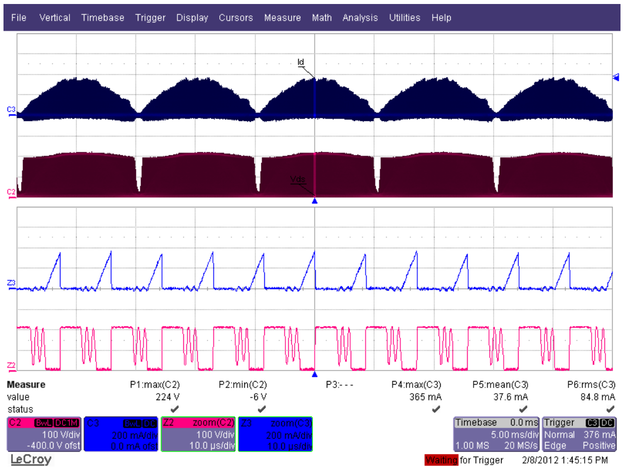

Figure 22 – 90 VAC / 50 Hz, 200 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

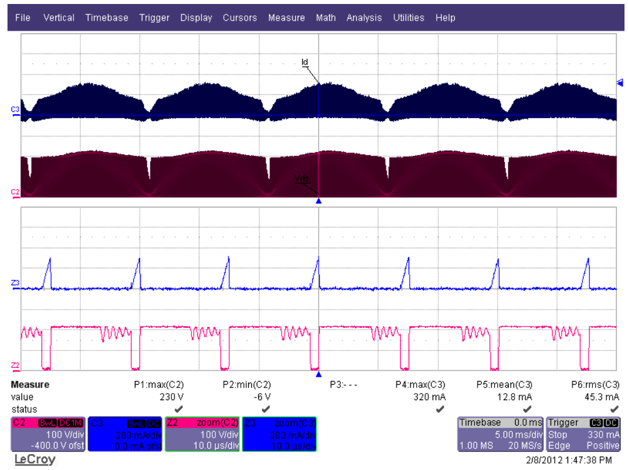

Figure 23 – 132 VAC / 50 Hz, 200 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale:5 ms / div.
Zoom Time Scale: 10 μs / div.

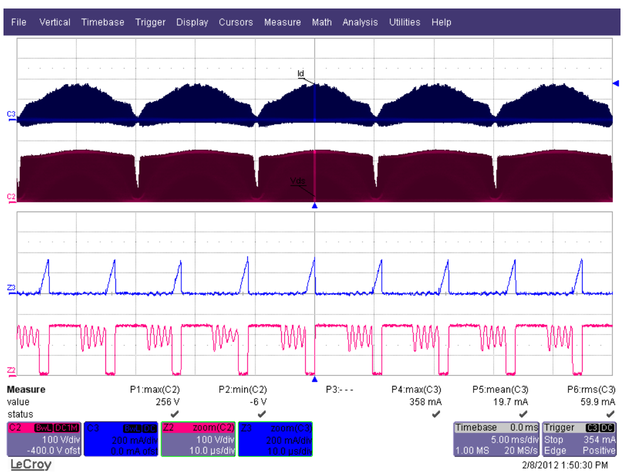

Figure 24 – 90 VAC / 50 Hz, 230 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

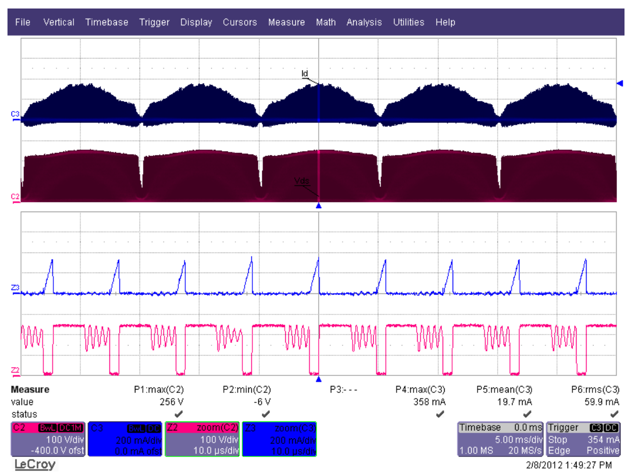

Figure 25 – 132 VAC / 50 Hz, 230 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale:5 ms / div.
Zoom Time Scale: 10 μs / div.

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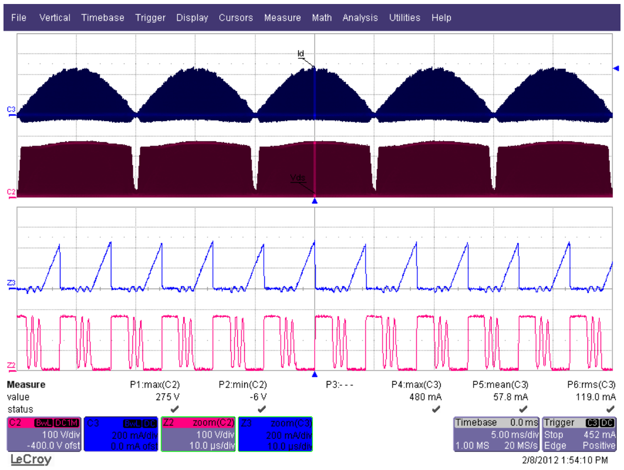

Figure 26 – 90 VAC / 50 Hz, 253 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

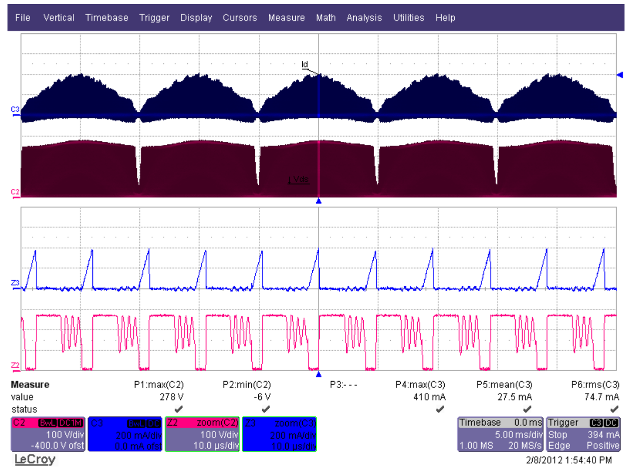

Figure 27 – 132 VAC / 50 Hz, 253 V LED String.
Ch2: V_{DRAIN}, 100 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale:5 ms / div.
Zoom Time Scale: 10 μs / div.

12.2 Drain Voltage and Current Start-up Profile

Start-up time <50 ms

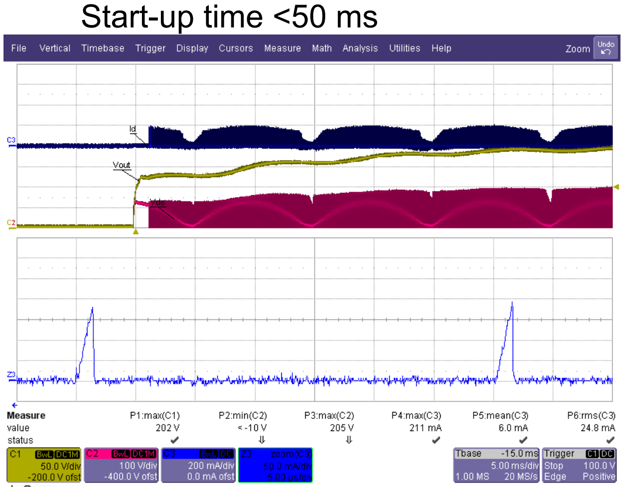

Figure 28 – 90 VAC / 50 Hz, 200 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div.

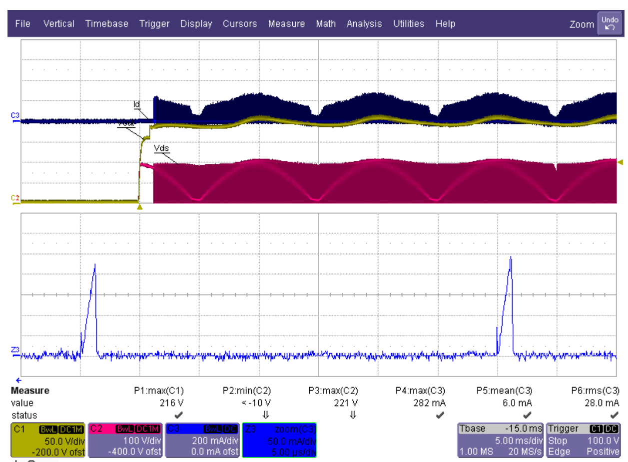

Figure 29 – 132 VAC / 50 Hz, 200 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div.

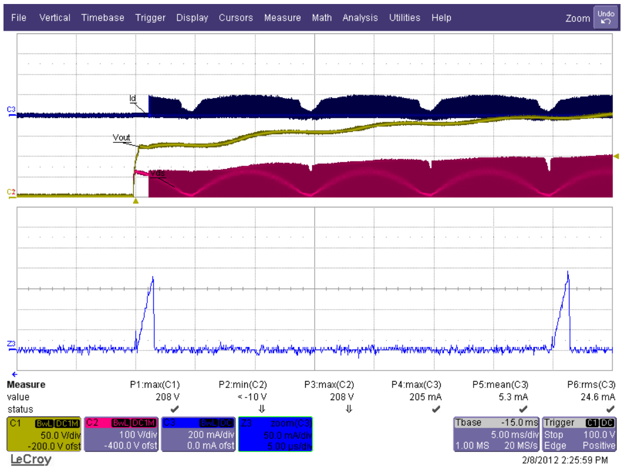

Figure 30 – 90 VAC / 50 Hz, 230 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div

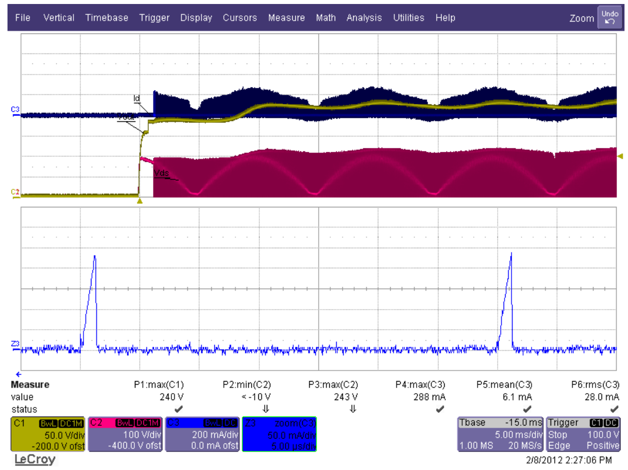

Figure 31 – 132 VAC / 50 Hz, 230 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div.

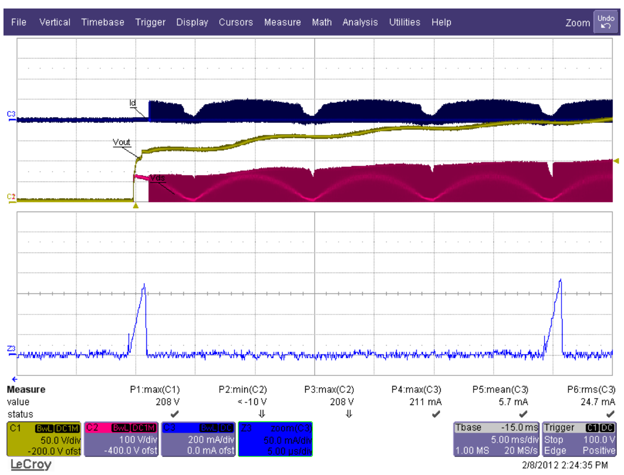

Figure 32 – 90 VAC / 50 Hz, 253 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div

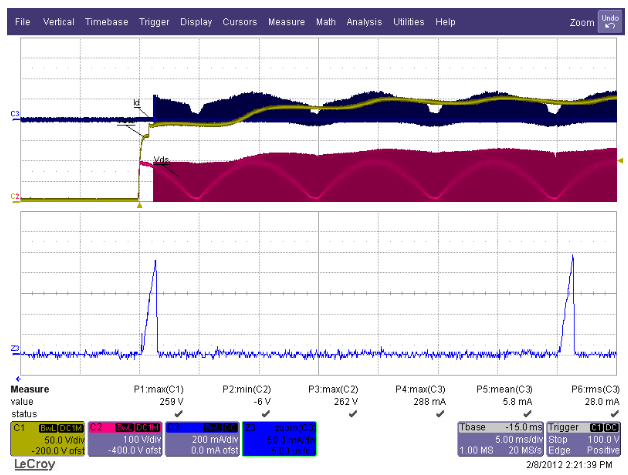

Figure 33 – 132 VAC / 50 Hz, 253 V LED String.
Ch1: V_{OUT}, 50 V / div.
Ch2: V_{DS}, 100 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale:5 ms / div.
Zoom Time Scale: 5 μs / div.

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12.3 Output Voltage Start-up Profile

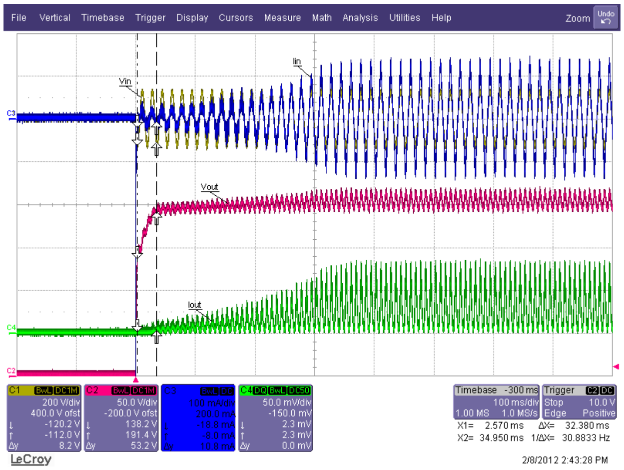

Figure 34 – 90 VAC / 60 Hz, 200 V LED
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

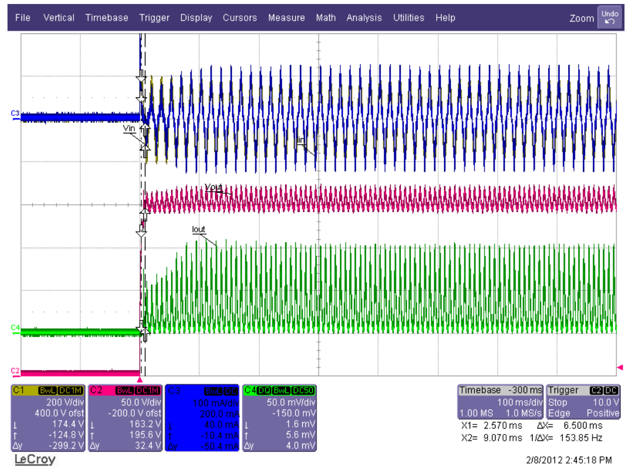

Figure 35 – 132 VAC / 60 Hz, 200 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

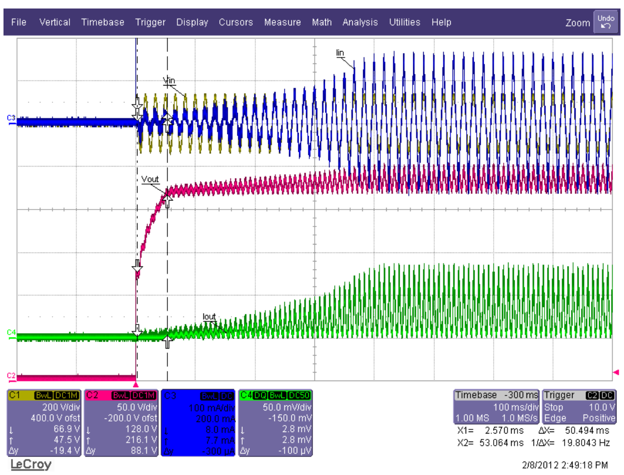

Figure 36 – 90 VAC / 60 Hz, 230 V LED
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

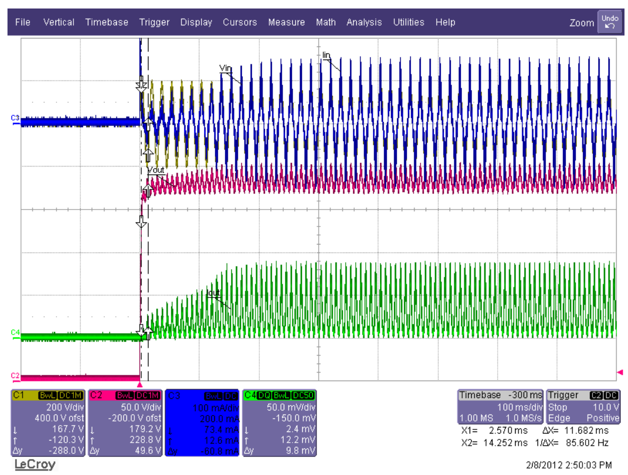

Figure 37 – 132 VAC / 60 Hz, 230 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

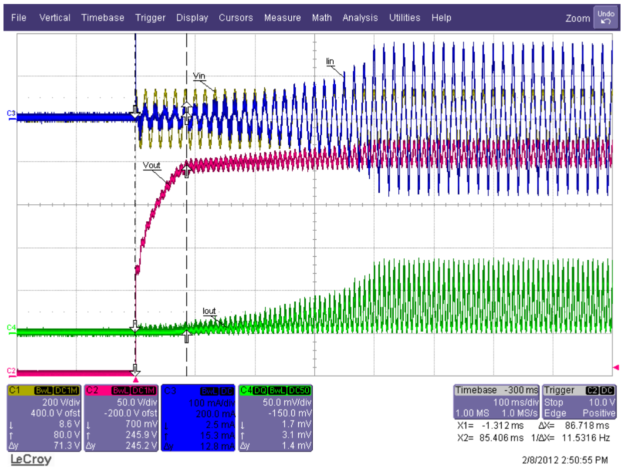

Figure 38 – 90 VAC / 60 Hz, 253 V LED
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

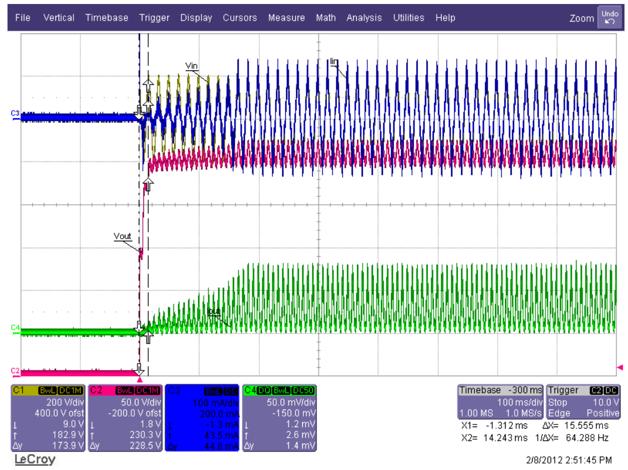

Figure 39 – 132 VAC / 60 Hz, 253 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 50 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 100 ms / div.

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12.4 Input and Output Voltage and Current Profiles

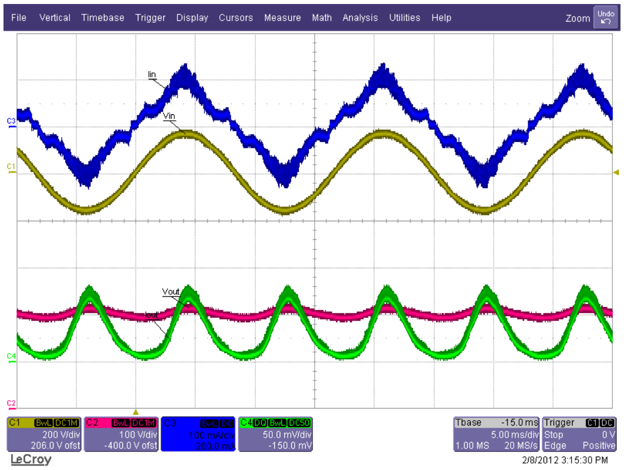

Figure 40 – 115 VAC / 50 Hz, 200 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 5 ms / div.

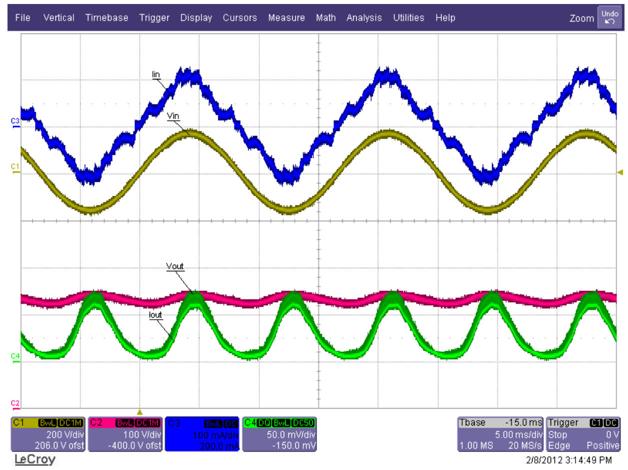

Figure 41 – 115 VAC / 50 Hz, 230 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 5 ms / div.

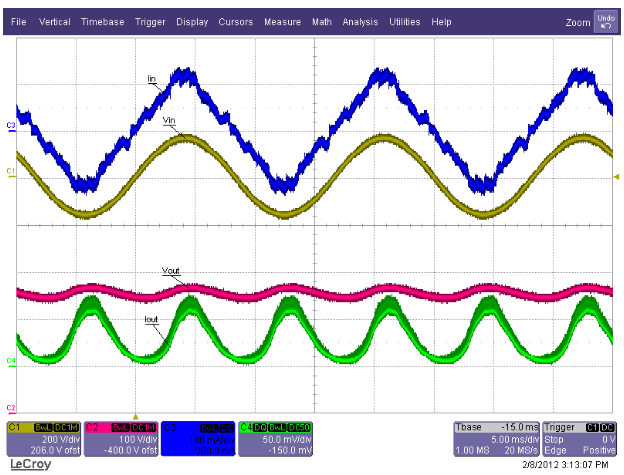

Figure 42 – 115 VAC / 50 Hz, 253 V LED String.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{IN}, 100 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 50 mA / div., 5 ms / div.

12.5 Drain Voltage and Current Profile: Normal Operation to Output Short

During an output short-circuit, the boost converter is isolated from the LED load via Q2 to prevent driver failure. Once isolated, the boost output voltage is regulated using the cycle skipping feature of U1.

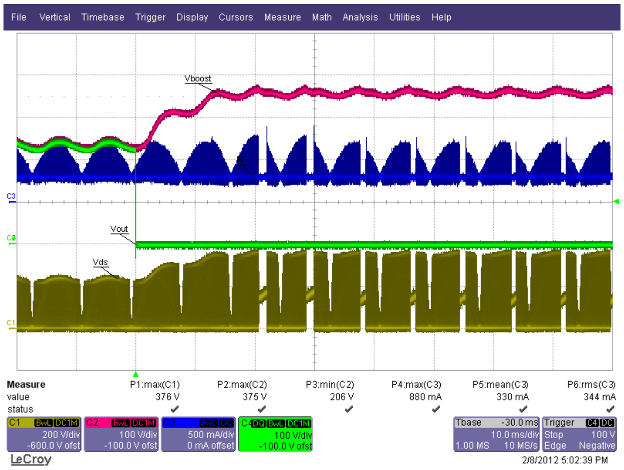

Figure 43 – 90 VAC / 60 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST-OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 10 ms / div.

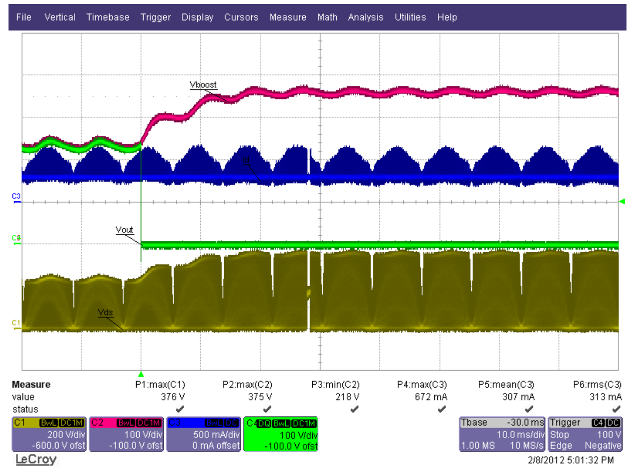

Figure 44 – 132 VAC / 60 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST-OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 10 ms / div..

12.6 Drain Voltage and Current Profile: Start-up with Output Shorted

During start-up short-circuit, the boost converter is isolated from the short via Q2.

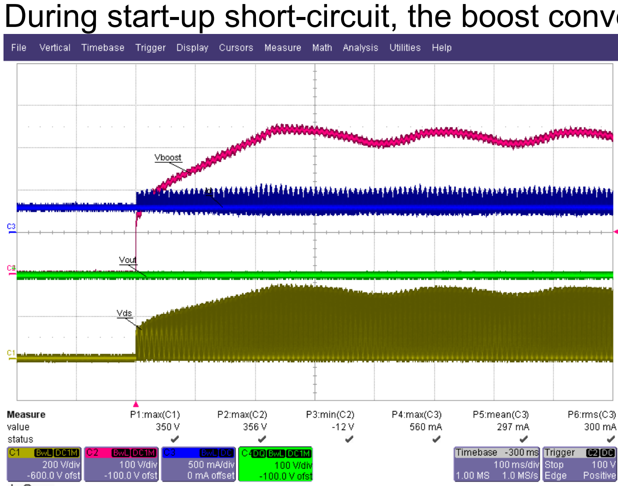

Figure 45 – 90 VAC / 60 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST-OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 100 ms / div.

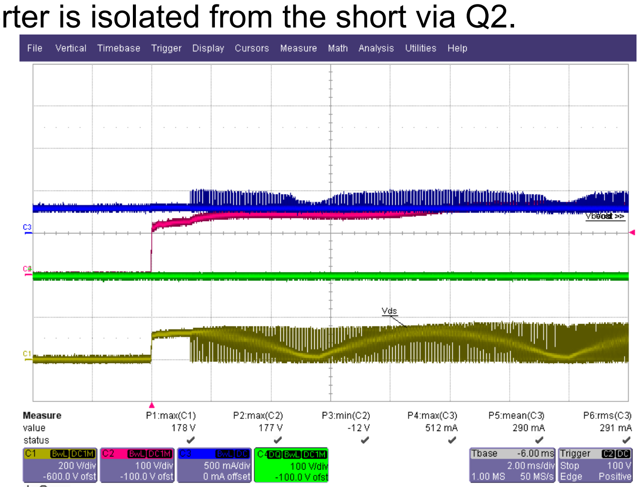

Figure 46 – 90 VAC / 60 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST-OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 2 ms / div.

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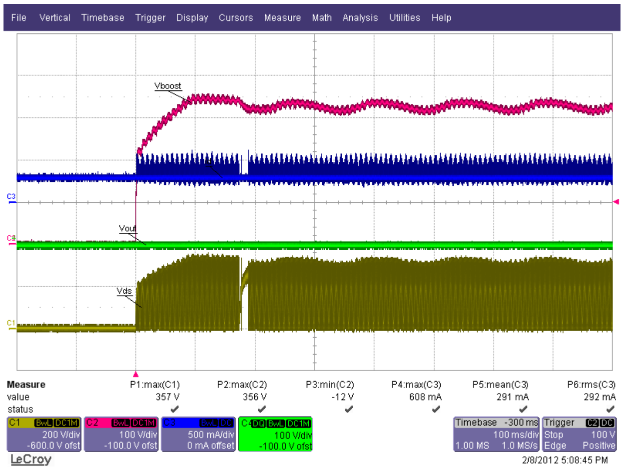

Figure 47 – 132 VAC / 60 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST\text{-}OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 100 ms / div.

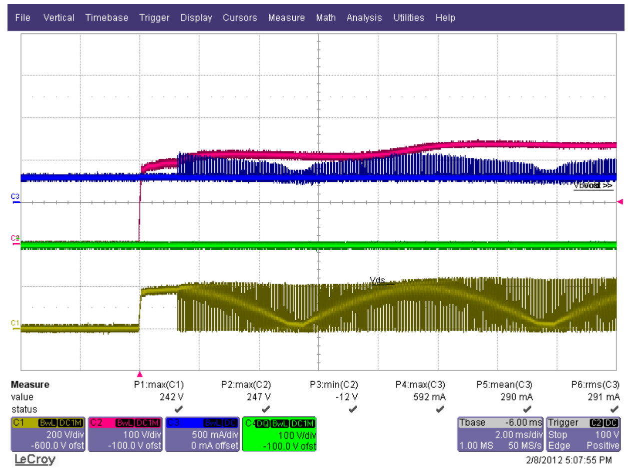

Figure 48 – 132 VAC / 60 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: $V_{BOOST\text{-}OUTPUT}$, 100 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT} , 100 V / div., 2 ms / div.

12.7 No-Load Operation

The driver is protected during no-load operation, U1 operating is cycle skipping mode.

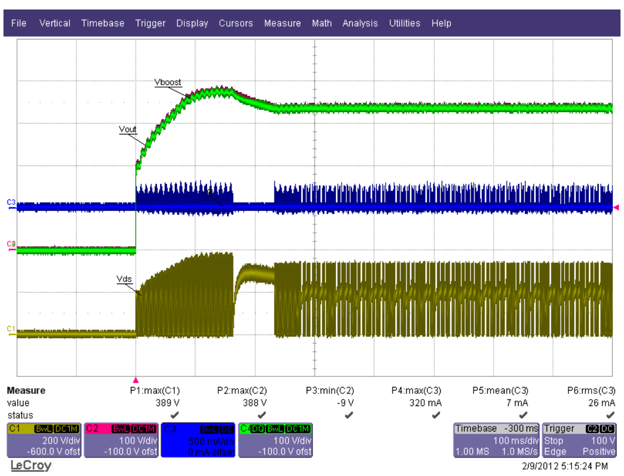

Figure 49 – 132 VAC / 60 Hz, Start-up No-load.
Ch1: V_{OUT}, 200 V / div.
Ch2: $V_{BOOST\text{-}OUTPUT}$, 100 V / div.
Ch2: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT}, 100 V / div.
Time Scale: 100 ms / div.

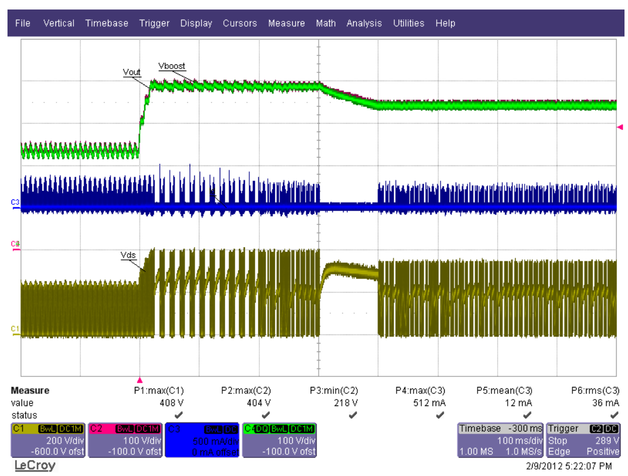

Figure 50 – 132 VAC / 60 Hz, Disconnected Load.
Ch1: V_{OUT}, 200 V / div.
Ch2: $V_{BOOST\text{-}OUTPUT}$, 100 V / div.
Ch2: I_{DRAIN}, 0.5 A / div.
Ch4: V_{OUT}, 100 V / div.
Time Scale: 100 ms / div.

12.8 AC Cycling

Advantage of a boost converter as compared to other topology is the fast start-up; the output capacitor is charged as soon as AC input is present.

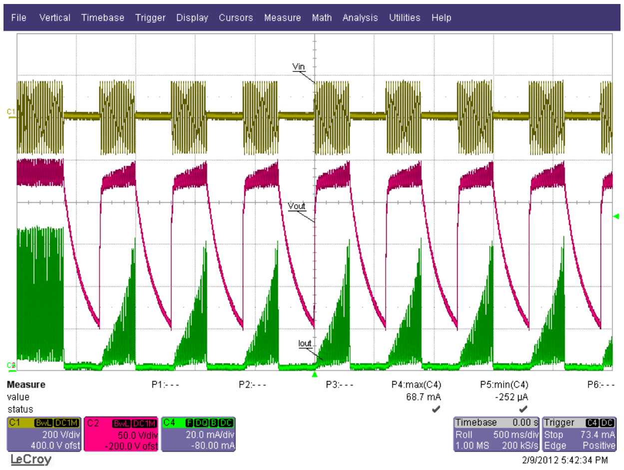

Figure 51 – 115 VAC / 50 Hz,
300 ms On – 300 ms Off.
Load: 230 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 20 mA / div.
Time Scale: 0.5 s / div.

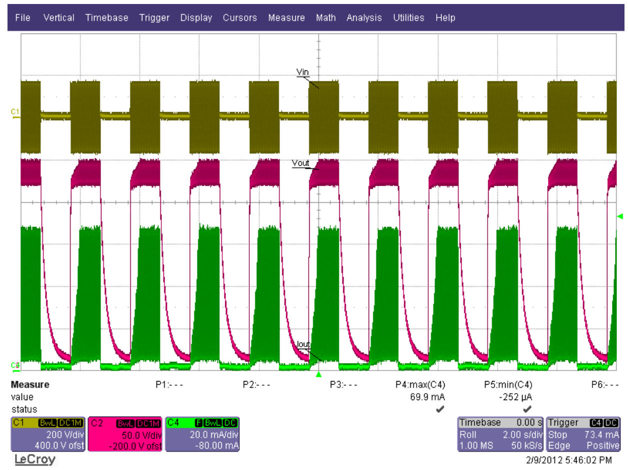

Figure 52 – 115 VAC / 50 Hz,
1s On – 1s Off.
Load: 230 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 20 mA / div.
Time Scale: 2 s / div.

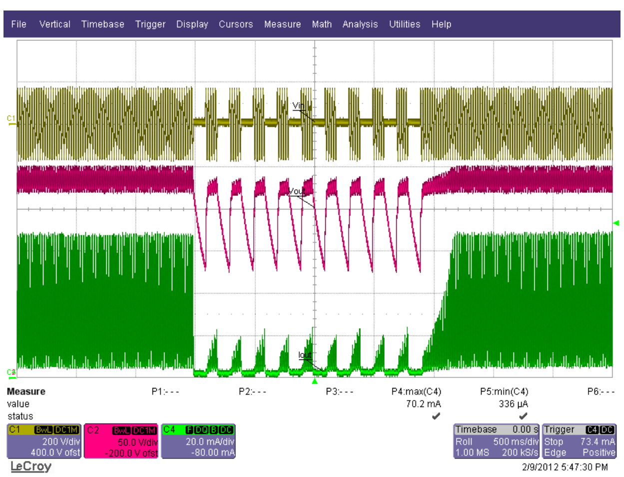

Figure 53 – 115 VAC / 50 Hz,
100 ms On – 100ms Off.
Load: 230 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 20 mA / div.
Time Scale: 0.5 s / div.

Figure 54 – 115 VAC / 50 Hz,
50 ms On – 50m s Off.
Load: 230 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 20 mA / div.
Time Scale: 0.5 s / div.

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12.9 Brown-out

An input voltage slew rate of 0.5 V / s from 90-0-90 VAC / 50 Hz was applied to the driver. No failures or unexpected driver operation observed.

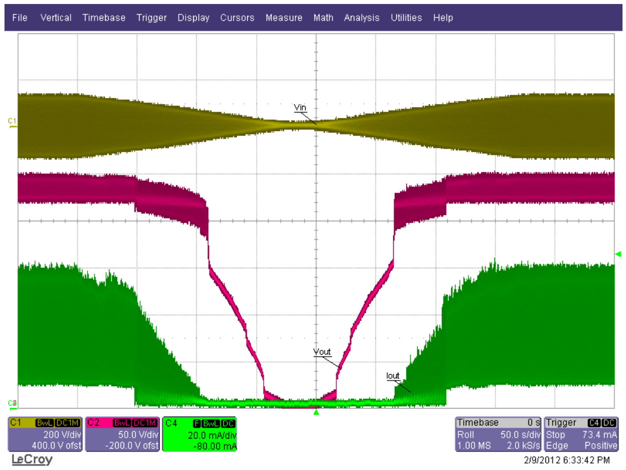

Figure 55 – 90 VAC / 50 Hz, 230 V LED String.
Ch1: V_{IN}, 20 V / div.
Ch2: V_{OUT}, 50 V / div.
Ch4: I_{OUT}, 200 mA / div.,
Time Scale: 50 s / div.

12.10 Line Surge Waveform

This reference design isolates the LED load in any event where the instantaneous input voltage is above the LED voltage therefore protecting it from high current transients.

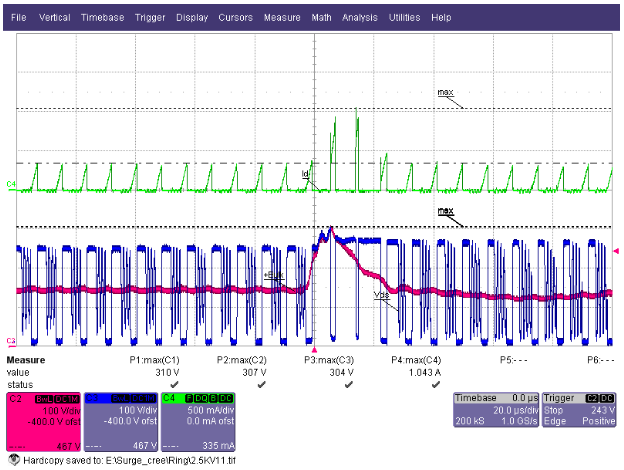

Figure 56 – 115 VAC / 60 Hz, 230 V Load,
V_{DS}=304 V_{PK}
(+) 2.5 kV Differential Ring Surge at 90º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale 20 µs / div.

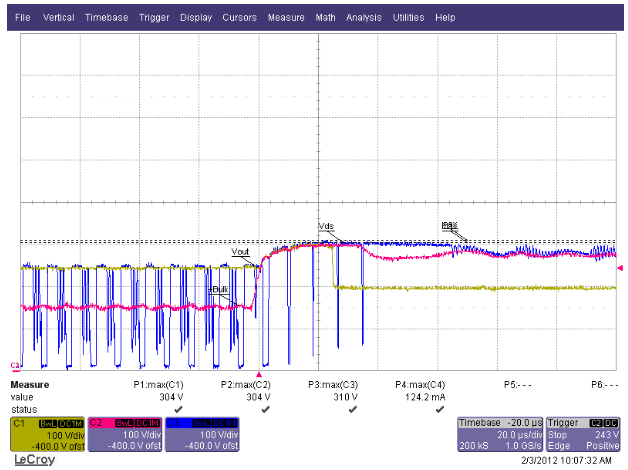

Figure 57 – 115 VAC / 60 Hz, 230 V Load,
V_{DS}=310 V_{PK}
(+) 500 V Differential Surge at 90º.
Ch1: V_{OUT}, 100 V / div.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Time Scale 20 µs / div.

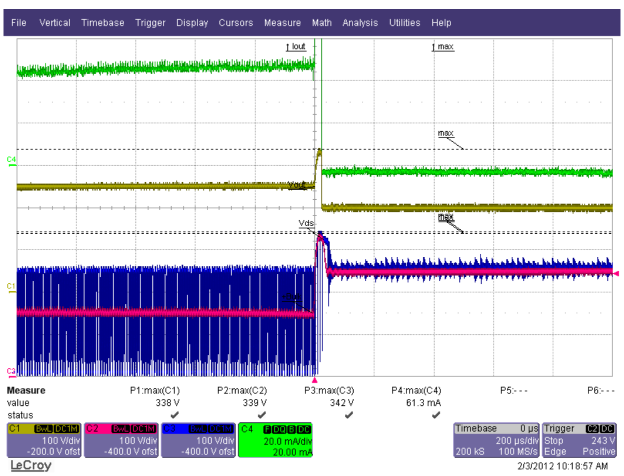

Figure 58 – 115 VAC / 60 Hz, 230 V Load,
V_{DS}=342 V_{PK}
(+) 500 V Differential Surge at 90º.
Ch1: V_{OUT}, 100 V / div.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 20m A / div.
Time Scale: 200 µs / div.

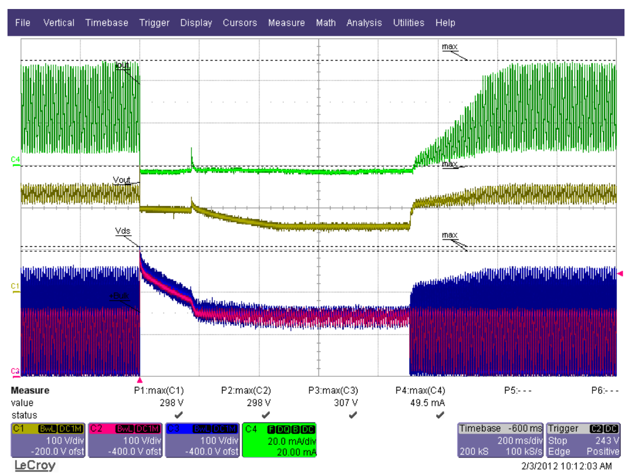

Figure 59 – 115 VAC / 60 Hz, 230 V Load,
V_{DS}=307 V_{PK}
(+) 500 V Differential Surge at 90º.
Ch1: V_{OUT}, 100 V / div.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 20 mA / div.
Time Scale: 200 ms / div.

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13 Line Surge

Input voltage was set at 115 VAC / 60 Hz. Output was loaded with 230 V LED string and operation was verified following each surge event. Two units were verified in the following conditions.

Differential input line 1.2 / 50 μs surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	115	L to N	0	Pass
-500	115	L to N	270	Pass
+500	115	L to N	90	Pass
-500	115	L to N	1800	Pass

Differential input line ring surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	115	L to N	0	Pass
-2500	115	L to N	270	Pass
+2500	115	L to N	90	Pass
-2500	115	L to N	1800	Pass

Unit passes under all test conditions.

14 Conducted EMI

14.1 Equipment

Receiver:

Rohde & Schwartz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Schwartz
Two-Line-V-Network
Model No: ENV216

14.2 EMI Test Set-up

LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

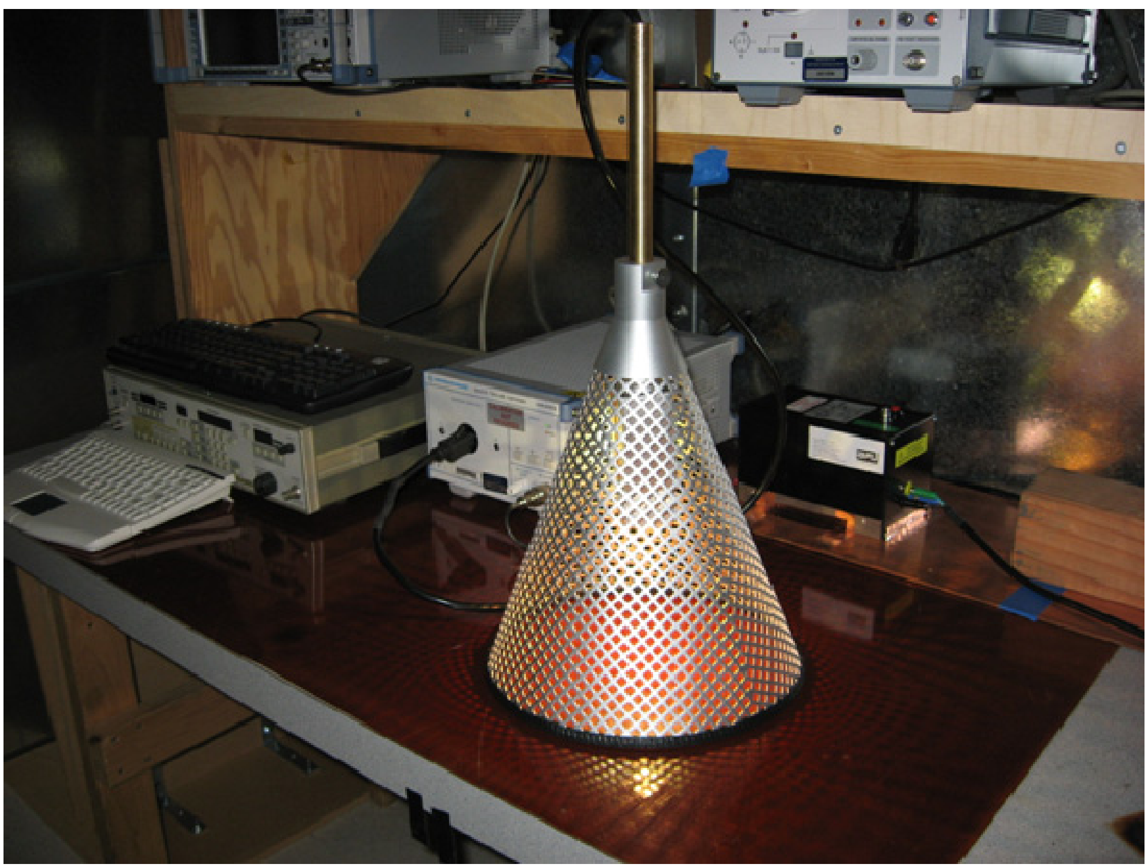

Figure 60 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

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14.3 EMI Test Result

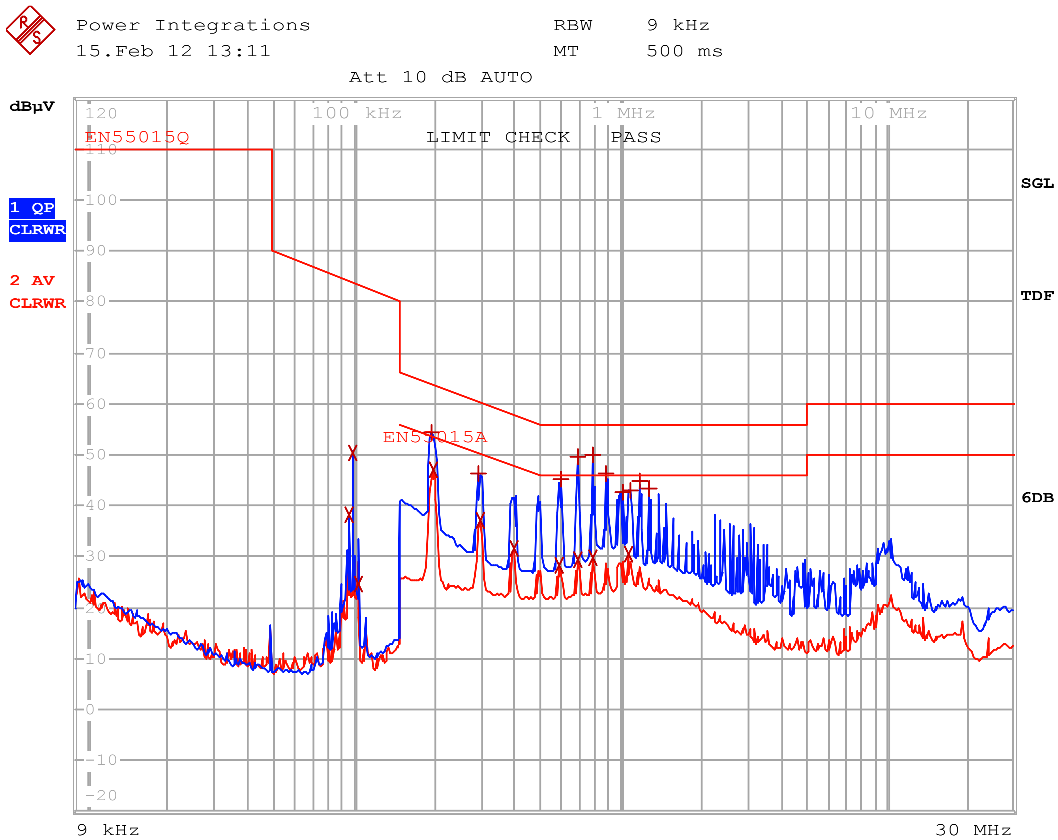

Figure 61 – Conducted EMI, 230 V output / 30 mA Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q

Trace2: EN55015A

Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	95.14984736 kHz	38.10	L1 gnd	
2	Average	99.0133127137 kHz	50.18	L1 gnd	
2	Average	103.033650253 kHz	24.62	L1 gnd	
1	Quasi Peak	194.288447245 kHz	54.45	L1 gnd	-9.39
2	Average	198.193645035 kHz	47.19	N gnd	-6.49
1	Quasi Peak	292.161713188 kHz	46.30	L1 gnd	-14.15
2	Average	295.08333032 kHz	36.98	N gnd	-13.39
2	Average	393.789848222 kHz	31.74	N gnd	-16.24
2	Average	586.299423673 kHz	28.24	N gnd	-17.75
1	Quasi Peak	592.16241791 kHz	45.32	L1 gnd	-10.67
1	Quasi Peak	687.48218373 kHz	49.52	L1 gnd	-6.47
2	Average	687.48218373 kHz	29.24	N gnd	-16.75
2	Average	782.418853721 kHz	29.88	N gnd	-16.11
1	Quasi Peak	790.243042258 kHz	49.87	L1 gnd	-6.12
1	Quasi Peak	881.64914842 kHz	46.19	N gnd	-9.80
1	Quasi Peak	1.01343296123 MHz	42.74	L1 gnd	-13.25
2	Average	1.07577950963 MHz	30.64	N gnd	-15.35
1	Quasi Peak	1.08653730473 MHz	43.15	L1 gnd	-12.84
1	Quasi Peak	1.17656420634 MHz	44.77	N gnd	-11.22
1	Quasi Peak	1.27405044044 MHz	43.26	N gnd	-12.73

Figure 62 – Conducted EMI, 230 V / 30 mA Steady-State Load Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits. Line and Neutral Scan Design Margin Measurement.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
14-Mar-12	JDC	1.0	Initial Release	Apps & Mktg

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