Design Example Report

Title	***4.5 W Power Factor Corrected LED Driver (Non-Isolated Buck Boost) Using LinkSwitch^{TM}-PL LNK458KG***
Specification	190 VAC – 265 VAC Input; 48 V, 93 mA Output
Application	LED Driver for B10 Lamp Replacement
Author	Applications Engineering Department
Document Number	DER-304
Date	January 11, 2012
Revision	1.0

Summary and Features

- Single-stage power factor corrected and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Highly energy efficient, >85.5% at 230 VAC input for 48 V
- Superior performance and end user experience
  - Fast start-up time (<300 ms) – no perceptible delay
- Integrated protection and reliability features
  - Single shot no-load protection / output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
  - No damage during brown-out conditions
- PF >0.9 at 230 VAC
- %A THD <20% at 230 VAC
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI

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Table of Contents

Important Note:
Although this board is designed to satisfy safety requirements for non-isolated LED drivers, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK458KG from the LinkSwitch-PL family of devices.

The driver provides a single constant current output with an output power of 4.5 W.

The key design goals were high efficiency and small size, enabling the driver to fit into candelabra and B10 sized lamps.

The board was optimized to operate over the high AC input voltage range (190 VAC to 265 VAC, 47 Hz to 63 Hz). LinkSwitch-PL based designs provide a high power factor (>0.9) meeting current international requirements.

The form factor of the board was chosen to meet the requirements for standard B10 LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The design was not optimized for operation with phase controlled (TRIAC) dimmers but this is possible with some modification. For an example of a dimmable version please visit http://www.powerint.com/en/applications/led-lighting.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet and performance data.

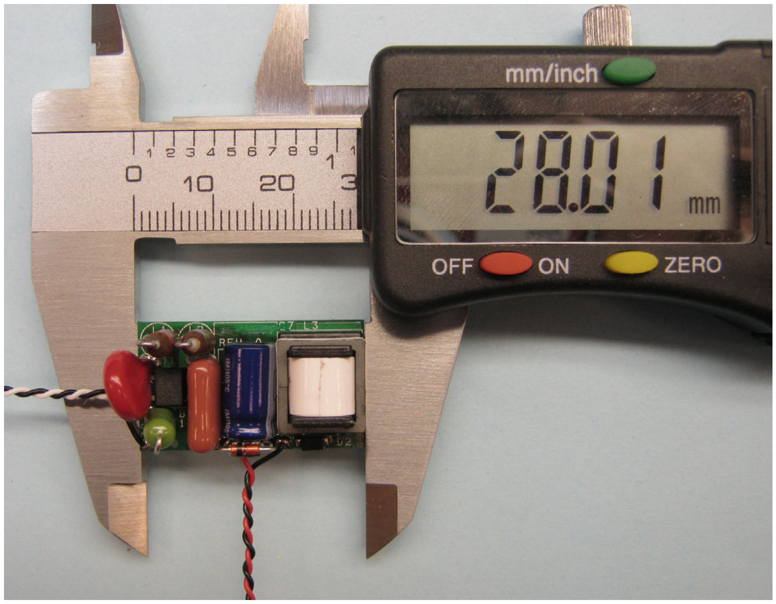

Figure 1 – Size of a Populated Circuit Board; Length = 28 mm.

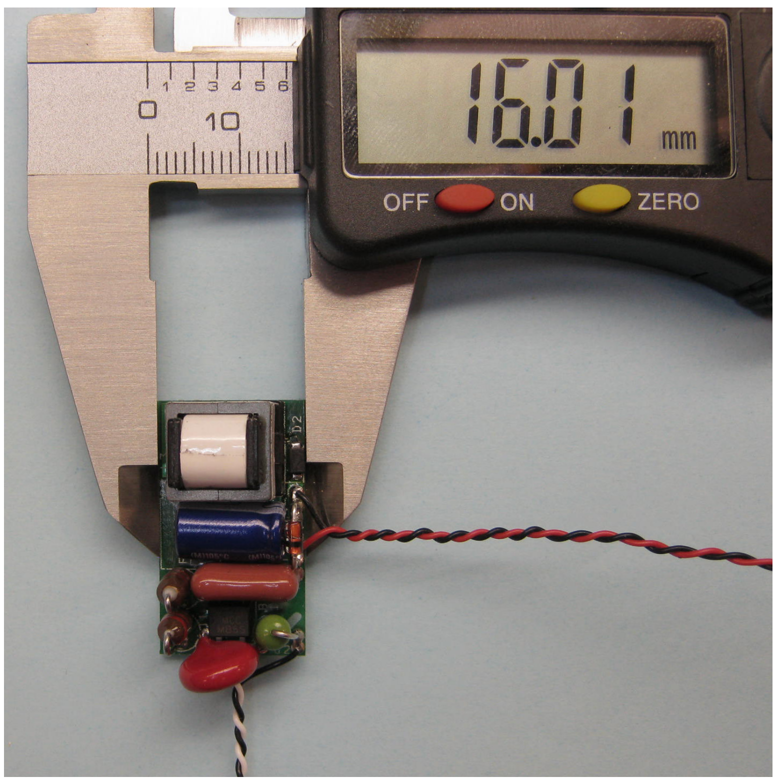

Figure 2 – Size of a Populated Circuit Board; Width = 16 mm.

Note: The populated circuit board shown above used DER-297 PCB

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2 Power Supply Specifications

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
%ATHD				20		At any line input voltage
Output						
Output Voltage	V_{OUT}		48		V	
Output Current	I_{OUT}	87	93	97	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		4.5		W	
Efficiency						
Nominal	η	85.5			%	Measured at P_{OUT} 25°C at 230 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			1		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω short-circuit Series Impedance
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class D (C)				Class C specifies Class D Limits when P_{IN} <25 W

3 Schematic

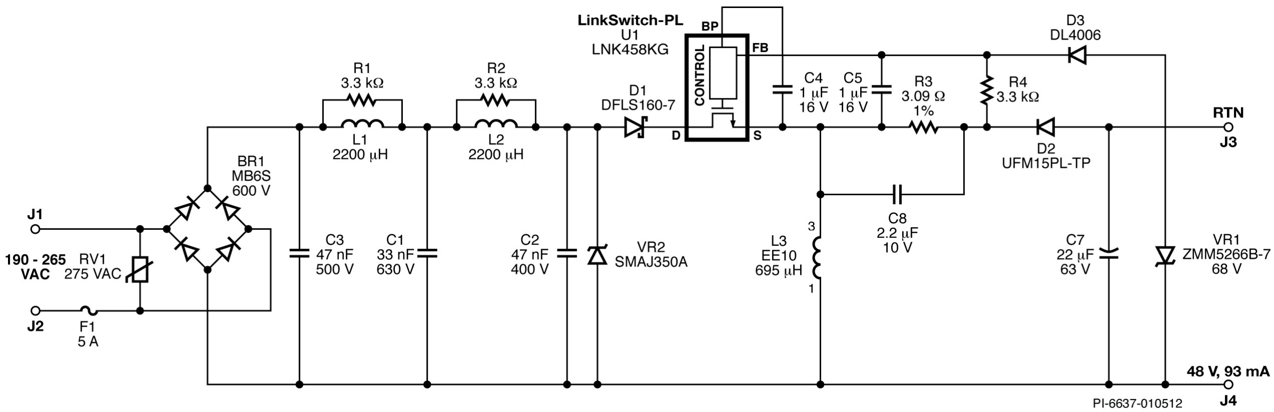

Figure 3 – Schematic

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4 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary-side controller intended for use in LED driver applications. The LinkSwitch-PL provides high power factor in a single-stage conversion topology while regulating the output current across a range of input (190 VAC -265 VAC) and output voltage variations typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus a high-voltage power MOSFET is incorporated into the IC.

4.1 Input EMI Filtering

Fuse F1 provides protection against component failure. A fast 5 A rating (this being relatively high) was needed to prevent false opening during line surges. The maximum input voltage is clamped by RV1 and by VR2 (TVS) during differential line surges. Zener diode VR2 can be removed for a differential line surge requirement of ≤500 V.

The AC input is full wave rectified by BR1 to achieve good power factor and THD.

Capacitor C1, C2, C3 and differential choke L1 and L2 perform EMI filtering while the limited total capacitance maintains high power factor. This 2-π filter network plus the frequency jittering feature of LinkSwitch-PL ensures compliance with Class B emission limits. Resistor R1 and R2 are used to damp the resonance of the EMI filter, preventing peaks in the conducted EMI measurements when measured in a system (driver plus enclosure).

- Inductor L1 and L2 are positioned after the bridge to avoid an imbalance in the EMI scan between line and neutral. This also allows the use of small high-voltage ceramic capacitors in the input filter.

4.2 Buck Boost Using LinkSwitch-PL

The buck boost power train is composed of U1 (power switch + control), D2 (free-wheeling diode), C7 (output capacitor), and L3 (inductor). Diode D1 was used to prevent negative voltage appearing across the drain-source of U1 especially near the zero-crossing of the input voltage. Capacitor C8 reduces the RMS current through R3, improving efficiency. The bypass capacitor C4 provides the internal supply for the device when the power MOSFET is on.

- Diode D1 is a low drop diode (Schottky) type to maximize efficiency. An ultrafast type may be substituted if lower efficiency is acceptable.
- Inductor L3 winding construction and wire gauge were optimized to minimize inter-winding capacitance and to reduce AC losses.
- As this was a non-dimming design, no external bias supply is required to supply the BP pin of U1.

4.3 Output Feedback

The output current feedback is sensed on the voltage drop across R3 and then filtered by a low pass filter (R4 and C5) to keep the LinkSwitch-PL operating point such that the average FEEDBACK (FB) pin voltage is 290 mV in steady-state operation.

4.4 Disconnected Load Protection

In order to avoid catastrophic failure of the output capacitor (C7) if the load is not connected, the output is protected by an auto-restart overvoltage protection circuit. Zener VR1 is connected to V_{OUT+} and in series with blocking diode D3. If a no-load condition is present on the output of the supply, the output overvoltage Zener diode VR1 will conduct once its threshold is reached. A voltage V_{OV} in excess of $V_{FB(AR)}$ = 2 V will appear across the FB pin and the IC will enter auto-restart.

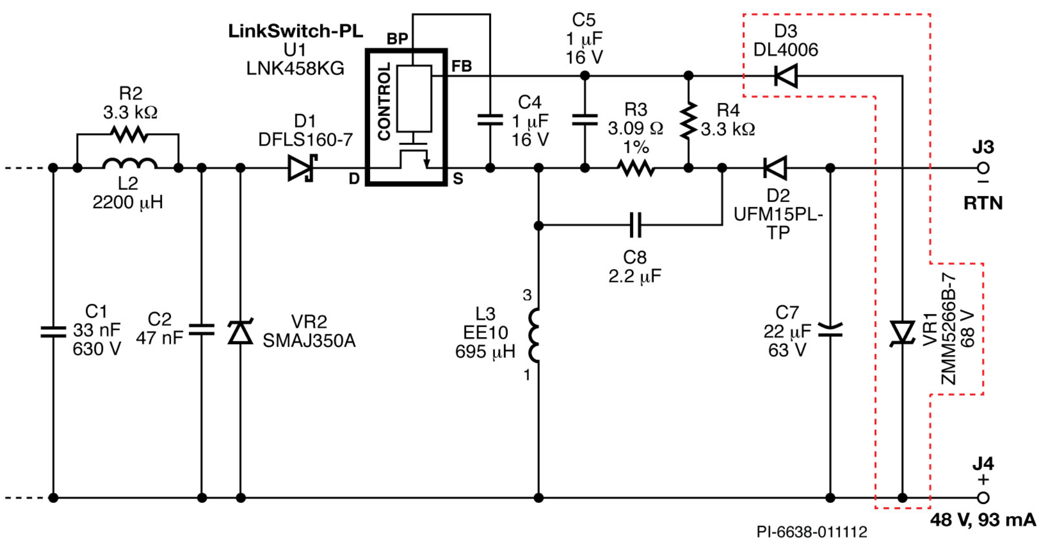

Figure 4 – Auto-Restart Overvoltage Protection with Buck-Boost Configuration.

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5 PCB Layout

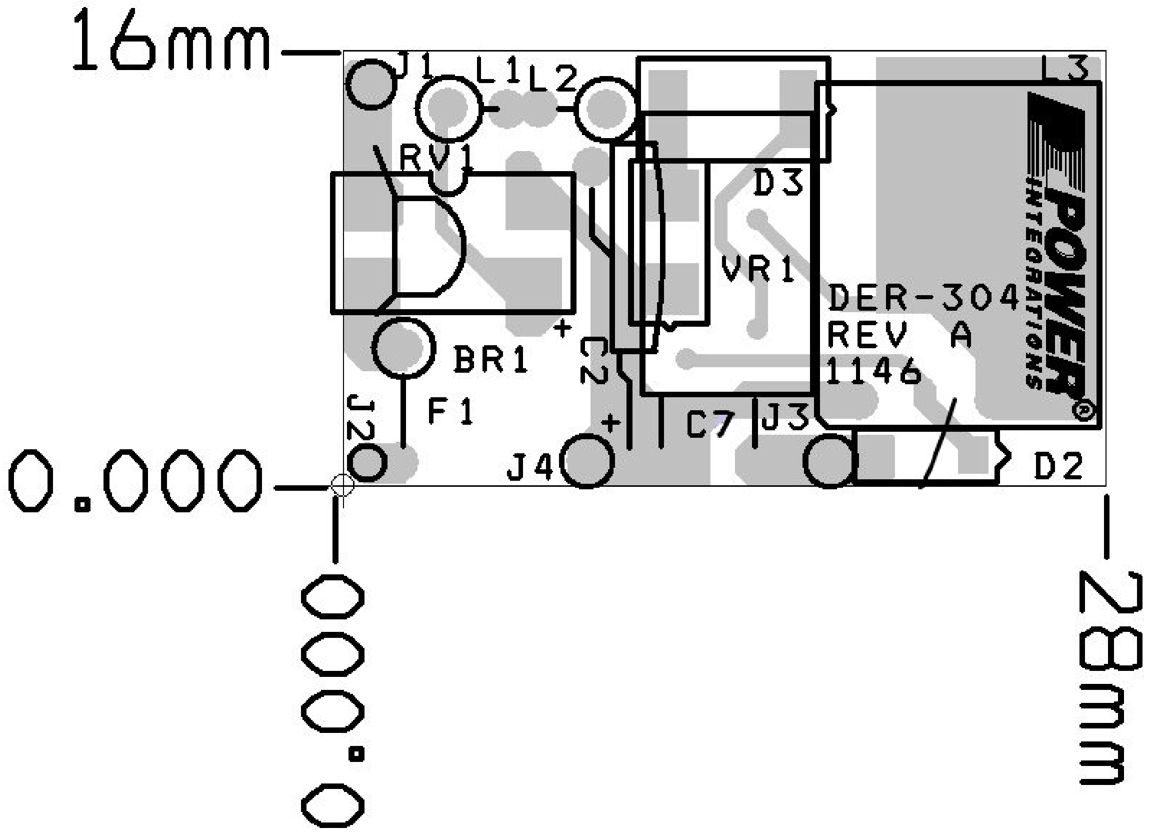

Figure 5 – Printed Circuit Layout, Top.

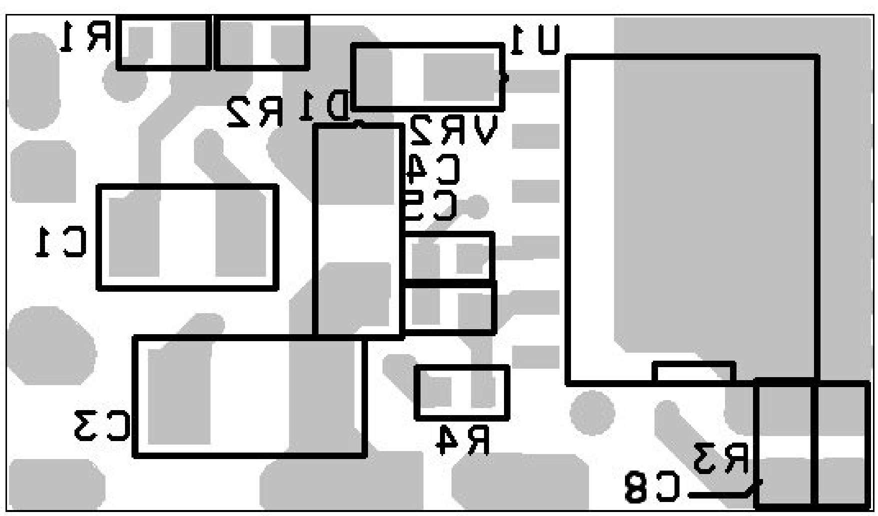

Figure 6 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	33 nF, 630 V, Ceramic, X7R, 1210	GRM32DR72J333KW01L	Murata
3	1	C2	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
4	1	C3	47 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y473KXEAT	Vishay
5	2	C4 C5	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
6	1	C7	22 μF, 63 V, Electrolytic, Low ESR, 1000 mΩ, (6.3 x 11.5)	ELXZ630ELL220MFB5D	Nippon Chemi-Con
7	1	C8	2.2 μF, 10 V, Ceramic, X7R, 0805	GRM21BR71A225MA01L	Murata
8	1	D1	60 V, 1 A, DIODE SCHOTTKY, PWRDI 123	DFLS160-7	Diodes, Inc.
9	1	D2	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
10	1	D3	800 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4006-13-F	Diodes, Inc.
11	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	Littlefuse
12	4	J1 J2 J3 J4	PCB Terminal Hole, #30 AWG	N/A	N/A
13	2	L1 L2	2200 μH, 80 mA, 34.7 Ω, Axial Ferrite Inductor	B78108S1225J	Epcos
14	1	L3	Custom EE10 Inductor, 695 μH	TF-1003	Taiwan Shulin
15	3	R1 R2 R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
16	1	R3	3.09 Ω, 1%, 1/8 W, Thick Film, 0805	RC0805FR-073R09L	Yageo
17	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
18	1	U1	LinkSwitch-PL, eSOP-12P	LNK458KG	Power Integrations
19	1	VR1	68 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5266B-7	Diodes, Inc.
20	1	VR2	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	Littlefuse

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7 Inductor Specification

7.1 Electrical Diagram

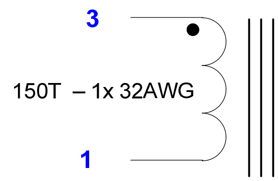

Figure 7 – 48 V Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	695 µH ±5%

7.3 Materials

Item	Description
[1]	Core: EE10/PC40
[2]	Bobbin: EE10, Horizontal, 8 pins, (4/4), Taiwan Shulin Enterprise Co., Ltd. or Kunshan Fengshunhe Electronics Co., Ltd Equivalent
[3]	Magnet Wire: 1 x #32 AWG
[4]	Loctite Super Glue Control Gel

7.4 Inductor Build Diagram

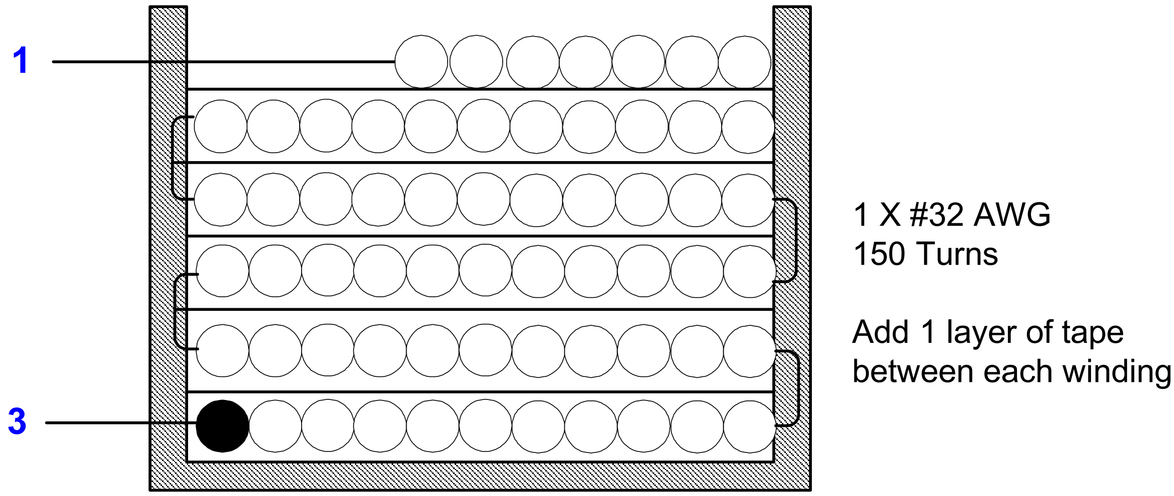

Figure 8 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left (Figure 10). Winding direction is counter-clockwise.
WD1	Start at pin 3. Wind enough turns of item [3] as shown in Figure 10 with 1 layer of tape between the windings. Continue winding and terminate at pin 1. Note: eliminating the tape between layers will increase capacitance and reduce driver efficiency
Finish	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 2, 4, 5, 6, 7 and 8. Apply adhesive item [4] to core and bobbin to prevent core movement.

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8 Inductor Design Spreadsheet

ACDC_LinkSwitch-PL-Buck-Boost_021811; Rev.0.1; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL-Buck-Boost_021811; LinkSwitch-PL Buck-Boost Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	190		190	V	Minimum AC input voltage
VACNOM	230		230	V	Nominal AC input voltage
VACMAX	265		265	V	Maximum AC input voltage
FL	50		50	Hz	Minimum line frequency
VO_MIN	42.00		42.0	V	Minimum output voltage tolerance
VO_NOM	48.00		48.0	V	Nominal Output Voltage
VO_MAX	54.00		54.0	V	Maximum output voltage tolerance
IO	0.090		0.090	A	Average output current specification
n	0.85		0.850	%/100	Total power supply efficiency
Z			0.5		Loss allocation factor
Enclosure	Retrofit Lamp		Retrofit Lamp		Enclosure selections determines thermal conditions and maximum power
PO			4.32	W	Total output power
VD	0.50		0.5	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES					
Device	LNK458		LNK458		Chosen LinkSwitch-PL Device
TON			1.43	us	Expected on-time of MOSFET at low line and PO
FSW			60.1	kHz	Expected switching frequency at low line and PO
Duty Cycle			8.6	%	Expected operating duty cycle at low line and PO
VDRAIN			449	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS			0.080	A	Nominal RMS current through the switch
IPK			0.784	A	Worst Case Peak current
ILIM_MIN			1.012	A	Minimum device current limit
KDP	1.60		1.58		Ratio between off-time of switch and reset time of core at VACNOM
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			3.222	Ohms	Output current sense resistor
Standard RSENSE			3.24	Ohms	Closest 1% value for RSENSE
PSENSE			26.1	mW	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE10		EE10		Core Type
Core Part Number			Custom		Core Part Number (if Available)
Bobbin Part Number			Custom		Bobbin Part Number (if available)
AE	12.10		12.10	mm^2	Core Effective Cross Sectional Area
LE	26.10		26.10	mm	Core Effective Path Length
AL	850		850	nH/T^2	Ungapped Core Effective Inductance
BW	6.30		6.3	mm	Bobbin Physical Winding Width
L	6		6		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			694.8	uH	Primary Inductance

LP Tolerance	5.00		5	%	Tolerance of Primary Inductance
N	150		150	Turns	Number of Turns
ALG			31	nH/T^2	Gapped Core Effective Inductance
BM		*Info*	3001	Gauss	Reduce BM < 3000 G. Decrease BP (increase NP) or increase core size.
BAC			1500	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP		*Warning*	5177	Gauss	!!! Reduce peak flux density (BP < 3600 G) by increasing NP, selecting a bigger core or decreasing KDP
LG			0.492	mm	Gap Length (Lg > 0.1 mm)
BWE			37.8	mm	Effective Bobbin Width
L_IRMS			0.254	A	RMS Curren through the inductor
OD			0.25	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.20	mm	Bare conductor diameter
AWG			32	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			64	Cmils	Bare conductor effective area in circular mils
CMA			252	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)			7.93	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters					
IRIPPLE					Maximum Capacitor Ripple Current
IO			0.090	A	Expected Output Current
PIVS			472.2	V	Peak Inverse Voltage at VO_MAX on output diode

Note: Peak flux density is limited by slowly increasing the duty cycle of LinkSwitch-PL family during start-up. No core saturation occurred when tested for start-up short, running short, with the core temperature raised to 100 ºC.

9 Performance Data

All measurements performed at 25 ºC room temperature, 60 Hz input frequency unless otherwise specified.

9.1 Active Mode Efficiency

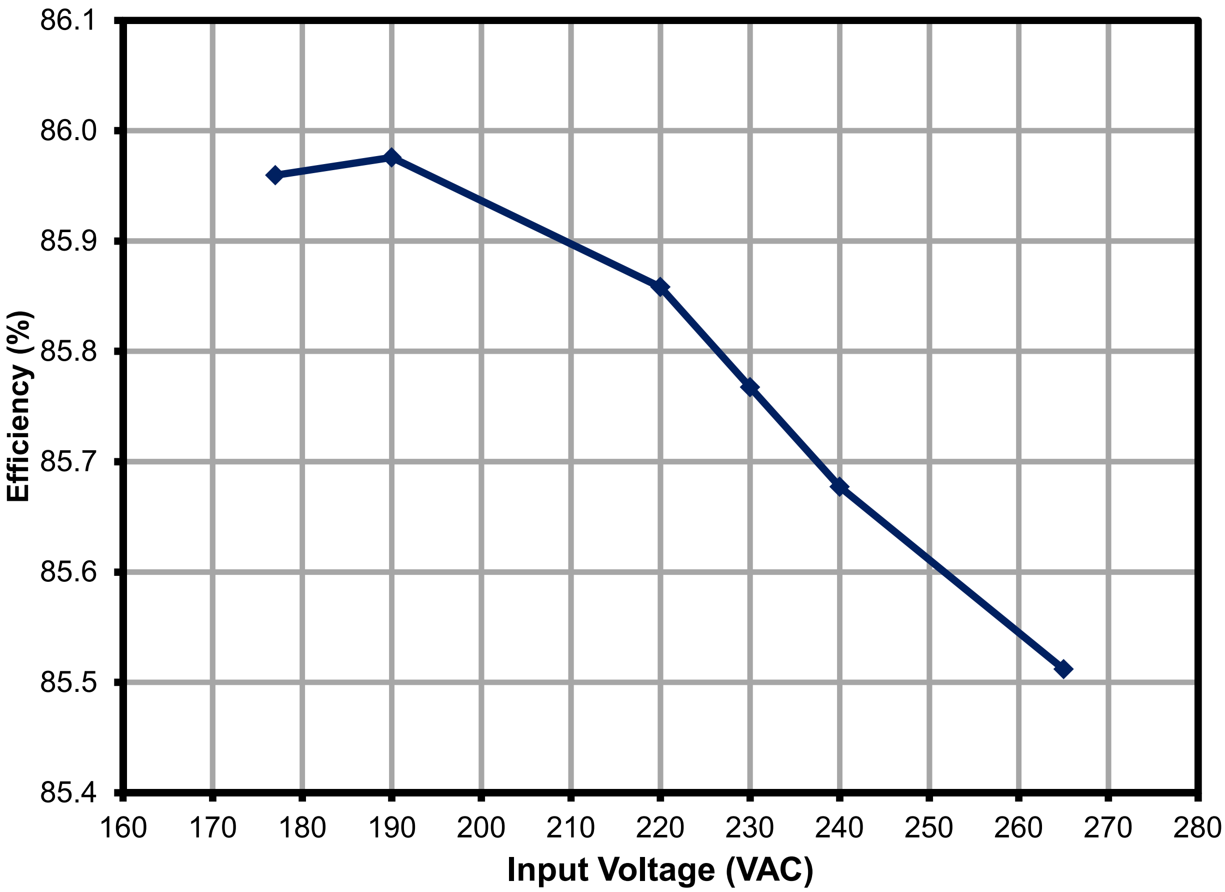

Figure 9 – Efficiency with Respect to AC Input Voltage.

9.2 Line Regulation

The LinkSwitch-PL device regulates the output by controlling the power MOSFET on-time and switching frequency to maintain the average FB pin at its 0.29 V threshold. Slight changes in output current may be observed when input or output conditions are changed or after AC cycling due to the device selecting a slightly different operating state (selection of on-time and frequency).

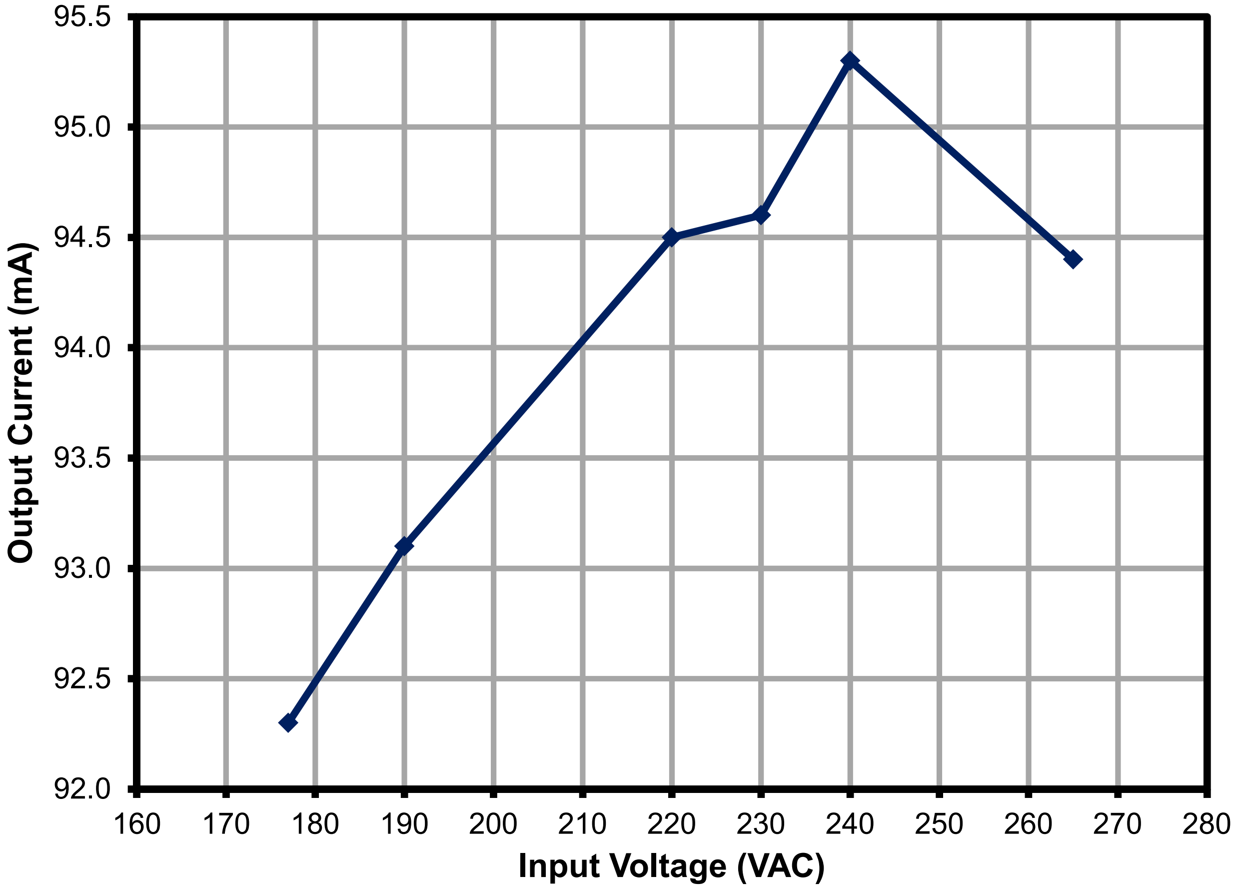

Figure 10 – Line Regulation, Room Temperature.

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9.3 Power Factor

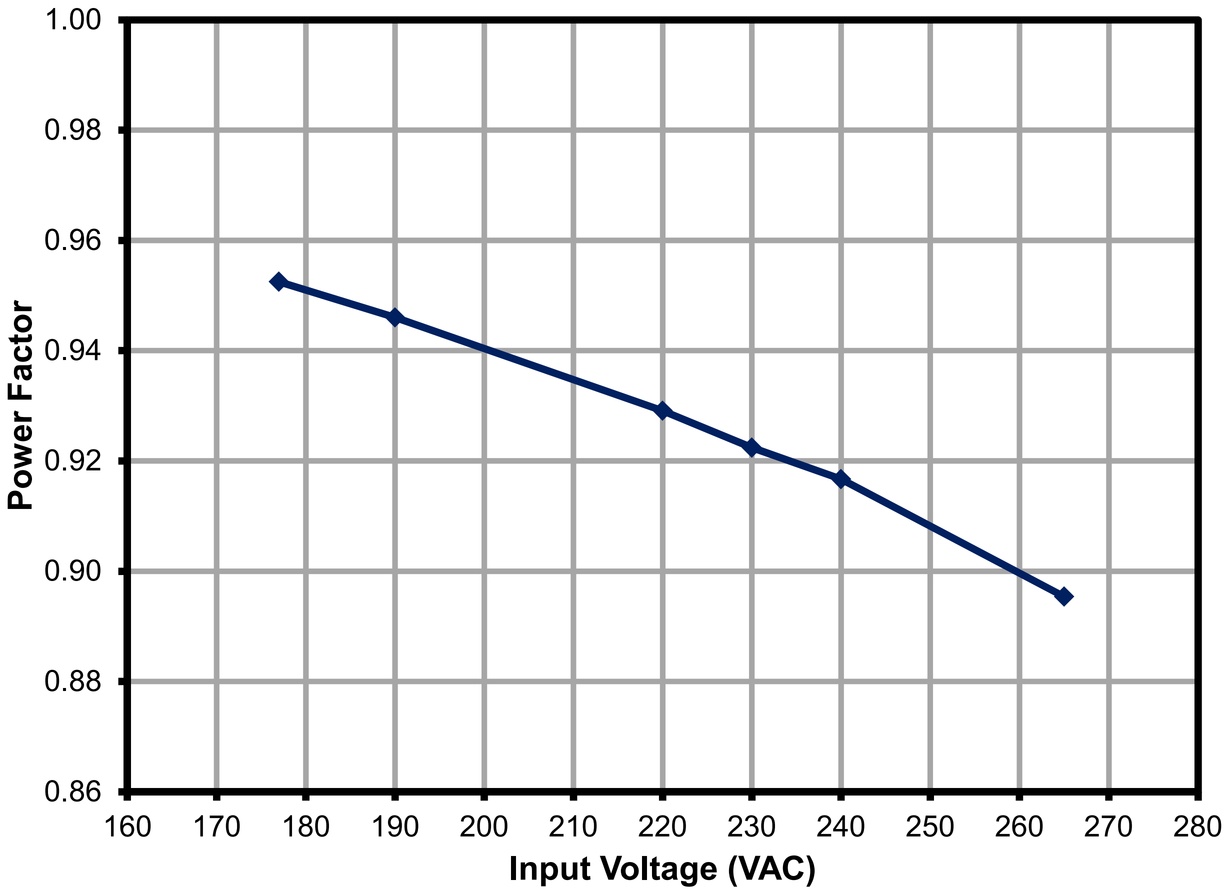

Figure 11 – High Power Factor Within the Operating Range.

9.4 %THD

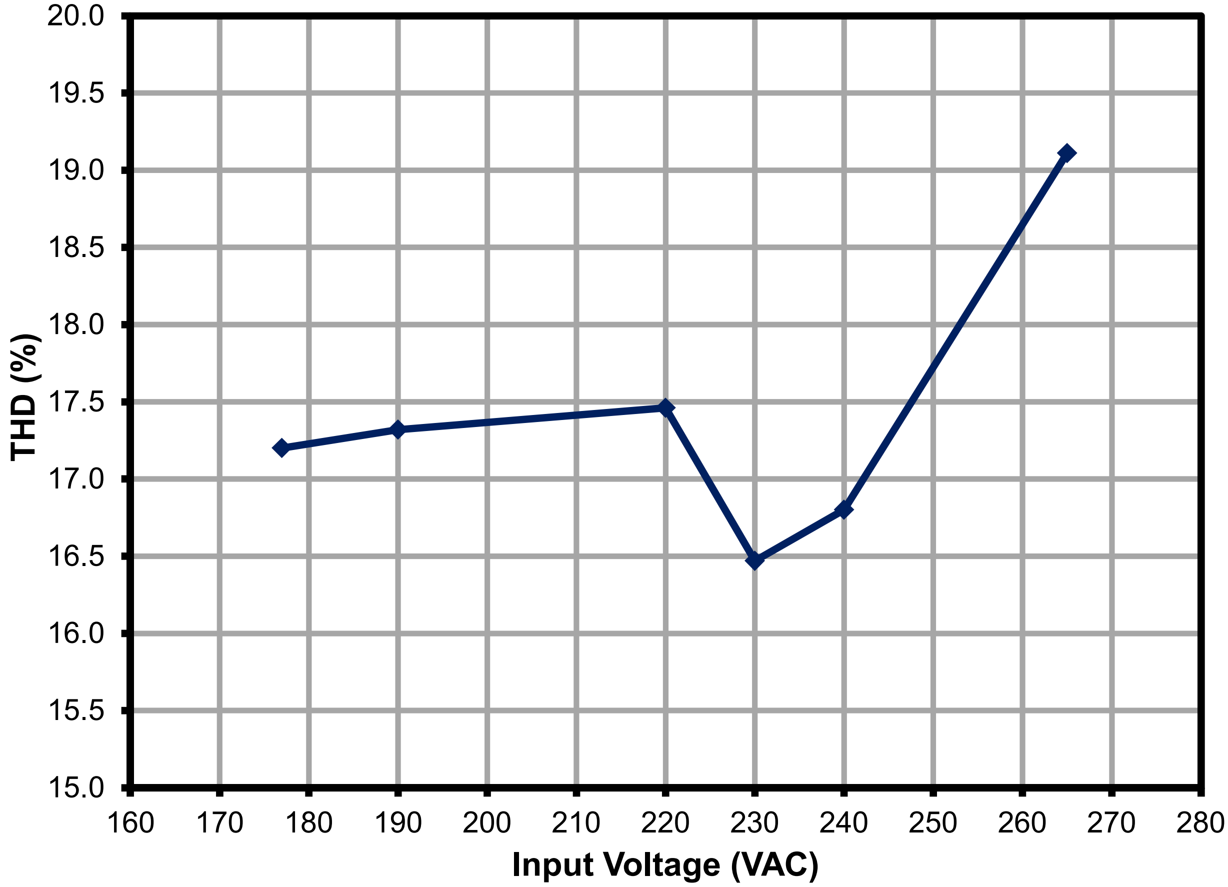

Figure 12 – Very Low %ATHD Within the Operating Range.

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9.5 Harmonics

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment[1]. Therefore the limits shown in the charts below are Class D limits which must not be exceeded to meet Class C compliance.

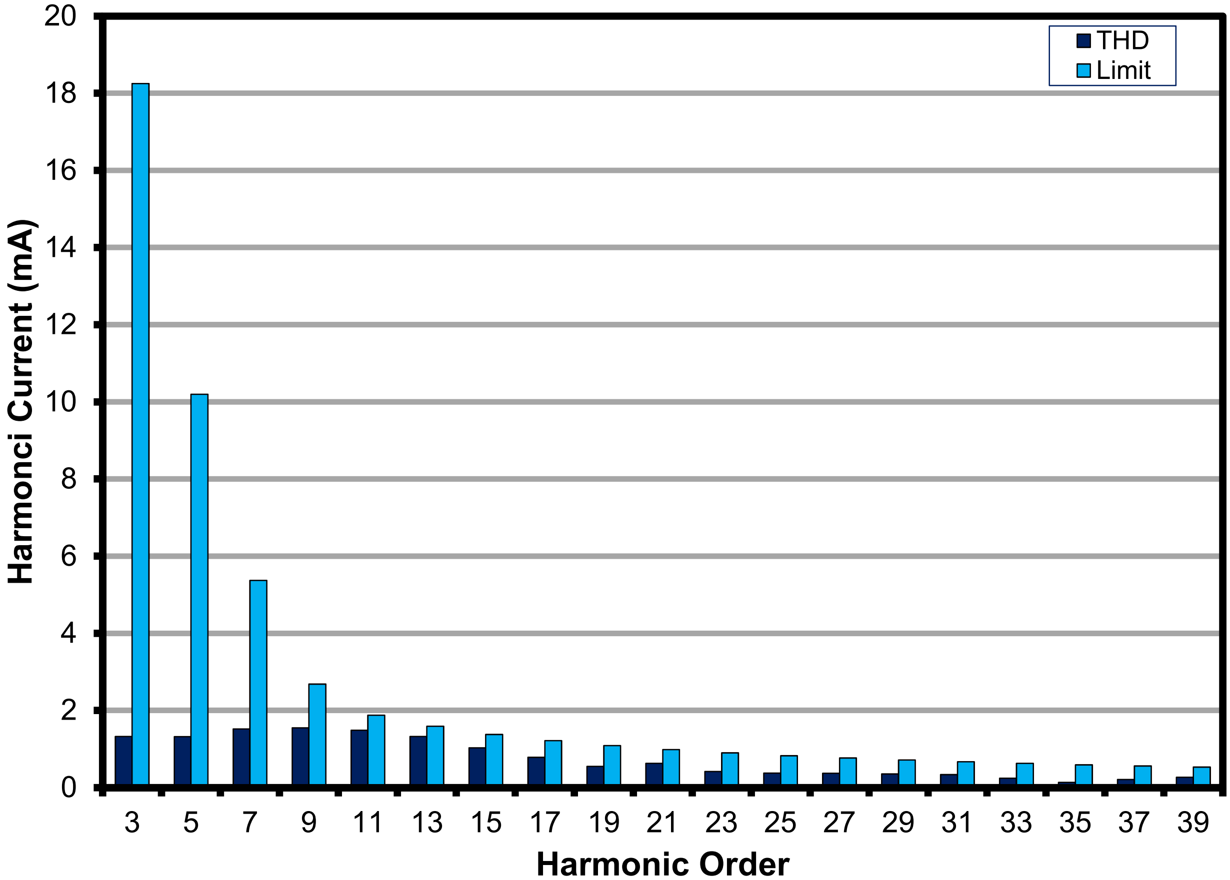

Figure 13 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W.

[1] IEC6000-3-2 Section 7.3, table 2, column 2.

9.6 Harmonic Measurements

V	Freq	I (mA)	P	PF
230	50.00	25.32	5.3680	0.9224
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	24.61			
2	0.05	0.19%		
3	1.33	5.39%	18.2512	Pass
5	1.32	5.36%	10.1992	Pass
7	1.52	6.17%	5.3680	Pass
9	1.55	6.30%	2.6840	Pass
11	1.49	6.05%	1.8788	Pass
13	1.32	5.38%	1.5898	Pass
15	1.03	4.19%	1.3778	Pass
17	0.78	3.18%	1.2157	Pass
19	0.55	2.22%	1.0877	Pass
21	0.63	2.56%	0.9841	Pass
23	0.42	1.69%	0.8986	Pass
25	0.38	1.53%	0.8267	Pass
27	0.37	1.50%	0.7654	Pass
29	0.35	1.44%	0.7126	Pass
31	0.34	1.36%	0.6667	Pass
33	0.24	0.98%	0.6263	Pass
35	0.14	0.55%	0.5905	Pass
37	0.21	0.84%	0.5586	Pass
39	0.27	1.08%	0.5299	Pass

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9.7 Thermal Scans

The scan is conducted at ambient temperature of 25 ºC, 190 VAC / 50 Hz input.

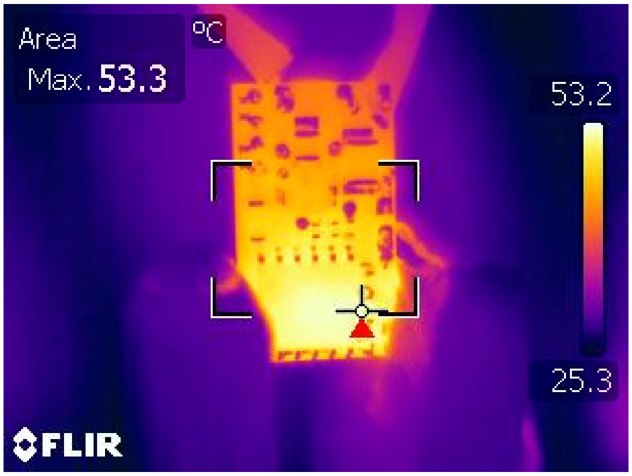

Figure 14 – Bottom Side.
Hottest Component: U1, 53.3 °C.

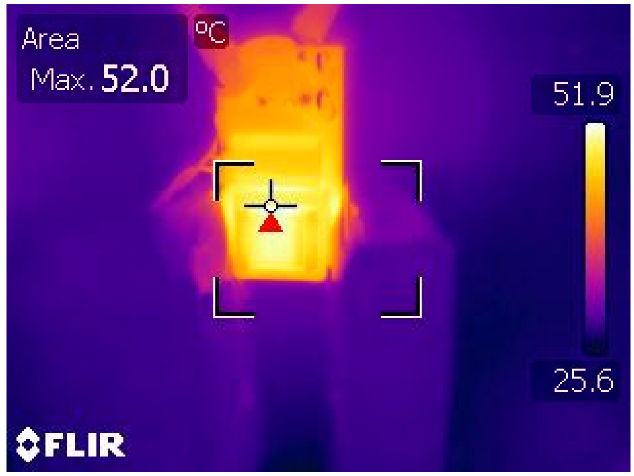

Figure 15 – Top Side.
Hottest Component: T1, 52.0 °C.

10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

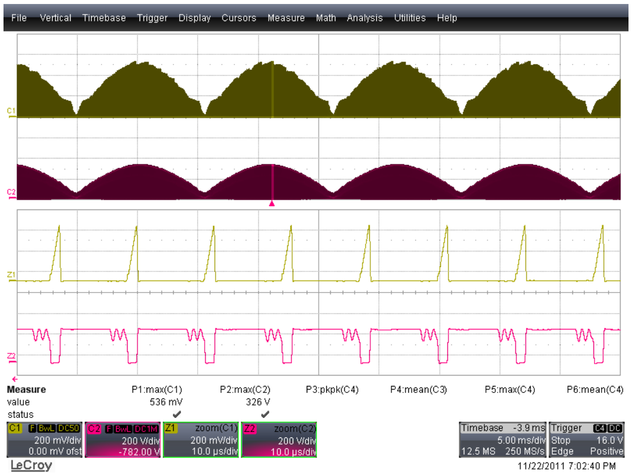

Figure 16 – 190 VAC / 47 Hz, 48 V LED String.
Ch1: I_{DRAIN}, 0.2 A / div.
Ch2: V_{DRAIN}, 200 V / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

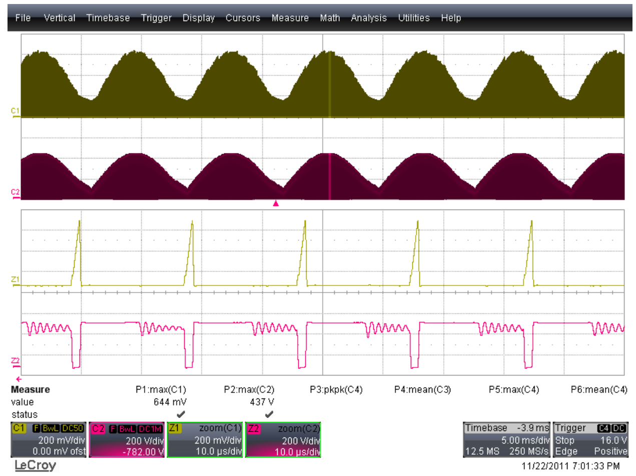

Figure 17 – 265 VAC / 63 Hz, 48 V LED String.
Ch1: I_{DRAIN}, 0.2 A / div.
Ch2: V_{DRAIN}, 200 V / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

10.2 Drain Voltage and Current Start-up Profile

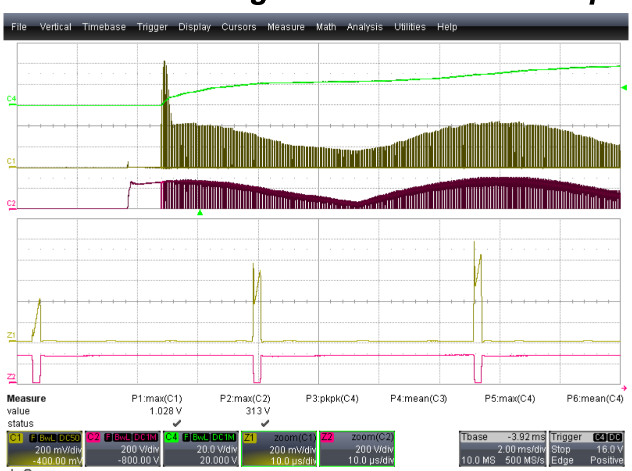

Figure 18 – 190 VAC / 47 Hz, 48 V LED String.
Ch1: I_{DRAIN}, 0.2 A / div.
Ch2: V_{DRAIN}, 200 V / div.
Time Scale: 2 ms / div.
Zoom Time Scale: 10 μs / div.

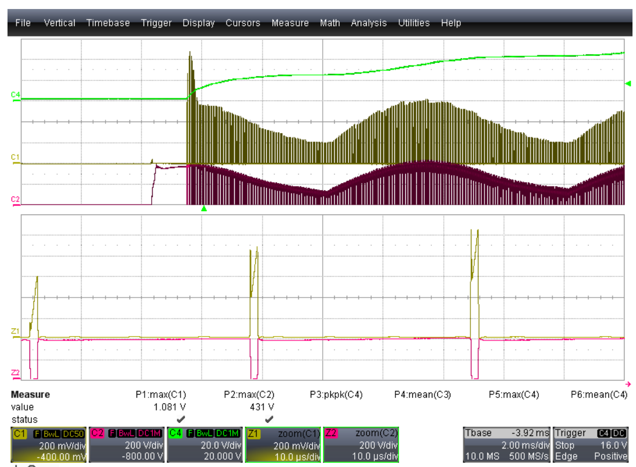

Figure 19 – 265 VAC / 63 Hz, 48 V LED String.
Ch1: I_{DRAIN}, 0.2 A / div.
Ch2: V_{DRAIN}, 200 V / div.
Time Scale: 2 ms / div.
Zoom Time Scale: 10 μs / div.

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10.3 Output Voltage Start-up Profile

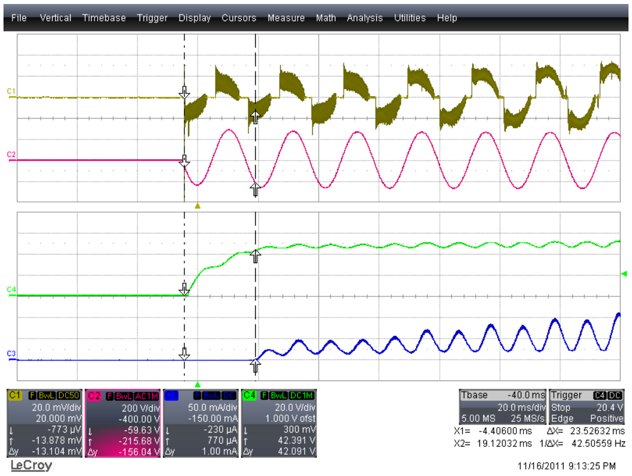

Figure 20 – 190 VAC / 47 Hz, 48 V LED String.
Ch1: I_{IN}, 20 mA / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 20 ms / div.

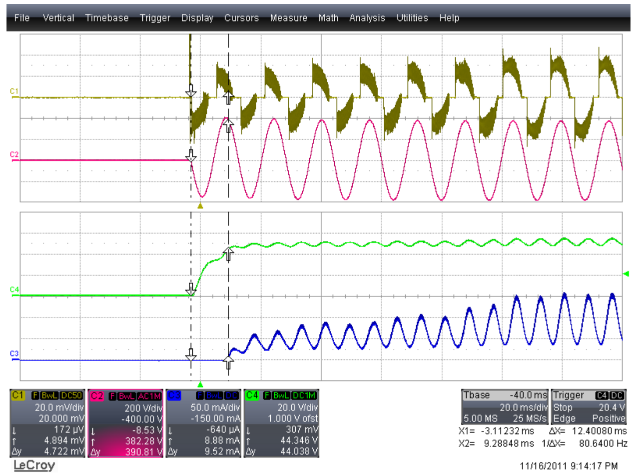

Figure 21 – 265 VAC / 63 Hz, 48 V LED String.
Ch1: I_{IN}, 20 mA / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 20 ms / div.

10.4 Input and Output Voltage and Current Profiles

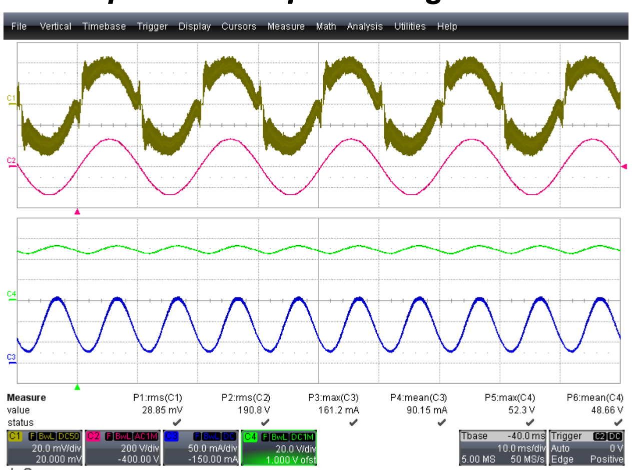

Figure 22 – 190 VAC / 50 Hz, 48 V LED String.
Ch1: I_{IN}, 20 mA / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 10 ms / div.

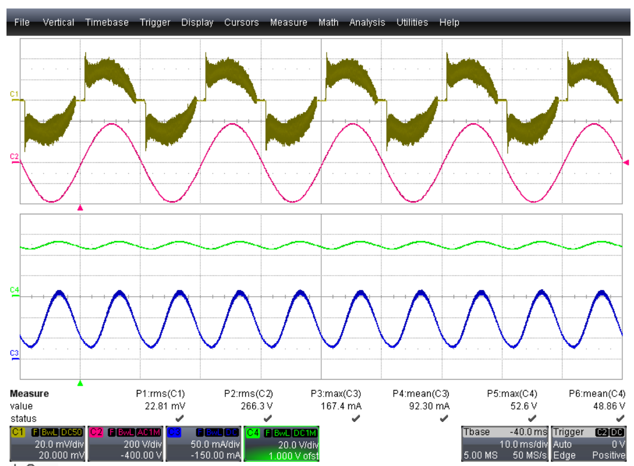

Figure 23 – 265 VAC / 50 Hz, 48 V LED String.
Ch1: I_{IN}, 20 mA / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 10 ms / div.

10.5 Drain Voltage and Current Profile with Output Shorted

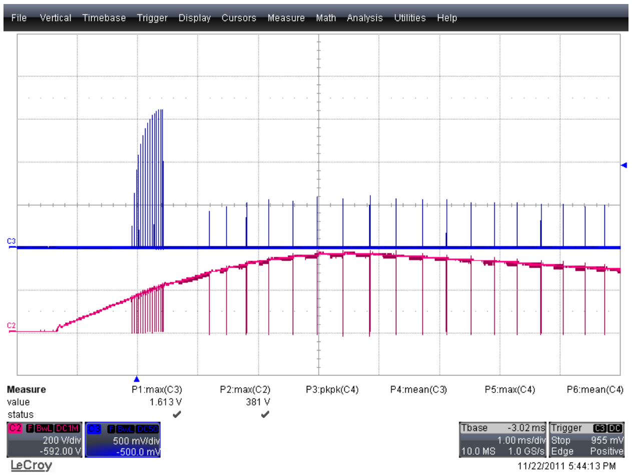

Figure 24 – 265 VAC / 50 Hz, 48 V LED String.
Ch2: V_{DRAIN}, 200 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Time Scale: 1 ms / div.

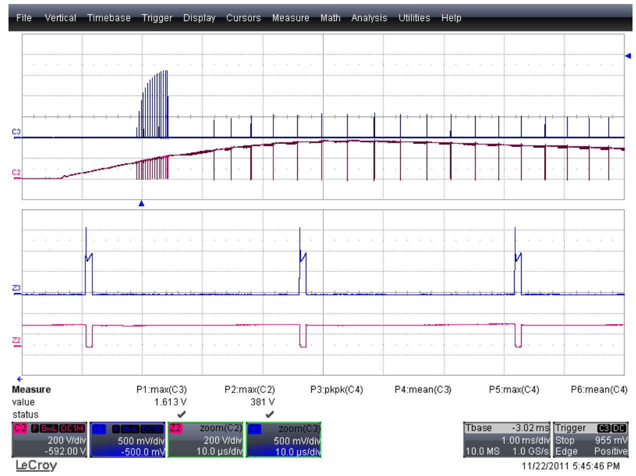

Figure 25 – 265 VAC / 50 Hz, 48 V LED String.
Ch2: V_{DRAIN}, 200 V / div.
Ch3: I_{DRAIN}, 0.5 A / div.
Time Scale: 1 ms / div.
Zoom Time Scale: 10 μs / div.

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10.6 Line Transient Response

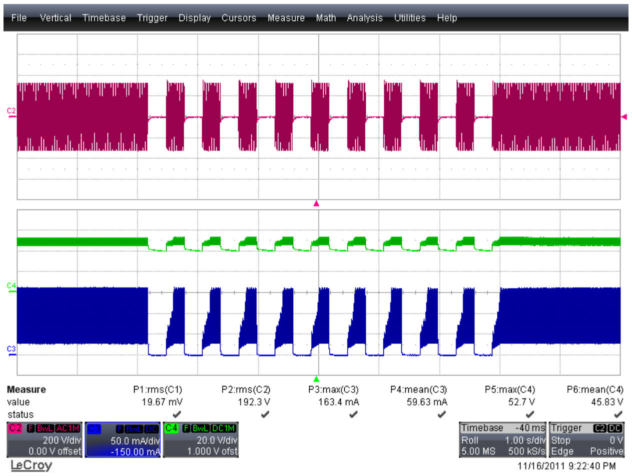

Figure 26 – 230 VAC / 50 Hz, 48 V LED String.
300 ms On – 300 ms Off
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 1 s / div.

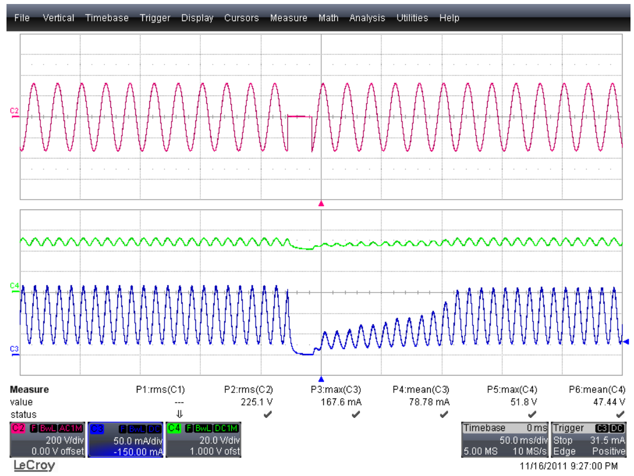

Figure 27 – 230 VAC / 50 Hz, 48 V LED String.
1-Cycle Drop-Out
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 50 ms / div.

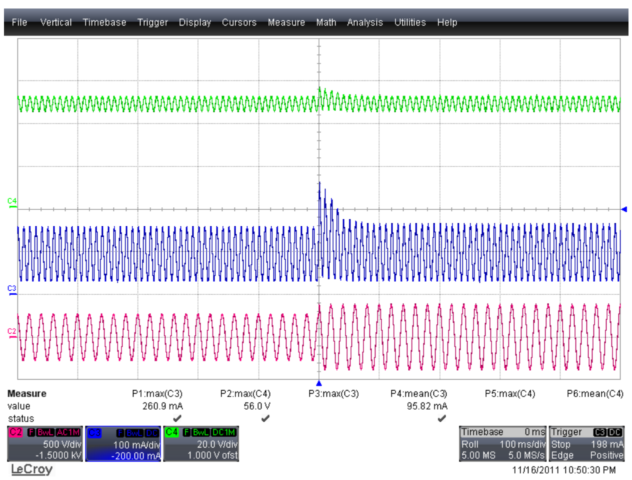

Figure 28 – Line Transient from 190 VAC to 265 VAC.
Ch2: V_{IN}, 500 V / div.
Ch3: I_{OUT}, 100 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 0.1 s / div.

10.7 Brown-out

Input voltage slew rate of 1 V / s from 190-0-190 VAC / 50 Hz line input variation; no failure observed.

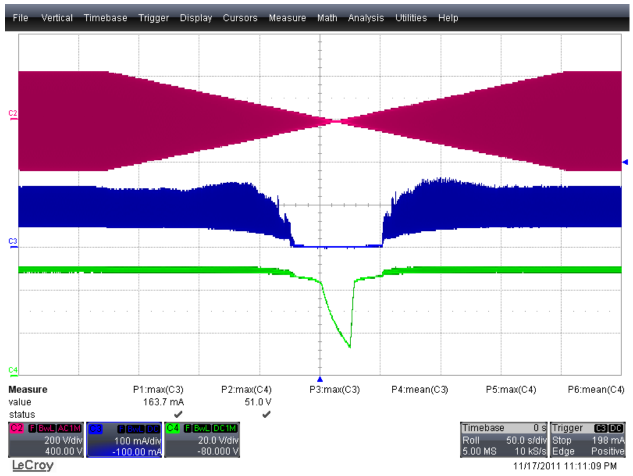

Figure 29 – 230 VAC / 50 Hz, 48 V LED String.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{OUT}, 100 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 50 s / div.

10.8 Disconnected Load

This LED driver is protected by VR1 in case of no-load condition in order to avoid leakage from the output capacitor.

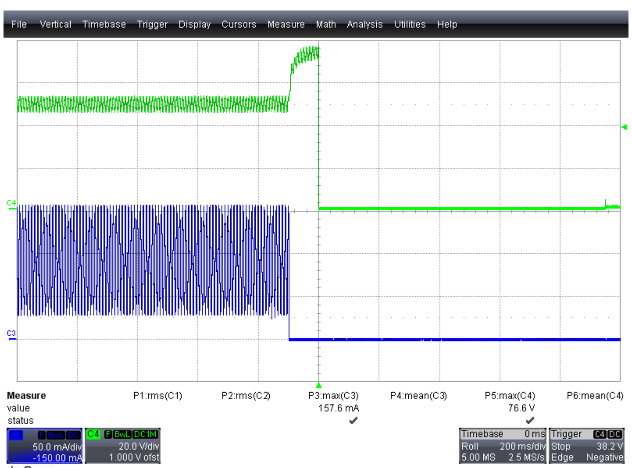

Figure 30 – 230 VAC / 50 Hz, 48 V LED String.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 0.2 s / div.

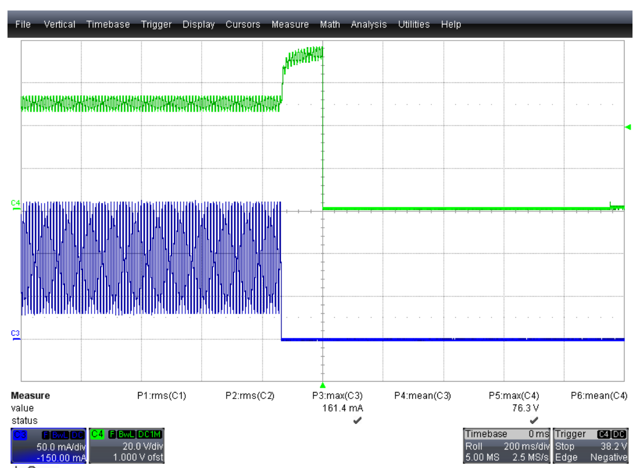

Figure 31 – 265 VAC / 50 Hz, 48 V LED String.
Ch3: I_{OUT}, 50 mA / div.
Ch4: V_{OUT}, 20 V / div.
Time Scale: 0.2 s / div.

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10.9 Line Surge Waveform

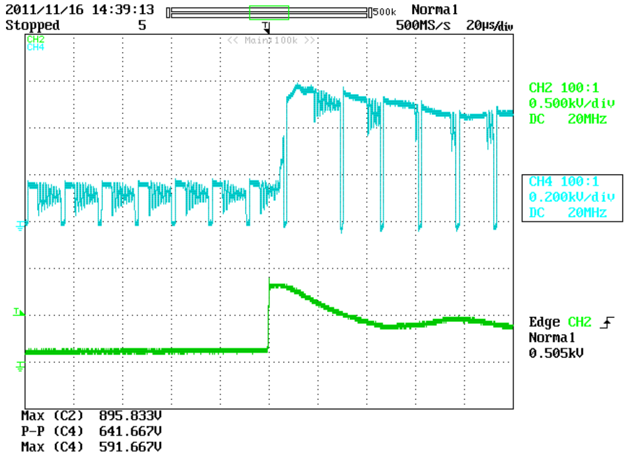

Figure 32 – 230 VAC / 60 Hz,
(+)1 kV Differential Line Surge at 0°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 591.67 V_{PK}

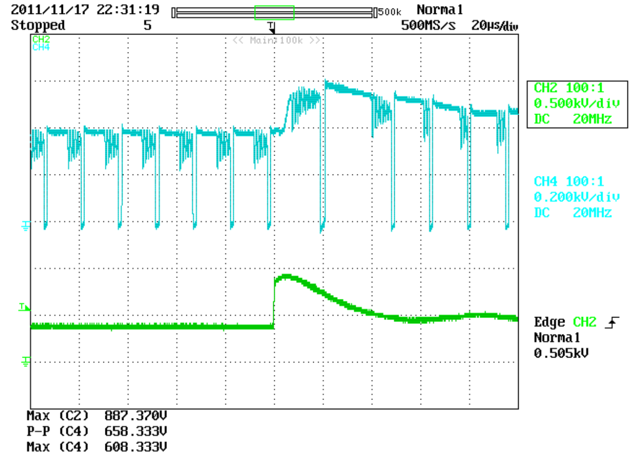

Figure 33 – 230 VAC / 60 Hz,
(+)1 kV Differential Line Surge at 90°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 608.33 V_{PK}

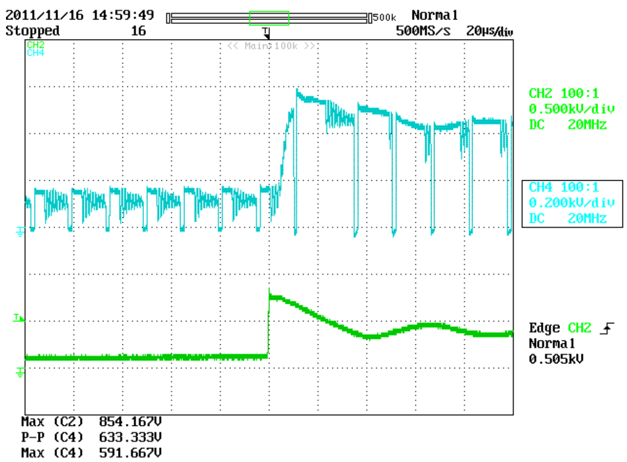

Figure 34 – 230 VAC / 60 Hz,
(-)1 kV Differential Line Surge at 0°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 591.67 V_{PK}.

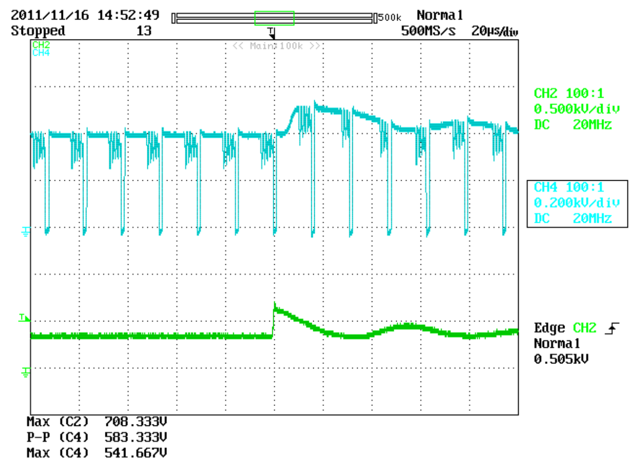

Figure 35 – 230 VAC / 60 Hz,
(-)1 kV Differential Line Surge at 90°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 541.67 V_{PK}.

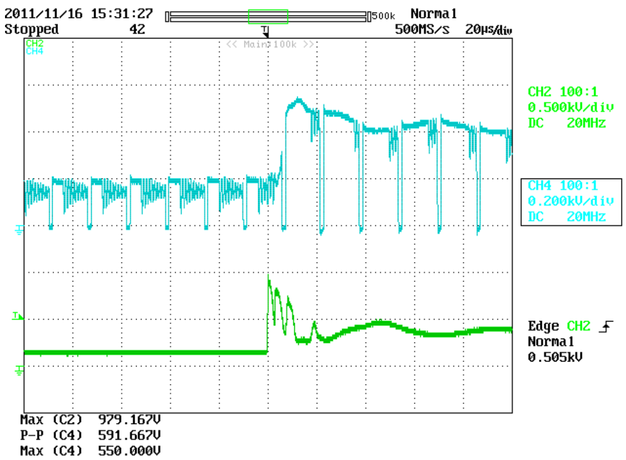

Figure 36 – 230 VAC / 60 Hz,
(+)2.5 kV Differential Ring Surge at 0°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 550.00 V_{PK}.

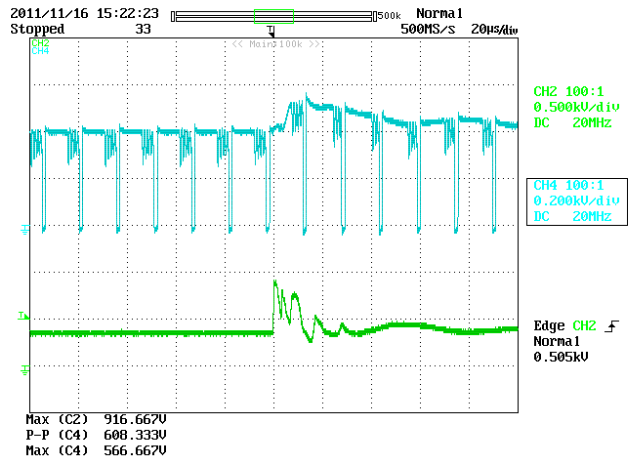

Figure 37 – 230 VAC / 60 Hz,
(+)2.5 kV Differential Ring Surge at 90°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 566.67 V_{PK}.

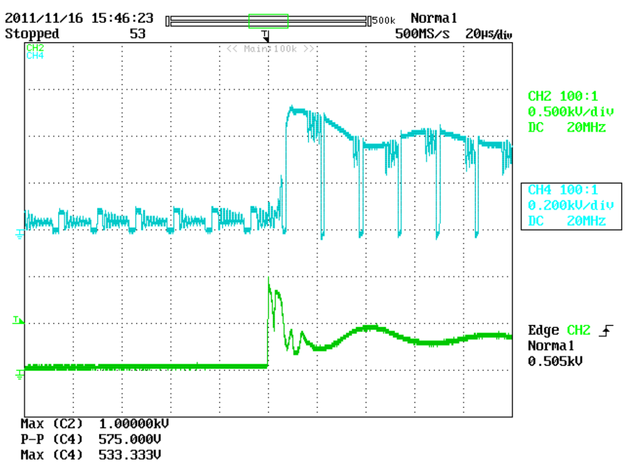

Figure 38 – 230 VAC / 60 Hz,
(-)2.5 kV Differential Ring Surge at 0°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 533.33 V_{PK}.

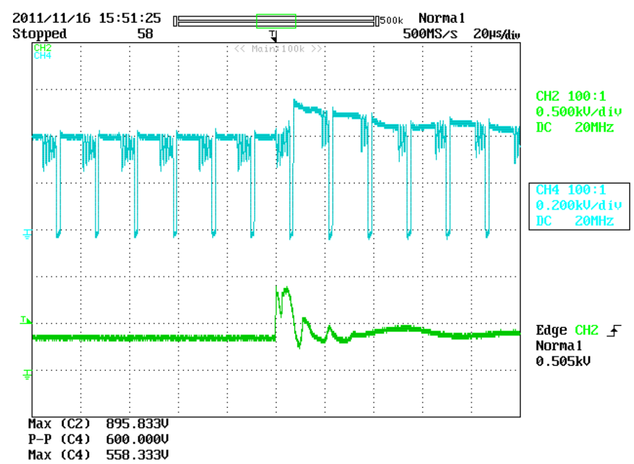

Figure 39 – 230 VAC / 60 Hz,
(-)2.5 kV Differential Ring Surge at 90°.
Ch2: V_{IN}, 500 V / div.
Ch4: V_{DS}, 200 V / div.
Time Scale: 20 µs / div.
V_{DS}: 558.33 V_{PK}.

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11 Line Surge

Input voltage was set at 230 VAC / 60 Hz. Output was loaded with 48 V LED string and operation was verified following each surge event.

Differential input line 1.2 / 50 μs surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

Differential input line ring surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass

Unit passes under all test conditions.

12 Conducted EMI

12.1 Equipment

Receiver:

Rohde & Schwartz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Schwartz
Two-Line-V-Network
Model No: ENV216

12.2 EMI Test Set-up

LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

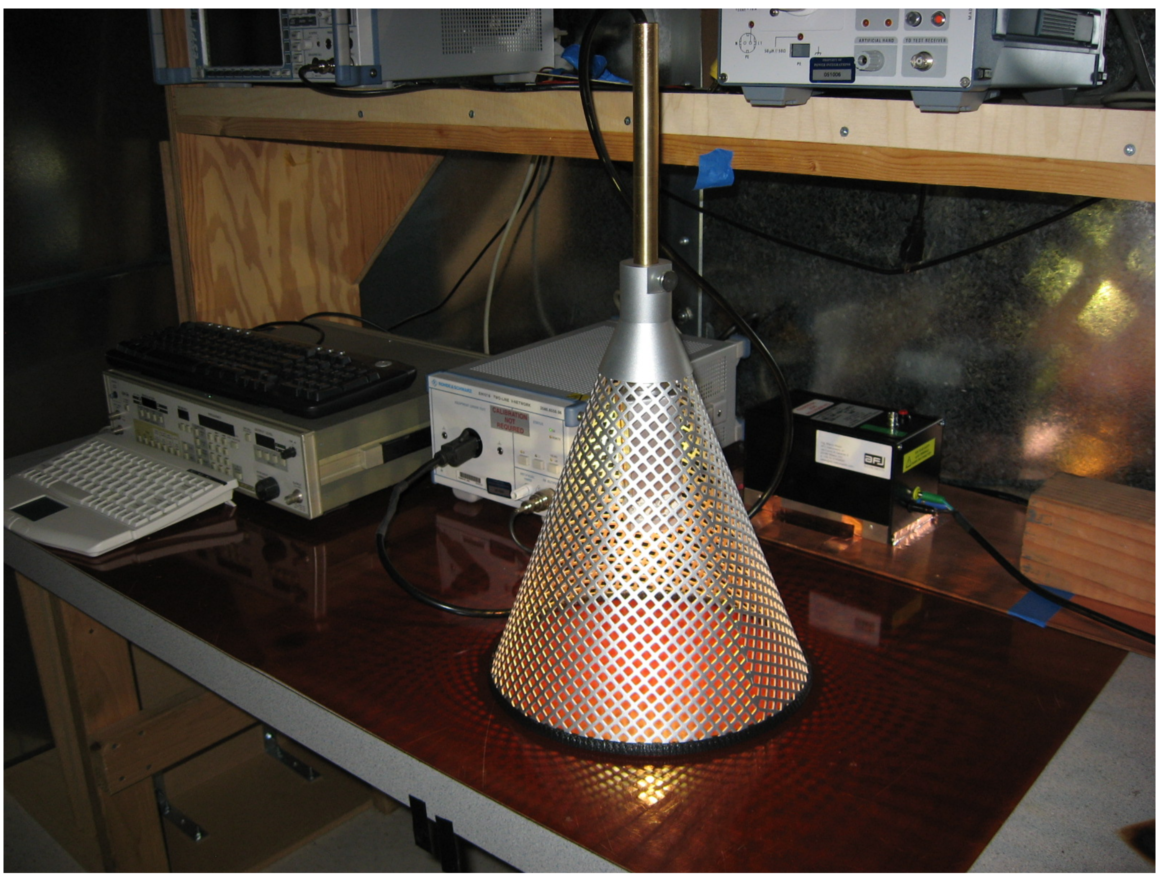

Figure 40 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

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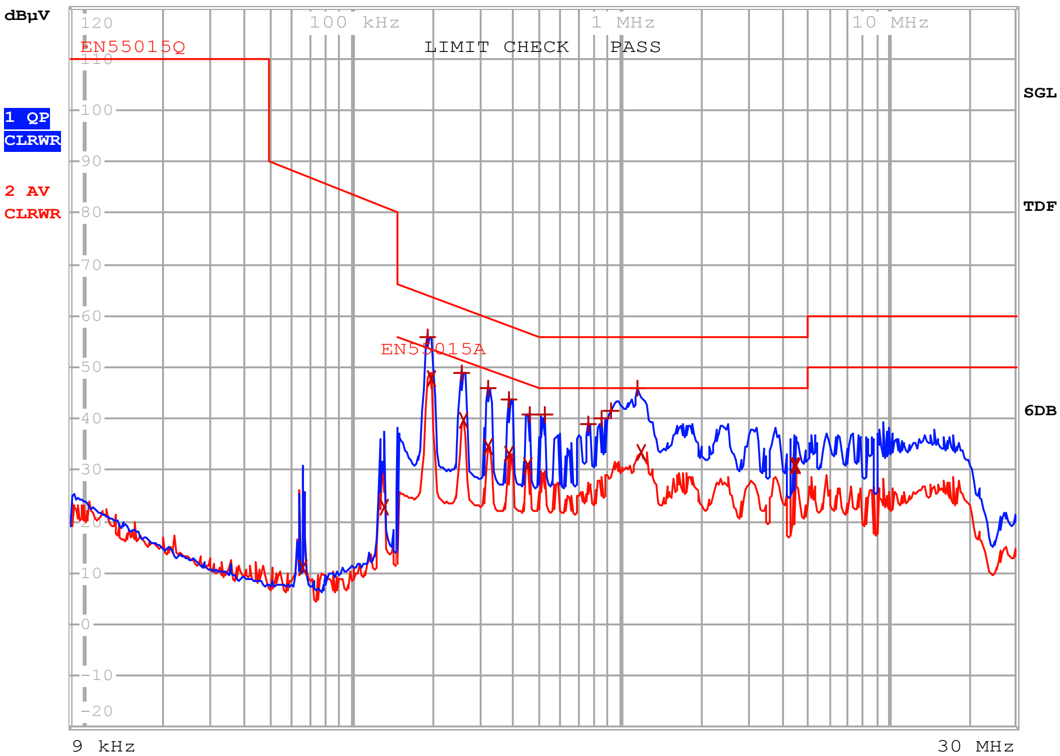
12.3 EMI Test Result



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	65.1922382836 kHz	10.99	N gnd	
2	Average	132.133649648 kHz	22.93	L1 gnd	
1	Quasi Peak	192.364799253 kHz	56.06	L1 gnd	-7.87
2	Average	196.231331718 kHz	47.61	L1 gnd	-6.15
1	Quasi Peak	256.711570318 kHz	48.95	L1 gnd	-12.58
2	Average	259.278686021 kHz	39.69	N gnd	-11.76
1	Quasi Peak	319.532962956 kHz	45.94	L1 gnd	-13.77
2	Average	322.728292586 kHz	34.63	L1 gnd	-15.00
1	Quasi Peak	386.030632509 kHz	43.63	L1 gnd	-14.51
2	Average	386.030632509 kHz	33.11	L1 gnd	-15.03
2	Average	452.651275966 kHz	31.04	L1 gnd	-15.77
1	Quasi Peak	461.749566613 kHz	40.97	L1 gnd	-15.68
1	Quasi Peak	525.514079005 kHz	40.72	L1 gnd	-15.27
1	Quasi Peak	759.408030975 kHz	39.14	L1 gnd	-16.85
1	Quasi Peak	855.719977385 kHz	40.06	L1 gnd	-15.93
1	Quasi Peak	917.447639259 kHz	41.60	L1 gnd	-14.39
1	Quasi Peak	1.16491505578 MHz	46.10	L1 gnd	-9.89
2	Average	1.1883298484 MHz	33.48	L1 gnd	-12.51
2	Average	4.46354295875 MHz	30.82	L1 gnd	-15.17
2	Average	4.55326017222 MHz	30.96	L1 gnd	-15.03

Figure 41 – Conducted EMI, 48 V / 90 mA Steady-State Load, 230 VAC, 60 Hz, and EN55015 Limits.

13 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Jan-12	DS	1.0	Initial Release	Apps & Mktg

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