Design Example Report

Title	***33W Dual Output DC-DC Power Forward Converter with Synchronous Rectification Forward using DPA425R***
Specification	Input: 36 - 72 VDC Output: 6.7V/4.2A, 11.1V/0.5A
Application	Satellite Receiver
Author	Power Integrations Applications Department
Document Number	DER-29
Date	March 30, 2004
Revision	1.0

Summary and Features

- Low Parts Count
- High Efficiency (90% at 48V with DPA425)
- Simple self-driven Synchronous Rectification
- 300kHz Operation
- Good Cross-regulation using Coupled Output Inductor
- Very low ripple on 6.7V output (<20mVp-p)
- Tight regulation (3% on 6.7V and 4% on 11.1V)

Power Integrations, Inc.
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Table of Contents

1 Introduction 3
2 Power Supply Specification 4
2.1 Schematic 5
2.2 Circuit Operation 6
2.3 Bill Of Materials 8
3 Layout 10
4 Design Spreadsheet 11
5 Transformer - T1 13
5.1 Transformer Construction 14
6 Inductor - L2 15
6.1 Inductor Construction 16
7 Performance Data 17
7.1 Efficiency 17
7.2 Regulation 17
7.2.1 Load Regulation 17
7.2.2 Line Regulation 18
7.3 Miscellaneous Performance 19
8 Performance Measurements 20
8.1 Drain Voltage and Current, Normal Operation 20
8.2 Output Voltage Startup 21
8.3 Load Transient Response (10% to 100% Load Step on 6.7V Output – 1kHz) 22
8.4 Load Transient Response (10% to 100% Load Step on the 6.7V Output) – Alternate repetition rate 23
8.5 Output Ripple Measurements 24
8.5.1 Ripple and Transient Load Measurement Setup 24
8.5.2 High Frequency (Switching Ripple) - Measurement Results 25
8.5.3 Lower Frequency Ripple - Measurement Results 25
9 Revision History 27

Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

1 Introduction

This document is an engineering report describing a dual output Forward converter using the DPA425R. The input voltage range is 36 to 72VDC providing two outputs of 6.7V and 11.1V at 33.7W. The power supply achieves approximately 89% efficiency with self-driven synchronous rectification on one output and a coupled output inductor for dual output regulation.

This document contains the power supply specification, schematic, and bill of materials, transformer documentation, printed circuit layout, and performance data .of the prototype supply.

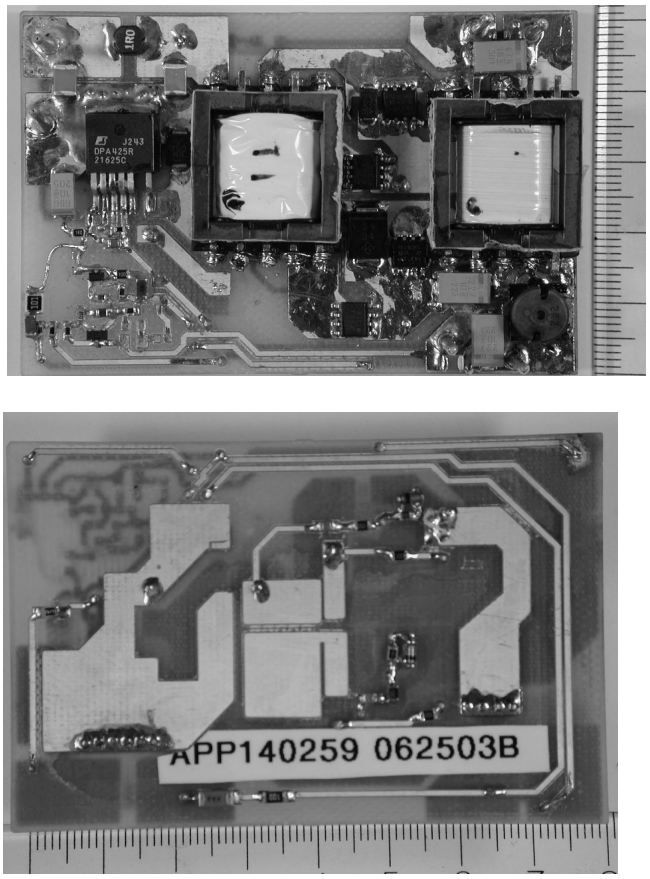


Figure 1 - Populated Circuit Board.

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	36		72	V_{DC}	Startup specified at < 36V.
Overload Input Current			-	1.28	A	Maximum allowed input current (36 V – 72 V)
Output1						
Output Voltage 1	V_{OUT1}	6.50	6.7	6.90	V	± 3%
Output Ripple Voltage 1	$V_{RIP1P-P}$			20	mVp-p	20 MHz Bandwidth
	$V_{RIP1RMS}$				mVrms	20 MHz Bandwidth
Output Dynamic Resp Voltage 1	V_{DYN1}			±300	mVp-p	200us settle time at 25°C 1A/us (10%-100% step, 1kHz)
Output Current 1	I_{OUT1}	0		4.2	A	
Output Over Current 1	I_{OUT1OC}	120		200	%	Autorecovery
Output Voltage 2	V_{OUT2}	10.66	11.1	11.54	V	± 4%
Output Ripple Voltage 2	$V_{RIP2P-P}$			100	mVp-p	20 MHz Bandwidth
	$V_{RIP2RMS}$				mVrms	20 MHz Bandwidth
Output Dynamic Resp Voltage 2	V_{DYN2}			±500	mVp-p	200us settle time at 25°C 1A/us (10%-100% step, 1kHz)
Output Current 2	I_{OUT2}	0.11		0.5	A	
Output Over Current 2	I_{OUT2OC}	120		800	%	Autorecovery
Total Output Power						
Continuous Output Power	P_{OUT}			33.7	W	
Peak Output Power	P_{OUT_PEAK}		-		W	
Efficiency	η	88			%	
Ambient Temperature	T_{AMB}	-40	25	90	°C	Free convection, Sea level

Desired physical dimensions: 6 x 2 x 0.5inches

2.1 Schematic

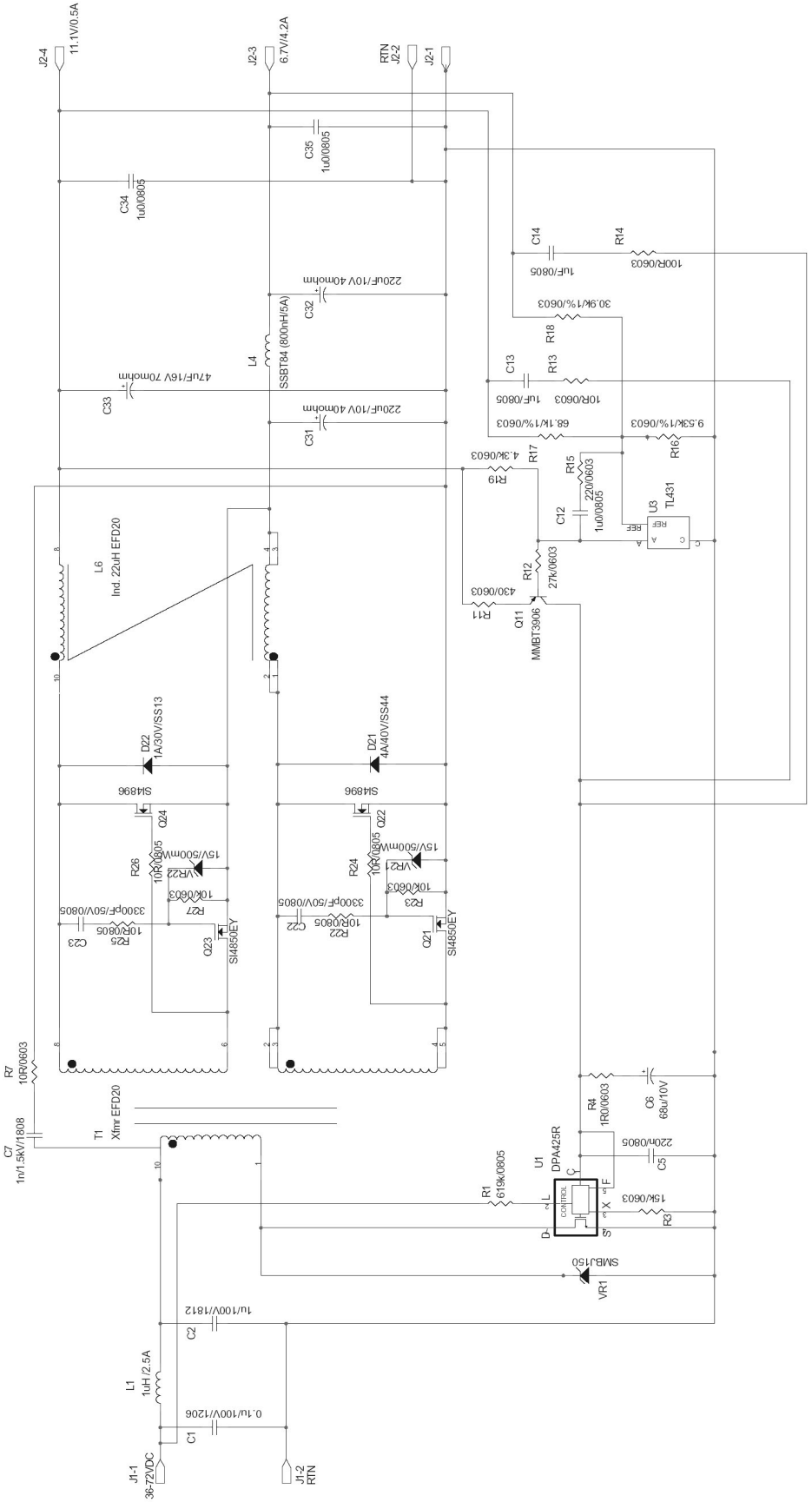


Figure 2 - Schematic

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

2.2 Circuit Operation

This circuit is design using synchronous rectification for the 6.7V and 11.1V outputs. The circuit also uses a coupled output inductor (L6) for better cross-regulation of both outputs, and the 11.1V is DC-stacked on top of the 6.7V output. Both outputs share regulation via the TL431.

The DPA425R is used to implement a forward converter with two outputs using a coupled inductor. The power supply also implements self-driven synchronous rectification to improve the efficiency. DPA425 is used for best efficiency.

The DC input voltage is filtered by C1, C2 and L1. The capacitor C1 is only present to minimize emissions back to the input line (it is not involved in the switching conversion). The zener diode VR1 is used to clamp the drain of the DPA-Switch to a safe level in the event of excessive voltage, though normally the resonant reset technique limits the voltage without the zener diode conducting.

The DPA-Switch has a local decoupling capacitor (C5) placed very close to Control and Source pins of the device. Also there is a larger decoupling capacitor (C6) which, in combination with R4, contributes to the control loop compensation. Resistor R3 sets the DPA-Switch external current limit to a safe level. This level will allow power delivery under normal operation, but programs the DPA-Switch maximum drain current to limit at a level above the normal operating peak current. This feature limits overload power delivery to the secondary during fault conditions and in-turn limits the maximum power that the supply will draw from the input line (even during fault conditions). The DPA-Switch also includes built-in short-circuit protection and other safety features. Resistor R1 programs the under-voltage and over-voltages start and stop thresholds for the device.

Capacitor C7 and resistor R7 are used to reduce common mode EMI emissions (and are optional). Under normal operation, the bias for the DPA-Switch comes directly from the 11.1V output. The transistor Q11 feeds back a current control signal from the secondary error signal circuit. The resistor R11 programs the high frequency gain of the secondary error signal circuit. Resistor R12 provides a connection to the TL431 error amplifier circuit. Due to the high gain of the transistor Q11, the resistor R12 can be chosen with a relatively high value also. If a low-value is chosen for the resistor R12 then the design may run into startup problems, whereby the parasitic collector-base diode of Q11 will load down the DPA-Switch control pin preventing startup. Therefore it is advisable to keep resistor R12 above 5 to 10kohm. The TL431 (U3) sinks a current through R12 to drive the transistor Q11. Capacitor C12 and resistor R15 provide compensation around the TL431. Resistor R18 is connected to the 6.7V output, R17 is connected to the 11.1V output and the resistor R16 provides the bottom resistor in the divider chain. These resistors control the TL431 thresholds which in turn control the DC-regulation point of the output voltages. Capacitor C13 and R13 provide phase boost to the control loop at higher frequencies

from the 11.1V output. This improves the transient response of the power supply. Capacitor C14 and R14 do the same from the 6.7V output.

The secondary is rectified using self-driven synchronous rectification. The 6.7V and 11.1V windings capacitively drive the two forward MOSFETs Q21 and Q23 through capacitors C22 and C23 with series resistors R22 and R25. The maximum voltage on the gate of Q21 and Q23 is clamped by Zener diodes VR21 and VR22. These diodes also provide a discharge path to deplete the charge in the C22 and C23 during the off-time for MOSFETs Q21 and Q23. The resistors R22 and R25 prevent low noise signals from interfering with the MOSFET drive (these resistor are optional). Resistor R23 and R27 ensure that the MOSFET is biased passively in the off-state to prevent accidental turn-on.

The catch MOSFETs Q22 and Q24 are driven directly from the 6.7V and 11.1V windings through series resistors R24 and R26. The catch MOSFETs do not conduct for the entire DPA-Switch off-time, and therefore parallel diodes D21 and D22 provide a conduction path for the remainder of the off-time when Q22 and Q24 are not active.

The two outputs are coupled through inductor L6. This inductor improves the cross-regulation between the two outputs (over that of non-coupled inductors). The load current is filtered by capacitors C31 and C32 on the 6.7V and C33 on the 11.1V output. There is an additional high frequency decoupling capacitor (C35 for 6.7V and C34 for 11.1V), placed right at the output pins of the supply.

Output inductor L4 in the 6.7V output attenuates the switching noise. However this inductor has to be chosen with the power supply transient response in mind.

Note1: output capacitor C33 is sized to accommodate the ripple current that can flow in this capacitor during an overload on the 11.1V output. The other components on the 11.1V output are chosen to also withstand overload conditions.

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

2.3 Bill Of Materials

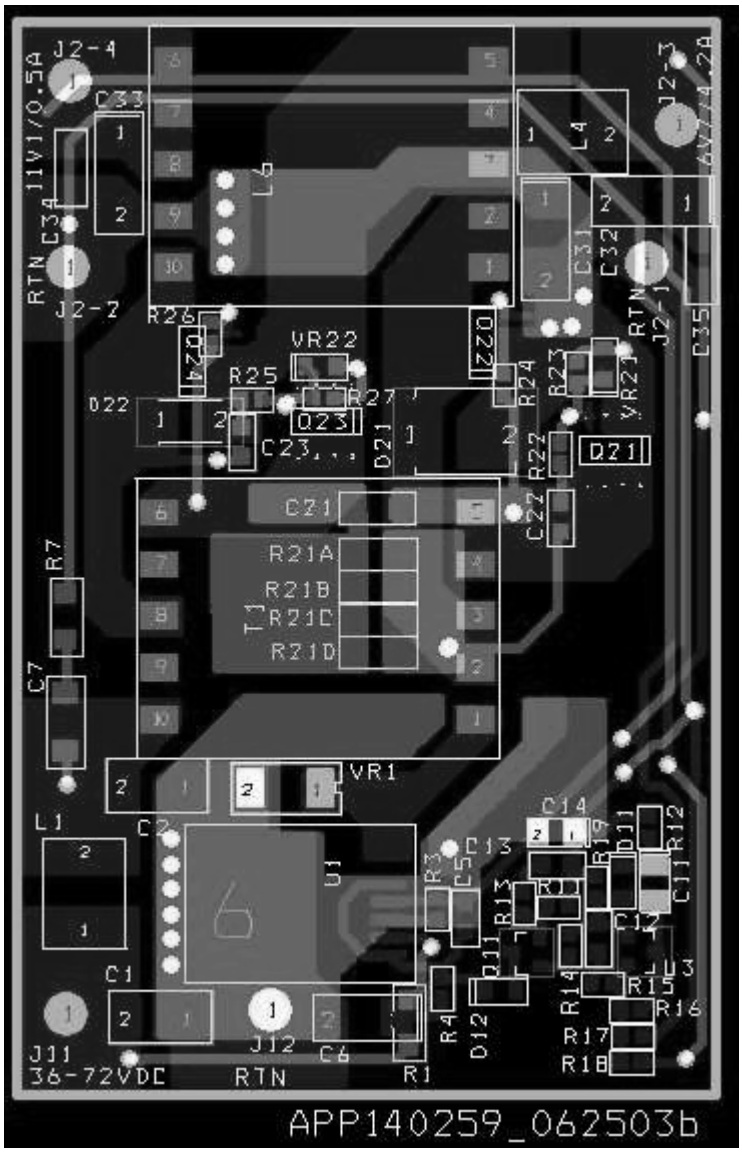
App140259 - 29W 6.4V/3.8A, 11.1V/0.5A - 061303c Revised: Thursday, June 12, 2003
Bill Of Materials

Item	Quantity	Reference	Part
1	1	C1	0.1u/100V/1206
2	1	C2	1u/100V/1812
3	1	C5	220n/0805
4	1	C6	68u/10V
5	1	C7	1n/1.5kV/1808
6	3	C12	1u0/0805
		C34	1u0/0805
		C35	1u0/0805
7	2	C14	1uF/0805
		C13	1uF/0805
8	2	C23	3300pF/50V/0805
		C22	3300pF/50V/0805
9	2	C32	220uF/10V 40mohm (Kemet - T520D227M010ASE040)
		C31	220uF/10V 40mohm (Kemet - T520D227M010ASE040)
10	1	C33	47uF/16V 70mohm (Kemet - T520D476M016ASE070)
11	1	D21	4A/40V/SS44
12	1	D22	1A/30V/SS13
13	1	L1	1uH /2.5A
14	1	L4	Inductor (modified to 800nH/5A [3T 2x29AWG]– (Tokin SSBT84)
15	1	L6	Coupled Inductor 22uH (EFD20)
16	1	Q11	MMBT3906
17	1	Q21	SI4850EY
18	2	Q24	SI4896
		Q22	SI4896
19	1	Q23	SI4850EY
20	1	R1	619k/0805
21	1	R3	15k/0603
22	1	R4	1R0/0603
23	2	R13	10R/0603
		R7	10R/0603
24	1	R11	430/0603
25	1	R12	27k/0603
26	1	R14	100R/0603
27	1	R15	220/0603
28	1	R16	9.53k/1%/0603
29	1	R17	68.1k/1%/0603
30	1	R18	30.9k/1%/0603

31	1	R19	4.3k/0603
32	4	R22	10R/0805
		R24	10R/0805
		R25	10R/0805
		R26	10R/0805
33	2	R27	10k/0603
		R23	10k/0603
34	1	T1	Customer Transformer (EFD20)
35	1	U1	DPA425R
36	1	U3	TL431
37	1	VR1	150V Clamp Zener SMBJ150
38	2	VR22	15V/500mW
		VR21	15V/500mW

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

3 Layout


J2-4
11V1/0.5A
C33
C34
RTN
J2-2
L4
L5
J2-3
6V/14.2A
C31
C32
RTN
J2-1
C35
R26
VR22
R25
R27
Q24
Q22
Q23
D22
C23
D21
R24
R23
VR21
R22
D21
C22
C21
R21A
R21B
T1
R21C
R21D
R7
C7
VR1
L1
C2
U1
C14
C13
R3
C5
R13
R9
D11
R12
C11
C12
C1
J11
36-72VDC
J12
RTN
C6
R1
R4
D12
R14
R15
R16
R17
R18
APP140259_062503b

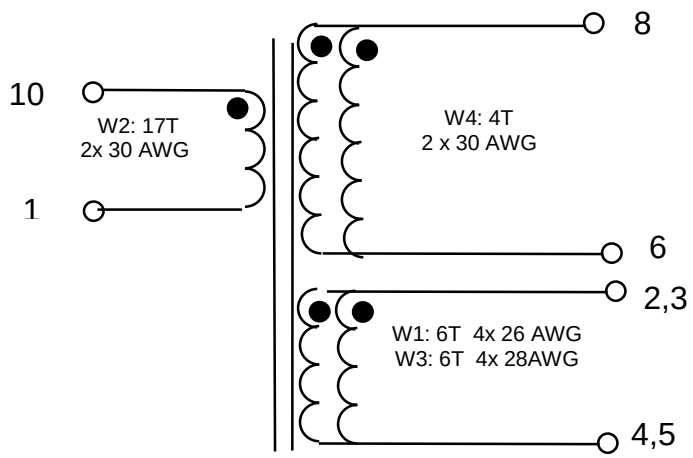
4 Design Spreadsheet

DCDC_DPAFwd_rev1.03_092702 Copyright Power Integrations Inc. 2002	INPUT	INFO	OUTPUT	UNIT	DPA_092702_R102xls: DPA-Switch Forward Transformer Design Spreadsheet
OUTPUT VOLTAGE AND CURRENT					
VMAIN	6.7			Volts	Main output voltage
IMAIN	4.2			Amps	Main output current
VOUT2	11.1			Volts	Output2 voltage
IOUT2	0.5			Amps	Output2 current
POUT			33.69	Watts	Total output power
VBIAS	12.0			Volts	DC bias voltage from output inductor winding
INPUT VOLTAGE AND UV/OV					
VMIN	36			DC volts	Minimum DC input voltage
VMAX	75			DC volts	Maximum DC input voltage
		min	max		
VUV OFF		29.34	32.35573	DC volts	Minimum undervoltage On-Off threshold
VUV ON		31.45101	33.8636	DC volts	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		73.06809	-	DC volts	Minimum overvoltage Off-On threshold
VOV OFF		-	92.36876	DC Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			603.1461	kOhm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
ENTER DPA-Switch VARIABLES					
DPA-Switch	**dpa425**			16VDC	36VDC
Chosen Device	*#N/A*		Power	31W	70W
ILIMIT	*#REF!*	5.35		Amps	From DPA-Switch datasheet
Frequency - (F)=400kHz, (L)=300kHz					Low (L) frequency option - 300kHz
fS	*#REF!*	317000	300000	Hertz	From DPA-Switch datasheet
KI	0.45				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITEXT			2.0925	Amps	External current limit. Use 1% resistor to set current limit
RX			14.99575	kOhm	Current Limit resistor value (X-pin) - assumes minimum datasheet curve (fig 32)
DUVON GOAL	0.67		0.67		Maximum allowed duty cycle at VUV ON MIN undervoltage threshold
KDI	0.15		0.15		Maximum current ripple factor
VDS			0.9	Volts	DPA-Switch average on-state Drain to Source Voltage
VDSOP			174.6585	Volts	Required drain voltage for guaranteed transformer reset
DIODE Vf SELECTION					
VDMAIN	0.05		0.05	Volts	Main output diodes forward voltage drop
VDOUT2	0.05		0.05	Volts	Secondary output diodes forward voltage drop
VDB			0.7	Volts	Bias diode forward voltage drop
TRANSFORMER CORE SELECTION					
Core Type	**efd20**				
Core		EFD20		P/N:	EFD20-3F3-Exxx-xx
Bobbin		EFD20_Bobbin		P/N:	CPHS-EFD20-1S-10P-T
AE			0.31	cm^2	Core Effective Cross Sectional Area
LE			4.7	cm	Core Effective Path Length
AL			1200	nH/T^2	Ungapped Core Effective Inductance
BW			13.5	mm	Bobbin Physical Winding Width
LG MAX			0.002	mm	Maximum actual gap when zero gap specified
D FACTOR			1		Duty cycle factor
L	1.00				Transformer primary layers (split primary recommended)
NMAIN	6		6		Main rounded turns
NS2	4		4		Vout2 rounded secondary turns (AC stacked winding)
VOUT2 ACTUAL			11.2	Volts	Approximate Output2 voltage of with NS2 = 4 turns (AC stacked secondary)

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

TRANSFORMER DESIGN PARAMETERS					
NP			18		Primary rounded turns
BM			1286.891	Gauss	Max operating flux density at minimum switching frequency
BP			2468.015	Gauss	Max transient flux density at minimum switching frequency
LP MIN			0.366237	mHenries	Minimum primary magnetizing inductance (assumes LG MAX=2um)
IMAG			0.184307	Amps	Peak magnetizing current at minimum input voltage
OD_P			0.825979	mm	Primary wire outer diameter
AWG_P		Warning	20	AWG	!!! Primary < 27AWG: decrease L, increase NP, consider multifilar winding
DUTY CYCLE VALUES					
DUVON MIN			0.662826		Duty cycle at minimum undervoltage threshold
DVMIN			0.576923		Duty cycle at minimum DC input voltage
DVMAX		Warning	0.273279		!!! DVMAX > derated duty cycle limit: decrease DUVON GOAL
DOVOFF MAX			0.221387		Duty cycle at maximum DC overvoltage threshold
CURRENT WAVESHAPE PARAMETERS					
IP		Warning	1.890914	Amps	!!! Exceeds derated current limit: increase KI, decrease KDI, increase DPA-Switch s
IPRMS			1.274364	Amps	Maximum primary RMS current at minimum DC input voltage
COUPLED INDUCTOR OUTPUT PARAMETERS					
LMAIN			21.65724	uHenries	Main / Output2 coupled output inductance (referred to Main winding)
WLMAIN			274.3371	uJoules	Main / Output2 coupled output inductor full-load stored energy
KDIMAIN			0.15		Current ripple factor of combined Main and Output2 outputs
nOUT2			1.651852		Approximate turns ratio for Output2 winding
nBIAS			1.881481		Approximate turns ratio for Bias winding
SECONDARY OUTPUT PARAMETERS					No derating
ISMAINRMSLL			3.569906	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
ISOUT2RMSLL			0.379777	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
IDAVMAIN			3.052227	Amps	Maximum average current, Main rectifier (single device rating)
IDAVOUT2			0.36336	Amps	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			0.181865	Amps	Maximum RMS current, Main output capacitor
IRMSOUT2			0.021651	Amps	Maximum RMS current, Out2 output capacitor
VPIVMAIN			48.43949	Volts	Main rectifiers peak-inverse voltage
VPIVOUT2			80.73248	Volts	Output2 rectifiers peak-inverse voltage
VPIVB			56.77612	Volts	Bias output rectifier peak-inverse voltage

5 Transformer - T1



MATERIALS

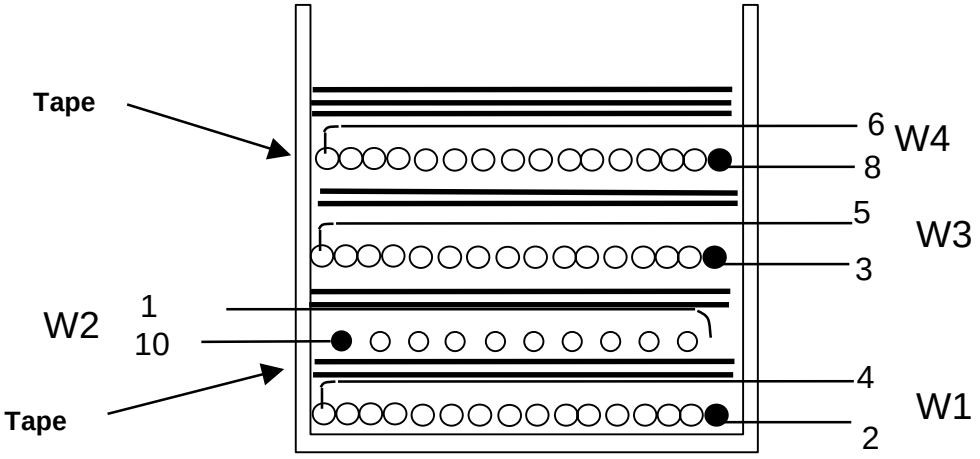
Item	Description
[1]	Core: EFD20 3F3 Material Ferroxcube P/N EFD20-3F3 **ungapped**
[2]	Bobbin: 10 pin EFD20 surface mount B&B B-060 or equivalent
[4]	Magnet Wire: #30 AWG Double Coated
[5a]	Magnet Wire: #26 AWG Double Coated
[5b]	Magnet Wire: #28 AWG Double Coated
[6]	16.7mm Insulation Tape
[7]	Varnish

ELECTRICAL SPECIFICATIONS:

Electrical Strength	1 second, from Pins 1, 10 to Pins 2,3,4,5,6,7,8,9	1500 VDC
Creepage	Between Pins 1,10 and Pins 2,3,4,5,6,7,8,9	N/A
Primary Inductance	Pins 1,10, all other windings open, measured at 100KHz, 400mVRMS	327 µH, (384uH actual) ±25 %
Resonant Frequency	Pins 1,10, all other windings open	2.006 MHz (Min.)
Primary Leakage Inductance	Pins 1,10, with Pins 2,3,4,5,6,7,8,9 shorted, measured at 100KHz, 400mVRMS	0.900 µH (Max.)

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

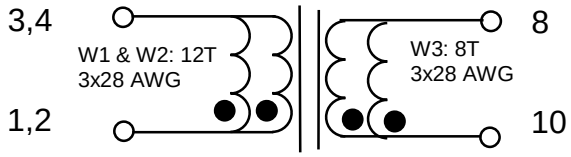
5.1 Transformer Construction



WINDING INSTRUCTIONS:

W2 (Sec1a)	With two windings in parallel: Start at Pin 2. Wind **6 turns quad** item [5a] Finish on Pin 4
Insulation	Use two layers of item [6] for insulation.
W2 (Primary)	Start at Pin 10. Wind 17 **turns bifilar** of item [4] in 1 layer. Finish at Pin 1. .
Insulation	Use two layers of item [6] for insulation.
W3 (Sec1b)	Start at Pin 3. Wind **6 turns quad** item [5b] Finish on Pin 5
Insulation	Use two layers of item [6] for insulation.
W4 (Sec2)	Start at Pin 8. Wind **4 turns bifilar** item [4] Finish on Pin 6. Spread evenly over single layer
Outer Wrap	Wrap windings with 3 layers of tape item [6].
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [7]).

6 Inductor - L2



MATERIALS

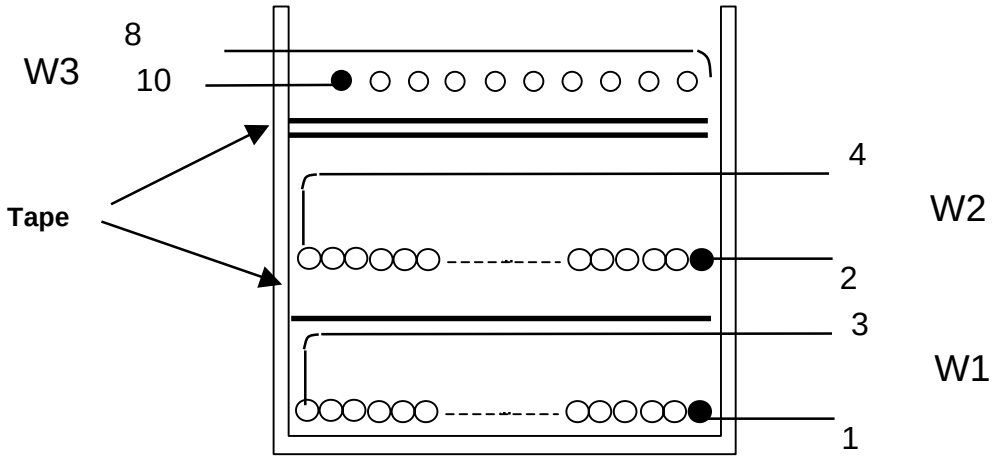
Item	Description
[1]	Core: EFD20 3F3 Material Ferroxcube P/N EFD20-3F3 gap for A_L of 153 nH/T^2
[2]	Bobbin: 10 pin EFD20 surface mount B&B B-060 or equivalent
[3]	Magnet Wire: #26 AWG Double coated
[5]	Insulation Tape
[6]	Varnish

ELECTRICAL SPECIFICATIONS:

Electrical Strength		N/A
Creepage		N/A
Primary Inductance	Pins 1,2-3,4 all other windings open, measured at 100KHz, 400mVRMS	22µH, (actual 23.735uH) ±25 %
Resonant Frequency	Pins 1,2-3,4, all other windings open	8.366 MHz (Min.)
Primary Leakage Inductance		0.651uH

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

6.1 Inductor Construction



WINDING INSTRUCTIONS:

W1	With two windings in parallel: Start at Pin 1. Wind **12 turns trifilar** item [3] Finish on Pin 3
Basic Insulation	Use layer of item [6] for basic insulation.
W2	With two windings in parallel: Start at Pin 2. Wind **12 turns trifilar** item [3]. Finish on Pin 4
Basic Insulation	Use layer of item [6] for basic insulation.
W3	Start at Pin 10. Wind **8 turns trifilar** item [4]. Finish on Pin 8
Outer Wrap	Wrap windings with 3 layers of tape item [5].
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [6]).

7 Performance Data

All measurements performed at room temperature.

7.1 Efficiency

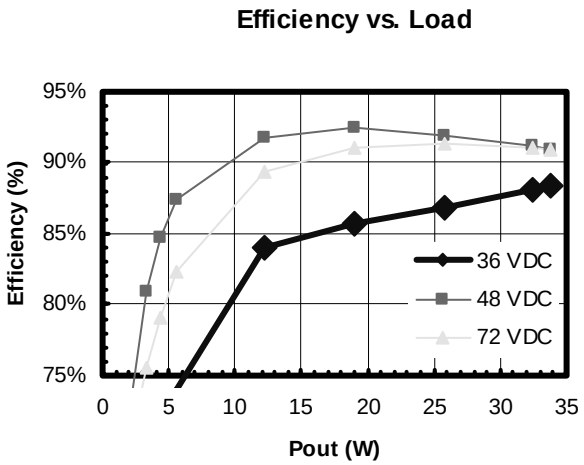


Figure 3- Efficiency vs. Load, Room Temperature

7.2 Regulation

7.2.1 Load Regulation

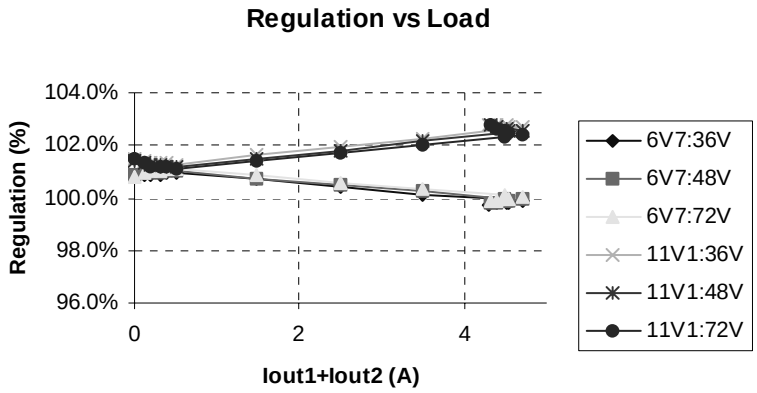


Figure 4 – Load Regulation, Room Temperature

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

7.2.2 Line Regulation

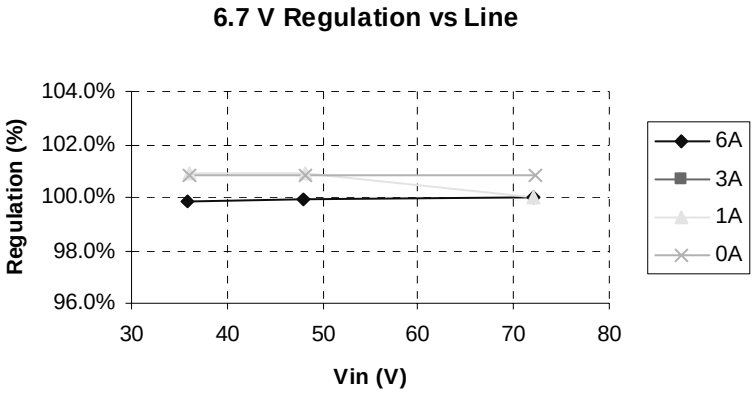


Figure 5 – Line Regulation, Room Temperature, Full Load

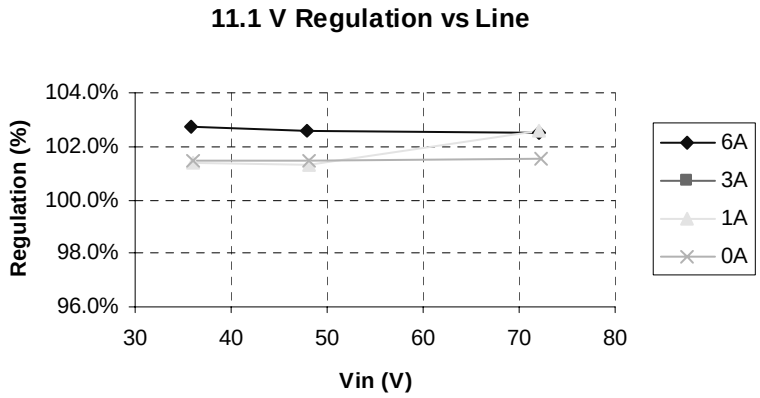


Figure 6 – Line Regulation, Room Temperature, Full Load

7.3 Miscellaneous Performance

Max/Min Regulation Performance over all Line and Load conditions

Description	Min	Max	Min	Max
6.7V Output	6.6825	6.775	99.7 %	101.1 %
11.1V Output	11.222	11.412	101.1 %	102.8 %

Max/Min Regulation Performance over all Line and Load conditions

Description	Input Current (Max)	Input Voltage	Output Current	% of Max load
6.7V Overload	1.27 A	36 V	5.88 A	140 %
11.1V Overload	1.25 A	36 V	3.53 A	706%

Line Under/Overvoltage

Description	V off (min)	V off (max)	V on (min)	V on (max)
Undervoltage	29.3 V	32.4 V	31.5 V	33.9 V
Overvoltage	73.1V	-	-	92.4 V

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

8 Performance Measurements

8.1 Drain Voltage and Current, Normal Operation

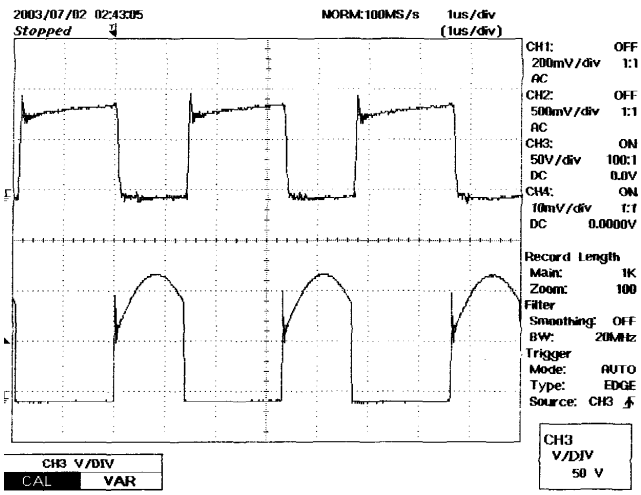


Figure 7 – 36 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: I_{DRAIN}, 1 A/ div
Lower: V_{DRAIN}, 50 V/ div, 1 µs / div

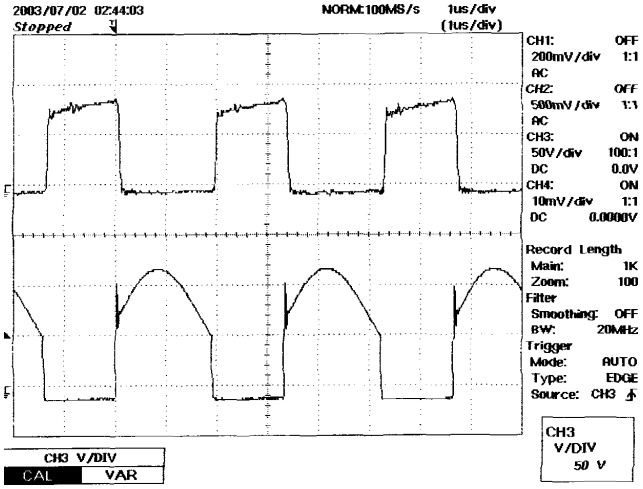


Figure 8 – 48 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: I_{DRAIN}, 1 A/ div
Lower: V_{DRAIN}, 50 V/ div, 1 µs / div

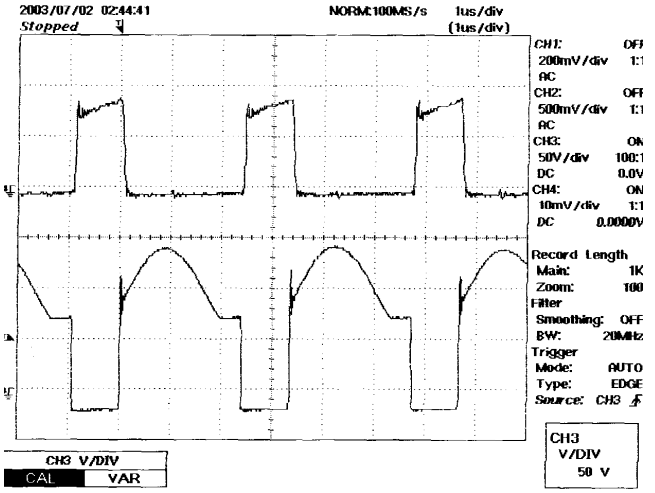


Figure 9 – 72 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: I_{DRAIN}, 1 A/ div
Lower: V_{DRAIN}, 50 V/ div, 1 µs / div

8.2 Output Voltage Startup

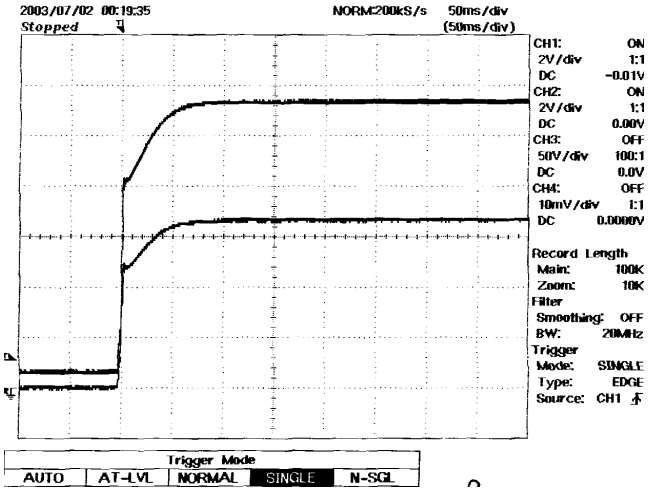


Figure 10 – 36 VDC Startup, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: $V_{11.1V}$, 2 V / div
Lower: V_{6V7}, 2 V/ div, 50 ms / div

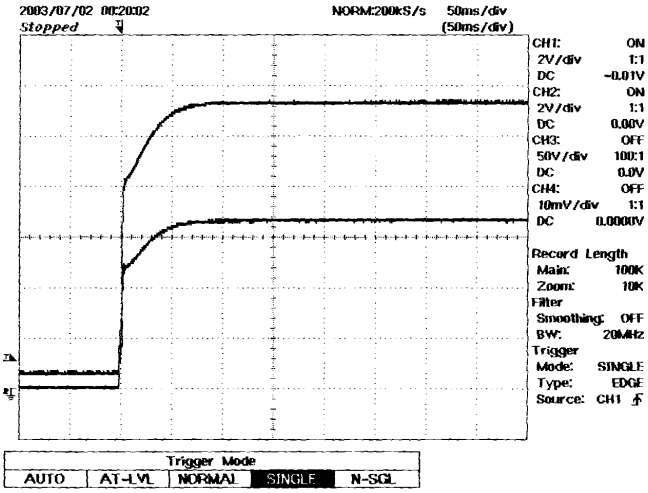


Figure 11 – 48 VDC Startup, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: $V_{11.1V}$, 2 V / div
Lower: V_{6V7}, 2 V/ div, 50 ms / div

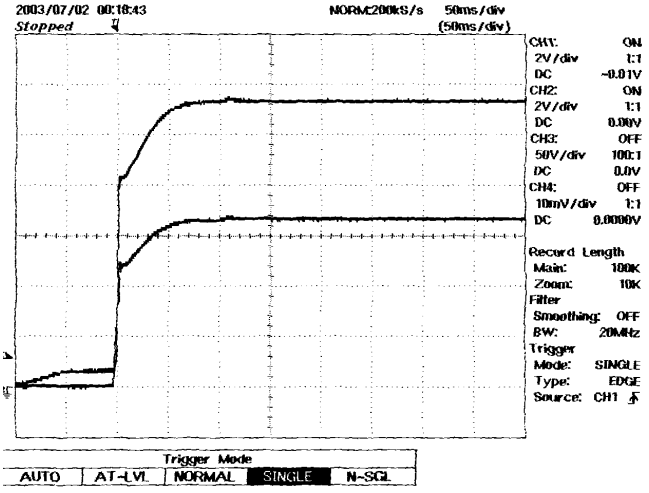


Figure 12 – 72 VDC Startup, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: $V_{11.1V}$, 2 V / div
Lower: V_{6V7}, 2 V/ div, 50 ms / div

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

8.3 Load Transient Response (10% to 100% Load Step on 6.7V Output – 1kHz)

In these figures shown below, no averaging was used. .

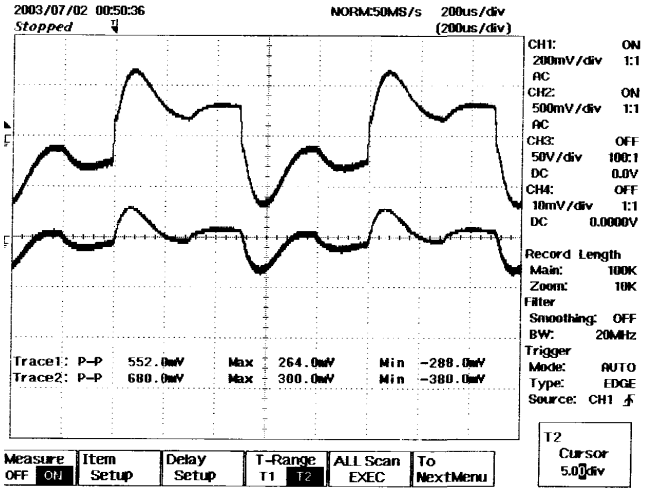


Figure 13 – 36 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 200 µs / div.

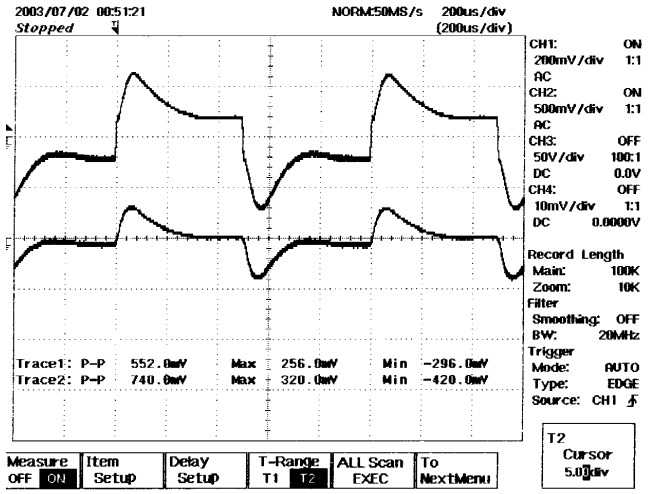


Figure 14 – 48 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step on (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 200 µs / div.

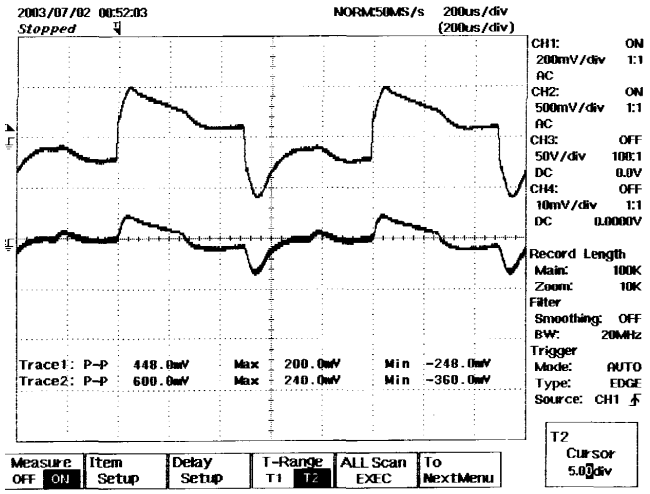


Figure 15 – 72 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step on (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 200 µs / div.

8.4 Load Transient Response (10% to 100% Load Step on the 6.7V Output) – Alternate repetition rate

In these figures shown below, no averaging was used. .

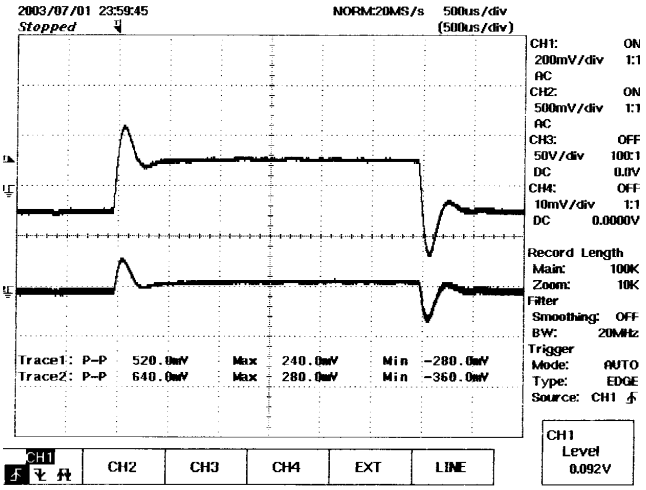


Figure 16 – 36 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step on (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 500 µs / div.

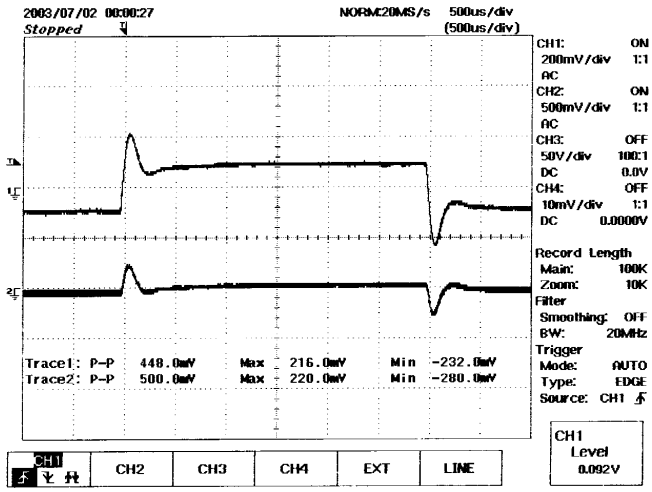


Figure 17 – 48 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step on (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 500 µs / div.

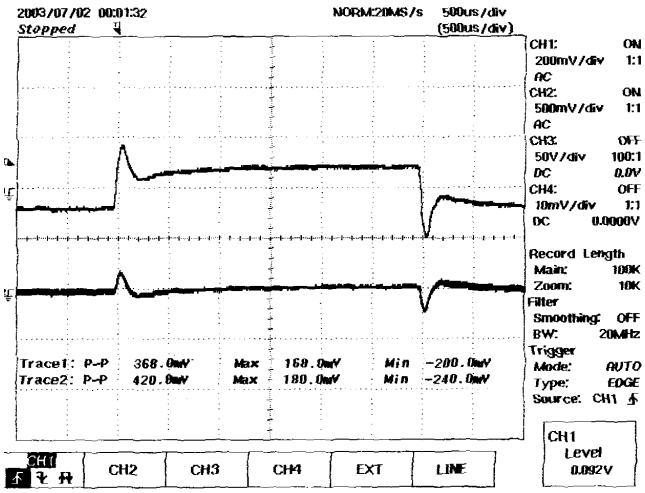


Figure 18 – 72 VDC Load Transient, 6.7V output 4.2-0.42-4.2 Amp Load Step on (1A/us slew-rate).
Top: 6.7V Output Voltage 200 mV / div
Lower : 11.1V Output Voltage 500 mV, 500 µs / div.

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

8.5 Output Ripple Measurements

8.5.1 Ripple and Transient Load Measurement Setup

Two copper strips are used at the output pins of the power supply. On these copper strips a 1uF ceramic capacitor is placed close to the output pins followed by a 10uF/50V capacitor. The voltage is remotely measured at the actual pins of the power supply. The electronic load is applied at the end of the copper strips.

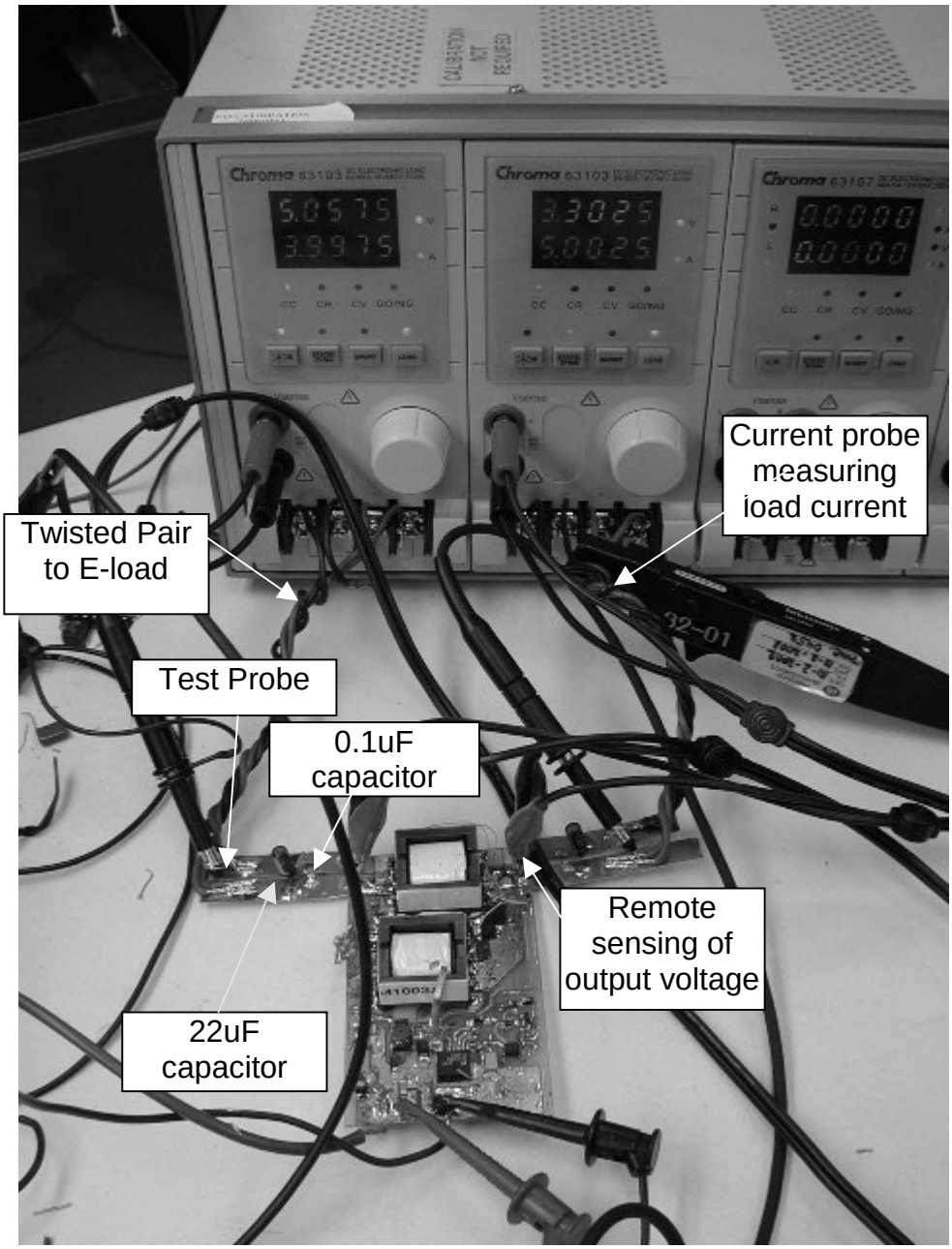


Figure 19 – Transient load and ripple measurement set up

8.5.2 High Frequency (Switching Ripple) - Measurement Results

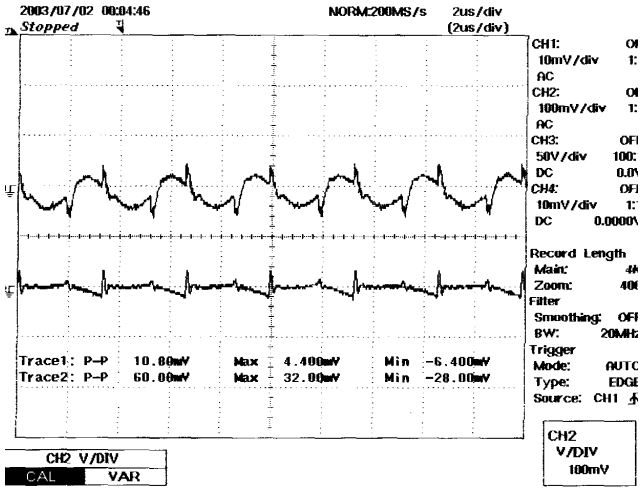


Figure 20 - Ripple, 36 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 2 us, 100 mV / div

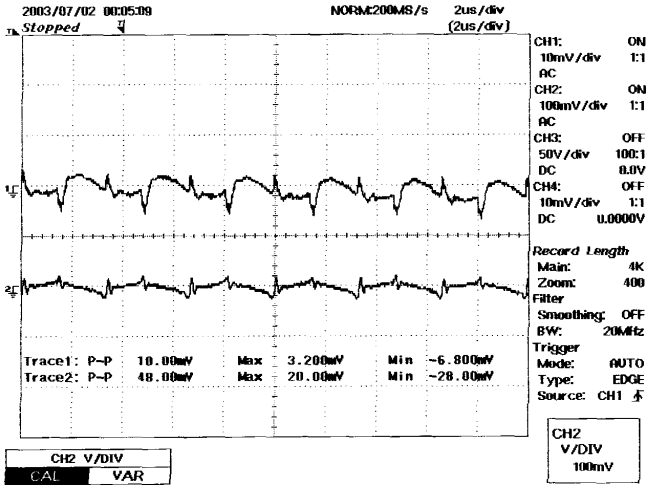


Figure 21 - Ripple, 48 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 2 us, 100 mV / div

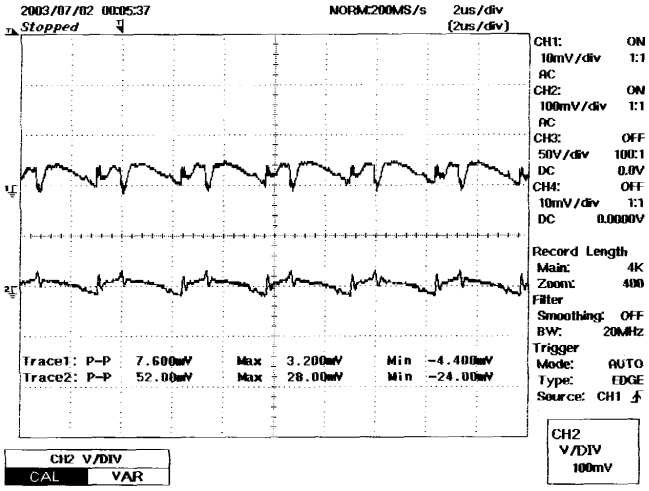


Figure 22 - Ripple, 72 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 2 us, 100 mV / div

8.5.3 Lower Frequency Ripple - Measurement Results

Power Integrations, Inc.
Tel: +1 408 414 9660 Fax: +1 408 414 9760
www.powerint.com

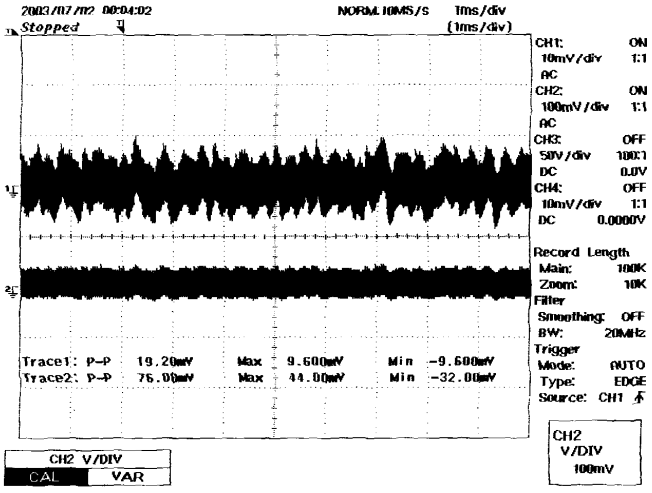


Figure 23 - Ripple, 36 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 1 ms, 100 mV / div

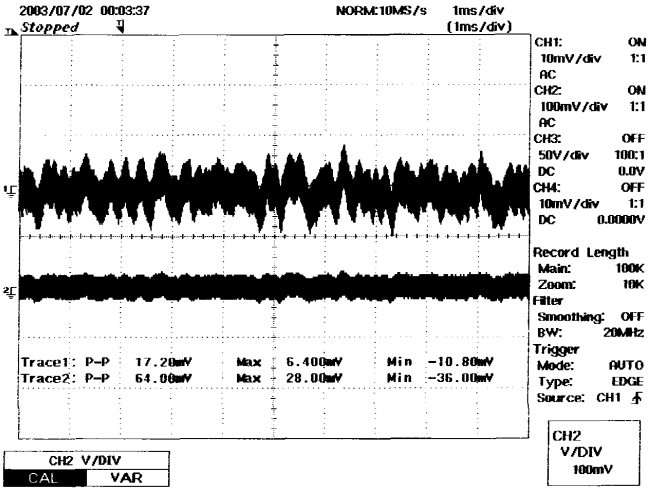


Figure 24 - Ripple, 48 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 1 ms, 100 mV / div

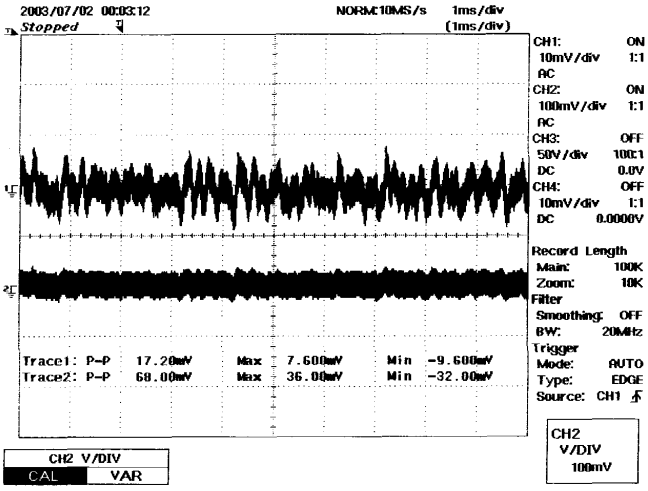


Figure 25 - Ripple, 72 VDC, Full Load (6.7V/4.2 A,11.1V/0.5 A)
Upper: 6.7V Output 10 mV / div
Lower: 11.1V Output, 1 ms, 100 mV / div

9 Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	RM	1.0	Initial release	VC / AM

Power Integrations, Inc.
Tel: +1 408 414 9660 Fax: +1 408 414 9760
www.powerint.com

For the latest updates, visit our Web site: *www.powerint.com*

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein, nor does it convey any license under its patent rights or the rights of others.

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at *www.powerint.com*.

The PI Logo, ***TOPSwitch, TinySwitch***, ***LinkSwitch***, and ***EcoSmart*** are registered trademarks of Power Integrations, Inc. ***PI Expert*** and ***DPA-Switch*** are trademarks of Power Integrations, Inc.

WORLD HEADQUARTERS AMERICAS
Power Integrations, Inc.
5245 Hellyer Avenue
San Jose, CA 95138 USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
E-Mail:
usasales@powerint.com

EUROPE & AFRICA
Power Integrations (Europe) Ltd.
Centennial Court
Easthampstead Road
Bracknell
Berkshire RG12 1YQ,
United Kingdom
Phone: +44-1344-462-300
Fax: +44-1344-311-732
E-Mail:
eurosales@powerint.com

SINGAPORE
Power Integrations, Singapore
51 Goldhill Plaza #16-05
Republic of Singapore 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
E-Mail:
singaporesales@powerint.com

TAIWAN
Power Integrations
International Holdings, Inc.
17F-3, No. 510,
Chung Hsiao E. Rd., Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
E-Mail:
taiwansales@powerint.com

CHINA
Power Integrations
International Holdings, Inc.
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu
Shenzhen Guangdong,
518031, China
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
E-Mail:
chinasales@powerint.com

KOREA
Power Integrations
International Holdings, Inc.
8th Floor, DongSung Building
17-8, Yoido-dong,
Youngdeungpo-gu,
Seoul, 150-874, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
E-Mail:
koreasales@powerint.com

JAPAN
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
E-Mail:
japansales@powerint.com

INDIA (Technical Support)
Innovatech
#1, 8th Main Road
Vasanthnagar
Bangalore, India 560052
Phone: +91-80-226-6023
Fax: +91-80-228-9727
E-Mail:
indiasales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760