Design Example Report

Title	***No Electrolytic Capacitor, High Efficiency (≥82%), High Power Factor (>0.9) TRIAC Dimmable 7 W_{TYP} LED Driver Using LinkSwitch™-PH LNK403EG***
Specification	90 VAC – 265 VAC Input; 18 V_{TYP}, 0.38 A Output
Application	LED Driver
Author	Applications Engineering Department
Document Number	DER-277
Date	March 28, 2011
Revision	1.0

Summary and Features

- No electrolytic capacitor
- TRIAC dimmer compatible (including low cost leading edge type)
  - No output flicker
  - >100:1 dimming range
- Clean monotonic start-up – no output blinking
- Fast start-up (<100 ms) – no perceptible delay
- Consistent dimming performance unit to unit
- Highly energy efficient
  - ≥82% at 115 VAC, ≥85% at 230 VAC
- Low cost, low component count and small printed circuit board footprint solution
  - No current sensing required
  - Frequency jitter for smaller, lower cost EMI filter components
- Integrated protection and reliability features
  - Output open circuit / output short-circuit protected with auto-recovery
  - Line input overvoltage shutdown extends voltage withstand during line faults.
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
  - No damage during brown-out or brown-in conditions
- Meets IEC 61000-4-5 ring wave, IEC 61000-3-2 Class C harmonics and EN55015 B conducted EMI

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PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a power-factor corrected dimmable LED driver designed to drive an LED string of 18 V at a current of 0.38 A (both nominal) from an input voltage range of 90 VAC to 265 VAC. The LED driver utilizes the LNK403EG from Power Integrations. The design specifically eliminates electrolytic capacitors which limit operating life, especially when operated at high temperature.

LinkSwitch-PH ICs allow the implementation of cost effective and low component count LED drivers which both meet power factor and harmonics limits but also offer enhanced end user experience. This includes ultra-wide dimming range, flicker-free operation (even with low cost with AC line TRIAC dimmers) and fast, clean turn on.

The topology used is an isolated flyback operating in continuous conduction mode. Output current regulation is sensed entirely from the primary side eliminating the need for secondary side feedback components. No external current sensing is required on the primary side either as this is performed inside the IC further reducing components and losses. The internal controller adjusts the MOSFET duty cycle to maintain a sinusoidal input current and therefore high power factor and low harmonic currents.

The LNK403EG also provides a sophisticated range of protection features including auto-restart for open control loop and output short-circuit conditions. Line overvoltage provides extended line fault and surge withstand, output overvoltage protects the supply should the load be disconnect and accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

In any LED luminaire the driver determines many of the performance attributes experienced by the end customer (user) including start-up time, dimming, flicker and unit to unit consistency. For this design a focus was given to compatibility with as wider range of dimmers and as large of a dimming range as possible, at both 115 VAC and 230 VAC. However simplification of the design is possible for single input voltage operations, non-dimming or operation with a limited range of (higher quality) dimmers.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.

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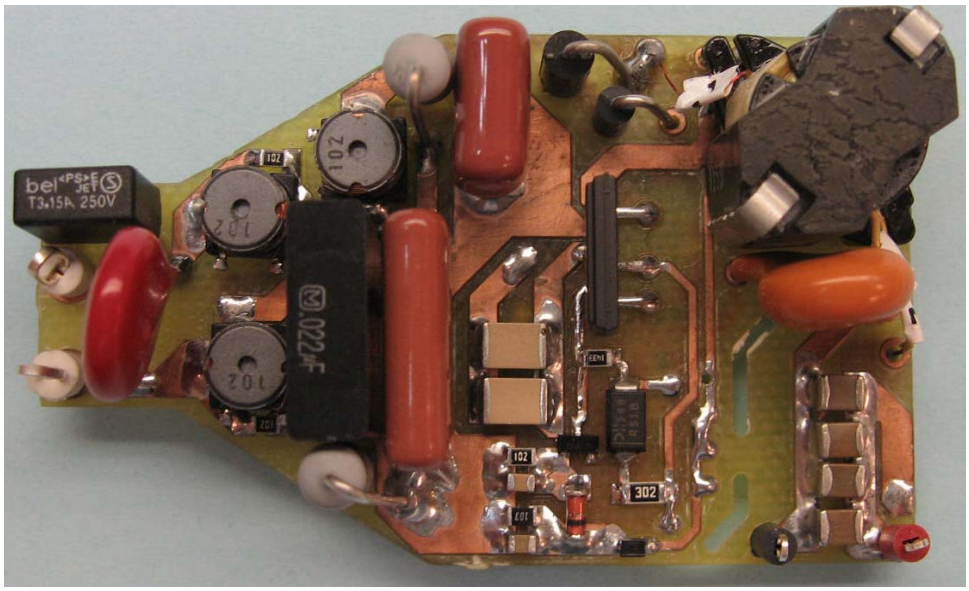

Figure 1 – Populated Circuit Board Photograph (Top View).
PCB Outline Designed to Fit Inside PAR20 Enclosure.

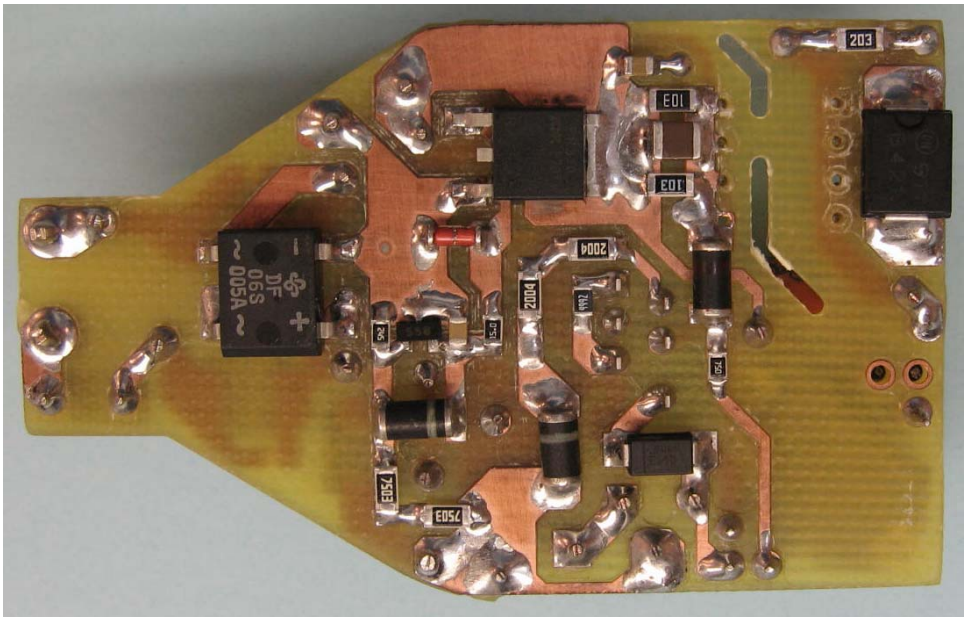

Figure 2 – Populated Circuit Board Photograph (Bottom View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage [a]	V_{IN}	90	115	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	15	18	21	V	
Output Current [a]	I_{OUT}		0.38		A	V_{OUT} = 21, V_{IN} = 115 VAC, 25°C
Total Output Power						
Continuous Output Power	P_{OUT}		7		W	
Efficiency						
Full Load	η	80			%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		Meets CISPR 15B / EN55015B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	IEC 61000-4-5 , 200 A
Common mode (L1/L2-PE)						
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 115/230 VAC
Harmonics		EN 61000-3-2 Class D				
Ambient Temperature [b]	T_{AMB}		40		°C	Free convection, sea level

Notes:

[a] When configured for phase controlled (TRIAC) dimming, in order to give the widest dimming range, the output current for a LinkSwitch-PH design varies with line voltage. Therefore the output current specification is defined at a single line voltage only. For this design a line voltage of 115 VAC was selected. At higher line voltages the output current will increase and reduce with lower line voltages. The typical output current variation is +30% for a +200% increase in line voltage. A single resistor value change can be used to center the nominal output current for a given nominal line voltage. See Table 1 for the feedback resistor value vs. nominal line voltage.

[b] Maximum ambient temperature specification may be increased by adding a small heat sink to the LinkSwitch-PH device.

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3 Schematic

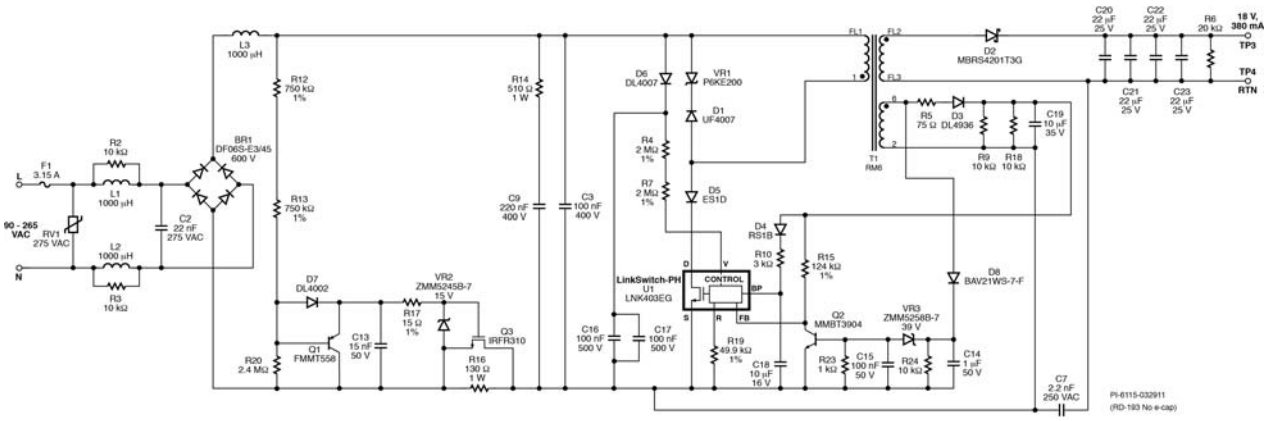

Figure 3 – Schematic.

Note: The power rating of R14 and R16 need to be double at 230 VAC input.

4 Circuit Description

The LinkSwitch-PH device is a controller and integrated 725 V MOSFET intended for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage continuous conduction mode flyback topology and provides a primary side regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 fuses the input and BR1 rectifies the AC line voltage. Inductor L1-L3, C2, R2, and R3 form the EMI filter and together with C7 (Y1 safety) capacitor allow the design to meet EN55015B conducted EMI limits. Capacitor C3 provides a low impedance path for the primary switching current, a low value of capacitance is necessary to maintain a power factor of greater than 0.9.

4.2 LinkSwitch-PH Primary

Diode D6 and high-voltage SMD ceramic capacitors C16 and C17 detect the peak AC line voltage. This voltage is converted to a current into the VOLTAGE MONITOR (V) pin via R4 and R7. This current is also used by the device to set the input over/undervoltage protection thresholds. The V pin current and the FEEDBACK (FB) pin current are used internally to control the average output LED current. TRIAC phase-angle dimming applications require 49.9 kΩ resistors on the REFERENCE (R) pin (R19) and 4 MΩ on the V pin (R4+R7) to provide a linear relationship between input voltage and the output current, allowing dimming with standard TRIAC dimmers. Resistor R19 also sets the internal references to select the line undervoltage threshold. In TRIAC dimming configuration (as shown here) the line undervoltage threshold is lowered to allow start-up at smaller TRIAC conduction angles.

Diode D1 and VR1 clamp the drain voltage to below the BV_{DSS} rating (725 V) of the internal power MOSFET in U1. Diode D5 is necessary to prevent reverse current from flowing through the LinkSwitch-PH device (the result of the minimal input capacitance).

4.3 Bias Supply and Output Overvoltage Sensing

Diode D3, C19, R5, R9 and R18 form the primary bias supply. This supplies the IC operating current into the BYPASS (BP) pin through D4 and R10 during normal operation. Resistor R5 provides filtering to improve output regulation while R9 and R10 act as a minimum load; this improves dimming range by causing the bias voltage to reduce as the output current falls.

Capacitor C18 is the supply decoupling for the LinkSwitch-PH. During start-up C18 is charged to ~6 V from an internal high-voltage current source tied to the device DRAIN (D) pin. Once charged the energy stored in C18 is used to run the device until the output and bias winding voltage rise.

A disconnected load / overvoltage shutdown function is provided by D8, C14, R24, VR3, C15, R23 and Q2. A second bias winding output voltage is used to eliminate the delay

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introduced by the larger value of C19 compared to C14. Should the output LED load be disconnected, the output voltage and therefore the bias winding voltage across C14 will rise. Once this exceeds the voltage rating of VR3 plus the VBE of Q2 then Q2 is bias on which pulls the FB pin down. Once the current into the FB pin of U1 falls the device enters auto-restart, thereby limiting the output voltage. Resistor R24, C15 and R23 all provide filtering.

4.4 Output Feedback

A current proportional to the output voltage from the primary bias winding is fed into the FB pin through R15. This information together with the line input voltage and the drain current are used to maintain a constant output current.

4.5 Output Rectification and Filtering

Diode D2 rectifies the secondary winding while ceramic capacitors C20, C21, C22 and C23 filter the output. A Schottky diode was selected for high efficiency.

4.6 TRIAC Phase Dimming Interface Circuitry

Components R12, R13, R20, R17, D7, Q1, C13, VR2, and Q3 in conjunction with R16 reduce the inrush current when the TRIAC dimmer turns on. This prevents the line inductance from peak charging input capacitance above the line voltage, causing flicker. During each AC cycle the input current flows through R16 for the first 0.6 ms at 115 VAC (0.3 ms at 230 VAC) of TRIAC conduction. After approximately 0.6 ms, Q3 turns on and shorts R16. This circuit allows the value of R16 to be large enough to limit the initial inrush current but keeps the power dissipation on R16 low for high-efficiency. Resistor R12, R13, R20 and C13 provide a 0.6 ms delay after the TRIAC conducts. Transistor Q1 discharges C13 when the TRIAC is not conducting. Zener diode VR2 clamps the gate voltage of Q3 to 15 V.

Capacitor C9 and R14 form a passive bleeder circuit with keep the AC input current above the holding current threshold for the TRIAC to prevent multiple firings on each AC cycle causing flicker and shimmer.

5 PCB Layout

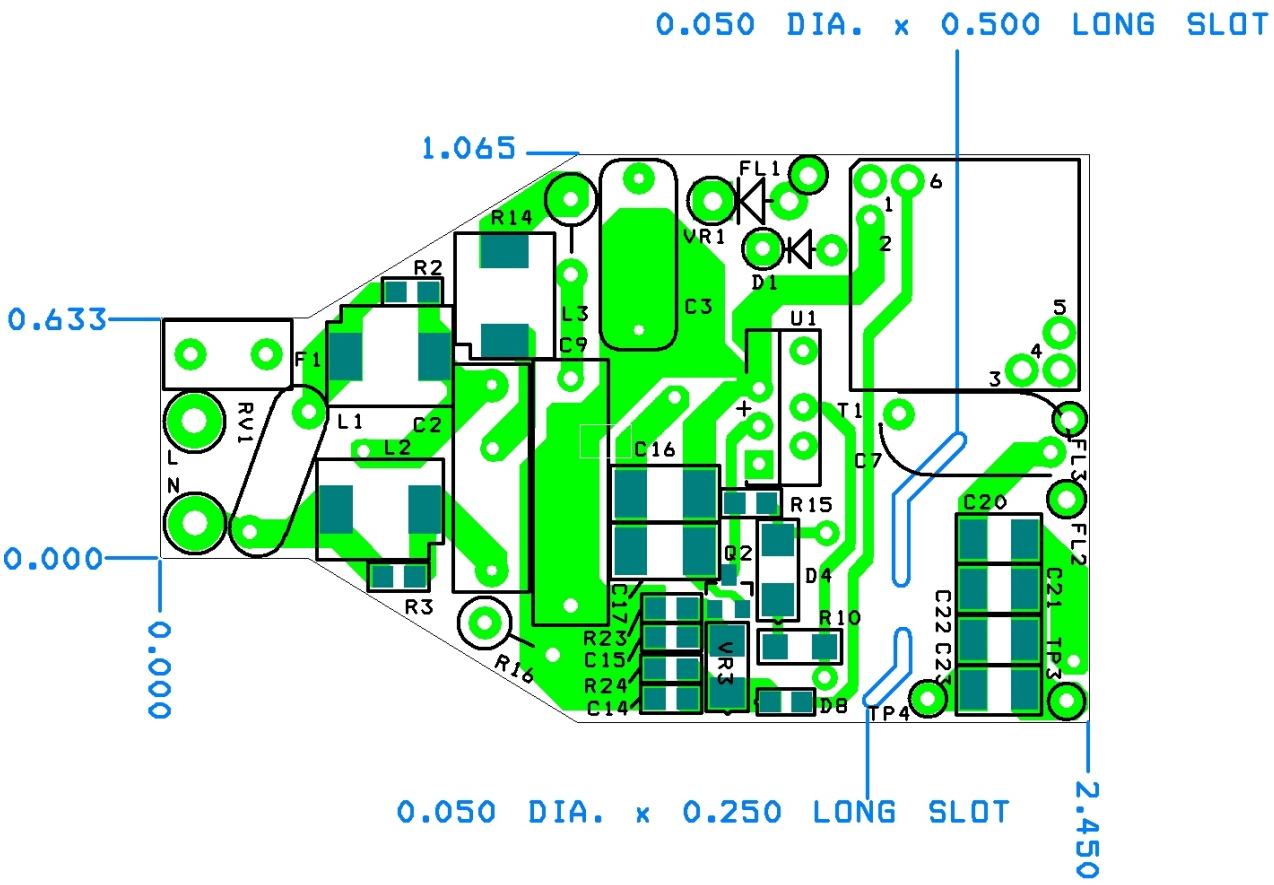

Figure 4 – Printed Circuit Layout Top. (Designed to Fit Inside PAR20 Lamp Form Factor).

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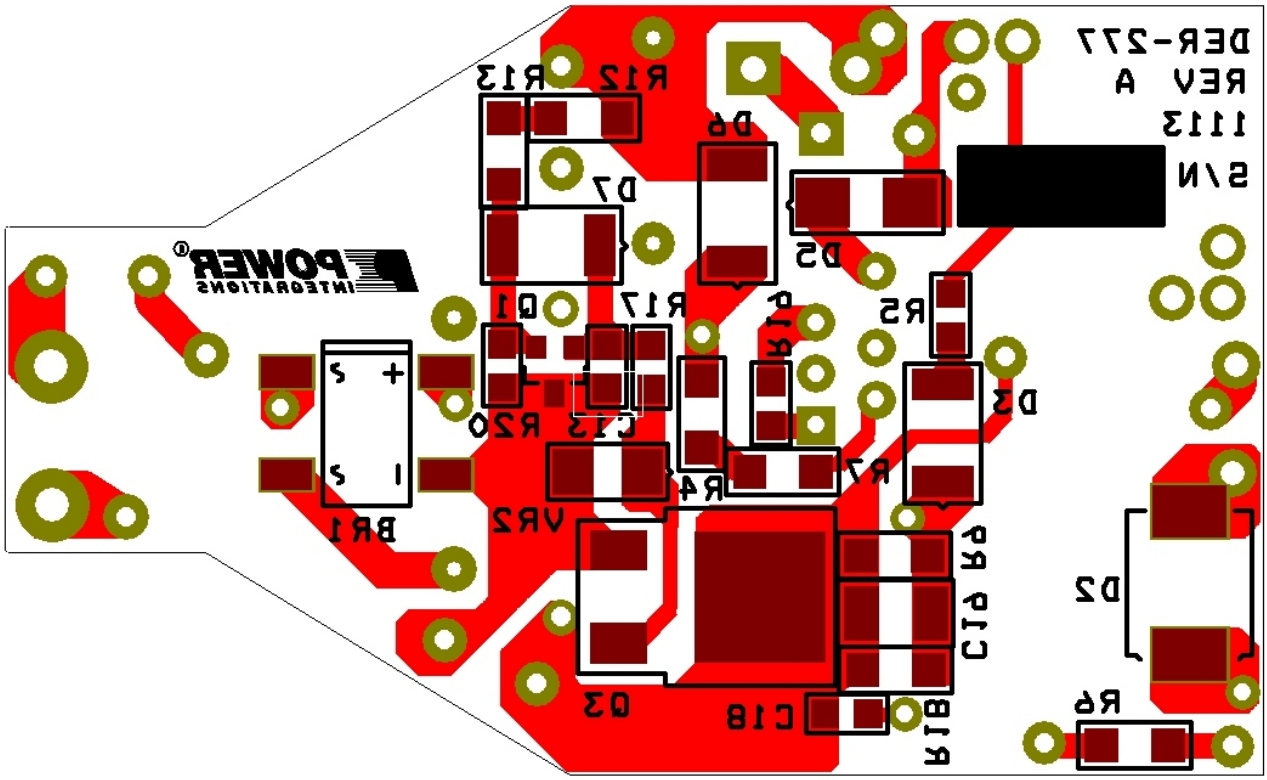

Figure 5 – Printed Circuit Layout Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, SMD, DFS	DF06S-E3/45	Vishay
2	1	C2	22 nF, 275 VAC, Film, X2	ECQ-U2A223ML	Panasonic
3	1	C3	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
4	1	C7	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
5	1	C9	220 nF, 400 V, Film	ECQ-E4224KF	Panasonic
6	1	C13	15 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H153K	Panasonic
7	1	C14	1 μF, 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX
8	1	C15	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Panasonic
9	2	C16 C17	100 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y104KXEAT	Vishay
10	1	C18	10 μF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
11	1	C19	10 μF, 35 V, Ceramic,Y5V, 1210	GMK325F106ZH-T	Taiyo Yuden
12	4	C20 C21 C22 C23	22 μF, 25 V, Ceramic, X5R, 1210	ECJ-4YB1E226M	Panasonic
13	1	D1	1000 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4007-E3	Vishay
14	1	D2	200 V, 4 A, Schottky, SMC, DO-214AB	MBRS4201T3G	On Semi
15	1	D3	400V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4936-13-F	Diodes, Inc
16	1	D4	100 V, 1 A, Fast Recovery, 150 ns, SMA	RS1B-13-F	Diodes, Inc
17	1	D5	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D	Vishay
18	1	D6	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc
19	1	D7	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002-13-F	Diodes, Inc
20	1	D8	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc
21	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
22	3	FL1 FL2 FL3	PCB Terminal Hole, 22 AWG	N/A	N/A
23	2	L N	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
24	3	L1 L2 L3	1000 μH, 0.14 A	SLF7045T-102MR14-PF	TDK
25	1	Q1	PNP, 400 V 150 MA, SOT-23	FMMT558TA	Zetex
26	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semi
27	1	Q3	400 V, 1.7 A, 3.6 Ω, N-Channel, DPAK	IRFR310TRPBF	Vishay
28	3	R2 R3 R24	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
29	2	R4 R7	2.00 M Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
30	1	R5	75 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ750V	Panasonic
31	1	R6	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
32	2	R9 R18	10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
33	1	R10	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
34	2	R12 R13	750 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7503V	Panasonic
35	1	R14	510 Ω, 5%, 2 W, Metal Oxide	RSF200JB-510R	Yageo
36	1	R15	124 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1243V	Panasonic
37	1	R16	130 Ω, 5%, 1 W, Metal Oxide	RSF100JB-130R	Yageo
38	1	R17	15 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF15R0V	Panasonic
39	1	R19	49.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4992V	Panasonic
40	1	R20	2.4 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ245V	Panasonic
41	1	R23	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
42	1	RV1	275 V, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
43	1	T1	Bobbin, RM6, Vertical, 6 pins	B65808-N1006-D1	Epcos
44	1	TP3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
45	1	TP4	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
46	1	U1	LinkSwitch, eSIP™	LNK403EG	Power Integrations
47	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	On Semi
48	1	VR2	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes, Inc
49	1	VR3	36 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5258B-7	Diodes, Inc

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7 Transformer Specification

7.1 Electrical Diagram

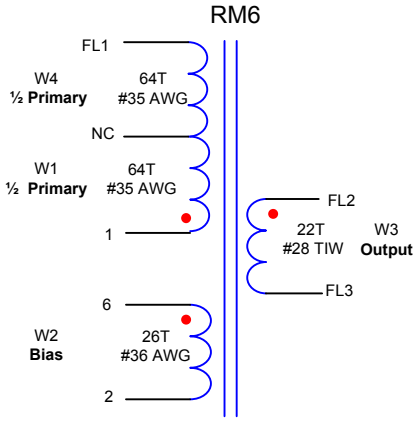

Figure 6 – Transformer Electrical Diagram.

Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 6, FL1 to FL2, FL3	3000 VAC
Primary Inductance	Pins 1-FL1, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	2.45 mH ±10%
Resonant Frequency	Pins 1-FL1, all other windings open	750 kHz (Min.)
Primary Leakage Inductance	Pins 1-FL1 with FL2-FL3 shorted, measured at 100 kHz, 0.4 V_{RMS}	35 μH ±10%

7.2 Materials

Item	Description
[1]	Core: PC95RM6 from TDK or equivalent, ALG = 149.5 nH/n^2
[2]	Bobbin: 6 pin vertical, B-RM6-V-6P from Epcos, or equivalent
[3]	Magnet Wire: #35 AWG.
[4]	Magnet Wire: #36 AWG
[5]	Magnet Wire: #28 AWG T.I.W.
[6]	Tape: 3M 1298 Polyester Film, 7 mm wide.
[7]	Mounting clip, CLI/P-RM6, and varnish.

7.3 Transformer Build Diagram

Pins Side

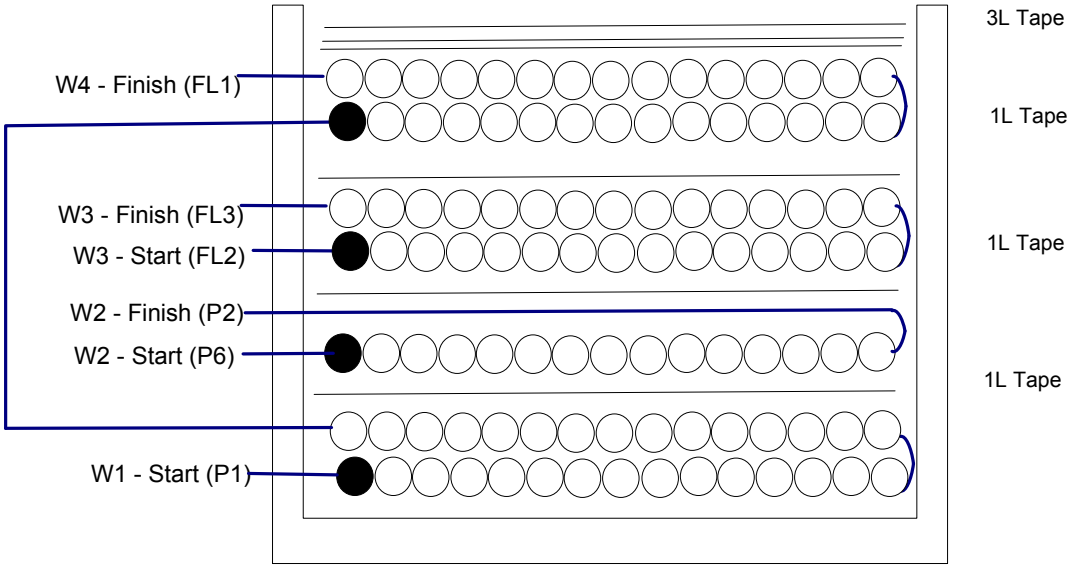

Figure 7 – Transformer Build Diagram.

7.4 Transformer Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WD 1	Start at pin 1, wind 64 turns of #35 AWG item [3] from left to right two layers. At the last turn exit the same slot, leave enough length wire floating to wind next 64 turns in WD4.
Insulation	Apply one layer of tape [6] for insulation.
WD 2	Start at pin 6, wind 26 turns of #36 AWG [4] wire from left to right. Finish at pin 2.
Insulation	Apple one layer of tape [6] for insulation.
WD 3	Leave about 1” of wire item [5], use small tape to mark as FL2, enter into slot of secondary side of bobbin, wind 22 turns in two layers. At the last turn exit the same slot, leave about 1”, and mark as FL3.
Insulation	Apple one layer of tape [6] for insulation.
WD 4	Continue to wind with floating wire, 64 turns of #35 AWG from left to right two layers. Leave 1” and mark as FL1
Insulation	Apply three layers of tape [6] for insulation.
Final Assembly	Cut FL1, FL2, FL3 wire length to 0.75”. Grind core. Assemble core and varnish using item [7].

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8 Transformer Design Spreadsheet

LinkSwitch-PH	INPUT	OUTPUT	UNIT	LinkSwitch-PH_042910: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
Dimming required	YES	YES		!!! Info. When configured for dimming, best output current line regulation is achieved over a single input voltage range.
VACMIN		90	V	Minimum AC Input Voltage
VACMAX		132	V	Maximum AC input voltage
fL		50	Hz	AC Mains Frequency
VO	18		V	Typical output voltage of LED string at full load
VO_MAX		19.80	V	Maximum expected LED string Voltage.
VO_MIN		16.20	V	Minimum expected LED string Voltage.
V_OVP		21.78	V	Overvoltage protection setpoint
IO	0.38			Typical full load LED current
PO		6.8	W	Output Power
n		0.8		Estimated efficiency of operation
VB	21	21	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES				
LinkSwitch-PH	LNK403		Universal	115 Doubled/230V
Chosen Device		Power Out	12.5W	12.5W
Current Limit Mode	Full	Full		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN		0.81	A	Minimum current limit
ILIMITMAX		0.92	A	Maximum current limit
fS		66000	Hz	Switching Frequency
fSmin		62000	Hz	Minimum Switching Frequency
fSmax		70000	Hz	Maximum Switching Frequency
IV		39.9	uA	V pin current
RV		4	M-ohms	Upper V pin resistor
RV2		1E+012	M-ohms	Lower V pin resistor
IFB		137.3	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1		131.1	k-ohms	FB pin resistor
VDS		10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.5		V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.7		V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters				
KP	0.99	0.99		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP		2460	uH	Primary Inductance
VOR	108	108	V	Reflected Output Voltage.
Expected IO (average)		0.39	A	Expected Average Output Current
KP_VACMAX		1.04		Expected ripple current ratio at VACMAX
TON_MIN		3.82	us	Minimum on time at maximum AC input voltage
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	RM6	RM6		
Bobbin			P/N:	#N/A
AE	0.36	0.36	cm^2	Core Effective Cross Sectional Area
LE	2.86	2.86	cm	Core Effective Path Length
AL	2280	2280	nH/T^2	Ungapped Core Effective Inductance

BW	6.4	6.4	mm	Bobbin Physical Winding Width
M		0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4	4		Number of Primary Layers
NS	22	22		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN		127	V	Peak input voltage at VACMIN
VMAX		187	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.48		Minimum duty cycle at peak of VACMIN
IAVG		0.39	A	Average Primary Current
IP		0.44	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS		0.14	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP		2460	uH	Primary Inductance
NP		128		Primary Winding Number of Turns
NB		26		Bias Winding Number of Turns
ALG		149	nH/T^2	Gapped Core Effective Inductance
BM		2330	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP		2820	Gauss	Peak Flux Density (BP<3700)
BAC		1153	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1441		Relative Permeability of Ungapped Core
LG		0.28	mm	Gap Length (Lg > 0.1 mm)
BWE		25.6	mm	Effective Bobbin Width
OD		0.20	mm	Maximum Primary Wire Diameter including insulation
INS		0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.16	mm	Bare conductor diameter
AWG		35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		32	Cmils	Bare conductor effective area in circular mils
CMA		224	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		2.56	A	Peak Secondary Current
ISRMS		0.82	A	Secondary RMS Current
IRIPPLE		0.72	A	Output Capacitor RMS Ripple Current
CMS		164	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.36	mm	Secondary Minimum Bare Conductor Diameter
ODS		0.29	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS				
VDRAIN		408	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS		54	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB		63	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)				
V pin Resistor Fine Tuning				
RV1		4.00	M-ohms	Upper V Pin Resistor Value
RV2		1.00E+12	M-ohms	Lower V Pin Resistor Value

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VAC1		115.0	V	Test Input Voltage Condition1
VAC2		230.0	V	Test Input Voltage Condition2
IO_VAC1		0.38	A	Measured Output Current at VAC1
IO_VAC2		0.38	A	Measured Output Current at VAC2
RV1 (new)		4.00	M-ohms	New RV1
RV2 (new)		20911.63	M-ohms	New RV2
V_OV		319.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV		66.3	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning				
RFB1		131	k-ohms	Upper FB Pin Resistor Value
RFB2		1.00E+12	k-ohms	Lower FB Pin Resistor Value
VB1		18.9	V	Test Bias Voltage Condition1
VB2		23.1	V	Test Bias Voltage Condition2
IO1		0.38	A	Measured Output Current at Vb1
IO2		0.38	A	Measured Output Current at Vb2
RFB1 (new)		131.1	k-ohms	New RFB1
RFB2 (new)		1.00E+12	k-ohms	New RFB2

9 Performance Data

All measurements performed at room temperature.

9.1 Efficiency vs. Line and Output (LED String) Voltage

9.1.1 18 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	8.2	18.50	335	6.60	**80**	
60	100	8.55	18.60	352	6.93	**81**	
60	115	9.06	18.70	376	7.45	**82**	**0.98**
60	130	9.56	18.70	401	7.98	**83**	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	195	11.59	19.30	488	9.87	**85**	
50	215	12.09	19.40	506	10.30	**85**	
50	230	12.4	19.40	519	10.60	**85**	**0.92**
50	245	12.7	19.40	530	10.85	**85**	
50	265	13.16	19.50	545	11.20	**85**	
50	195	11.59	19.30	488	9.87	**85**	

9.1.2 15 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	6.9	15.50	339	5.57	**81**	
60	100	7.2	15.60	358	5.87	**82**	
60	115	7.65	15.70	382	6.32	**83**	**0.98**
60	130	8.1	15.80	405	6.75	**83**	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	195	9.66	16.20	484	8.24	**85**	
50	215	10.1	16.20	502	8.60	**85**	
50	230	10.4	16.30	515	8.84	**85**	**0.89**
50	245	10.7	16.40	528	9.20	**86**	
50	265	11.1	16.50	543	9.40	**85**	
50	195	9.66	16.20	484	8.24	**85**	

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9.1.3 21 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	9.67	21.40	336	7.66	**79**	
60	100	10	21.50	352	8.05	**81**	
60	115	10.5	21.70	375	8.60	**82**	**0.97**
60	130	11.1	21.80	398	9.15	**82**	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	195	13.5	22.30	487	11.40	**84**	
50	215	14.1	22.40	507	11.90	**84**	
50	230	14.5	22.40	519	12.30	**85**	**0.93**
50	245	14.8	22.50	531	12.50	**84**	
50	265	15.3	22.60	545	12.90	**84**	
50	195	13.5	22.30	487	11.40	**84**	

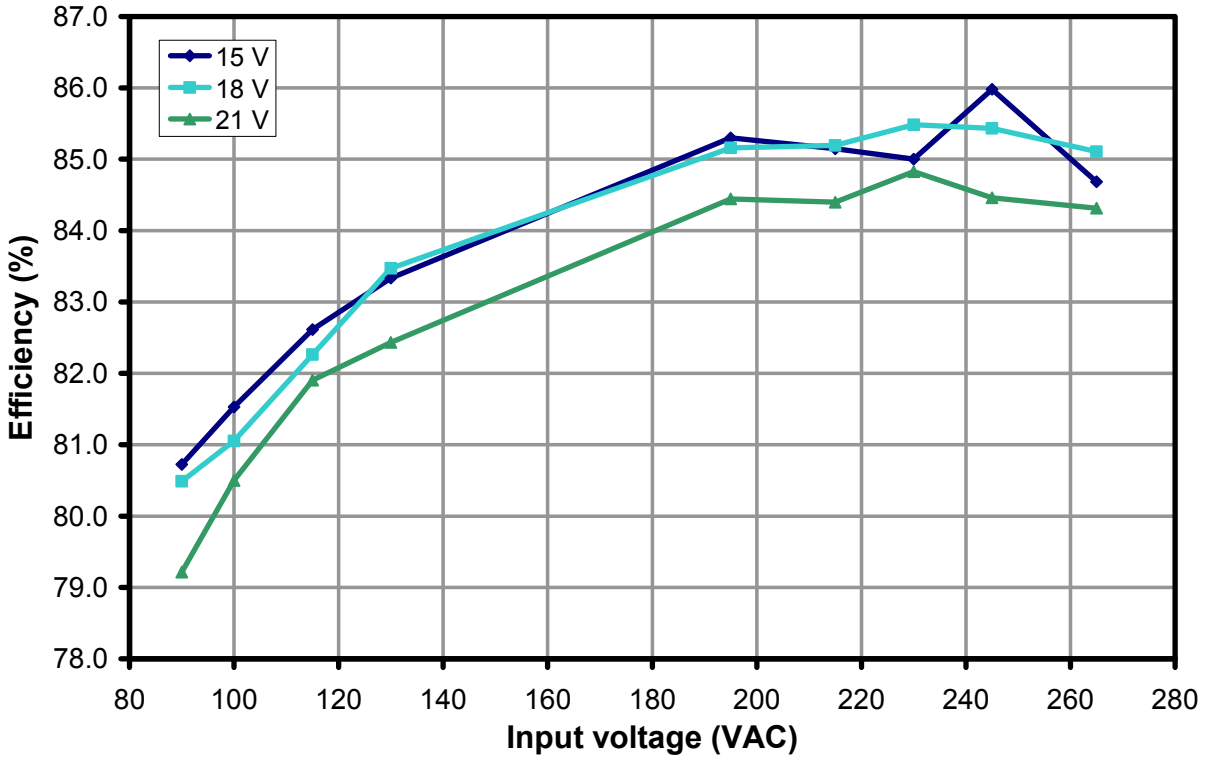

Figure 8 – Efficiency vs. Input Voltage, Room Temperature.

9.2 Regulation

9.2.1 Output Voltage and Line

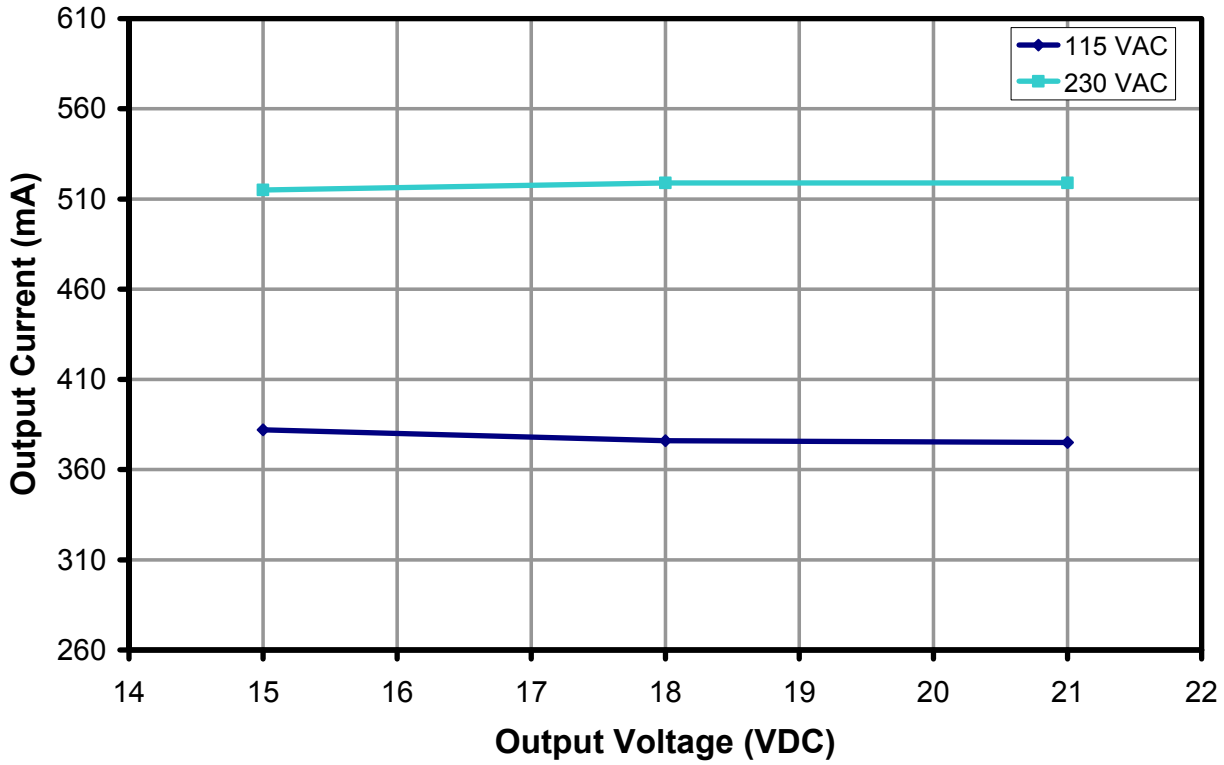

Figure 9 – Voltage and Line Regulation, Room Temperature.

The line regulation result shown above is typical for a design where the phase angle dimming mode of U1 is selected (to provide a very wide dimming range). For a given line voltage the output current can be centered by changing the value of the FEEDBACK pin resistor (R15). The table below shows the resistor values to adjust the mean output current at specific input voltages,

Line Voltage (VAC)	Value of R15 (kΩ)
100	118
115	127
230	174

Table 1 – Feedback Resistor Value to Center Output Current at Different Nominal Line Voltages.

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9.2.2 Line Regulation

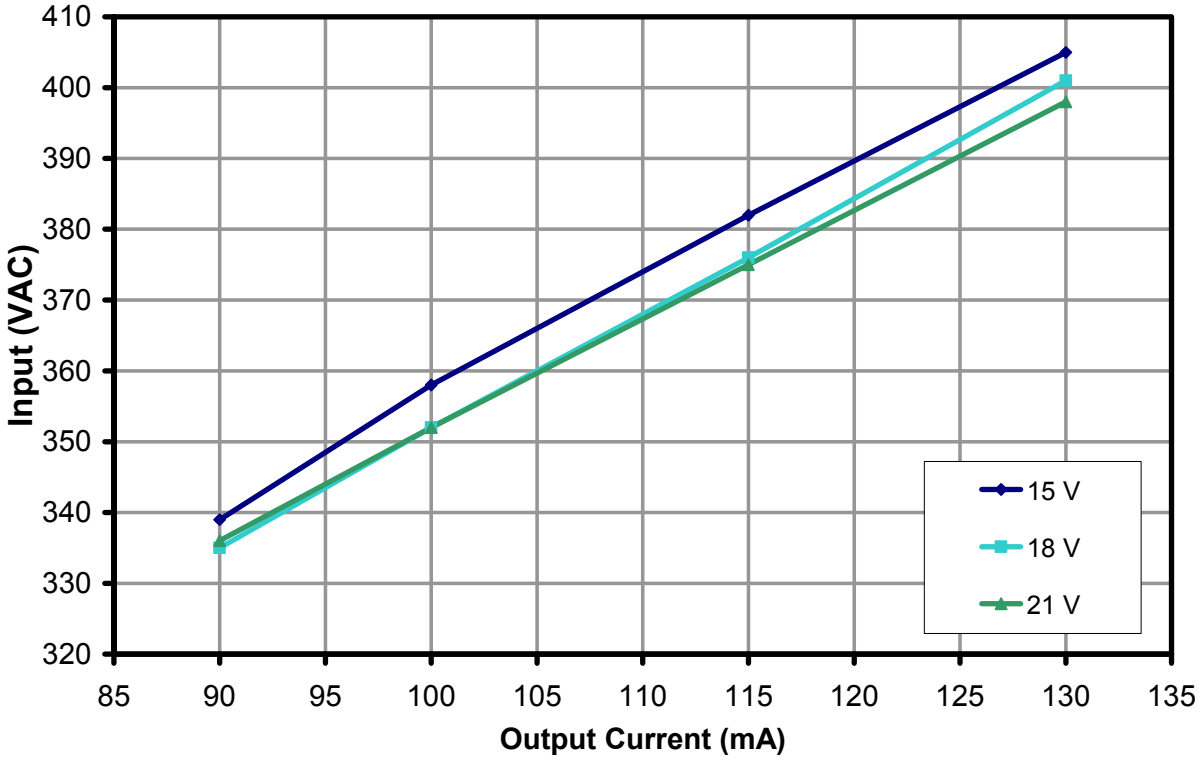

Figure 10 – Low-Line Regulation, Room Temperature, Full Load.

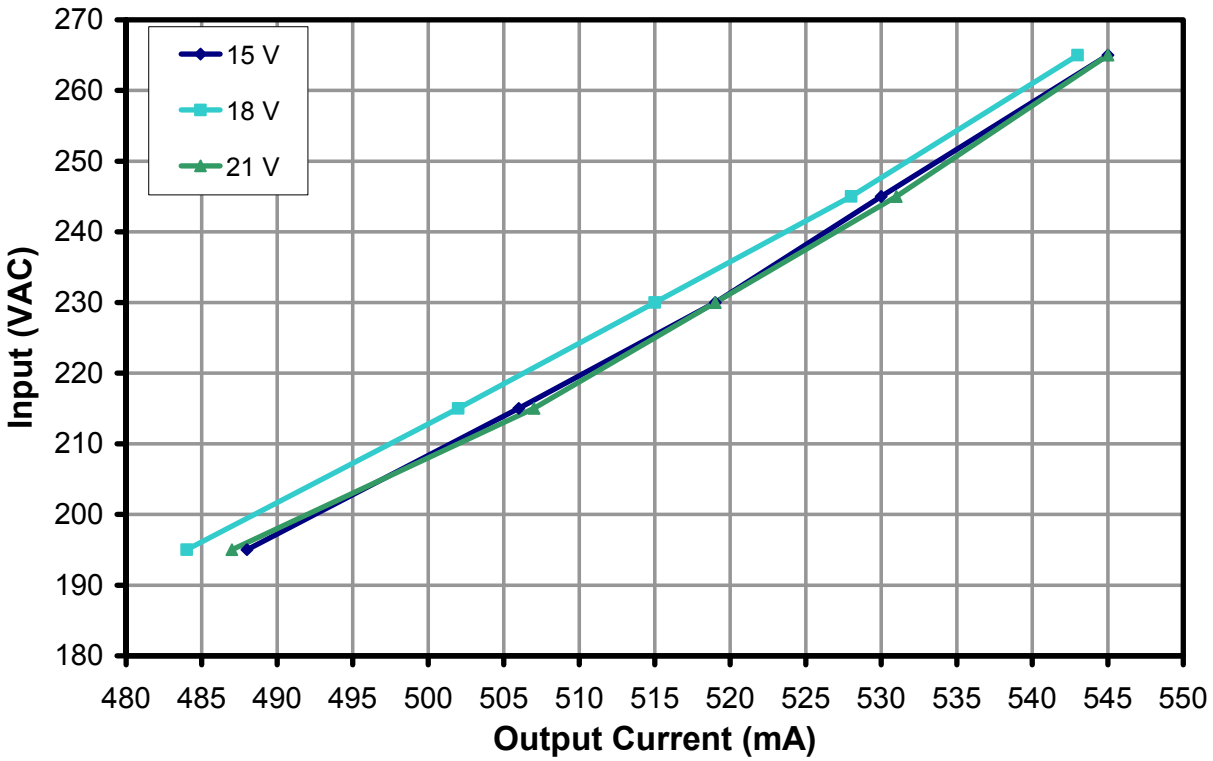

Figure 11 – High-Line Regulation, Room Temperature, Full Load.

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10 Thermal Performance

Images captured after running for 30 minutes at room temperature (25 °C), full load (18 V, 0.38 A). This indicates a LinkSwitch-PH (U1) operating temperature of ~80 °C at an external board ambient of 40 °C. As U1 is the highest temperature component on the board it provides effective thermal protection for the entire system via its internal thermal shutdown. The addition of a small heat sink (equal to the width of board) to U1 reduces the operating temperature by ~25 °C.

10.1 V_{IN} = 115 VAC

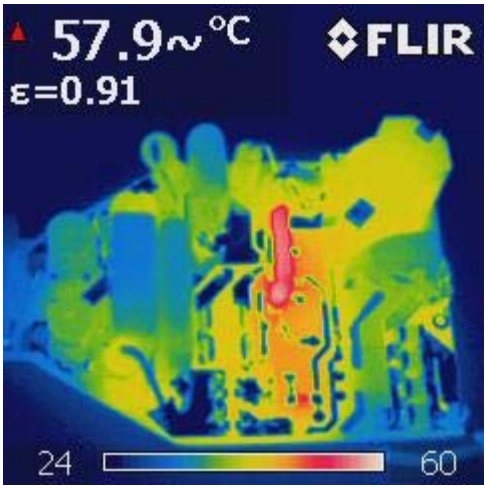

Figure 12 – Top Side.

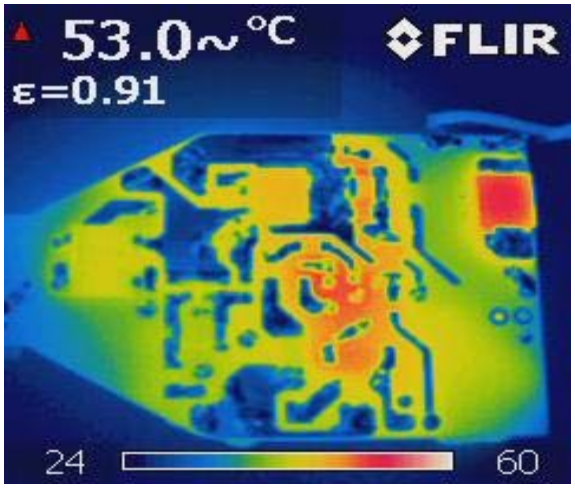

Figure 13 – Bottom Side.

10.2 V_{IN} = 230 VAC

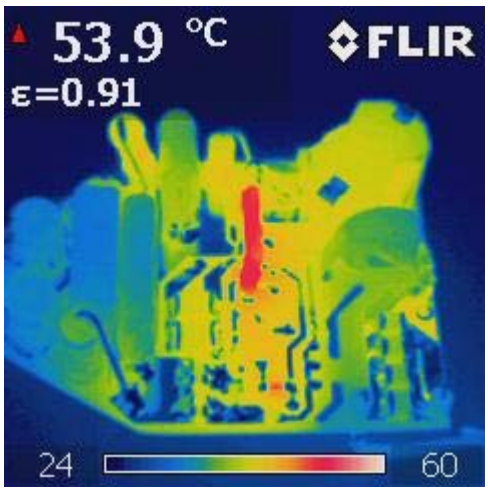

Figure 14 – Top Side.

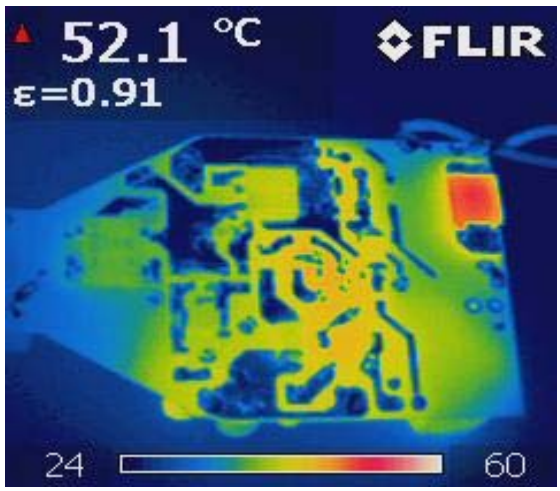

Figure 15 – Bottom Side.

11 Harmonic Data

The design passes Class C requirement.

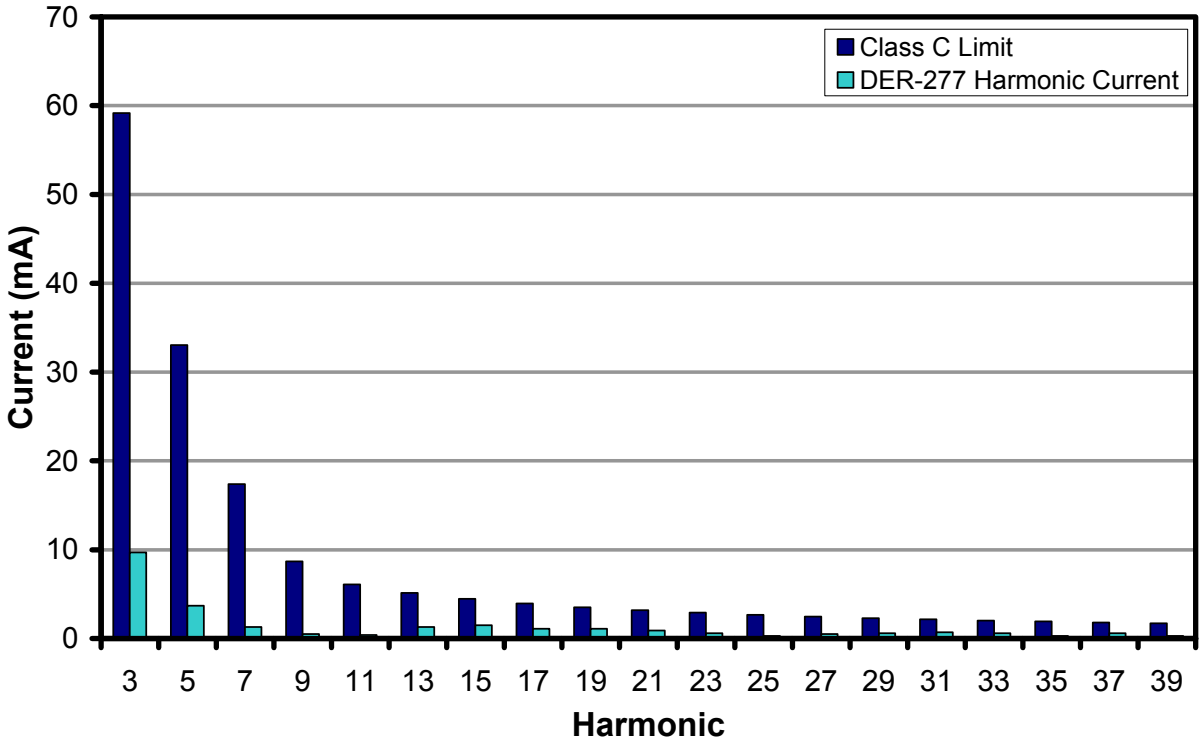

Figure 16 – 115 VAC Harmonic, Room Temperature, Full Load.

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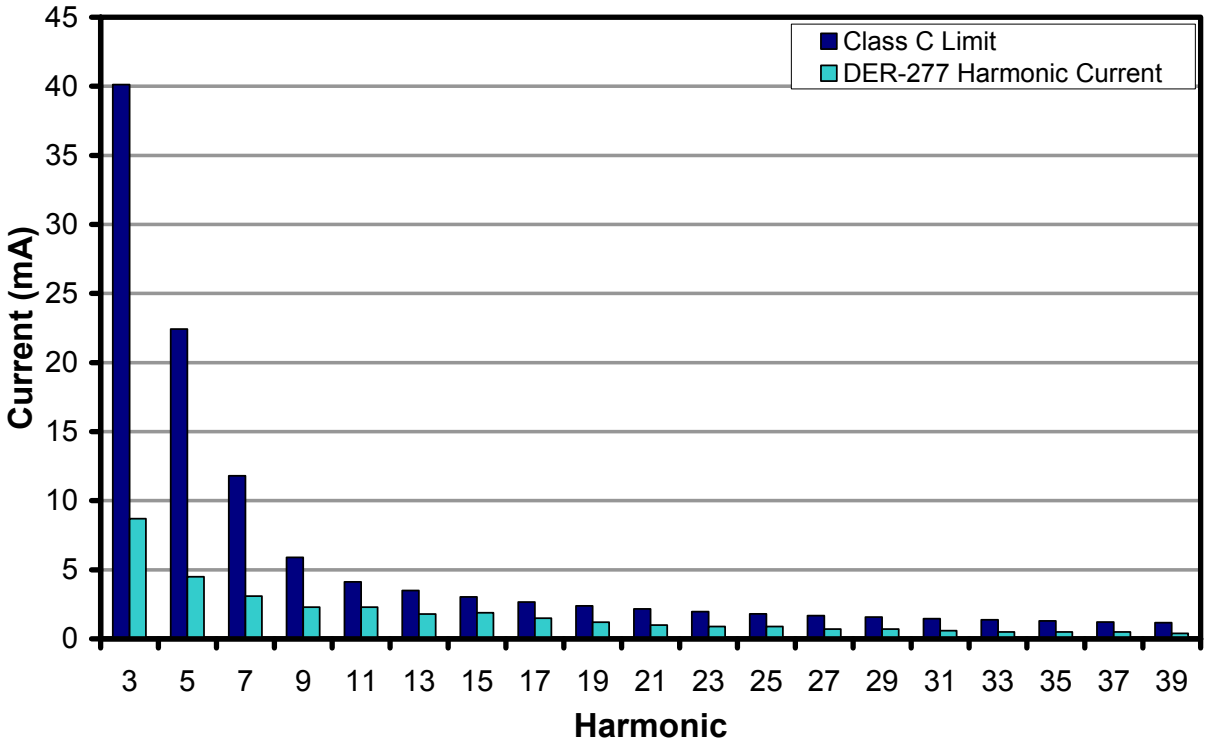

Figure 17 – 230 VAC Harmonic, Room Temperature, Full Load.

V_{IN} = 115 VAC		
THD (%)	**Limit (%)**	**Margin (%)**
14	**33**	**19**
V_{IN} = 230 VAC		
THD (%)	**Limit (%)**	**Margin (%)**
20	**33**	**13**

12 Waveforms

12.1 Input Line Voltage and Current

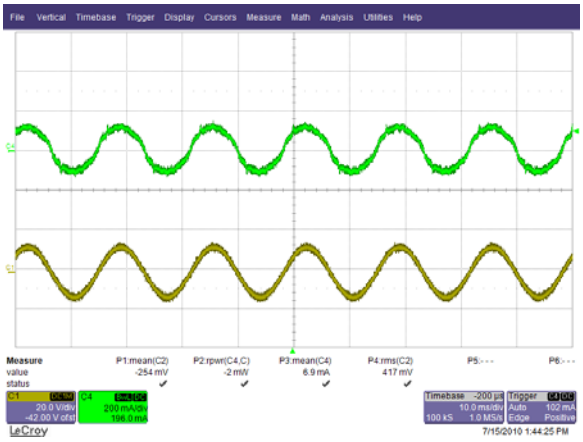

Figure 18 – 90 VAC, Full Load.
Upper: I_{IN}, 0.2 A / div.
Lower: V_{IN}, 200 V, 10 ms / div.

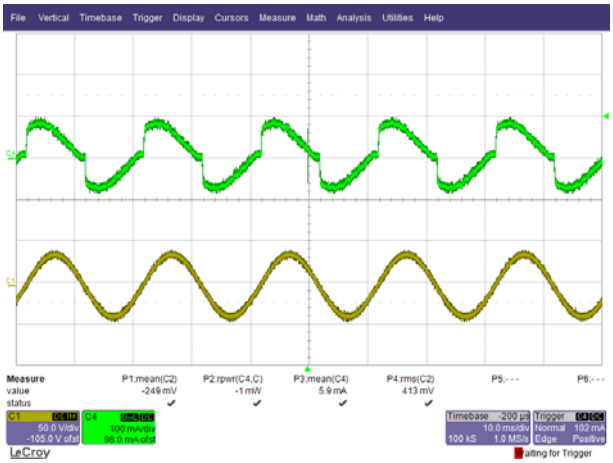

Figure 19 – 265 VAC, Full Load.
Upper: I_{IN}, 0.1 A / div.
Lower: V_{IN}, 500 V / div., 10 ms / div.

12.2 Drain Voltage and Current

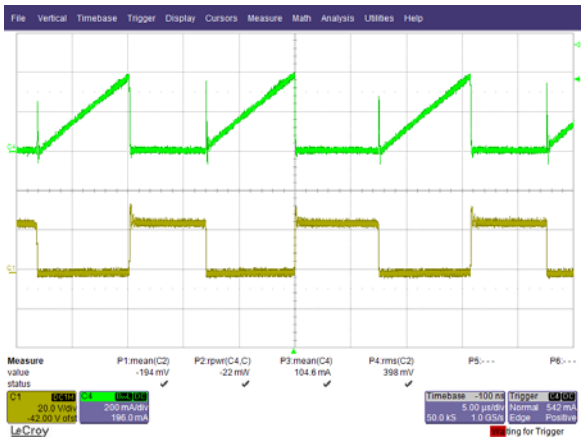

Figure 20 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 200 V, 5 µs / div.

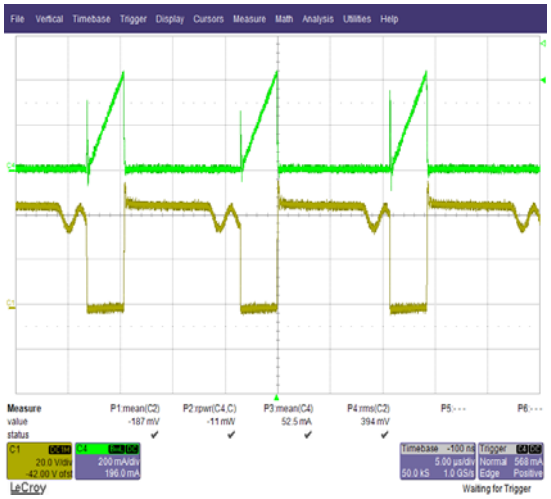

Figure 21 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 200 V / div., 5 µs / div.

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12.3 Output Voltage and Ripple Current

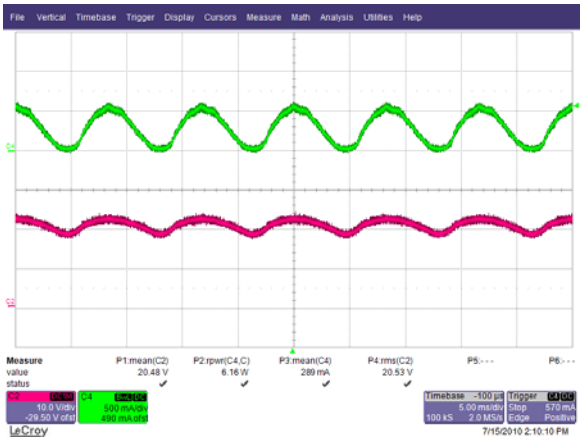

Figure 22 – 90 VAC, Full Load.
Upper: I_{RIPPLE}, 0.5 A / div.
Lower: V_{OUTPUT} 10 V, 5 ms / div.

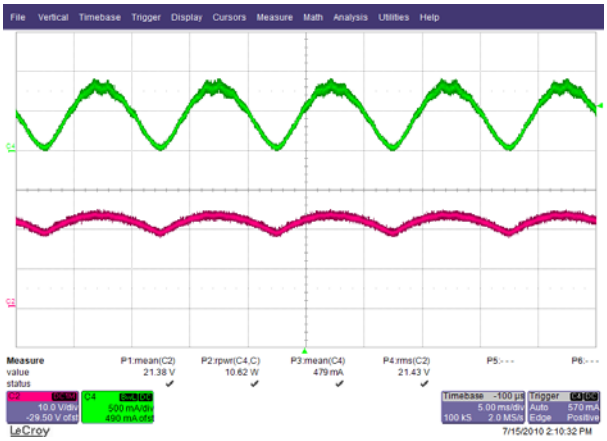

Figure 23 – 265 VAC, Full Load.
Upper: I_{RIPPLE}, 0.5 A / div.
Lower: V_{OUTPUT} 10 V, 5 ms / div.

12.4 Drain Voltage and Current Start-up Profile

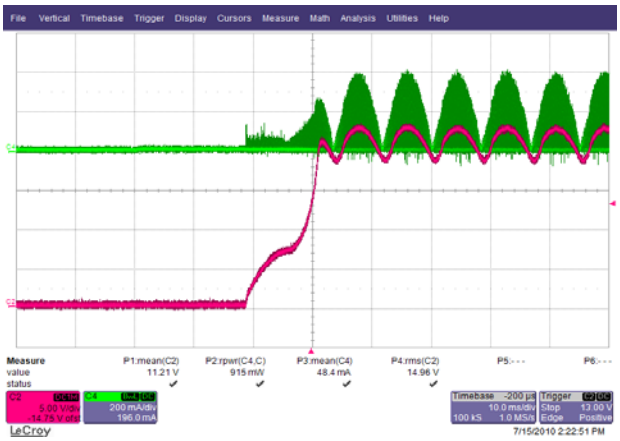

Figure 24 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: $V_{OUTPUT,}$ 5 V, 10 ms / div.

Figure 25 – 265 VAC, Full Load.
Upper: I_{RIPPLE}, 0.2 A / div.
Lower: $V_{OUTPUT,}$ 5 V, 10 ms / div.

12.5 Output Current and Drain Voltage at Shorted Output

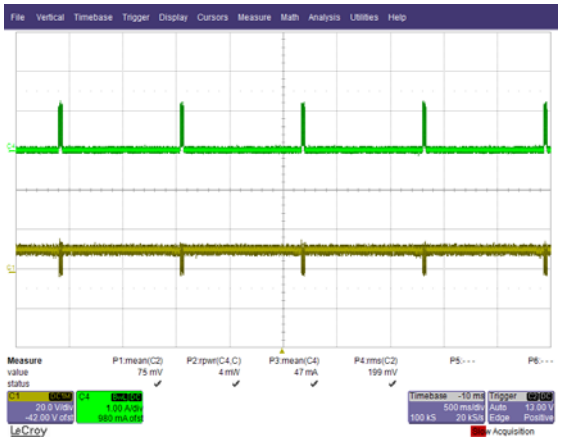

Figure 26 – 90 VAC, Full Load.
Upper: I_{OUTPUT}, 2 A / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

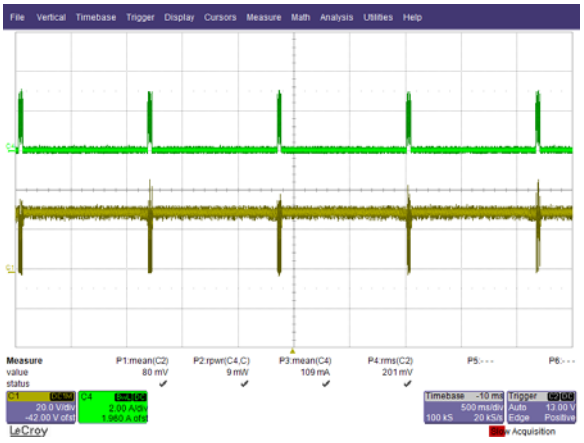

Figure 27 – 265 VAC, Full Load.
Upper: I_{OUTPUT}, 2 A / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

12.6 Open Load Output Voltage

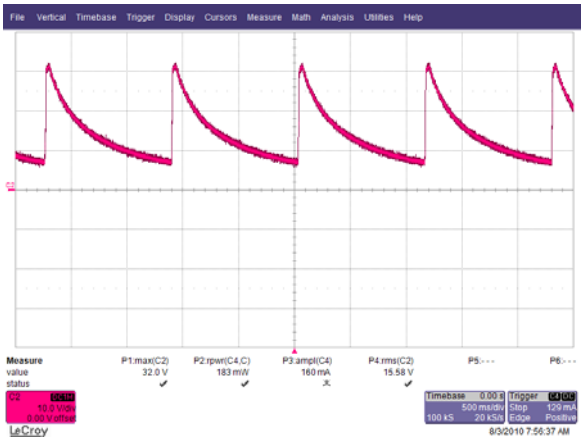

Figure 28 – Output Voltage: 115 VAC.
V_{OUT}, 10 V / div., 500 ms / div.

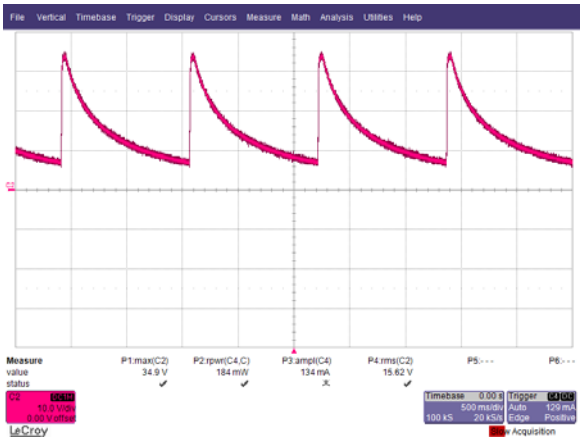

Figure 29 – Output Voltage: 230 VAC.
V_{OUT}, 10 V / div., 500 ms / div.

Note: Under open load conditions the OV shutdown function is designed to prevent the output voltage exceeding SELV limits (45 V). This is achieved, however, the voltage rating of the output capacitors is exceeded which is acceptable for a fault condition.

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13 Dimming

13.1 Input Phase vs. Output Current

115 VAC		230 VAC	
Phase angle	**I_{OUT}(mA)**	**Phase angle**	**I_{OUT}(mA)**
165	0.36	139	0.37
100	0.2	72	0.2
67	0.1	54	0.1
48	0.05	9	0.04
41	0.03	9	0.025
15	0.004	9	0.019

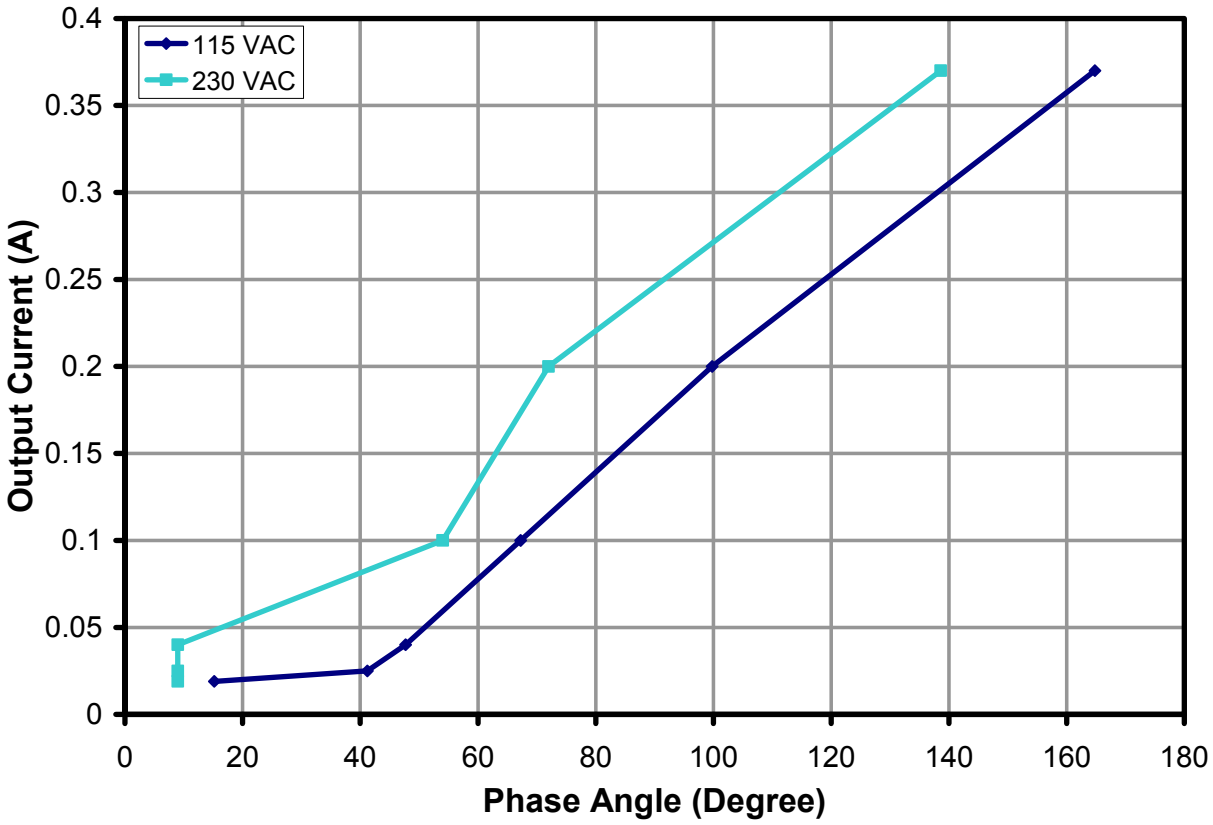

Figure 30 – Input Phase vs. Output Current.

13.2 Output Voltage and Input Current Waveforms During Dimming

13.2.1 V_{IN} = 115 VAC / 60 Hz

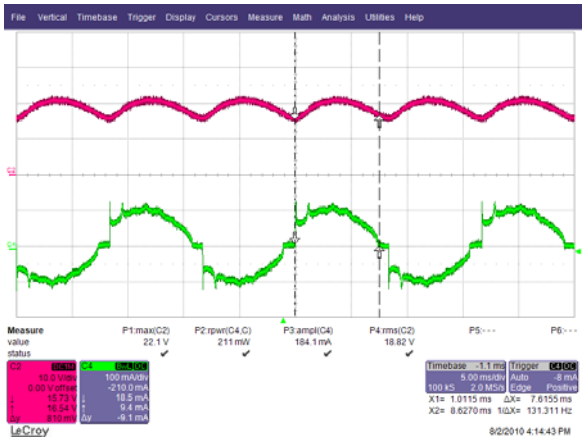

Figure 31 – 115 VAC, Full Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

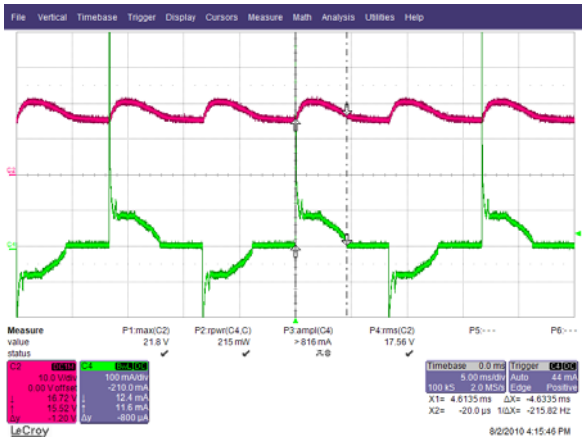

Figure 32 – 115 VAC, 67° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

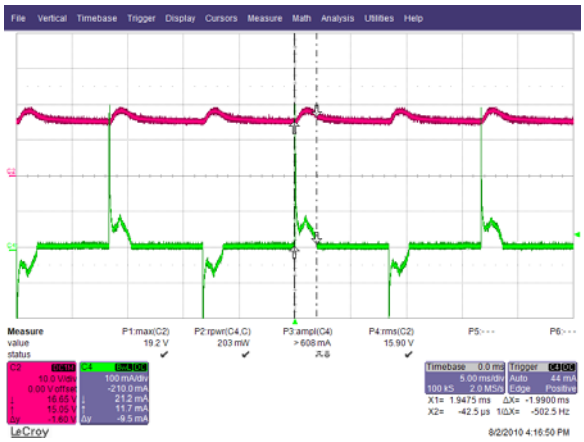

Figure 33 – 115 VAC, 48° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

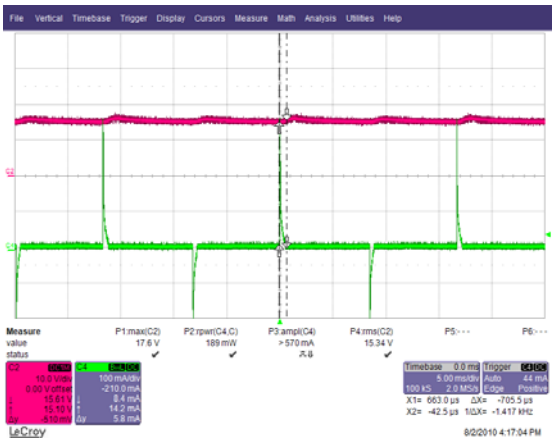

Figure 34 – 115 VAC, 15° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

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13.2.2 V_{IN} = 230 VAC / 50 Hz

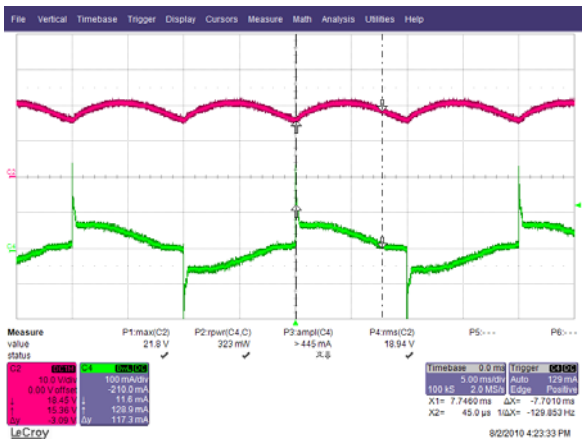

Figure 35 – 230 VAC, Full Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

Figure 36 – 230 VAC, 54° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

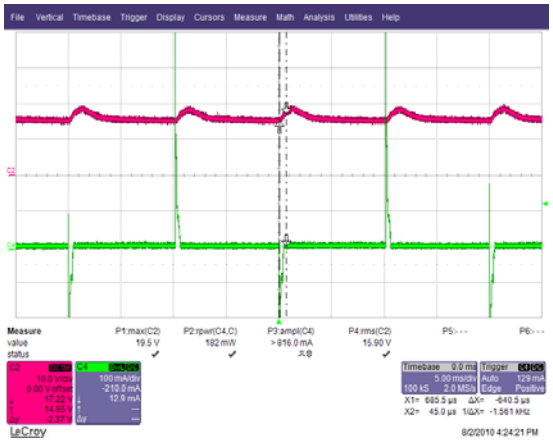

Figure 37 – 230 VAC, 9° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

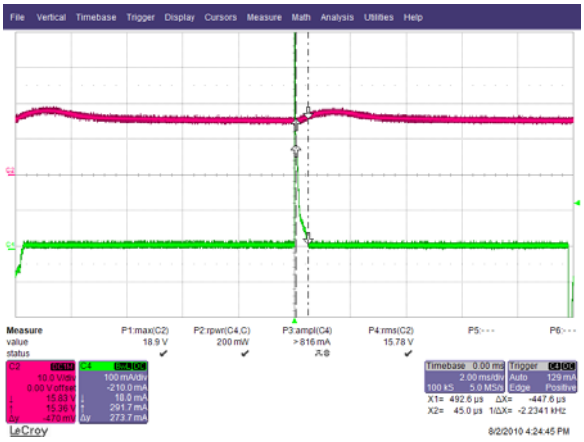

Figure 38 – 230 VAC, 9° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

14 Line Surge

Differential and common input line 200 A ring wave testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
2500	230	L to N	90	Pass
2500	230	L to N	90	Pass
2500	230	L to PE	90	Pass
2500	230	L to PE	90	Pass
2500	230	N to PE	90	Pass
2500	230	N to PE	90	Pass

Unit passes under all test conditions.

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15 Conducted EMI

Note: Refer to table for margin to standard – blue line is peak measurement but limit line is quasi peak.

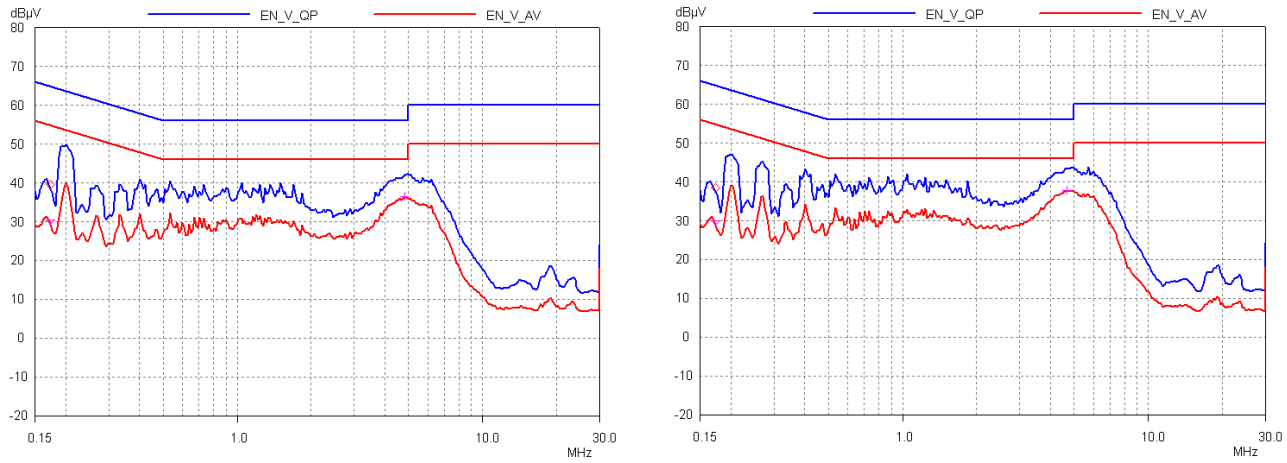

Figure 39 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 B Limits.

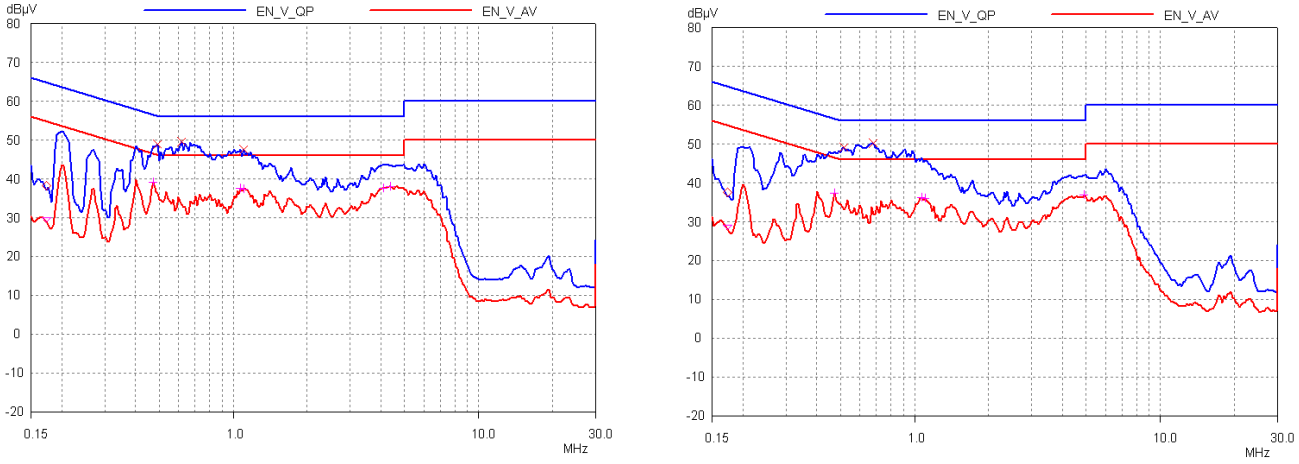

Figure 40 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 B Limits.

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
28-Mar-11	DK	1.0	Initial Release	Apps and Mktg

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