Design Example Report

Title	***5 W Cube Charger Using LinkSwitch™-II and EPC13 CORE***
Specification	85 VAC – 265 VAC Input; 5 V, 1 A Output
Application	Low-cost Charger or Adapter
Author	Applications Engineering Department
Document Number	DER-267
Date	February 9, 2011
Revision	1.1

Summary and Features

- Control concept provides very low cost, low part-count solution
  - Primary-side control eliminates secondary-side control and optocoupler
  - Provides ±5% constant voltage (CV) and ±10% constant current (CC) accuracy including output cable drop compensation
  - Over-temperature protection – tight tolerance (±5%) with hysteretic recovery for safe PCB temperatures under all conditions
  - Auto-restart output short circuit and open-loop protection
  - Extended pin creepage distance for reliable operation in humid environments; >3.2 mm at package
- EcoSmart™ – Easily meets all current international energy efficiency standards – China (CECP) / CEC / ENERGY STAR 2 / EU CoC
  - No-load consumption <150 mW at 230 VAC
  - Ultra-low leakage current: <5 μA at 265 VAC input (no Y capacitor required)
  - Design easily passes EN550022 and CISPR-22 Class B EMI testing with >8 dB margin

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 5 W constant voltage/constant current (CV/CC) universal-input power supply for cell phone or similar charger applications. This reference design is based on the LinkSwitch-II family.

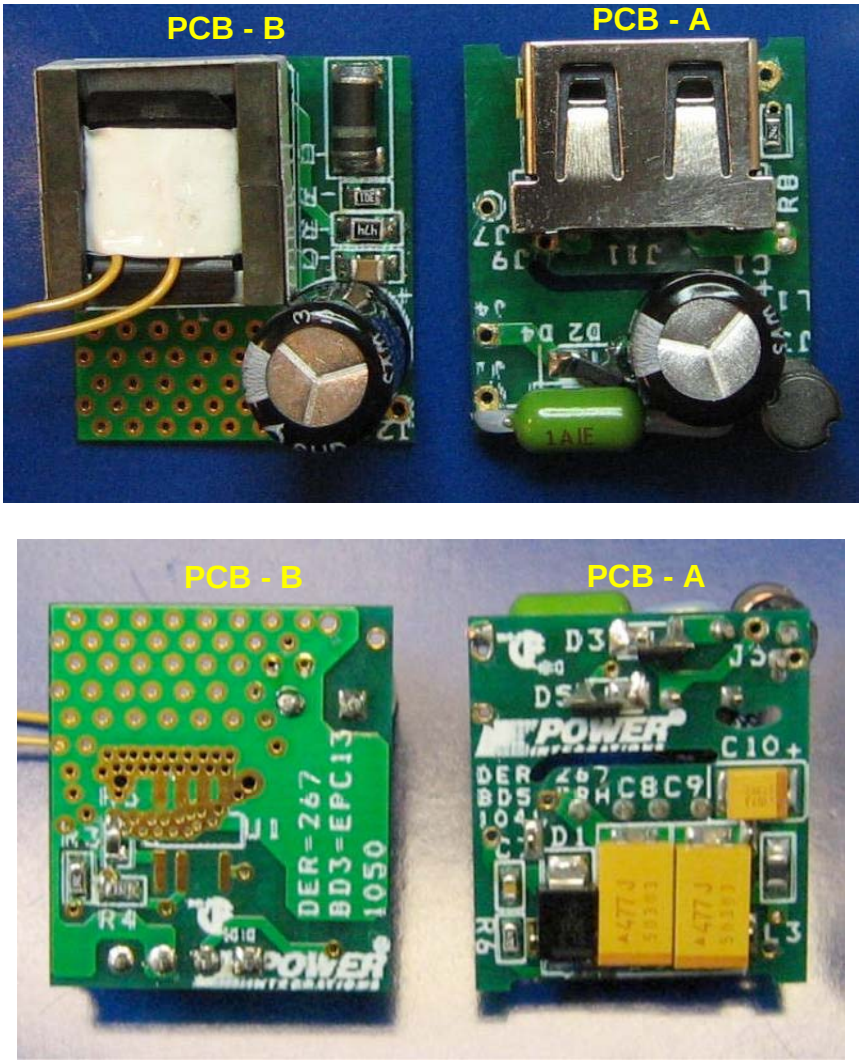

Figure 1 – DER-267 Board Photograph (Top and Bottom Views).

The LinkSwitch-II family of devices were developed to cost effectively replace all existing solutions in low-power charger and adapter applications. Its core controller is optimized for CV/CC charging applications with minimal external parts count and very tight control of both the output voltage and current, without the use of an optocoupler. The LinkSwitch-II device has an integrated 700 V switching MOSFET and ON/OFF control function which together deliver high efficiency under all load conditions and low no-load energy consumption. Both the operating efficiency and no-load performance exceed all current international energy efficiency standards.

The LinkSwitch-II device monolithically integrates the 700 V power MOSFET switch and controller. A unique ON/OFF control scheme provides CV regulation. The IC also incorporates both output cable voltage-drop compensation and tight regulation over a wide temperature range for enhanced CV control. The switching frequency is modulated to regulate the output current for a linear CC characteristic.

The LinkSwitch-II device consists of an oscillator, a feedback (sense and logic) circuit, a 5.8 V regulator, BYPASS pin programming functions, over-temperature protection, frequency jittering, a current-limit circuit, leading-edge blanking, a frequency controller for CC regulation, and an ON/OFF state machine for CV control.

The LinkSwitch-II device also provides a sophisticated range of protection features including auto-restart for control loop component open/short circuit faults and output short circuit conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and PCB), which is required in highly humid environments to prevent arcing and to further improve reliability.

The LinkSwitch-II device can be configured to either be self-biased from the high-voltage DRAIN pin, or to receive an optional external bias supply.

This document contains the power supply specifications, schematic, bill of materials, transformer specifications, and typical performance characteristics for this reference design.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power	P_{NL}			150	mW	Measured at V_{IN} = 230 VAC
Output						All measured at end of cable
Output Voltage	V_{OUT}	4.75	5.00	5.25	V	±5%
Output Ripple Voltage	V_{RIPPLE}			150	mV	20 MHz bandwidth
Output Current	I_{OUT}		1100		mA	±10%
Output Cable Resistance	R_{CBL}		0.25		Ω	
Output Power	P_{OUT}		5		W	
Name Plate Output Rating						
Name plate Voltage	V_{NP}		5		V	
Nameplate Current	I_{NP}		1000		mA	
Nameplate Power	P_{NP}		5		W	
Transient (0- 50% Step load)	V_{MIN}	4.2			V	Step load from 0 - 50%
Efficiency						
Average Active Mode	η		70		%	115 VAC / 230 VAC, 25 °C
Required average efficiency per Energy Star EPS v1.1 / CEC 2008	$\eta_{ESV1.1}$	64	Measured per Energy Star "Test Method for Calculating the Energy Efficiency of Single-Voltage External AC-DC and AC-AC Power Supplies (August 11, 2004)". η_{ESV1}:(0.09 ln(P_{NP})+0.5 η_{ESV2}:(0.075 ln(P_{NP})+0.561				
Required average efficiency per Energy Star EPS v2 April, 2008	η_{ESV2}	68				
Environmental						
Conducted EMI	Meets CISPR22B / EN55022B					>6 dB margin
Safety	Designed to meet IEC950, UL1950 Class II					
Line Surge						1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Differential		1			kV	
Common Mode		2			kV	
Ambient Temperature	T_{AMB}	0		45	°C	Case external, free convection, sea level

3 Schematic

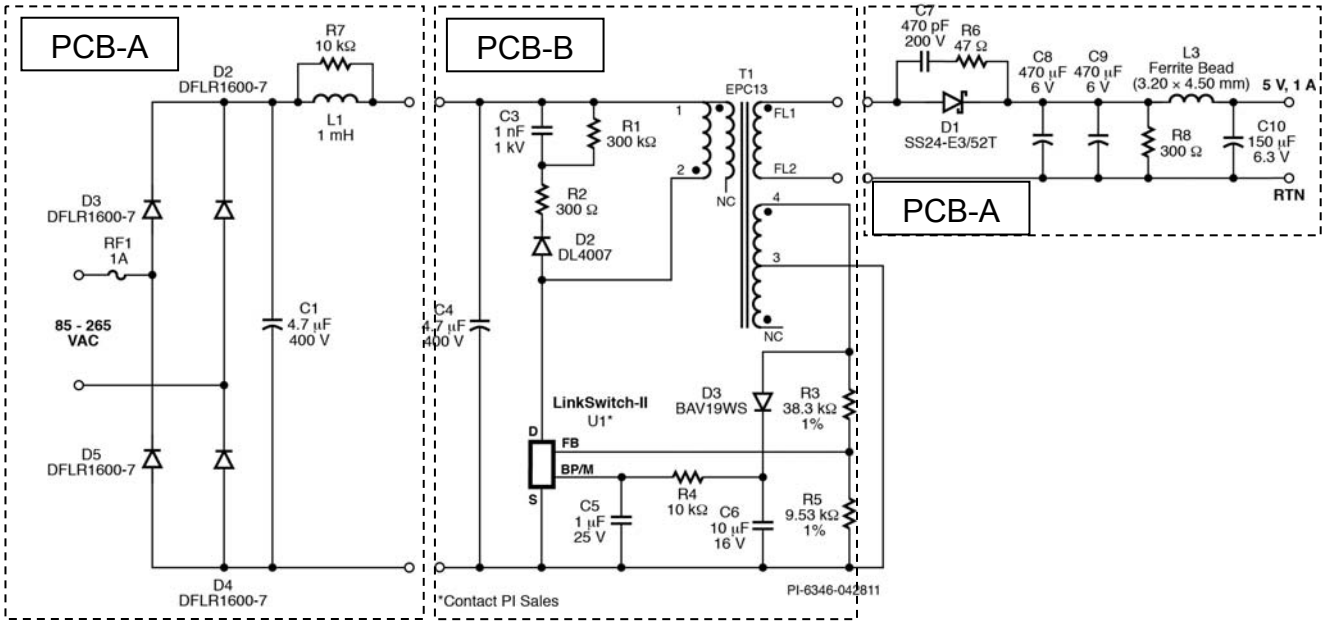

Figure 2 – Circuit Schematic.

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4 Circuit Description

This circuit uses the LinkSwitch-II device in a primary-side regulated flyback power supply configuration.

4.1 Input Filter

The AC input power is rectified by diodes D2 through D5. The rectified DC is filtered by the bulk storage capacitors C1 and C4. Inductor L1, with capacitors C1 and C4, form pi (π) filters to attenuate conducted differential-mode EMI noise. This configuration, along with Power Integrations' transformer E-shield™ technology, allows this design to meet EMI standard EN55022 class B with good margin and without a Y capacitor. The transformer construction also gives very good EMI repeatability. Fuse RF1 provides protection against catastrophic failure. Should a fusible resistor be used for RF1 it should be rated to withstand the instantaneous dissipation when the supply is first connected to the AC input (while the input capacitors charge) at VAC_{MAX}. This means choosing either an over-sized metal-film or a wire-wound type. This design uses a wire-wound resistor for RF1.

4.2 LinkSwitch-II Primary

The LinkSwitch-II device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and start-up and protection functions all on one IC. Its integrated 700 V MOSFET allows sufficient voltage margins in universal input AC applications, including extended line swells. The device is self-powered from the BYPASS pin via the decoupling capacitor C5. The value of C5 also programs the cable-drop voltage compensation. In this case, a 1 μF capacitor gives the 350 mV (7% of V_{NO}) compensation needed for the nominal #24 AWG cable, with 0.25 Ω impedance, used in this design. The bias circuit consisting of D3, C6, and R4 increases efficiency and reduces no-load input power to less than 150 mW.

The rectified and filtered input voltage is applied to one end of the transformer (T1) primary winding. The other side of the transformer's primary winding is driven by the internal MOSFET of U1. An RCD-R clamp consisting of D2, R1, R2, and C3 limits drain-voltage spikes caused by leakage inductance. Resistor R1 has a relatively large value to prevent any excessive ringing on the drain voltage waveform caused by the leakage inductance. Excessive ringing can increase output ripple by introducing an error in the sampled output voltage. IC U1 samples the feedback winding each cycle, 2.5 μs after turn-off of its internal MOSFET.

4.3 Output Rectification and Filtering

The transformer (T1) secondary is rectified by D1, a Schottky barrier-type diode (chosen for higher efficiency), and filtered by C8 and C9. In this application, C8 and C9 have sufficiently low ESR characteristics to allow meeting the output voltage ripple requirement without adding an LC post filter. However, post filter L3, C10 was employed to reduce ripple to less than 100 mV. Resistor R6 and capacitor C7 dampen high-frequency ringing and reduce the voltage stress on D1.

In designs where lower average efficiency is acceptable (by 3% to 4%) D7 may be replaced by a PN-junction to lower cost. In this case, ensure R3 and R5 are re-adjusted as necessary to keep the output voltage centered.

4.4 Output Regulation

The LinkSwitch-II device regulates the output using ON/OFF control for CV regulation, and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R3 and R5) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds. Resistor R8 provides a minimum load to maintain output regulation when the output is unloaded.

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5 PCB Layout

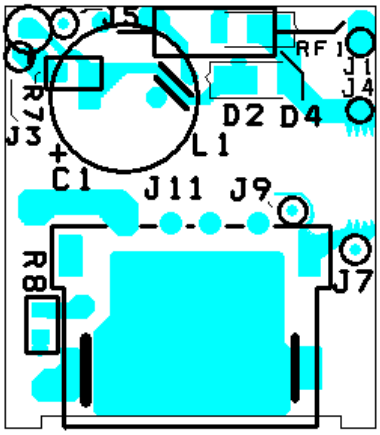
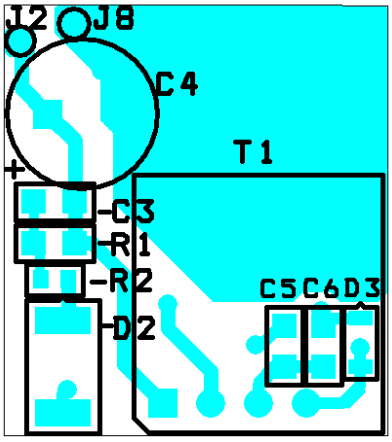
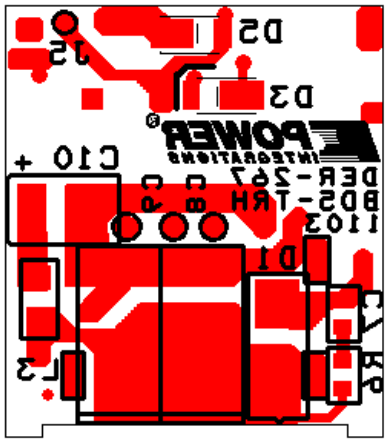
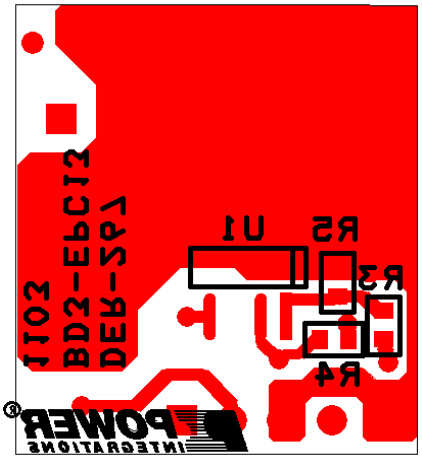
PCB – A **DIMENSION: 878 mils x 772 mils**	**PCB – B** **DIMENSION: 885 mils x 785 mils**
TOP: 	TOP: 
BOTTOM: 	BOTTOM: 

Figure 3 – Printed Circuit Layout.

6 Bill of Materials

6.1 PCB - A Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	SHD400WV 4.7uF	Sam Young
2	1	C7	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
3	2	C8 C9	470 μF, 6 V, Tant Electrolytic, E Case, SMD	TAJY477K006RNJ	AVX
4	1	C10	150 μF, 6.3 V, Tant Electrolytic, E Case, SMD	TCJH157M006R0200	AVX
5	1	D1	40 V, 2 A, Schottky, SMD, DO-214AA Low Drop	SS24-E3/52T	Vishay
6	4	D2 D3 D4 D5	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes Inc
7	6	J1 J3 J4 J5 J7 J9	PCB Terminal Hole, #18 AWG	N/A	N/A
8	1	J11	CONN USB VERT FMALE TYPE A	690-004-660-013	EDAC
9	1	L1	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
10	1	L3	Ferrite Bead, 70 mΩ DCR, 1206 SMD (This is a substitute – Efficiency will be slightly lower than the original inductor used which has 40mΩ DCR)	742792122	Wurth Elektronik
11	1	R6	47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
12	1	R7	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
13	1	R8	300 Ω, 5%, 1/10 W, Thick Film, 0805	ERJ-3GEYJ300V	Panasonic
14	1	RF1	1 A, 125 V, Fast, Picofuse, Axial	27511000001	Wickman

6.2 PCB - B Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C3	1 nF, 1000 V, Ceramic, X7R, 0805	C0805C102KDRACTU	Kemet
2	1	C4	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	SHD400WV 4.7uF	Sam Young
3	2	C5 C6	10 μF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
4	1	D2	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes Inc
5	1	D3	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes Inc
6	4	J2 J6 J8 J10	PCB Terminal Hole, #22 AWG	N/A	N/A
7	1	R1	330 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ334V	Panasonic
8	1	R2	300 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ301V	Panasonic
9	1	R3	38.3 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3832V	Panasonic
10	1	R4	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
11	1	R5	9.53 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9531V	Panasonic
12	1	T1	Bobbin, BEPC13, Horizontal, 10 pins	N/A	TDK or Equivalent
13	1	U1	LinkSwitch-II, CV/CC, SO-8C	LinkSwitch-II Contact PI Sales	Power Integrations

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7 Transformer Specification

7.1 Electrical Diagram

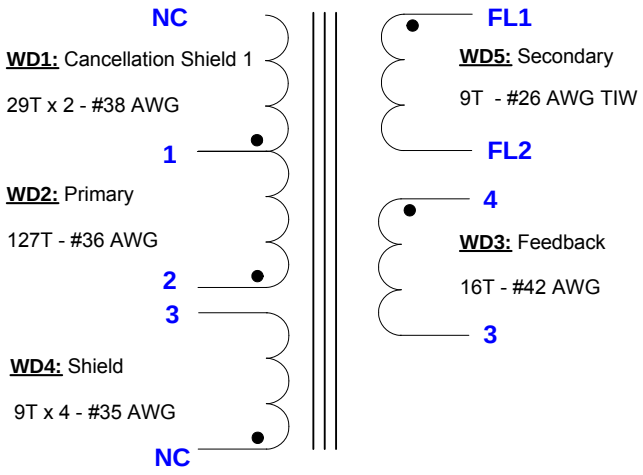

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-4 to flying leads FL1-FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 VRMS	970 µH, ±5%
Resonant Frequency	Pins 1-2, all other windings open	600 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with flying leads FL1-FL2 shorted, measured at 100 kHz, 0.4 VRMS	80 µH (Max.)

7.3 Materials

Item	Description
[1]	Core Type: EPC13; or equivalent.
[2]	Bobbin: BEPC13, Horizontal, 10 pins (5/5)
[3]	Magnet wire: #38 AWG double coated.
[4]	Magnet wire: #36 AWG double coated.
[5]	Magnet wire: #42 AWG double coated.
[6]	Magnet wire: #35 AWG double coated.
[7]	Magnet wire: #26 AWG Triple Insulated Wire.
[8]	Tape: 3M 1298 Polyester Film (white), 7.0 mm wide, 2.0 mils thick, or equivalent.
[9]	Varnish: Dolph BC-359, or equivalent.

7.4 Transformer Build Diagram

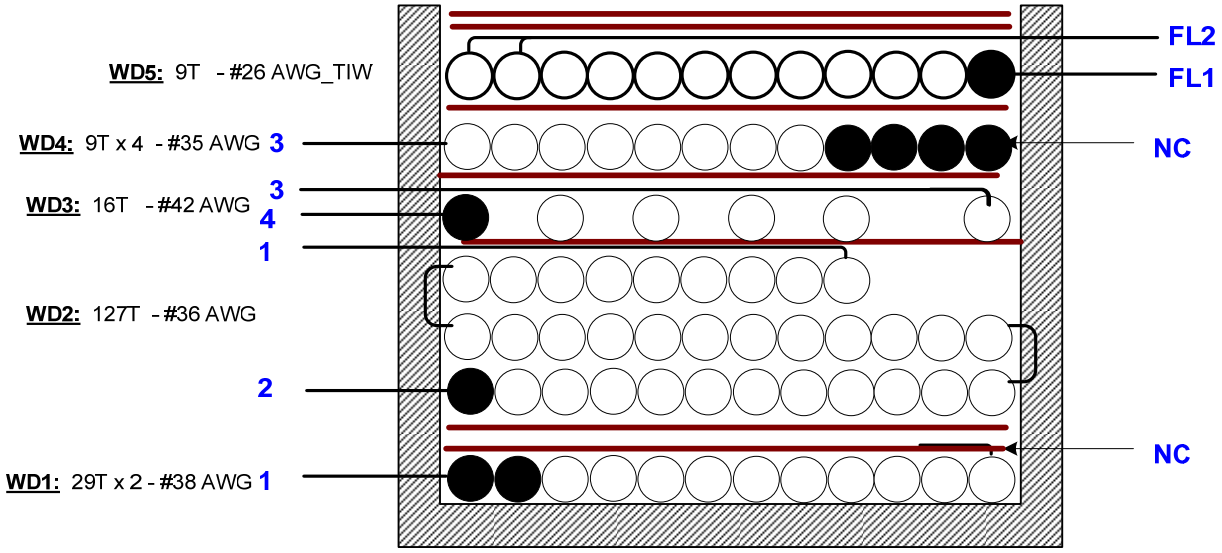

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Winding Preparation	Remove all secondary pins of bobbin item [2] and cut round the secondary flange, (see pictures below). Place the bobbin on the mandrel with pin side is on the left hand side. Winding direction is clock-wise direction.
WD1 Cancellation Shield 1	Start at pin 1, wind 30 bifilar turns of wire [3] in exactly 1 layer, from left to right. At the last turn cut short the wires not connected, bend 90 degree, and leave in the middle of the bobbin.
Insulation	2 layers of tape item [8]
WD2 Primary	Start at pin 2, wind 127 turns of wire item [4] in 2 1/2 layers, finish with tight tension, and evenly. At the last turn, bring the wire back to the left terminate at pin1.
Insulation	1 layer of tape item [8].
WD3 Feedback	Start at pin 4, wind 16 turns of wire item [5] from left to right. At the last turn bring the wires back the left to terminate at pin 3.
Insulation	1 layer of tape [8].
WD4 Shield	Start at pin 4, wind 9 quadfilar turns of wire item [6] from left to right. At the last turn bring the wires back the left to terminate at pin 3.
Insulation	1 layer of tape item [8].
WD5 Secondary	Start as FL1 from the right of bobbin, wind 9 turns of wire item [7] to the left. At the last turn bring the wires back to the right and let them floating as FL2.
Insulation	2 layers of tape item [8].
Finish	Cut short all secondary wires about 1” long and tin. Grind core halves to get 970 µH and assemble with tape. Varnish with item [9].

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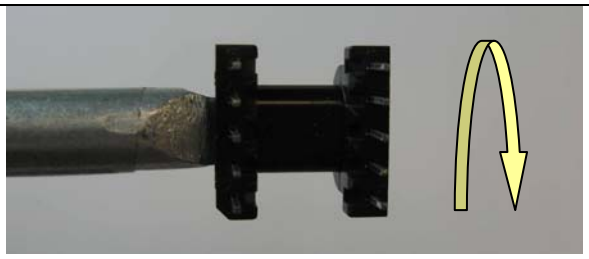
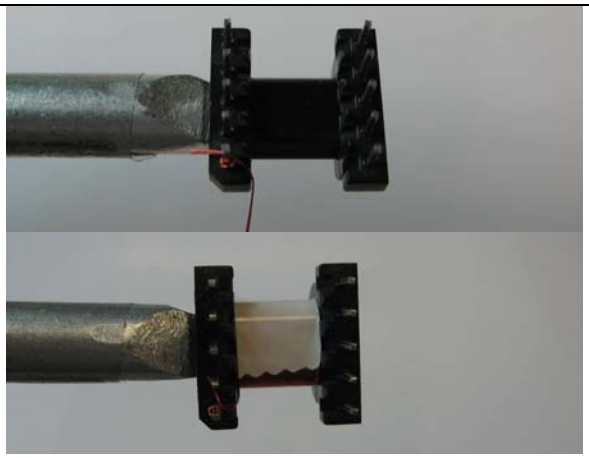
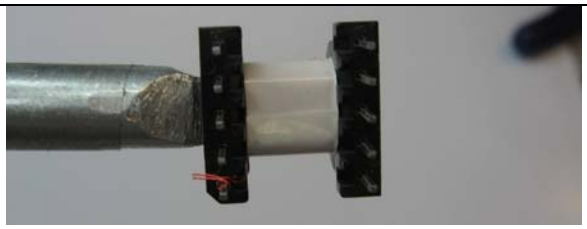
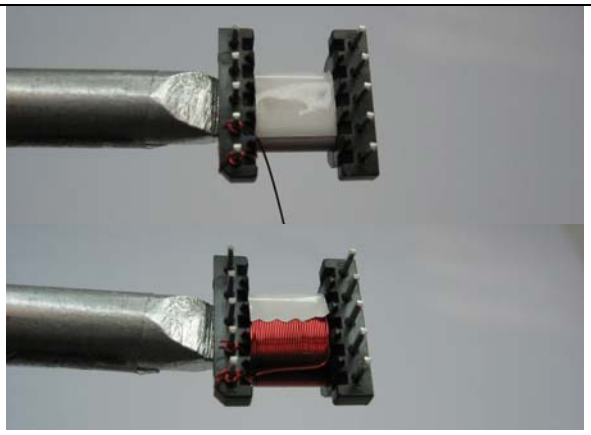
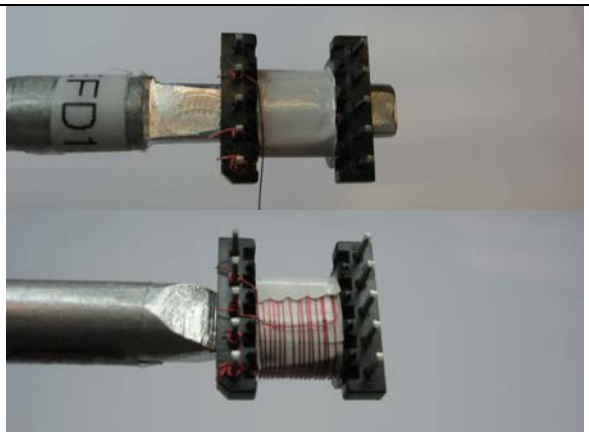
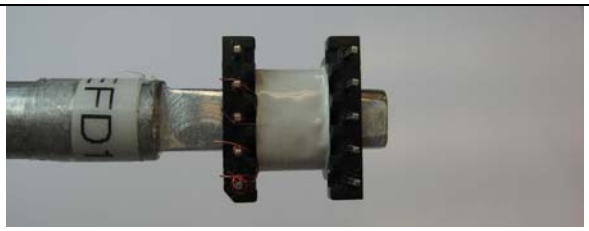
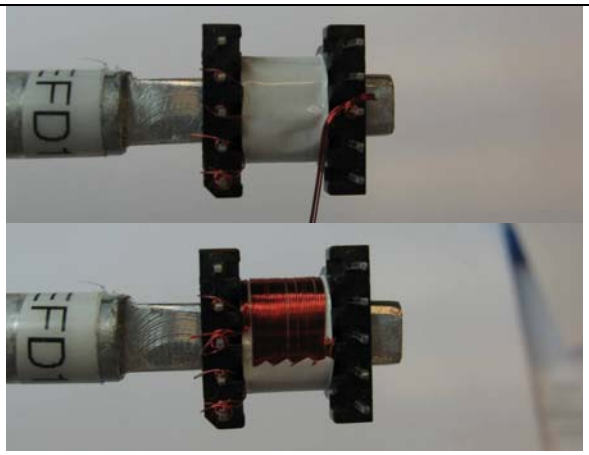
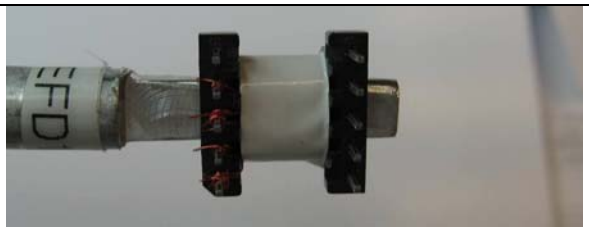
7.6 Winding Illustrations

Bobbin Preparation		Bobbin and Core.
Bobbin Prepare		Place the bobbin on the mandrel with pin side is on the left hand side. Winding direction is clock-wise.
WD1 (Cancellation)		Starting at pin 1, wind 29 bifilar turns of wire [3] in exactly 1 layer, from left to right. At the last turn cut short the wires not connected.
Tape		Apply 2 layer of tape item [8] for insulation.
WDG 2 (Primary)		Starting at Pin 2, wind 127 turns of wire item [4] in 2 1/2 layers. At the last turn, bring the wire back to the left terminate at pin 1.

Insulation		Apply one layer of tape item [8].
WDG 3 (Feedback)		Starting at pin 4, wind 16 turns of wire item [5] in one layer from left to right. At the last turn bring the wires back the left to terminate at pin 3.
Insulation		Apply one layer of tape item [8].
WDG 4 (Shield)		Start temporary at pin 8, wind 9 quadfilar turns of wire item [6] from right to left. Terminate at pin 3. Cut the wire at start, pin 8.
Insulation		Apply one layer of tape item [8].

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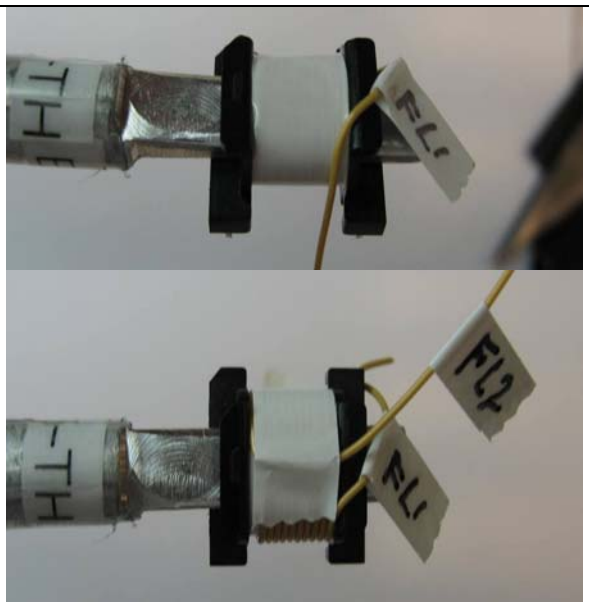
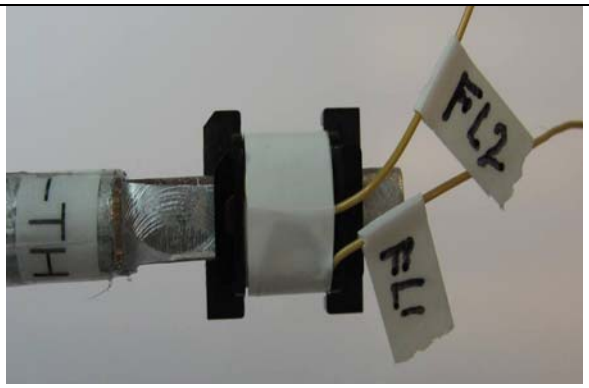
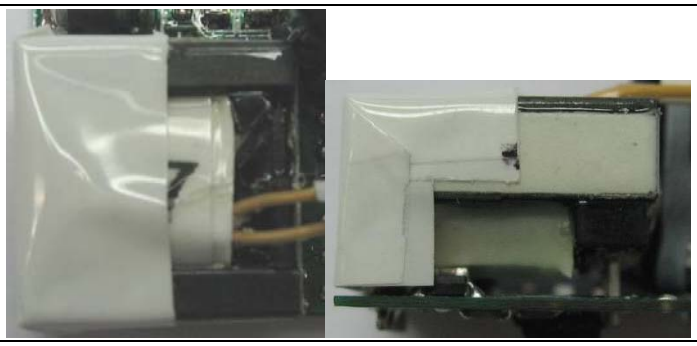
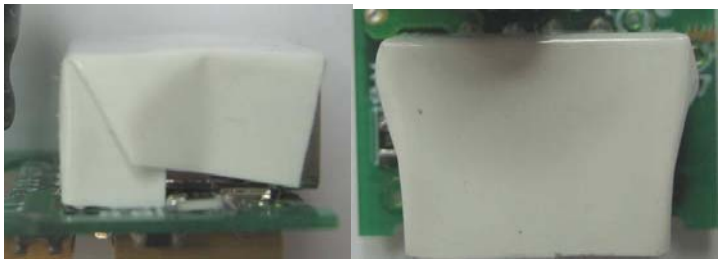
WDG 5		Start as FL1 from the right of bobbin, wind 9 turns of wire item [7] to the left. At the last turn bring the wires back to the right and let them floating as FL2.
Insulation		Apply 2 layer of tape item [8] for finish wrap.
Finish		Cut short all secondary wires about 1” long and tin. Grind core halves to get 970 μH and assemble with tape. Varnish with item [9].

8 Special Assembly Note

Insulating the Transformer		Apply 2 layers of tape to wrap transformer.
Insulating the USB Connector		Apply 2 layers of tape to wrap the USB connector.
Teflon Tube for C1		Insert 2 mm long Teflon tube for capacitor C1.
Jumper Wires		Insert 2” #28 jumper wire into J1, J4, J3, J5.
Assemble as Shown		FL1 to J9 FL2 to J7 J3 (B+) to J2 (B+) J5 (B-) to J8 (B-).

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9 Transformer Design Spreadsheet

ACDC_LinkSwitch-II_120209; Rev.1.11; Copyright Power Integrations 2009	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-II_120209_Rev1-11; LinkSwitch-II Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	5.00			V	Output Voltage (at continuous power)
IO	1.08			A	Power Supply Output Current (corresponding to peak power)
Power			5.40	W	Continuous Output Power
n	0.70		0.70		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
Add Bias Winding	no		no		Choose Yes to add a Bias winding to power the LinkSwitch-II.
CIN	9.40			uF	Input Capacitance
ENTER LinkSwitch-II VARIABLES					
Chosen Device	**LinkSwitch-II**		**LinkSwitch-II**		Chosen LinkSwitch-II device
Package	**PG**		PG		Select package (PG, GG or DG)
ILIMITMIN			0.39	A	Minimum Current Limit
ILIMITTYP			0.41	A	Typical Current Limit
ILIMITMAX			0.45	A	Maximum Current Limit
FS	81.00		81.00	kHz	Typical Device Switching Frequency at maximum power
VOR			77.61	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LinkSwitch-II on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			1.41		Ensure KDP > 1.3 for discontinuous mode operation
FEEDBACK WINDING PARAMETERS					
NFB	9.00		9.00		Feedback winding turns
VFLY			5.50	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			3.86	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
VB			N/A	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB			N/A		Bias Winding number of turns
REXT			N/A	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON			4.50	us	Output diode conduction time
TON			6.21	us	LinkSwitch-II On-time (calculated at minimum inductance)
RUPPER			21.31	k-ohm	Upper resistor in Feedback resistor divider
RLOWER			11.80	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	**EPC13**		EPC13		Enter Transformer Core. Based on the

					output power the recommended core sizes are EE19 or EE22
Bobbin			EPC13_BOBBIN		Generic EPC13_BOBBIN
AE	12.50		12.50	mm^2	Core Effective Cross Sectional Area
LE	31.00		31.00	mm^2	Core Effective Path Length
AL	870.00		870.00	nH/turn^2	Ungapped Core Effective Inductance
BW	6.88		6.88	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4.00		Number of Primary Layers
NS			9.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			54.41	V	Minimum DC bus voltage
VMAX			373.35	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Maximum duty cycle measured at VMIN
IAVG			0.17	A	Input Average current
IP			0.39	A	Peak primary current
IR			0.39	A	Primary ripple current
IRMS			0.18	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			866.83	uH	Minimum Primary Inductance
LPTYP			963.15	uH	Typical Primary inductance
LP_TOLERANCE			10.00	%	Tolerance in primary inductance
NP			127.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			59.72	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET			2500.00	Gauss	Target Flux Density
BM			2487.49	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended
BP		*Warning*	3009.87	Gauss	!!! Warning. Peak Flux density exceeds 3000 Gauss and is not recommended. Reduce BP by increasing NS
BAC			1243.75	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			171.70		Relative Permeability of Ungapped Core
LG			0.27	mm	Gap Length (LG > 0.1 mm)
BWE			27.52	mm	Effective Bobbin Width
OD			0.22	mm	Maximum Primary Wire Diameter including insulation
INS			0.04		Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.17	mm	Bare conductor diameter
AWG			34.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			40.32	Cmils	Bare conductor effective area in circular mils
CMA			218.40	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			5.50	A	Peak Secondary Current
ISRMS			2.18	A	Secondary RMS Current
IRIPPLE			1.89	A	Output Capacitor RMS Ripple Current
CMS			436.22	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			556.34	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10%

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					temperature tolerance)
PIVS			31.46	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL			21.31	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL			11.80	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measured) Output Voltage (VDC)			5.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)			1.08	Amps	Measured Output current from first prototype
RUPPER_FINE			21.31	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 21.5 k-ohms
RLOWER_FINE			11.80	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 11.8 k-ohms

Note: Warning note in BP marginally exceeds the recommended PIXls limit. This limit is designed to prevent core saturation at maximum ambient. As no evidence of saturation was observed in the Drain current waveform (high quality ferrite) this warning is acceptable.

10 Performance Data

All measurements were taken at room temperature unless otherwise specified, with 60 Hz input frequency. Measurements were taken at the end of a 0.25 Ω output cable.

10.1 Efficiency

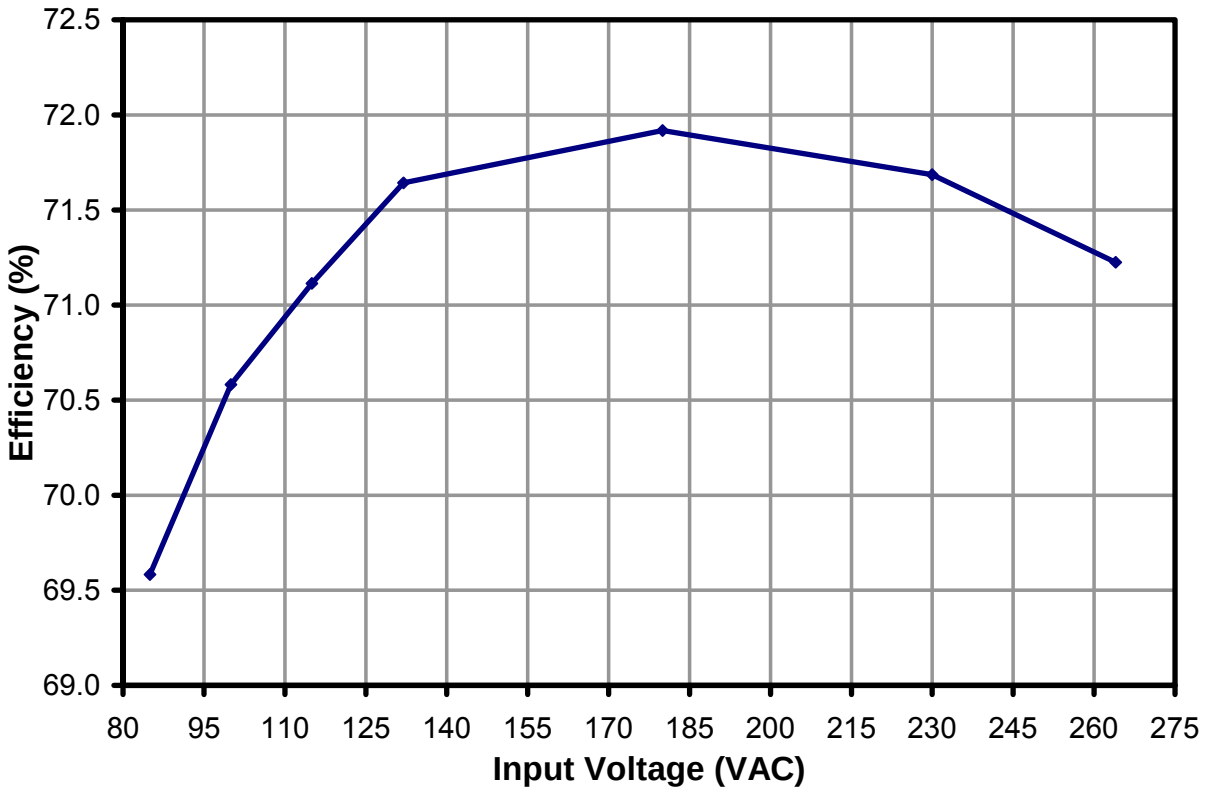

Figure 6 – Efficiency vs. Line.

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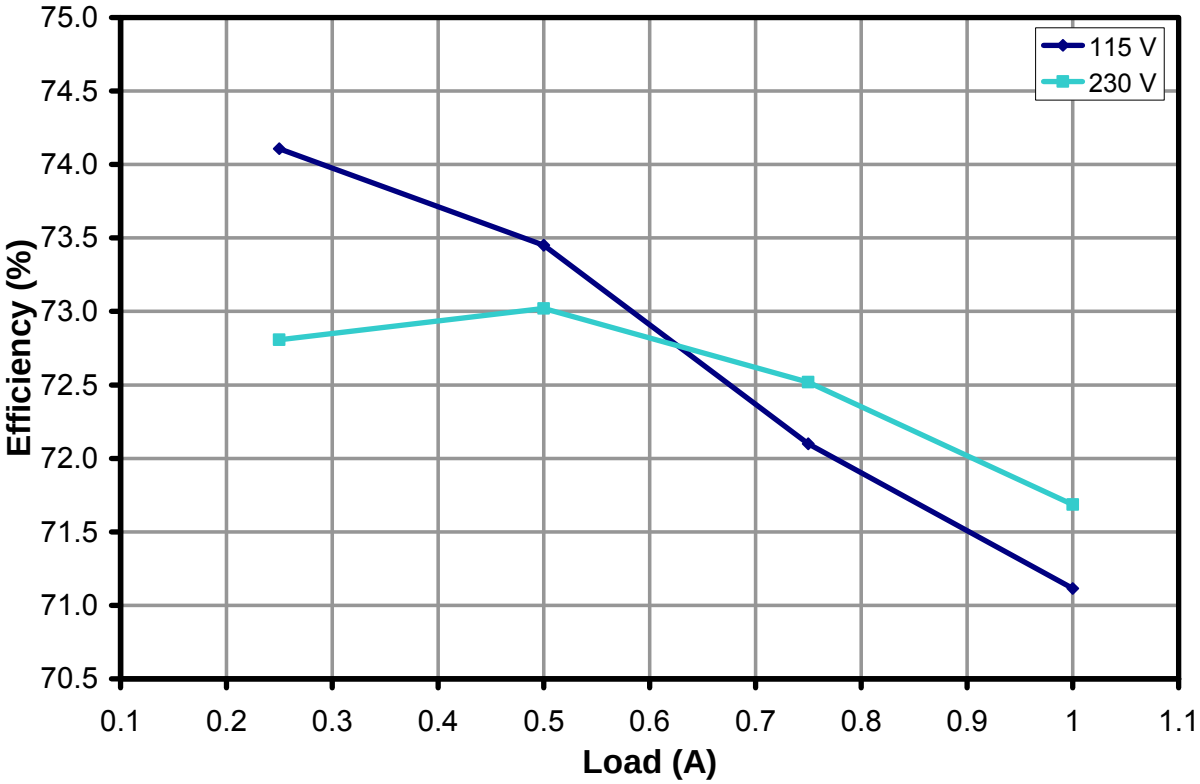

Figure 7 – Efficiency vs. Load.

10.2 Active Mode CEC Measurement Data

The power supply passes both Energy Star v1.1 and v2 (April 2008) limits.

% of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	71.11	71.69
50	72.10	72.52
75	73.45	73.02
100	74.11	72.81
Average	**72.69**	**72.51**
Energy Star v1.1	**64**	**64**
Energy Star v2	**67**	**67**

Figure 8 – Average Active Mode Efficiency.

10.2.1 Energy Star v1.1 / CEC (2008)

As part of the U. S. Energy Independence and Security Act of 2007 all single-output adapters, including those provided with products for sale in the USA after July 1, 2008, must meet the Energy Star v1.1 specification for minimum active-mode efficiency and no-load input power. Note that battery chargers are exempt from these requirements except in the state of California, where they must also be compliant.

Minimum active-mode efficiency is defined as the average efficiency at 25%, 50%, 75%, and 100% of rated output power with the limit based on the nameplate output power:

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_{NP}$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_{NP}) + 0.5$ [ln = natural log]
> 49 W	0.84

Nameplate Output (P_{NP})	Maximum No-load Input Power
All	≤ 0.5 W

For single-input voltage adapters the measurement is made at the rated (single) nominal input voltage only (either 115 VAC or 230 VAC). For universal input adapters, the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star v1.1 standard.

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10.2.2 Energy Star v2 (April 2008)

The Energy Star v2 specification (planned to take effect Nov 1, 2008) increases the previously stated requirements.

Standard Models

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation (Rounded to Hundreds)
≤ 1 W	≥ 0.48 × P_{NP} + 0.14
> 1 W to ≤ 49 W	≥ 0.0626 × ln (P_{NP}) + 0.622 [ln = natural log]
> 49 W	0.87

Nameplate Output (P_{NP})	Maximum No-load Input Power
0 to <50 W	≤ 0.3 W
≥50 to ≤250 W	≤ 0.5 W

Low-voltage Models

A low-voltage model is an external power supply (EPS) with a nameplate output voltage of less than 6 V and a nameplate output current greater than or equal to 550 mA.

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation (Rounded to Hundreds)
≤1 W	≥ 0.497 × P_{NP} + 0.067
>1 W to ≤49 W	≥ 0.075 × ln (P_{NP}) + 0.561 [ln = natural log]
>49 W	≥ 0.86

Nameplate Output (P_{NP})	Maximum No-load Input Power
0 to <50 W	≤ 0.3 W
≥50 to ≤250 W	≤ 0.5 W

For the latest up-to-date information, please visit the PI Green Room at *www.powerint.com*.

10.3 No-Load Input Power

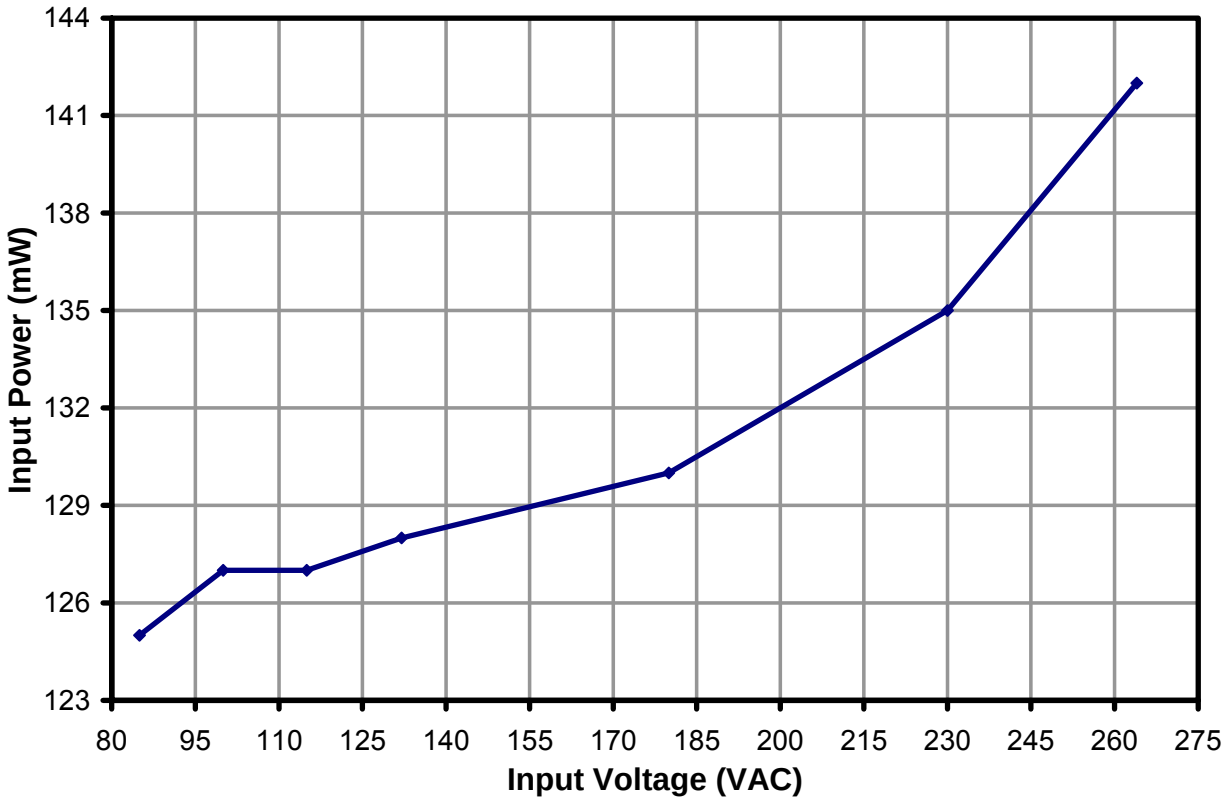

Figure 9 – Zero Load Input Power vs. Input Line Voltage, Room Temperature.

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11 Regulation

11.1 Load, Line and Temperature

The output characteristic was tested at the end of the output cable with the DC resistance of approximately 0.25 Ω.

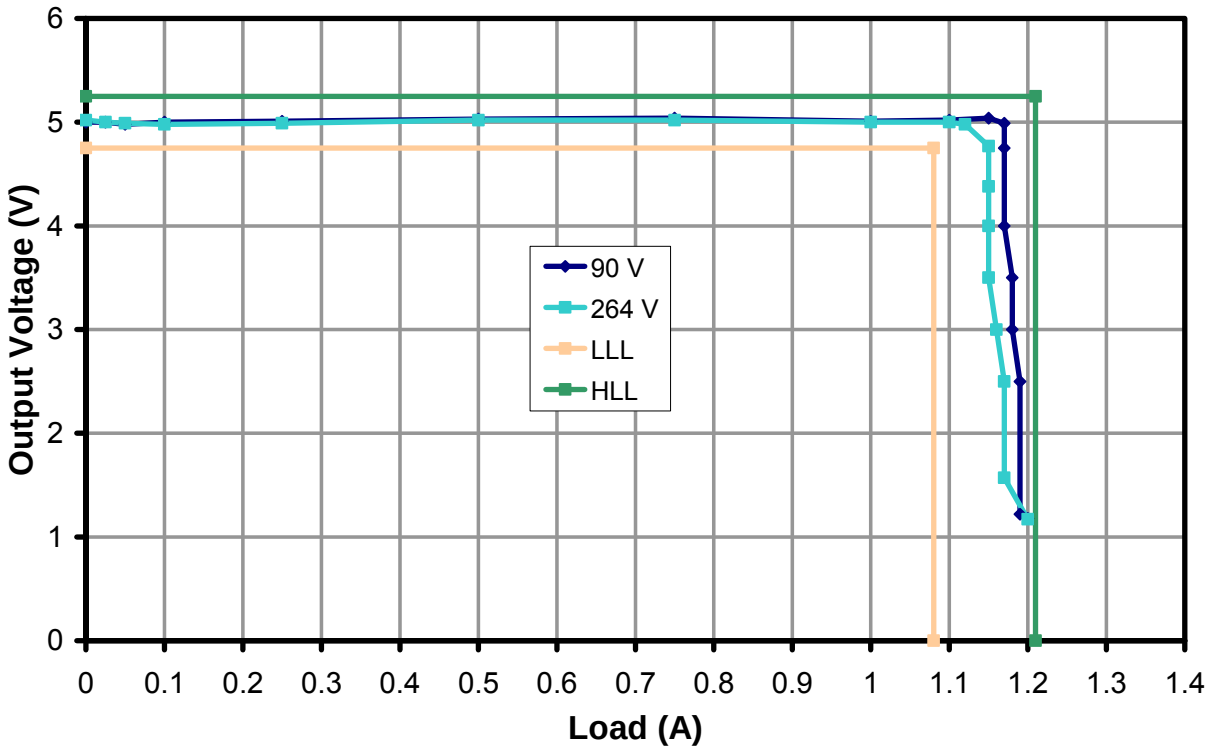

Figure 10 – Composite Output Regulation Across Load and Line; Room Temperature.

12 Thermal Performance

Thermal performance was measured inside an enclosure at full load with no airflow. A thermocouple was attached to the SOURCE pin of U1. Temperature stabilized after 1 hour.

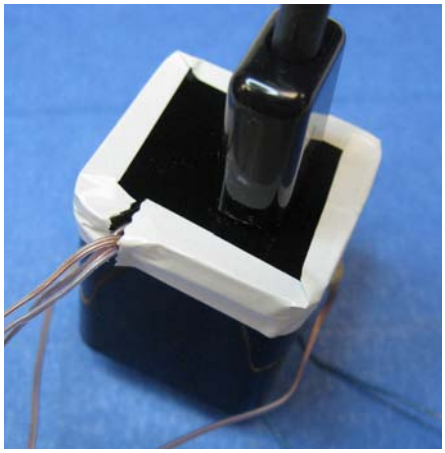

Figure 11 –Worst case thermal for surface temperature of the plastic case is upright position

Description	85 VAC / 50 Hz		265 VAC / 50 Hz		Unit
Plastic Case Surface (D1 Side)	50	70	48.2	68.2	ºC
Plastic Case Surface (U1 Side)	48.8	68.8	47.8	67.8	ºC
Output Diode (D1)	90.1	110.1	88.2	108.2	ºC
IC (U1)	86.7	106.7	80.5	100.5	ºC
Transformer (T1)	81.4	101.4	84.5	104.5	ºC
T-Ambient	25	45 (Projected)	25	45 (Projected)	ºC
P_{IN}	7.21	-	7.03	-	W
V_{OUT}	5.05	-	5.06	-	V
I_{OUT}	1.0	-	1.0	-	A
P_{OUT}	5.05	-	5.06	-	W
Efficiency	69.46	-	72.0	-	%

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13 Waveforms

13.1 Drain Voltage and Current, Normal Operation

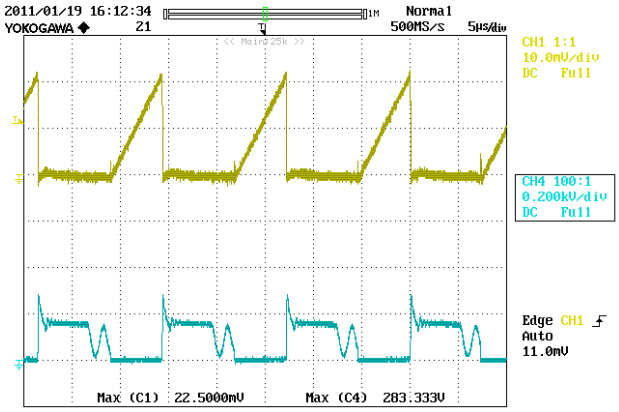

Figure 12 – 85 VAC, Full Load.
Lower: V_{DRAIN}, 200 V / div.
Upper: I_{DRAIN}, 200 mA / div., 5 µs / div.

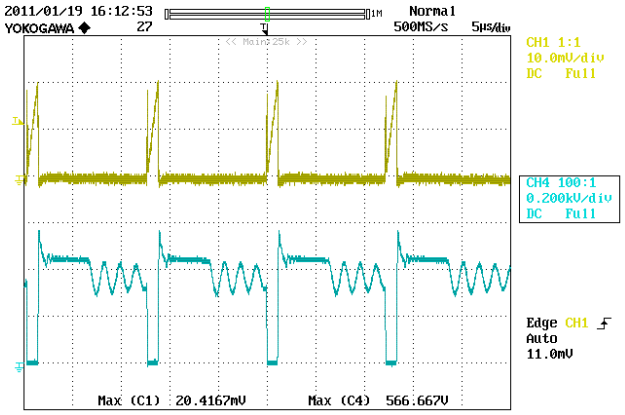

Figure 13 – 265 VAC, Full Load.
Lower: V_{DRAIN}, 200 V / div.
Upper: I_{DRAIN}, 200 mA / div., 5 µs / div.

13.2 Drain Voltage and Current Start-up Profile

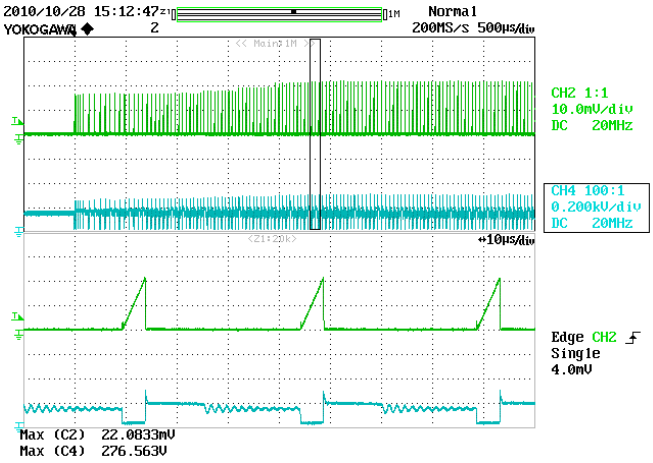

Figure 14 – 85 VAC, Full Load.
Lower: V_{DRAIN}, 200 V / div.
Upper: I_{DRAIN}, 200 mA / div., 10 µs / div.

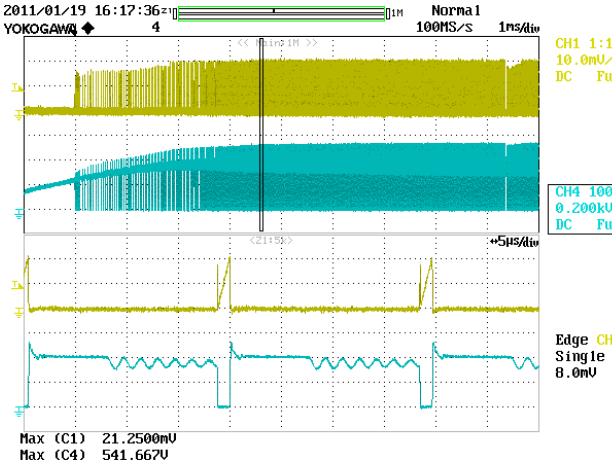

Figure 15 – 265 VAC, Full Load.
Lower: V_{DRAIN}, 200 V / div.
Upper: I_{DRAIN}, 200 mA / div., 5 µs / div.

13.3 Output Voltage Rectifier PIV

Measured stress of 31.9 V vs. 40 V diode rating or a derating of >20%.

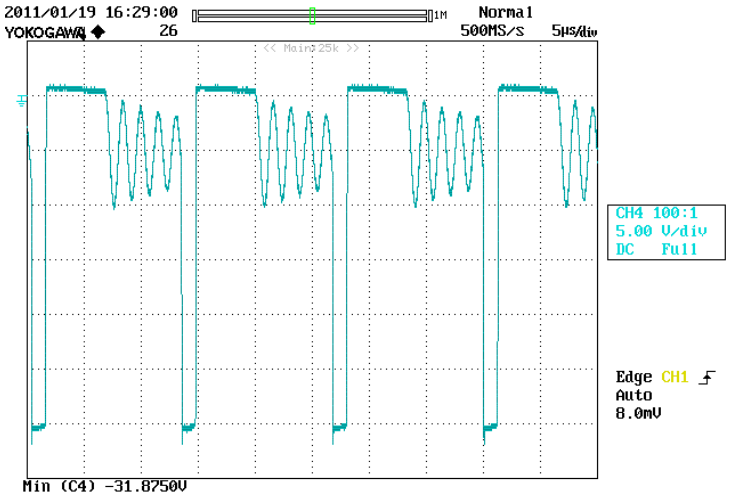

Figure 16 – 265 VAC, Full Load.
Upper: V_{PIV}, 5 V / div., 5 µs / div.

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13.4 Common Mode Noise Voltage of the DC Output

Specification: < 90 V_{P-P}

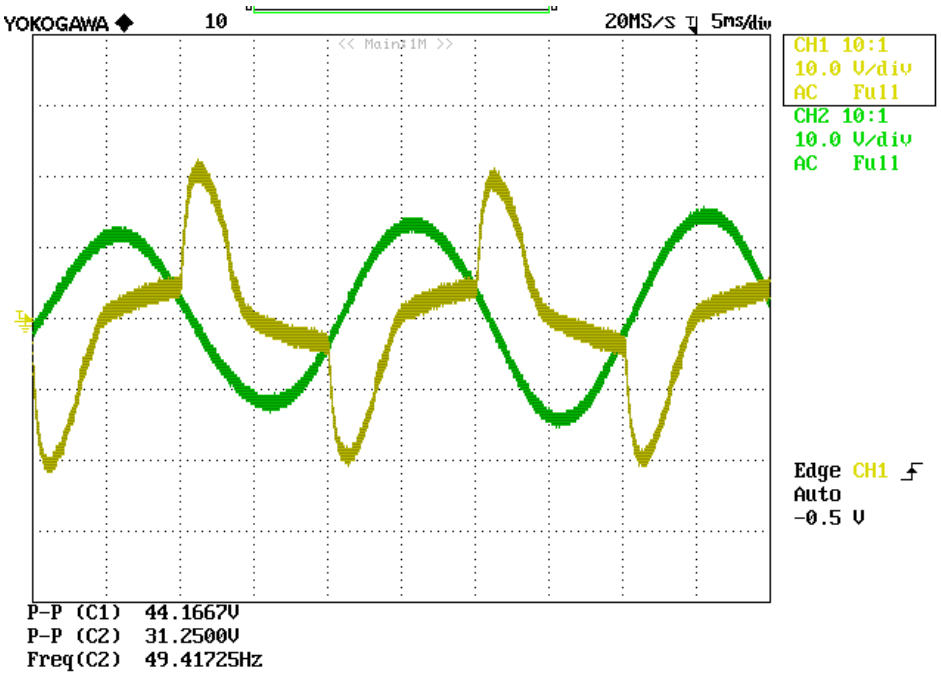
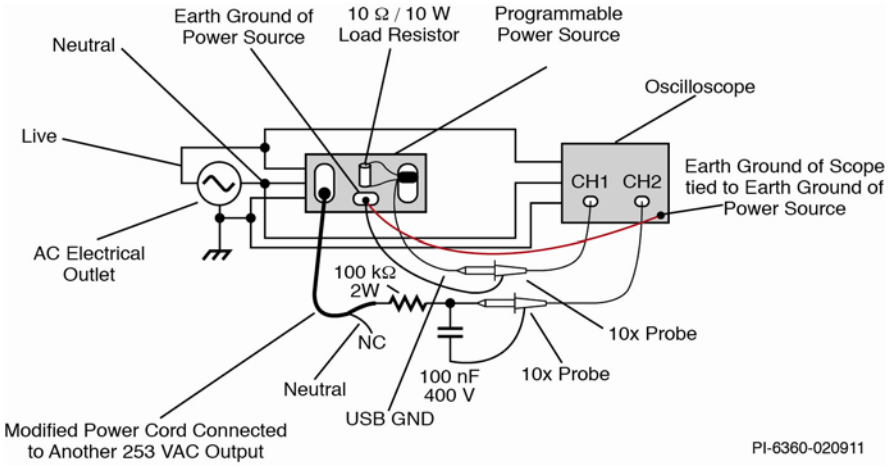


Figure 17 – 253 VAC 50 Hz, 10 Ω Load.
CH1: CM Voltage; 10 V / div., 5 ms / div.
CH2: Reference Voltage; 10 V / div., 5 ms / div.

13.4.1 Measurement Set-up Diagram



13.4.2 Common Mode Noise Voltage Verification Set-up

AC Source: Chroma Model 6408 set at V_{OUT}: 253 VAC / 50 Hz
Oscilloscope: Yokogawa DL1740E
CH1: TEST VOLTAGE; 10x PROBE; 10 V / DIV.; 5 ms / DIV.; Full BW
CH2: REFERENCE VOLTAGE; 10x PROBE; 10 V / DIV.; 5 ms / DIV.; Full BW

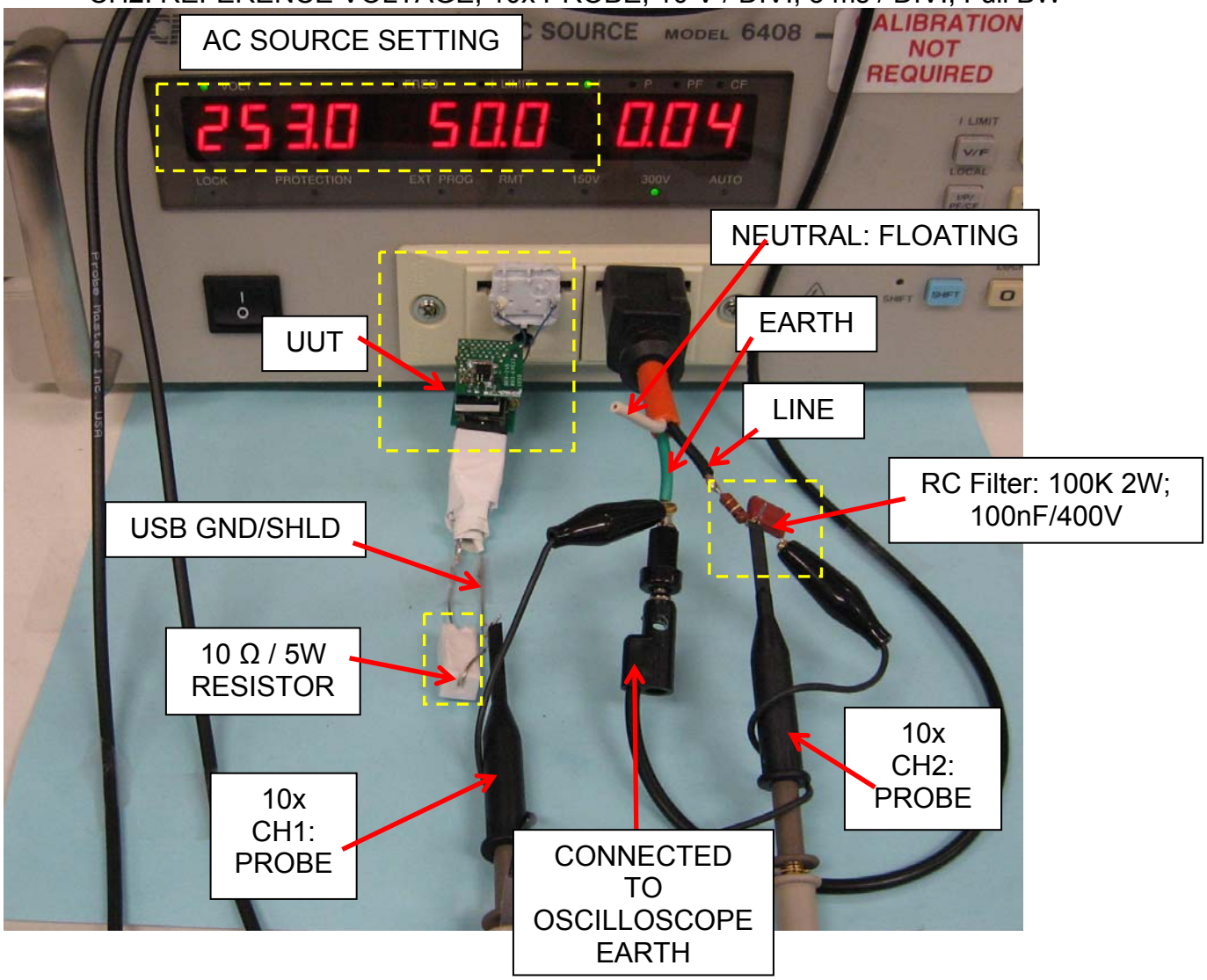


Figure 18 – Common Mode Noise Voltage Verification Test Set-up.

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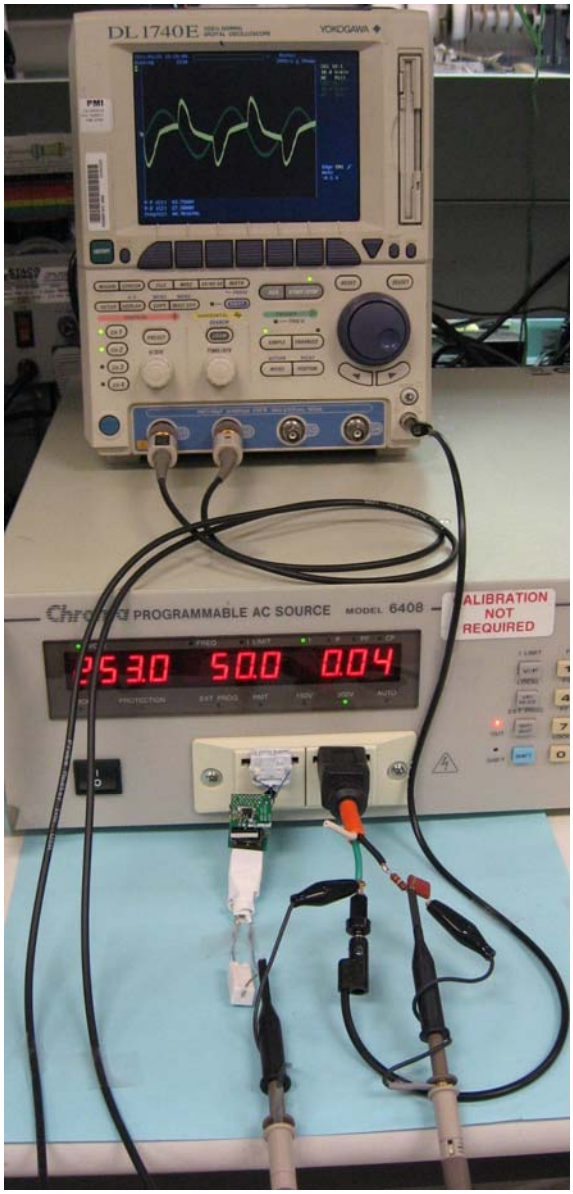

Figure 19 – Common Mode Noise Voltage Verification Test Set-up.

13.5 Load Transient Response

E-Load Setting: CR mode
Slew Rate: 100 mA / µs

Output filter as shown in Figure 2.

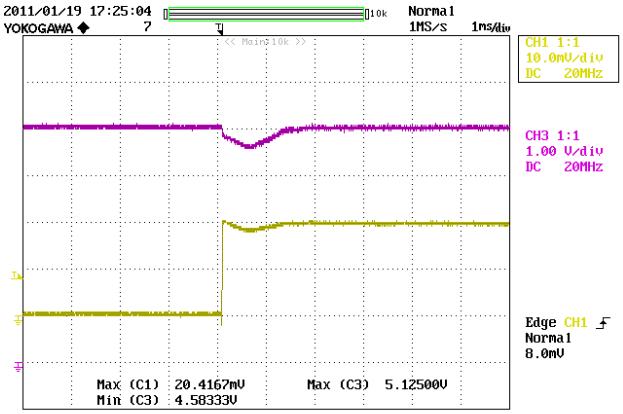

Figure 20 – Transient Response, 85 VAC.
0 to 50 mA Load Step
Output Voltage 1 V, 1 ms / div.

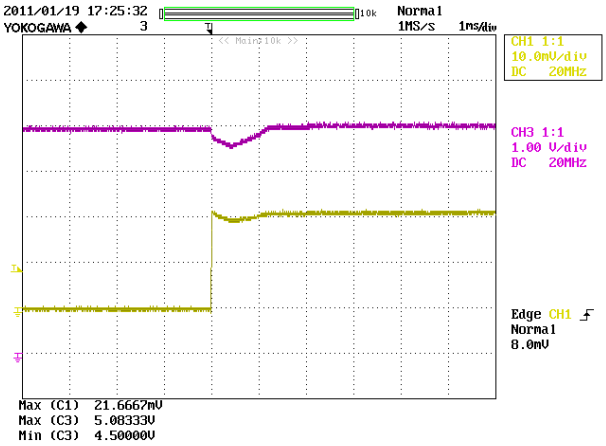

Figure 21 – Transient Response, 265 VAC.
0 to 500 mA Load Step
Output Voltage 1 V, 1 ms / div.

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13.6 Output Ripple Measurements

13.6.1 Ripple Measurement Set-up

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 50 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

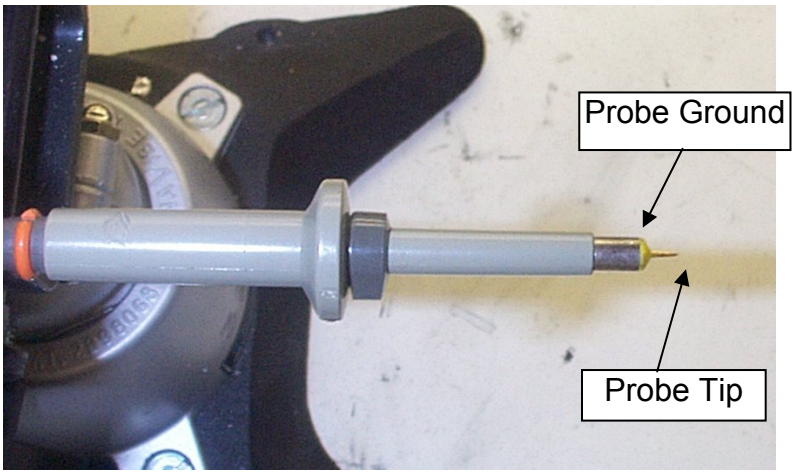


Figure 22 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

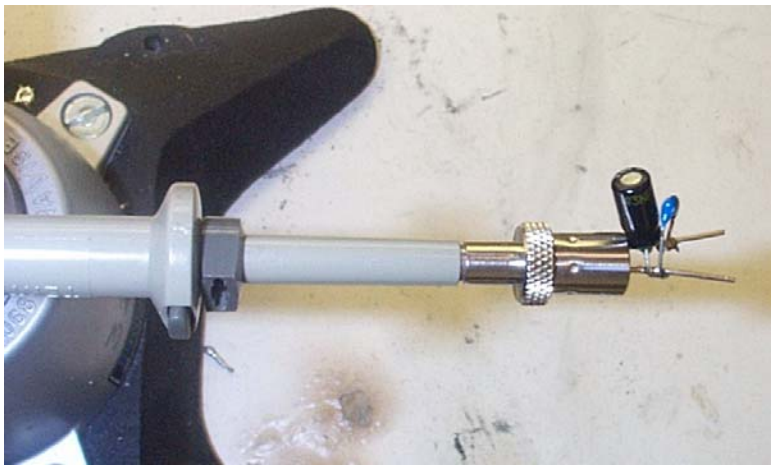


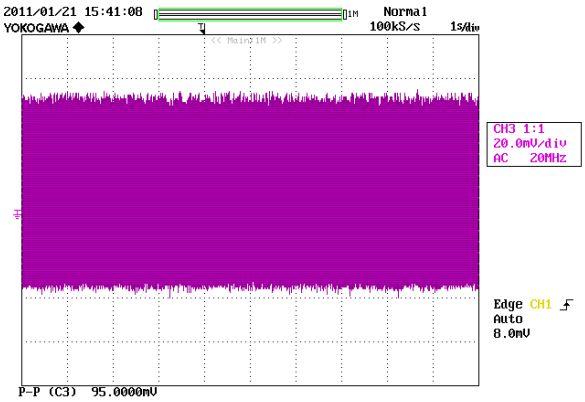
Figure 23 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

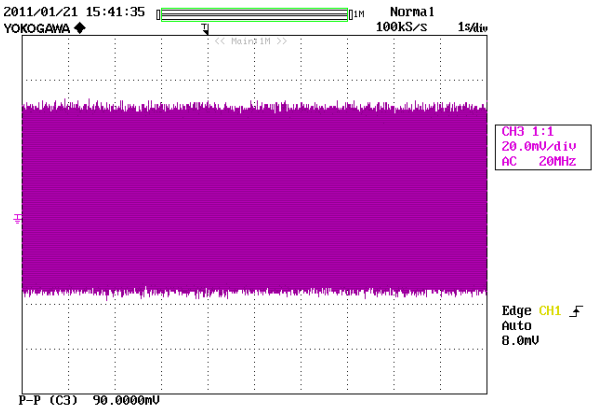
13.6.2 Ripple Measurement Results

Figure 24 – Ripple,85 VAC, Full load, 20 mV, 1 s / div.

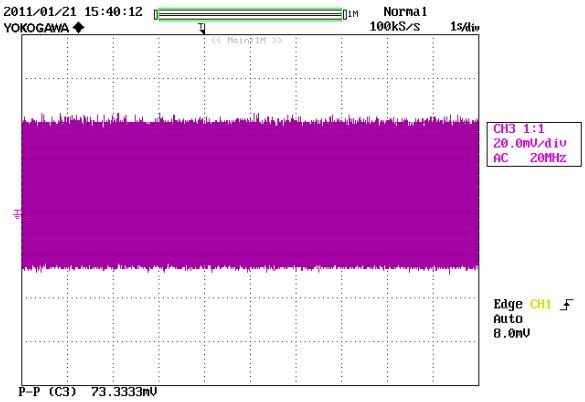
Figure 25 – Ripple, 265 VAC, Full Load, 20 mV, 1 s / div.

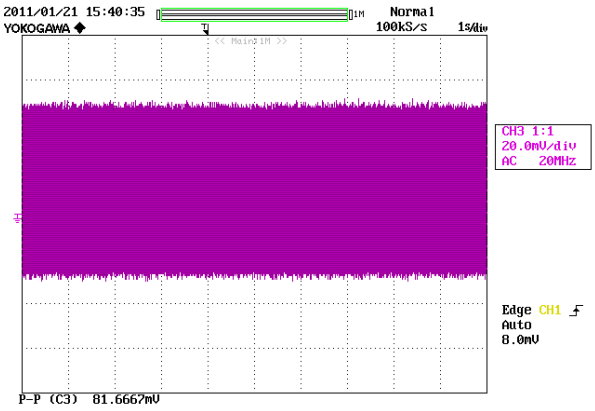
100% LOAD



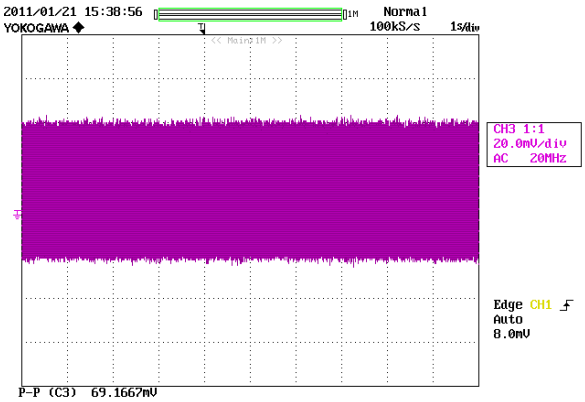


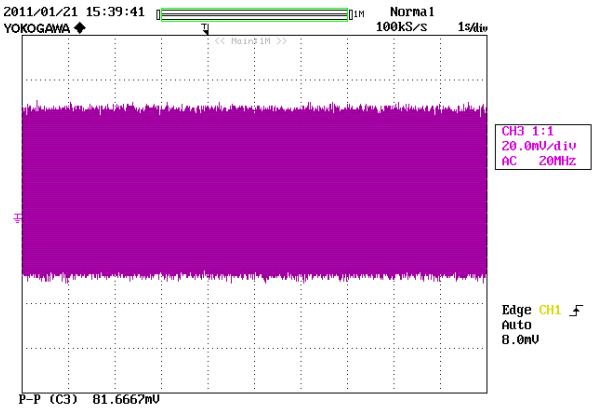
75% LOAD





50% LOAD





25% LOAD

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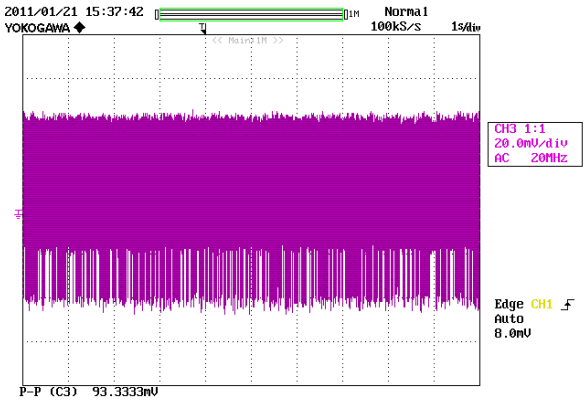
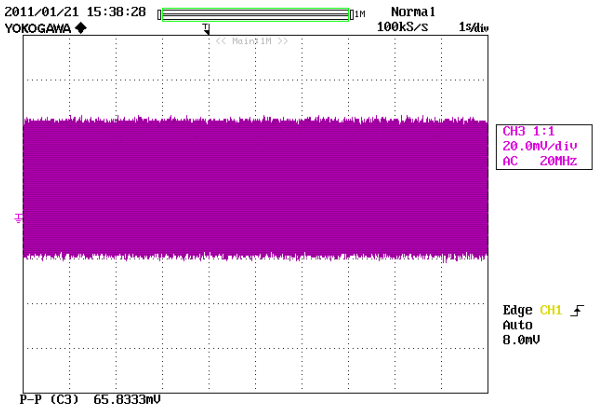
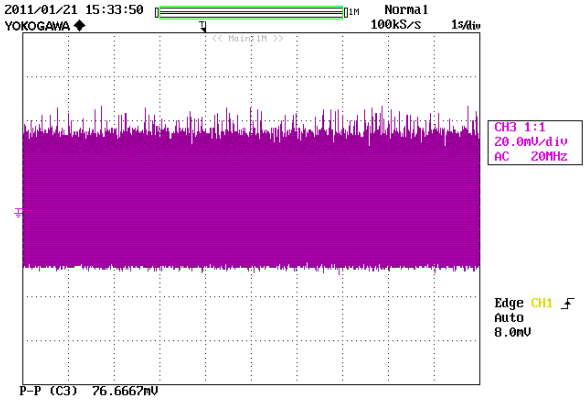
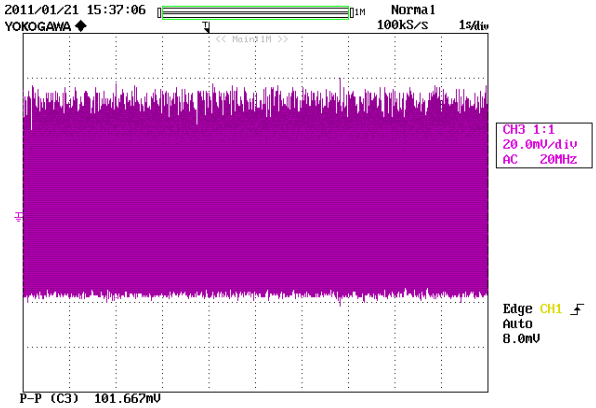

2011/01/21 15:37:42
YOKOGAWA
Normal
100kS/s
1s/div
CH3 1:1
20.0mV/div
AC 20MHz
Edge CH1
Auto
8.0mV
P-P (C3) 93.3333mV


2011/01/21 15:38:28
YOKOGAWA
Normal
100kS/s
1s/div
CH3 1:1
20.0mV/div
AC 20MHz
Edge CH1
Auto
8.0mV
P-P (C3) 65.8333mV

0 LOAD


2011/01/21 15:33:50
YOKOGAWA
Normal
100kS/s
1s/div
CH3 1:1
20.0mV/div
AC 20MHz
Edge CH1
Auto
8.0mV
P-P (C3) 76.6667mV


2011/01/21 15:37:06
YOKOGAWA
Normal
100kS/s
1s/div
CH3 1:1
20.0mV/div
AC 20MHz
Edge CH1
Auto
8.0mV
P-P (C3) 101.667mV

14 Line Surge Immunity

Differential input line 1.2 μs /50 μs/ 2 Ω surge testing to IEC61000-4-5 standards was completed on a single test unit. The input voltage was set at 230 VAC / 60 Hz. The output current was 1 A and operation was verified following each surge event.

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L - N	90	PASS
-1000	230	L - N	270	PASS

Common Mode input line 1.2 μs / 50 μs / 12 Ω surge testing to IEC61000-4-5 standards was completed on a single test unit. The input voltage was set at 230 VAC / 60 Hz. The output current was 1 A and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000	230	L, N - E	90	PASS
-2000	230	L, N - E	270	PASS

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15 Conducted EMI

LOAD: 5 Ω resistor load at end of 0.25 Ω output cable

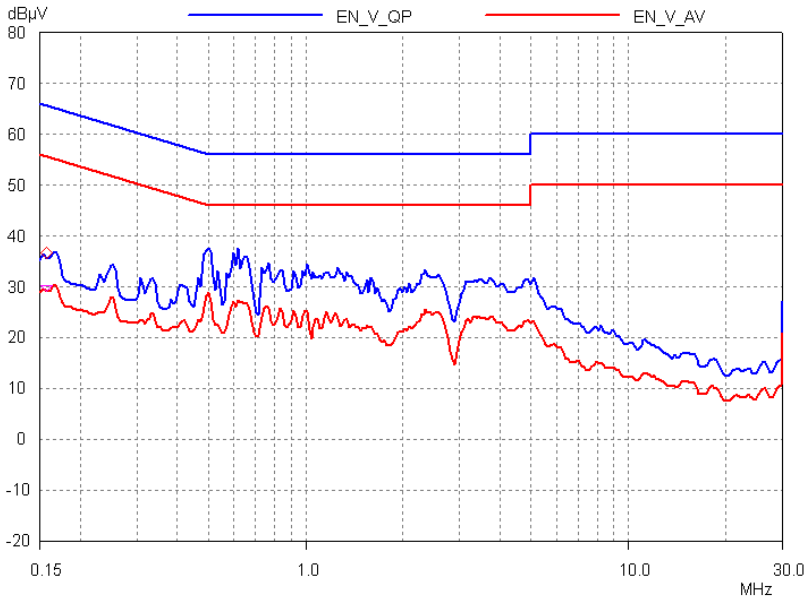

Figure 26 – 115 VAC Neutral, Output Artificial Hand NOT Connected.

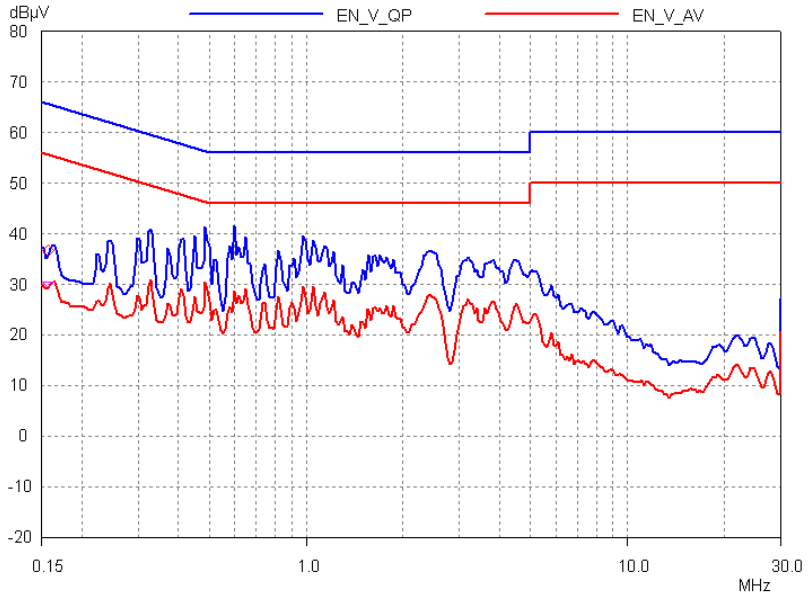

Figure 27 – 230 VAC Neutral, Output Artificial Hand NOT Connected.

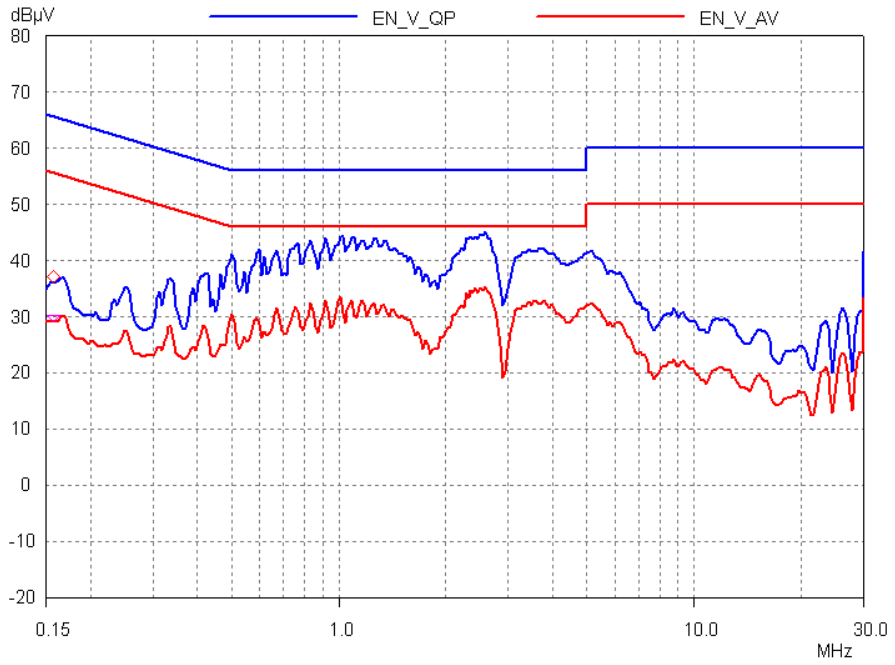

Figure 28 – 115 VAC Neutral, Output Artificial Hand Connected.

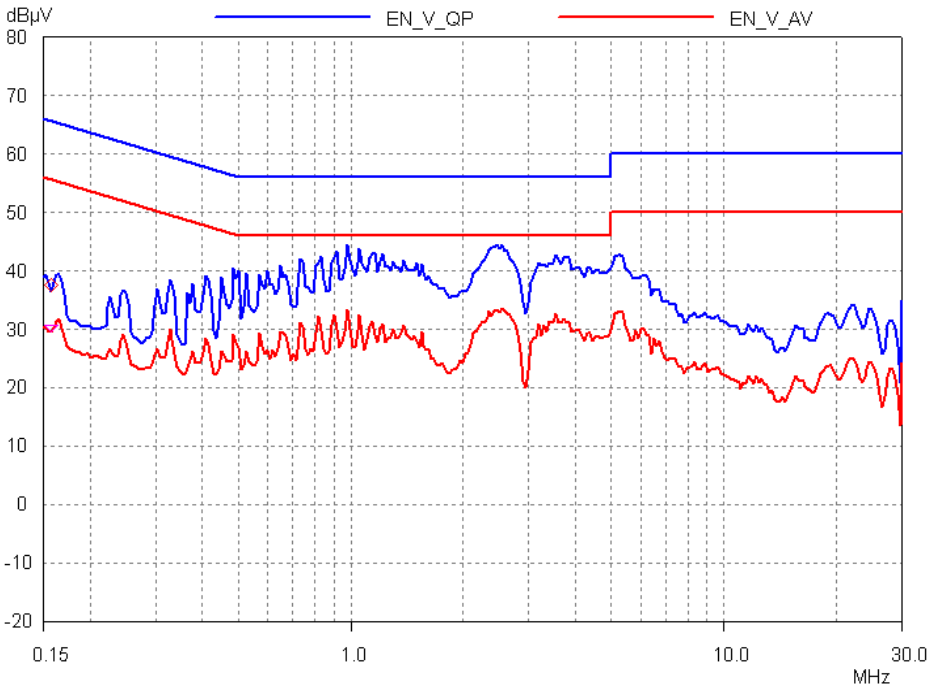

Figure 29 – 230 VAC Neutral, Output Artificial Hand Connected.

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
04-Feb-11	ME	1.0	First release	Apps & Mktg
09-Feb-11	ME	1.1	Added Section 13.5 Common Mode Voltage Set-up Diagram	

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