Design Example Report

Title	***2.75 W Single Output, Isolated Charger Using LNK363DN***
Specification	90 VAC – 264 VAC Input 5 V, 0.55 A, CVCC Output
Application	Cell Phone Charger
Author	Power Integrations Application Department
Document Number	DER-135
Date	September 5, 2007
Revision	1.0

Summary and Features

- Meets China USB Charger (CUC) Specifications
- Universal Input 90 to 264 VAC
- Input Power Consumption <200mW at 264 VAC
- Meets CISPR22B With No Y Cap
- Meets CEC Efficiency Requirement
- Provides CV/CC characteristic even with output short circuit

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 5 V, 0.55 A power supply utilizing a LNK363 in a SO8 package. The design has an USB connector and is intended to be used as a cell phone battery charger or supply for other applications that draw power via a USB port.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

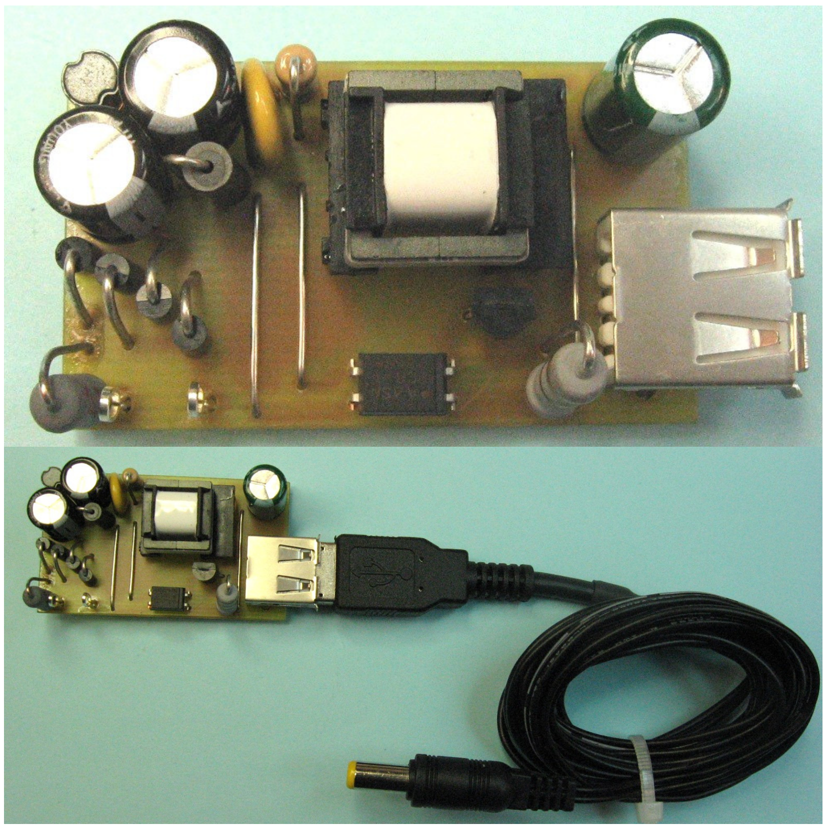

Figure 1 – Populated Circuit Board Photograph. With/ Without Output Cable Used to Measure Performance.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.3	W	
Output						
Output Voltage	$V_{OUT(CV)}$	4.75	5.00	5.25	V	Unit operating in CV mode measured at end of 0.17 Ω cable
	$V_{OUT(CC)}$	0		5.25	V	Unit operating in CC mode measured at end of 0.17 Ω cable
Output Ripple Voltage	V_{RIPPLE}			100	mV	20 MHz bandwidth
Output Current	I_{OUT1}	0.5	0.55	0.8	A	In CC Mode
Total Output Power						
Continuous Output Power	P_{OUT}			2.75	W	
Efficiency						
Full Load	η	59			%	Measured at Full Load 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{CEC}	58.10			%	Per California Energy Commission (CEC) / Energy Star requirements
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				Output floating or earth grounded
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Differential Mode		1			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Surge Common Mode		2			kV	
Ambient Temperature	T_{AMB}	-10		40	°C	Free convection, sea level, enclosed adapter

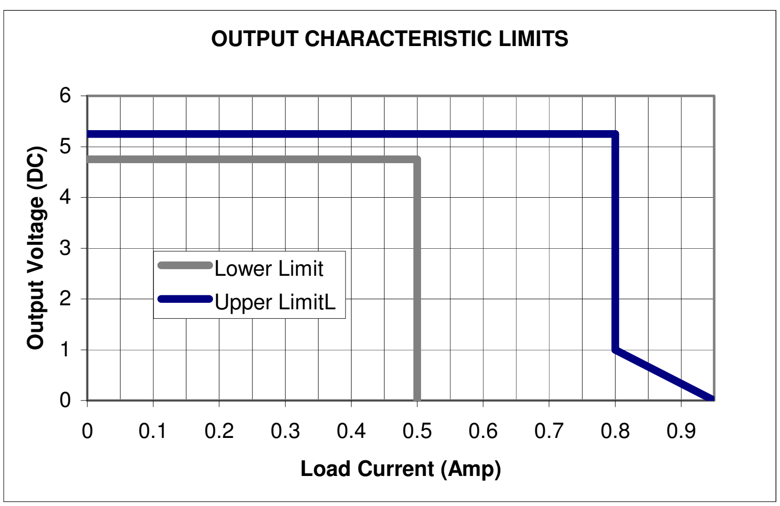

Figure 2 – Output Characteristic Limits.

3 Schematic

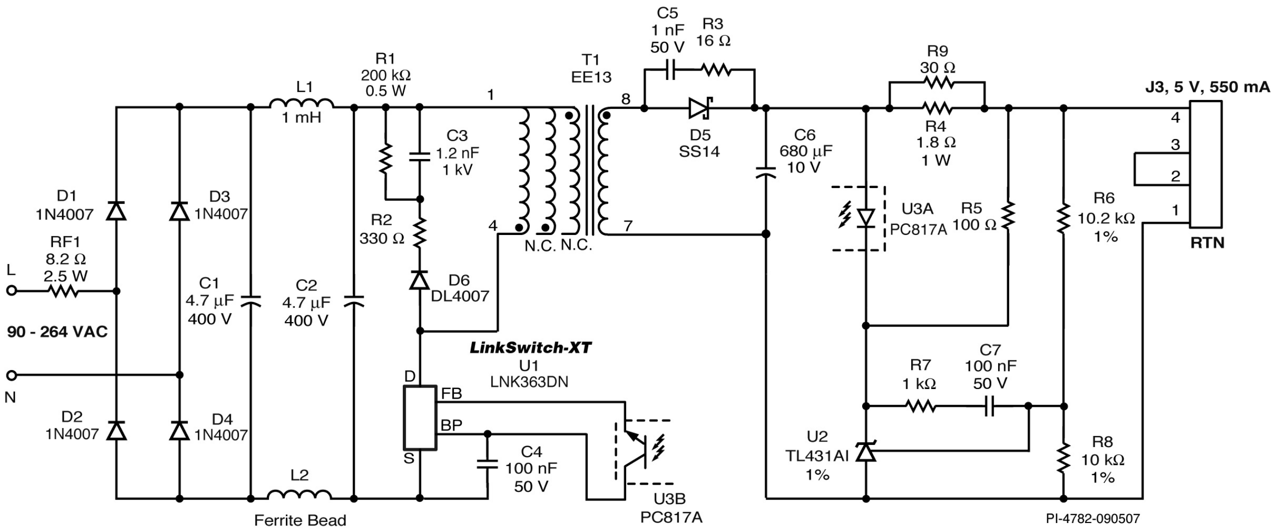

Figure 3 – Schematic.

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4 Circuit Description

The Flyback power supply shown in Figure 3 was designed around the LNK363D (U1). It is a constant voltage constant current (CVCC) power supply intended for use in a Universal Serial Bus (USB) charger.

4.1 Input Rectification and EMI Filtering

Diodes D1-D4 rectify the AC input voltage. Capacitors C1 and C2 filter the rectified AC input voltage. Inductor L1 and Ferrite bead L2 are used to provide differential mode filtering for EMI compliance.

4.2 LinkSwitch Primary

The LNK363DN device integrates the oscillator, controller, startup and other protection circuitry as well as the high voltage MOSFET on a single monolithic IC. Suffix D indicates the SO-8 package and the second suffix N indicates lead-free RoHS compliant device.

The LNK363 operates at a constant current limit while providing cycle by cycle limitation of primary current. It maintains output regulation by skipping switching cycles. The internal controller regulates the output voltage by skipping switching cycles (ON/OFF control) whenever the output voltage is above the reference level. During normal operation, MOSFET switching is disabled whenever the current flowing into the FEEDBACK (FB) pin is greater than 49 µA. If a current less than 49 µA flows into the FB pin when the oscillator's (internal) clock signal occurs, MOSFET switching is enabled for that particular switching cycle and the MOSFET turns on. That switching cycle terminates when the current through the MOSFET reaches I_{LIMIT}. The controller also has a maximum duty cycle (DC_{MAX}) signal that will turn the MOSFET off if I_{LIMIT} is not reached before the time duration equal to maximum duty cycle has elapsed.

At full load, few switching cycles will be skipped (disabled), resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the LinkSwitch-XT family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a fairly consistent efficiency over most of the load range.

4.3 Output Rectification

Diode D5 rectifies the output from transformer T1. This rectifier is a low drop Schottky diode. Output filtering was provided by capacitor C6 which is a super low ESR type.

4.4 Output Feedback

The output voltage (CV portion) is regulated by the TL431 (U2), which is a 1% reference shunt regulator. Resistors R6 and R8, both 1% resistors, program the output voltage to 5V. Resistor R7 and capacitor C7 provide loop compensation. A feedback current proportional to the output current flows through the optocoupler diode (U3A). On the primary side, phototransistor (U3B) delivers this feedback current into the FB pin. Just before the start of each cycle, the LinkSwitch controller checks this FB pin current. If this current is greater than 49 µA, that switching cycle is disabled.

The constant current (CC) portion is provided by sensing the voltage across sense resistors R4 and R9. R5 provides fine-tuning. At the set CC current, the voltage across this resistor exceeds the diode drop, and cycle skipping reduces the output voltage to give the characteristic shown in Figure 9.

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5 PCB Layout

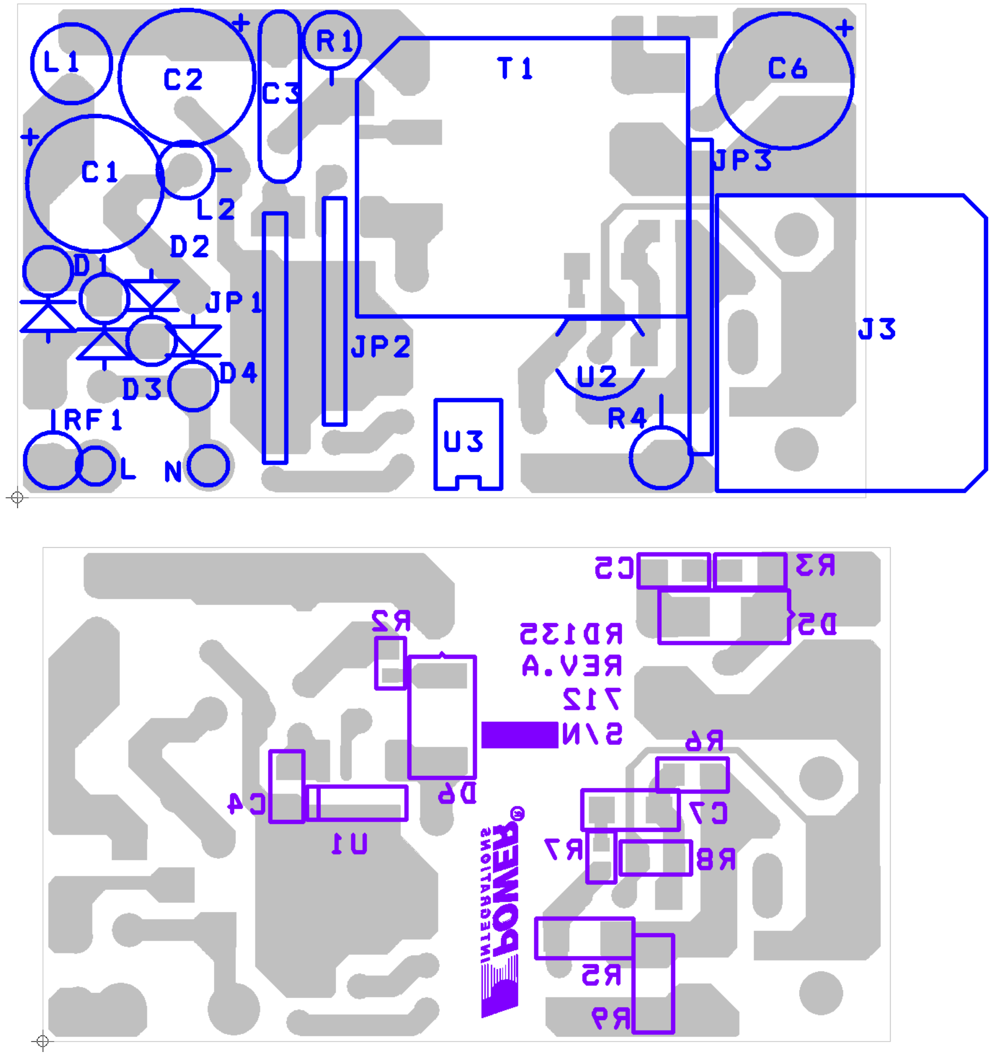

Figure 4 – Printed Circuit Layout.
Upper figure is silk screen top and bottom copper layers.
Lower figure is silk screen bottom and bottom copper layers.

6 Bill of Materials

Item	Part Ref	Qty	Value	Description	Mfg Part Number	Mfg
1	C1 C2	2	4.7 µF	4.7 uF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811 MLL3	Taicon Corporation
2	C3	1	1.2 nF	1.2 nF, 1 kV, Disc Ceramic	ECK-D3A122KBN	Panasonic
3	C4	1	100 nF	100 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H104K	Panasonic
4	C5	1	1 nF	1 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H102K	Panasonic
5	C6	1	680 µF	680 uF, 10 V, Electrolytic, Very Low ESR, 56 mOhm, (8 x 15)	EKZE100ELL681M H15D	Nippon Chemi-Con
6	C7	1	100 nF	100 nF, 50 V, Ceramic, X7R, 1206	ECJ-3VB1H104K	Panasonic
7	D1 D2 D3 D4	4	1N4007	1000 V, 1 A, Rectifier, DO-41	1N4007	Vishay
8	D5	1	SS14	40 V, 1 A, Schottky, DO-214AC	SS14	Vishay
9	D6	1	DL4007	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007	Diodes Inc
10	J3	1	CON4	CONN USB RTANG FMALE TYPE A PCB 4 Position (1 x 4	AU-Y1005	Assmann Electronics, INC.
11	JP1	1	J	Wire Jumper, Non insulated, 22 AWG, 0.7 in	298	Alpha
12	JP2	1	J	Wire Jumper, Non insulated, 22 AWG, 0.6 in	298	Alpha
13	JP3	1	J	Wire Jumper, Non insulated, 22 AWG, 0.8 in	298	Alpha
14	L1	1	1 mH	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
15	L2	1	Ferrite Bead (3.5 x 4.45 mm)	3.5 mm x 4.45 mm, 56 Ohms at 100 MHz, 22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
16	LINE	1	CON1	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
17	NTL	1	CON1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
18	R1	1	200 kΩ	200 k, 5%, 1/2 W, Carbon Film	CFR-50JB-200K	Yageo
19	R2	1	330 Ω	330 R, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ331V	Panasonic
20	R3	1	16 Ω	16 R, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ160V	Panasonic
21	R4	1	1.8 Ω	1.8 R, 5%, 1 W, Metal Oxide	RSF100JB-1R8	Yageo
22	R5	1	100 Ω	100 R, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ101V	Panasonic
23	R6	1	10.2 kΩ	10.2 k, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF1022V	Panasonic
24	R7	1	1 kΩ	1 k, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ102V	Panasonic
25	R8	1	10 kΩ	10 k, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF1002V	Panasonic
26	R9	1	30 Ω	30 R, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ300V	Panasonic
27	RF1	1	8.2 Ω	8.2 R, 2.5 W, Fusible/Flame Proof Wire Wound	CRF253-4 5T 8R2	Vitrohm
28	T1	1	EE13	Custom Transfomer, EE13, 8pins	548	Hical Magnetics
29	U1	1	LNK363DN	LinkSwitch-XT, LNK363DN, SO-8-DN	LNK363DN	Power Integrations
30	U2	1	TL431AI	2.495 V Shunt Regulator IC, 1%, 0 to 70C, TO-92	TL431AIP	Texas Instruments
31	U3	1	PC817A	Opto coupler, 35 V, CTR 80-160%, 4-DIP	PC817X1	Sharp

Note: Parts listed above are RoHS Compliant

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7 Transformer Design

7.1 Electrical Diagram

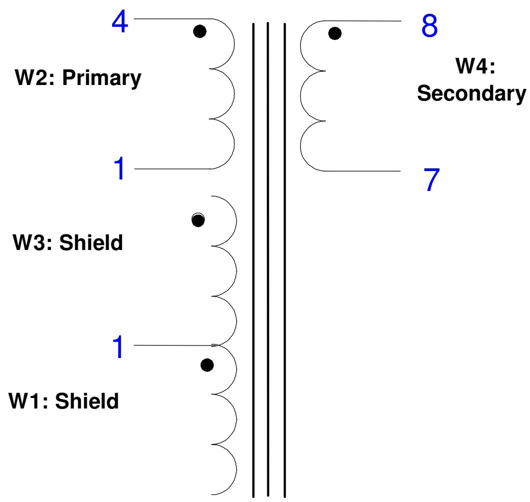

Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 second, 60 Hz, from Pins 1-4 to Pins 7-8	3000 VAC
Primary Inductance	Pins 1-4, all other windings open	1800 µH, -/+10%
Resonant Frequency	Pins 1-4, all other windings open	540kHz (Min.)
Primary Leakage Inductance	Pins 1-4, Pins 7-8 shorted.	94 µH (Max.)

7.3 *Material*

Item	Description
[1]	Core: PC44 EE13 Gapped for 71 nH/T^2
[2]	Bobbin: EE13, Horizontal, Hical Magnetics 548.
[3]	Magnet wire: #35 AWG, double coated.
[4]	Magnet wire: #37 AWG, double coated.
[5]	Magnet wire: #32 AWG, double coated.
[6]	Magnet wire: #26 AWG, Triple insulated.
[7]	Tape: 3M 1298 Polyester Film, 2 mils thick, 7.5mm wide.
[8]	Varnish.

7.4 Transformer Build Diagram

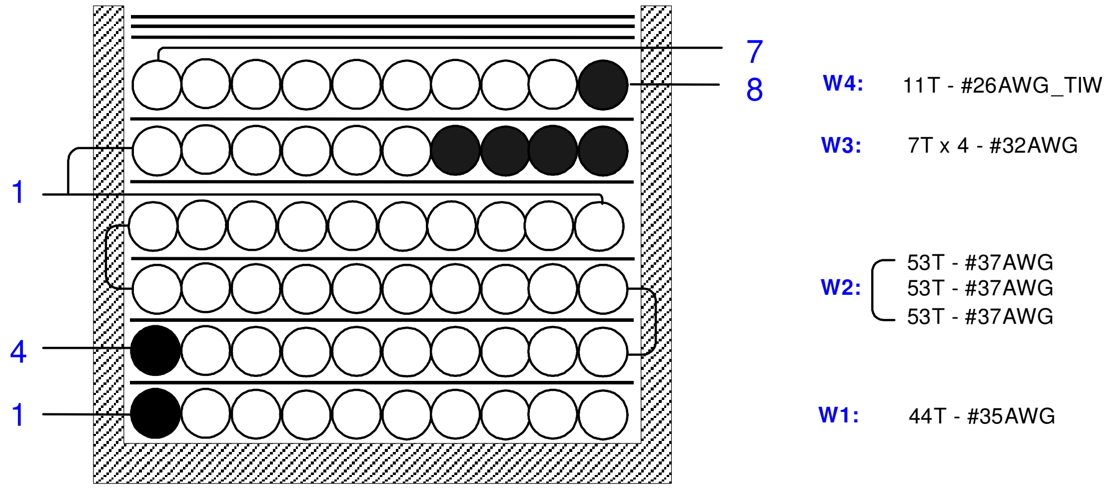

Figure 6 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Place the bobbin with primary pins on the left hand side. Winding direction is clockwise direction.
Winding 1: Shield	Start at pin 1, wind 44 turns of item [3] from left to right. Wind in a single uniform layer, and cut the finish end.
Insulation	1 layer of tape, item [7] for insulation.
Winding 2: Primary	Start at pin 4, wind 53 turns of item [4] from left to right , 1 layer of tape, item [7], continue wind another 53 turns from right to left, 1 layer of tape, item [7], continue wind another 53 turns from left to right. Place the wire with tight tension in a uniform winding. Terminate on pin 1.
Insulation	1 layer of tape, item [7] for insulation.
Winding 3: Shield	Temporary start at pin 7, wind 7 quad-filar turns of item [5] from right to left with tight tension, terminate at pin 1. Cut the start end.
Insulation	1 layer of tape, item [7] for insulation.
Winding 4: Secondary	Start at pin 8, wind 11 turns of item [6] from right to left with tight tension in a uniform winding. Terminate at pin 7.
Insulation	3 layer of tape, item [7] for insulation.
Finish	Varnish.

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8 Transformer Spreadsheet

ACDC_LinkSwitch-XT_090506; Rev.1.15; Copyright Power Integrations 2006	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-XT_090506_Rev1-15.xls; LinkSwitch-XT Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					XFR31
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	264			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	4.90			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.53			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	1.00			Volts	Voltage drop across sense resistor.
Output Cable Resistance			0.17	Ohms	Enter the resistance of the output cable (if used)
PO			3.14	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	Opto		Opto		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet.
Add Bias Winding	No		No		Choose 'YES' in the 'Bias Winding' drop down box at the top of this spreadsheet to add a Bias winding. Choose 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption.
Clampless design (LNK 362 only)	No		External Clamp		Choose 'YES' from the 'clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply.
n	0.60		0.6		Efficiency Estimate at output terminals
Z	0.75		0.75		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	9.40			uFarads	Input Capacitance
Input Rectification Type	F		*F*		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkSwitch-XT VARIABLES					
LinkSwitch-XT	**Auto**		**LNK363**		Recommended LinkSwitch-XT device
Chosen Device		*LNK363*			
ILIMITMIN			*0.195*	Amps	Minimum Current Limit
ILIMITMAX			*0.225*	Amps	Maximum Current Limit
fSmin			*124000*	Hertz	Minimum Device Switching Frequency
I^2fmin			4948	A^2Hz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	92.51		92.5090909	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-XT on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			1.08		Ripple to Peak Current Ratio (0.6 < KP < 6.0). For Clampless Designs use KP > 1.1
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE13**		**EE13**		User-Selected transformer core
Core		*EE13*		*P/N:*	PC40EE13-Z
Bobbin		*EE13_BOBBIN*		*P/N:*	EE13_BOBBIN
AE			0.171	cm^2	Core Effective Cross Sectional Area
LE			3.02	cm	Core Effective Path Length
AL			1130	nH/T^2	Ungapped Core Effective Inductance
BW			7.9	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3		Number of Primary Layers
NS			11		Number of Secondary Turns

NB			N/A		Bias winding not used
VB			N/A	Volts	Bias winding not used
PIVB			N/A	Volts	N/A - Bias Winding not in use
DC INPUT VOLTAGE PARAMETERS					
VMIN			98	Volts	Minimum DC Input Voltage
VMAX			373	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.49		Maximum Duty Cycle
IAVG			0.05	Amps	Average Primary Current
IP			0.20	Amps	Minimum Peak Primary Current
IR			0.20	Amps	Primary Ripple Current
IRMS			0.08	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1800	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			159		Primary Winding Number of Turns
ALG			71	nH/T^2	Gapped Core Effective Inductance
BM			1490	Gauss	Maximum Operating Flux Density, BM<1500 is recommended
BAC			745	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1588		Relative Permeability of Ungapped Core
LG			0.28	mm	Gap Length (Lg > 0.1 mm)
BWE			23.7	mm	Effective Bobbin Width
OD			0.15	mm	Maximum Primary Wire Diameter including insulation
INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.11	mm	Bare conductor diameter
AWG			37	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			20	Cmils	Bare conductor effective area in circular mils
CMA			266	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			2.82	Amps	Peak Secondary Current
ISRMS			1.07	Amps	Secondary RMS Current
IRIPPLE			0.93	Amps	Output Capacitor RMS Ripple Current
CMS			214	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			26	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.41	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.72	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.16	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			588	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			31	Volts	Output Rectifier Maximum Peak Inverse Voltage

Note – Transformer was dip-varnished to reduce audible noise to within imperceptible level.

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency. The measurements were done at the lead end of the output cable.

9.1 Efficiency

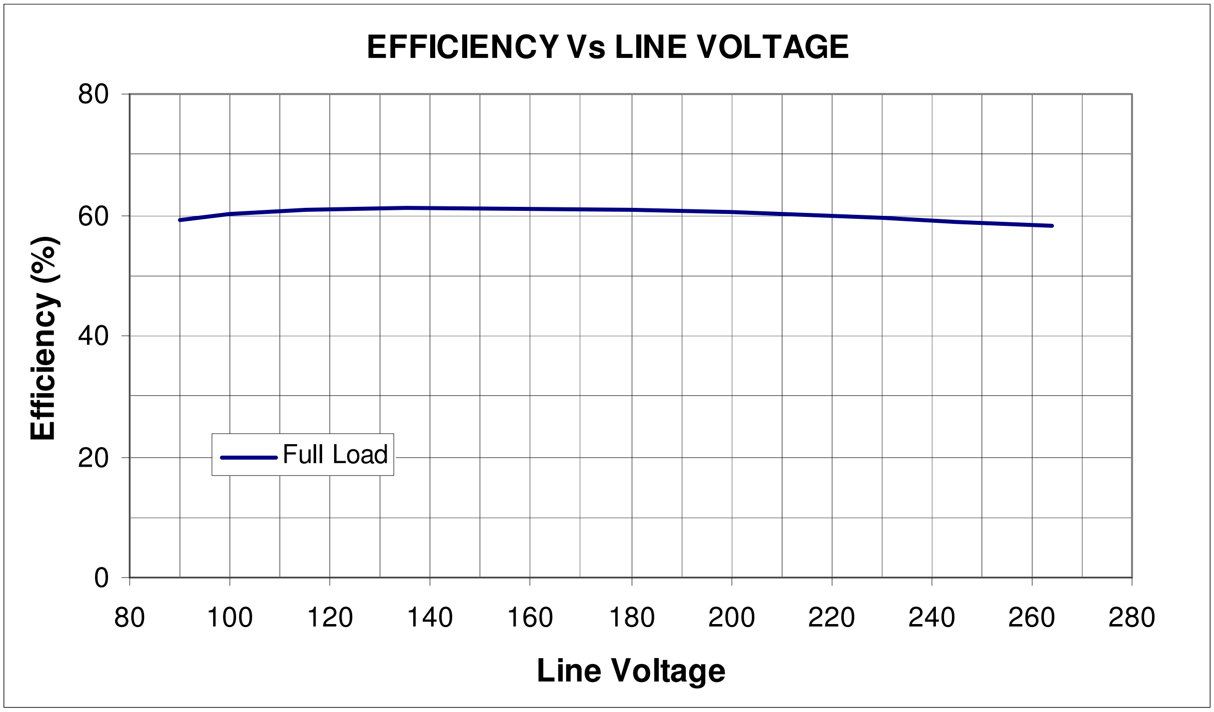

Figure 7 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

9.1.1 Active Mode CEC Measurement Data

All single output adapters, including those provided with products, for sale in California after Jan 1st, 2008 must meet the California Energy Commission (CEC) requirement for minimum active mode efficiency and no load input power. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of rated output power with the limit based on the nameplate output power:

Nameplate Output (P_O)	**Minimum Efficiency in Active Mode of Operation**
< 1 W	$0.49 \times P_O$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_O) + 0.5$ [ln = natural log]
> 49 W	0.85

For adapters that are single input voltage only, then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC); for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star standard.

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	63.01	58.79
50	64.79	61.88
75	63.45	61.54
100	61.60	59.77
Average	63.21	60.49
CEC specified minimum average efficiency (%)	59.10	

More states within the USA and other countries are adopting this standard; for the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2 No-load Input Power

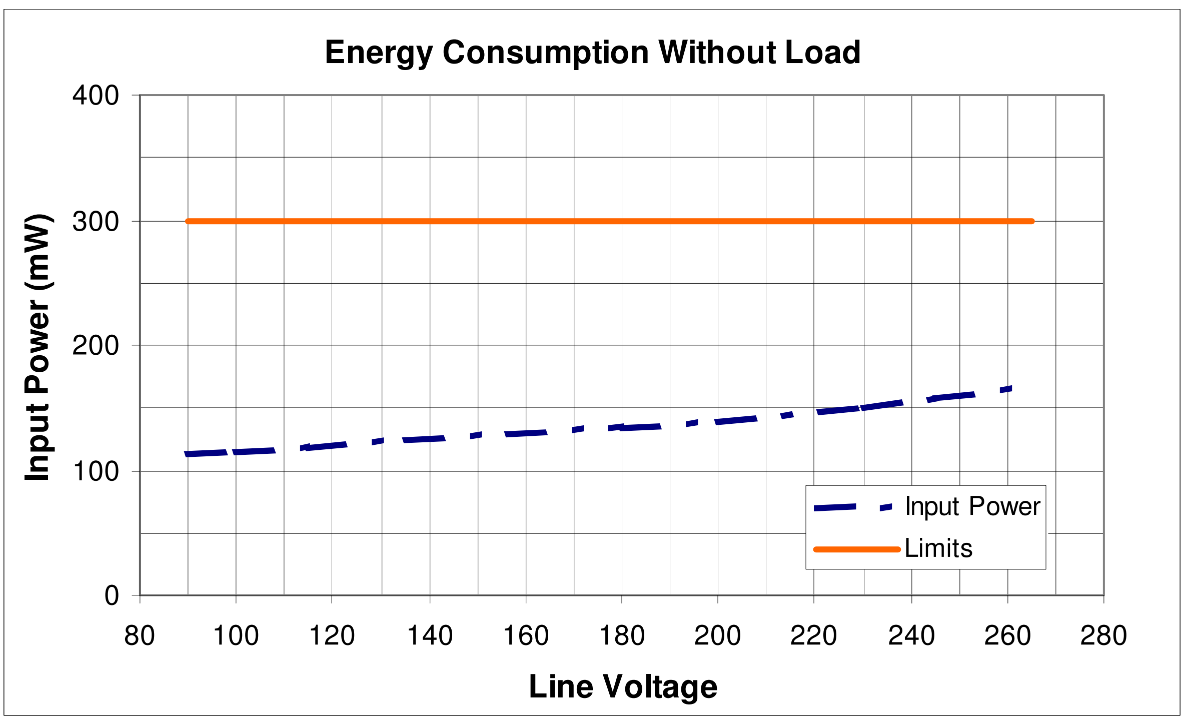

Figure 8 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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9.3 Regulation

9.3.1 Output Characteristic

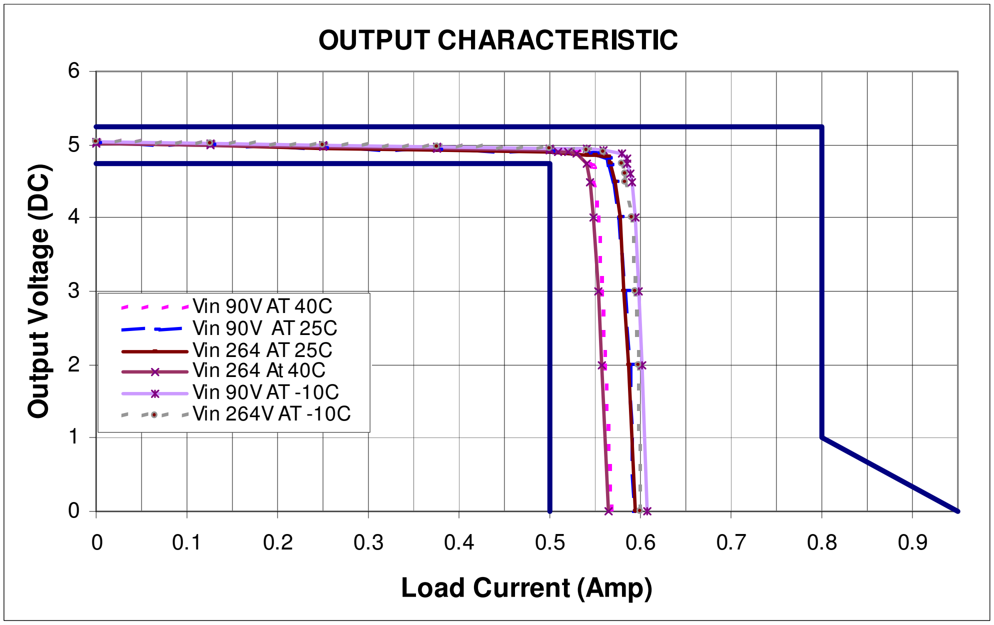

Figure 9 – Output Characteristic, Room Temperature.

9.3.2 Line

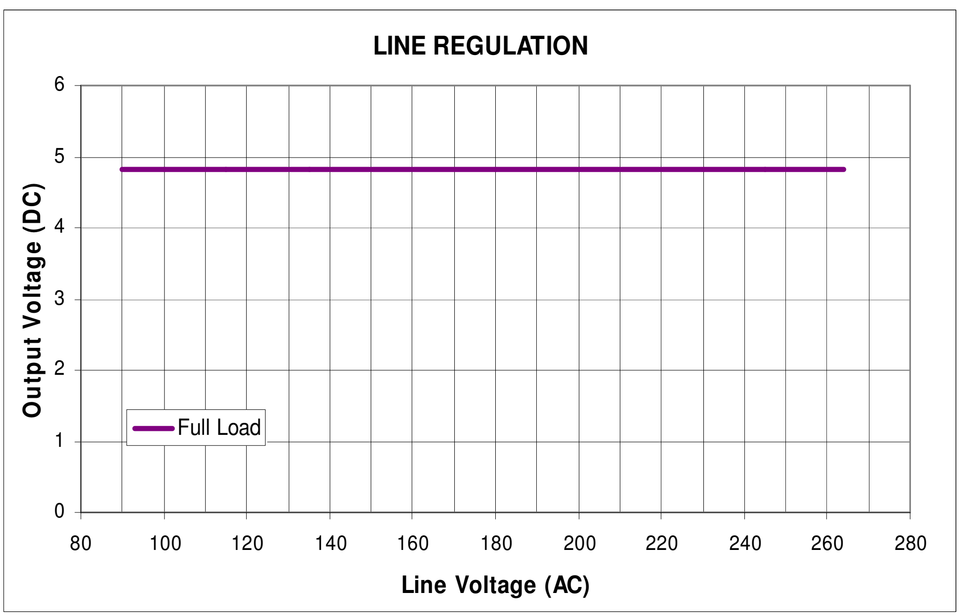

Figure 10 – Line Regulation, Room Temperature, Full Load.

10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

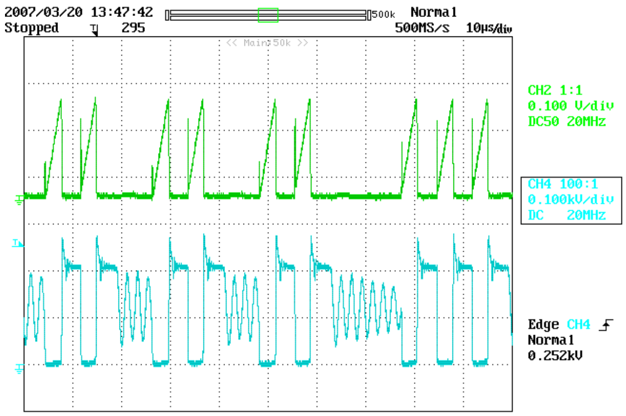

Figure 11 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.

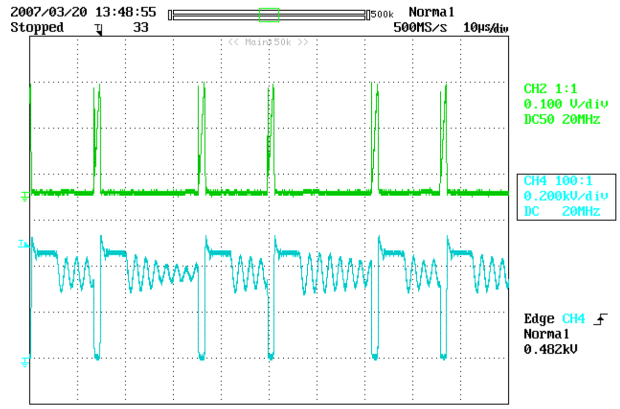

Figure 12 – 264 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 200 V, 10 µs / div.

10.2 Output Voltage Start-up Profile

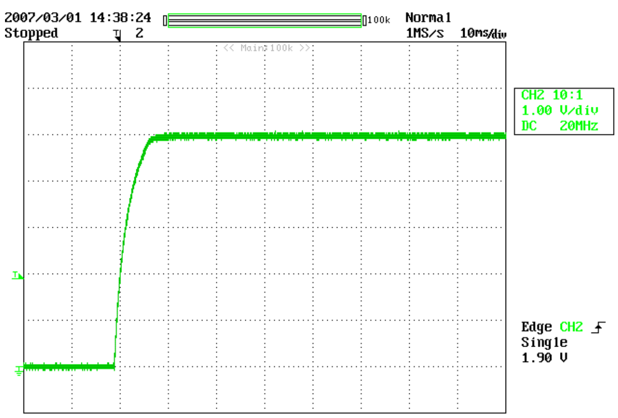

Figure 13 – Start-up Profile, 115 VAC
1 V, 10 ms / div.

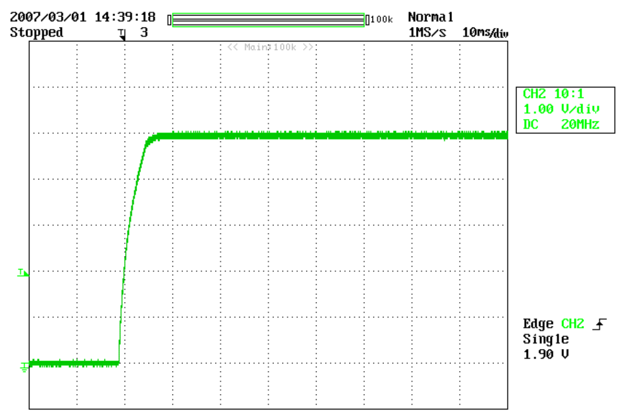

Figure 14 – Start-up Profile, 230 VAC
1 V, 10 ms / div.

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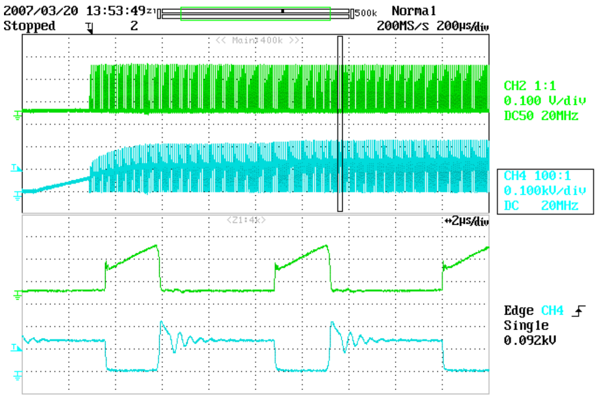
10.3 Drain Voltage and Current Start-up Profile



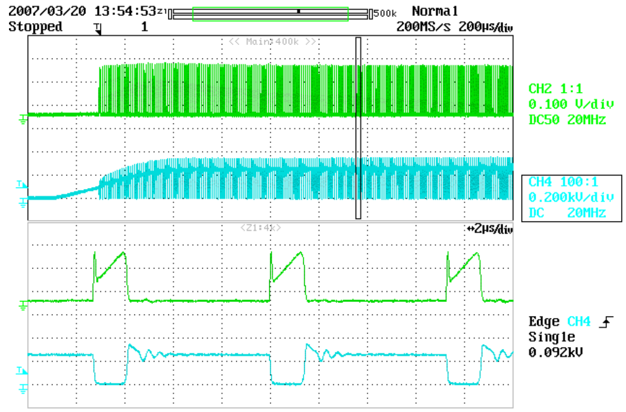
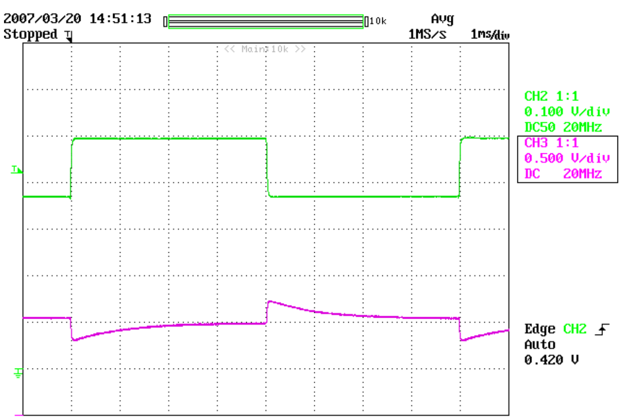


Figure 15 – 90 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div.

Figure 16 – 264 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 200 V div.

10.4 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.



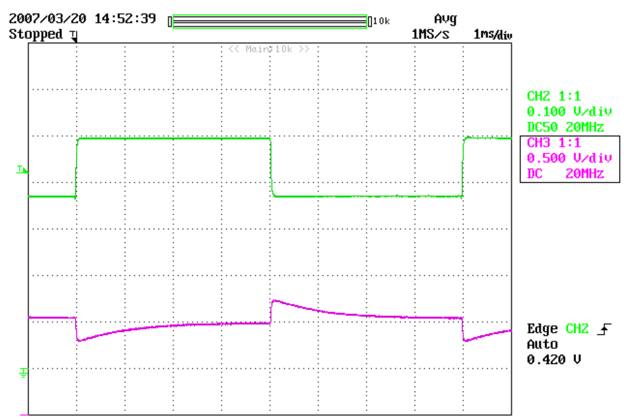


Figure 17 – Transient Response, 115 VAC, 75-100-75% Load Step.
Top: Load Current, 0.1 A/div.
Bottom: Output Voltage
500 mV / div.

Figure 18 – Transient Response, 230 VAC, 75-100-75% Load Step
Upper: Load Current, 0.1 A/ div.
Bottom: Output Voltage
500 mV / div.

10.5 Output Ripple Measurements

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

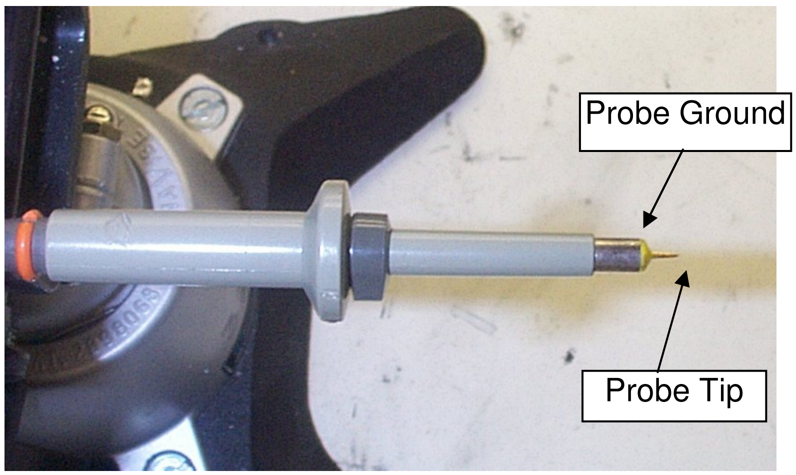


Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

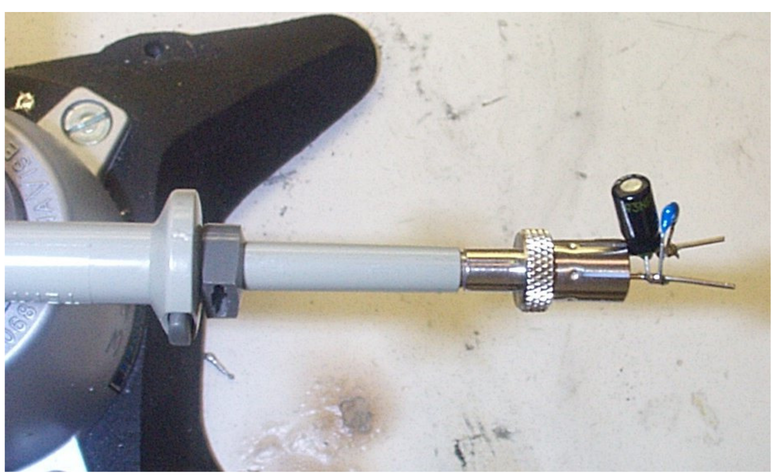


Figure 20 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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10.5.2 Measurement Results

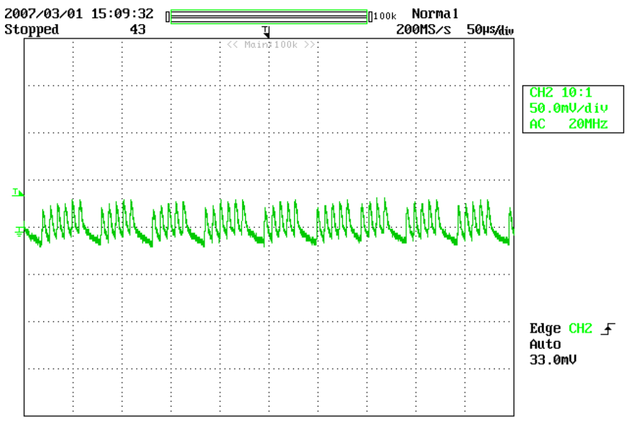

Figure 21 – Output Ripple, 90 VAC, Full Load.

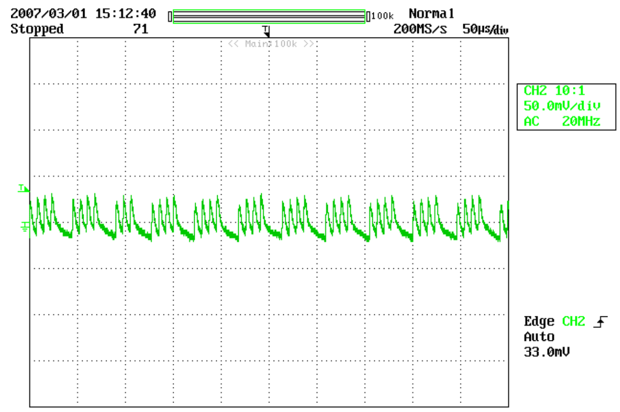

Figure 22 – Output Ripple, 115 VAC, Full Load.

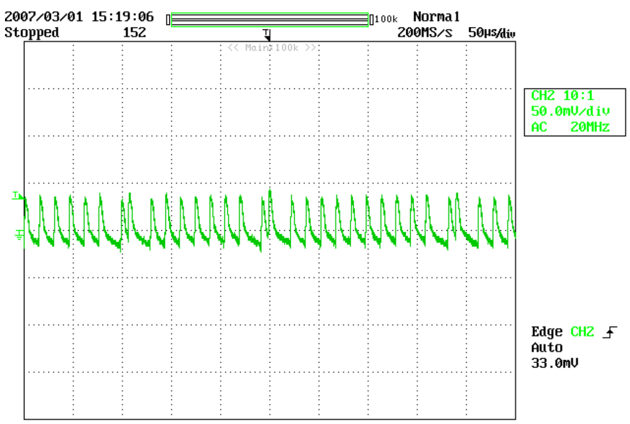

Figure 23 – Output Ripple, 230 VAC, Full Load.

11 Conducted EMI

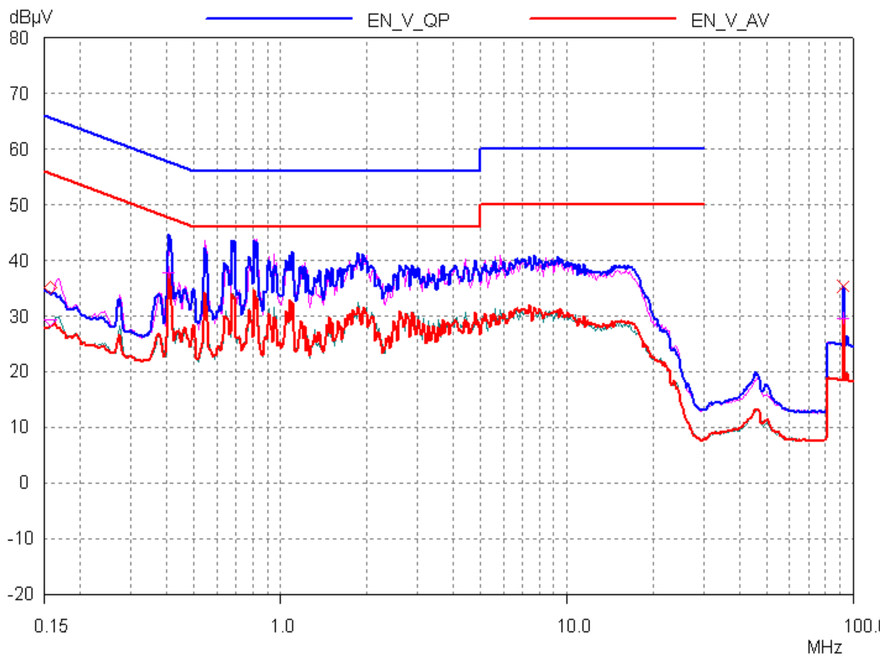

Figure 24 – Conducted EMI, Maximum Steady State, 115 VAC, 60 Hz and EN55022B Limits. Light Traces are for Noise Conducted Through the Neutral. Bold Traces are with Phase at L1.

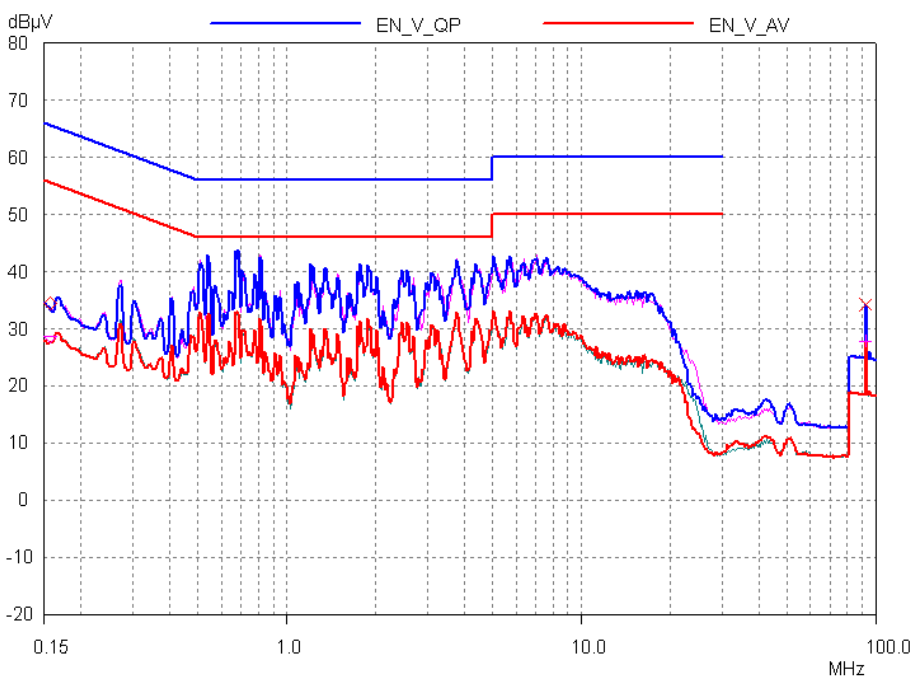

Figure 25 – Conducted EMI, Maximum Steady State, 230 VAC, 60 Hz and EN55022B limits. Light Traces are for Noise Conducted Through the Neutral. Bold Traces are with Phase at L1.

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12 Line Surge

Differential and Common mode 1.2/50 µs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load, and operation was verified following each surge event.

Surge	Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
1	+1000	230	L to N	90	Pass
2	+1000	230	L to N	90	Pass
3	+1000	230	L to N	90	Pass
4	+1000	230	L to N	90	Pass
5	+1000	230	L to N	90	Pass
6	+1000	230	L to N	90	Pass
7	+1000	230	L to N	90	Pass
8	+1000	230	L to N	90	Pass
9	+1000	230	L to N	90	Pass
10	+1000	230	L to N	90	Pass
1	-1000	230	L to N	270	Pass
2	-1000	230	L to N	270	Pass
3	-1000	230	L to N	270	Pass
4	-1000	230	L to N	270	Pass
5	-1000	230	L to N	270	Pass
6	-1000	230	L to N	270	Pass
7	-1000	230	L to N	270	Pass
8	-1000	230	L to N	270	Pass
9	-1000	230	L to N	270	Pass
10	-1000	230	L to N	270	Pass
1	+2000	230	L,N to GND	90	Pass
2	+2000	230	L,N to GND	90	Pass
3	+2000	230	L,N to GND	90	Pass
4	+2000	230	L,N to GND	90	Pass
5	+2000	230	L,N to GND	90	Pass
6	+2000	230	L,N to GND	90	Pass
7	+2000	230	L,N to GND	90	Pass
8	+2000	230	L,N to GND	90	Pass
9	+2000	230	L,N to GND	90	Pass
10	+2000	230	L,N to GND	90	Pass
1	-2000	230	L,N to GND	270	Pass
2	-2000	230	L,N to GND	270	Pass
3	-2000	230	L,N to GND	270	Pass
4	-2000	230	L,N to GND	270	Pass
5	-2000	230	L,N to GND	270	Pass

6	-2000	230	L,N to GND	270	Pass
7	-2000	230	L,N to GND	270	Pass
8	-2000	230	L,N to GND	270	Pass
9	-2000	230	L,N to GND	270	Pass
10	-2000	230	L,N to GND	270	Pass

Unit passes under all test conditions.

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
02-Mar-07	VC	0.1	First Draft	SGK
13-Mar-07	VC	0.2	Updated BOM, Added thermal data	SGK / PV
15-Mar-07	VC	0.3	Updated spreadsheet	SGK
20-Apr-07	SGK	0.4	Minor formatting	
24-Apr-07	VC	0.5	Updated L2	
01-Oct-07	KM	1.0	Initial Release	

Notes

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3911
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

JAPAN
Kosei Dai-3 Bldg.,
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-41138020
Fax: +91-80-41138023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

UNITED KINGDOM
1st Floor, St. James's House
East Street, Farnham
Surrey, GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
Rm A, B & C 4th Floor, Block C,
Electronics Science and
Technology Building, 2070
Shennan Zhong Rd,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY
Via De Amicis 2
20091 Bresso MI – Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760