Design Example Report

Title	***3.15W Adapter with < 100 mW standby using LNK500P***
Specification	Input: 90 – 264 VAC Output: 4.5V / 0.7A
Application	General Purpose Power Adapter
Author	Power Integrations Applications Department
Document Number	DER-111
Date	October 26, 2005
Revision	1.0

Summary and Features

- No load power consumption ~89 mW @ 230 V
- Uses LNK500
- Low cost, low parts count
- No Y-cap needed to meet CISPR-22 EMI
- Very low AC leakage current

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is an engineering report describing a 4.5 VDC, 700 mA CV adapter utilizing a LNK500P.

The LNK500P is implemented as a low-side switch. Cancellation techniques are adopted in the transformer design to make the power supply meet EMI without Y capacitors.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

2 Photograph

Figure 1 – Populated Circuit Board Photograph

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3 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.1	W	
Output						
Output Voltage 1	V_{OUT1}		4.5		V	±7%
Output Ripple Voltage 1	$V_{RIPPLE1}$			100	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}			0.7	A	
Efficiency	η		72		%	Measured at P_{OUT} (43 W), 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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4 Schematic

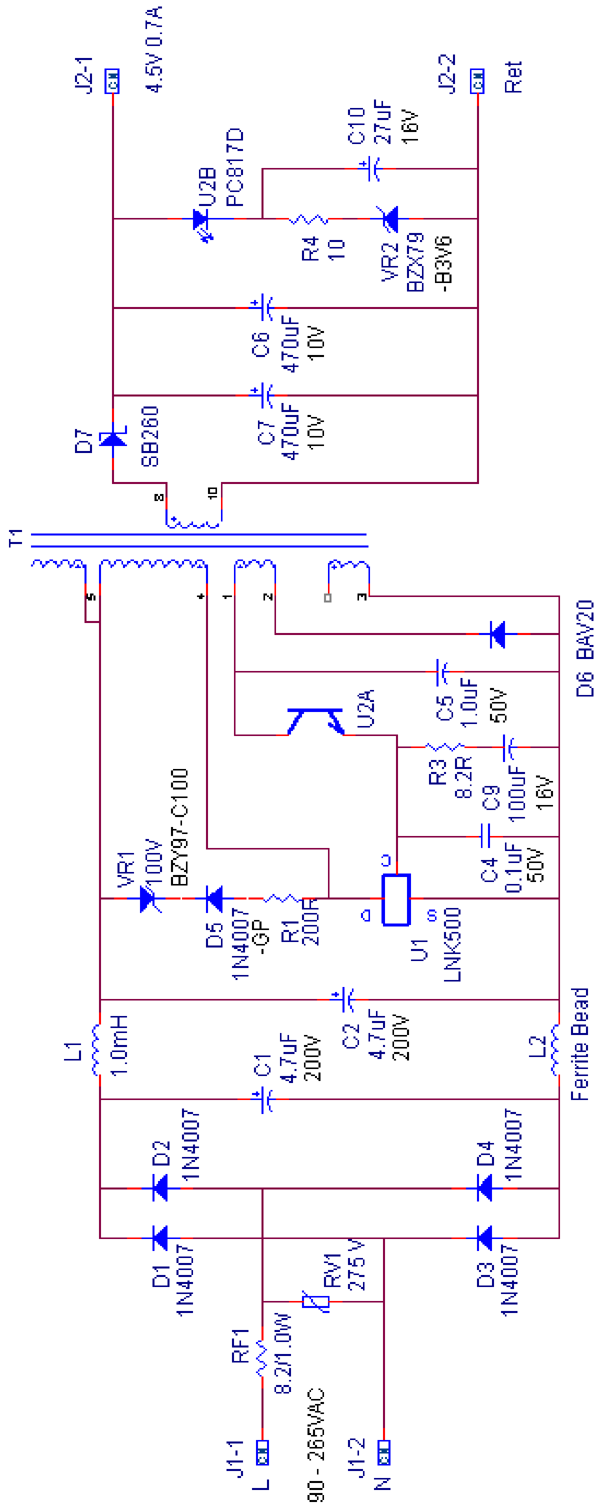

Figure 2 – Schematic

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5 Circuit Description

This circuit is configured as a Flyback operating in discontinuous conduction mode. The low standby consumption is achieved by using a high gain opto-coupler, using a bias winding that provides about 8 V during no-load, and by designing a low-capacitance transformer.

5.1 Input Rectification, Bulk Capacitance and EMI Filtering

AC input power is rectified by a full bridge, consisting of D1 through D4. The rectified DC is then filtered by the bulk storage capacitors C1 and C2. Inductor L1 and Ferrite bead L2 separate C1 and C2 from each other. L1, C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI noise. Fusible resistor RF1 has multiple functions. It is a fuse, an in-rush current limiting device, a final low pass filter stage (with C1) for conducted EMI attenuation and an initial stage of input surge voltage attenuation.

5.2 Primary DRAIN Voltage Clamp Circuit

The DRAIN voltage clamp circuit is comprised of Zener diode VR1, R1 and diode D5. D5 and VR1 clamp the amplitude of the voltage spike that the transformer leakage inductance generates, at switch turn-off, to keep it beneath the device's maximum DRAIN to SOURCE voltage rating (700 V). R1 damps the high frequency ringing caused by leakage inductance, which improves the conducted EMI performance of the circuit. The reflected output voltage V_{OR}, which is determined by the transformer turns ratio (13:1), has been kept low (70 V) to minimize the power dissipation in the clamp circuit.

5.3 Auxiliary Bias Supply

The auxiliary bias supply circuit is made up of the primary-side transformer bias winding, diode D6 and capacitor C5. D6 rectifies the output of the winding and C5 filters it. The winding was given just enough turns so that its minimum output voltage stays at 7V at no-load to minimize power consumption. C4 is the standard BP pin decoupling capacitor, which should always be a 50 V 0.1µF ceramic capacitor that is located close to the IC. R3 and C9 are compensation network, along with the Linkswitch Control pin resistance, form a pole and a zero to stabilize the control loop.

5.4 Output Rectification and Filtering

Output rectification and filtering are accomplished by Schottky diode D7, capacitors C6 and C7. D7 rectifies the output of the transformer, T1.

5.5 Output Voltage Sensing and Feedback

Resistors R4, Zener diode VR2 and opto-isolator U2 sense the output voltage and feedback to the LinkSwitch. C10 provides power for the LinkSwitch during the time of power up, it also acts as a soft start capacitor.

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6 PCB Layout

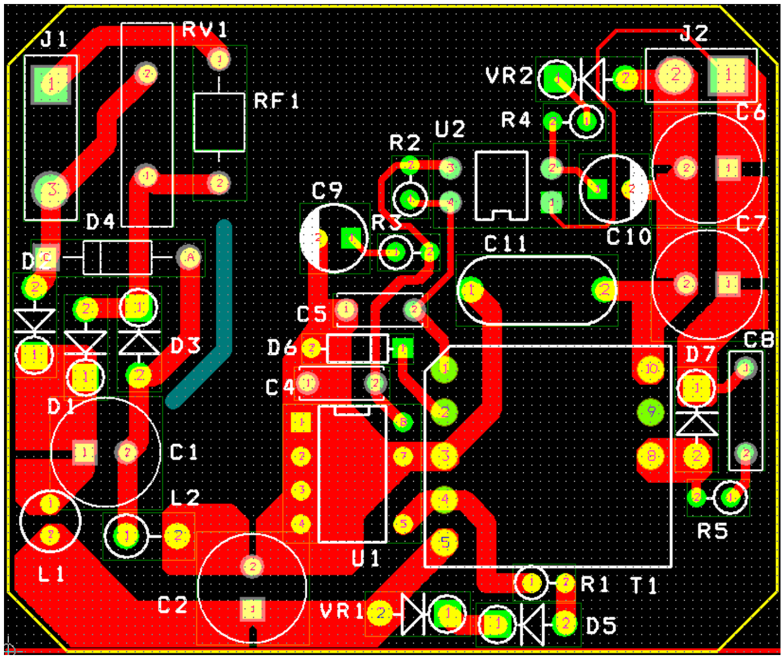

Figure 3 – Printed Circuit Layout

Note: R2, R5, C8 and C11 are not stuffed.

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7 Bill Of Materials

Item	Qty	Ref	Description	P/N	Mfg
1	2	C1, C2	4.7uF/200V, Electrolytic cap		Any
2	1	C4	0.1uF/50V, ceramic		Any
3	1	C5	1.0uF/50V, electrolytic		Any
4	2	C6, C7	470uF/10V, electrolytic cap low esr		Any
5	1	C9	100uF/16V, electrolytic cap		Any
6	1	C10	27uF/16V, electrolytic cap		Any
7	4	D1-D4	1A/1000V, general diode	1N4007	Diode
8	1	D5	1A//1000V, glass passive	1N4007G	Philips
9	1	D6	0.25A/200V	BAV20	Vishay
10	1	D7	2.0A/60V, schottky diode	SB260	ANY
11	1	VR1	100V TVS	BZY97-C100	Any
12	1	VR2	3.6V 2% zener diode	BZX79B3V6	Any
13	1	L1	1.0 mH	47HY102	Tokin
14	1	L2	Ferrite bead		Any
15	1	RF1	8.2R, 1W, fusible		Any
16	1	RV1	MOV, 275V, 14mm		Any
17	1	R1	200R, 1/4W		Any
18	1	R3	8.2R, 1/8W		Any
19	1	R4	10R, 1/8W		Any
20	1	T1	EE16 customized transformer		
21	1	U1	LNK500P		PI
22	1	U2	Opto-coupler	PC817D	Sharp

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8 Transformer Specification

8.1 Electrical Diagram

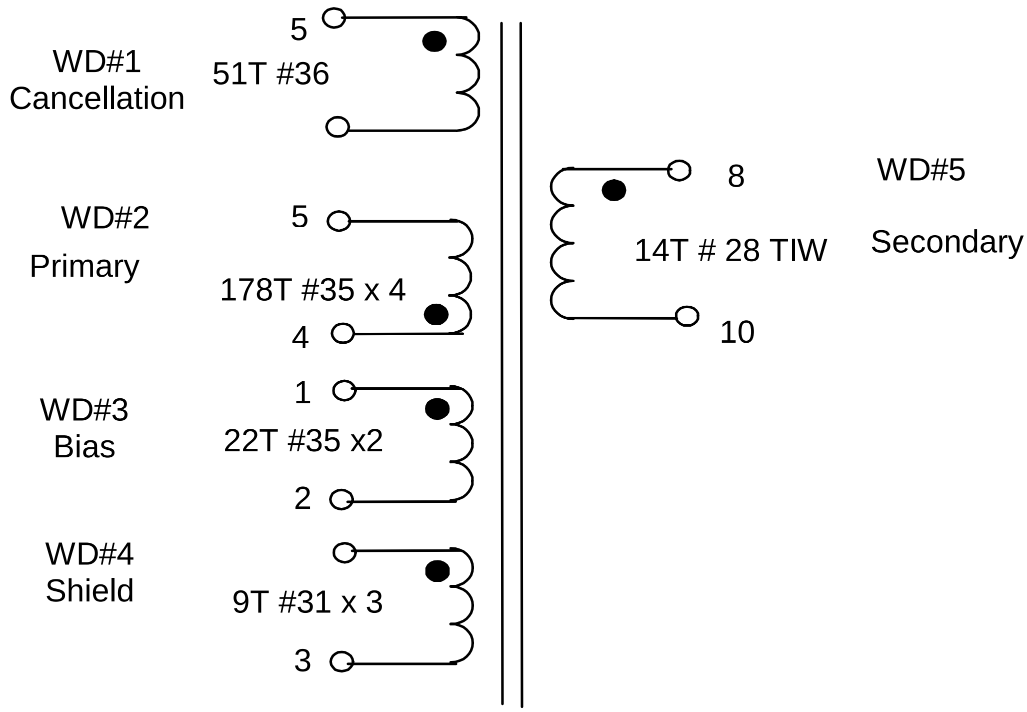

Figure 4 – Transformer Electrical Diagram

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1 - 5 to Pins 6 -10	3000 VAC
Primary Inductance	Pins 4-5, all other windings open, measured at 42 kHz, 0.4 VRMS	4.44 mH, -10/+10%
Resonant Frequency	Pins 4-5, all other windings open	300 kHz (Min.)
Primary Leakage Inductance	Pins 4-5, with Pins 8-10 shorted, measured at 42 kHz, 0.4 VRMS	200 μH (Max.)

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8.3 Materials

Item	Description
[1]	Core: PC40EE16-Z, TDK or equivalent Gapped for AL of 139 nH/T^2
[2]	Bobbin: Horizontal 10 pin
[3]	Magnet Wire: #36 AWG
[4]	Magnet Wire: #35 AWG
[5]	Magnet Wire: #31 AWG
[6]	Triple Insulated Wire: #28 AWG.
[7]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 8.4 mm wide
[8]	Varnish

8.4 Transformer Build Diagram

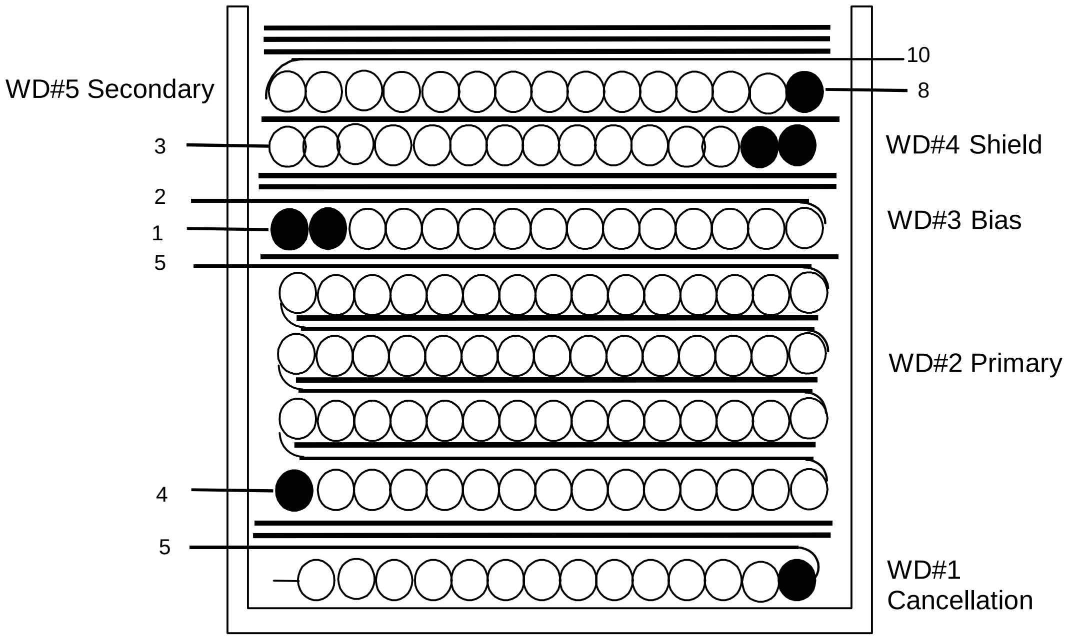

Figure 5 – Transformer Build Diagram

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8.5 Transformer Construction

Bobbin Preparation	Primary pin side of the bobbin orients to the left hand side.
WD1 Cancellation	Start on Pin 6 temporarily. Wind 51 turns of item [3] from right to left. Wind with tight tension across entire bobbin evenly. Cut the wire after finishing 51st turn. Fold the starting lead back and finish it on Pin 5.
Insulation	2 Layers of tape [7] for insulation
WD#2 Primary	Start on pin 4, wind 46 turns of item [4] from left to right. Apply one layer of type [7]. Then bring the wire back to left side, wind another 46 turns from left to right. Apply one layer of type [7]. Then bring the wire back to left side, wind another 46 turns from left to right. Apply one layer of type [7]. Then bring the wire back to left side, wind 40 turns from left to right. Apply one layer of type [7]. After finishing the 178th turn, bring the wire back and finish it on pin 5.
Insulation	1 Layers of tape [7] for insulation.
WD#3 Bias	Start on Pin 1, wind 11 bifilar turns of item [4]. Wind from left to right with tight tension. Wind uniformly, in a single layer across entire width of bobbin. Finish on Pin 2.
Insulation	2 Layers of tape [7] for insulation.
WD #4 Shield	Start at Pin 8 temporarily, wind 9 trifilar turns of item [5]. Wind from right to left with tight tension. Wind uniformly, in a single layer across entire width of bobbin. Finish on Pin 3. Cut the starting lead.
Insulation	1 Layers of tape [7] for insulation.
WD #5	Start at pin 8, wind 14 turns of item [6] from right to left. Wind uniformly, in a single layer across entire bobbin evenly. Finish on pin 10
Insulation	3 Layers of tape [7] for insulation.

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9 Transformer Spreadsheets

LinkSwitch 090803 rev1B; Copyright Power Integrations Inc. 2003	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**LinkSwitch 090803 rev1B; Copyright Power Integrations Inc. 2003**
ENTER APPLICATION VARIABLES					**EP12 Power Supply**
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	4.5			Volts	Output Voltage
IO	1			Amps	!!! Output Power exceeds chip capability; reduce load current, choose higher LinkSwitch
VBIAS	7				
tC	3			msec	Bridge Rectifier Conduction Time Estimate
CIN	**9.4**			uFarads	Input Filter Capacitor
TARGETED / ESTIMATED LOSSES					
P_NO_LOAD_GOAL	100		100	mW	Target noload losses must be in excess of 300mW
PCORE			225.2	mW	Estimated Core Losses at peak Flux Density (BP)
RCLAMP			380.0	Kohm	
CTRF			50.0	pF	
RSEC	0.1		0.1	Ohms	Estimated Resistance of transformer secondary winding.
P_NO_LOAD_LOSS			217	mW	Calculated no load loss is greater than goal. Decrease VOR, increase RCLAMP, decrease CTRF, decrease VBIAS.
DC INPUT VOLTAGE PARAMETERS					
VMIN			82	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
ENTER OUTPUT CABLE PARAMETERS					
RCABLE			0.3	Ohms	Resistance of total length of cable from power supply terminals to load and back.
VCABLE			0.300	Volts	Drop along cable connecting power supply to load
ENTER LinkSWITCH & OUTPUT DIODE VARIABLES					
LinkSwitch	**LNK501**			*Universal*	*115 Doubled/230*
			Power	*3*	*5*
I^2 f			2710	A^2 Hz	I^2 f (typical) co-efficient for LinkSwitch
VOR	70	*Increase Vor*	70.00	Volts	!!! Reflected output Voltage pushes power supply into continuous mode of operation; Increase VOR
VLEAK			2.00	Volts	Error in Feedback voltage as a result of leakage inductance in primary circuit.
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop (0.5~0.7V for schottky and 0.7~1.0V for PN diode)
VR			60	Volts	Rated Peak Rep Reverse Voltage of secondary diode
ID	2			Amps	Rated Average Forward current for secondary diode
DISCONTINUOUS MODE CHECK					
KDP			0.57		Ensure KDP > 1.15 to for discontinuous mode operation.
TON			14.69	us	Linkswitch conduction time
TDON			16.02	us	Secondary Diode conduction time
VOLTAGE STRESS ON LinkSWITCH AND OUTPUT DIODE					
VDRAIN			542	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			33.9	Volts	Output Rectifier Maximum Reverse Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					

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DMAX			0.62		Maximum Operating Duty Cycle
IAVG			0.078	Amps	Average Primary Current
IRMS			0.115	Amps	Primary RMS Current
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**ee16**				
Core		*PC40EE16-Z*			
Bobbin		*BE-16-116CP*			
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
VE			795	mm^3	Effective Core Volume
BW			8.5	mm	Bobbin Physical Winding Width
KCORE			552	kW/m^3	Core losses per unit volume
T(n)	0.922		0.9220		Estimated transformer efficiency. T(n)=(PSCU+PCORE/2)/POEFF. Re-iterate with n = 0.9406
M			0	mm	Safety Margin Width
NS	**14**				Number of Secondary Turns
TRANSFORMER PRIMARY DESIGN PARAMETERS					
dLP	1		1.000		Constant to account for reduction of inductance at higher flux densities. (0.999<dLP<1.05)
LP			4415	uHenries	Primary Inductance
L	4		**4**		Number of Primary Layers
LBIAS	0.25		**0.25**		
NP			**178**		Primary Winding Number of Turns
NB			**15**		
ALG			139	nH/T^2	Gapped Core Effective Inductance
BP			**3446**	Gauss	Peak Flux Density (BP<3500)
LG			0.15	mm	Core Gap Length for primary inductance
OD			0.19	mm	Maximum Primary Wire Diameter including insulation to give specified number of layers.
DIA			0.15	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CMA			**278**	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
AWG_BIAS			23	AWG	
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			3.23	Amps	Peak Secondary Current
ISRMS			1.53	Amps	Secondary RMS Current
IRIPPLE			1.16	Amps	Output Capacitor RMS Ripple Current
AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.36	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.61	mm	Secondary Maximum Insulated Wire Outside Diameter
INSS			0.12	mm	Maximum Secondary Insulation Wall Thickness
VSEC			0.100	Volts	Voltage Drop across secondary winding

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10 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

10.1 Efficiency

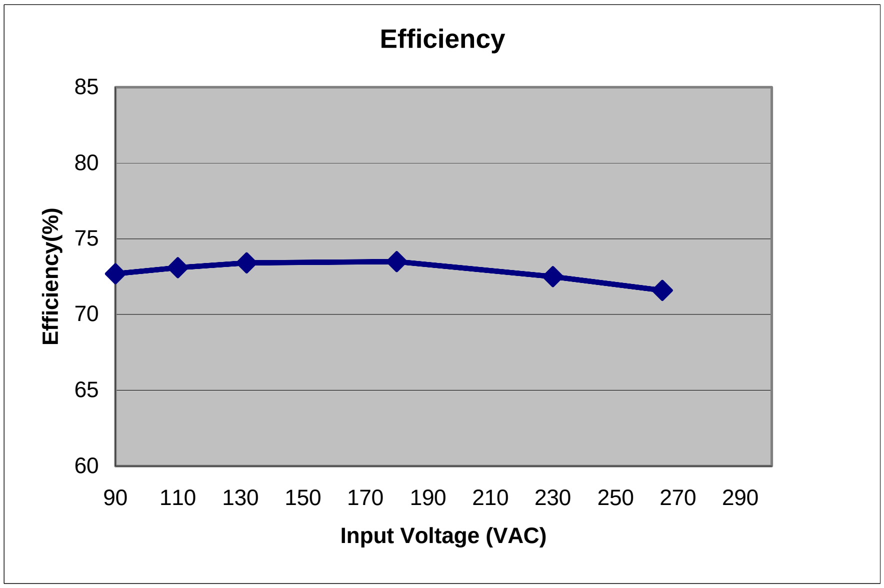

Figure 6 – Efficiency vs. Input Voltage at full load, Room Temperature, 60 Hz.

10.2 No-load Input Power

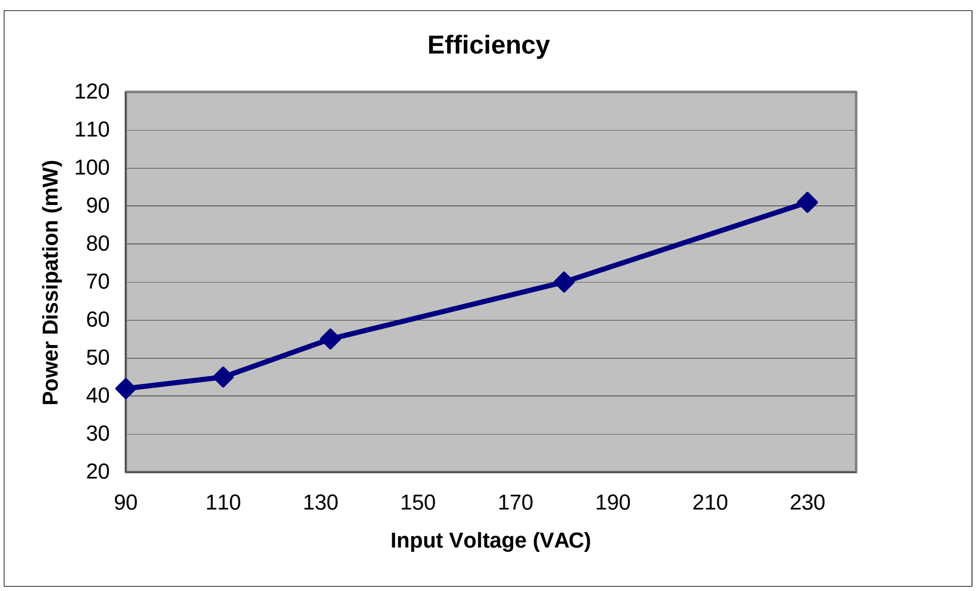

Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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10.3 Load and Line Regulation

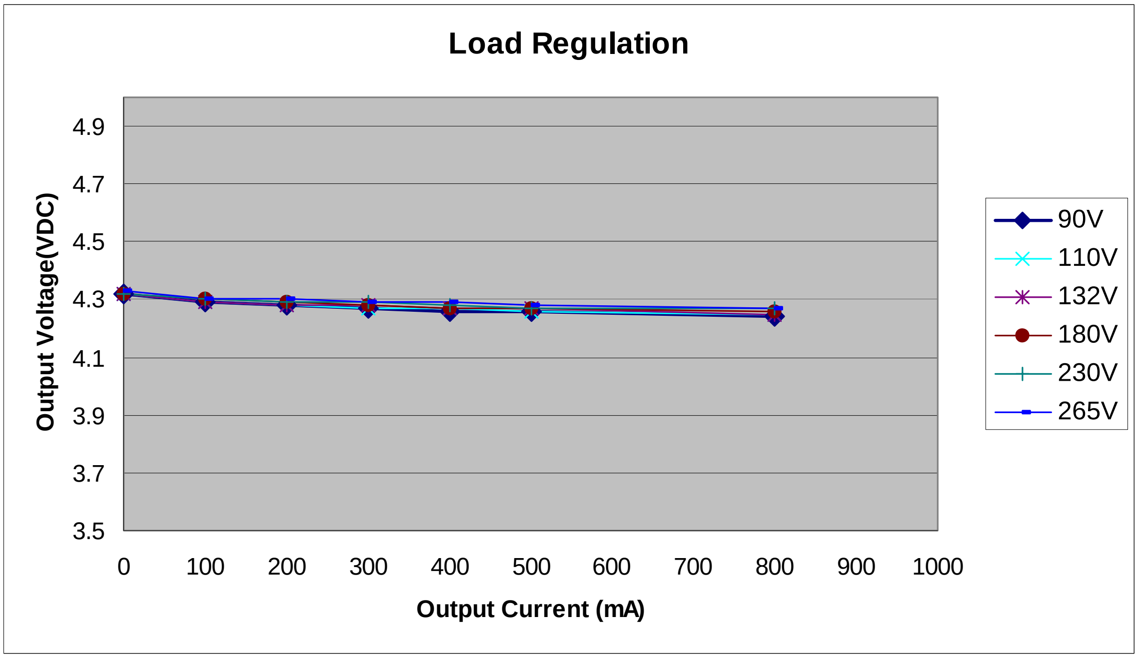

Figure 8 – Load Regulation, Room Temperature

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11 Thermal Performance

Test Condition: Open Air, 0.5A load

Temperature (°C)		
Item	**85 VAC**	**265 VAC**
Ambient (Deg.C)	25	25
Transformer (T1)	32	34
***TOPSwitch* (U1)**	38	34
Rectifier (D7)	48	47

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12 Waveforms

12.1 Drain Voltage Normal Operation

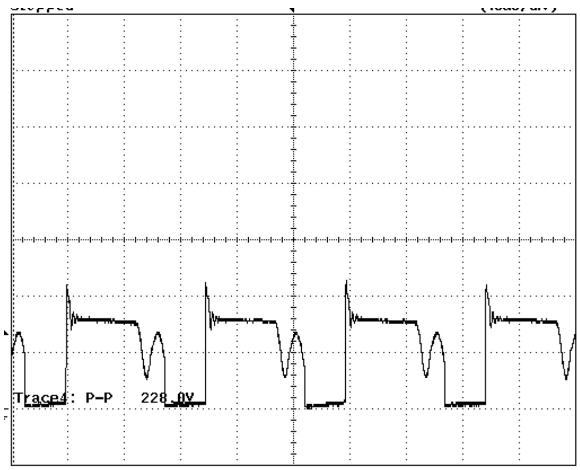

Figure 9 – 90 VAC, Full Load.
Lower: V_{DRAIN}, 100 V, 10 µs / div

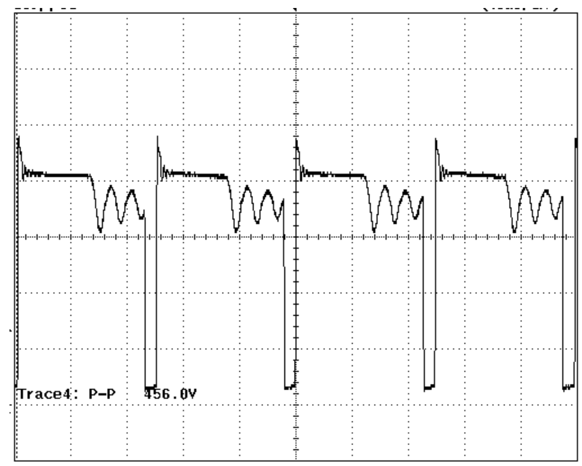

Figure 10 – 265 VAC, Full Load
V_{DRAIN}, 100 V, 10 µs / div

12.2 Output Voltage Start-up Profile

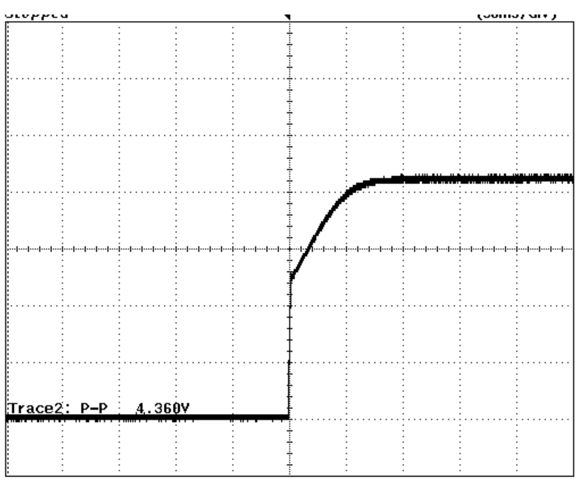

Figure 11 – Start-up Profile, 90VAC
1 V, 50 ms / div.

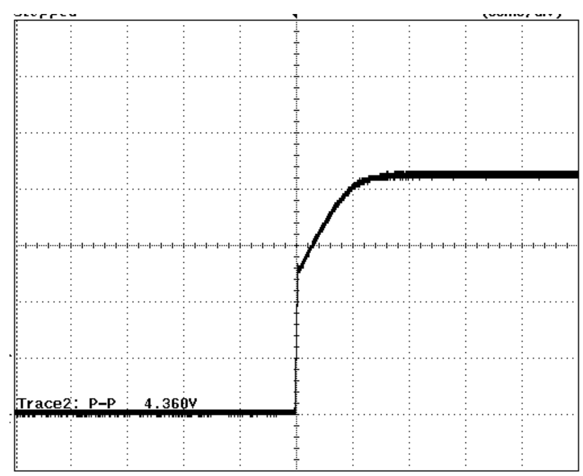

Figure 12 – Start-up Profile, 265 VAC
1 V, 50 ms / div.

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12.3 Drain Voltage Start-up Profile

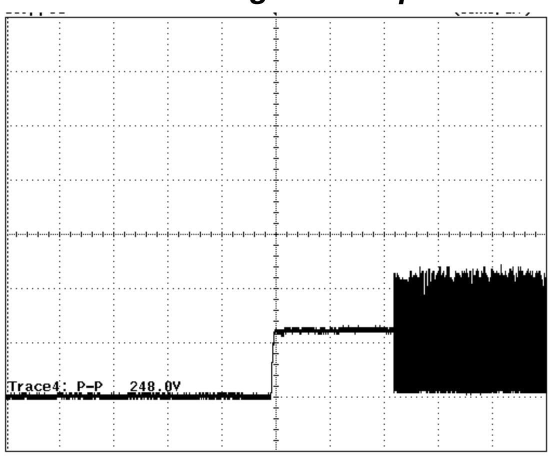

Figure 13 – 90 VAC Input and Maximum Load. V_{DRAIN}, 100 V & 50 ms / div.

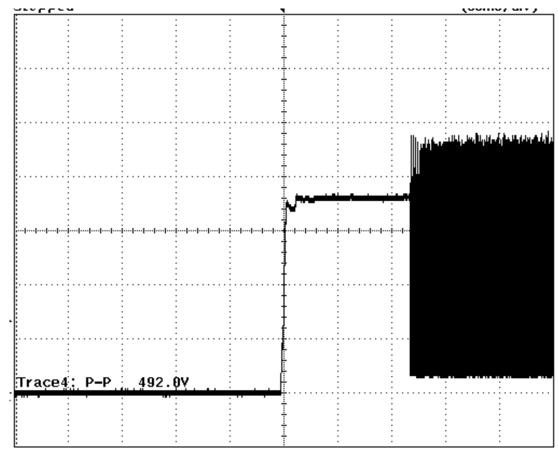

Figure 14 – 265 VAC Input and Maximum Load. V_{DRAIN}, 100 V & 50 ms / div.

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12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 15 and Figure 16.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

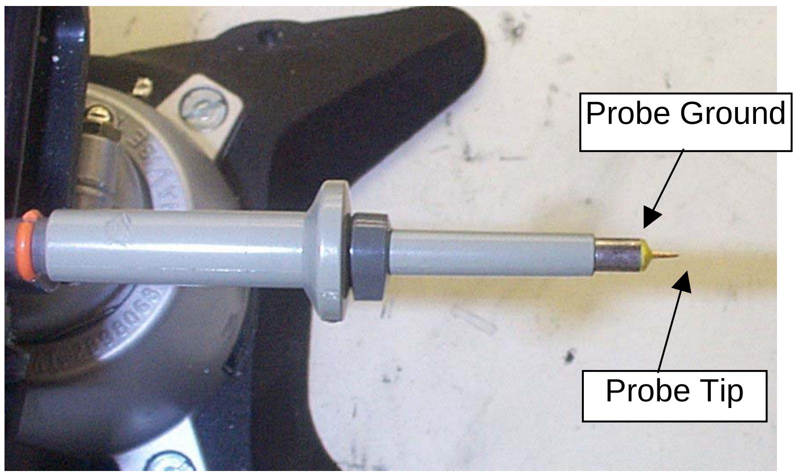

Figure 15 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 16 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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12.4.2 Measurement Results

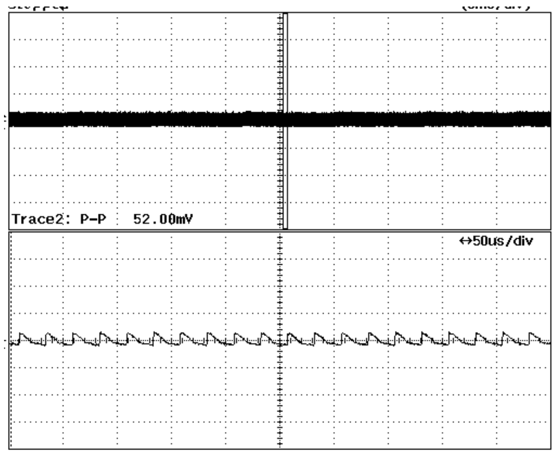

Figure 17 – Ripple, 90 VAC, Full Load.
5 ms, 100 mV / div

Figure 18 – 5 V Ripple, 115 VAC, Full Load.
5 ms, 100 mV / div

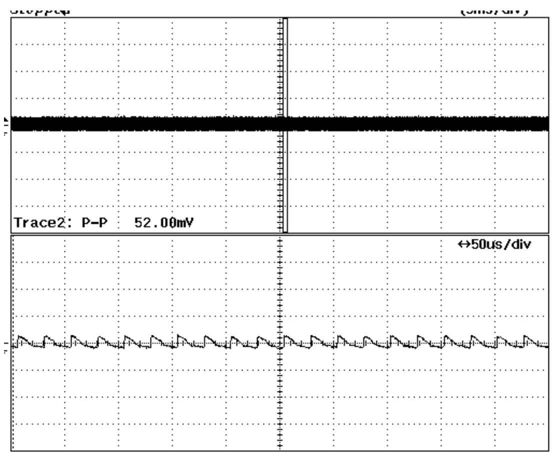

Figure 19 – Ripple, 230 VAC, Full Load.
5 ms, 100 mV /div

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13 Conducted EMI

EMI was tested at room temperature, 230 VAC input, full load

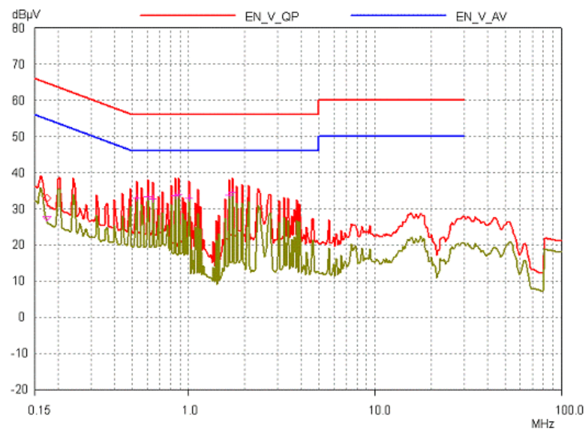

Figure 20 – Line, floating

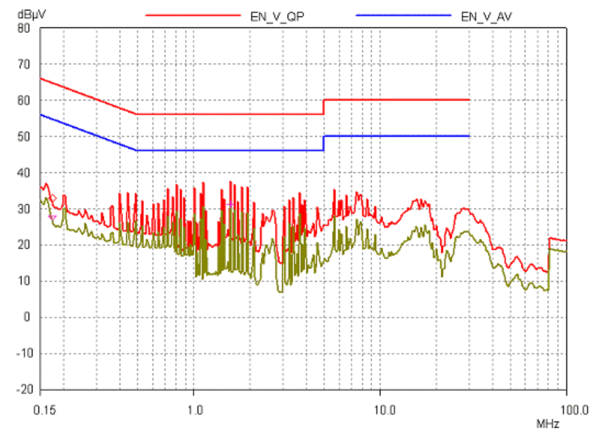

Figure 21 – Line, artificial hand

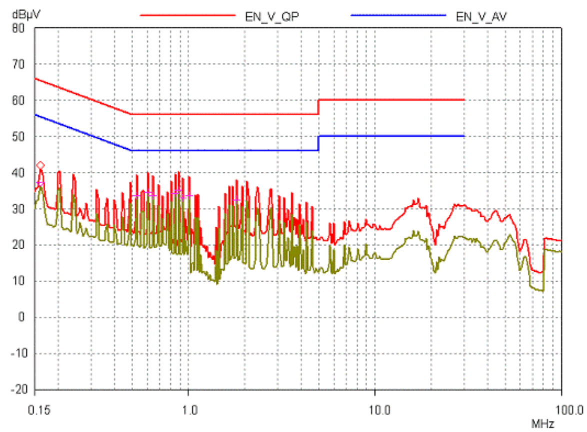

Figure 22 – Neutral, floating

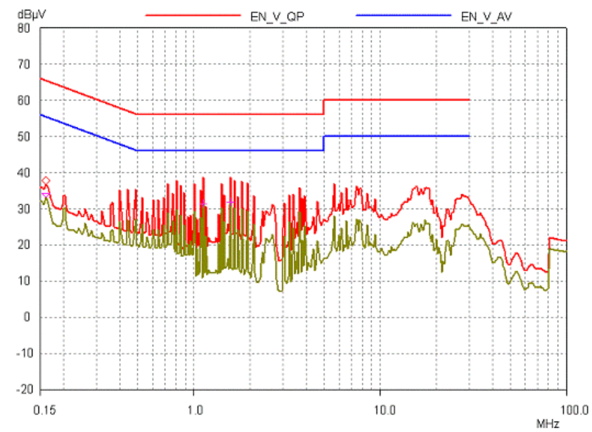

Figure 24 – Neutral, artificial hand

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
10-26-05	DZ	1.0	Initial Release	KM/JC/VC

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