AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			399	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			5.03	Amps/mm^2	Primary Winding Current density (3.8 < J < 9.75)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			5.85	Amps	Peak Secondary Current
ISRMS			2.78	Amps	Secondary RMS Current
IO_PEAK			1.67	Amps	Secondary Peak Output Current
IO			1.67	Amps	Average Power Supply Output Current
IRIPPLE			2.22	Amps	Output Capacitor RMS Ripple Current
CMS			556	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			22	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.65	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.56	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.46	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			575	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			59	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			55	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12	Volts	Output Voltage
IO1_AVG			1.67	Amps	Average DC Output Current
PO1_AVG			20.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			10.00		Output Winding Number of Turns
ISRMS1			2.778	Amps	Output Winding RMS Current
IRIPPLE1			2.22	Amps	Output Capacitor RMS Ripple Current
PIVS1			59	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			556	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.65	mm	Minimum Bare Conductor Diameter
ODS1			1.56	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.56		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils

AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.56		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			20	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

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10 Power Supply Performance

All tests were performed open frame at room temperature (+25 °C) and 60 Hz line frequency, unless noted otherwise.

10.1 Energy Efficiency

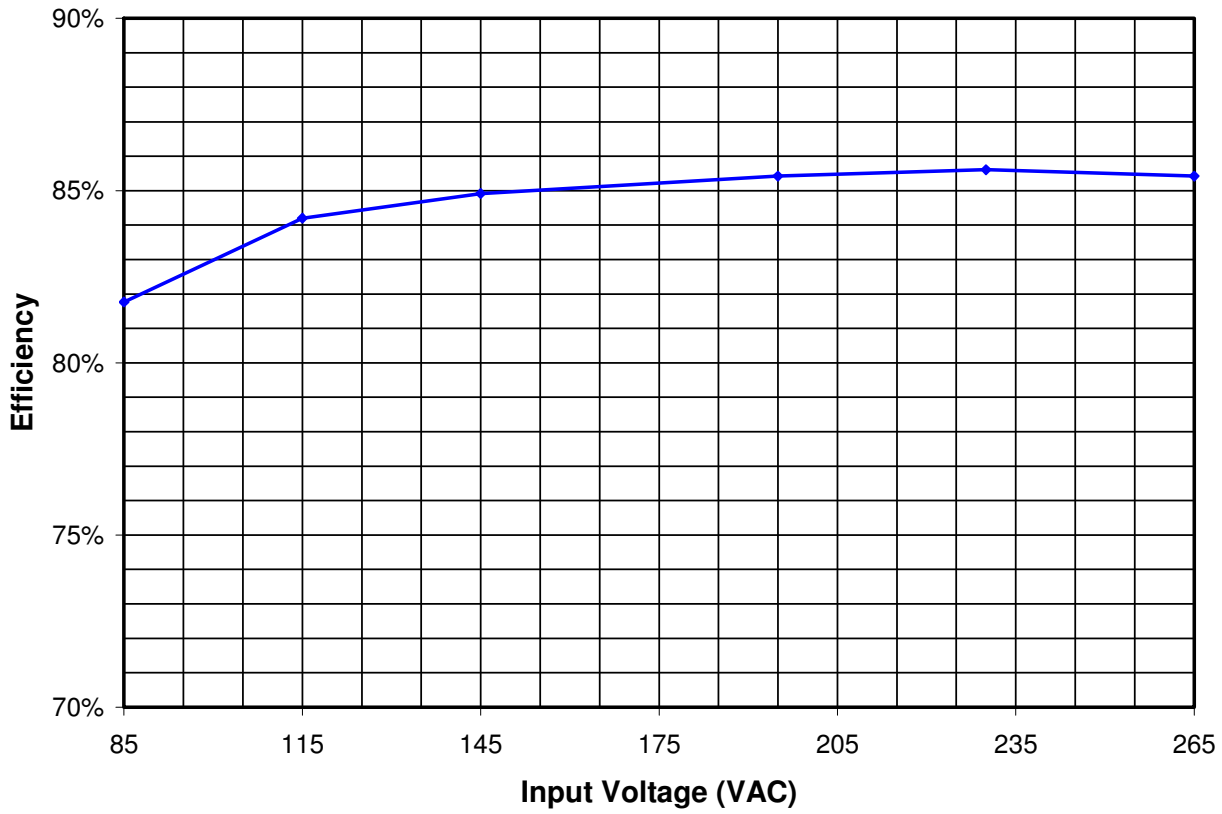

Figure 6 – Full Load Efficiency Over Input Voltage Range.

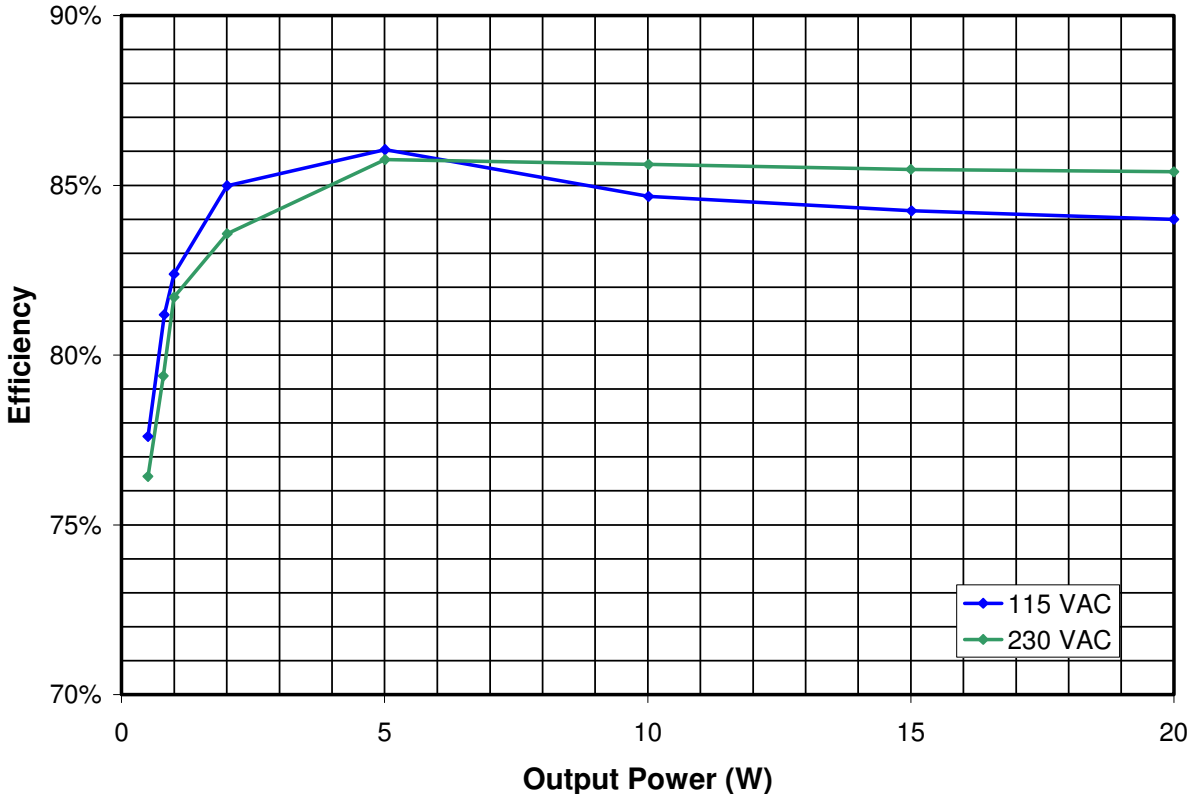

Figure 7 – Efficiency Over Load.

Table 2 lists the average active-on efficiency as defined by the Energy Star 2.0 specification (Final April 23, 2008).

Input Voltage	Efficiency at Relative Load Point				Average Efficiency
	25%	50%	75%	100%	
115 VAC	86.05%	84.67%	84.25%	84.00%	85%
230 VAC	85.76%	85.61%	85.47%	85.40%	86%
	Minimum efficiency Energy Star 2.0: 0.0626 * LN(20) + 0.622				81%

Table 2 – Average Active-on Efficiency.

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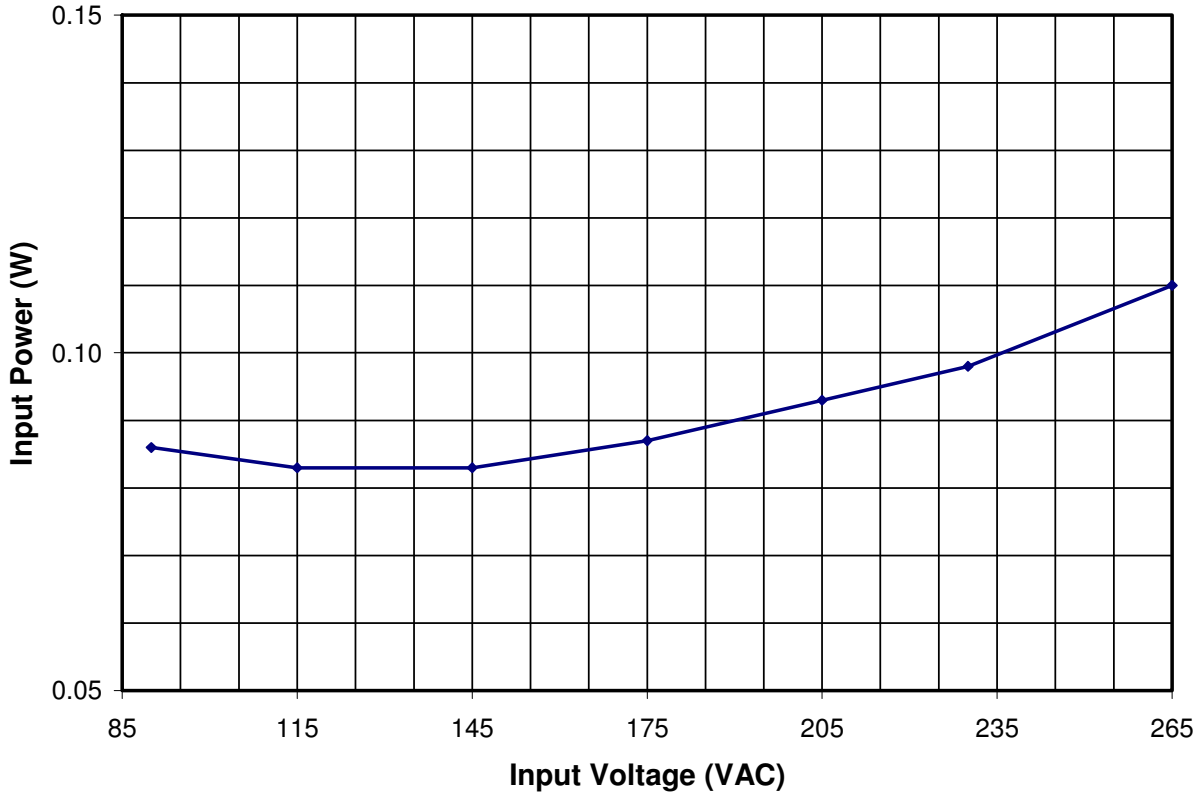

Figure 8 – No-load Input Power Consumption Over Line.

Figure 9 depicts the available output power in standby with the input power limited to 1.0 W.

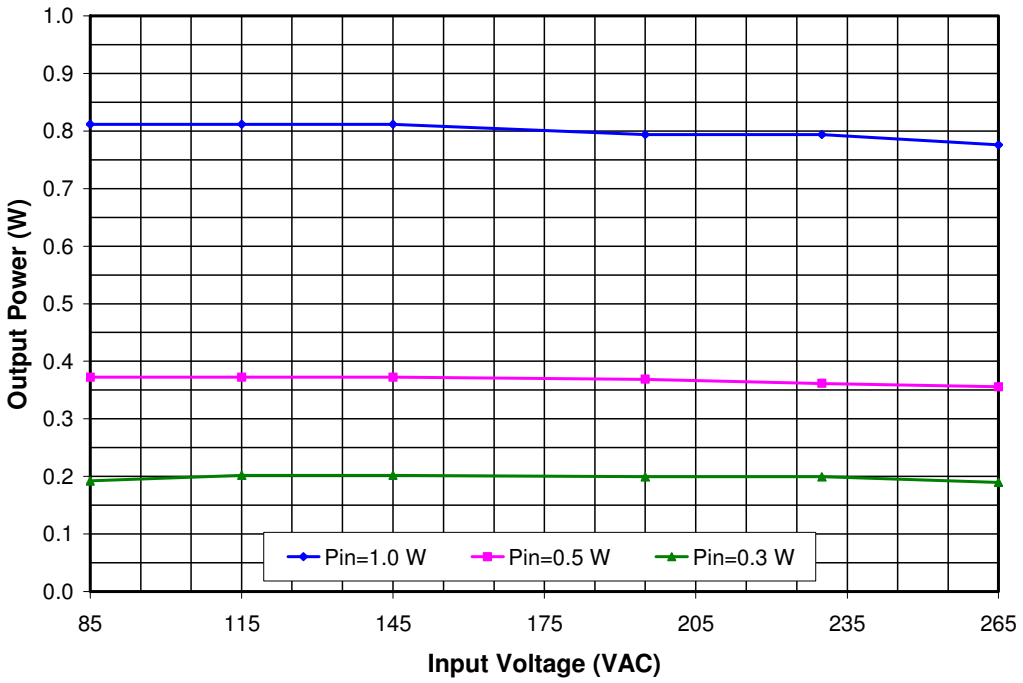

Figure 9 – Standby Output Power Over Line and Input Power.

10.2 Output Regulation and Quality

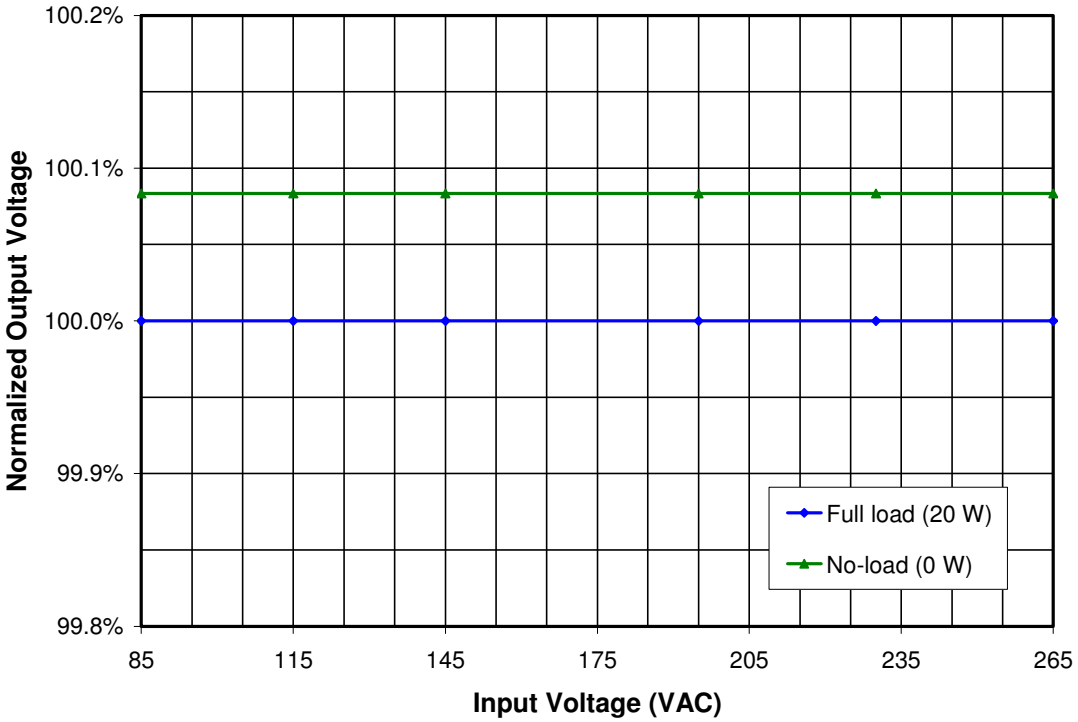

Figure 10 – Regulation Over Line and Load.

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Figures 11 to 15 depict output noise and ripple performance at various load and line conditions. The measurements were taken with a local voltage probe decoupling capacitance of 1 µF/50 V (electrolytic) and 0.1 µF/50 V (ceramic) with a 20 MHz DSO input filter.

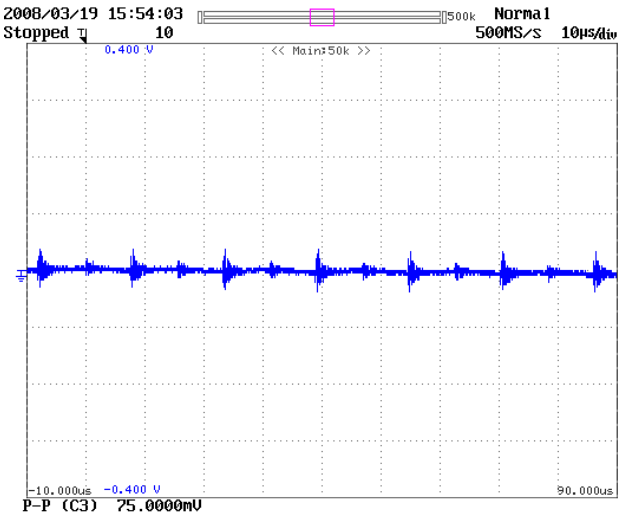

Figure 11 – Output Noise at 20 W, 85 VAC.
V_{OUT} (100 mV/Div, 10 µs/div).

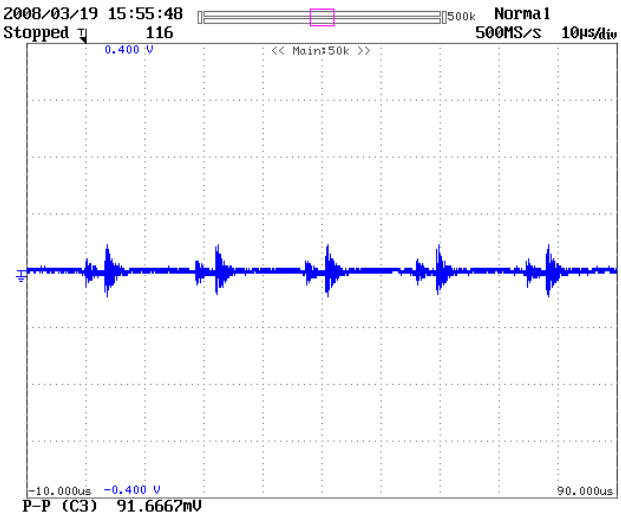

Figure 12 – Output Noise at 20 W, 265 VAC.
V_{OUT} (100 mV/Div, 10 µs/div).

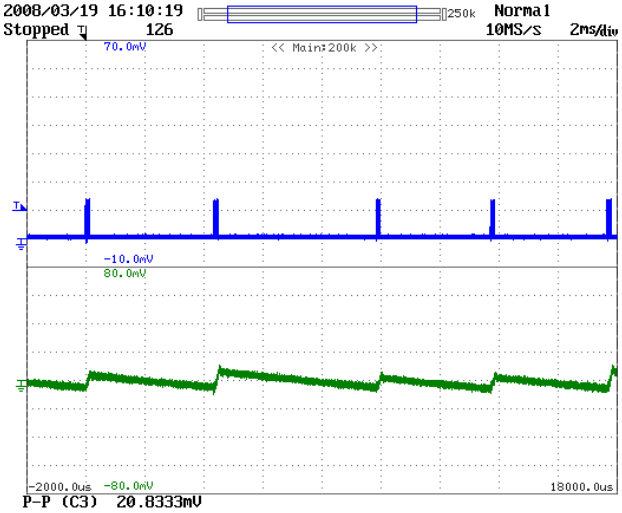

Figure 13 – Output Noise at No-load, 85 VAC.
Upper: I_D (0.2 A/Div, 2 ms/div).
Lower: V_{OUT} (20 mV/div).

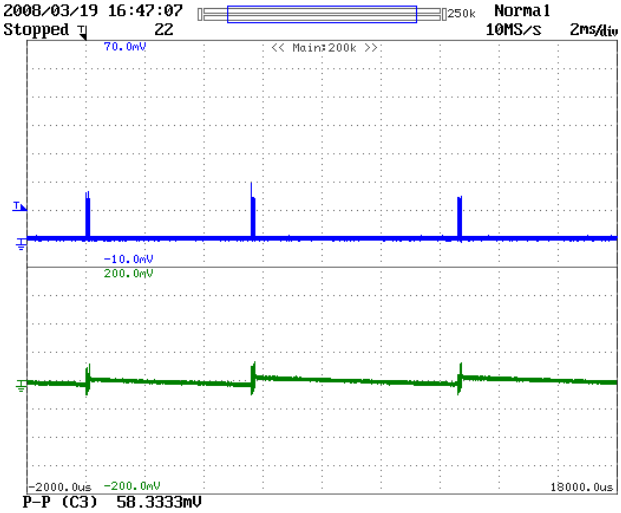

Figure 14 – Output Noise at No-load, 265 VAC.
Upper: I_D (0.2 A /Div, 2 ms/div).
Lower: V_{OUT} (50 mV/div).

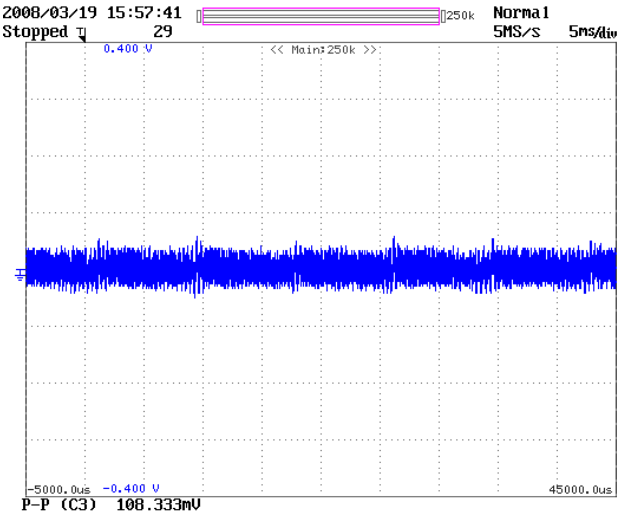

Figure 15 – Output Ripple at 20 W, 85 VAC.
V_{OUT} (0.1 V/Div, 5 ms/div).

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10.3 Transient Load

Figures 16 through 19 depict the step-load performance at various load combination and line-voltage conditions. The current slew rate was set to 10 mA/µs.

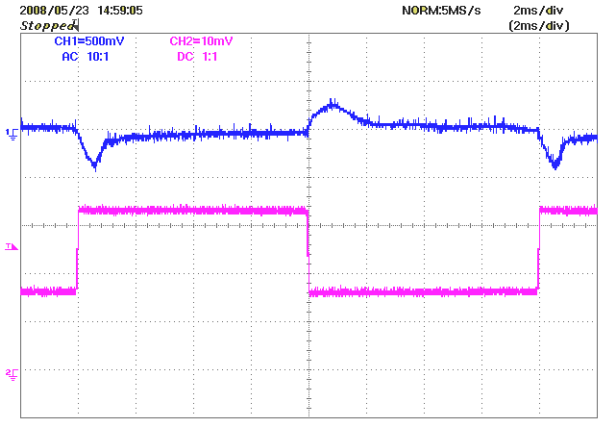

Figure 16 – Step Load 50-100%, 85 VAC.
Upper: V_{OUT} (0.5 V/div, 2 ms/div).
Lower: I_{LOAD} (0.5 A/div).

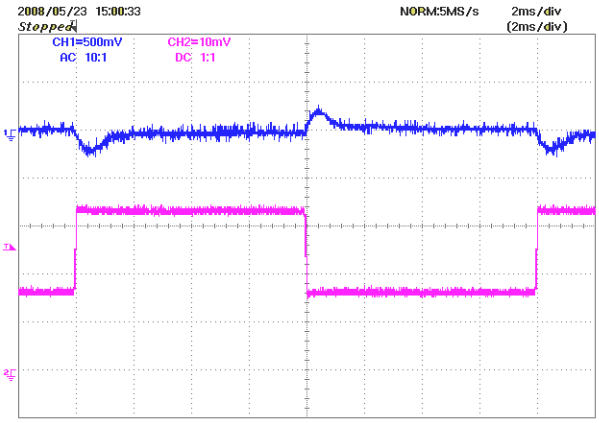

Figure 17 – Step Load 50-100%, 265 VAC.
Upper: V_{OUT} (0.5 V/div, 2 ms/div).
Lower: I_{LOAD} (0.5 A/div).

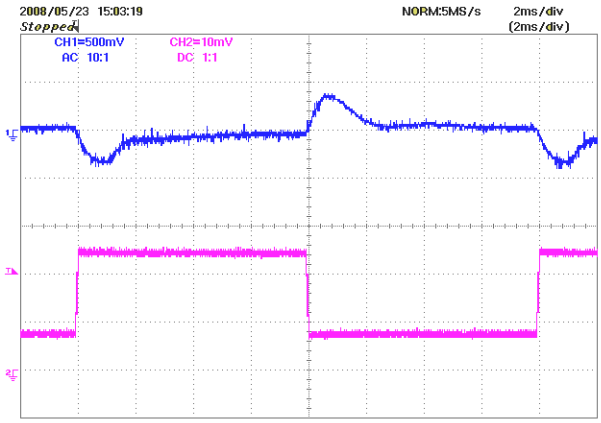

Figure 18 – Step Load 25-75%, 85 VAC.
Upper: V_{OUT} (0.5 V/div, 2 ms/div).
Lower: I_{LOAD} (0.5 A/div).

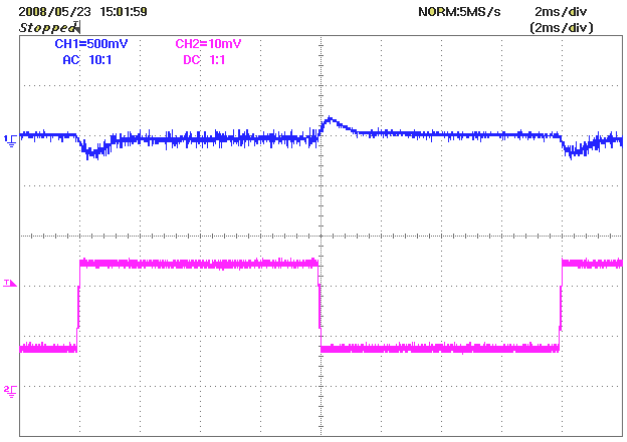

Figure 19 – Step Load 25-75%, 265 VAC.
Upper: V_{OUT} (0.5 V/div, 2 ms/div).
Lower: I_{LOAD} (0.5 A/div).

10.4 Startup

Figures 20 through 23 depict the startup performance at various load and line conditions.

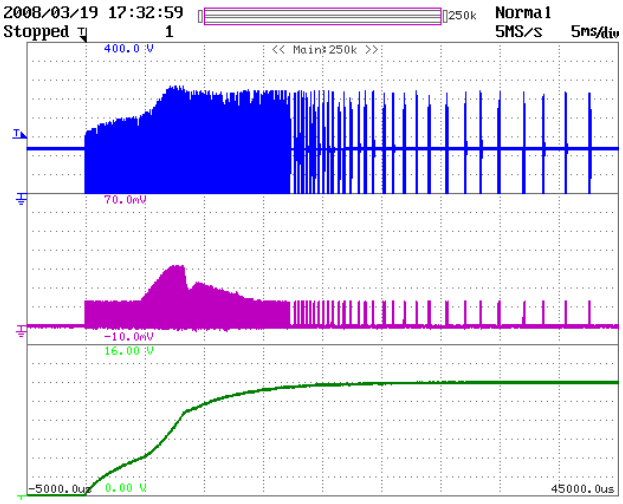

Figure 20 – Startup at no-load, 85 VAC.
Upper: V_{DS} (50 V/div, 5 ms/div).
Middle: I_D (0.2 A/div).
Lower: V_{OUT} (2 V/div).

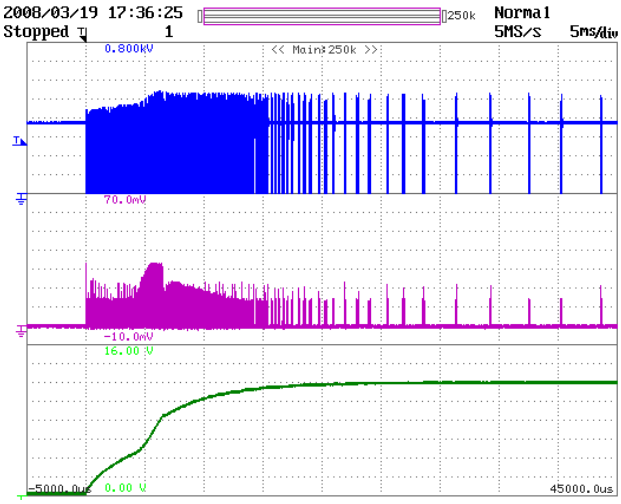

Figure 21 – Startup at no-load, 265 VAC.
Upper: V_{DS} (100 V/div, 5 ms/div).
Middle: I_D (0.2 A/div).
Lower: V_{OUT} (2 V/div).

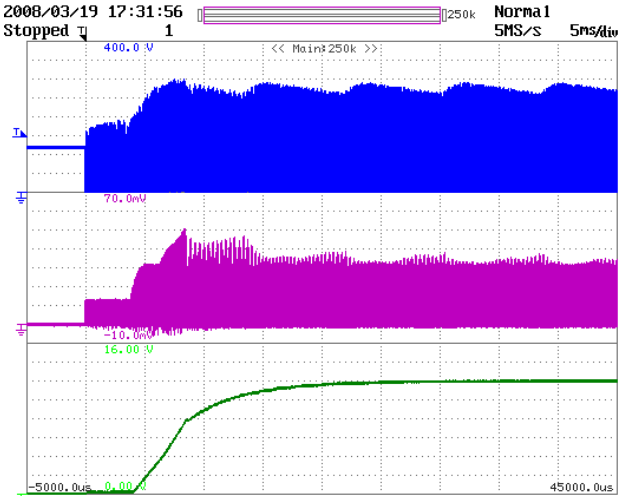

Figure 22 – Startup at 20 W, 85 VAC.
Upper: V_{DS} (50 V/div, 5 ms/div).
Middle: I_D (0.2 A/div).
Lower: V_{OUT} (2 V/div).

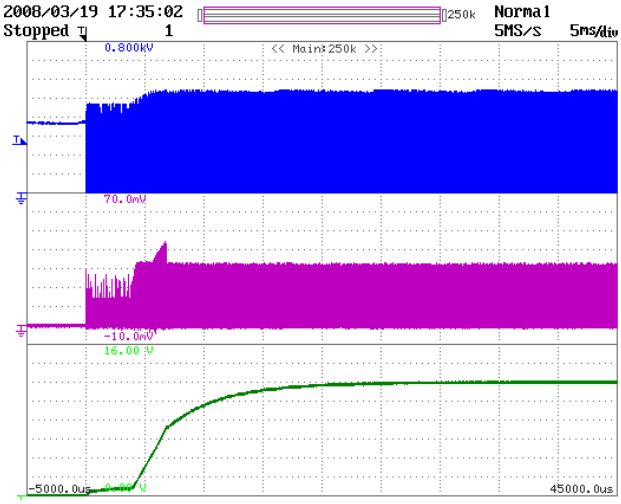

Figure 23 – Startup at 20 W, 265 VAC.
Upper: V_{DS} (100 V/div, 5 ms/div).
Middle: I_D (0.2 A/div).
Lower: V_{OUT} (2 V/div).

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11 Conducted EMI

Conducted EMI was measured with a 7.2 Ω resistive load (20 W).

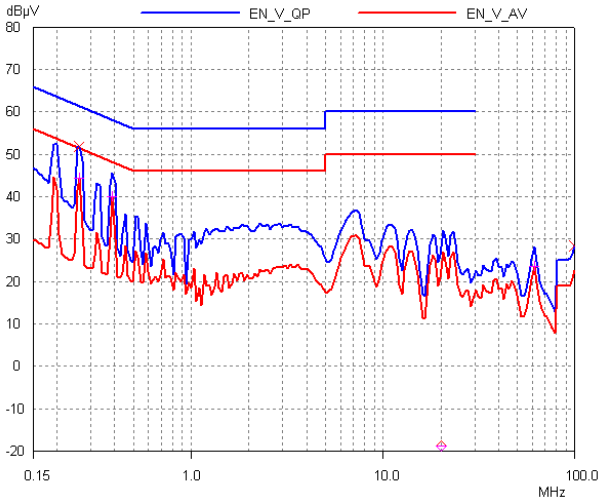

Figure 24 – Conducted EMI, 115 VAC. Output RTN Floating.

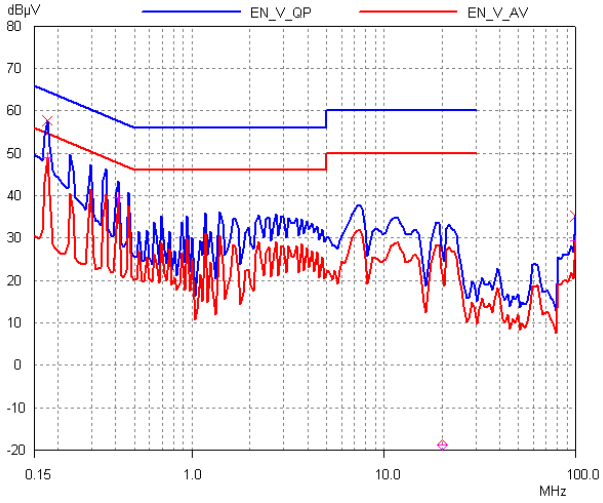

Figure 25 – Conducted EMI, 230 VAC. Output RTN Floating.

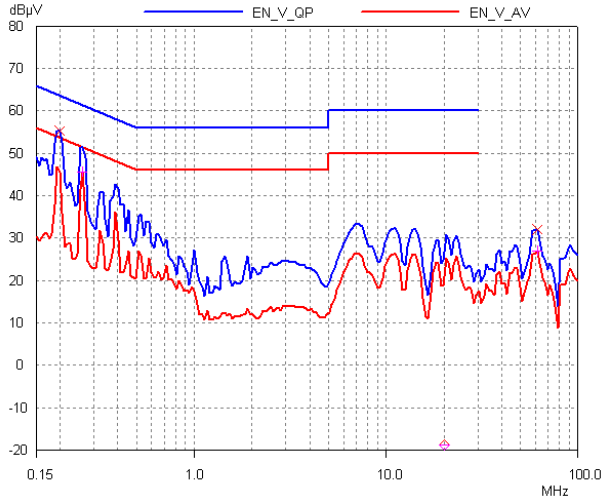

Figure 26 – Conducted EMI, 115 VAC. Output RTN Connected to Artificial Hand.

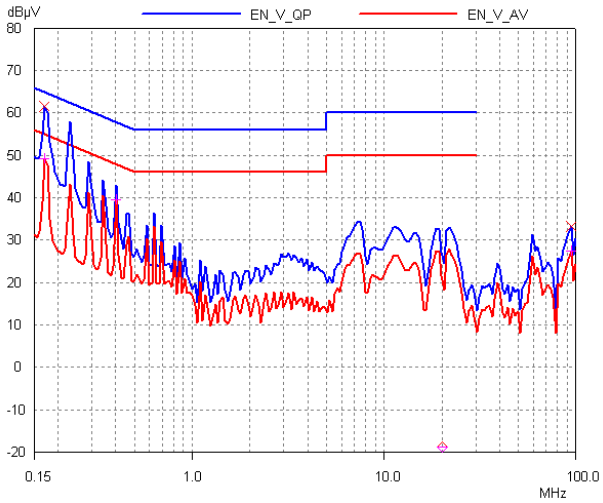

Figure 27 – Conducted EMI, 230 VAC. Output RTN Connected to Artificial Hand.

11.1 Waveform Plots

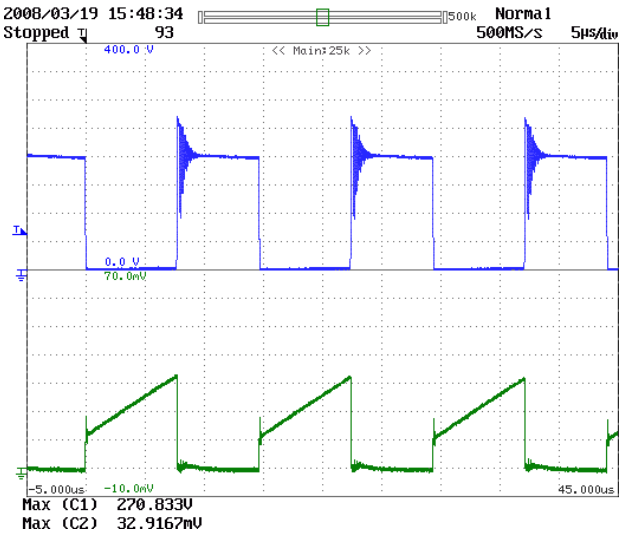

Figure 28 – Drain Waveforms at 20 W, 85 VAC.
Upper: V_{DS} (50 V/div, 5 µs/div).
Lower: I_D (0.2 A/div).

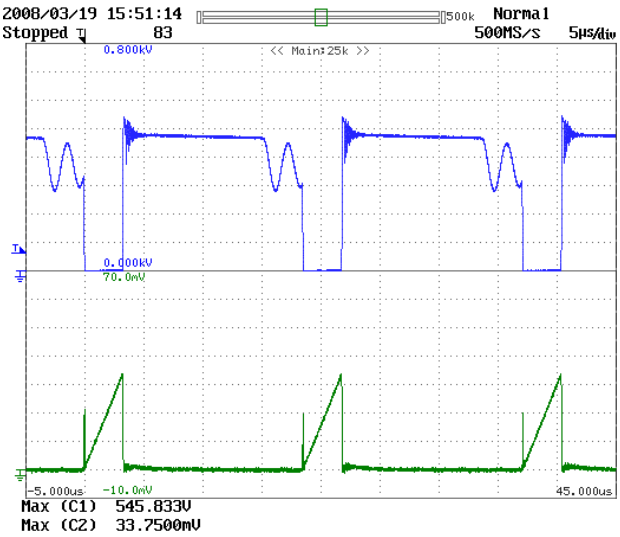

Figure 29 – Drain Waveforms at 20 W, 265 VAC.
Upper: V_{DS} (100 V/div, 5 µs/div).
Lower: I_D (0.2 A/div).

Figure 32 depicts the output voltage and Drain waveforms during an output short circuit (applied at the DC load). The input power under this condition is 0.9 W.

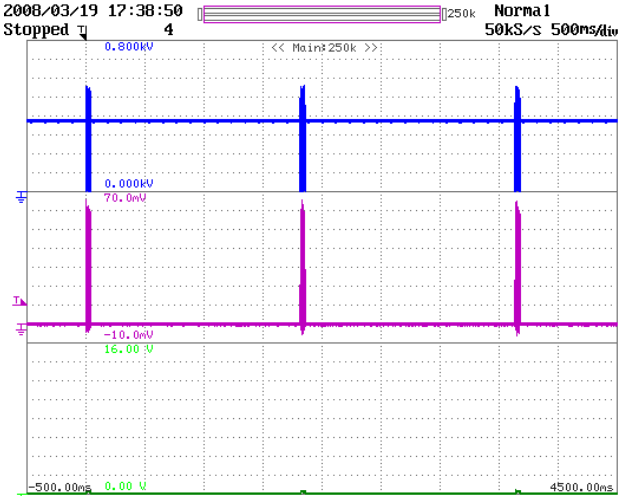

Figure 30 – Output Short Circuit, 265 VAC.
Upper: V_{DS} (100 V/div, 500 ms/div).
Middle: I_D (0.2 A/div).
Lower: V_{OUT} (2 V/div).

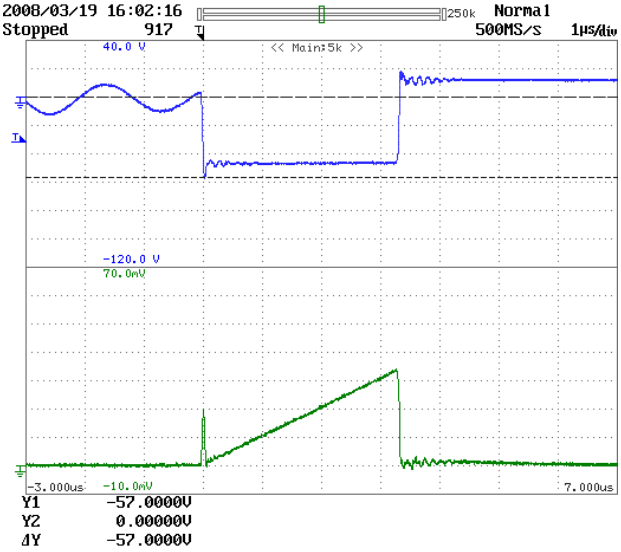

Figure 31 – Output diode reverse voltage at 20 W, 265 VAC.
Upper: $V_{RR(D7)}$ (20 V/div, 1 µs/div).
Lower: I_D (0.2 A/div).

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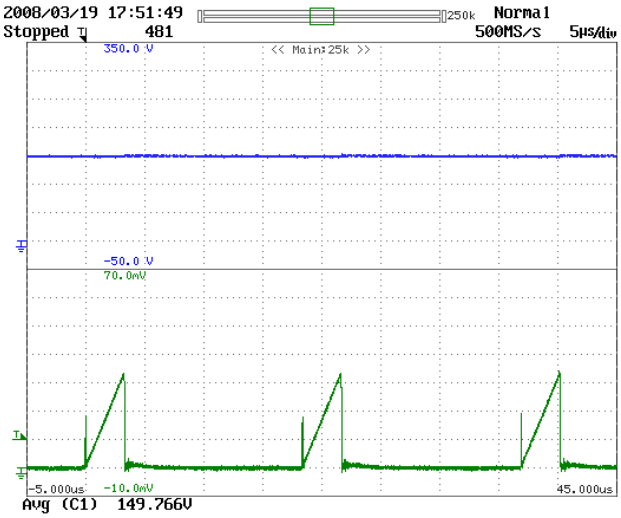

Figure 32 – Clamp Zener Voltage at 20 W, 265 VAC.
Upper: V_{VR1} (50 V/div, 5 µs/div).
Lower: I_D (0.2 A/div).

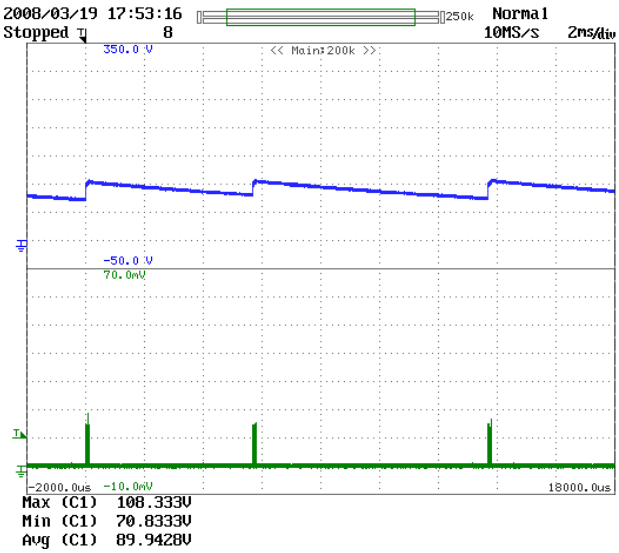

Figure 33 – Clamp Zener Voltage at 0 W, 265 VAC.
Upper: V_{VR1} (50 V/div, 2 ms/div).
Lower: I_D (0.2 A/div).

12 Revision History

Date	Author	Rev.	Description & changes	Reviewed
30-Sep-08	SGK	1.0	Initial Release	

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