9.2.6.1 Output Voltage Start-up Behavior

The start-up behavior of each rail was measured using resistive loads on the outputs. Figure 32 shows the start-up behavior of the 1V2, 2V5, 3V3 and 5V rails whilst Figure 33 shows the 6V6 and 12V rails with the 1V2 start-up as a reference.

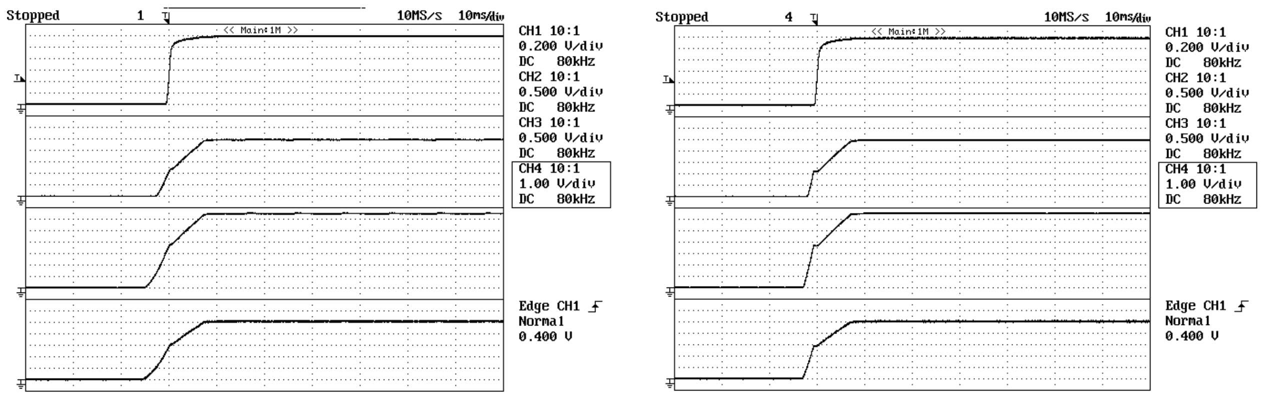

Figure 32 - Start-up Behavior of 1V2 (Top 0.2V/div), 2V5 (Second From Top 0.5V/div), 3V3 (Third from Top 0.5V/div), 5V (Bottom 1V/div). Left Hand Side is 85V_{ac} input and Right Hand Side is 265V_{ac}. Timebase is 10ms/div

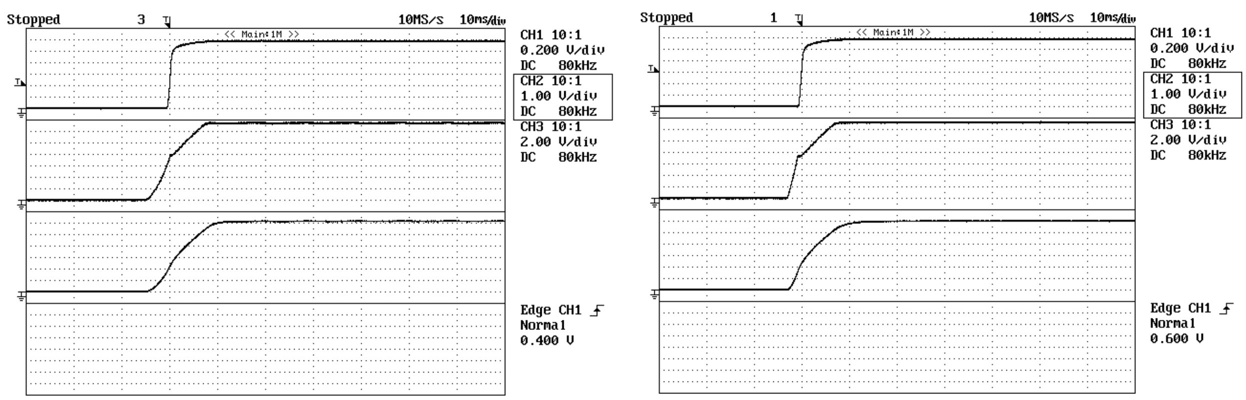

Figure 33 - Start-up Behavior of 1V2 (Top 0.2V/div), 6V6 (Second From Top 1V/div), 12V (Bottom 2V/div). Left Hand Side is 85V_{ac} input and Right Hand Side is 265V_{ac}. Timebase is 10ms/div

All rails start-up within 10ms and have zero voltage overshoot.

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9.2.6.2 Measured Noise and Ripple

All waveforms were measured with 115V mains input and at full operating power. All results AC coupled.

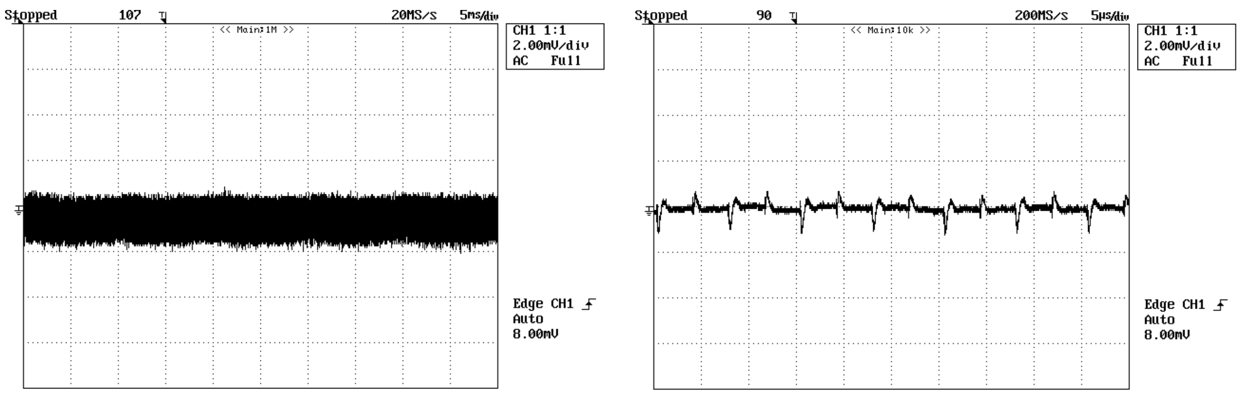

Figure 34 – 1V2 Rail. Output 100Hz ripple (LHS, 5ms/div and 2mV/div) and 132kHz noise (RHS, 5us/div and 2mV/div)

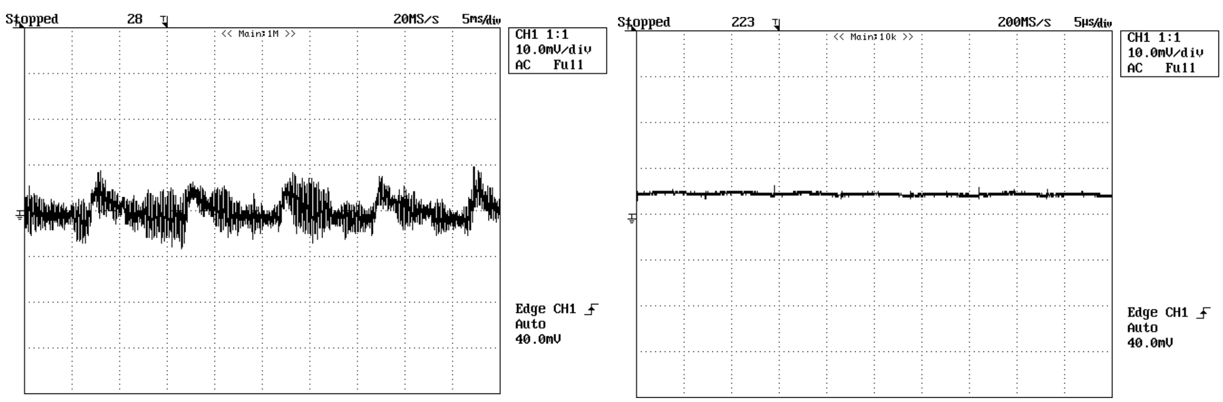

Figure 35 – 2V5 Rail. Output 100Hz ripple (LHS, 5ms/div and 10mV/div) and 132kHz noise (RHS, 5us/div and 10mV/div)

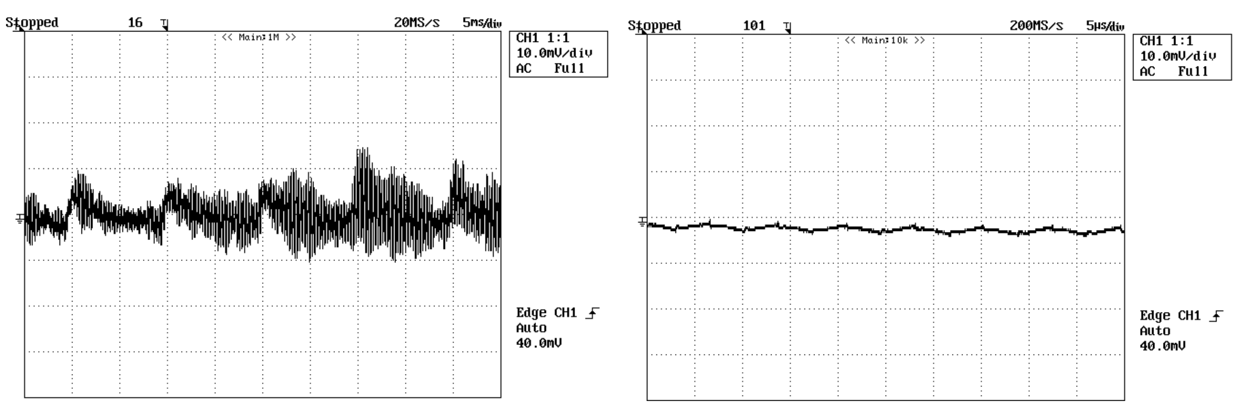

Figure 36 – 3V3 Rail. Output 100Hz ripple (LHS, 5ms/div and 10mV/div) and 132kHz noise (RHS, 5us/div and 10mV/div)

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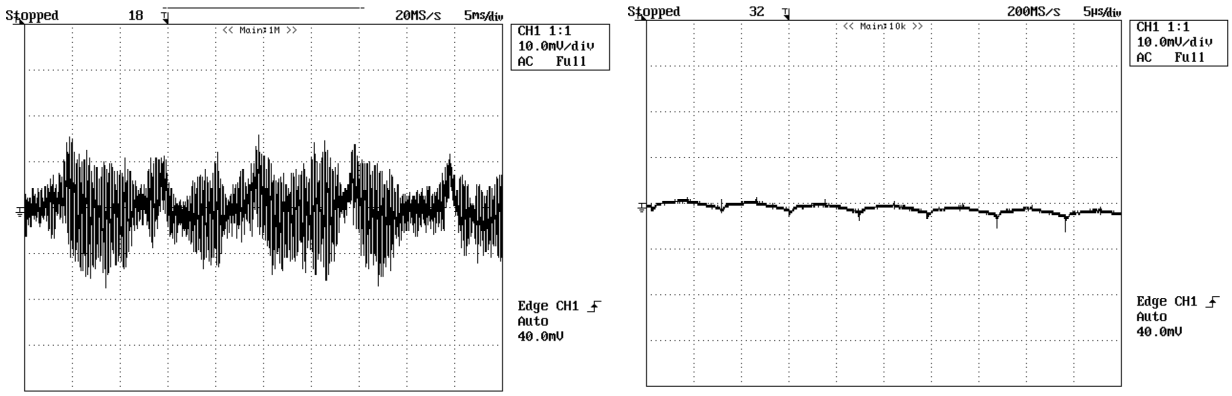

Figure 37 – 5V Rail. Output 100Hz ripple (LHS, 5ms/div and 10mV/div) and 132kHz noise (RHS, 5us/div and 10mV/div)

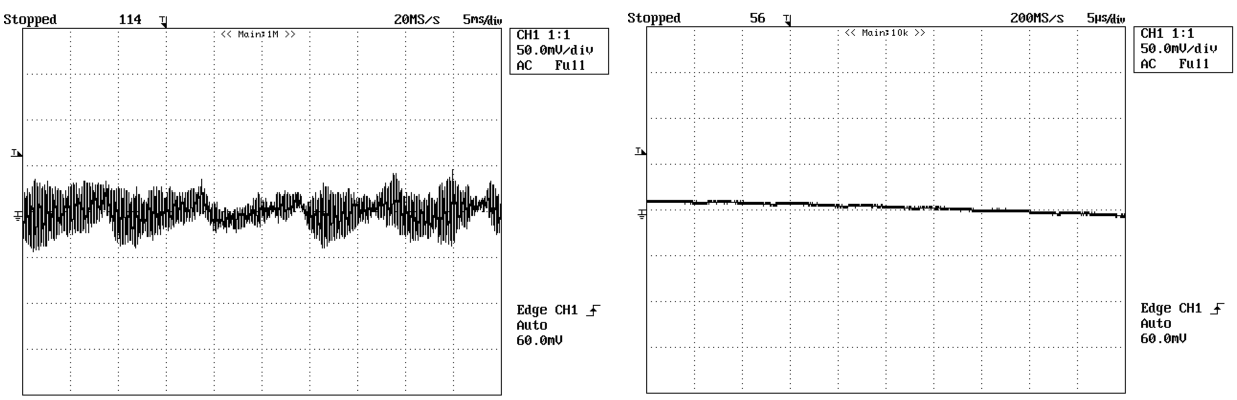

Figure 38 – 6V6 Rail. Output 100Hz ripple (LHS, 5ms/div and 50mV/div) and 132kHz noise (RHS, 5us/div and 50mV/div)

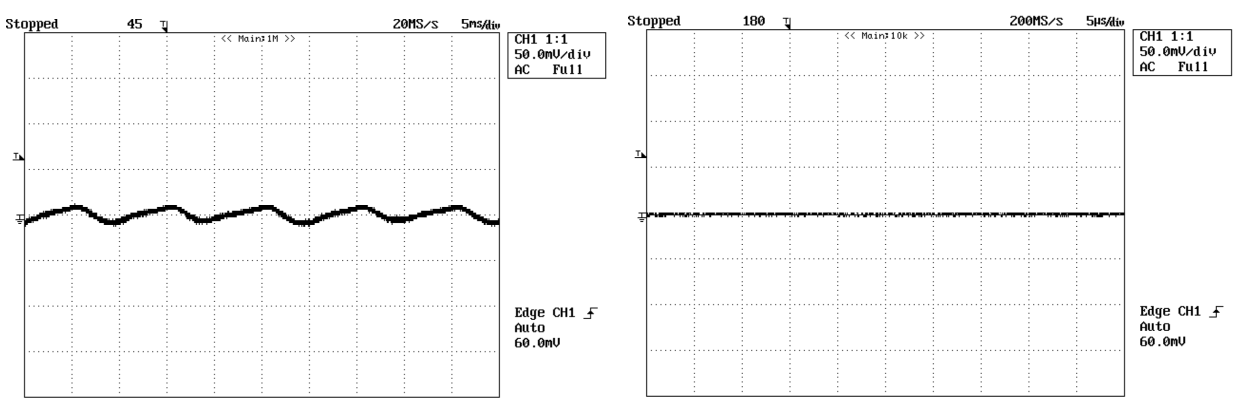

Figure 39 – 12V Rail. Output 100Hz ripple (LHS, 5ms/div and 50mV/div) and 132kHz noise (RHS, 5us/div and 50mV/div)

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9.2.6.3 Transient Loading

In order to give an indication of loop stability, the load on the 3V3 rail was switched from 50% to 100% and the response of the rail measured. Figure 40 shows the results at $85V_{ac}$ and $265V_{ac}$.

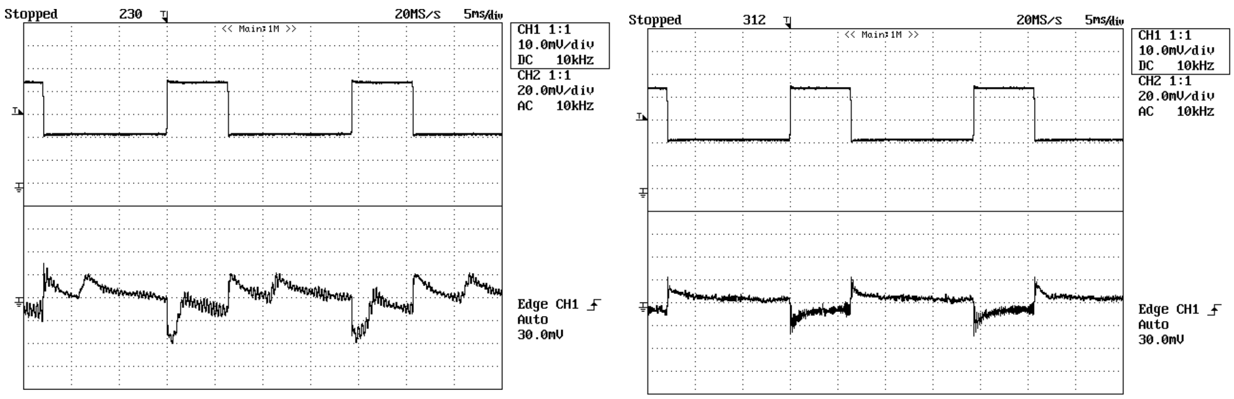

Figure 40 – Transient response on 3V3 rail. Upper is rail current at 0.1A/div and lower is AC coupled rail voltage at 20mV/div. Left Hand Side is $85V_{ac}$ input and Right Hand Side is $265V_{ac}$.

The voltage response shows a well damped behavior which indicates a good phase/gain margin. For production verification, a network analyzer should be used to measure the control loop response at extremes of load, line voltage and operating temperature. In the measurement of with $85V_{AC}$ input, there is a small component of ripple due to 100Hz breakthrough which shows up in the transient response plot. The level is very low and completely independent of the transient recovery behavior.

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9.2.7 Conducted EMI Measurements

The measurements presented in this section are pre-compliance and should only be used for guidance. Measurements are performed with 115V input and full power output. Figure 41 gives the conducted EMI measurement with the output floating and Figure 42 with the output grounded to protective earth to simulate grounding through a SCART lead.

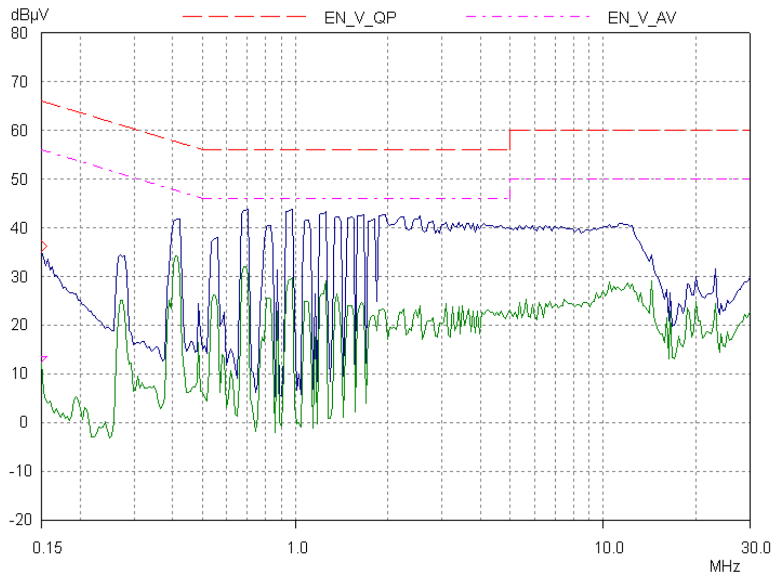

Figure 41 - EMI with Output Floating

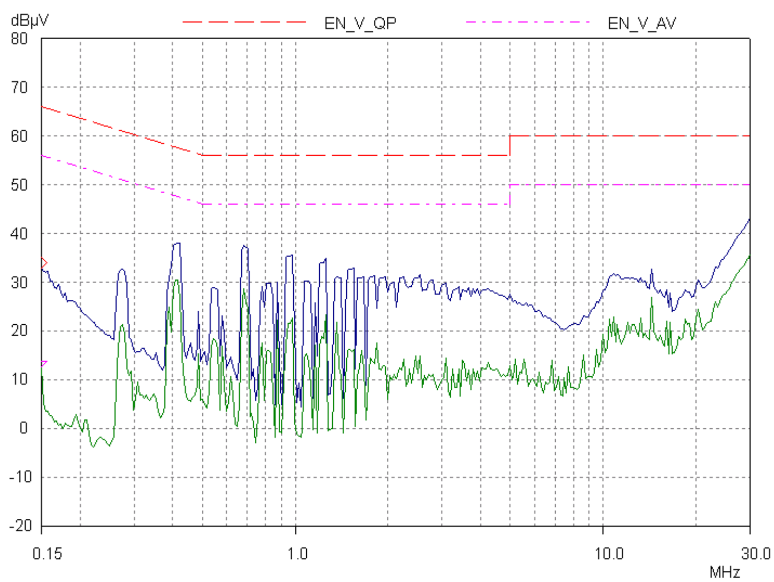

Figure 42 - EMI with Output Grounded to Protective Earth

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10 Appendix A – Tolerance of Linear Regulated Outputs

10.1 2V5 Linear Regulated Output

The 2V5 output is provided via a diode drop from the 3V3 rail. The diode forward voltage will be a function of both diode current and temperature.

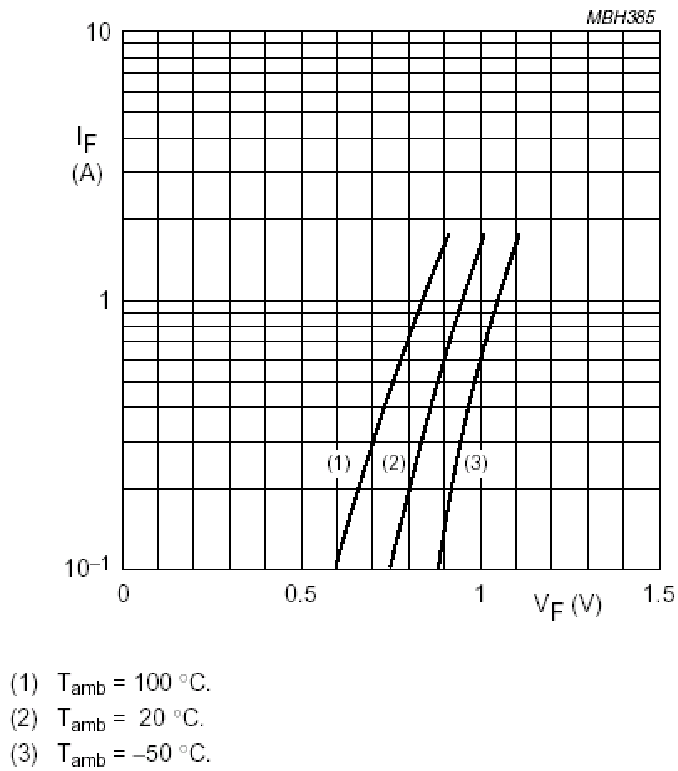

Figure 43 – 1N4005 Diode Forward Voltage Behavior [Source - Philips Semiconductors]

The load current will vary from 30mA to 215mA and this will give a variation in diode drop of 0.7V to around 0.8V respectively. At 215mA and 20°C, the required 0.8V drop will be achieved giving 2.5V output.

With an operating ambient of 0-50°C, the likely diode temperature will be between 50°C and 100°C and therefore the voltage-current curve will lie between lines 1 and 2 on Figure 43.

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10.2 1V2 Discrete Linear Regulator

The 1V2 linear regulator uses the circuit shown below to drop to 1.2V from 3.3V.

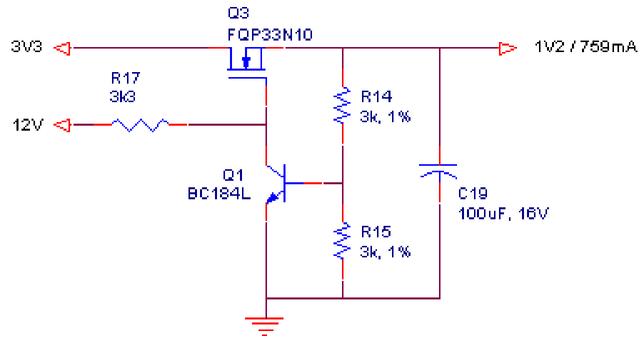

Figure 44 - 1V2 Discrete Linear Regulator

This circuit uses the base-emitter (V_{be}) voltage of Q1 to set the output voltage via R15 and R14. V_{be} is determined by the device temperature and the collector bias current. Pspice was used to simulate the variation of base-emitter voltage with collector current at 0, 25 and 50°C. The results are given in Figure 45 below.

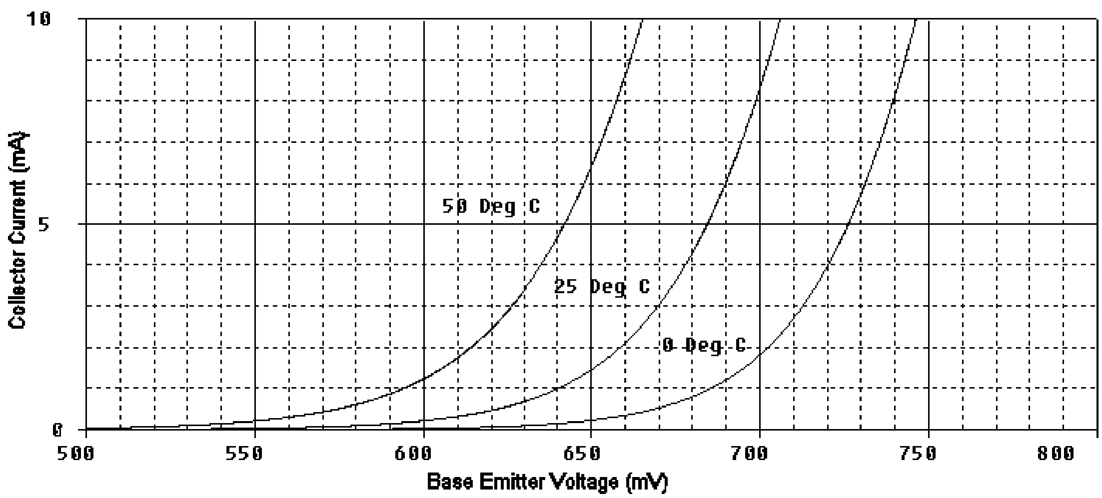

Figure 45 - Simulation of base-emitter voltage variation

Collector current in Q1 can be found from - $I_C = \dfrac{V_{Bias} - (V_{GS} + 1.2)}{R_{17}}$

V_{BIAS}=Bias Voltage for Regulator (6.6V nominal here)
V_{GS} = Gate-Source voltage of Q3

Therefore, the collector current will vary with V_{BIAS}, V_{GS} and R_{17}. Differentiation of the I_C expression with respect to each of the three quantities will give the dependency.

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$$\frac{dI_C}{dV_{BIAS}} = \frac{1}{R_{17}}, \quad \frac{dI_C}{dV_{GS}} = -\frac{1}{R_{17}} \quad \text{and} \quad \frac{dI_C}{dR_{17}} = \frac{-(V_{BIAS} - (V_{GS} + 1.2))}{(R_{17})^2}$$

With the values chosen,

$$\frac{dI_C}{dV_{BIAS}} = 0.3mA/V$$

$$\frac{dI_C}{dV_{GS}} = -0.3mA/V$$

$$\frac{dI_C}{dR_{17}} = -0.6\mu A/V$$

Thus, the two dominant mechanisms affecting the 1.2V output are variations in the regulator bias voltage (12V) and variations in the Gate-Source voltage of Q3. The bias voltage tolerance is 10% and this will give ±0.36mA variation in collector current. The gate-source voltage behaviour of Q3 is shown below.

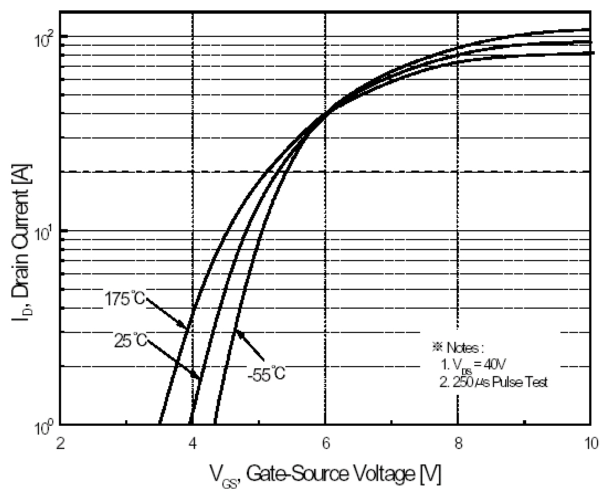

Figure 46 - Gate-Source Voltage Behaviour of QFP33N10

Figure 46 indicates that the gate-source voltage will vary by a maximum of around 0.5V over variations in temperature and drain current (0 to 1A). Thus, variations in the collector current of Q1 due to changes in the gate-source voltage of Q3 will be around ±0.15mA. The combined changes in collector current will be ±0.45mA and this will have a very small effect on output voltage. Temperature changes will influence V_{BE} to a greater effect and Figure 45 shows V_{BE} changes from 715mV at 0°C and 2mA to 615mV at 50°C and 2mA. This gives an output voltage from the linear regulator circuit of 1.3V at 0°C and 1.12V at 50°C.

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11 Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	IM	1.0	Initial release	VC / AM

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