DI-146 Design Idea
TOPSwitch®-HX

35 W LCD Monitor Power Supply

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
LCD Monitor	TOP258PN	35 W	90 – 264 VAC	5 V, 15 V	Flyback

Design Highlights

- High efficiency
  - >83% full load efficiency (Meets CEC 2008 requirements of 82%)
  - Delivers 35 W at 50° C ambient without requiring an external heat sink
- Low no-load and standby power consumption
  - 0.55 W standby output power for <1 W input
  - No-load power consumption <160 mW at 230 VAC
- Integrated safety/reliability features:
  - Accurate, auto-recovering, hysteretic thermal shutdown function maintains safe IC temperatures under all conditions
  - Auto-restart protects against output short circuits and open feedback loops
  - Output OVP configurable for latching or self recovering
- Meets EN55022 and CISPR-22 Class B conducted EMI with >10 dBµV margin

Operation

The isolated flyback converter shown in Figure 1 was designed around a member of the TOPSwitch-HX family, the TOP258PN (U1). A device in the P package (8-pin DIP) was selected to minimize cost by eliminating external heatsinks. Ideal applications include LCD monitor power supplies, which typically require low standby and no-load power consumption.

The AC input is rectified (D1–D4), filtered (C4) and connected across the primary side power components (T1 and U1). Diodes D1 and D3 were selected as fast recovery diodes for better EMI performance. EMI filtering is provided by components, C4, C5, L1, C7 and C11. Thermistor RT1 limits the inrush current drawn by the circuit on application of input AC.

To optimize efficiency under all load conditions, U1 operates in one of four modes. From no-load to full load, these are: multi-cycle modulation, fixed frequency PWM (25 kHz), variable frequency PWM and fixed frequency PWM (66 kHz). In all modes the controller maintains a linear relationship between duty cycle and control pin current so that the transition between modes is seamless.

Zener diode VR2 and resistor R5 form the latching output over-voltage protection (OVP) circuit. Increased voltage at the output

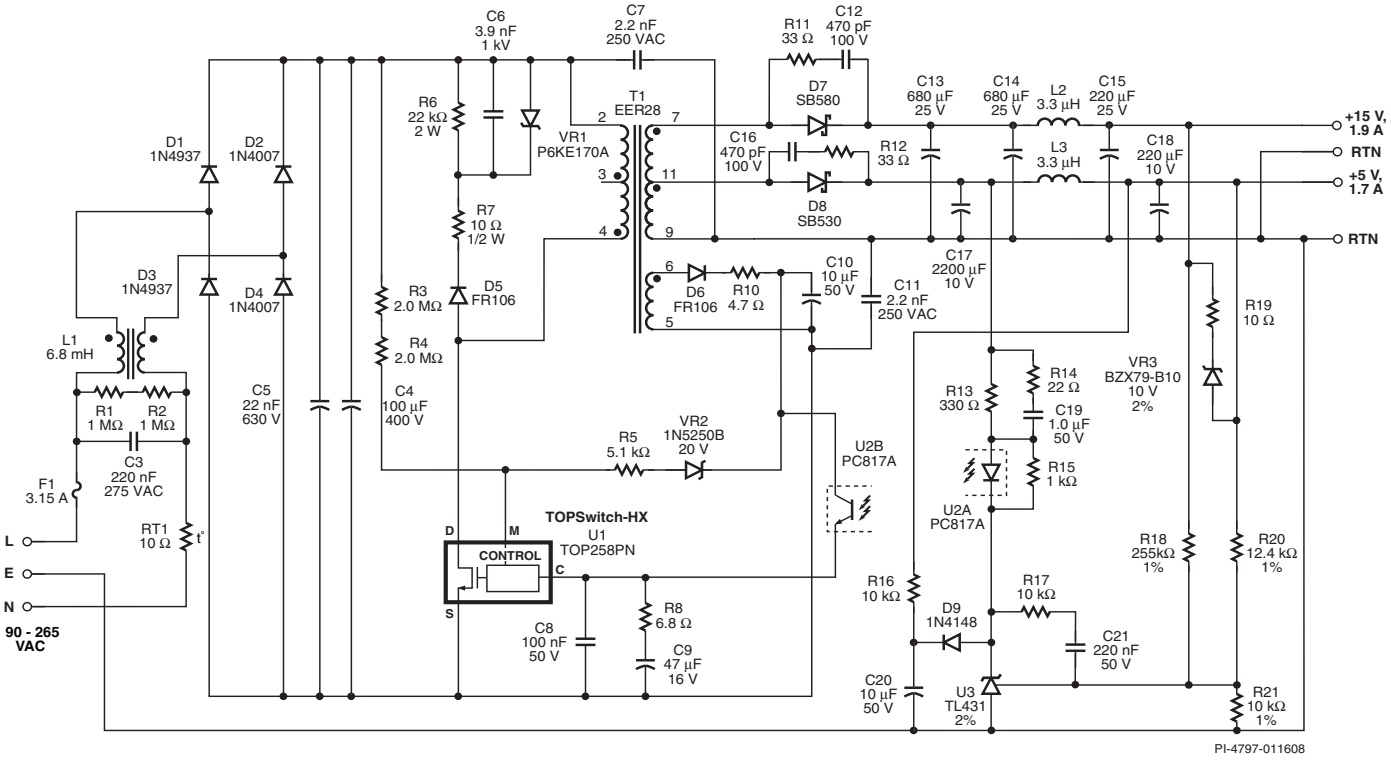

Figure 1. Universal input, 35 W Output, LCD Power Supply, Using a TOP258PN With No External Heat Sink.

will also result in an increased voltage at the output of the bias winding. Zener VR2 will break down, and current will flow into the M pin of U1. When the M pin current exceeds 112 µA, the M pin voltage is internally reduced by 0.5 V. If the M pin current exceeds 336 µA, the OV condition causes a latched shutdown. If the M pin current is between 112 µA and 336 µA for >100 µs, the shutdown is hysteretic. Resistor R5 defines the M pin current.

Output voltage feedback is derived from both the outputs for better cross-regulation. Capacitor C19 and resistor R14 form the phase boost network and provide adequate phase margin to ensure stable operation over the entire operating voltage range. Resistors R19 and VR3 improve cross regulation when only the 5 V output is loaded, preventing the 15 V output operating at the higher end of the specification.

Key Design Points

- Capacitor C5 is a decoupling capacitor connected across the DC supply and is located physically close to the high frequency switching circuit, which helps in reducing differential mode EMI.
- If latching OVP is desired, the value of R5 should be reduced to 20 Ω to allow for more current into the M pin.
- Design the RCD clamp (R6, R7, C6 and D5) for normal operation, thereby maximizing efficiency at light load. Zener diode VR1 provides a defined maximum clamp voltage and typically only conducts during load transients or during an overload condition.
- The secondary side snubber (R11, C12, R12 and C16) reduce high frequency secondary diode ringing and improve EMI.
- In a three-wire system, placing Y capacitors between line/neutral and earth ground helps reduce common mode EMI.
- As the output return is connected to safety earth ground, two 2.2 nF Y capacitors (C7 and C11) are acceptable. For floating outputs, the maximum capacitance is normally limited to 1 x 2.2 nF due to line frequency leakage current limits.
- Soft finish capacitor C20 ensures no output overshoot at start-up. Diode D9 isolates this capacitor from the feedback loop after start-up. Resistor R16 allows a path for this capacitor to discharge into the 5 V load.

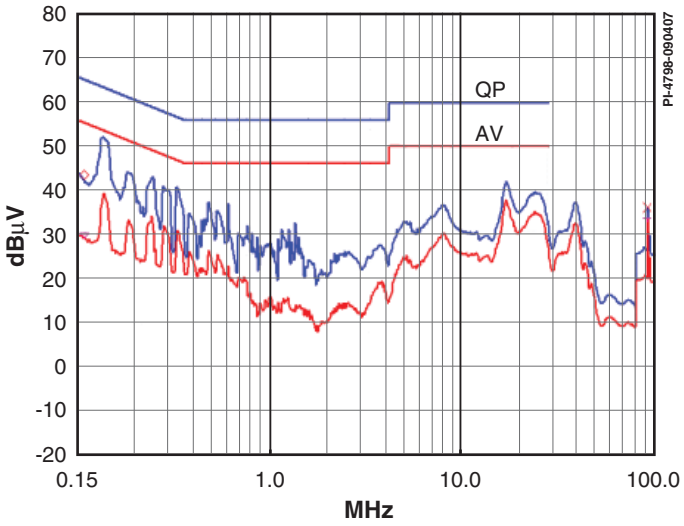

Figure 2. Worst Case Conducted EMI (230 VAC).

Transformer Parameters

Core Material	EER28 NC-2H or equivalent, gapped for ALG of 148 nH/t²
Bobbin	EER28, 12 pin, Horizontal
Winding Details	3mm margins on both sides of bobbin to meet safety Primary: 20T × 1 AWG 26, tape Bias: 9T × 2, AWG 26, 3 layers, tape 5 V: 3T, foil 0.52 mm thickness 15 V: 5T × 3, AWG 26, 3 layers tape Primary: 50T × 1, AWG 26, tape
Winding Order	Primary-1 (4-3), Bias (6-5), 5 V (11-9), 15 V (7-11), Primary-2 (3-2)
Primary Inductance	1041 µH, ±10%
Resonant Frequency	1000 kHz (minimum)
Leakage Inductance	30 µH (maximum)

Table 1. Transformer Parameters. (NC = No Connection).

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