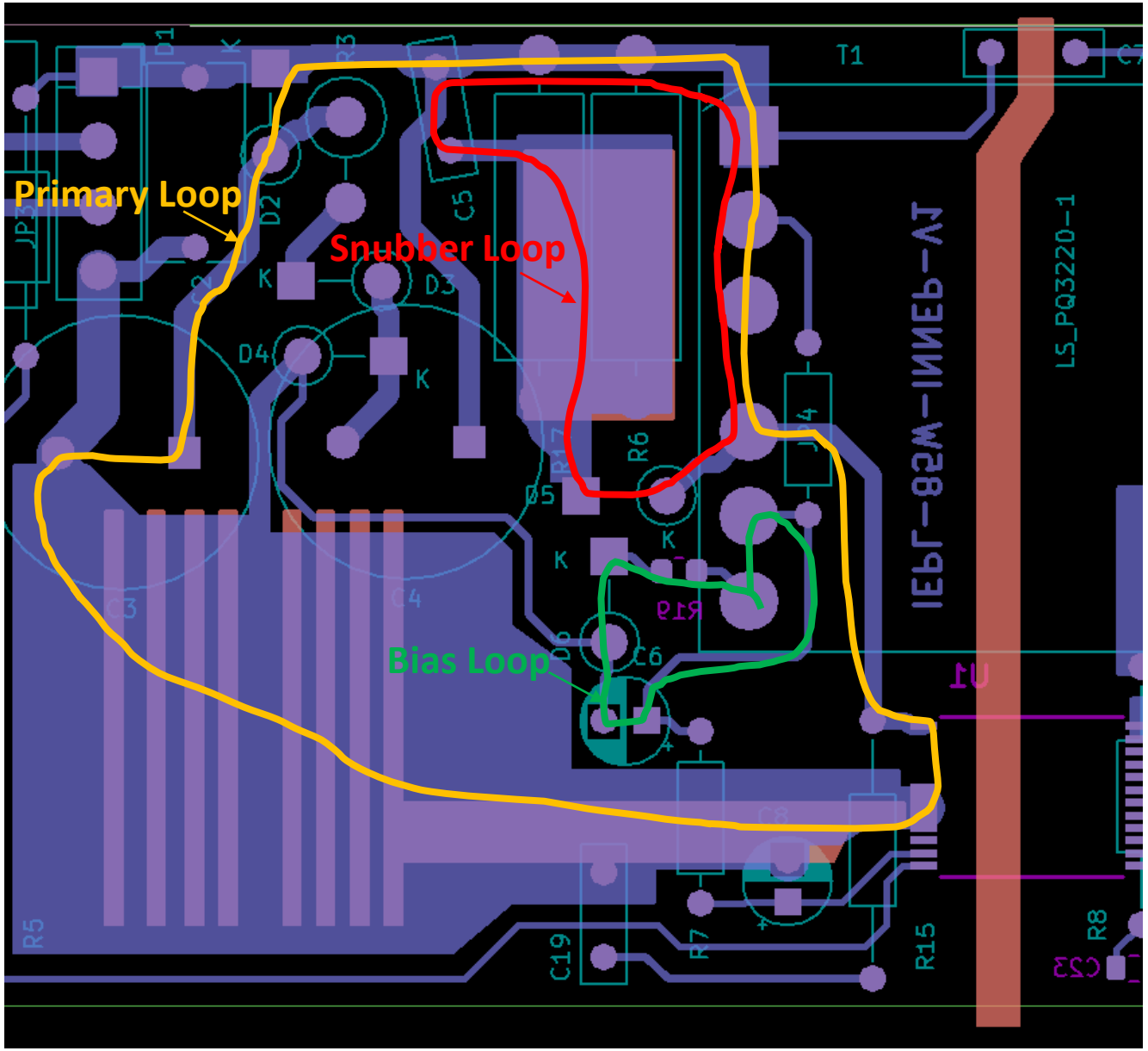
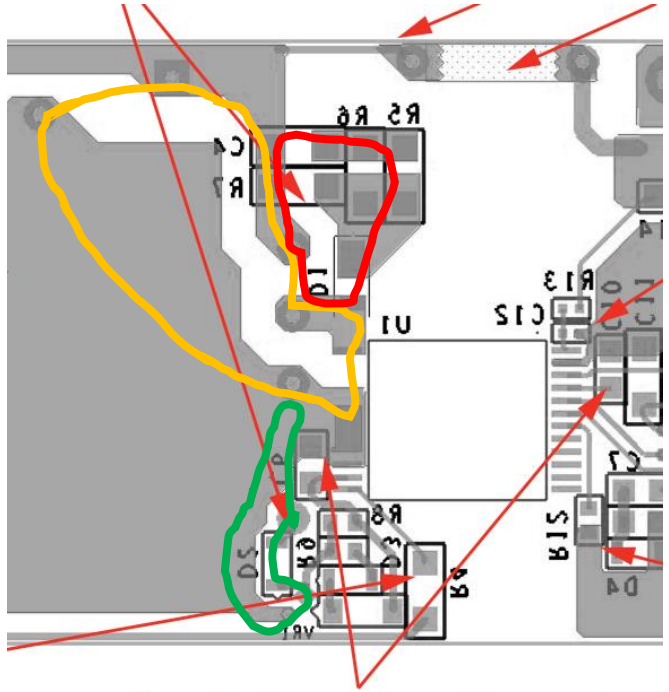
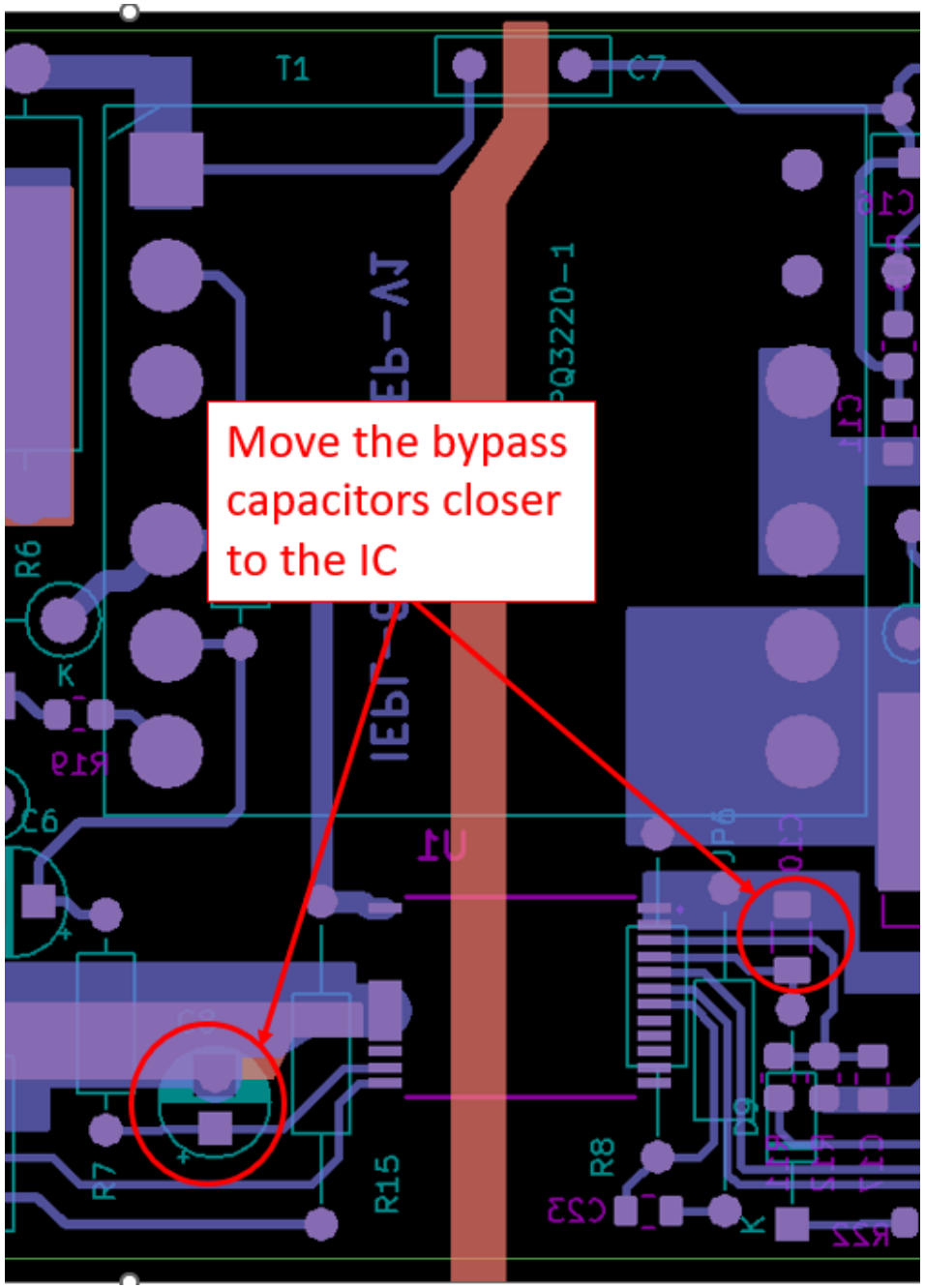


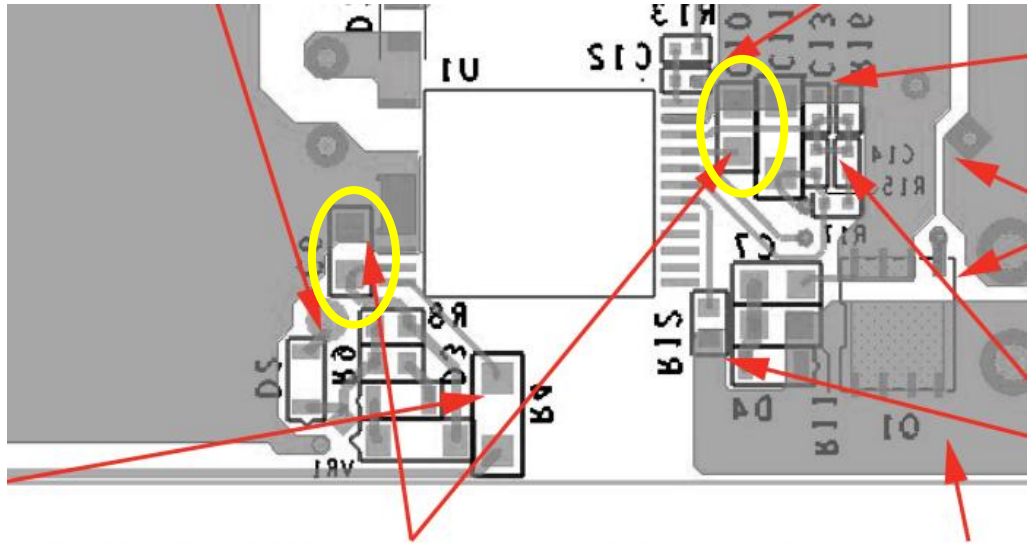
All loop should form a small and compact as possible.

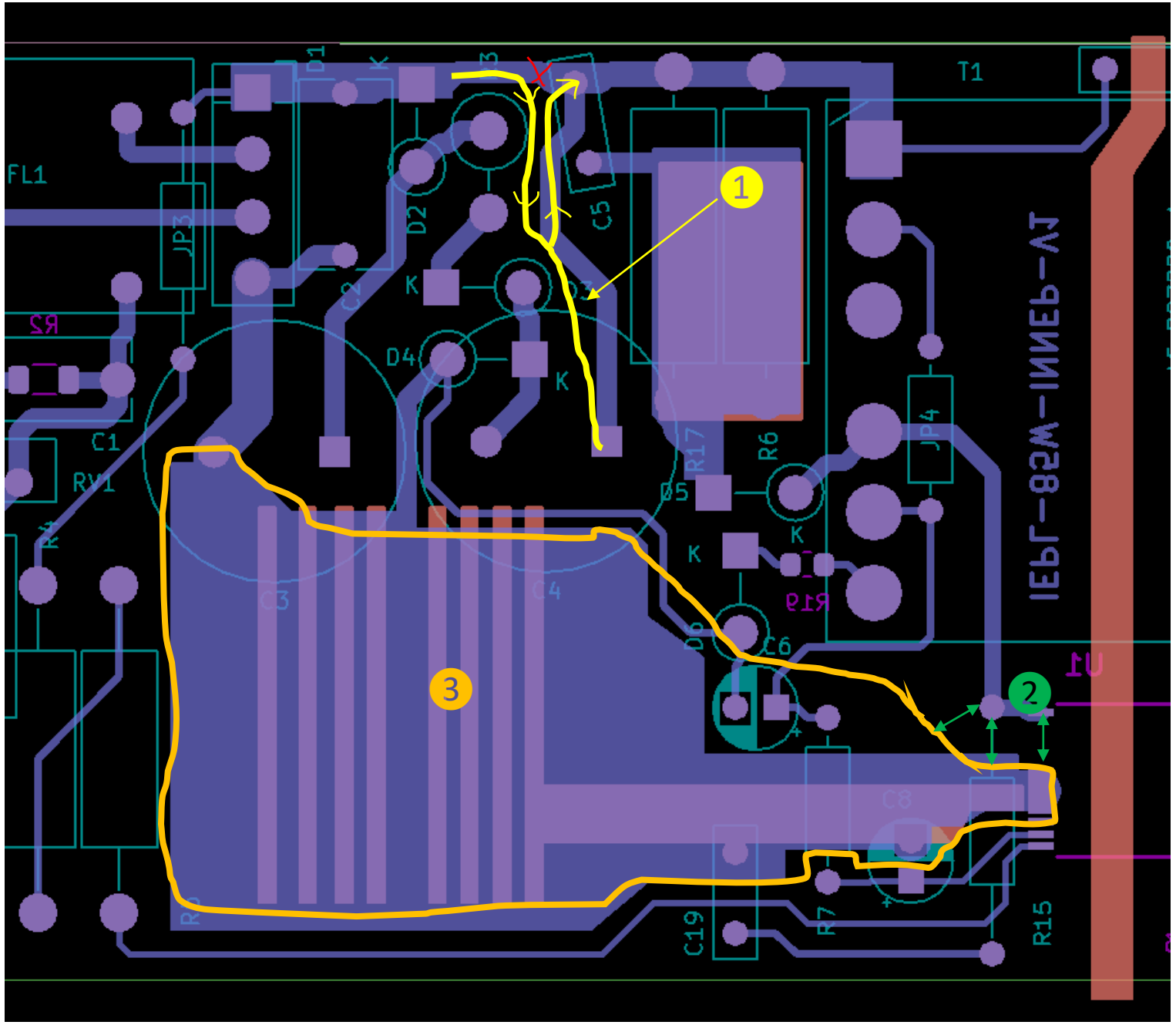
It is recommended that Snubber and Bias loop should be in the outside of Primary loop. The reason for this is that we are working on a high dV/dt switching power supply, any additional inductance(copper trace) will introduce unwanted signal that may result to unwanted behavior. Please see image below for your reference





Please move the C8 and C10 closer to the BPP and BPS of the InnoSwitch. If this not close to the pin, it may introduce unwanted behavior. I strongly recommend also using ceramic capacitor for C8 as shown in the image.



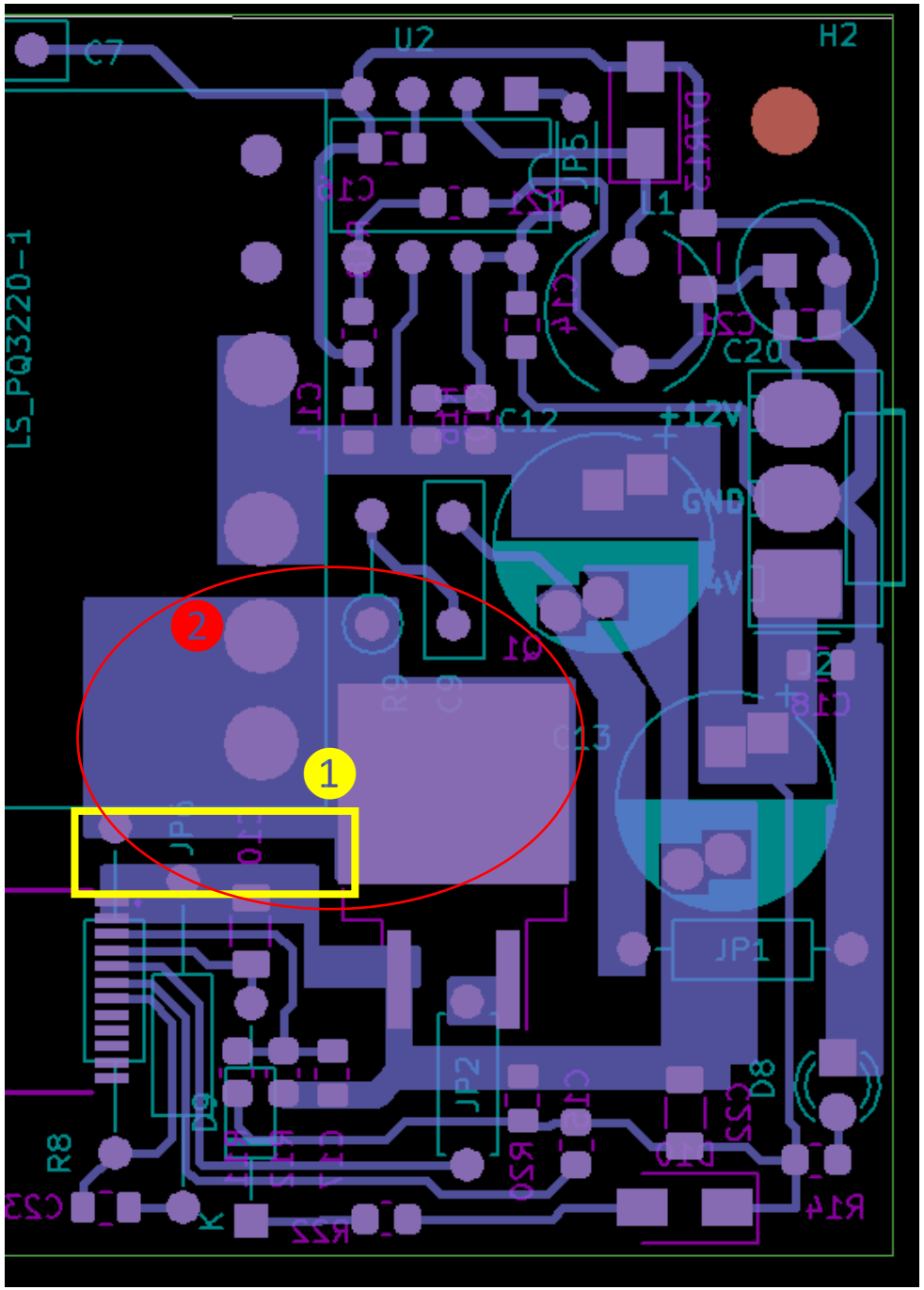


❶ The positive terminal of C4 should be connected in start connection. The source should flow first in the C4 before it goes to transformer terminal 1.

❷ Make sure that distance between the source ground and the drain pin connection should be the same as creepage between the source and drain pin of the Innoswitch. Switching across this pins is high dV/dt.

❸ Larger PCB heatsink is needed since you are dealing with a 90W power supply. Adding vias may also help.

Noticed also that some of the through hole components are overlapped.



❶PCB Copper layout distance between the ground and switching node of the mosfet Q1 is too close. I strongly recommend to move the Q1 further and copper to the ground.

❷ Since the secondary rms current is around 5A, a larger PCB copper area is need in Q1. A thermal runway may happen that couse unwanted signal especially the mosfet used is 180mΩ rds(on). I would also recommend using lower rds(on) mosfets (<10mΩ). Adding vias also may help.

As much as possible. Please follow the layout recommendation especially the peripheral connections near the IC.

You can also check the DER-993, as sample reference. This design uses PQ transformer.

Layout Example