Design Example Report

Title	***24 W HVDCP Quick Charge 2.0 Compatible High Efficiency CV/CC Adaptor Using TOPSwitch™-JX TOP268VG and ChiPhy™ CHY100D***
Specification	90 VAC – 265 VAC Input; 12 V, 9 V, 5 V / 2 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	DER-381
Date	April 11, 2014
Revision	1.2

Summary and Features

- HVDCP (High Voltage Dedicated Charging Port) Quick Charge compatible
- Fully supports Quick Charge 2.0 class A specification (5 V, 9 V, and 12 V output voltages)
- Small PCB size, 67 mm x 39 mm
- 132 kHz switching frequency reduces size of magnetics
- Tight voltage regulation for CV mode and tight current regulation for CC mode
- Excellent transient load response
- Hysteretic thermal overload and overvoltage protection with automatic recovery
- Power Integrations eDIP low-profile package
- Meets conducted EMI with >-4dB QP margin

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing an adapter power supply utilizing a TOPSwitch-JX TOP268VG. This power supply is intended as a general purpose evaluation platform for ChiPhy family. This adapter designed with CHY100D operates from universal input and provides selectable output voltages (i.e. 5 V, 9 V, and 12 V) with a maximum constant current of 2 A.

The TOPSwitch-JX, by design, maintains virtually constant efficiency across a very wide load range without using special operating modes to meet specific load thresholds. This optimizes performance for existing and emerging energy-efficiency regulations. Maintaining constant efficiency ensures design optimization for future energy-efficiency regulation changes without the need for redesign.

The low MOSFET capacitance of TOPSwitch-JX allows a higher switching frequency without the efficiency penalty which occurs with standard discrete MOSFETs. The 132 kHz switching frequency (rather than the 40 kHz to 60 kHz frequency used for a discrete MOSFETs) reduces the transformer size required, thus reduces cost.

The power supply meets Energy Star 2.0 >80% average-efficiency, no-load <300 mW at 230 VAC and meets CISPR conducted EMI with more than 4dB margin.

This power supply offers thermal overload protection with auto-recovery using large hysteresis. It is primary-side sensed output overload and overvoltage protection, even with a single fault.

This document provides complete design details including specifications, the schematic, bill of materials, PCB layout and transformer design and construction information. This information includes performance results pertaining to regulation, efficiency, transient load, and conducted EMI scans.

Figure 1 – Plastic Enclosure (Dimension: 74 mm x 44 mm x 23 mm).

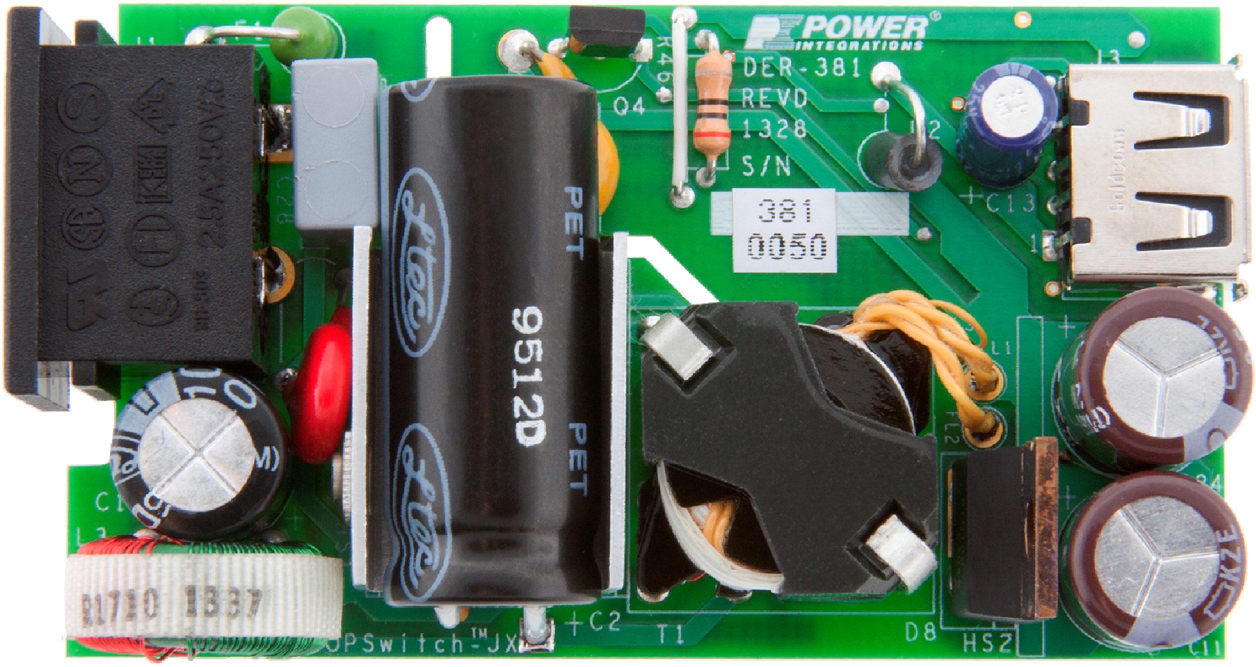


Figure 2 – Populated Circuit Board Photograph, Top.

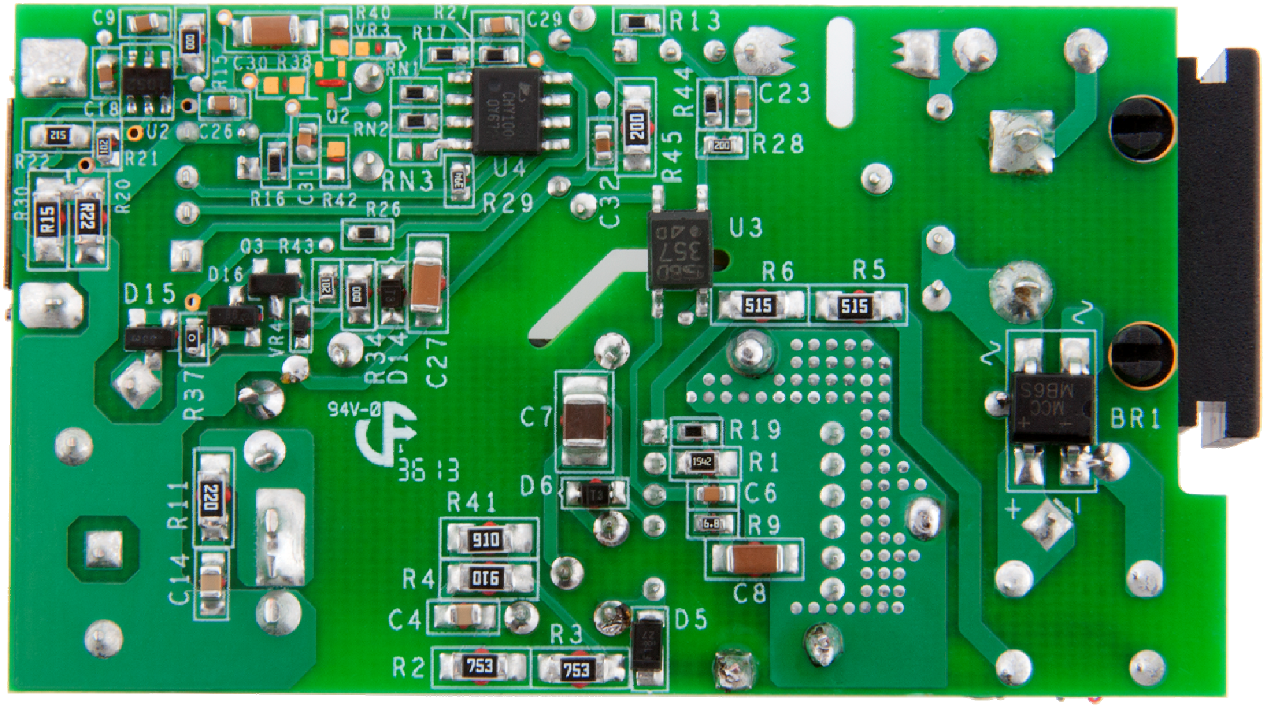


Figure 3 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.15	W	5V
Output						
Output Voltage 1	V_{OUT1}		12		V	± 2%, PCB
Output Current 1	I_{OUT1}	0		2	A	
Output Ripple Voltage 1	$V_{RIPPLE1}$			120	mV_{PP}	20 MHz bandwidth
Output Voltage 2	V_{OUT2}		9		V	± 2%, PCB
Output Current 2	I_{OUT2}	0		2	A	
Output Ripple Voltage 2	$V_{RIPPLE2}$			100	mV_{PP}	20 MHz bandwidth
Output Voltage 3	V_{OUT3}		5		V	± 2%, PCB
Output Current 3	I_{OUT3}	0		2	A	
Output Ripple Voltage 3	$V_{RIPPLE3}$			100	mV_{PP}	20 MHz bandwidth
Total Output Power						
Continuous Output Power	P_{OUT}			24	W	Measured at P_{OUT} 25 °C; 12 V Output- 1.5 A Load
Efficiency						
Full Load	η		85		%	Measured at P_{OUT} 25 °C; 12 V Output- 1.5 A Load
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	$\eta_{ES2.0}$	82			%	Per ENERGY STAR V2.0
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	-5	25	35	°C	Free convection, sea level

3 Schematic

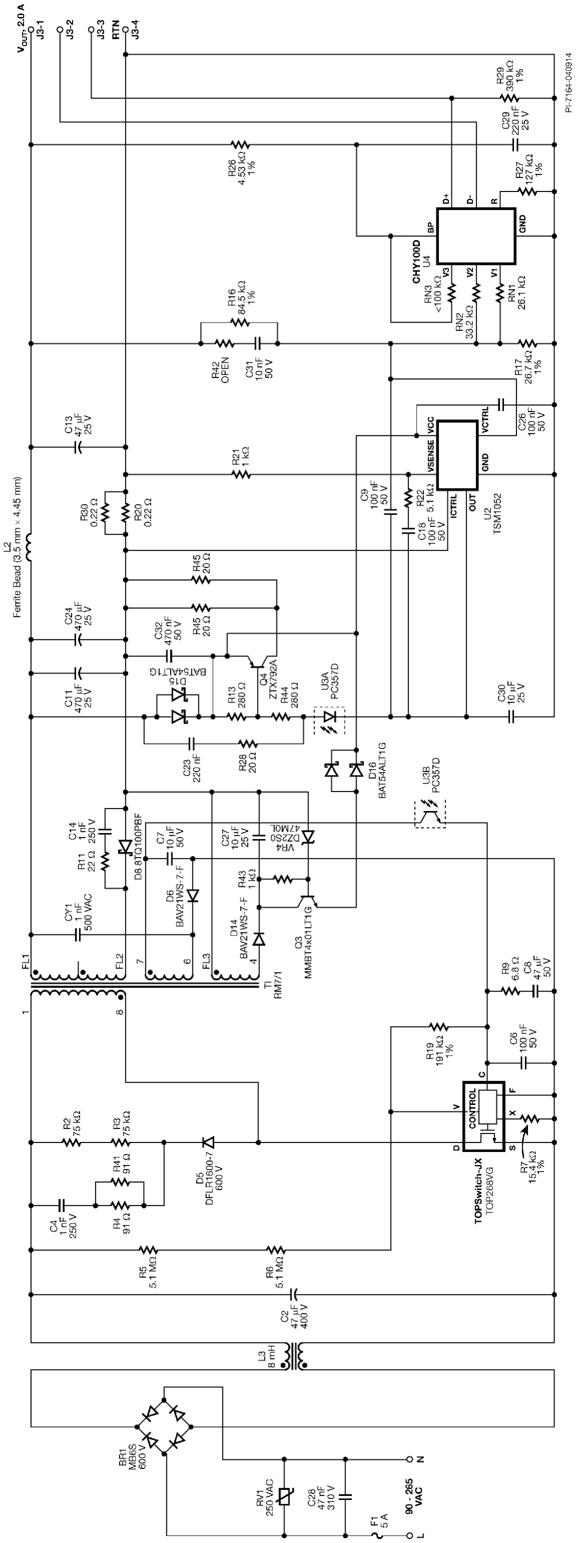


Figure 4 – Schematic.

4 Circuit Description

This power supply employs a TOP268VG integrated off-line switcher IC, (U1), in a flyback topology for low no-load, high efficiency and compact power supply operating from universal inputs and providing selectable outputs namely 12 V – 2 A, 9 V – 2 A, 5 V – 2 A output. IC U1 has an integrated 725 V MOSFET and a multi-mode controller. It regulates the output by adjusting the MOSFET duty cycle, based on the current fed into its CONTROL (C) pin.

4.1 High-Voltage Dedicated Charging Port (CHY100D) for Quick Charge Feature

The power supply was designed to provide selectable output voltages (i.e. 5 V, 9 V, and 12 V) with a maximum constant current of 2 A. The default output (i.e. No-load is connected) is 5 V. The output voltage selection is determined from the logic signal interfaced through D+ and D- from a load. The logic signal will generate a logic signal low from its outputs (i.e. V1-SEL_N, V1-SEL_N, V3-SEL_N) to pull down the nodes of the divider network R17, RN1, RN2, and RN3 to provide a corresponding output voltage.

4.2 Input EMI Filtering

Fuse F1 provides catastrophic fault protection to the circuit, and isolates it from the AC source. Diode BR1 rectifies the AC input. Capacitor C1 and C2 filters the resulting DC. Bulk capacitor C1 reduces differential-mode noise EMI. Inductor L3 filters common-mode EMI. This input filter is compliant to UL standard 60950-1 without bleed resistor to allow safe removal of the AC source.

4.3 TOPSwitch-JX Primary

The EcoSmart® feature of U1 automatically provides constant efficiency over the entire load range. It uses a proprietary Multi-cycle-modulation (MCM) function to eliminate the need for special operating modes triggered at specific loads. This simplifies circuit design since it removes the need to design for aberrant or specific operating conditions or load thresholds.

A switching frequency of 132 kHz was chosen (vs. 66 kHz) to minimize transformer size. This high frequency operation has no major impact on efficiency or EMI thanks to very low capacitance PI power MOSFET technology and proprietary frequency jitter feature.

The TOP268VG regulates the output by adjusting the duty cycle based on the current into its CONTROL (C) pin. The power supply output voltage and current are sensed on the secondary side by shunt regulator U2 and provides a feedback signal to the primary side through optocoupler U3.

Capacitor C8 provides the auto-restart timing for U1, start-up and loop compensation. At start-up this capacitor is charged through the DRAIN (D) pin. Once it is charged U1 begins to switch. Capacitor C8 stores enough energy to ensure the power supply output reaches regulation. After start-up, the bias winding powers the controller via the current through the opto coupler into the CONTROL pin. Bypass capacitor C6 is placed as physically close as possible to U1. Resistor R9 provides additional compensation to the feedback loop.

The clamp network formed by C4, R2, R3, R4, R41 and D5 limits the drain voltage (preventing spikes at MOSFET turn off) and dissipates transformer leakage inductance energy.

To further improve the no load input power at high input voltage resistor R19 was added to provide a current of 25 µA into the V pin from the C pin. This changes the operating point of the CONTROL pin (line feed forward function). With R19 fitted, the absolute current into the CONTROL pin to set a given duty cycle is reduced by ~50% reducing power consumption from both the bias winding and output. Line sense resistors R5 and R6 value were set at approximately 75 VAC for the cut-in voltage.

X pin resistor R1 was set to reduce the internal current limit of U1. This allows the supply to limit the output power to <100 VA at high line and deliver the rated output at low line.

4.4 Thermal Overload Protection

IC U1 has an integrated, 100% tested, accurate latching thermal-overload protection feature. If the junction temperature reaches +142 °C (during a fault condition), U1 shuts down. The latch condition resets once the input voltage has been removed and C1 and C2 discharge.

4.5 Output Rectification, Filtering, Secondary Bias and Feedback Control

Schottky diode D8 rectifies the output. A snubber network (C14, R11) dampens ringing across the diodes and reduces high frequency conducted and radiated noise. These two components were chosen with smaller values to allow high-frequency ringing to be damped while keeping any power dissipation they cause at no-load to a minimum. Ferrite bead L2 and capacitor C13 form an output second stage filter. Capacitors C11 and C24 provide output filtering.

Because of the CV/CC function, the secondary bias has to be derived from both the output voltage (flyback winding) and forward bias winding. For CV operation mode, secondary bias comes from the output voltage, since D16 is blocked by the output voltage. Diode D14 and C27 rectifies the forward bias winding, and a linear regulator formed by Q3, R34, R43 and VR4, convert the voltage across C27 to a constant voltage around 4 V. During CC operation mode, once the output voltage is lower than the output voltage of the linear regulator, the secondary control circuit will be biased from the forward winding.

Resistors R16, RN1, RN2,RN3 and R17 form a voltage divider and set the DC set point of the output. The output voltage is selected through an external toggle board, which has a pre-programmed micro-controller. The micro-controller will determine the output voltage (i.e. 5 V, 9 V, or 12 V) required by the load based on the logic signal from USB terminals D+ and D-. Capacitor C9 and R15 provide compensation for the feedback control loop.

While capacitor C18 and resistor R22 provide compensation feedback control when operating in constant current mode. Resistor R13 and R44 limit the gain of the feedback system to ensure power supply stability throughout the range of operation. RC network C23 and R28 provides phase boost at higher cross over frequency. Resistor R13, R45, R46 and Q4 are used to discharge the output capacitor during output toggle from high voltage to 5 V. At light load, the output discharge network is very important, since the feedback voltage can be higher than reference for long time to saturate the error amplifier, and thus cause huge undershoots.

5 PCB Layout

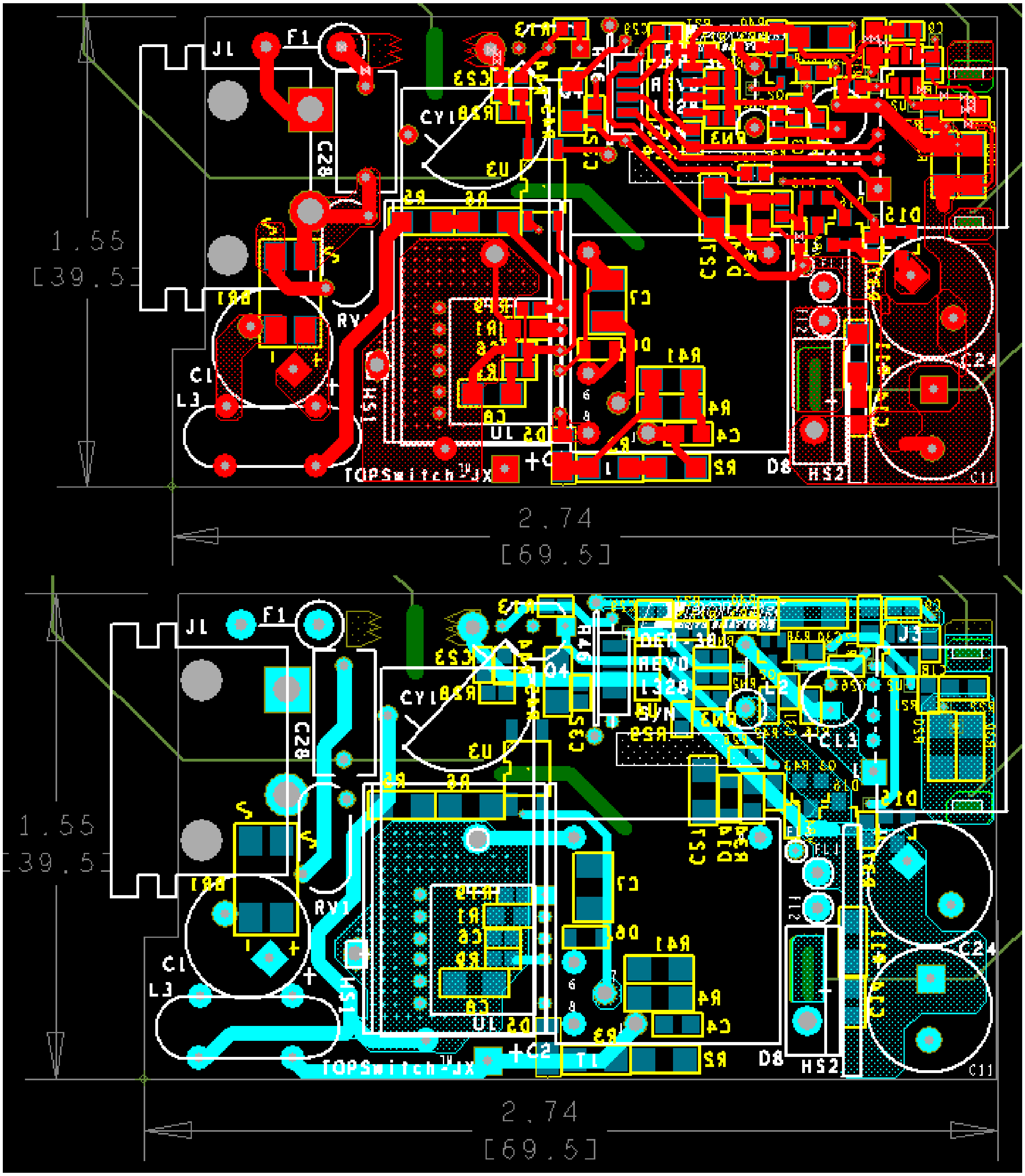


Figure 5 – Printed Circuit Layout Top and Bottom (69.5 mm x 39.5 mm).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	10 µF, 400 V, Electrolytic, Low ESR, 79 mA, (10 x 12.5)	TYD2GM100G13O	Ltec
3	1	C2	47 µF, 400 V, Electrolytic, Low ESR, (12.5 x 30)	EPAG401ELL470MK30S	Nippon Chemi-Con
4	2	C4 C14	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
5	4	C6 C9 C18 C26	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K	TDK
6	1	C7	10 µF, 50 V, Ceramic,X5R, 1210	UMK325BJ106KM-T	Taiyo Yuden
7	1	C8	47µF, 16 V, X5R, 1206	3216X5R1C476M	TDK
8	2	C11 C24	470 µF, 25 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE250ELL471MJ16S	Nippon Chemi-Con
9	1	C13	47 µF, 25 V, Electrolytic, Low ESR, 500 mΩ, (5 x 11.5)	ELXZ250ELL470MEB5D	Nippon Chemi-Con
10	2	C23 C29	220 nF, 25 V, Ceramic, X7R, 0603	06033D224KAT2A	AVX
11	2	C27 C30	10 µF, 25 V, Ceramic, X7R, 1206	C3216X7R1E106M	TDK
12	1	C28	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
13	1	C31	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
14	1	C32	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
15	1	CY1	1 nF, 500Vac, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
16	1	D5	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
17	2	D6 D14	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	D8	100 V, 8 A, Schottky, TO-220AC	8TQ100PBF	Vishay
19	2	D15 D16	30 V,0.2 A, Schottky, SMD, SOT-23	BAT54ALT1G	Diodes, Inc.
20	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	Littlefuse
21	2	FL1 FL2	PCB Terminal Hole, 22 AWG	N/A	N/A
22	1	FL3	PCB Terminal Hole, 30 AWG	N/A	N/A
23	1	HS1	Heat Sink, Custom, Al, 1100, 0.032" Thk		Custom
24	1	J1	AC Input Receptacle	S-01-02A	Sunfair
25	1	J3	CONN USB FMALE TYPE A	USB-AF-DIP-094-H	GOLDCONN
26	1	L2	3.5 mm x 4.45 mm, 68 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2743001112	Fair-Rite
27	1	L3	8 mH, xA, Ferite Toroid, 4 Pin, Output	SNX-1710	Santronics
28	1	Q2	open		
29	1	Q3	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
30	1	Q4	PNP, Power BJT, 70 V, 2 A, TO-92	ZTX792A	Zetex
31	1	R1	15.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1542V	Panasonic
32	2	R2 R3	75 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ753V	Panasonic
33	2	R4 R41	91 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ910V	Panasonic
34	2	R5 R6	5.1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ515V	Panasonic
35	1	R9	6.8 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ6R8V	Panasonic
36	1	R11	22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
37	2	R13 R44	280 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2800V	Panasonic
38	2	R15 R34	0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
39	1	R16	84.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF8452V	Panasonic
40	1	R17	26.7 kΩ, 1%, 1/16 W, Thick Film,	ERJ-3EKF2672V	Panasonic

			0603		
41	1	R19	191 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1913V	Panasonic
42	1	R20	0.22 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQJR22V	Panasonic
43	3	R21 R43	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
44	1	R22	5.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
45	1	R26	4.53 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4531V	Panasonic
46	1	R27	127 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1273V	Panasonic
47	1	R28	20 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ200V	Panasonic
48	1	R29	390 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ394V	Panasonic
49	1	R30	0.15 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8RSJR15V	Panasonic
50	1	R37	0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
51	1	R38,R40,R42,RN3	open		
52	1	R45	20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
53	1	R46	20 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-20R	Yageo
54	1	RN1	26.1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2612V	Panasonic
55	1	RN2	33.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3322V	Panasonic
56	1	RN3	open		
57	1	RV1	250 V, 21 J, 7 mm, RADIAL LA	V250LA4P	Littlefuse
58	1	T1	Bobbin, RM7/I, Vertical, 8 pins with mtg clip CLI/P-RM7 Transformer Transformer	CSV-RM7-1S-8P-C. Clip PN CLI/P-RM7 SNX-R1711 POL-JX025	Ferroxcube Santronics Premier Magnetics
59	1	U1	TOPSwitch-JX, eDIP-12P	TOP268VG	Power Integrations
60	1	U2	IC CONTROLLER CC/CV SMPS, SOT23-6	TSM1052	ST Micro
61	1	U3	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N4J00F	Sharp
62	1	U4	High Voltage Driver	CHY100D	Power Integrations
63	1	VR3	open		
64	1	VR4	4.7 V, 5%, 150 mW, SSMINI-2	DZ2S047M0L	Panasonic
65	1	INSULATION1	Tubing & Sleeving-Non Shrink, #20 AWG TUBING PTFE	TFT20-NT	Parker/Texloc (Atlantic Tubing)
66	1	TAPE1	THERMAL TAPE DOUBLE SIDED .008"	BOND PLY 108 10X10"	Bergquist
67	1	RTV1	RTV 670810.10ZCLR Silico	RTV670810.10ZCLR	GE
68	1	Jumper	0.4 inch #24 AWG, 0.4 (next to R46)	1808	Alpha

7 Transformer Specification

7.1 Electrical Diagram

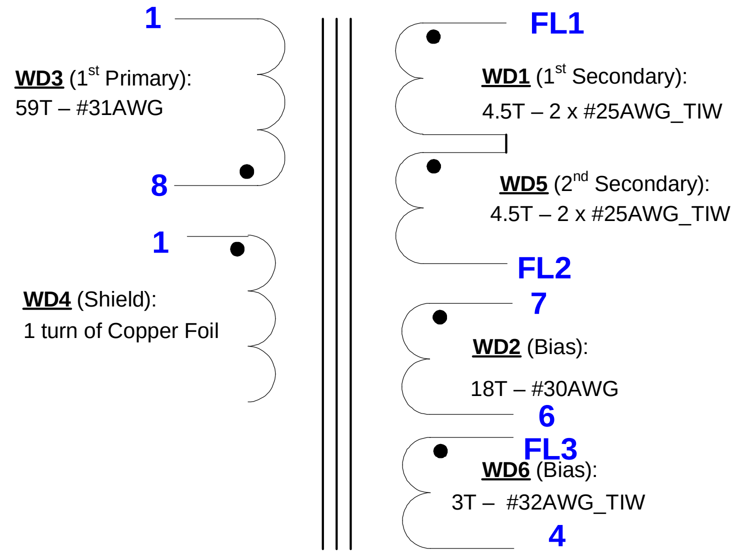


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-8 to pins FL1-FL2.	3000 VAC
Primary Inductance	Pins 1-8, all other windings open, measured at 132 kHz, 0.4 V_{RMS}.	570 µH +5%
Resonant Frequency	Pins 1-8, all other windings open.	>1 MHz
Primary Leakage Inductance	Pins 1-8, with pins FL1-FL2 shorted, measured at 132 kHz, 0.4 V_{RMS}.	<15 µH

7.3 Material

Item	Description
[1]	Core: RM7/I Ferroxcube 3F3 - RM07.
[2]	Bobbin: RM7/I, Vertical, 8 pins (4/4); PI P/N: 25-01014-00.
[3]	Magnet wire: #31 AWG (double coated).
[4]	Magnet wire: #30 AWG (double coated).
[5]	Magnet wire: #25 AWG – Triple Insulated Wire.
[6]	Cooper Foil Tape: 2 mils thick, 6.5 mm wide, 42 mm length, see figures and pictures below for construction.
[7]	Tape: 3M 1298 Polyester Film, 7.0mm wide.
[8]	Tape: 3M 1298 Polyester Film, 11 mm wide.
[9]	Magnet wire: #32 AWG – Triple Insulated Wire.
[10]	Varnish.

7.4 Build Diagram

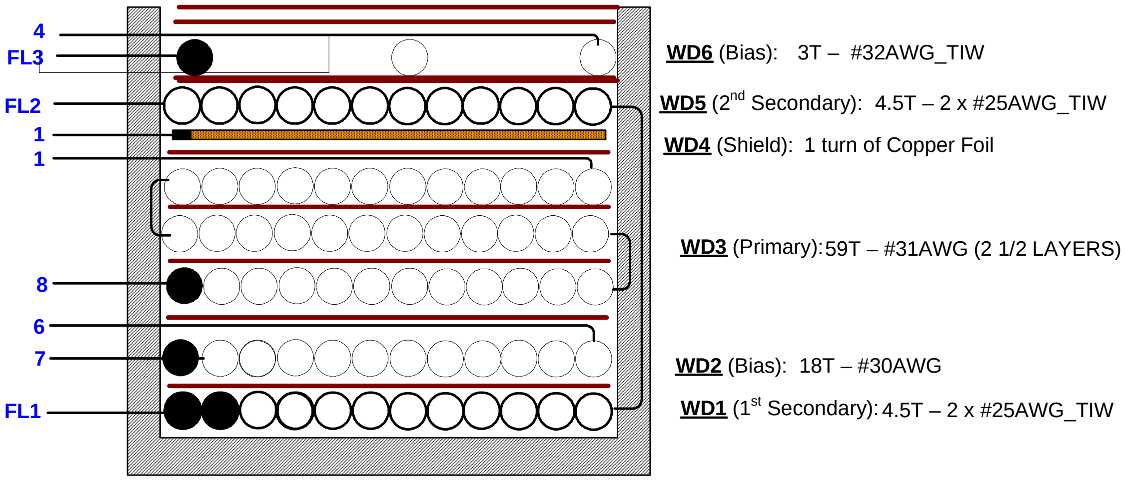


Figure 7 – Transformer Build Diagram.

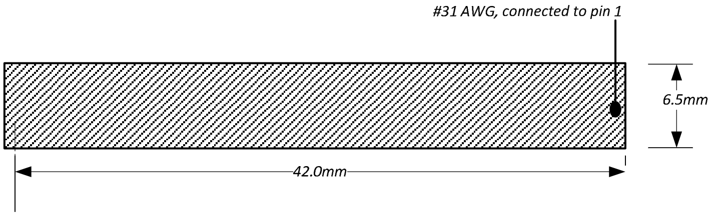


Figure 8 – Copper Foil Tape.

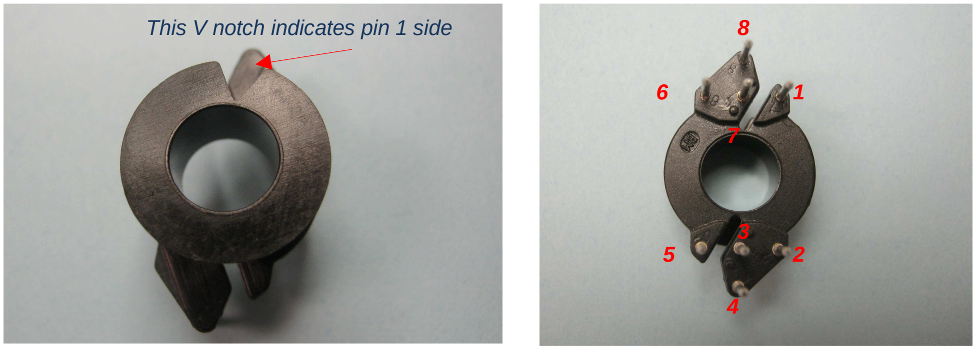
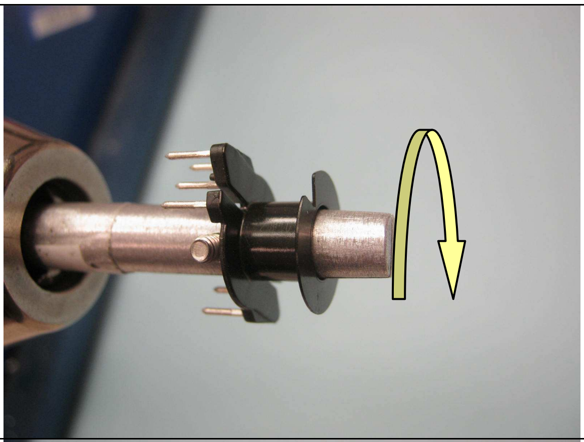
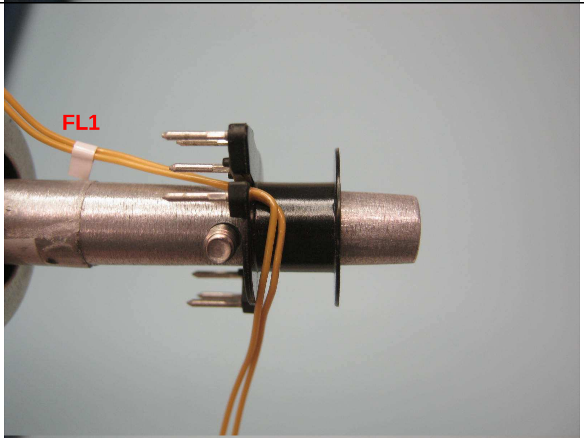


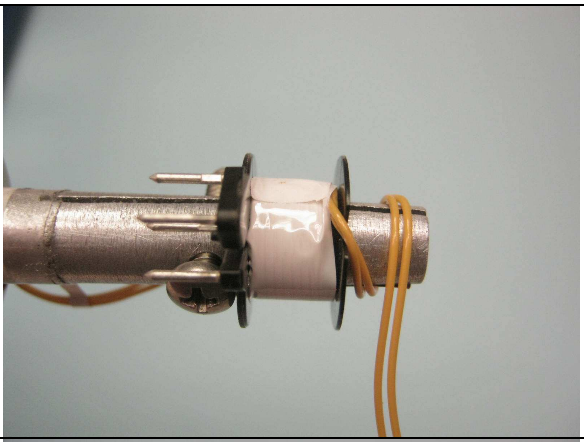
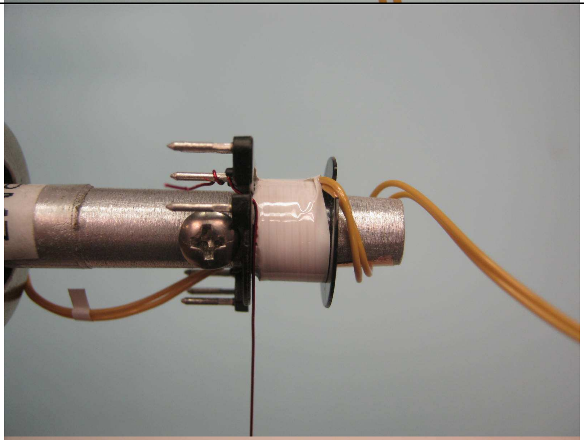
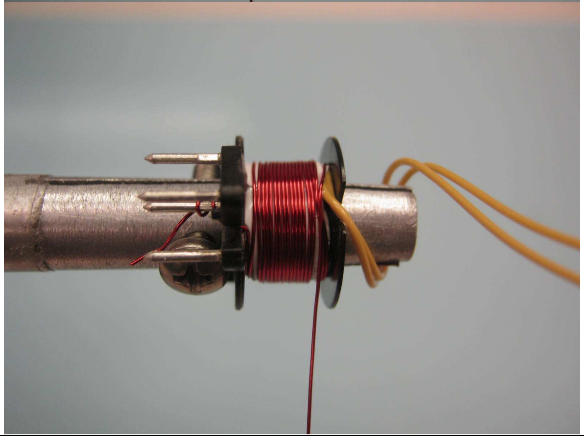
Figure 9 – Pin Out of Bobbin RM7/I – 8 Pins(4/4).

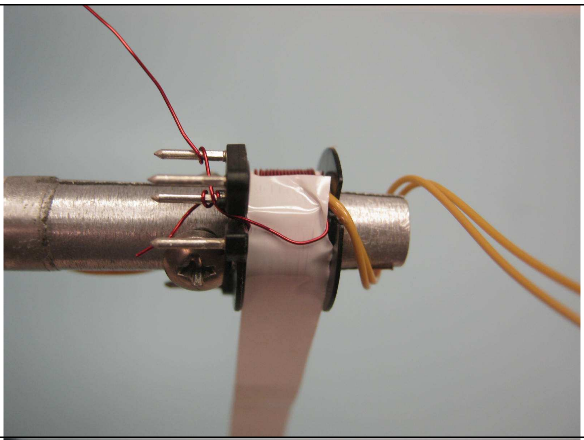
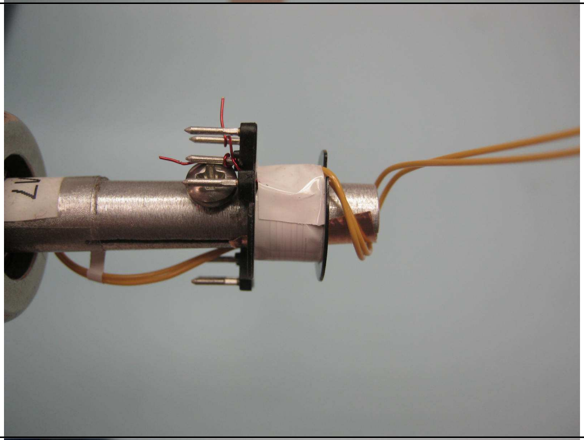
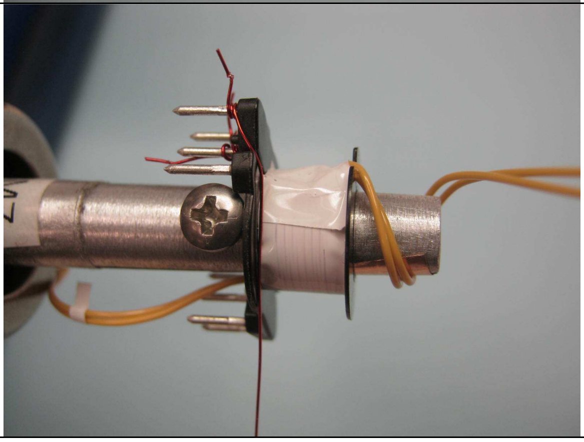
7.5 Construction

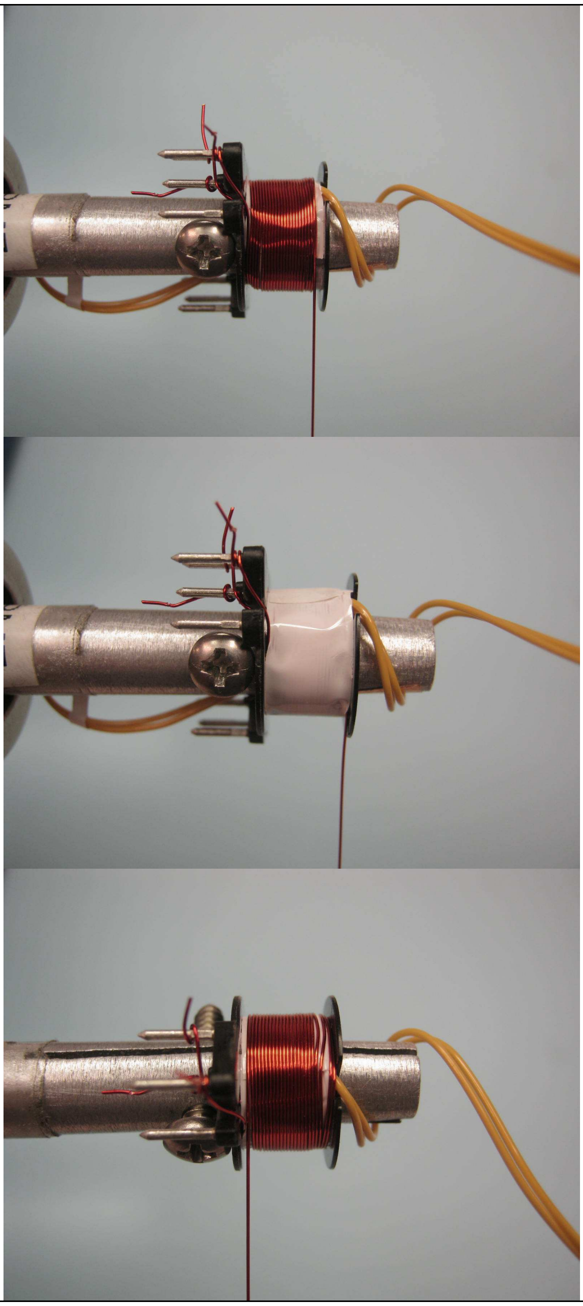
Bobbin preparation	Position the bobbin on the mandrel so pin side on the left hand side. Winding direction is clockwise direction.
WD1 **1st Secondary**	Take about 16” of wire item [5] and leave start end about 1/2 inch at pin 5 position for FL1, wind 4.5 bifilar turns of item from left to right and let the remaining wires hang to the rightmost of the bobbin. Note that the remaining wires will be used in WD6.
Insulation	1 layer of tape item [7].
WD2 **Bias**	Start at pin 7, wind 18 turns of item [4] from left to right, spread the wires evenly on the bobbin, and bring the wires back to the left to terminate at pin 6.
Insulation	1 layer of tape item [7].
WD3 **Primary**	Start at pin 8, wind 22 turns of wire item [3] from left to right for the first layer, then from right to left 22 turns for second layer, continue from left to right 15 turns for third layer, and terminate at pin 1. Place tape item [7] between each layer.
Insulation	1 layer of tape item [7].
WD4 **Shield**	Use copper tape item [6], start at pin 1wind 1 turn, should be overlapped and tuck with tape item [7] when apply tape for insulation to avoid shorting.
Insulation	1 layer of tape item [7].
WD5 **2nd Secondary**	Continue winding the remaining wires from WD1 for 4.5 turns and leave 1/2 inch near pin 5 (FL2).
Insulation	1 layer of tape item [7]
WD6 **Bias**	Start at pin 5 position, also leave ~1” of item [9] for FL3, wind 3 turns from left to right, spread the wires evenly on the bobbin, and bring the wires back to the left to terminate at pin 4.
Insulation	2 layers of tape item [7].
Finish	Gap cores to get 570 µH inductance. Assemble and secure the cores with clips. Dip varnish then dry.

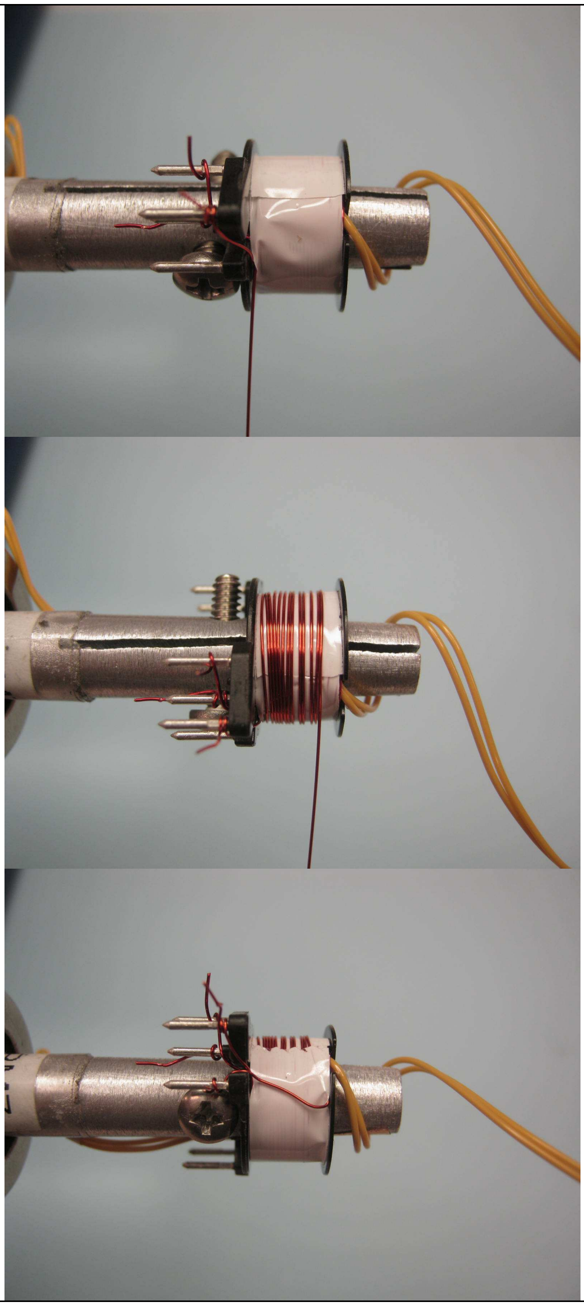
7.6 Winding Illustrations

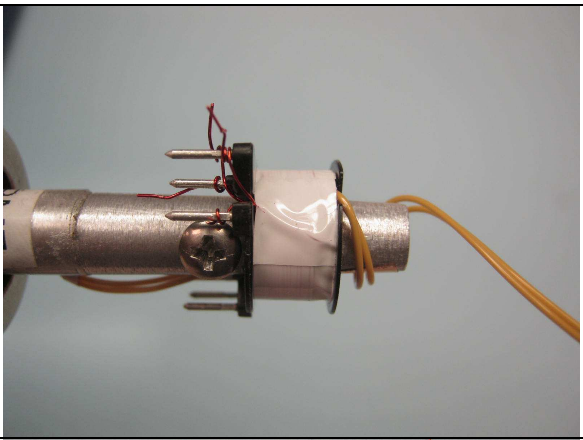
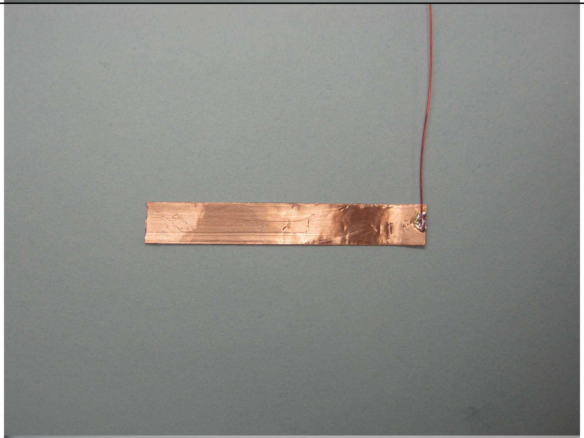
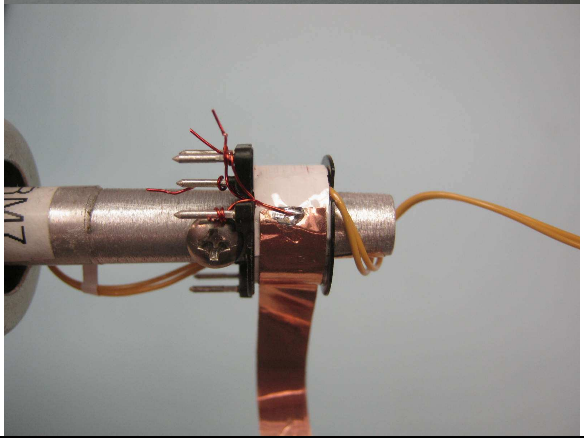
Bobbin Preparation		Position the bobbin on the mandrel so pin side on the left hand side. Winding direction is clockwise direction.
WD1 **1st Secondary**	 	Take about 16" of wire item [5] and leave start end about 1/2 inch at pin 5 position for FL1, wind 4.5 bifilar turns of item from left to right and let the remaining wires hang to the rightmost of the bobbin. Note that the remaining wires will be used in WD6.

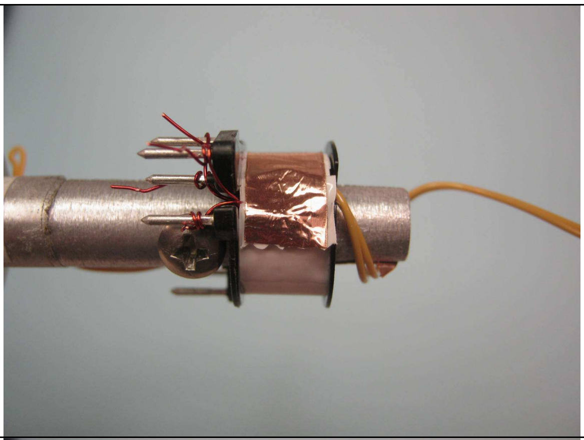
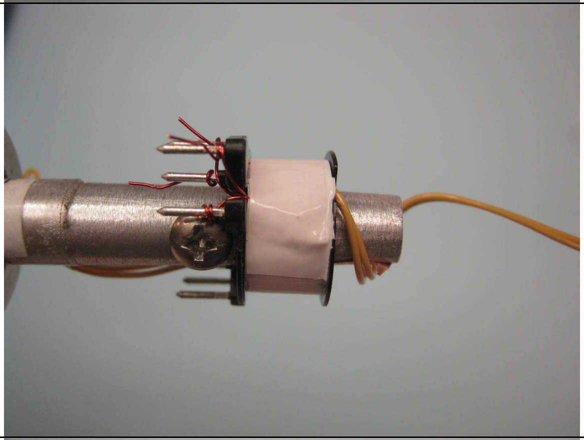
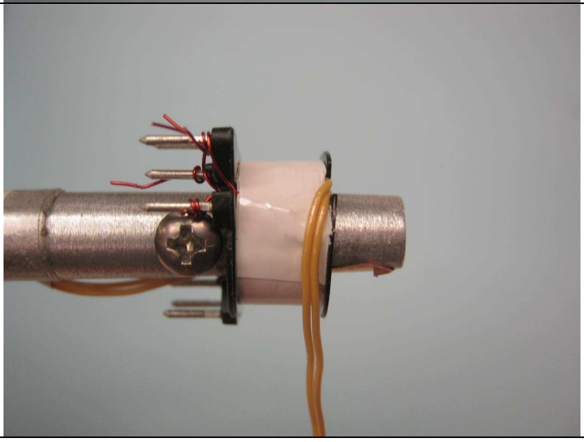
Insulation		1 layer of tape item [7].
WD2 **Bias**	 	Start at pin 7, wind 18 turns of item [4] from left to right, spread the wires evenly on the bobbin, and bring the wires back to the left to terminate at pin 6.

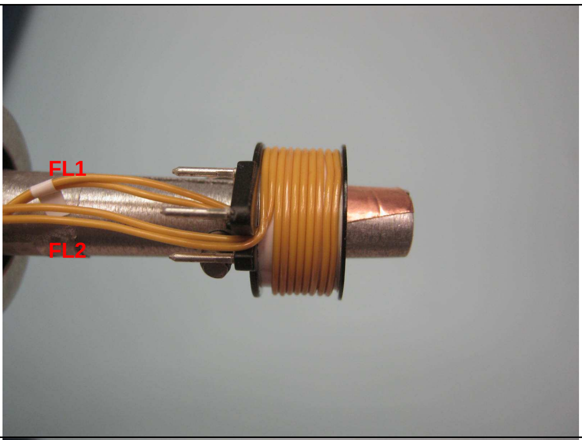
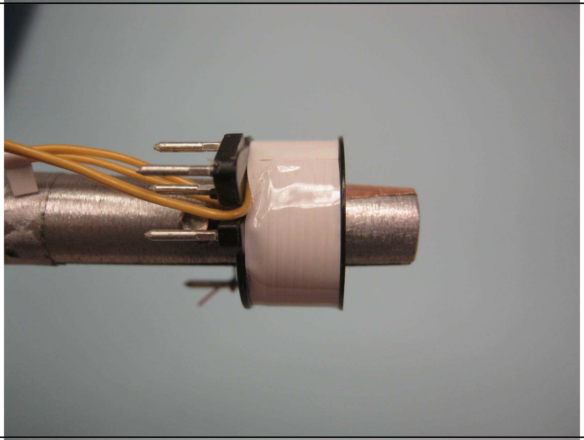
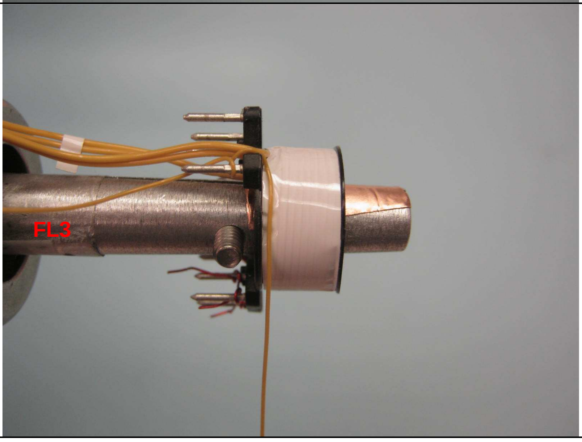
		
Insulation		1 layer of tape item [7].
WD3 **Primary**		Start at pin 8, wind 22 turns of wire item [3] from left to right for the first layer, then from right to left 22 turns for second layer,

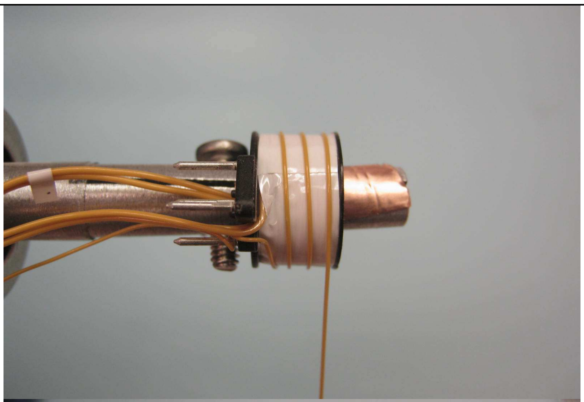
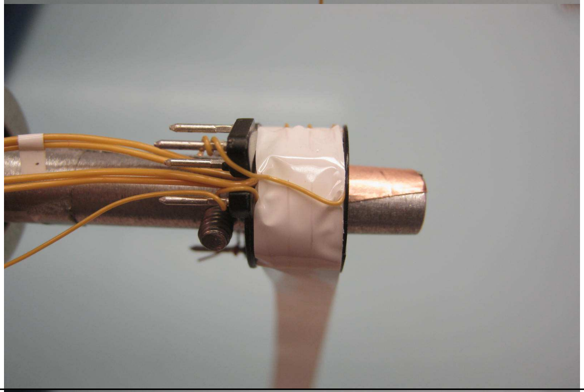
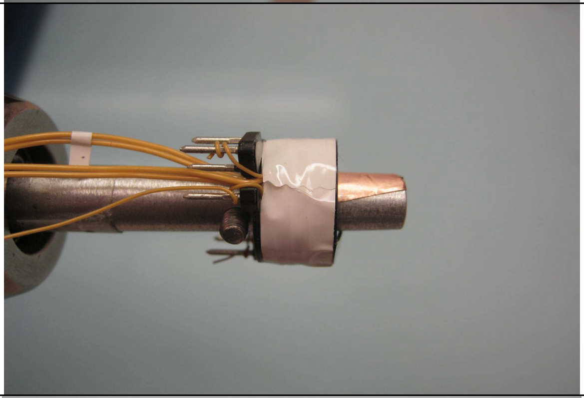
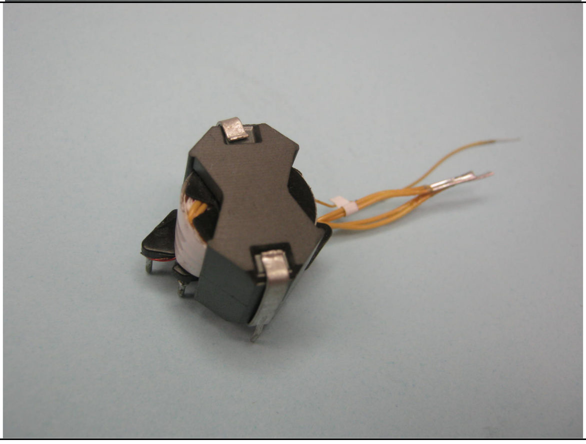
		

WD3 Primary (Cont'd)		continue from left to right 15 turns for third layer, and terminate at pin 1. Place tape item [7] between each layer.

Insulation		1 layer of tape item [7].
WD4 **Shield**	 	Use copper tape item [6], start at pin 1wind 1 turn, should be overlapped and tuck with tape item [7] when apply tape for insulation to avoid shorting.

		
Insulation		1 layer of tape item [7].
WD5 **2nd Secondary**		Continue winding the remaining wires from WD1 for 4.5 turns and leave 1/2 inch near pin 5 (FL2).

		
Insulation		1 layer of tape item [7].
WD6 **Bias**		Start at pin 5 position, also leave ~1” of item [9] for FL3, wind 3 turns from left to right, spread the wires evenly on the bobbin, and bring the wires back to the left to terminate at pin 4.

	 	
Insulation		2 layers of tape item [7].
Finish		Gap cores to get 570 µH inductance. Assemble and secure the cores with clips. Dip varnish then dry.

8 Common Mode Coke Specification (L3)

8.1 Electrical Diagram

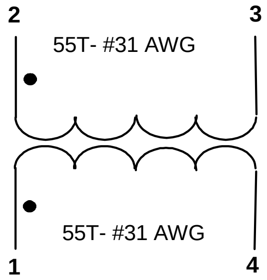


Figure 10 – CMC Electrical Diagram.

8.2 Electrical Specifications

Inductance (LCM)	Pins 1-4 or 2-3. Measured at 100 kHz.	8 mH (Min.)
Leakage (LL)	Pins 1-4 with pins 2-3 shorted or versa at 100 kHz.	80 µH (Max.) ±20%
Core Effective Inductance		4400 nH/N²

8.3 Materials

Item	Description
[1]	Toroid Core: Shenzhen JLW T14*8*5.5C-JL10; Core, Toroidal, 14.35 mm O.D., 7.5 mm Th, 5.5 mm ID; PI P/N: 32-00286-00.
[2]	Magnet Wire: #31 AWG, Heavy Nyleze.
[3]	Center Barrier: FSHP-30, 6.6 mmX 8.1 mm.

8.4 Winding Instructions

- Put item [3] in the middle of the core.
- Use 4 ft of item [2], start at pin 1 wind 55 turns end at pin 4.
- Do the same for another half of toroid, start at pin 2 and end at pin 3.

8.5 Illustrations

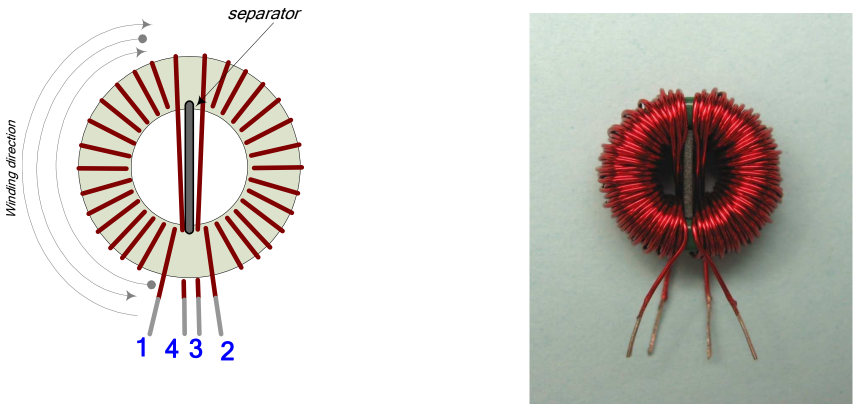


Figure 11 – CMC Build Illustration.

9 Transformer Design Spreadsheet

ACDC_TOPSwitchJX_101012; Rev.1.6; Copyright Power Integrations 2010	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**TOP_JX_101012: TOPSwitch-JX Continuous/Discontinuous Flyback Transformer Design Spreadsheet**
ENTER APPLICATION VARIABLES					
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main)
PO_AVG	24.00			Watts	Average Output Power
PO_PEAK			30.00	Watts	Peak Output Power
Heatsink Type	External		External		Heatsink Type
Enclosure	Adapter				Open Frame enclosure assumes sufficient airflow, while Adapter means a sealed enclosure.
n	0.85			%/100	Efficiency Estimate
Z	0.50				Loss allocation factor
VB	40			Volts	Bias Voltage - Verify that VB is > 8 V at no load and VMAX
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	56.0		56	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	TOP268V			Universal / Peak	115 Doubled/230V
Chosen Device		TOP268V	Power Out	70 W / 112 W	105W
KI	0.37				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			1.119	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			1.845	Amps	Use 1% resistor in setting external ILIMIT. Includes tolerance over temperature. See Fig 37 of datasheet
Frequency (F)=132kHz, (H)=66kHz	F		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	135.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.75				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)
PROTECTION FEATURES					
LINE SENSING					V pin functionality
VUV_STARTUP			101	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			490	Volts	Typical DC Bus Voltage at which

					power supply will shut-down (Max)
RLS			4.4	M-ohms	Use two standard, 2.2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			47	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.07		Margin to current limit at low line.
ILIMIT_EXT_VMIN			1.03	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			1.05	A	Peak Primary Current at VMAX
RIL			15.49	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EFD20		RM7		Core Type
Custom Core (Optional)	RM7				If Custom core is used - Enter Part number here
Bobbin		#N/A		P/N:	#N/A
AE	0.4400		0.44	cm^2	Core Effective Cross Sectional Area
LE	3.0000		3	cm	Core Effective Path Length
AL	2700.0		2700	nH/T^2	Ungapped Core Effective Inductance
BW	6.9		6.9	mm	Bobbin Physical Winding Width
M				mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00				Number of Primary Layers
NS	9		9		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			86	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.64		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.41	Amps	Average Primary Current (calculated at average output power)
IP			1.03	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.77	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.54	Amps	Primary RMS Current (calculated at average output power)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			572	uHenries	Primary Inductance
LP Tolerance	3		3		Tolerance of Primary Inductance
NP			59		Primary Winding Number of Turns
NB			18		Bias Winding Number of Turns
ALG			163	nH/T^2	Gapped Core Effective Inductance
BM			2253	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)

BP			4168	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			845	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1465		Relative Permeability of Ungapped Core
LG			0.32	mm	Gap Length (Lg > 0.1 mm)
BWE			27.6	mm	Effective Bobbin Width
OD			0.47	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.40	mm	Bare conductor diameter
AWG			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			203	Cmils	Bare conductor effective area in circular mils
CMA			374	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			5.32	Amps/mm^2	Primary Winding Current density (3.8 < J < 9.75)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			6.76	Amps	Peak Secondary Current
ISRMS			2.68	Amps	Secondary RMS Current
IO_PEAK			1.50	Amps	Secondary Peak Output Current
IO			1.50	Amps	Average Power Supply Output Current
IRIPPLE			2.23	Amps	Output Capacitor RMS Ripple Current
CMS			537	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			22	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.65	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.77	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.06	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			638	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			77	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			153	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			20	Volts	Output Voltage
IO1_AVG			1.50	Amps	Average DC Output Current
PO1_AVG			30.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			9.00		Output Winding Number of Turns
ISRMS1			2.684	Amps	Output Winding RMS Current
IRIPPLE1			2.23	Amps	Output Capacitor RMS Ripple Current

PIVS1			77	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			537	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.65	mm	Minimum Bare Conductor Diameter
ODS1			0.77	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2	23.00			Volts	Output Voltage
IO2_AVG	0.01			Amps	Average DC Output Current
PO2_AVG			0.23	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			10.40		Output Winding Number of Turns
ISRMS2			0.018	Amps	Output Winding RMS Current
IRIPPLE2			0.01	Amps	Output Capacitor RMS Ripple Current
PIVS2			89	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			4	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			44	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			0.05	mm	Minimum Bare Conductor Diameter
ODS2			0.66	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.31		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire

10 U1 Heat Sink Assembly

The following mechanical drawings are for the custom mechanical designs used in this power supply.

10.1 Heat Sink Fabrication Drawing

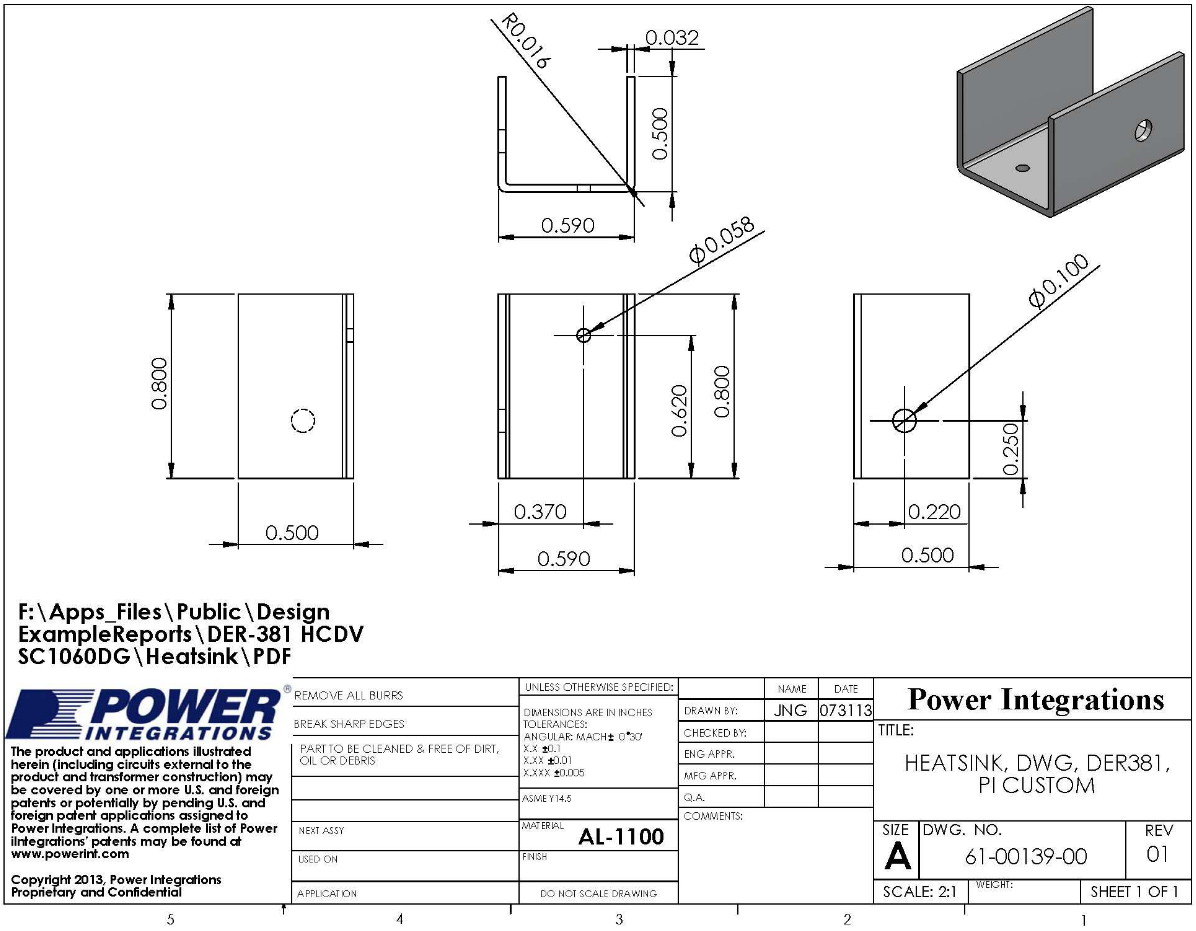
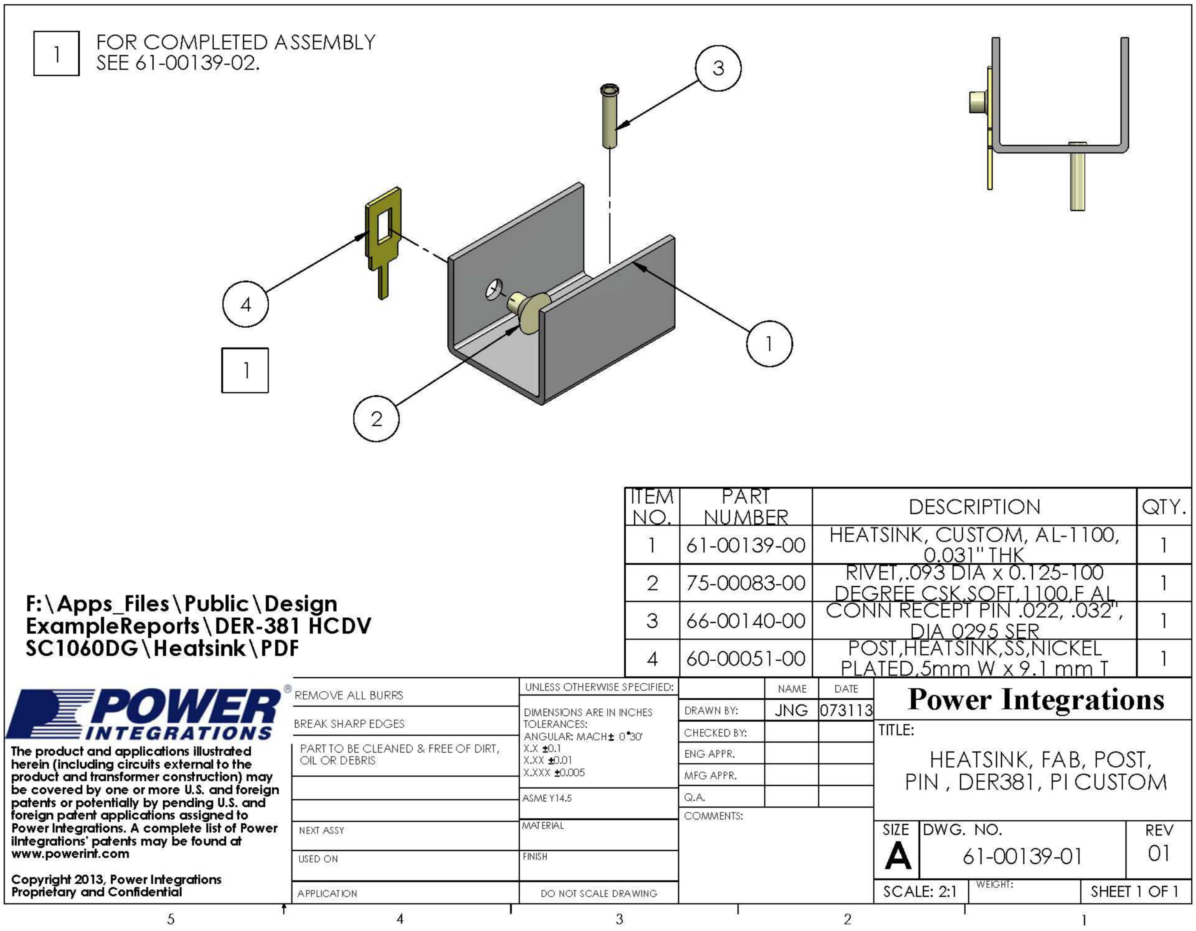


Figure 12 – Heat Sink Fabrication Drawing.

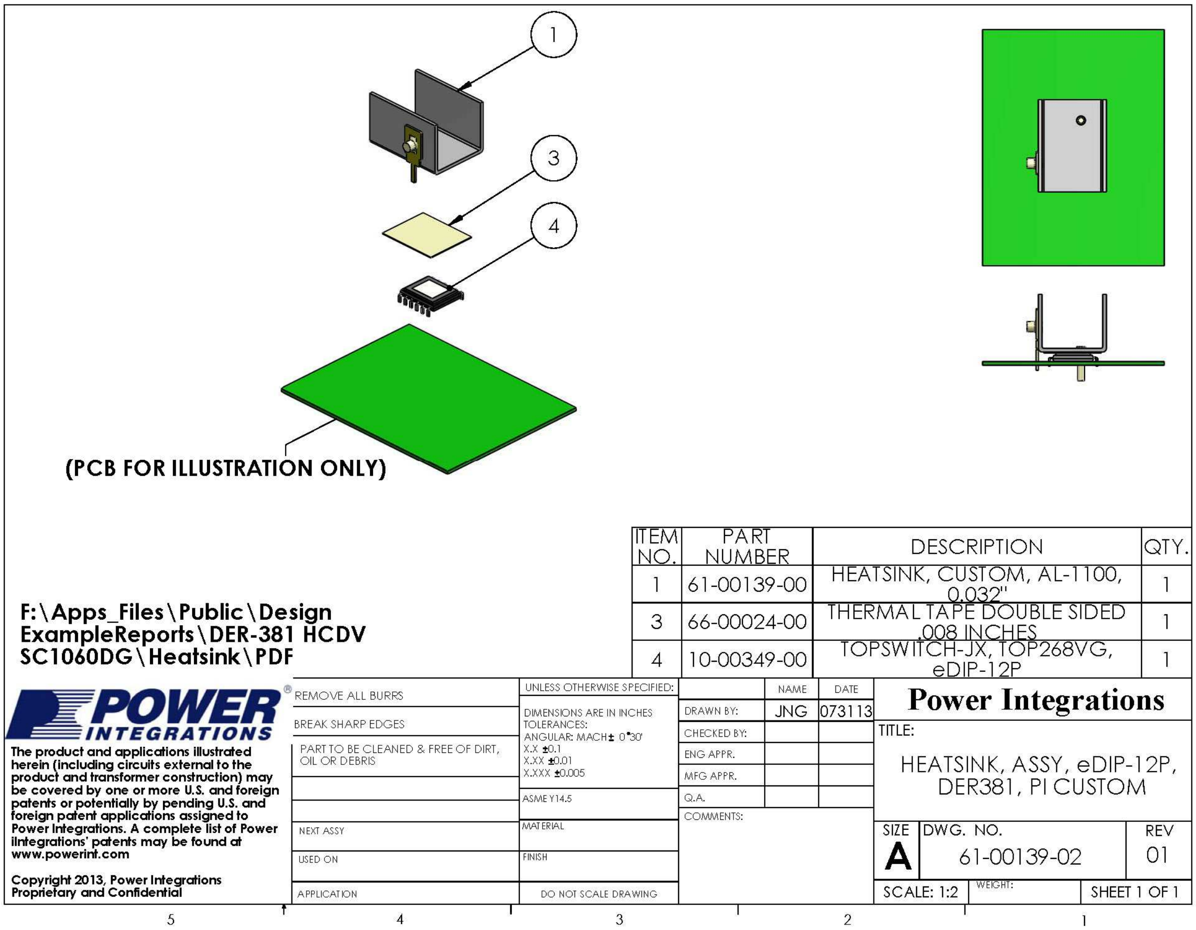
10.2 Heat Sink Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00139-00	HEATSINK, CUSTOM, AL-1100, 0.031" THK	1
2	75-00083-00	RIVET,.093 DIA x 0.125-100 DEGREE CSK,SOFT,1100,F AL	1
3	66-00140-00	CONN RECEPT PIN .022, .032", DIA .0295 SER	1
4	60-00051-00	POST,HEATSINK,SS,NICKEL PLATED,5mm W x 9.1 mm T	1

Figure 13 – Heat Sink Assembly Drawing.

10.3 *Heat Sink and U1 Assembly Drawing.*



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00139-00	HEATSINK, CUSTOM, AL-1100, 0.032"	1
3	66-00024-00	THERMAL TAPE DOUBLE SIDED .008 INCHES	1
4	10-00349-00	TOPSWITCH-JX, TOP268VG, eDIP-12P	1

F:\Apps_Files\Public\Design ExampleReports\DER-381 HCDV SC1060DG\Heatsink\PDF

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power iIntegrations' patents may be found at www.powerint.com

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	073113
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE:
HEATSINK, ASSY, eDIP-12P, DER381, PI CUSTOM

SIZE A
DWG. NO. 61-00139-02
REV 01
SCALE: 1:2
WEIGHT:
SHEET 1 OF 1

Figure 14 – Heat Sink and U1 Assembly Drawing.

11 Performance Data

All tests were performed at room temperature with 90 V / 50 Hz, 115 V / 60 Hz, 230 V / 50 Hz, and 265 V / 50 Hz line input voltages and corresponding frequencies unless otherwise noted. The power supply was put in a plastic case and allowed to warm up for 30 minutes at full load. The input was provided via a 1 meter AC cable. The output was measured at the USB connector mounted on the board.

11.1 Full Load Efficiency

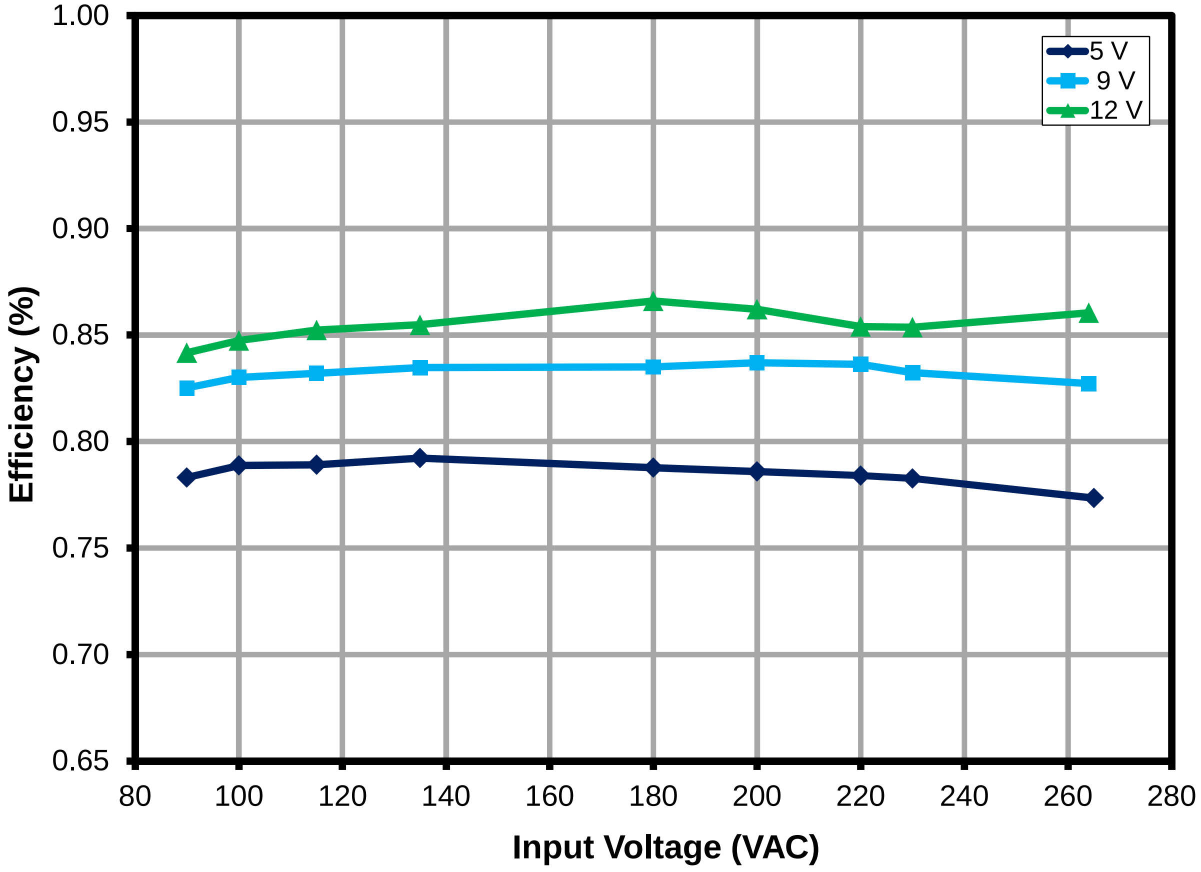


Figure 15 – Efficiency vs. Input Voltage, Room Temperature.

11.2 Active Mode Efficiency

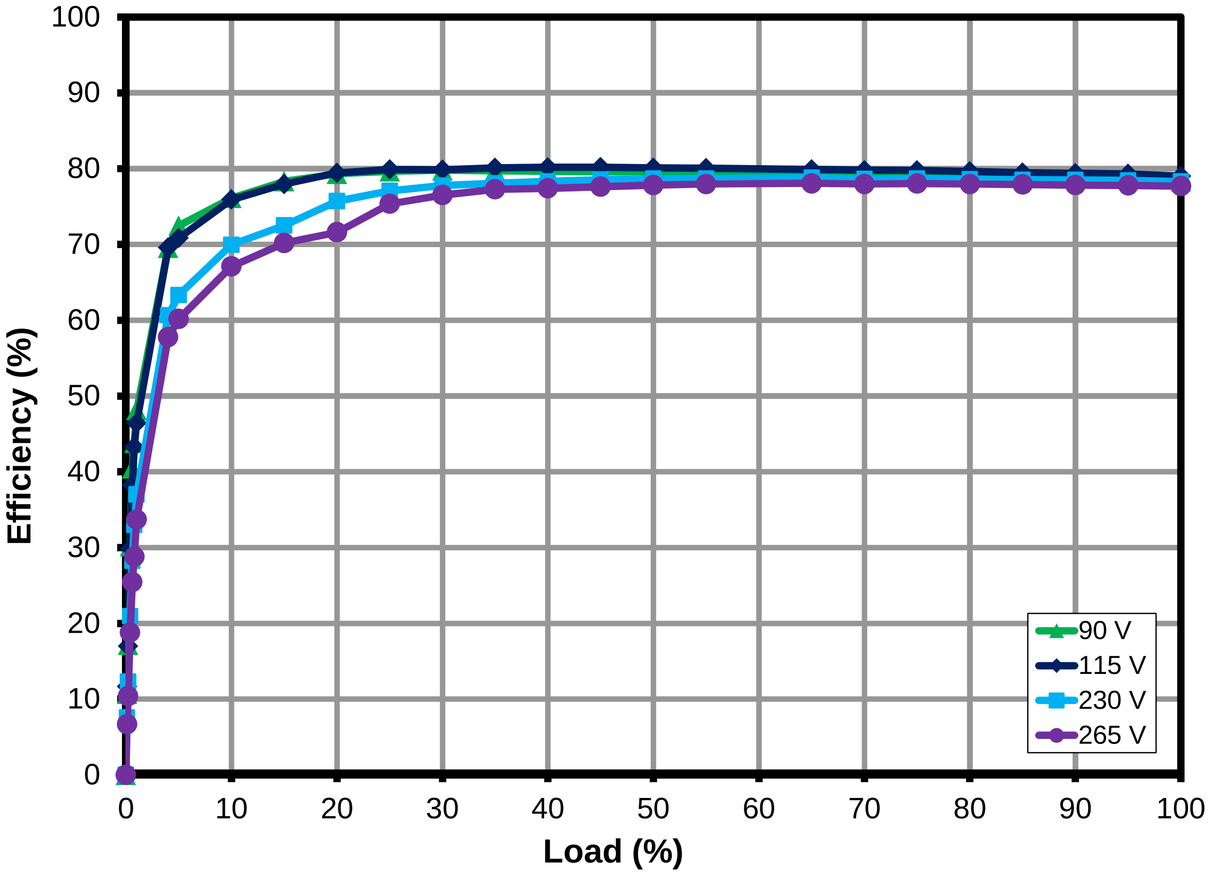


Figure 16 – Efficiency vs. Load 5 V.

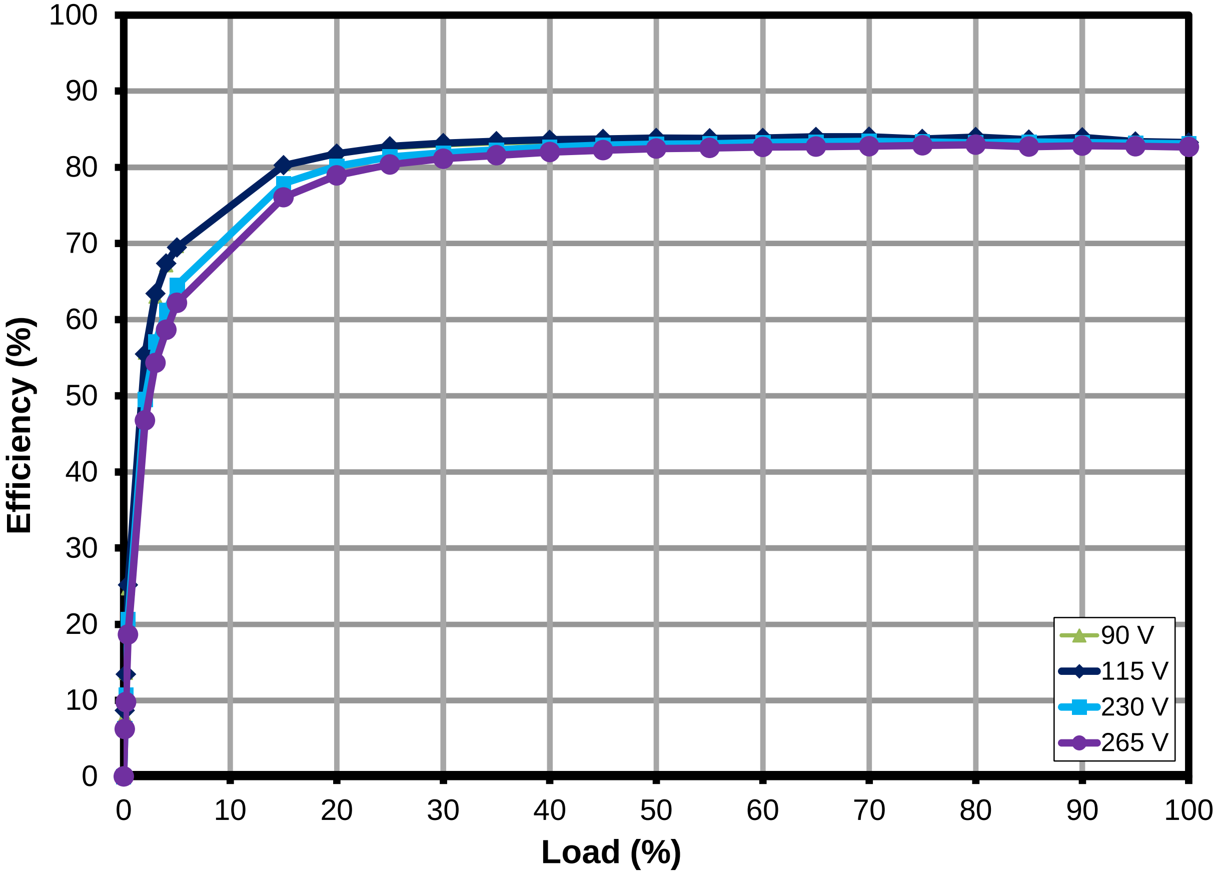


Figure 17 – Efficienc vs. Load 9 V.

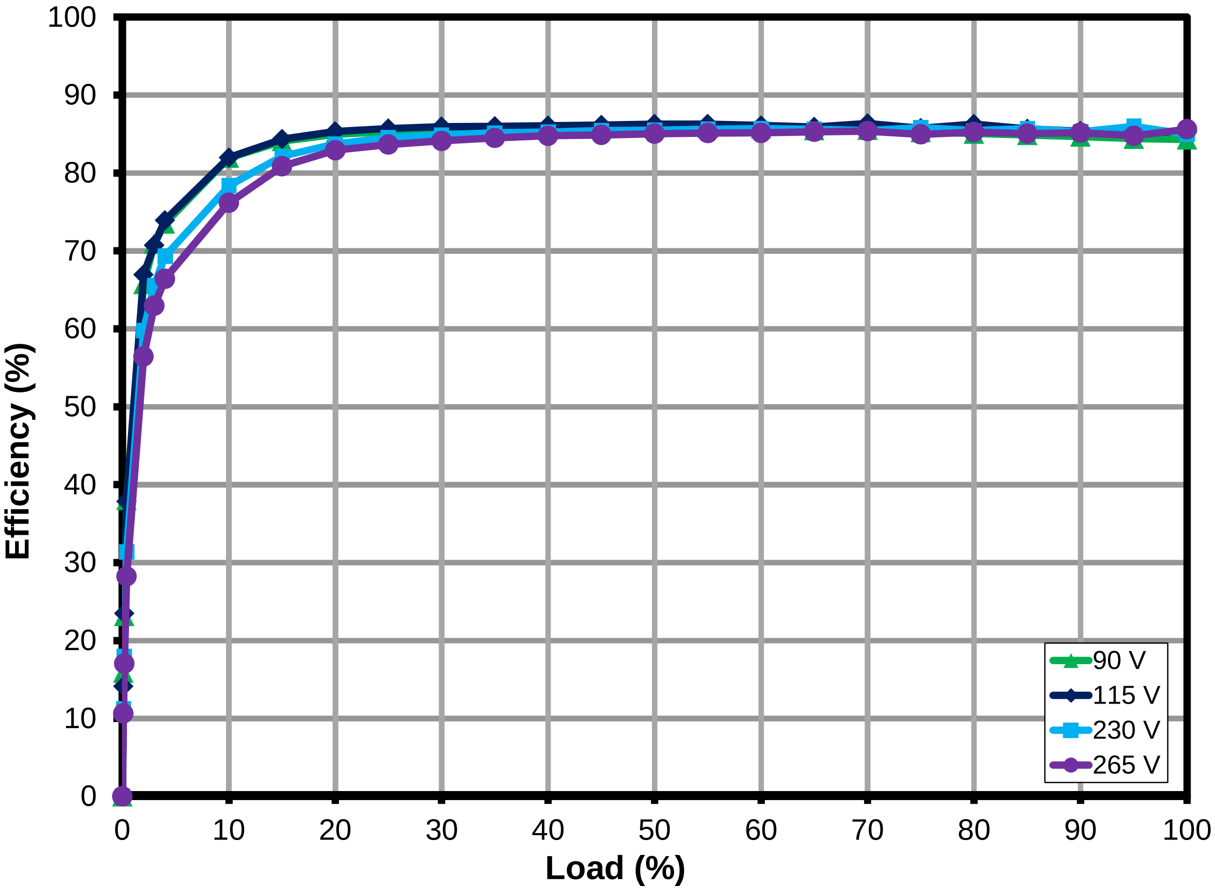


Figure 18 – Efficiency vs. Load 12 V.

Percent of Full Load	12 V Efficiency (%)	
(%)	115 VAC	230 VAC
100	85.21	84.96
90	85.39	85.28
80	86.30	85.44
75	85.75	85.85
70	86.37	85.43
60	86.09	85.73
50	86.27	85.49
40	86.05	85.27
30	85.95	84.90
25	85.73	84.54
20	85.31	83.76
10	82.00	78.38
Average	**85.7**	**85.2**
US EISA (2007) Requirement	***79***	
ENERGY STAR EPS v2, EC CoC v4, EUP Tier 2	***82***	

11.3 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

11.3.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln (P_O) + 0.5$
> 51 W	0.85

Ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

11.3.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln (P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq$ 550 mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln (P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

11.4 No-Load Input Power

Test results shows that the toggle board affects the no load input power, and thus on no load data for 5 V without toggle board is shown in this report.

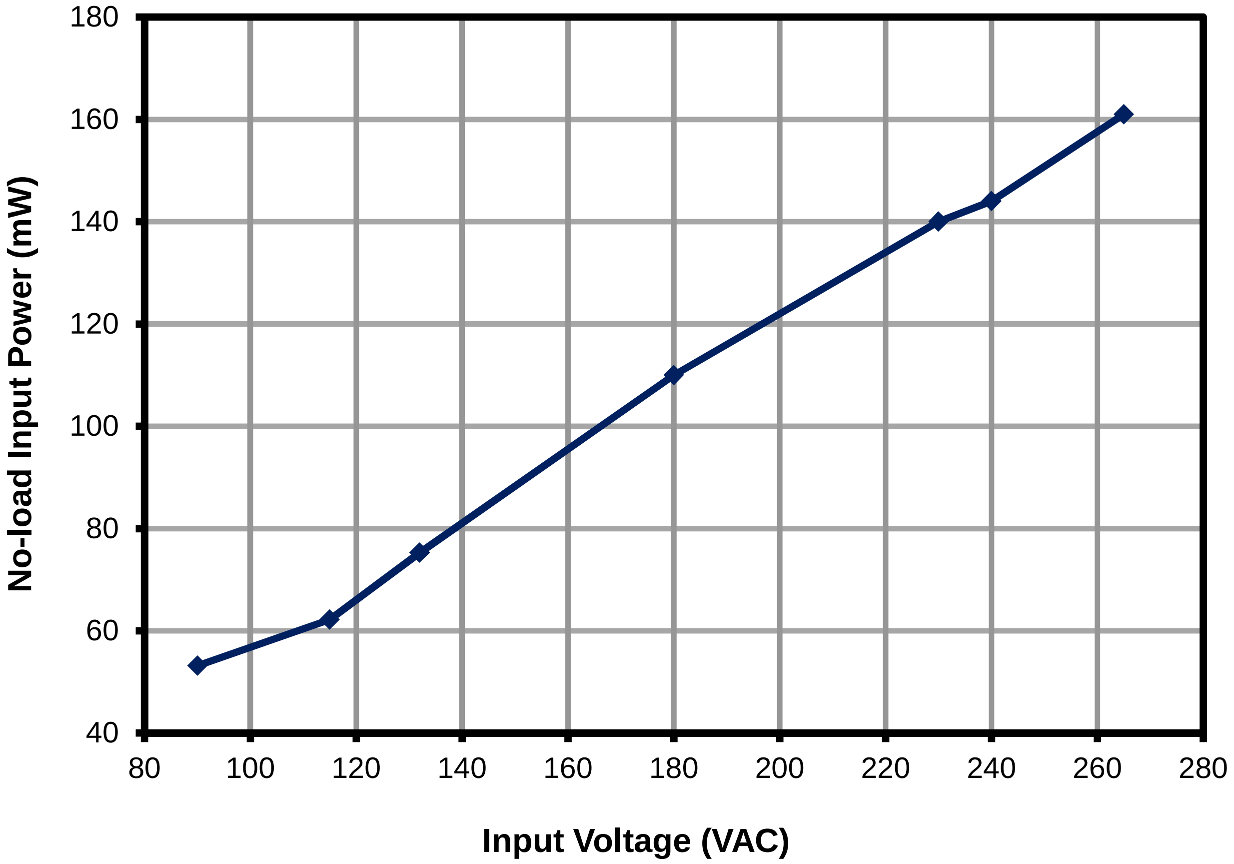


Figure 19 – No-Load Input Power at 5 V and Without Toggle Board.

11.5 CV/CC

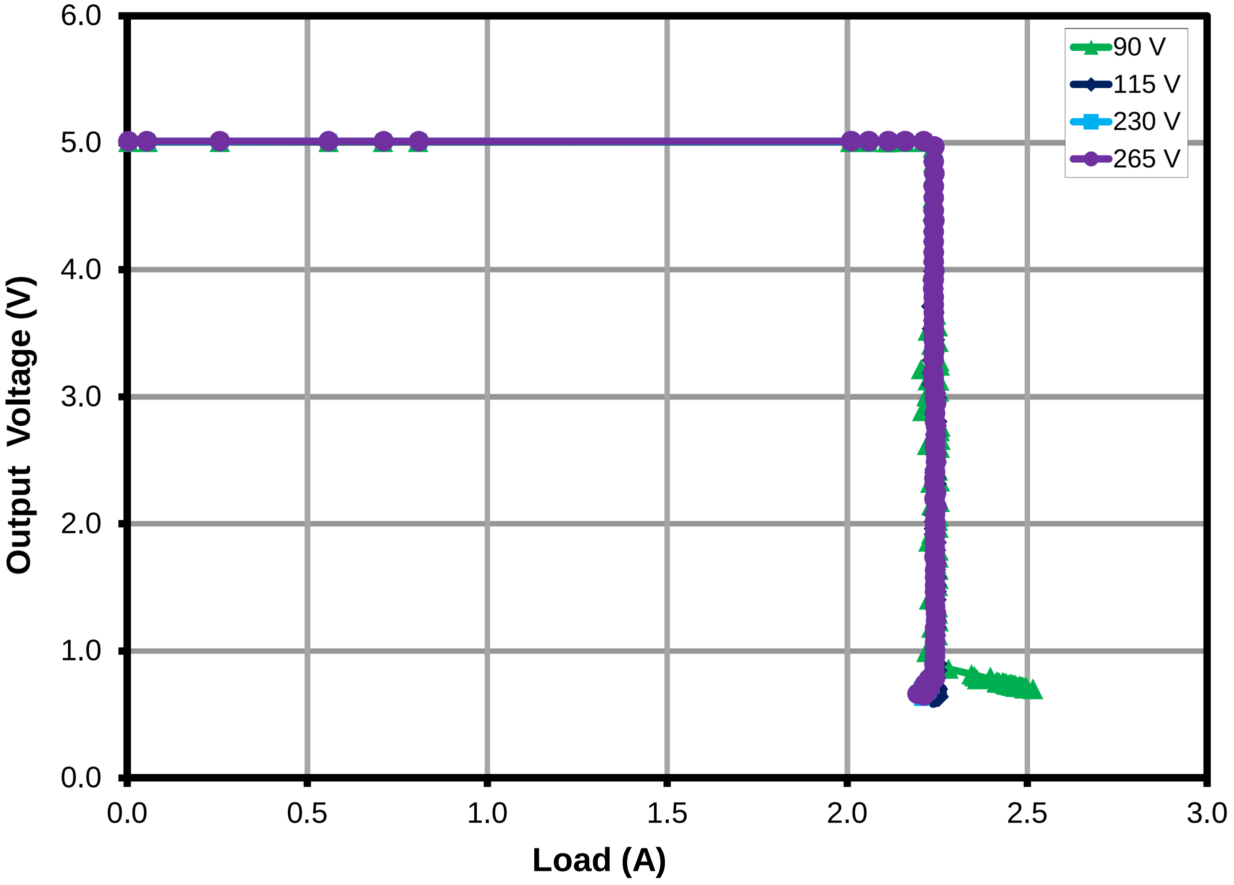


Figure 20 – 5 V CV/CC, Room Temperature.

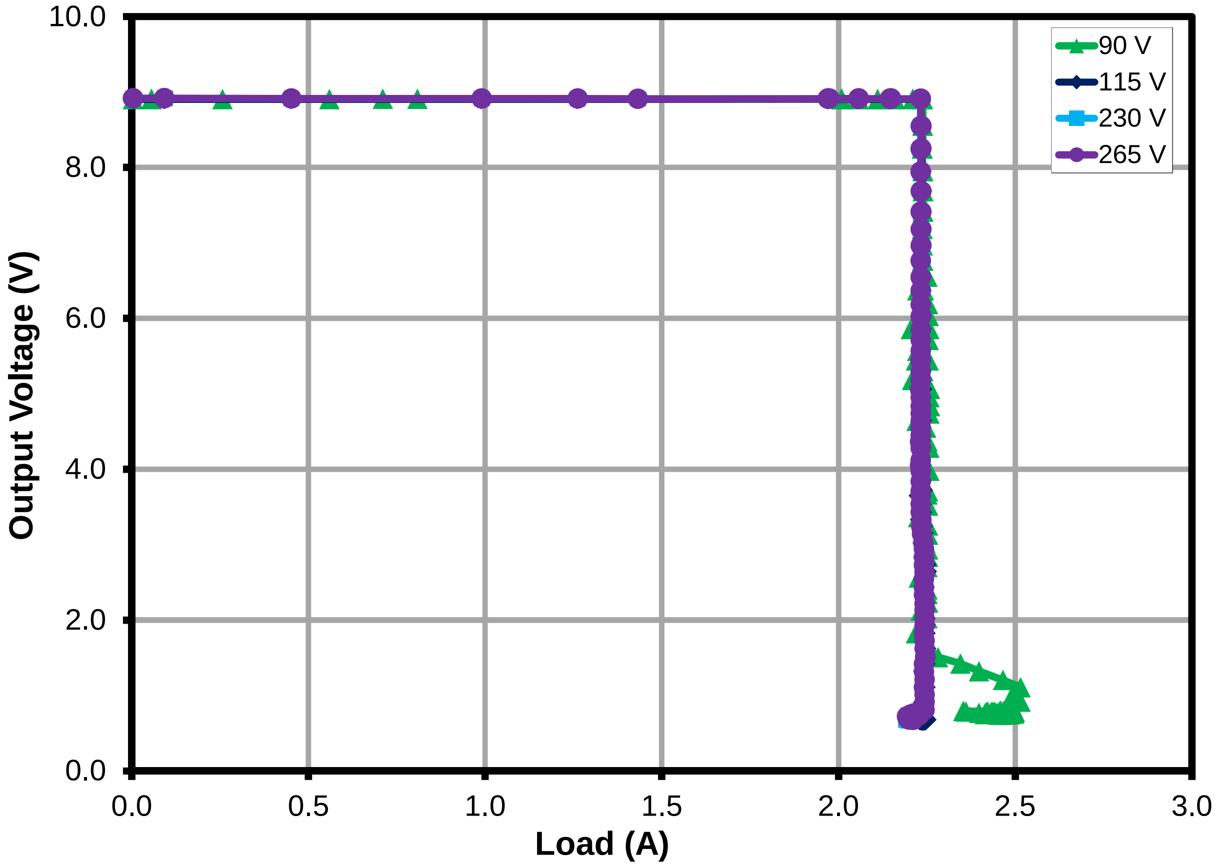


Figure 21 – 9 V CV/CC, Room Temperature.

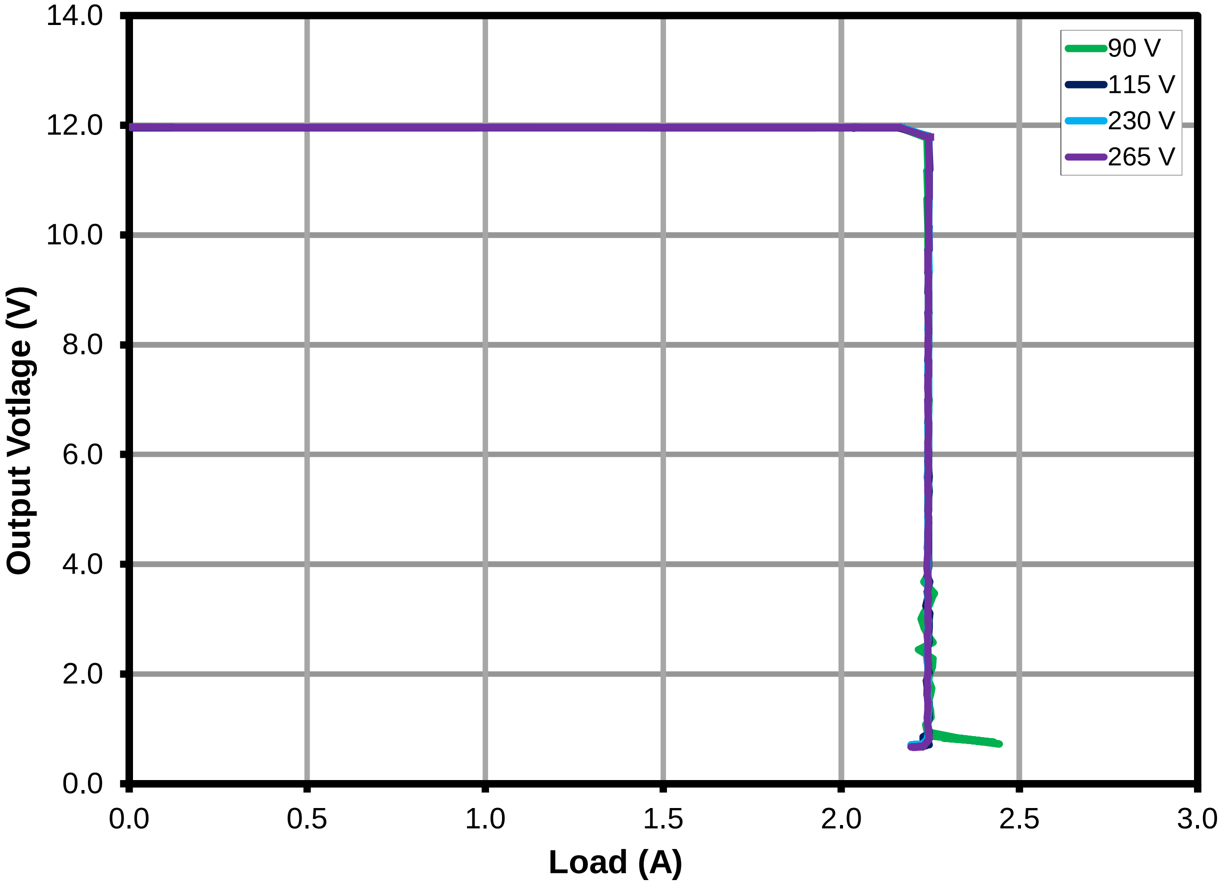


Figure 22 – 12 V CV/CC, Room Temperature.

12 Thermal Performance

At room ambient, thermal performance was tested with12 V, 2 A load and 12 V, 1.5 A load.

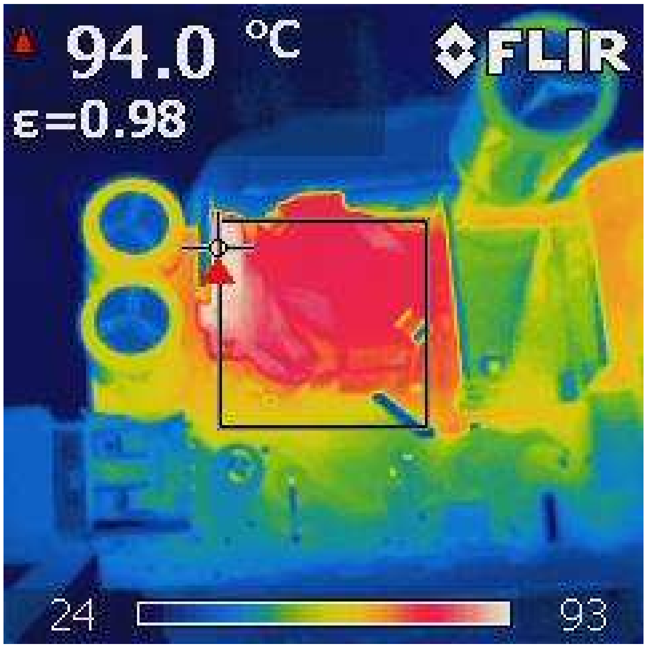


Figure 23 – Thermal at 90 VAC 12 V, 2 A.

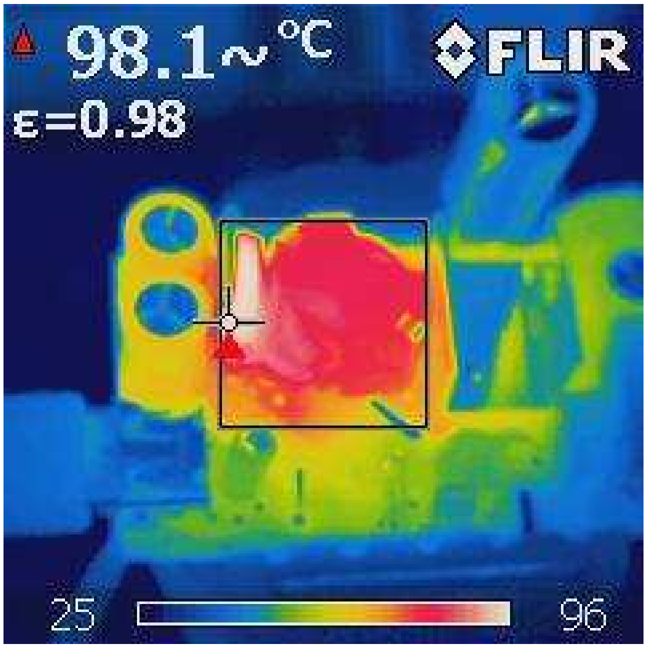


Figure 24 – Thermal at 265 VAC, 2 A.

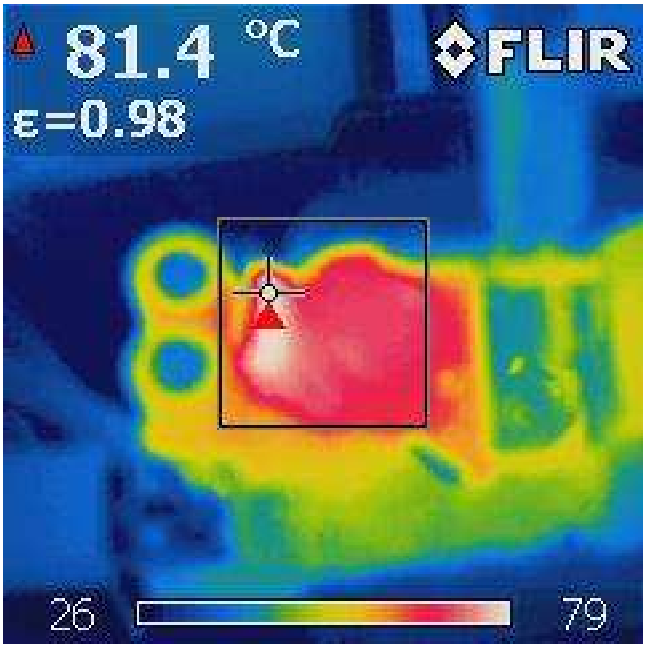


Figure 25 – Thermal at 90 VAC 12 V, 1.5 A.

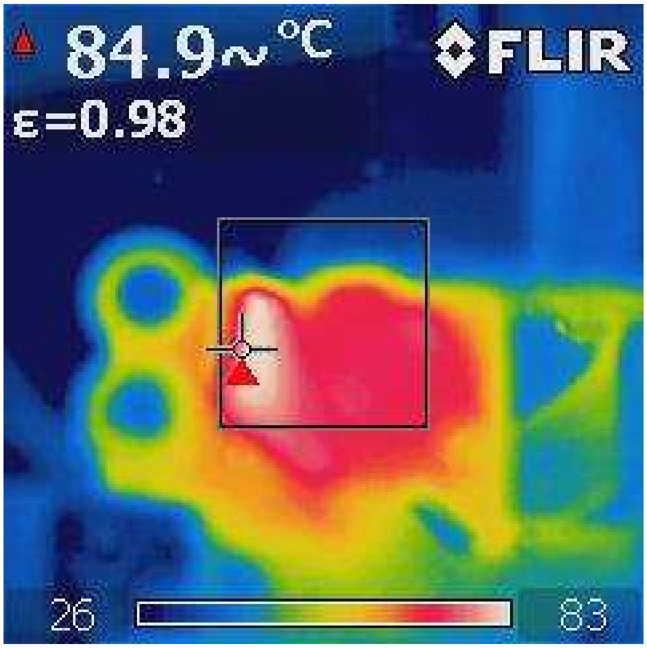
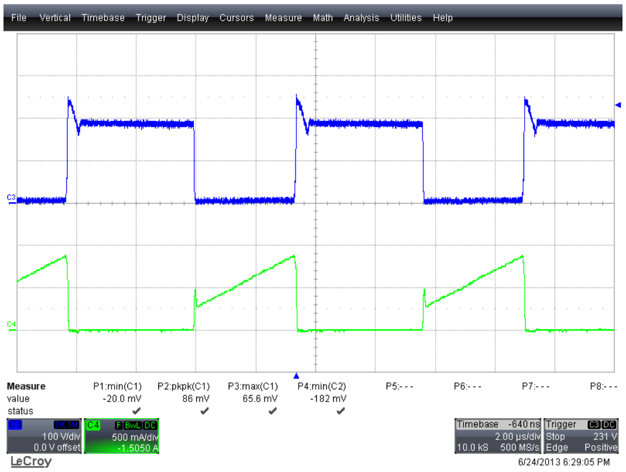


Figure 26 – Thermal at 265 VAC, 1.5 A.

13 Waveforms

13.1 Drain Voltage and Current, Normal Operation



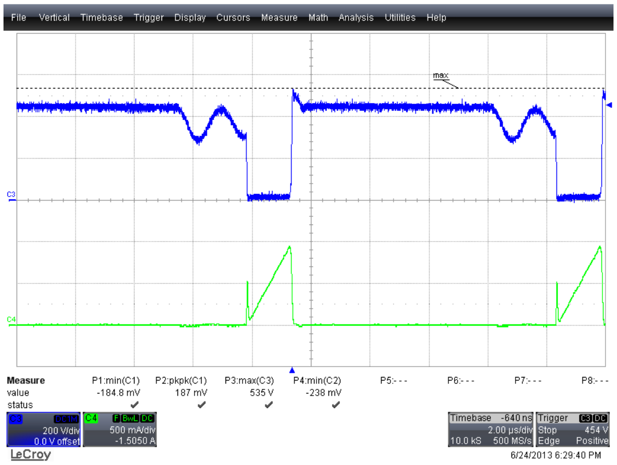
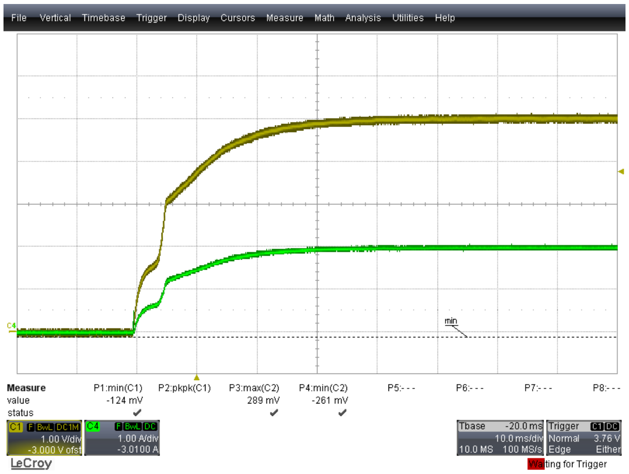


Figure 27 – 90 VAC, 12 V, 2 A.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 µs / div.

Figure 28 – 265 VAC, 12 V, 2 A.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 µs / div.

13.2 Output Voltage Start-up Profile

13.2.1 5 V, 2 A CR Load Start-up



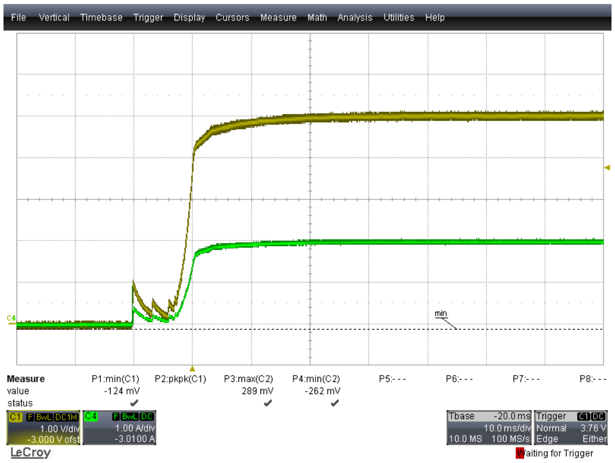
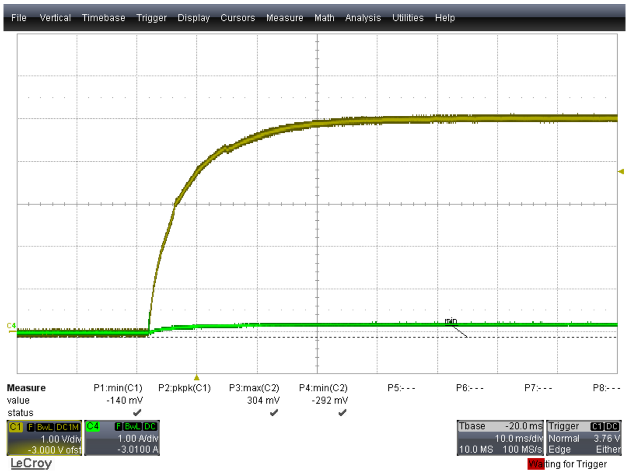


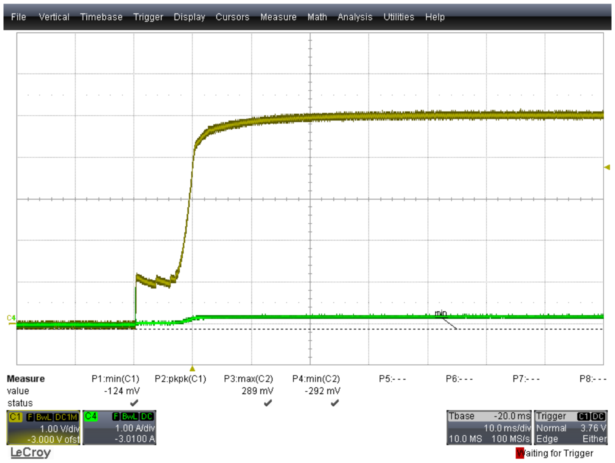
Figure 29 – Start-up Profile, 90 VAC.
5 V, 2 A CR Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 0.5 A, 5 ms / div.

Figure 30 – Start-up Profile, 265 VAC.
5 V, 2 A CR Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 0.5 A, 5 ms / div.

13.2.2 5 V, 0.2 A CR Load Start-up



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-140 mV		304 mV	-292 mV				
status	✓		✓	✓				



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-124 mV		289 mV	-292 mV				
status	✓		✓	✓				

Figure 31 – Start-up Profile, 90 VAC.
5 V, 0.2 A CR Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 0.5 A, 5 ms / div.

Figure 32 – Start-up Profile, 265 VAC.
5 V, 0.2 A CR Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 0.5 A, 5 ms / div.

13.3 Drain Voltage and Current Start-up Profile

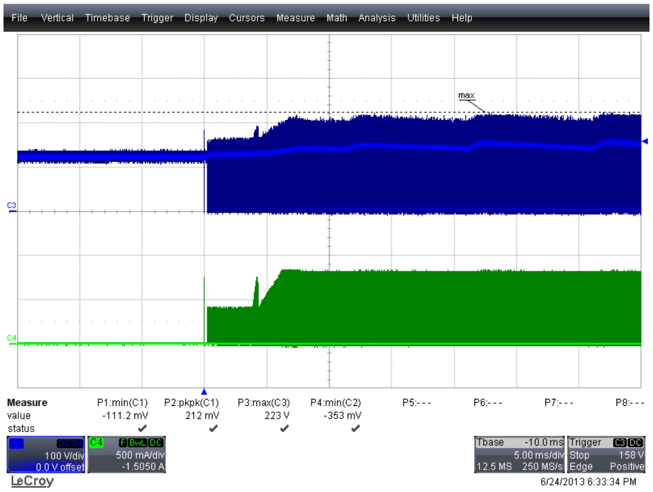


Figure 33 – 90 VAC, 5 V, 2 A.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A, 5 ms / div.

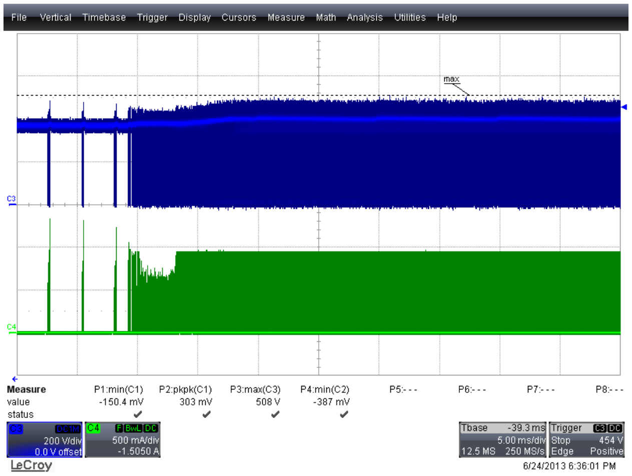


Figure 34 – 265 VAC, 5 V, 2 A.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 5 ms / div.

13.4 Output Diode Peak Inverse Voltage

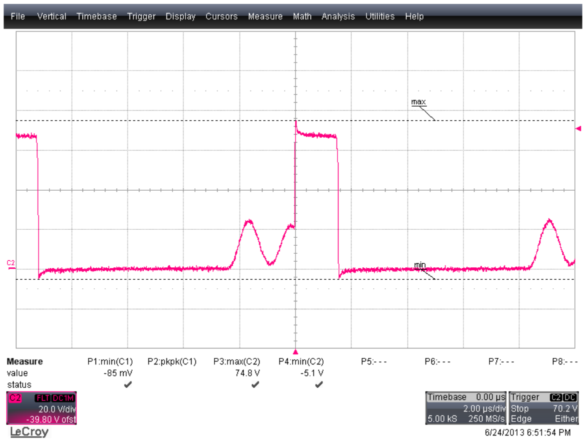
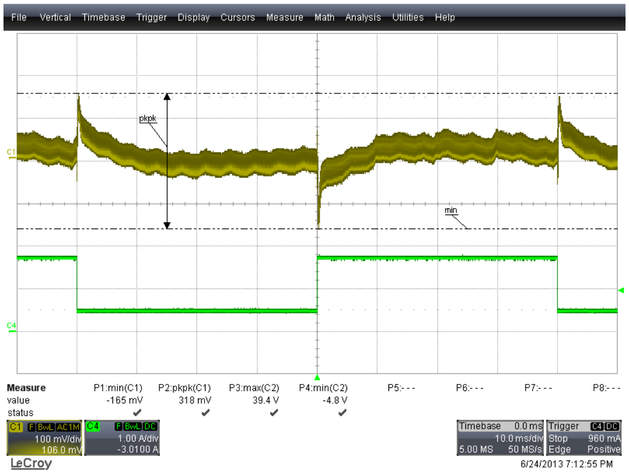


Figure 35 – 265 VAC, 12 V Output, 2 A Load.
V_{DIODE}, 20 V, 2 µs / div.

13.5 Load Transient Response

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response. Note the DC shifts are due to the output cable resistance.

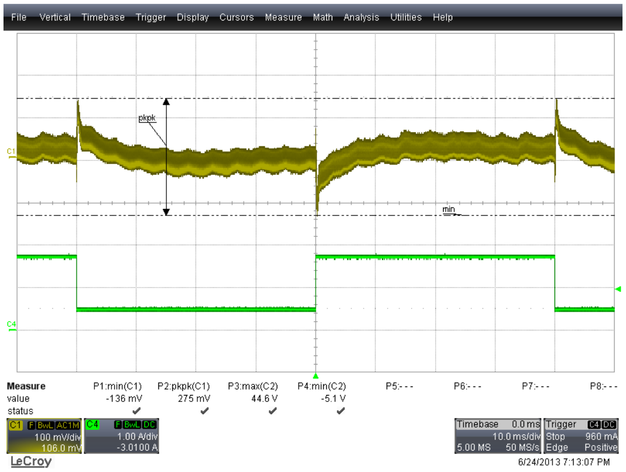
13.5.1 12 V Output; 0.5 A - 1.75 A - 0.5 A Load Step



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-165 mV	318 mV	39.4 V	-4.8 V				
status	✓	✓	✓	✓				

C1 F BwL AC1M 100 mV/div 106.0 mV
C4 F BwL DC 1.00 A/div -3.0100 A
Timebase 0.0 ms 10.0 ms/div 5.00 MS 50 MS/s
Trigger C4 DC Stop 960 mA Edge Positive
6/24/2013 7:12:55 PM

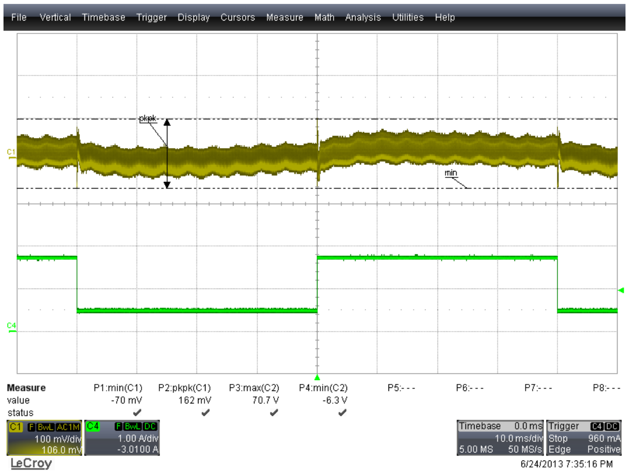
Figure 36 – Transient Response, 90 VAC,
318 mV_{PK-PK}.
Upper: V_{RIPPLE}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-136 mV	275 mV	44.6 V	-5.1 V				
status	✓	✓	✓	✓				

C1 F BwL AC1M 100 mV/div 106.0 mV
C4 F BwL DC 1.00 A/div -3.0100 A
Timebase 0.0 ms 10.0 ms/div 5.00 MS 50 MS/s
Trigger C4 DC Stop 960 mA Edge Positive
6/24/2013 7:13:07 PM

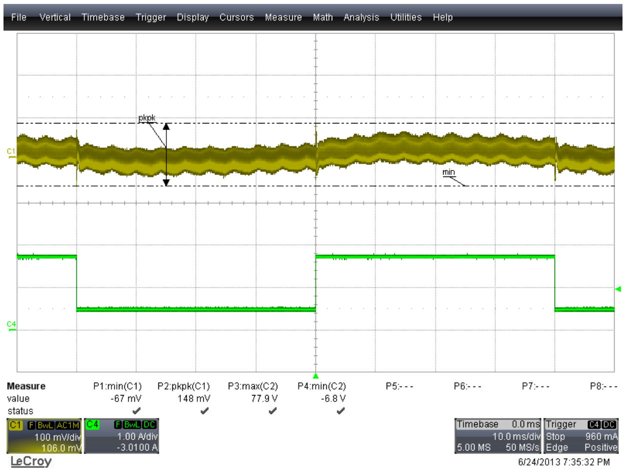
Figure 37 – Transient Response, 115 VAC,
275 mV_{PK-PK}.
Upper: V_{RIPPLE}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-70 mV	162 mV	70.7 V	-6.3 V				
status	✓	✓	✓	✓				

C1 F BwL AC1M 100 mV/div 106.0 mV
C4 F BwL DC 1.00 A/div -3.0100 A
Timebase 0.0 ms 10.0 ms/div 5.00 MS 50 MS/s
Trigger C4 DC Stop 960 mA Edge Positive
6/24/2013 7:35:16 PM

Figure 38 – Transient Response, 230 VAC,
160 mV_{PK-PK}.
Upper: V_{OUT}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 5 ms / div.

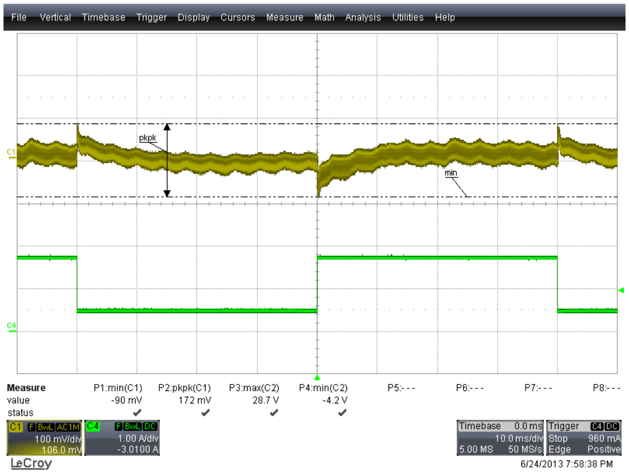


Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-67 mV	148 mV	77.9 V	-6.8 V				
status	✓	✓	✓	✓				

C1 F BwL AC1M 100 mV/div 106.0 mV
C4 F BwL DC 1.00 A/div -3.0100 A
Timebase 0.0 ms 10.0 ms/div 5.00 MS 50 MS/s
Trigger C4 DC Stop 960 mA Edge Positive
6/24/2013 7:35:32 PM

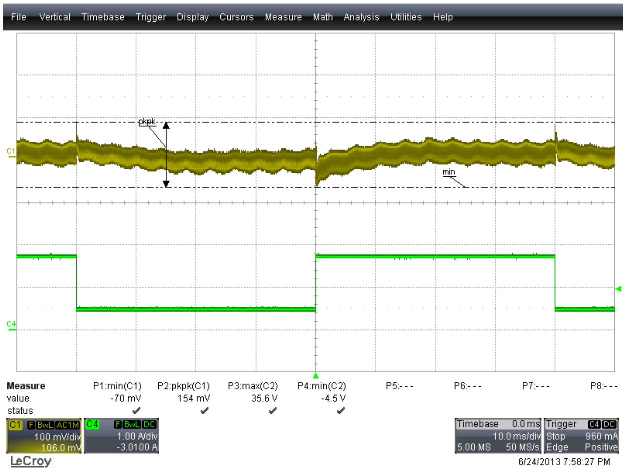
Figure 39 – Transient Response, 265 VAC,
148 mV_{PK-PK}.
Upper: V_{OUT}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 5 ms / div.

13.5.2 5 V Output; 0.5 A - 1.75 A - 0.5 A Load Step



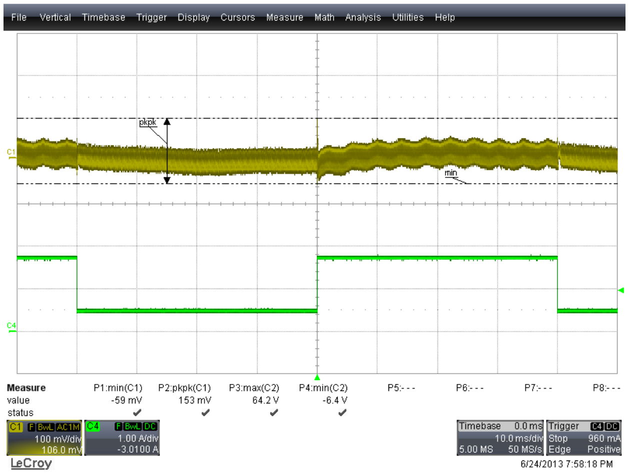
```
Measure  P1:min(C1)  P2:pkpk(C1)  P3:max(C2)  P4:min(C2)  P5:- - -  P6:- - -  P7:- - -  P8:- - -
value        -90 mV       172 mV      28.7 V      -4.2 V
status          ✓            ✓           ✓           ✓
C1 F BwL AC1M   C4 F BwL DC                        Timebase   0.0 ms   Trigger   C4 DC
  100 mV/div     1.00 A/div                                 10.0 ms/div Stop     960 mA
  106.0 mV      -3.0100 A                          5.00 MS   50 MS/s   Edge    Positive
                                                              6/24/2013 7:58:38 PM
```

Figure 40 – Transient Response, 90 VAC,
172 mV_{PK-PK}.
Upper: V_{RIPPLE}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 10 ms / div.



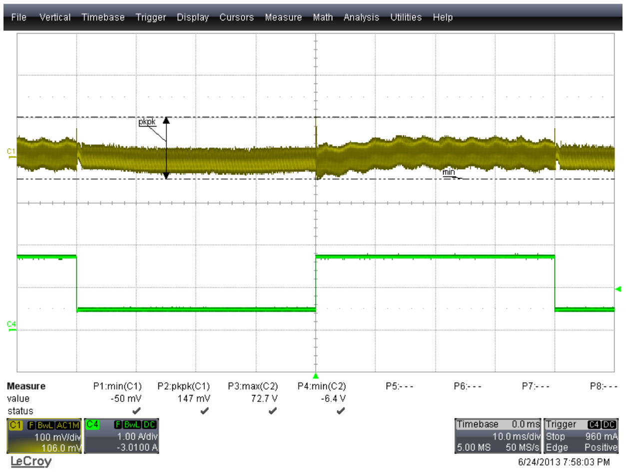
```
Measure  P1:min(C1)  P2:pkpk(C1)  P3:max(C2)  P4:min(C2)  P5:- - -  P6:- - -  P7:- - -  P8:- - -
value        -70 mV       154 mV      35.6 V      -4.5 V
status          ✓            ✓           ✓           ✓
C1 F BwL AC1M   C4 F BwL DC                        Timebase   0.0 ms   Trigger   C4 DC
  100 mV/div     1.00 A/div                                 10.0 ms/div Stop     960 mA
  106.0 mV      -3.0100 A                          5.00 MS   50 MS/s   Edge    Positive
                                                              6/24/2013 7:58:27 PM
```

Figure 41 – Transient Response, 115 VAC,
154 mV_{PK-PK}.
Upper: V_{RIPPLE}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 10 ms / div.



```
Measure  P1:min(C1)  P2:pkpk(C1)  P3:max(C2)  P4:min(C2)  P5:- - -  P6:- - -  P7:- - -  P8:- - -
value        -59 mV       153 mV      64.2 V      -6.4 V
status          ✓            ✓           ✓           ✓
C1 F BwL AC1M   C4 F BwL DC                        Timebase   0.0 ms   Trigger   C4 DC
  100 mV/div     1.00 A/div                                 10.0 ms/div Stop     960 mA
  106.0 mV      -3.0100 A                          5.00 MS   50 MS/s   Edge    Positive
                                                              6/24/2013 7:58:18 PM
```

Figure 42 – Transient Response, 230 VAC,
153 mV_{PK-PK}.
Upper: V_{OUT},100 mV / div.
Lower: I_{LOAD}, 1 A, 10 ms / div.



```
Measure  P1:min(C1)  P2:pkpk(C1)  P3:max(C2)  P4:min(C2)  P5:- - -  P6:- - -  P7:- - -  P8:- - -
value        -50 mV       147 mV      72.7 V      -6.4 V
status          ✓            ✓           ✓           ✓
C1 F BwL AC1M   C4 F BwL DC                        Timebase   0.0 ms   Trigger   C4 DC
  100 mV/div     1.00 A/div                                 10.0 ms/div Stop     960 mA
  106.0 mV      -3.0100 A                          5.00 MS   50 MS/s   Edge    Positive
                                                              6/24/2013 7:58:03 PM
```

Figure 43 – Transient Response, 265 VAC,
147 mV_{PK-PK}.
Upper: V_{OUT}, 100 mV / div.
Lower: I_{LOAD}, 1 A, 5 ms / div.

13.6 Output Ripple Measurements

13.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 10.0 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

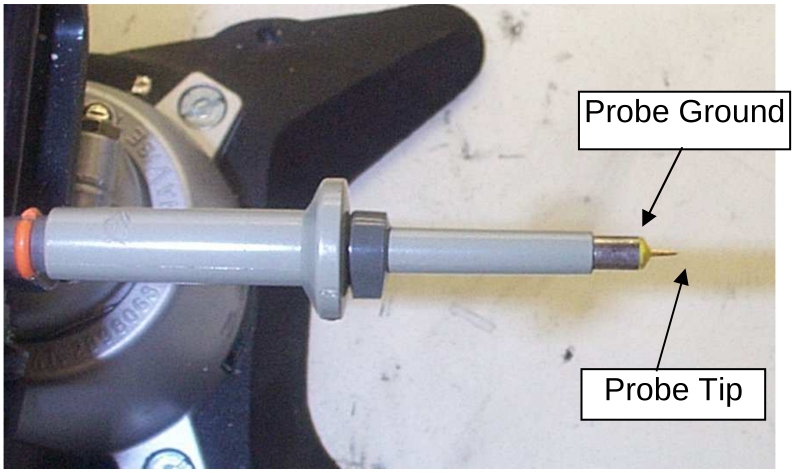


Figure 44 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

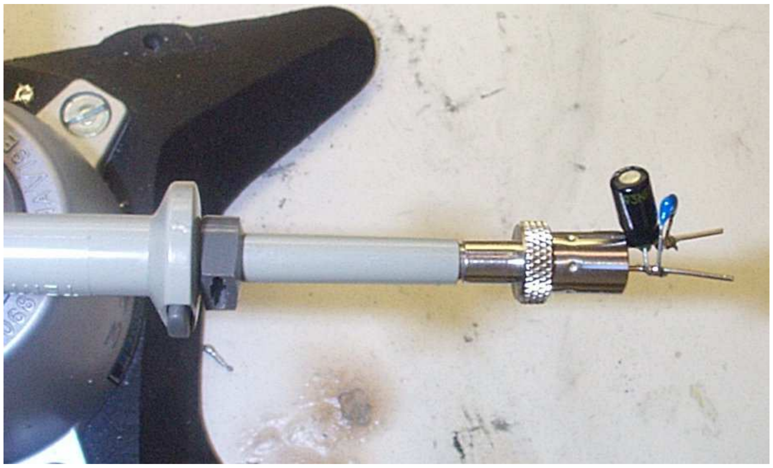


Figure 45 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.6.2 Measurement Results at PCB

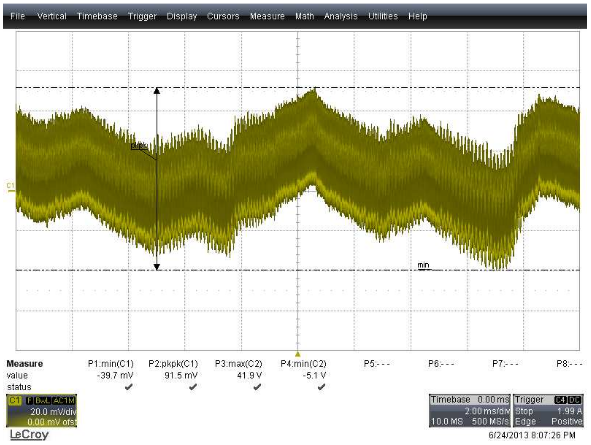


Figure 46 – Ripple, 90 VAC, 12 V, 2 A.
91.5 mV$_{PK-PK}$.
2 ms, 20 mV / div.

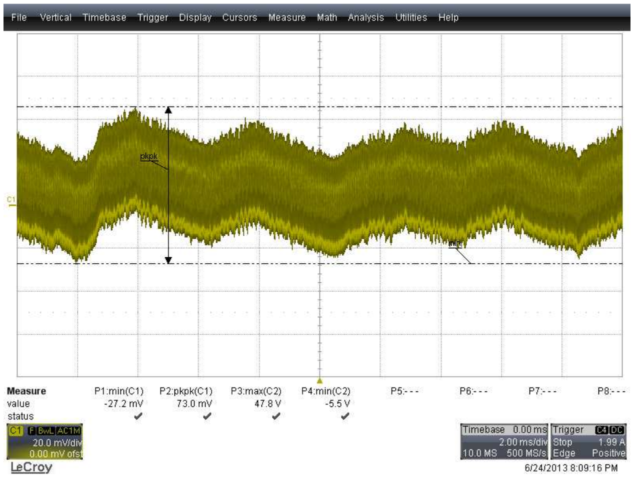


Figure 47 – Ripple, 115 VAC, 12 V, 2 A.
73 mV$_{PK-PK}$.
2 ms, 20 mV / div.

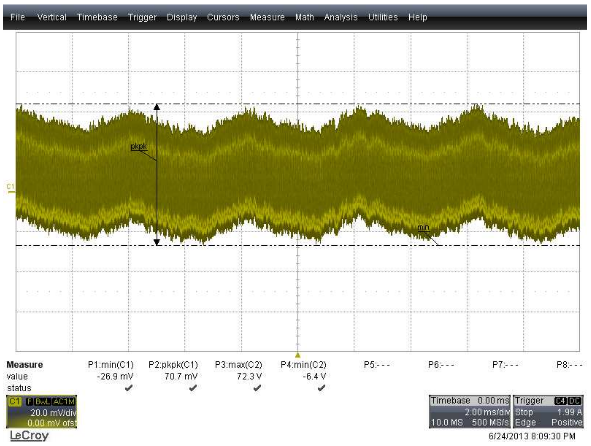


Figure 48 – Ripple, 230 VAC, 12 V, 2 A.
71 mV$_{PK-PK}$.
2 ms, 20 mV / div.

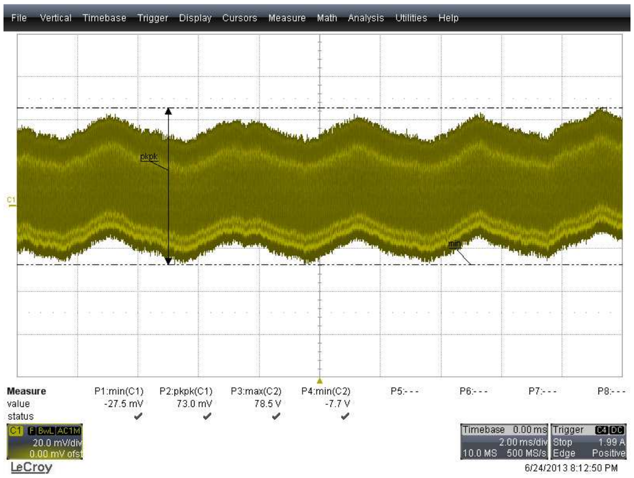
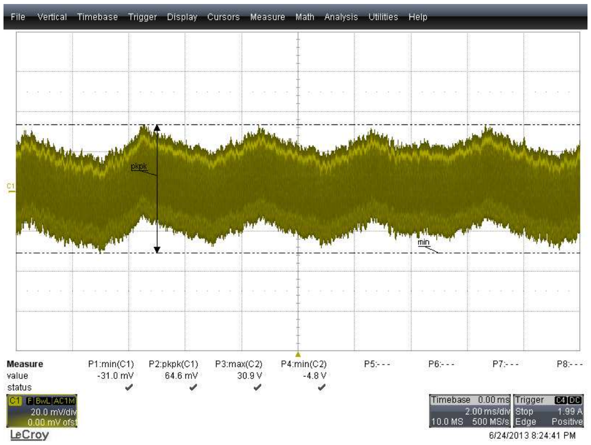
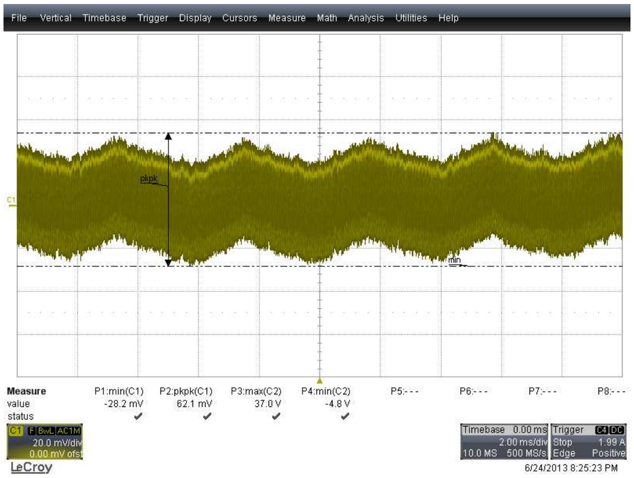


Figure 49 – Ripple, 265 VAC, 12 V, 2 A.
73 mV$_{PK-PK}$.
2 ms, 20 mV / div.



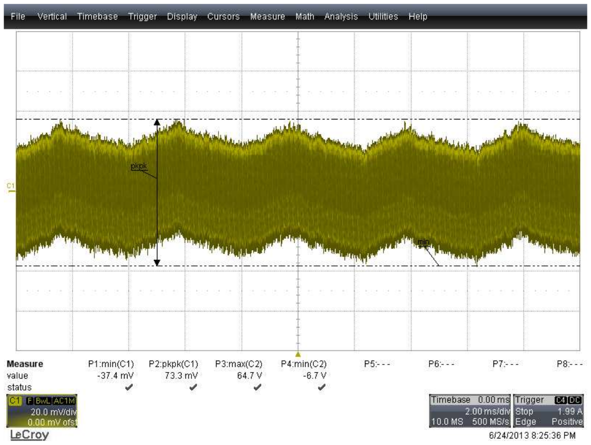
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-31.0 mV	64.6 mV	30.9 V	-4.8 V				
status	✓	✓	✓	✓				

Figure 50 – Ripple, 90 VAC, 5 V, 2 A.
65 mV$_{PK-PK}$.
2 ms, 20 mV / div.



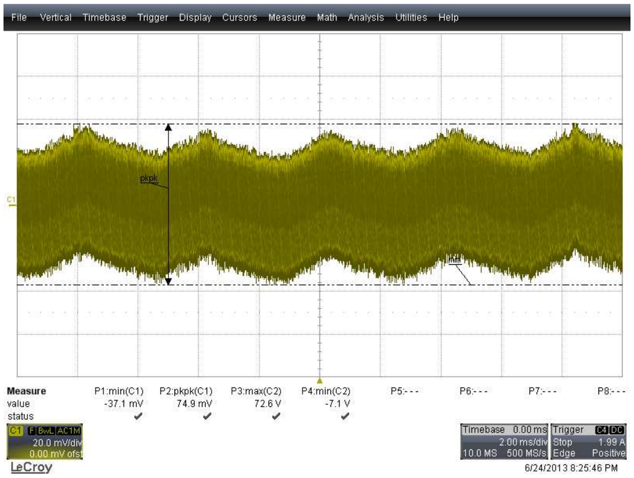
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-28.2 mV	62.1 mV	37.0 V	-4.8 V				
status	✓	✓	✓	✓				

Figure 51 – Ripple, 115 VAC, 5 V, 2 A.
62.5 mV$_{PK-PK}$.
2 ms, 50 mV / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-37.4 mV	73.3 mV	64.7 V	-6.7 V				
status	✓	✓	✓	✓				

Figure 52 – Ripple, 230 VAC, 5 V, 2 A.
73 mV$_{PK-PK}$.
2 ms, 50 mV / div.

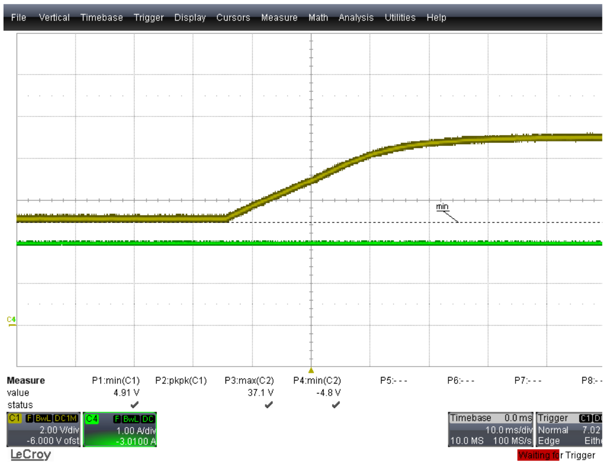


Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	-37.1 mV	74.9 mV	72.6 V	-7.1 V				
status	✓	✓	✓	✓				

Figure 53 – Ripple, 265 VAC, 5 V, 2 A.
97 mV$_{PK-PK}$.
2 ms, 50 mV / div.

13.7 Output Voltage Toggle

13.7.1 Output Toggle Up at Full Load 2 A



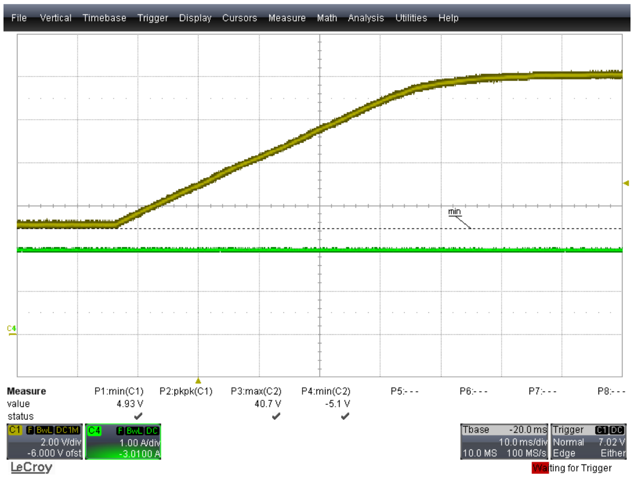
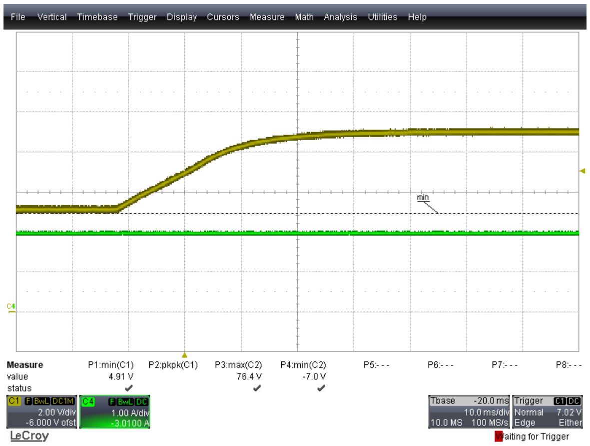


Figure 54 – V$_{OUT}$ from 5 V to 9 V, 90 VAC 2 A.
Upper: V$_{OUT}$, 2 V / div.
Lower: I$_{OUT}$, 1 A, 10 ms / div.

Figure 55 – V$_{OUT}$ from 5 V to 12 V, 90 VAC 2 A.
Upper: V$_{OUT}$, 2 V / div.
Lower: I$_{OUT}$, 1 A, 10 ms / div.



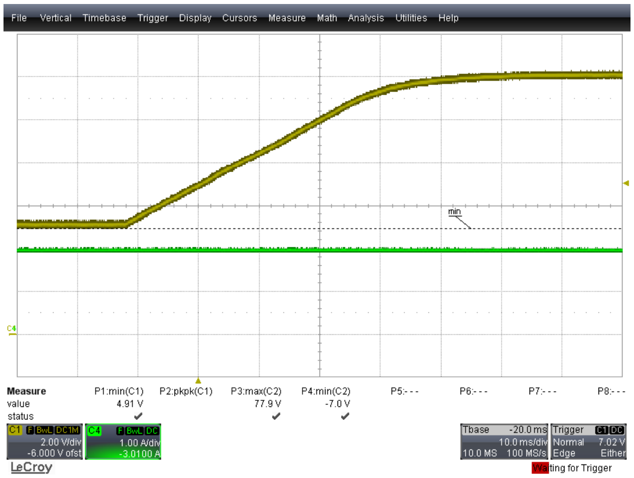


Figure 56 – V$_{OUT}$ from 5 V to 9 V, 265 VAC 2 A.
Upper: V$_{OUT}$, 2 V / div.
Lower: I$_{OUT}$, 1 A, 10 ms / div.

Figure 57 – V$_{OUT}$ from 5 V to 12 V, 265 VAC 2 A.
Upper: V$_{OUT}$, 2 V / div.
Lower: I$_{OUT}$, 1 A, 10 ms / div.

13.7.2 Output Toggle Up at Half Load 1 A

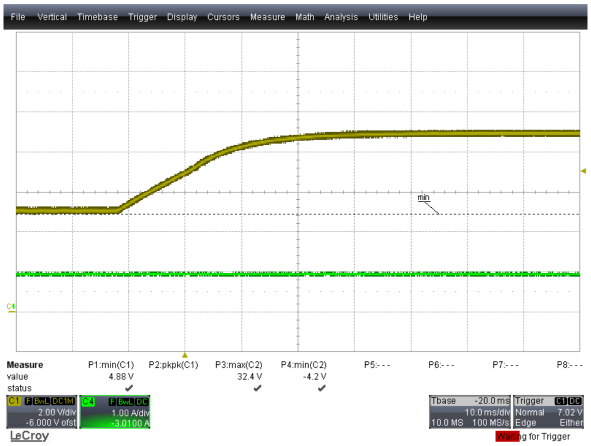


Figure 58 – V_{OUT} from 5 V to 9 V, 90 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

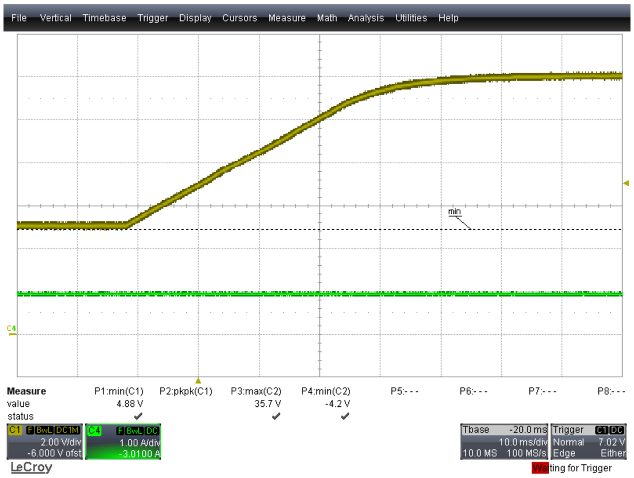


Figure 59 – V_{OUT} from 5 V to 12 V, 90 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

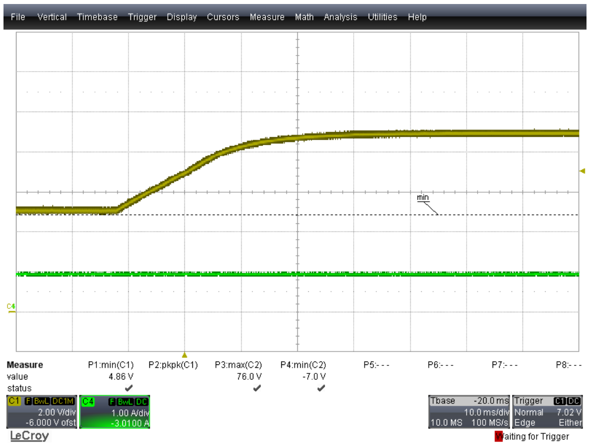


Figure 60 – V_{OUT} from 5 V to 9 V, 265 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

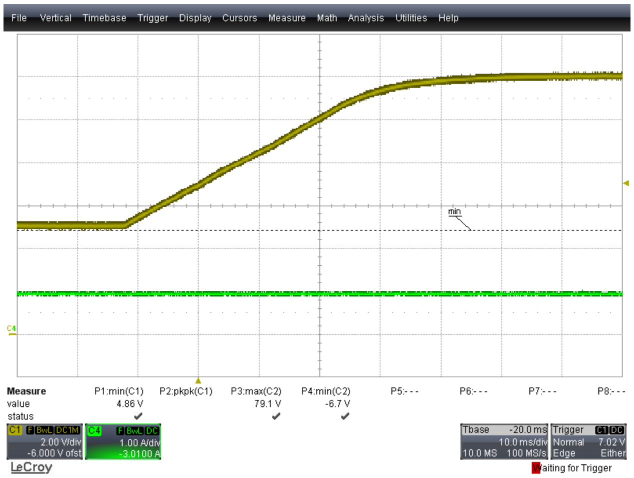
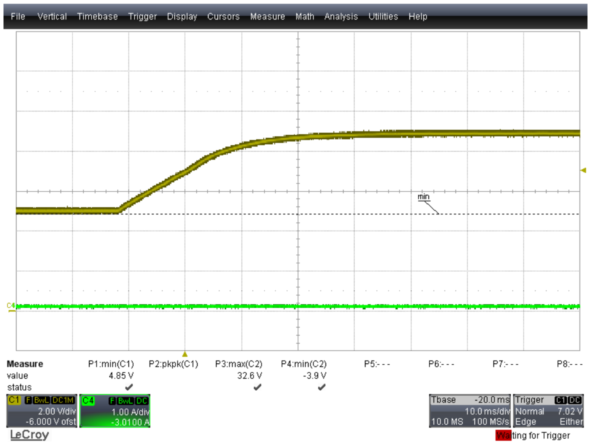


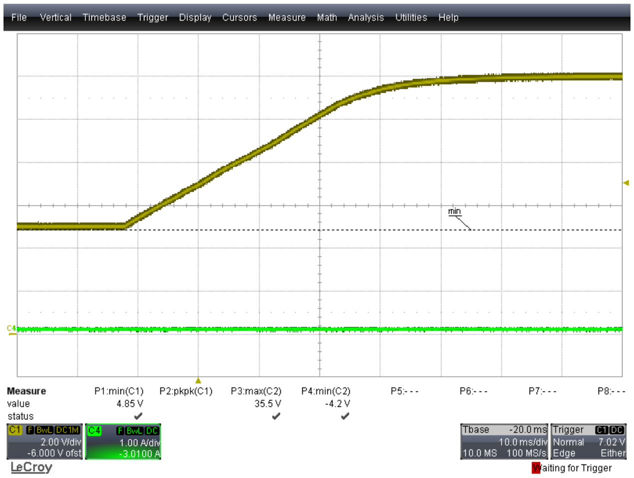
Figure 61 – V_{OUT} from 5 V to 12 V, 265 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

13.7.3 Output Toggle Up at Light Load 0.15 A



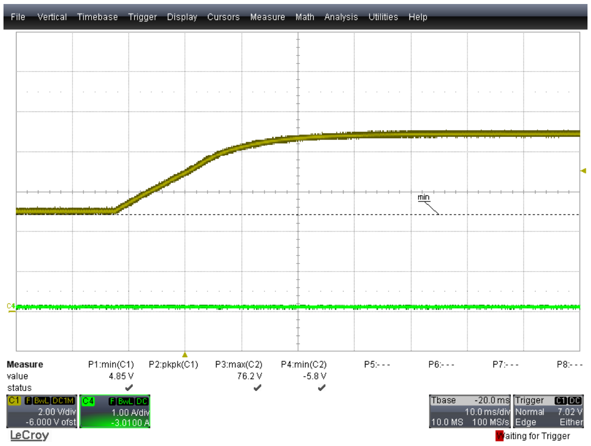
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		32.6 V	-3.9 V				
status	✓		✓	✓				

Figure 62 – V_{OUT} from 5 V to 9 V, 90 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



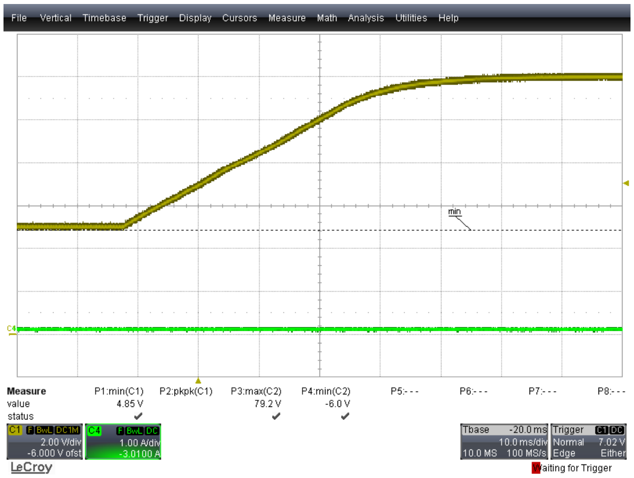
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		35.5 V	-4.2 V				
status	✓		✓	✓				

Figure 63 – V_{OUT} from 5 V to 12 V, 90 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		76.2 V	-5.8 V				
status	✓		✓	✓				

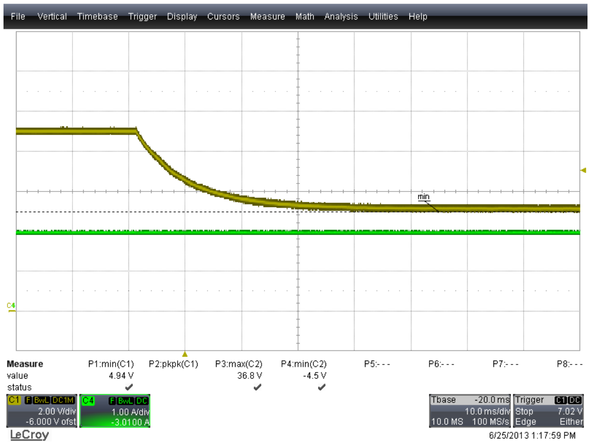
Figure 64 – V_{OUT} from 5 V to 9 V, 265 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		79.2 V	-6.0 V				
status	✓		✓	✓				

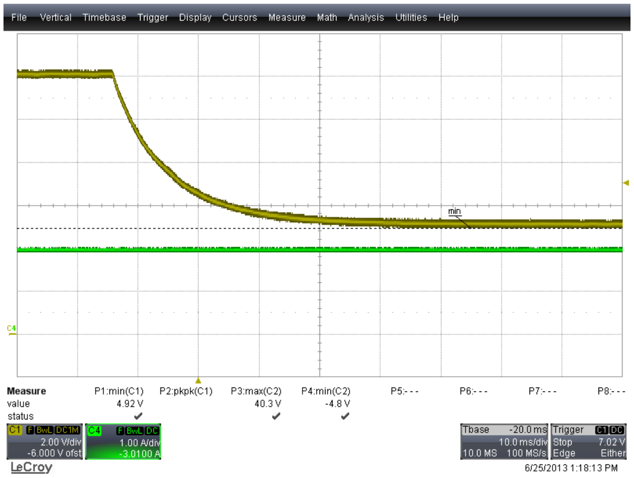
Figure 65 – V_{OUT} from 5 V to 12 V, 265 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

13.7.4 Voltage Toggle Down at Full Load 2 A



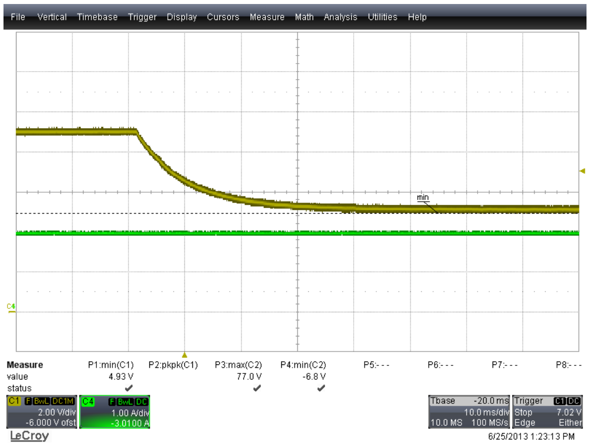
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.94 V		36.8 V	-4.5 V				
status	✓		✓	✓				

Figure 66 – V_{OUT} from 9 V to 5 V, 90 VAC 2 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



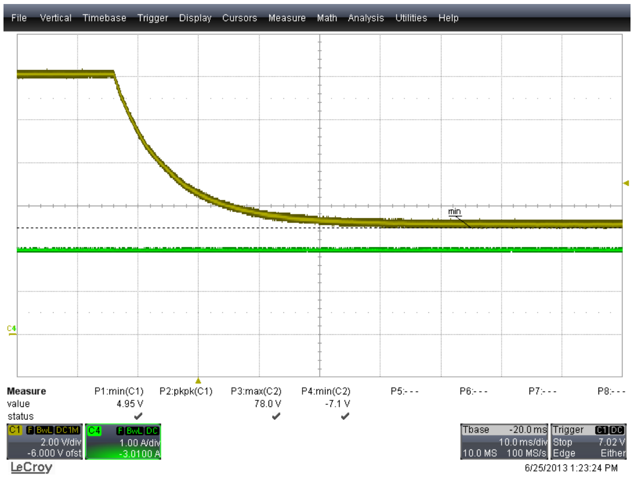
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.92 V		40.3 V	-4.8 V				
status	✓		✓	✓				

Figure 67 – V_{OUT} from 12 V to 5 V, 90 VAC 2 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.93 V		77.0 V	-6.8 V				
status	✓		✓	✓				

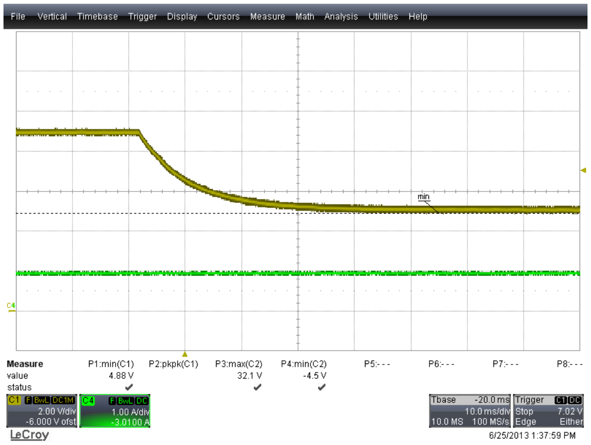
Figure 68 – V_{OUT} from 9 V to 5 V, 265 VAC 2 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



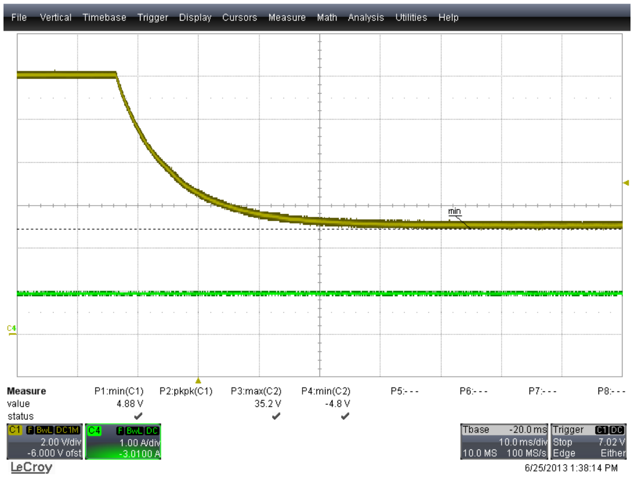
Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.95 V		78.0 V	-7.1 V				
status	✓		✓	✓				

Figure 69 – V_{OUT} from 12 V to 5 V, 265 VAC 2 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

13.7.5 Voltage Toggle Down at Half Load 1 A



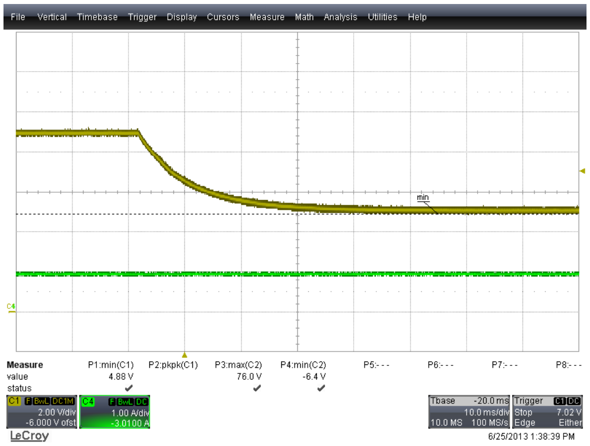
Measure P1:min(C1) P2:pkpk(C1) P3:max(C2) P4:min(C2) P5:- - - P6:- - - P7:- - - P8:- - -
value 4.88 V 32.1 V -4.5 V
C1 2.00 V/div -6.000 V ofst
C4 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:37:59 PM



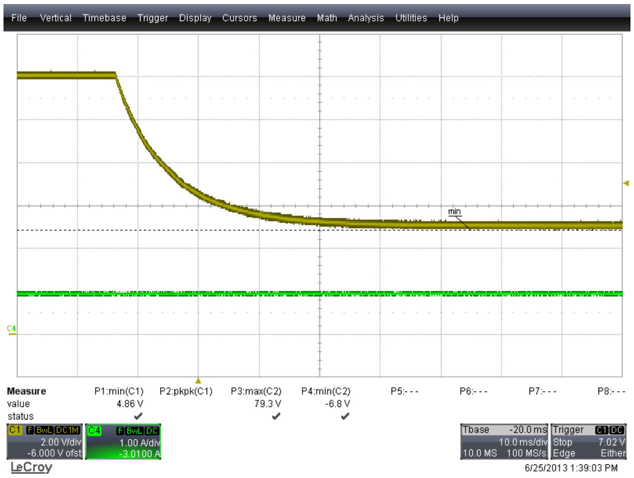
Measure P1:min(C1) P2:pkpk(C1) P3:max(C2) P4:min(C2) P5:- - - P6:- - - P7:- - - P8:- - -
value 4.88 V 35.2 V -4.8 V
C1 2.00 V/div -6.000 V ofst
C4 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:38:14 PM

Figure 70 – V_{OUT} from 9 V to 5 V, 90 VAC 1 A.
Upper: Vo, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

Figure 71 – V_{OUT} from 12 V to 5 V, 90 VAC 1A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure P1:min(C1) P2:pkpk(C1) P3:max(C2) P4:min(C2) P5:- - - P6:- - - P7:- - - P8:- - -
value 4.88 V 76.0 V -6.4 V
C1 2.00 V/div -6.000 V ofst
C4 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:38:39 PM

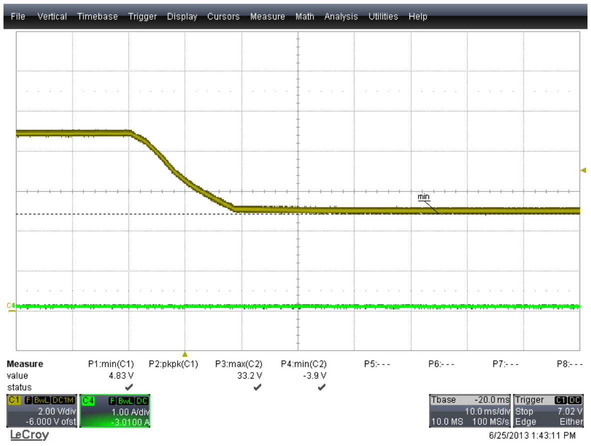


Measure P1:min(C1) P2:pkpk(C1) P3:max(C2) P4:min(C2) P5:- - - P6:- - - P7:- - - P8:- - -
value 4.86 V 79.3 V -6.8 V
C1 2.00 V/div -6.000 V ofst
C4 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:39:03 PM

Figure 72 – V_{OUT} from 9 V to 5 V, 265 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

Figure 73 – V_{OUT} from 12 V to 5 V, 265 VAC 1 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

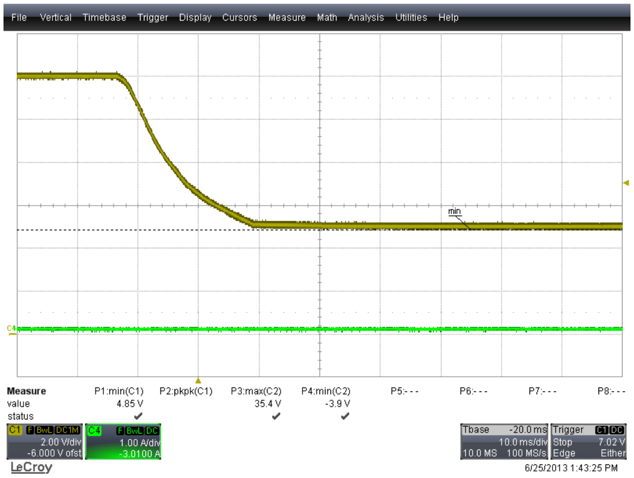
13.7.6 Voltage Toggle Down at Light Load 0.15 A



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.83 V		33.2 V	-3.9 V				
status	✓		✓	✓				

C1 F BwL DC1M 2.00 V/div -6.000 V ofst
C4 F BwL DC 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:43:11 PM

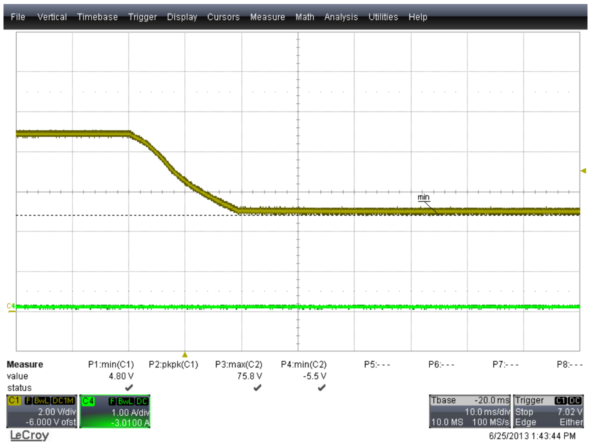
Figure 74 – V_{OUT} from 9 V to 5 V, 90 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		35.4 V	-3.9 V				
status	✓		✓	✓				

C1 F BwL DC1M 2.00 V/div -6.000 V ofst
C4 F BwL DC 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:43:25 PM

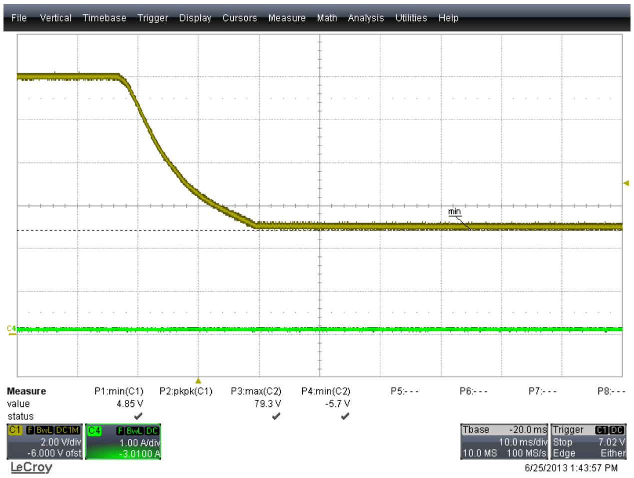
Figure 75 – V_{OUT} from 12 V to 5 V, 90 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.80 V		75.8 V	-5.5 V				
status	✓		✓	✓				

C1 F BwL DC1M 2.00 V/div -6.000 V ofst
C4 F BwL DC 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:43:44 PM

Figure 76 – V_{OUT} from 9 V to 5 V, 265 VAC 0.15 A.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.



Measure	P1:min(C1)	P2:pkpk(C1)	P3:max(C2)	P4:min(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	4.85 V		79.3 V	-5.7 V				
status	✓		✓	✓				

C1 F BwL DC1M 2.00 V/div -6.000 V ofst
C4 F BwL DC 1.00 A/div -3.0100 A
Tbase -20.0 ms 10.0 ms/div 10.0 MS 100 MS/s
Trigger C1 DC Stop 7.02 V Edge Either
6/25/2013 1:43:57 PM

Figure 77 – V_{OUT} from 12 V to 5 V, 265 VAC 0.15 A.
Upper: V_{OUT}, 2V / div.
Lower: I_{OUT}, 1 A, 10 ms / div.

13.8 USB Unplugged Wavforms

13.8.1 9 V USB Unplugged Waveforms

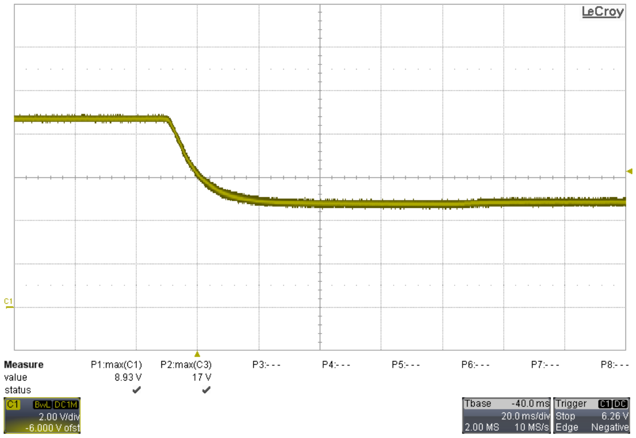


Figure 78 – 9 V, 115 VAC USB Unplugged.
V_{OUT}, 2 V, 20 ms / div.

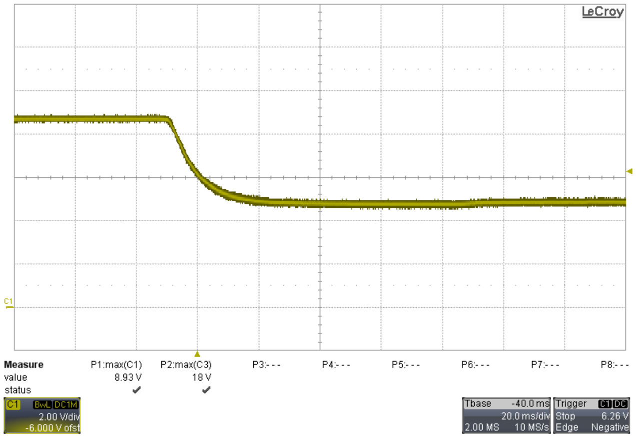


Figure 79 – 9 V, 230 VAC USB Unplugged.
V_{OUT}, 2 V, 20 ms / div.

13.8.2 12 V USB Unplugged Waveforms

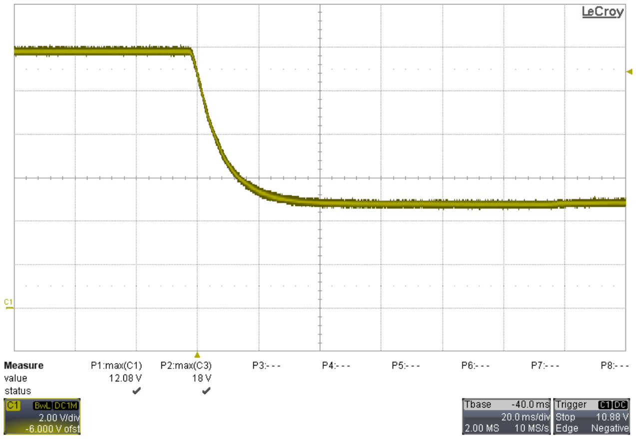


Figure 80 – 12 V, 115 VAC USB Unplugged.
V_{OUT}, 2 V, 20 ms / div.

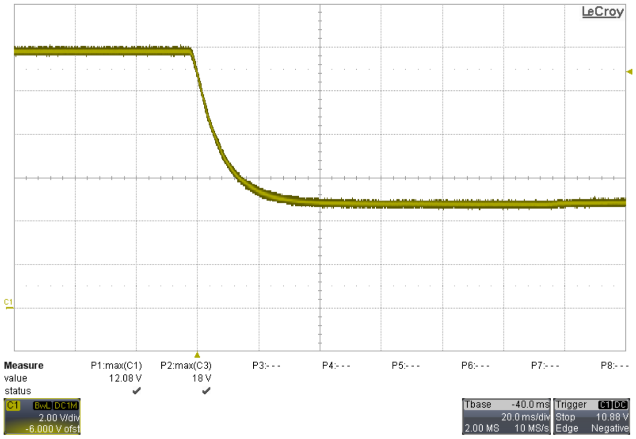


Figure 81 – 12 V, 230 VAC USB Unplugged.
V_{OUT}, 2 V, 20 ms / div.

13.9 Control Loop Measurements

13.9.1 12 V Loop Test

	Half Load		**Full Load**	
Input (VAC)	**Cross Over Frequency (kHz)**	**Phase Margin (º)**	**Cross Over Frequency (kHz)**	**Phase Margin (º)**
115	3.4	83	2.95	80
230	2.5	82	2.2	78

13.9.2 5 V Loop Test

	Half Load		**Full Load**	
Input (VAC)	**Cross Over Frequency (kHz)**	**Phase Margin (º)**	**Cross Over Frequency (kHz)**	**Phase Margin (º)**
115	4	86	3.8	75
230	7.5	85	8	62

14 Conducted EMI

Equipment used: Rohde and Schwarz ESPI3 (PN: m1142.8007.03 / EMI Test Receiver 9 kHz to 3 GHz).

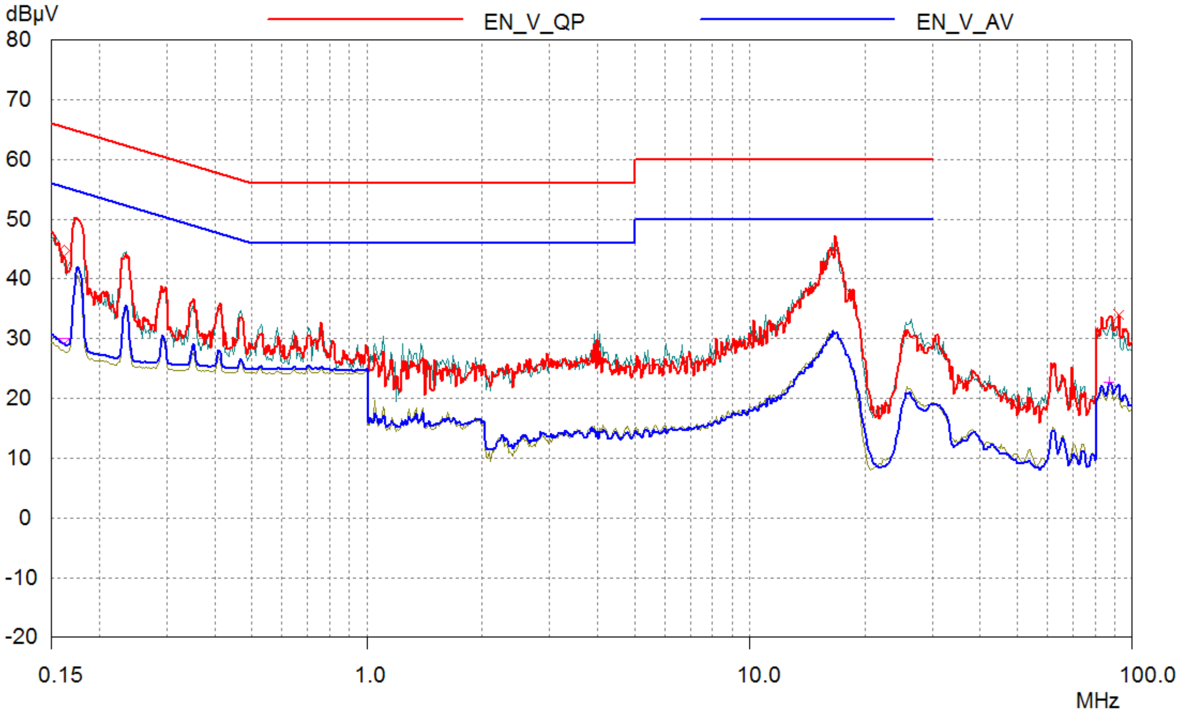


Figure 82 – Conducted EMI, 2 A Resistor Load, 115 VAC, 60 Hz, 5 V Output. Output Connected to PE.

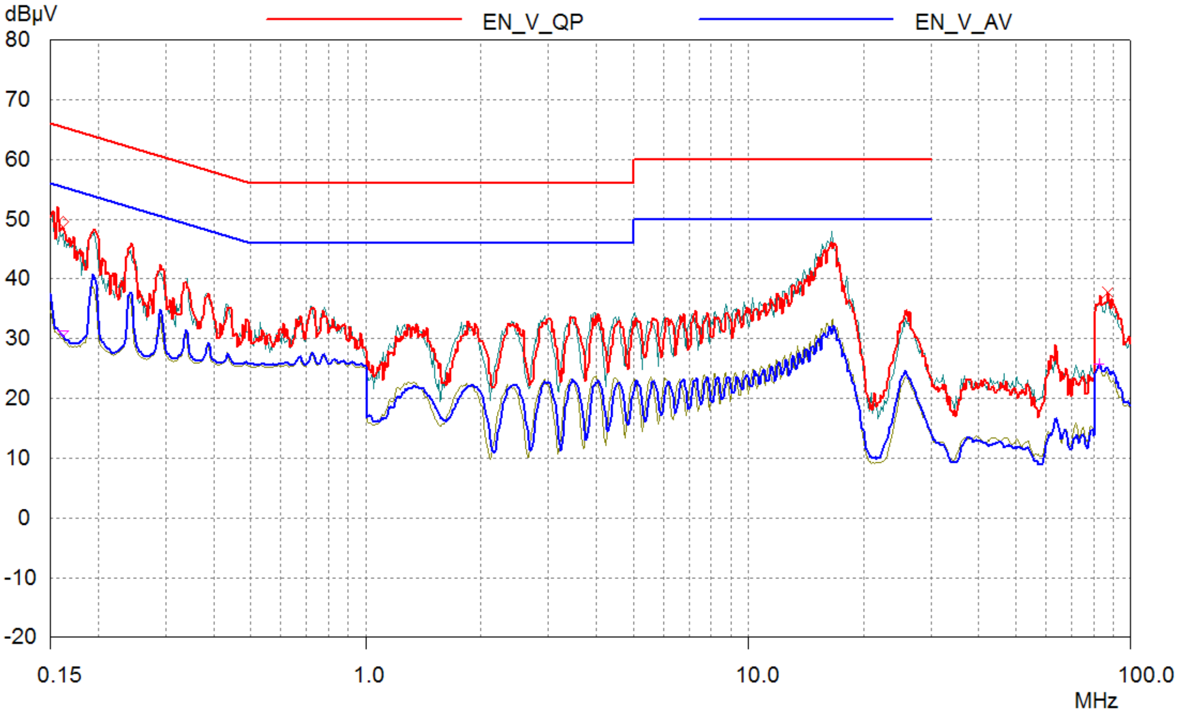


Figure 83 – Conducted EMI, 2A Resistor Load, 230 VAC, 60 Hz, 5 V Output. Output Connected to PE.

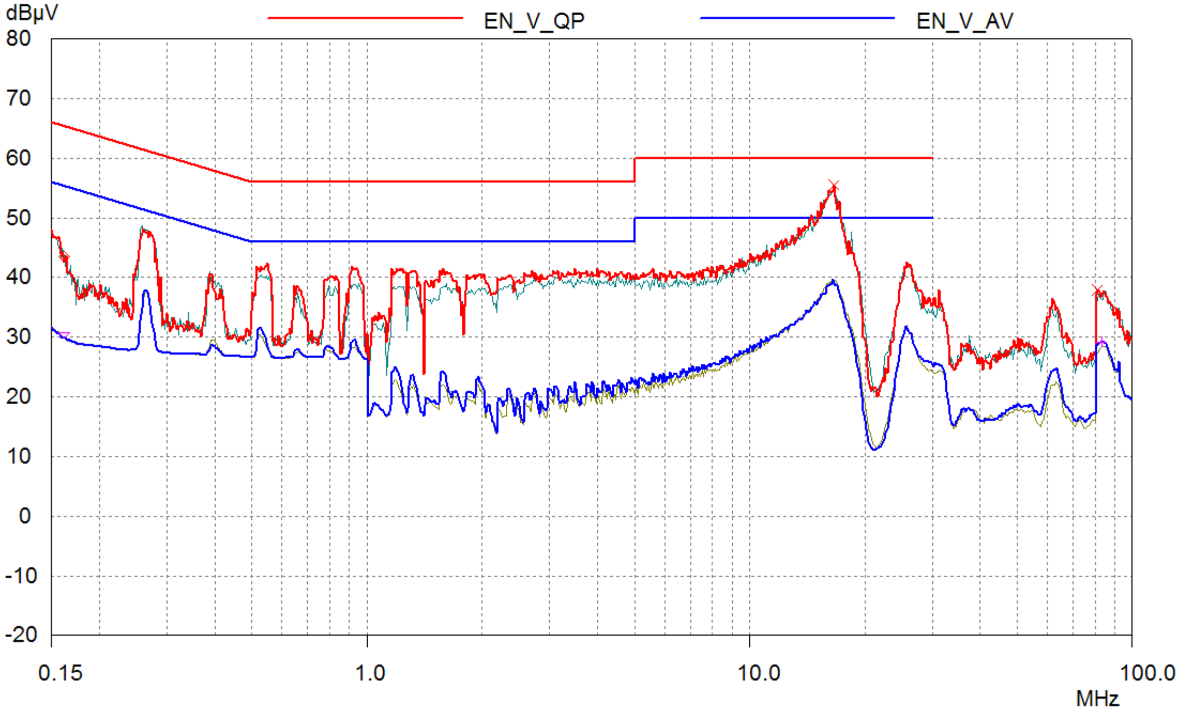


Figure 84 – Conducted EMI, 2 A Resistor Load, 115 VAC, 60 Hz, 12 V output. Output Connected to PE.

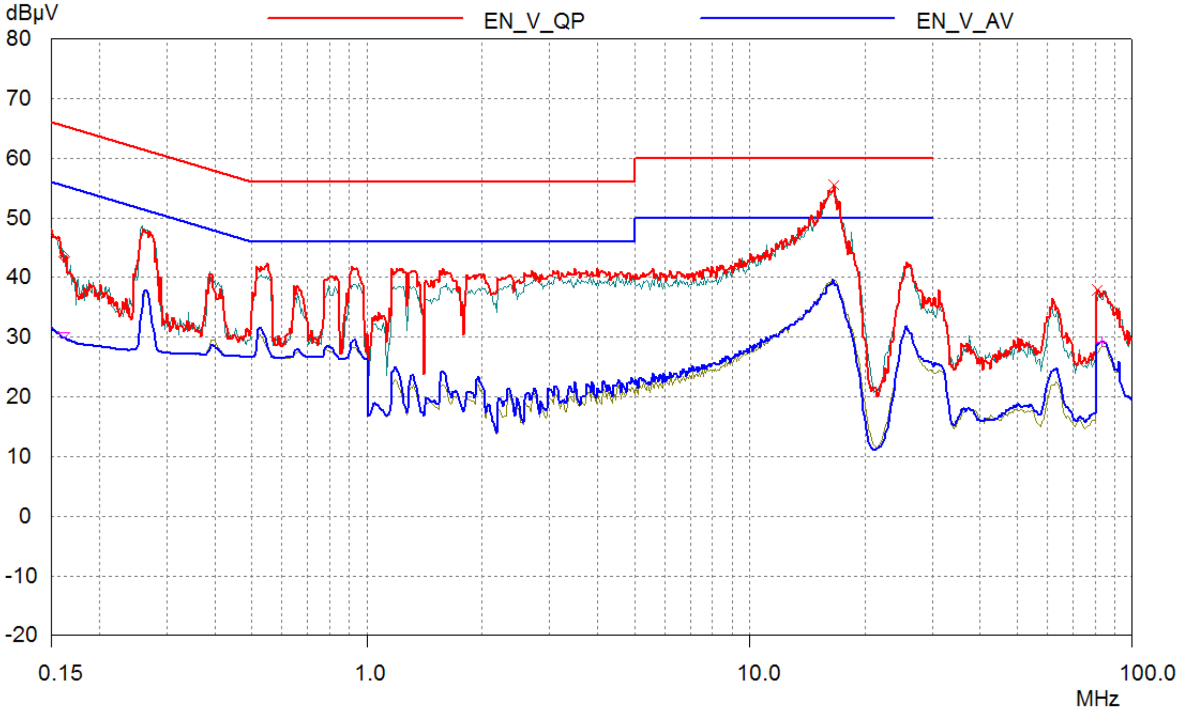


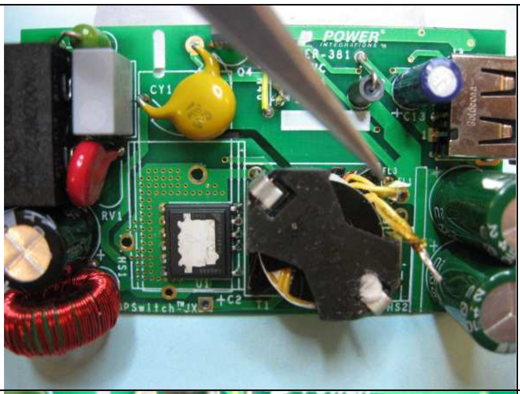
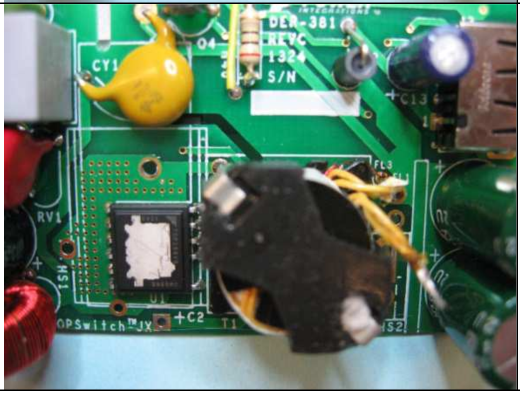
Figure 85 – Conducted EMI, 2 A Resistor Load, 230 VAC, 60 Hz, 12 V Output. Output Connected to PE.

15 Appendix A - Special Assembly Instruction

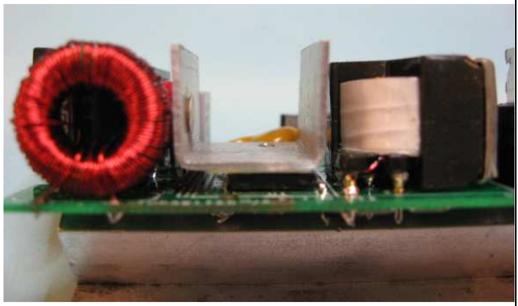
15.1 Materials

Item	Description
[1]	RTV 670810, GE, 66-00038-00.
[2]	RTV Application Gun.
[3]	Teflon Tubing, 66-00132-00.
[4]	Double Sided Thermal Tape, 60-00024-00.

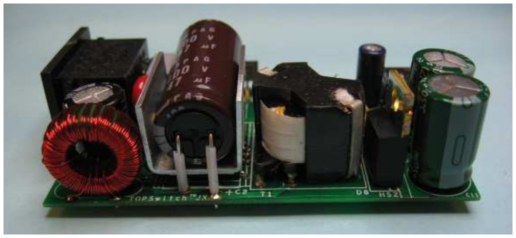
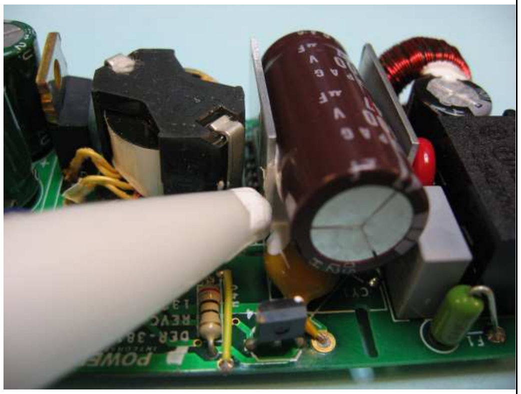
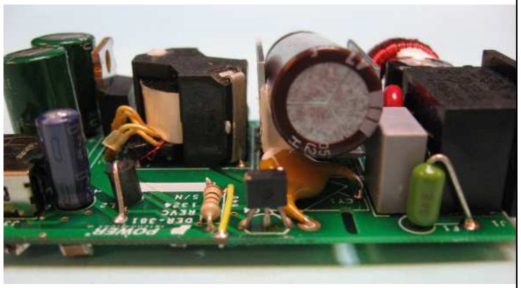
15.2 Transformer Installation (T1)

FL1, FL3		Install and solder T1 primary side pins. Locate the FL1 tagged secondary lead and insert into the designated FL1 board reference and solder. Locate the FL3 tagged bias lead and insert into the designated FL3 board reference and solder.
FL2		Locate the FL2 lead and insert into the FL2 board reference. Apply solder.

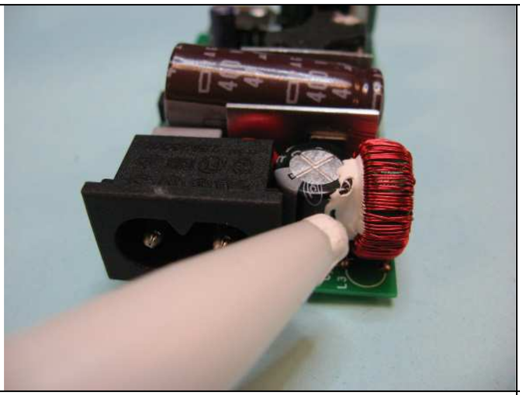
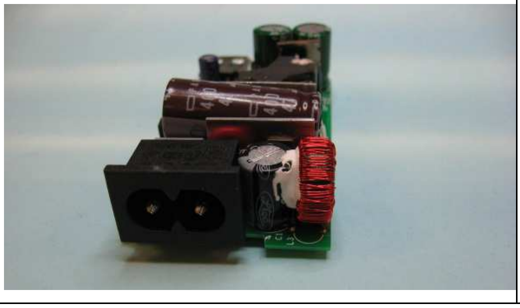
15.3 Heat Sink Installation

Cut Thermal Tape **PI # 60-00042-00**		Cut a piece of double sided thermal tape to .50” x.50”.
Apply Thermal Tape		Apply the termal tape to the bottom side of the heat sink.
Remove Tape Backing		Remove the backing from thermal tape.
Install Heat Sink		Install the heatsink and apply enough pressure to make sure that it sits securely on top of the device. Solder both heat sink pins.

15.4 Capacitor Installation (C2)

Cut Teflon Tubing		Cut two lengths of teflon tubing to .350” and slide over each of the leads of C2.
Install C2		Locate the C2 board reference and solder C2 in between the fins of the heat sink.
Apply RTV **PI # 66-00038-00**		Apply RTV to C2 making sure that there is a slight gap between the body of the capacitor and the heat sink.
Check Spacing		Check the gap between the capacitor and the heat sink. The capacitor should not have any contact with the heat sink.

15.5 Apply RTV (C1 and L3)

Apply RTV **PI # 66-00038-00**		Apply RTV to secure L3 to C1.
Check Alignment		Make sure that L3 is straight and does not lean outside the boundary of the circuit board.

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
08-Oct-13	PL	1.0	Initial release	Apps & Mktg
31-Mar-14	KM	1.1	Added transformer supplier	
11-Apr-14	KM	1.2	Corrected schematic	

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

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