Design Example Report

Title	***70 W USB In-Wall Charger using InnoSwitch™4-CZ with PowiGaN™ INN4074C-H182 and ClampZero™ CPZ1062M (High-Line Input)***
Specification	180 VAC – 265 VAC Input*; 5 V / 6.5 A, 9 V / 5 A, 15 V / 4 A, 20 V / 3.5 A Outputs
Application	USB Wall Outlet, Power Strip with USB Charging Ports
Author	Applications Engineering Department
Document Number	DER-958
Date	November 10, 2022
Revision	1.0

Summary and Features

- 70 W low profile compact power supply for high power USB Type-A/C port charging
- >94.5% Full Load Efficiency at nominal Input
- *Optimized for 180 VAC to 265 VAC operation but can operate down to 100 VAC to accommodate unstable mains grids
- <20 mW system no-load input power
- PowiGaN-based InnoSwitch4-CZ benefits
    - Highly integrated switcher IC with integrated high-voltage switch, synchronous rectification and FluxLink™ feedback
    - Zero voltage switching in both CCM and DCM operating conditions
    - GAN-based Integrated MOSFET enables heat sink-less design
    - Fast instantaneous transient response with 0%-100%-0% load step
    - Constant Power (CP) profile minimizes charging time with continuous adjustment of output current and voltage
- Low components count (<60)
- Easily meets DOE6 efficiency requirements
- Integrated protection and reliability features
    - Output short-circuit protection
    - OVP, OCP and OTP protection
- Meets 2.0 kV differential surge and EN55022 conducted EMI

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
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www.power.com

- Suitable for compact enclosures with high operating ambient temperature
- Very high power density: 24.9 W/in^3 without enclosure (70 W / 2.24 in X 1.54 in X 0.82 in)

Table of Contents

Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes an off-line 70 W isolated flyback power supply designed to operate at an input voltage range from 180 VAC to 265 VAC within its 4 selectable output ranges (20 V / 3.5 A, 15 V / 4 A, 9 V / 5 A and 5 V / 6.5 A). This power supply uses active clamp topology featuring Power Integrations' InnoSwitch4-CZ (INN4074-H182) partnered with ClampZero (CPZ1062M).

The InnoSwitc4-CZ family of ICs partners with the ClampZero family of active clamp ICs to dramatically improve the efficiency of flyback power converters, particularly those requiring a compact form-factor. This combination of ICs greatly reduces system and primary switch losses, allowing for extremely high power densities.

The InnoSwitch4-CZ family incorporates primary and secondary controllers and safety-rated feedback into a single IC. It also includes multiple protection features including output overvoltage and over-current limiting, and over-temperature shutdown.

DER-958 offers a high efficiency (94.5%), low component count, and heatsink-less design to meet increasing demands for power savings and small form factor enclosures. It is also suitable for compact enclosures with high operating ambient temperatures due to InnoSwitch4-CZ's excellent thermal performance and the use of a four-layer PCB design.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet, and performance data.

Figure 1 – Populated Circuit Board.

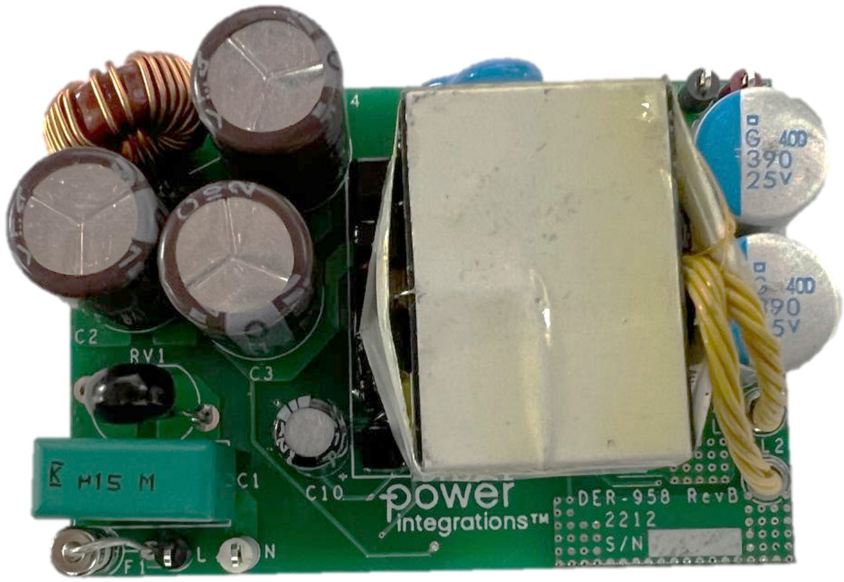


Figure 2 – Populated Circuit Board, Top View.

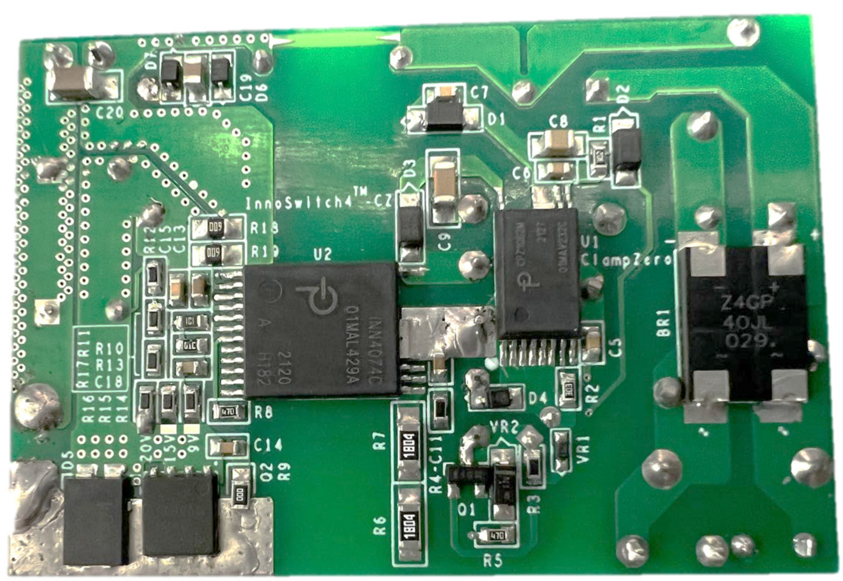


Figure 3 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	180	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50		Hz	
No-load Input Power (230 VAC)			15		mW	Measured at 230 VAC, 5 V Output.
5 V Output						
Output Voltage	V_{OUT}		5		V	±3%
Output Ripple Voltage	V_{RIPPLE}			98	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			6.5	A	20 MHz Bandwidth.
Efficiency	n		90			Measured at 230 VAC.
9 V Output						
Output Voltage	V_{OUT}		9		V	±5%
Output Ripple Voltage	V_{RIPPLE}			115	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			5	A	20 MHz Bandwidth.
Efficiency	n		93.5		%	Measured at 230 VAC.
15 V Output						
Output Voltage	I_{OUT}		15		V	±5%
Output Ripple Voltage	V_{RIPPLE}			117	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			4	A	20 MHz Bandwidth.
Efficiency	n		94.6		%	Measured at 230 VAC.
20 V Output						
Output Voltage	V_{OUT}		20		V	±5%
Output Ripple Voltage	V_{RIPPLE}			128	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			3.5	A	20 MHz Bandwidth.
Efficiency	n		94.7		%	Measured at 230 VAC.

For extended output load requirement at 9 V output.

9 V Output						
Output Voltage	V_{OUT}		9		V	±5%
Output Ripple Voltage	V_{RIPPLE}			86	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			6	A	20 MHz Bandwidth.
Efficiency	n		93		%	Measured at 230 VAC.

3 Schematic

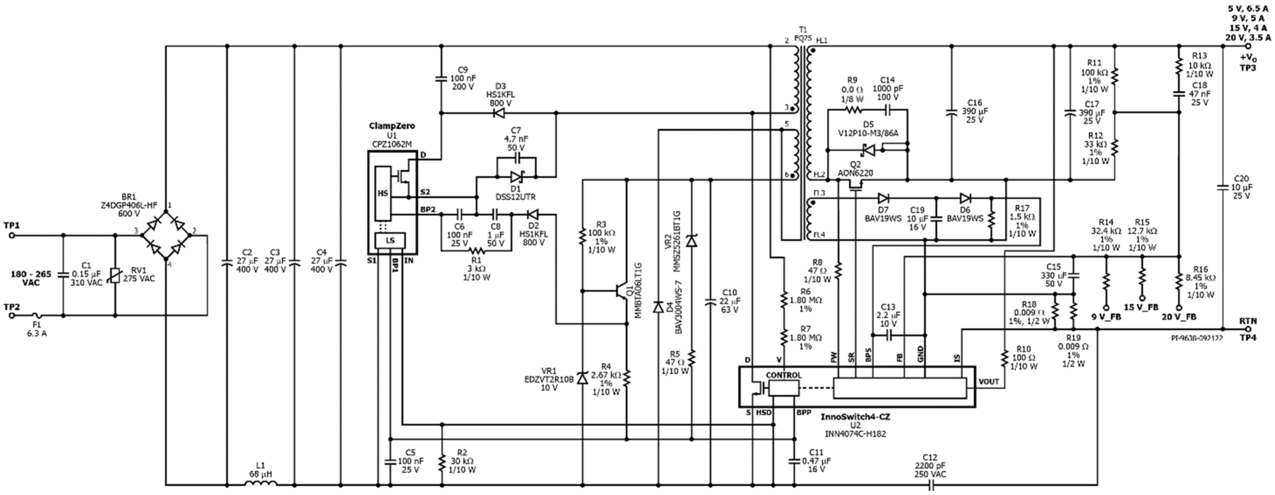


Figure 4 – Main Board Schematic.

4 Circuit Description

The circuit is an active clamp flyback power supply with synchronous rectification controlled by the InnoSwitch4-CZ IC (U4) using PowiGaN as primary-side switch. Besides the high-voltage PowiGaN switch, the IC incorporates primary-side controller, secondary-side controller and FluxLink feedback signals in one single package. Moreover, it controls the ClampZero IC (U2) for the active clamp operation needed to obtain ultra-high efficiencies. The decreased switching losses allows the InnoSwitch4-CZ IC to operate at high switching frequencies, resulting to smaller magnetics and decreased overall form factor of the power supply.

4.1 Input EMI Filter and Rectifier

The input fuse (F1) provides safety protection from component failures. Metal oxide varistor (RV1) help prevents component failure in the event of high-voltage input line surge. The AC input voltage is full wave rectified by the bridge rectifier (BR1) and then filtered by the bulk capacitors (C2, C3, and C4) to provide a smooth DC input voltage supply to the flyback circuitry. Input differential mode choke (L1) is connected between C2 and C3 to provide differential mode noise filtering and at the same time forms a PI filter circuit. A low ESR electrolytic capacitor is recommended for the bulk capacitors (C2, C3, and C4) for better differential mode noise filtering and higher efficiency. Y capacitor (C12) bypass common mode noise back to the primary power ground. X capacitor (C1) helps reduce the differential mode EMI noise.

4.2 Primary-side Controller: InnoSwitch4-CZ

The power transformer (T1) is designed for flyback power conversion. For a better EMI shielding, the primary winding start terminal (pin 3) must be connected to the noisy DRAIN pin of the PowiGaN switch inside InnoSwitch4-CZ IC and the finish terminal (pin 2) is connected to the positive terminal of the bulk capacitor (C4). Snubber circuit formed by D3 and C9 cuts down leakage voltage spike and help minimize the voltage stress across the PowiGaN switch. Fast recovery diode is recommended for D3.

In contrast with the traditional RCD clamp, this snubber configuration used by InnoSwitch4-CZ IC does not use resistors to dissipate energy from the leakage inductance. Rather, the energy from the leakage inductance gets stored in C9 and eventually recycled to achieve zero-voltage switching (ZVS) across the PowiGaN. Right before the next turn-on of the PowiGaN the high-side switch of the ClampZero IC turns on, causing energy from C9 to flow and charge up the leakage inductance. The current stored across the leakage inductance then forces the output capacitance of the PowiGaN to discharge down to zero, just in time before the PowiGaN turns on again. This ZVS behavior dramatically lowers the switching losses across the PowiGaN, allowing it to operate at much higher frequencies.

The switching pattern of U2 serves as key to achieving ZVS. When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ IC generates a signal coming from its HSD pin to turn on the ClampZero IC (via the IN pin) for a fixed duration, t_{HSD}. During this time, C9 charges the leakage inductance, in case of CCM operation, or both the leakage and magnetizing inductances, in case of DCM operation. After charging the leakage, the ClampZero IC turns off while the InnoSwitch4-CZ IC waits for a certain delay time (t_{LLDL} at lowline input or t_{HLDL} at highline input) before turning on the PowiGaN switch. During this delay time, the voltage stored across the PowiGaN's drain capacitance gets discharged by the leakage inductance, forcing it to go down to zero volts and achieve ZVS operation as the PowiGaN turns on again.

The delay time is fixed when operating at highline, equivalent to t_{HLDL}, while the value for lowline delay time, t_{LLDL}, is programmed via HSD resistor, R2, connected between the HSD pin and the SOURCE pin.

The InnoSwitch4-CZ IC is self-starting, where an internal high-voltage current source coming from the DRAIN pin charges the PRIMARY BYPASS pin (BPP) capacitor C11 that powers the primary-side controller. During normal operation, the primary-side controller is powered via the bias winding of the transformer T1. Output of this bias winding is rectified by diode D4 and filtered by capacitor C10. The bias voltage across C10 powers the linear regulator formed by Zener diode VR1, biasing resistor R3, transistor Q1, and limiting resistor R4. The voltage formed across R4 (Q1 emitter voltage minus BPP shunt voltage) divided by its resistance defines the current supplied to the BPP.

Output regulation is achieved using a modulation technique where the switching frequency, F_{SW}, and primary current limit, I_{LIM}, are adjusted based on the output load. At heavy loads, the primary pulses occur at high F_{SW} and terminates at a high value of I_{LIM} in the selected I_{LIM} range. As the load decreases, both F_{SW} and I_{LIM} also decrease. At light loads or no-load condition, F_{SW} goes down to its minimum value and several pulses get disabled (cycle skipping).

The V pin resistors (R6 and R7) serves as input line voltage monitoring. It is connected between high-voltage positive bulk capacitor (C3 and C4) and V pin terminal. The input line voltage is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds. The value selected for R6 and R7 in total was 3.6 MΩ to get the optimum efficiency at highline input voltage.

4.3 Active Clamp: ClampZero

Capacitor C5 serves as local decoupling to the BP1 pin of the ClampZero IC, which provides power to its low-side control. Diode D2 and capacitor C8 form a bootstrap circuit to provide the bias for the high-side BP2 pin by getting power from the linear regulator derived from Q1. Resistor R1 serves as current limiting to BP2 (similar in function to R4) while C6 acts as a local decoupling capacitor.

Ultrafast diode D1 prevents current from the leakage inductance to flow through its body diode at the instant the PowiGaN switch of InnoSwitch4-CZ IC turns off.

Signal from the HSD pin of InnoSwitch4-CZ IC goes to the IN pin of ClampZero IC and is then communicated by the low-side control to the high-side drive to turn on the ClampZero switch. Once on, the ClampZero IC switch provides an energy path from C9 towards the leakage inductance of T1.

As previously mentioned, the on-time of the ClampZero IC is a constant, defined by t_{HSD}, while the delay time between the ClampZero IC turn-off and the InnoSwitch4-CZ IC turn-on is defined by R2 at lowline (t_{LLDL}) or a fixed value at highline (t_{HLDL}).

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR2 with current limiting resistor R5. In a flyback converter, output of the bias winding tracks the output voltage of the converter by the winding turns-ratio. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4-CZ IC U2. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U2 controller auto-restarts to prevent any further increase in output voltage.

4.4 Secondary-Side Control

The secondary winding start terminal (FL1) of the transformer (T1) is connected to the positive terminal of output capacitor C16 and C17 while the finish terminal is connected to the DRAIN pin of the SR FET (Q2). The secondary winding voltage is rectified by the SR FET and then filtered by the output capacitors C16 and C17. Leakage voltage spike and ringing across SR FET drain to source during off time is minimized by the secondary RC snubber (R9 and C14). For high efficiency requirement, shorting R9 will help improve the efficiency. Schottky diode D5 helps improve full load efficiency specially at 5 V where output current is highest.

The secondary-side circuity of the IC is initially self-powered by the internal regulator which is supplied by either the secondary winding forward voltage (through FW pin) or by the output voltage (through VO pin). However, to improve the system efficiency and reduce the secondary-side internal consumption, a bias winding circuit was used. It is designed to supply current to the IC when the output voltage is set to 20 V. Bias winding voltage is rectified by diode D7 and filtered by capacitor C19. Resistor R17 limits the current flowing to the BPS pin of U2. Diode D6 blocks BPS from charging C19 that might affect startup operation. Capacitor C13 connected to the BPS pin of IC U2 provides decoupling for the internal circuitry.

When the output voltage (VO) falls during constant current mode operation, the secondary-side internal regulator will be supplied by the secondary winding forward voltage through FORWARD (FWD) pin resistor (R8). This will maintain the output current regulation down to the minimum BPS pin auto-restart voltage threshold. Below this level the unit enters auto-restart until the output load is reduced. A 47 Ω resistor is recommended for FWD pin resistor (R8) to ensure sufficient IC supply current.

The forward voltage sensed by FWD pin from secondary winding is also used for both handshaking and switching control for the SR FET (Q2), which is driven by the SYNCHRONOUS RECTIFIER DRIVE (SR) pin. The FWD pin voltage is used to determine when to turn off the SR FET in discontinuous conduction mode (DCM). The SR FET is turned off when the voltage drop across the MOSFET falls below $V_{SR(TH)}$. In continuous conduction mode (CCM), the SR FET is turned off just prior to the secondary-side commanding a new switching cycle to the primary.

Output current is sensed by monitoring the voltage drop across resistors R18 and R19 between the IS and SECONDARY GROUND pins. The internal constant current sense threshold is approximately 35 mV. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

Below the CC threshold, the device operates in constant voltage mode. The external resistor divider network (R11 and R12) is used for output voltage sensing to regulate the output voltage. The rest of the lower voltage divider resistors (R14, R15, and R16) are used to set output voltage from 5 V to 9 V, 15 V and 20 V respectively. The internal voltage comparator reference voltage is V_{FB} (1.265 V). A phase boost RC network (R13 and C18) is added to optimize ripple voltage.

5 PCB Layout

PCB specifications:

- Layer count: 2 layers
- Solder mask: Green
- Silkscreen: White
- Finish: LF HASL
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz.
- Material: FR4

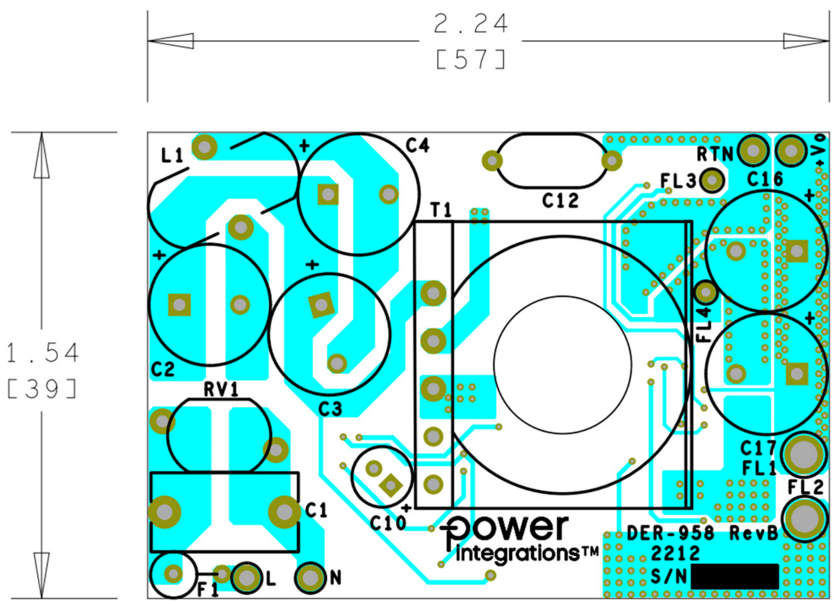


Figure 5 – Top Side.

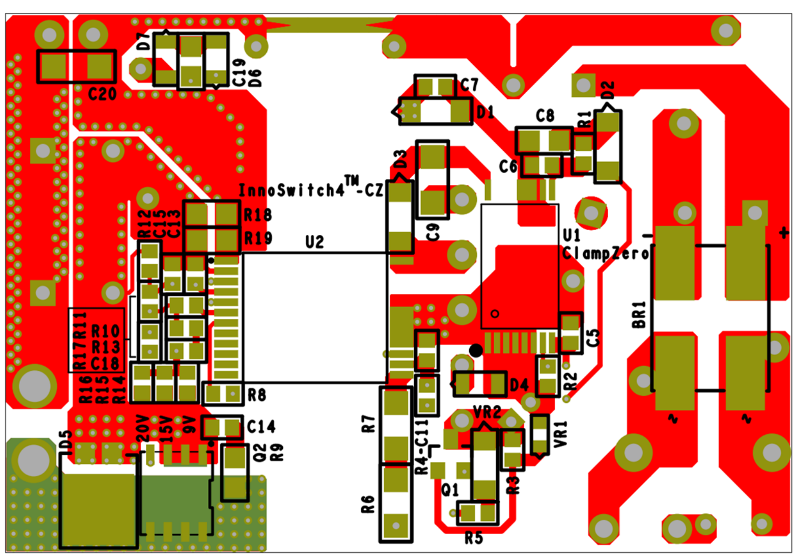


Figure 6 – Bottom Side (flipped).

6 Bill of Materials

6.1 Electrical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 600 V, 4 A, Z4-D, -55 °C ~ 175 °C (TJ)	Z4DGP406L-HF	Comchip
2	1	C1	0.15 µF, Film, 310 VAC 630 VDC, Polypropylene (PP), Metallized Radial, X2	F861AP154M310C	KEMET
3	3	C2 C3 C4	27 µF, ±20%, 400 V, Electrolytic (10 x 15)	KCX ECAP 27uF 400V 10x15	www.sh-ymin.com
4	2	C5 C6	100 nF, 0.1 µF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
5	1	C7	4.7 nF 50 V, Ceramic, X7R, 0603	CL10B472KB8NNNC	Samsung
6	1	C8	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
7	1	C9	100 nF, 200 V, Ceramic, X7R, 1206	C1206C104K2RACTU	Kemet
8	1	C10	22 µF, ±20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
9	1	C11	0.47 µF, 10%, 16 V, X7R, 0603	GRM188R71C474KA88D	Murata
10	1	C12	2200 pF ±20%, 250 VAC Ceramic E Radial, Disc, X1, Y1	DE1E3RA222MN4AN01F	Murata
11	1	C13	2.2 µF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
12	1	C14	1000 pF, ±10%, 100 V, Ceramic, X7R, 0603	C0603C102K1RACTU	Kemet
13	1	C15	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
14	2	C16 C17	390 µF, 25 V, Al Organic Polymer, Gen. Purpose, 20% 10 x 13	APSG250ELL391MJB5S	United Chemi-con
15	1	C18	47 nF 25 V, Ceramic, X7R, 0603	CC0603KRX7R8BB473	Yago
16	1	C19	10 µF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
17	1	C20	10 µF, ±10%, 25V, Ceramic X7R, 1206	C3216X7R1E106K160AB	TDK
18	1	D1	Diode, Schottky, 20 V, 1 A, SMT, SOD-123FL	DSS12UTR	SMC Diode
19	2	D2 D3	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
20	1	D4	Diode, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
21	1	D5	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay
22	2	D6 D7	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
23	1	F1	6.3 A, 250 V AC DC, Fuse Cartridge, Ceramic Through Hole Cartridge, Non-Standard (Axial)	087706.3MRET1P	Littelfuse
24	1	L1	68 VH, Unshielded Toroidal Inductor, 2 A, 55 mΩ Max, Radial, Vertical (Open)	7447033	Wurth
25	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
26	1	Q2	MOSFET, N-CH, 100V, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
27	1	R1	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
28	1	R2	RES, 30 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ303V	Panasonic
29	2	R3 R11	RES, 100 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
30	1	R4	RES, 2.67 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2671V	Panasonic
31	2	R5 R8	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
32	2	R6 R7	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
33	1	R9	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole
34	1	R10	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
35	1	R12	RES, SMD, 33 kΩ, 1%, 1/10W, ±100ppm/°C, 0603	RC0603FR-0733KL	Yageo
36	1	R13	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
37	1	R14	RES, 32.4 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
38	1	R15	RES, 12.7 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1272V	Panasonic
39	1	R16	RES, 8.45 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8451V	Panasonic
40	1	R17	RES, 1.5 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1501V	Panasonic

41	2	R18 R19	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
42	1	RV1	275 V, 1.2 kA, Varistor, 1 Circuit, Through Hole, Disc 7 mm	ERZ-E05A431	Panasonic
43	1	T1	Bobbin, EQ25, 6 pins, 6pri, 0sec	POT-2501	Shenzhen xin yu jia
44	1	U1	ClampZero, MinSOP-16	CPZ1062M	Power Integrations
45	1	U2	InnoSwitch4-CZ, 75 W, insop-24D	INN4074C-H182	Power Integrations
46	1	VR1	10 V, 5%, 150 mW, SSMINI-2, SC-79, SOD-523, EMD2	EDZVT2R10B	Rohm Semi
47	1	VR2	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi

6.2 Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	TP1 TP4	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
2	1	TP2	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
3	1	TP3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone

7 Power Transformer Specification (T1)

7.1 Electrical Diagram

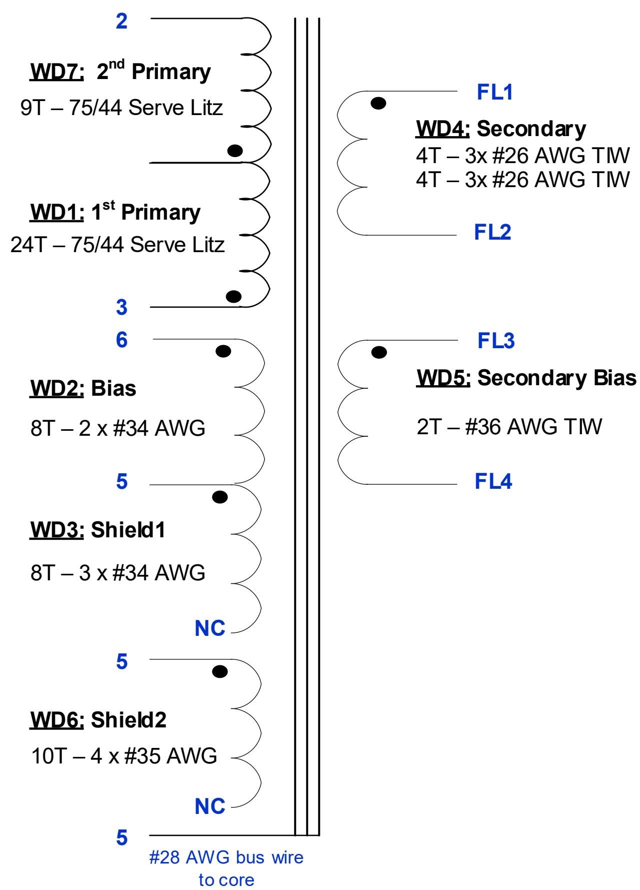


Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and 3, with all other windings open.	504 μH ± 5%
Resonant Frequency	Between pin 2 and 3, other windings open.	1,000 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and 3, with pins: FL1-FL2 shorted.	7.5 μH ± 4%

7.3 Material List

Item	Description
[1]	Core: EQ25, Material 3C95. FerroxCube.
[2]	Bobbin. EQ25-V-6pins. PI#: 25-01136-00.
[3]	Magnet Wire: Litz Wire 75/44
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #36 AWG, Triple Insulated Wire.
[7]	Magnet Wire: #35 AWG, Double Coated.
[8]	Bus Wire: #28 AWG (Solid) Tinned Copper.
[9]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 8 mm Width.
[10]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[11]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

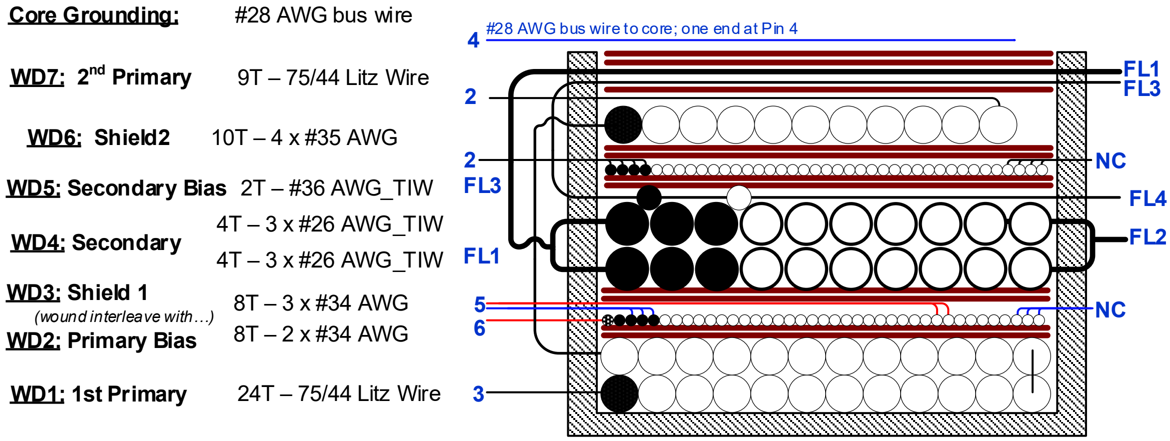
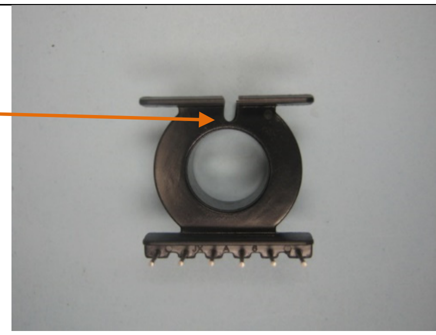
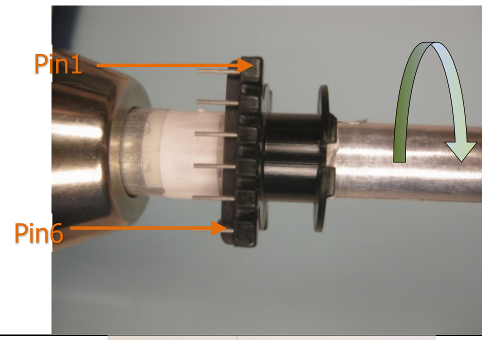
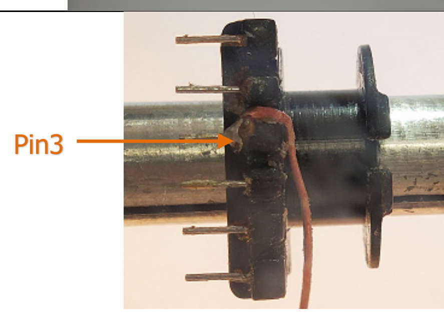
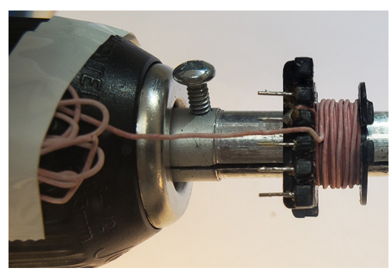
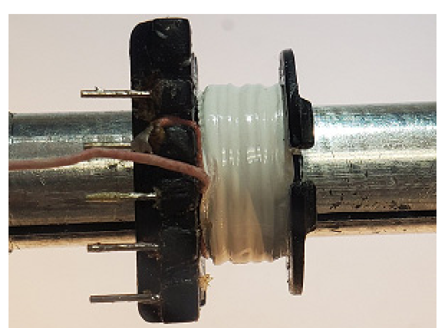


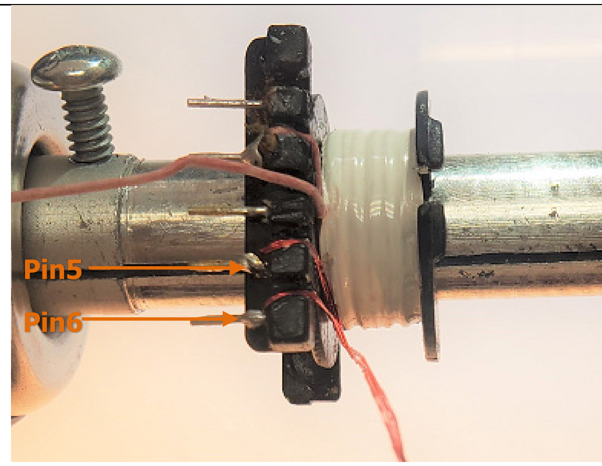
Figure 8 – Transformer Build Diagram.

7.5 Winding Illustrations

Bobbin Preparation <u>Make slots with 2.0 mm width</u> on both flanges of secondary-side of bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary-side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.	
Winding Directions Bobbin is oriented on winder jig such that terminal Pin 1- 6 are in the left side facing upward. The winding direction is clockwise.	
Winding 1- 1st Primary Use a 75/42 Litz wire, Item [3]. Start at Pin 3 and wind 12 turns evenly in 2 layers.	
Set aside an extension on the left side of the bobbin long enough for 9 turns (Winding 7).	
Apply 2 layer of polyester tape, Item [9] for insulation	

Winding 2 and 3 – Bias and shield 1

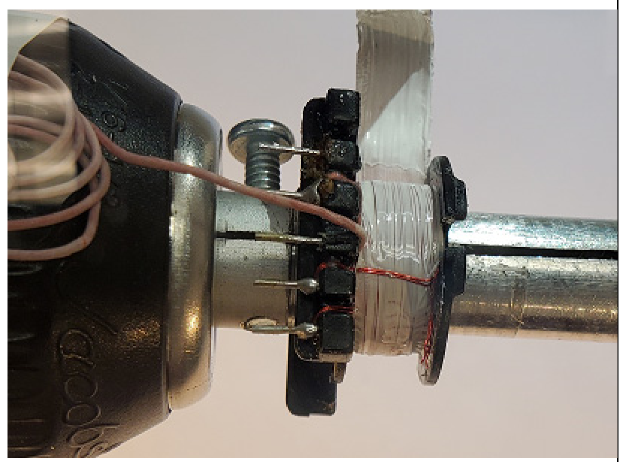
Use magnetic wire, Item [4] - AWG#34 for winding 2 and 3. Prepare bifilar wire for winding 2 and three (trifilar) wires for winding 3. For Winding 2, start at pin 6 while for winding 3, start at pin 5.



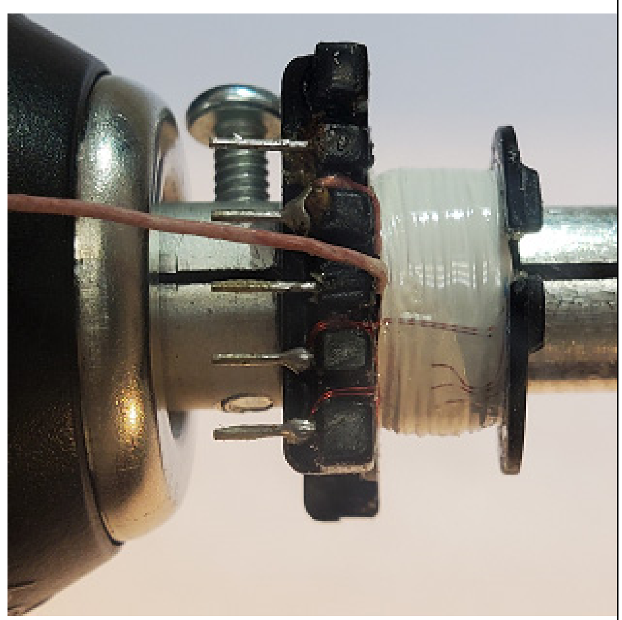
Wind winding 2 and 3 evenly together for 8 turns from left to right.

For winding 2, Finish the winding back to the left on Pin 5.

For winding 3, cut the finish terminal as shown in the figure.



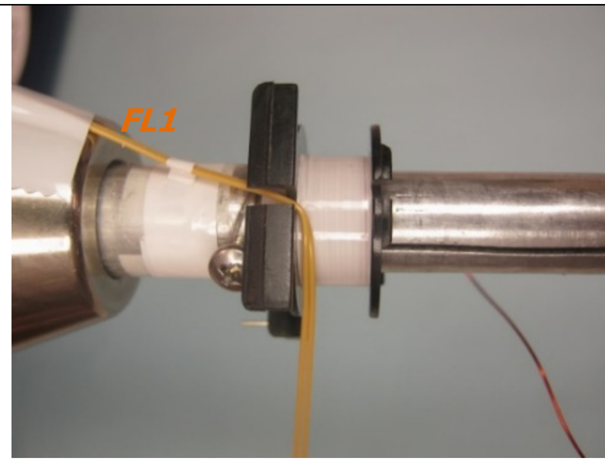
Apply 2 layer of polyester tape, Item [9] for insulation



Winding 4 and 5 - Secondary Winding and Secondary Bias Winding

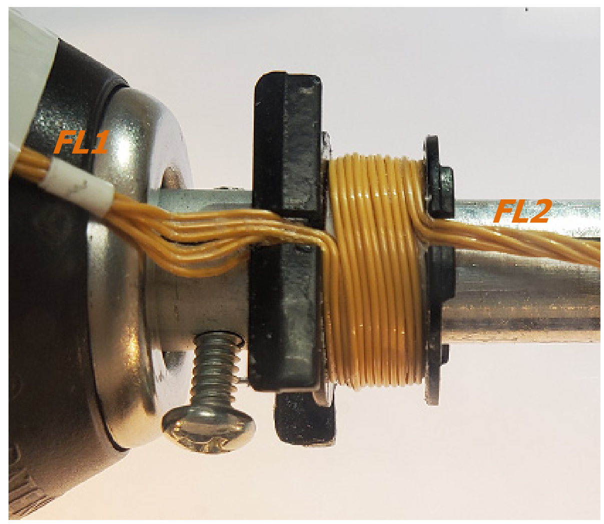
Position the bobbin on the other side with the secondary wire slot facing upward. Use TIW wire Item [5] – AWG#26.

First Layer - Prepare 3 (trifilar) wires and secure 75 mm fly lead (FL1) extension on the left side. Wind 4 turns evenly from left to right. Fix the finish fly lead terminal (FL2) on the right side of the jig and cut with around 75mm wire extension



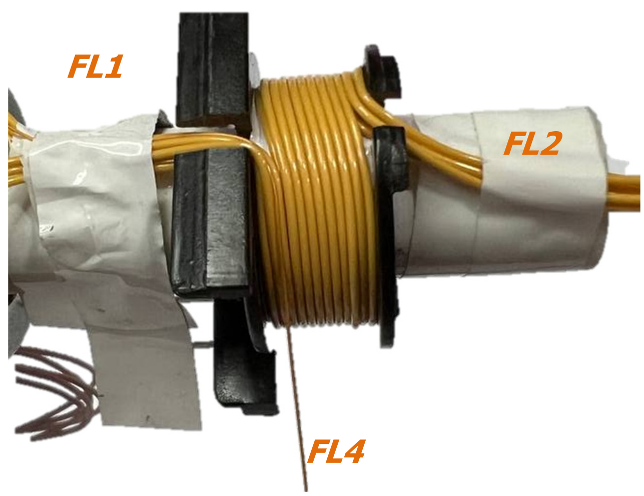
Second Layer – Same with the first layer, prepare 3 (trifilar) wires and secure 75 mm fly lead (FL1) extension on the left side. Wind 4 turns evenly from left to right. Fix the finish fly lead terminal (FL2) on the right side of the jig and cut with around 75mm wire extension.

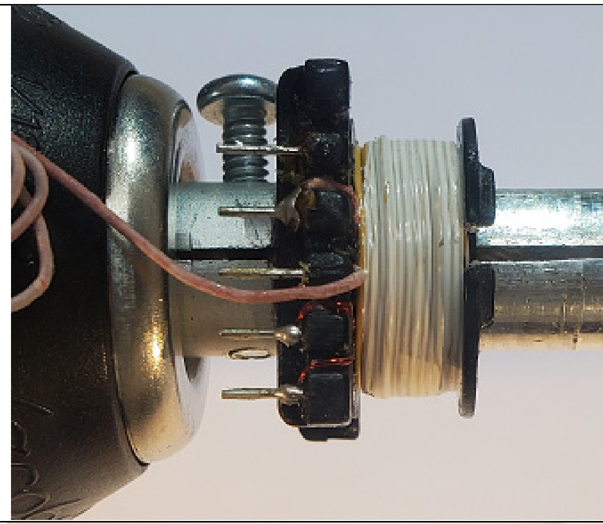
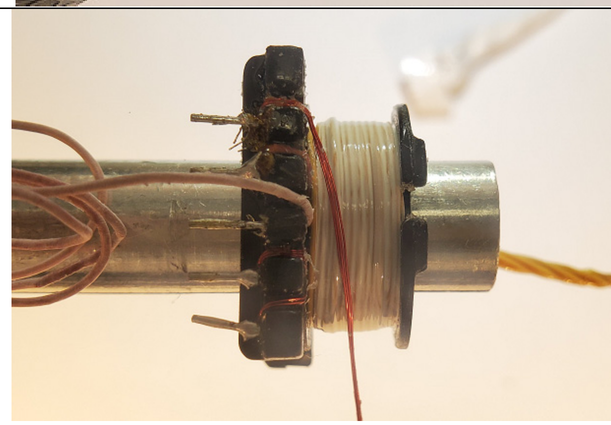
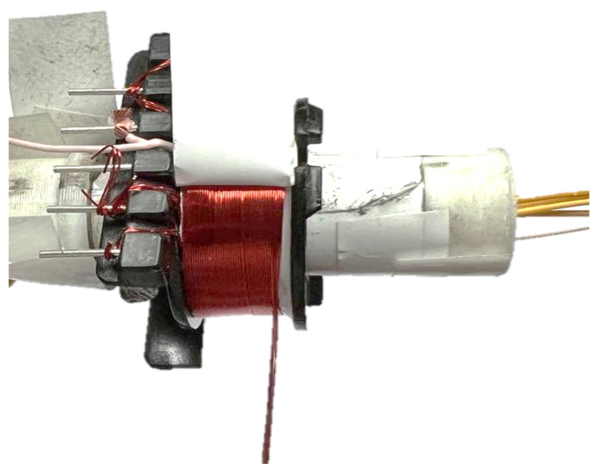
Combine fly lead wires from first and second layer and add polarity marking.



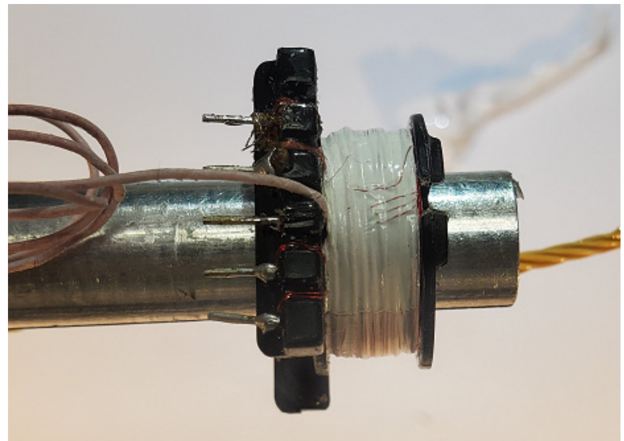
For Winding 5, Use TIW wire Item[6] AWG#36 and secure a 70mm fly lead (FL3) extension of the left side. Wind 2 turns from left to right. Fix the finish fly lead terminal (FL4) on the right side of the jig and cut with around 70mm wire extension.

Follow the ridges made by the secondary winding to minimize the bump in the next shield layer



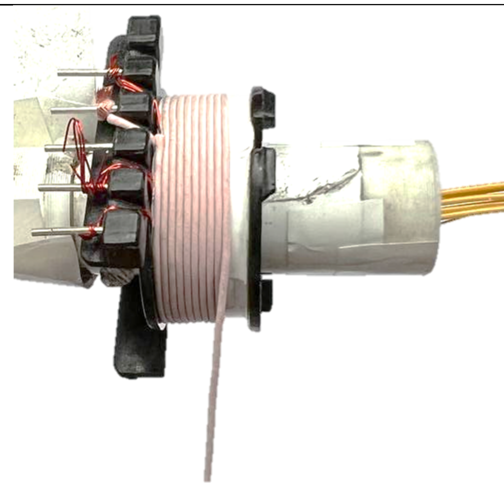
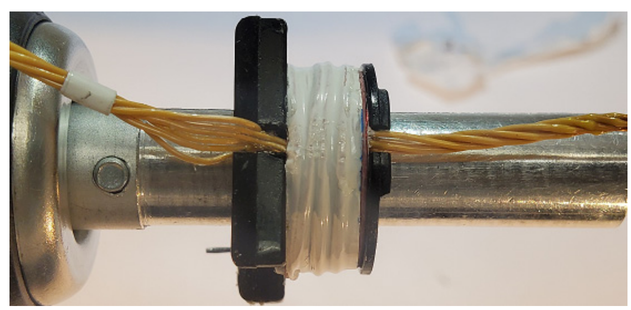
Apply 2 layer of polyester tape, Item [9] for insulation	
Winding 6 - Shield 2 Use magnetic wire, Item [7] - AWG#35. Prepare 4 wires (quadrifilar). Start at Pin 2 and wind 10 turns evenly from left to right for 1 layer.	 

<table>
<tr><td>Finish the winding at the right side of the bobbin and cut the wire as shown in the figure.

Apply 2 layer of polyester tape, Item [9] for insulation</td><td></td></tr>
<tr><td>Winding 7 - 2nd Primary

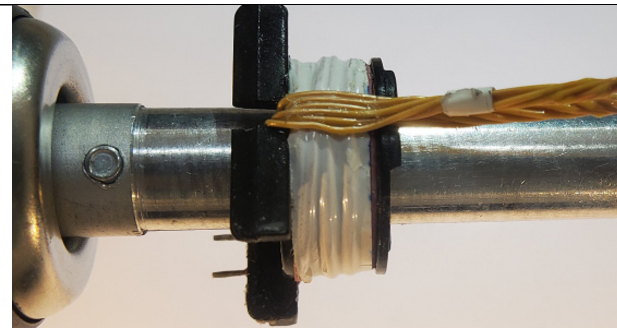
Use the remaining wires set aside from winding 1. Wind 9 turns from left to right with no gaps in between as shown in the figure.

Finish the winding on Pin 2.

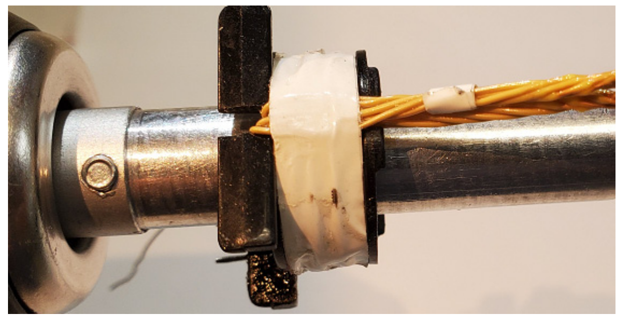
Apply 1 layer of polyester tape, Item [9] for insulation</td><td>
</td></tr>
</table>

Secondary Wire

Fold the secondary fly lead wires (FL1) from left to right as shown in the figure.

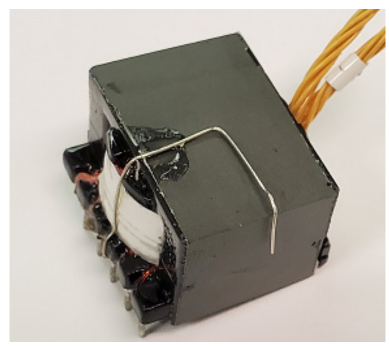


Apply 2 layer of polyester tape, Item [9] for insulation

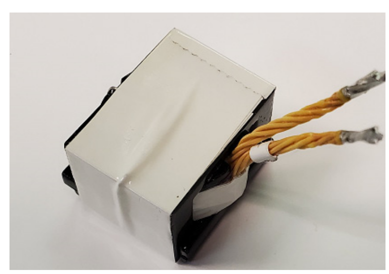


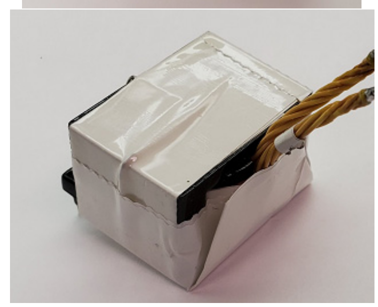
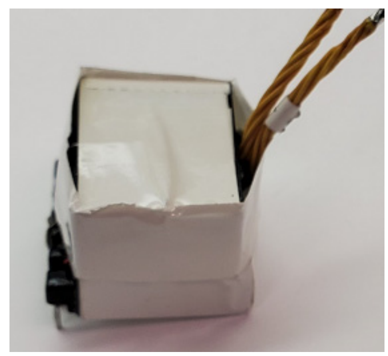
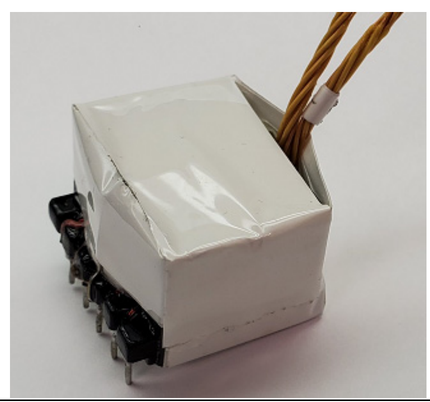
Core Fixing and Varnishing

Prepare a AWG # 28 TIN wire, Item [8]. Terminate the wire on Pin 4 and lay it out on top of the core as shown in the figure.



Fix top and bottom core together with the TIN wire with tape, Item [10]



Safety Insulation Tape Add double layer safety Insulation tapes as shown in the figures.	   

8 Transformer (T1) Spreadsheet

1	**ACDC_InnoSwitch4-CZ_USBPD_Flyback_021722; Rev.3.1; Copyright Power Integrations 2022**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch4-CZ USB-PD Flyback Design Spreadsheet**
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	180		180	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			HIGH LINE		Input voltage range
7	FLINE	50		50	Hz	AC Input voltage frequency
8	CAP_INPUT			70.0	uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	3.500		3.500	A	Output current 1
13	POUT1			70.00	W	Output power 1
14	EFFICIENCY1	0.95		0.95		Converter efficiency for output 1
15	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
18	**SET-POINT 2**					
19	VOUT2	15.00		15.00	V	Output voltage 2
20	IOUT2	4.000		4.000	A	Output current 2
21	POUT2			60.00	W	Output power 2
22	EFFICIENCY2	0.89		0.89		Converter efficiency for output 2
23	Z_FACTOR2	0.50		0.50		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
26	**SET-POINT 3**					
27	VOUT3	9.00		9.00	V	Output voltage 3
28	IOUT3	5.000		5.000	A	Output current 3
29	POUT3			45.00	W	Output power 3
30	EFFICIENCY3	0.89		0.89		Converter efficiency for output 3
31	Z_FACTOR3	0.50		0.50		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
34	**SET-POINT 4**					
35	VOUT4	5.00		5.00	V	Output voltage 4
36	IOUT4	6.500		6.500	A	Output current 4
37	POUT4			32.50	W	Output power 4
38	EFFICIENCY4	0.89		0.89		Converter efficiency for output 4
39	Z_FACTOR4	0.50		0.50		Z-factor for output 4
40	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
82	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at full load
86	**PRIMARY CONTROLLER SELECTION**					
87	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure

88	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
89	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
90	DEVICE_GENERIC	INN4074		INN4074		Device selection
91	DEVICE_CODE			INN4074C		Device code
92	PDEVICE_MAX			85	W	Device maximum power capability
93	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.953	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.100	A	Primary switch typical current limit
96	ILIMIT_MAX			2.247	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.20	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			588.31	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	82000		82000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
104	VOR	165.0		165.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			219.28	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.873		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.346		Primary switch duty cycle
109	TIME_ON			5.10	us	Primary switch on-time
110	TIME_OFF			7.51	us	Primary switch off-time
111	LPRIMARY_MIN			479.0	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			504.2	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			529.4	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.328	A	Primary switch average current
118	IPEAK_PRIMARY			2.136	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.218	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.136	A	Primary switch ripple current
121	IRMS_PRIMARY			0.683	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			17.620	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			1.801	A	Secondary winding pedestal current
126	IRMS_SECONDARY			8.465	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			5.804	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	EQ25		EQ25		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
134	CORE NAME			EQ25-3C95		Core code
135	AE			100.0	mm^2	Core cross sectional area

136	LE			41.4	mm	Core magnetic path length
137	AL			5710	nH	Ungapped core effective inductance per turns squared
138	VE			4145	mm^3	Core volume
139	BOBBIN NAME			TBI-235-01091.1206		Bobbin name
140	AW			34.8	mm^2	Bobbin window area
141	BW			8.10	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	**PRIMARY WINDING**					
145	NPRIMARY			33		Primary winding number of turns
146	BPEAK			3759	Gauss	Peak flux density
147	BMAX			3385	Gauss	Maximum flux density
148	BAC			1693	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			463	nH	Typical gapped core effective inductance per turns squared
150	LG			0.249	mm	Core gap length
152	**PRIMARY BIAS WINDING**					
153	NBIAS_PRIMARY			8		Primary bias winding number of turns
155	**SECONDARY WINDING**					
156	NSECONDARY	4		4		Secondary winding number of turns
158	**SECONDARY BIAS WINDING**					
159	NBIAS_SECONDARY			2		Secondary bias winding number of turns
162	**PRIMARY COMPONENTS SELECTION**					
163	**CLAMPZERO**					
164	LLEAK			5.04	uH	Primary winding leakage inductance
165	CCLAMP			100.0	nF	Primary clamp capacitor
166	RD_CLAMPZERO	30		30	kΩ	HSD resistor
167	TLLDL/THLDL			430.0	ns	HSD resistor programmed delay
168	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			375.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
169	TIME_VDS_VALLEY			46.3	ns	Time taken by the VDS ring to reach its first valley
170	IPEAK_CLAMPZERO			2.087	A	Active clamp peak current
172	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
173	BROWN-IN REQURED	70.00		70.00	V	Required AC RMS/DC line brown-in threshold
174	RLS			3.48	MΩ	Connect two 1.74 MOhm resistors to the V-pin for the required UV/OV threshold
175	BROWN-IN ACTUAL			69.80	V	Actual AC RMS/DC brown-in threshold using standard resistors
176	BROWN-OUT ACTUAL			63.13	V	Actual AC RMS/DC brown-out threshold using standard resistors
177	OVERVOLTAGE_LINE			290.83	V	Actual AC RMS/DC line over-voltage threshold
179	**PRIMARY BIAS WINDING**					
180	VBIAS_PRIMARY			9.00	V	Rectified primary bias voltage at the cable-disconnect (5V) set-point
181	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop

182	VREVERSE_BIASDIODE_PRIMARY			130.50	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
184	CBPP			0.47	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					
190	VDRAIN_OFF_SRFET			65.43	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AUTO		SIR804DP		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			10.3	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
195	**SECONDARY BIAS WINDING**					
196	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
197	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load
198	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
199	VREVERSE_BIASDIODE_SECONDARY			73.87	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
200	CBIAS_SECONDARY			10	uF	Secondary bias winding rectification capacitor
201	CBPS			2.20	uF	BPS pin capacitor

9 Performance Data

All measurements were performed at room ambient temperature otherwise specified.
Please refer to below output voltage selector guide when changing output voltage.

Output Voltage Selector Guide

V_{OUT} = 5 V – All 3 shorting pads are open

V_{OUT} = 9 V – Short 9 V pad to GND

V_{OUT} = 15 V – Short 15 V pad to GND

V_{OUT} = 20 V – Short 20 V pad to GND

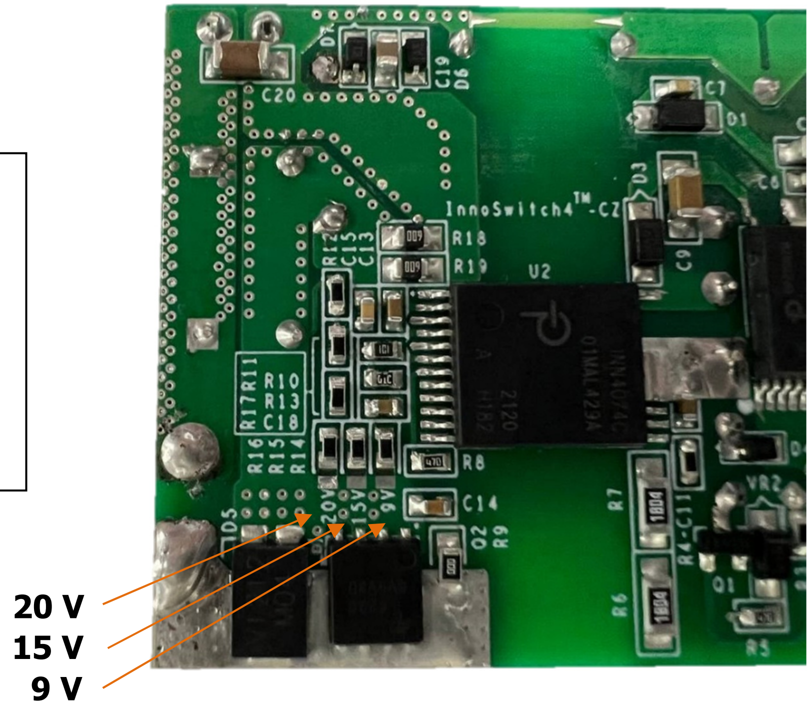


Figure 9 – Output Voltage Selector Guide.

9.1 System Full Load Efficiency

Output voltage was measured at PCB output terminal pin
Note: Unit tested with 15 mins soak time and 3 min soak time every input line.

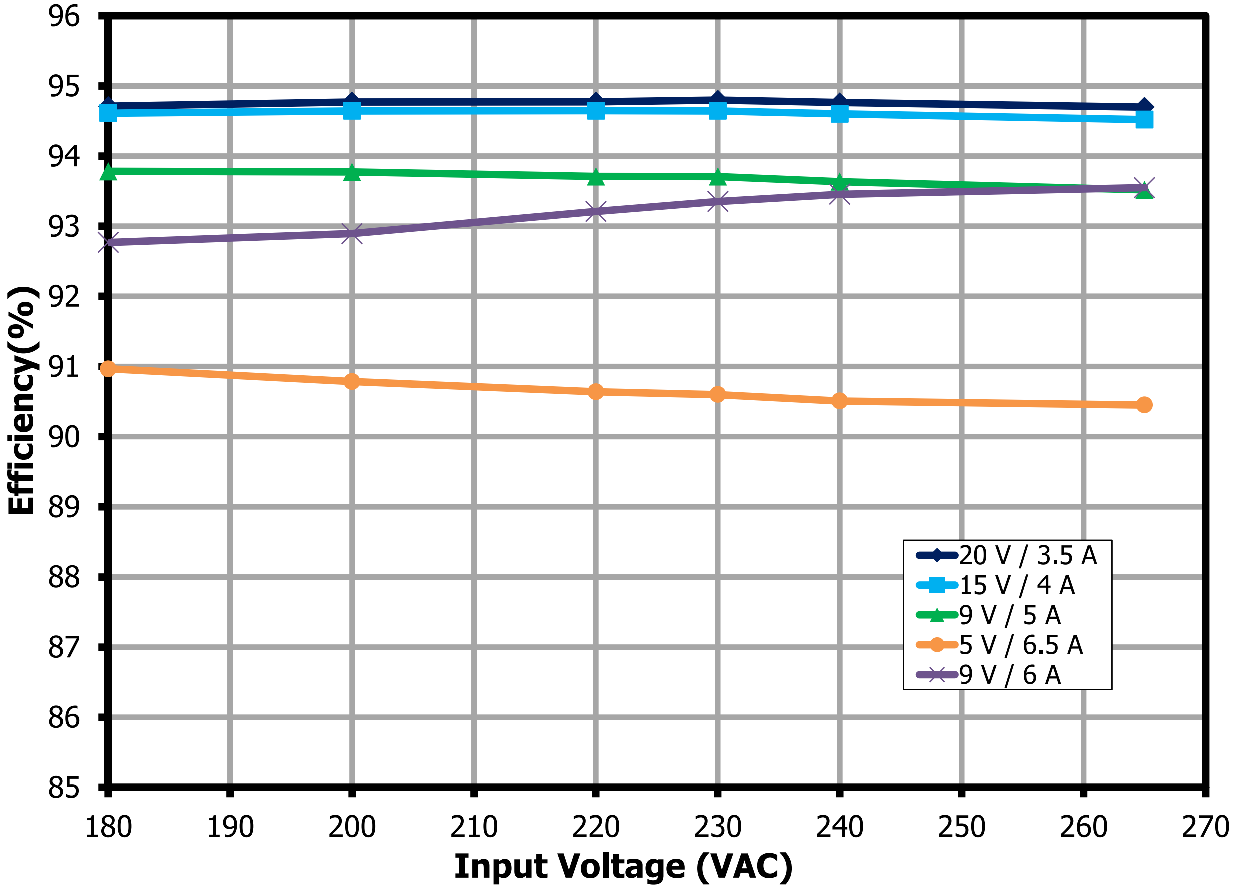


Figure 10 – System Full Load Efficiency vs. Line.

9.2 Energy Efficiency

9.2.1 System Average Efficiency

Note: Unit tested with 10 mins soak time and 3 min soak time per load step.

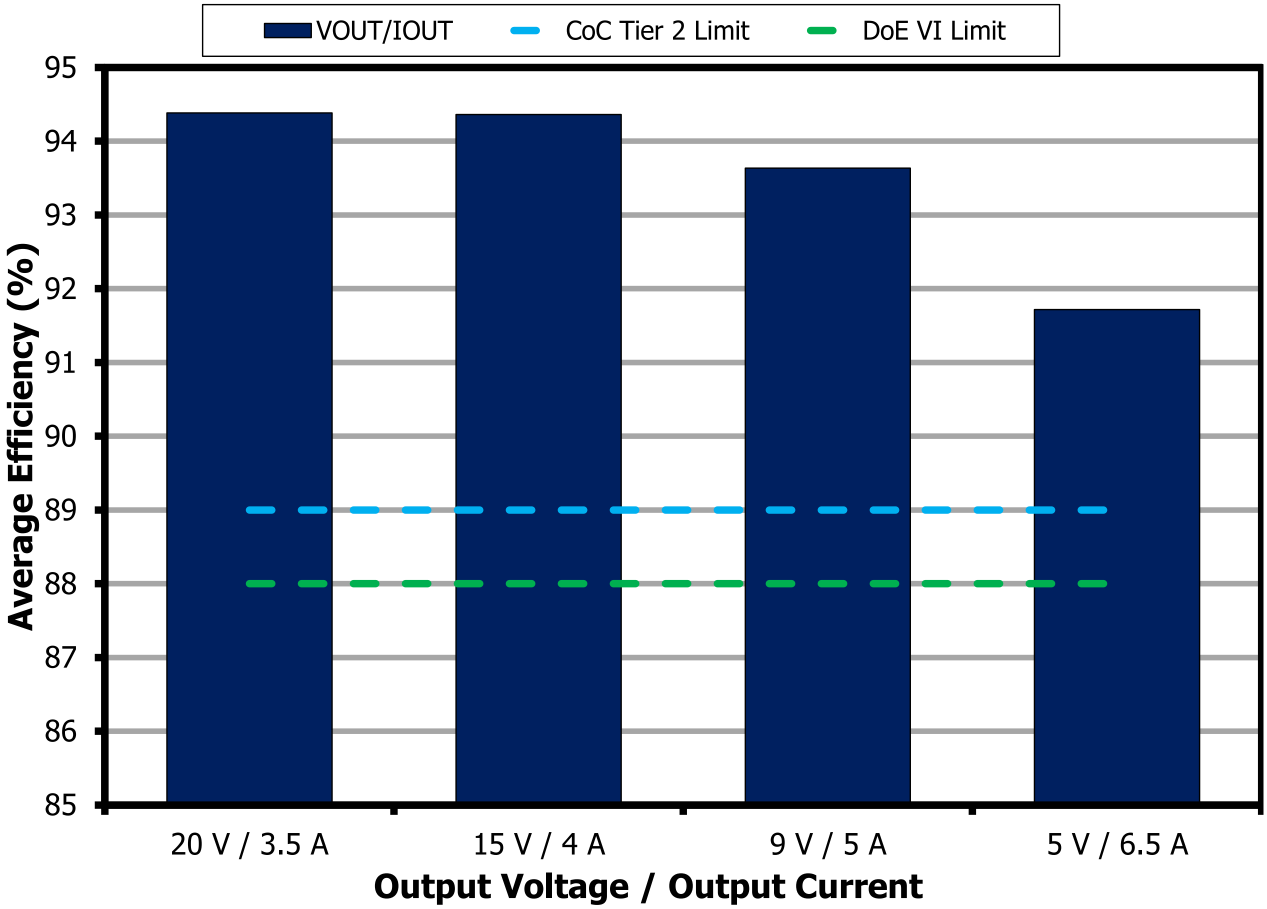


Figure 11 – Average Efficiency at 230 VAC 50 Hz.

9.2.2 Efficiency at 10% Load

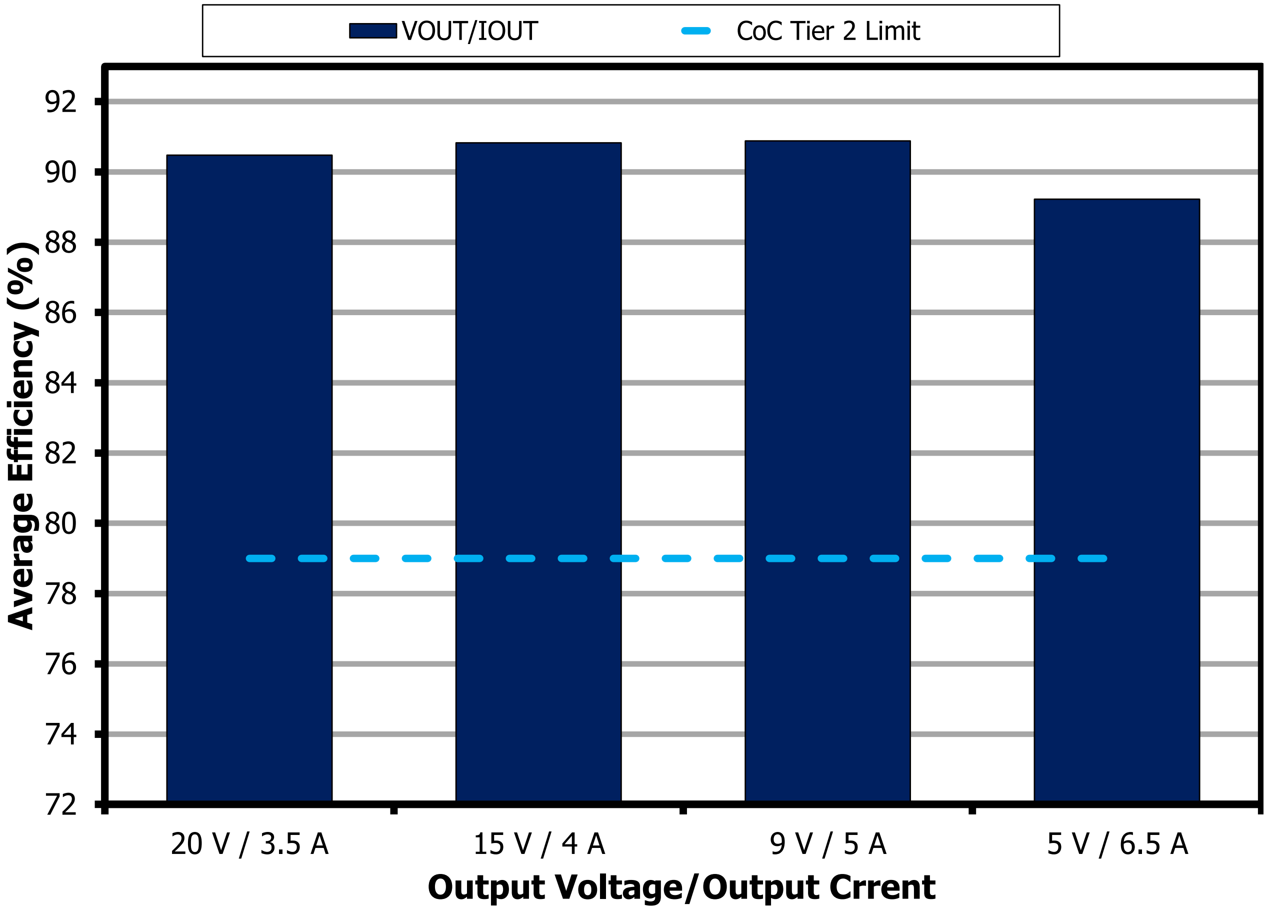


Figure 12 – Efficiency at 10 % Load, 230 VAC 50 Hz.

9.3 Efficiency vs. Load

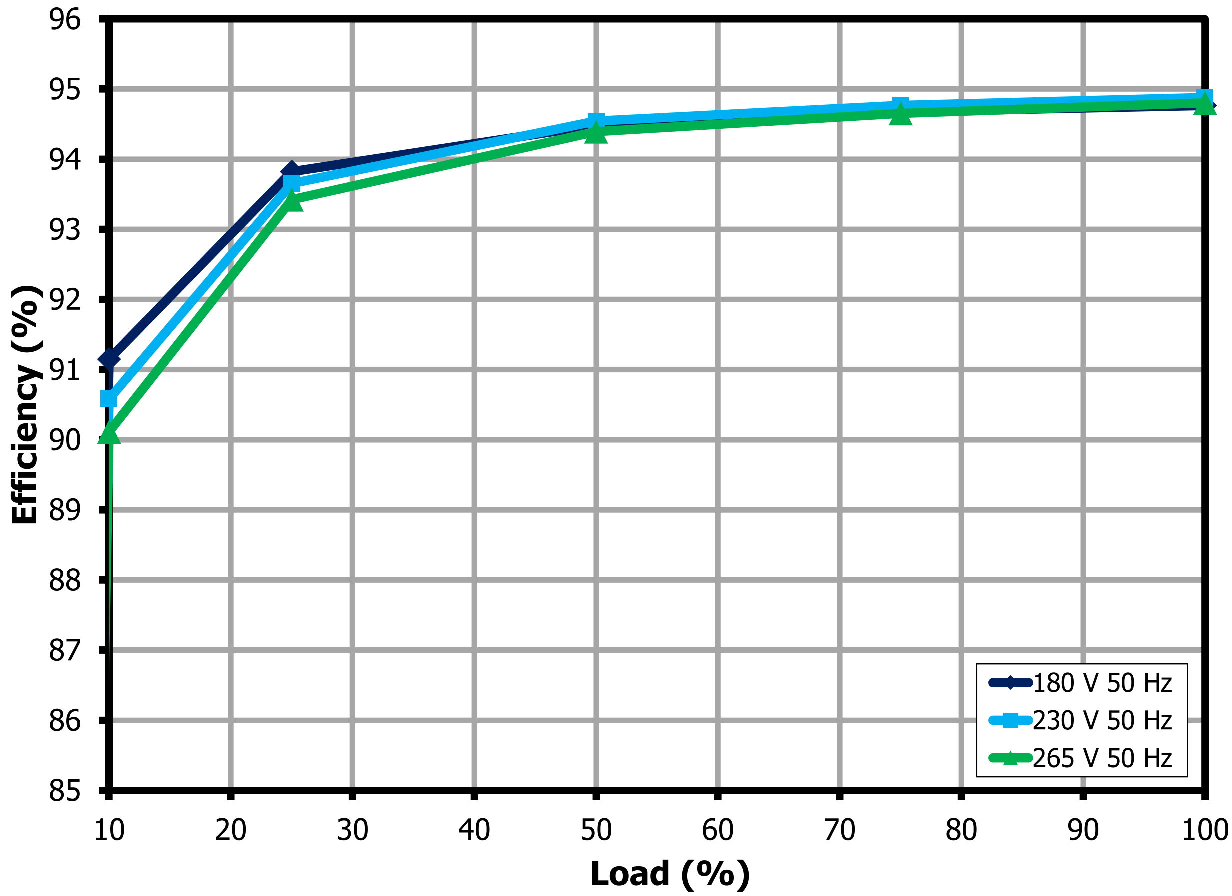


Figure 13 – System Efficiency vs. Load at V_{OUT} = 20 VDC.

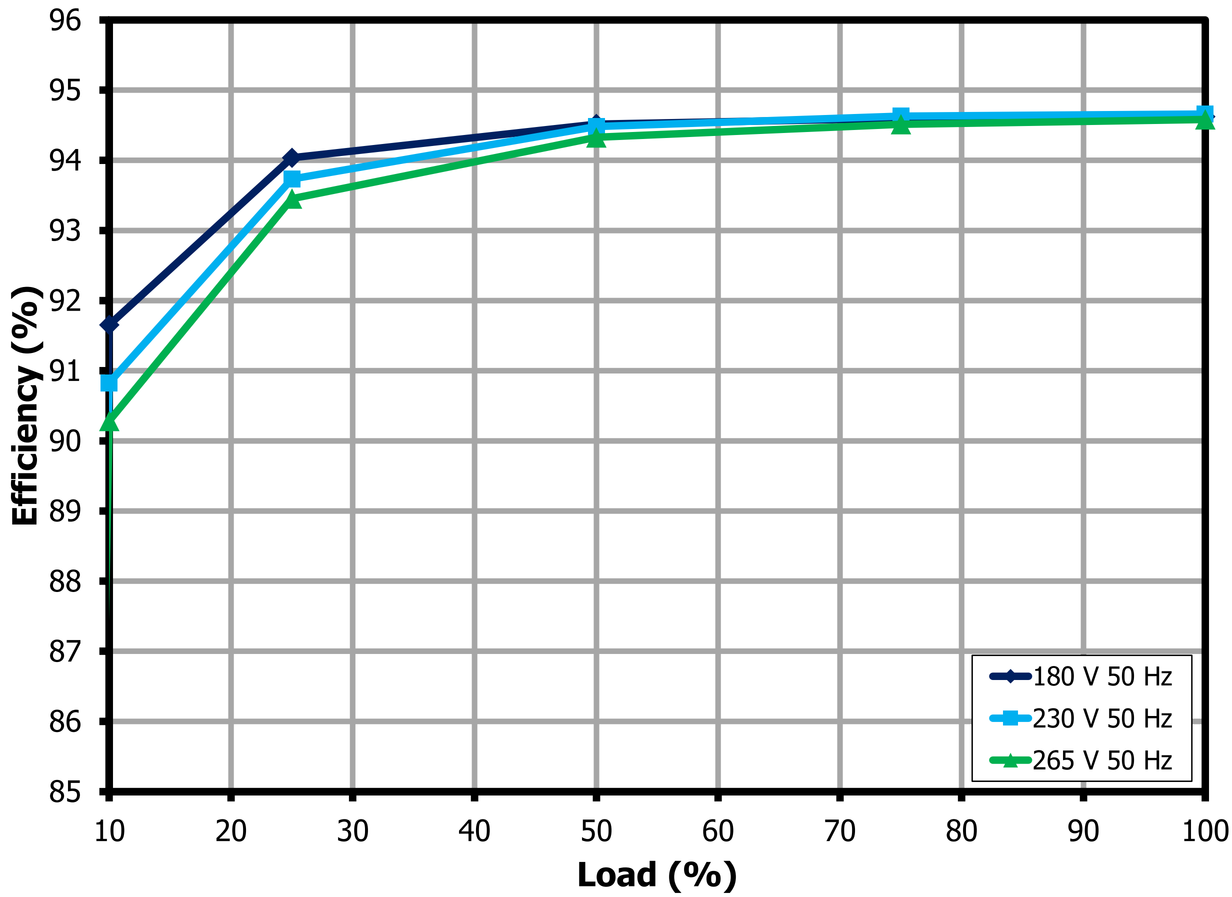


Figure 14 – System Efficiency vs. Load at V_{OUT} = 15 VDC.

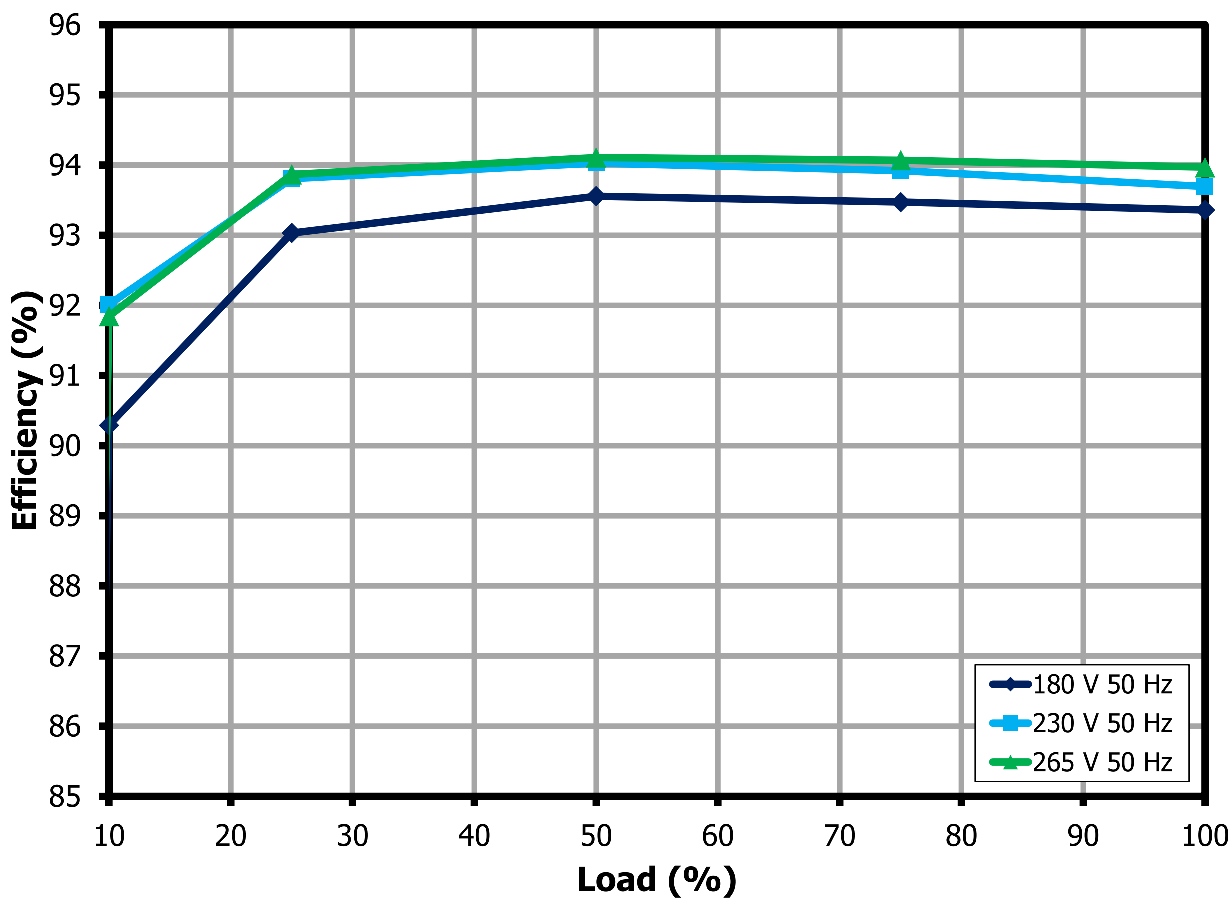


Figure 15 – System Efficiency vs. Load at V_{OUT} = 9 VDC.

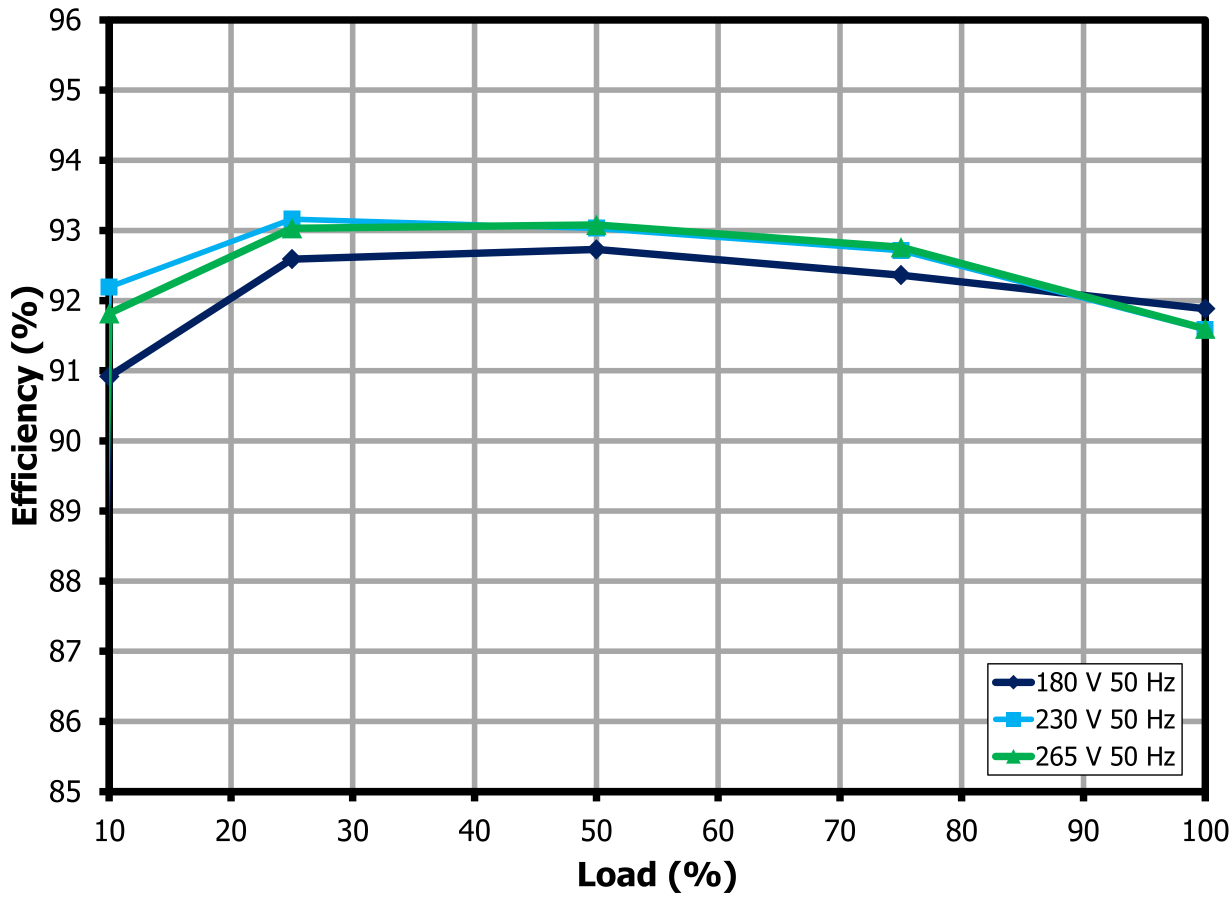


Figure 16 – System Efficiency vs. Load at V_{OUT} = 5 VDC.

9.4 No-Load Input Power

Note: Tested at V_{OUT} = 5 V, with 30 seconds soak time every input line.

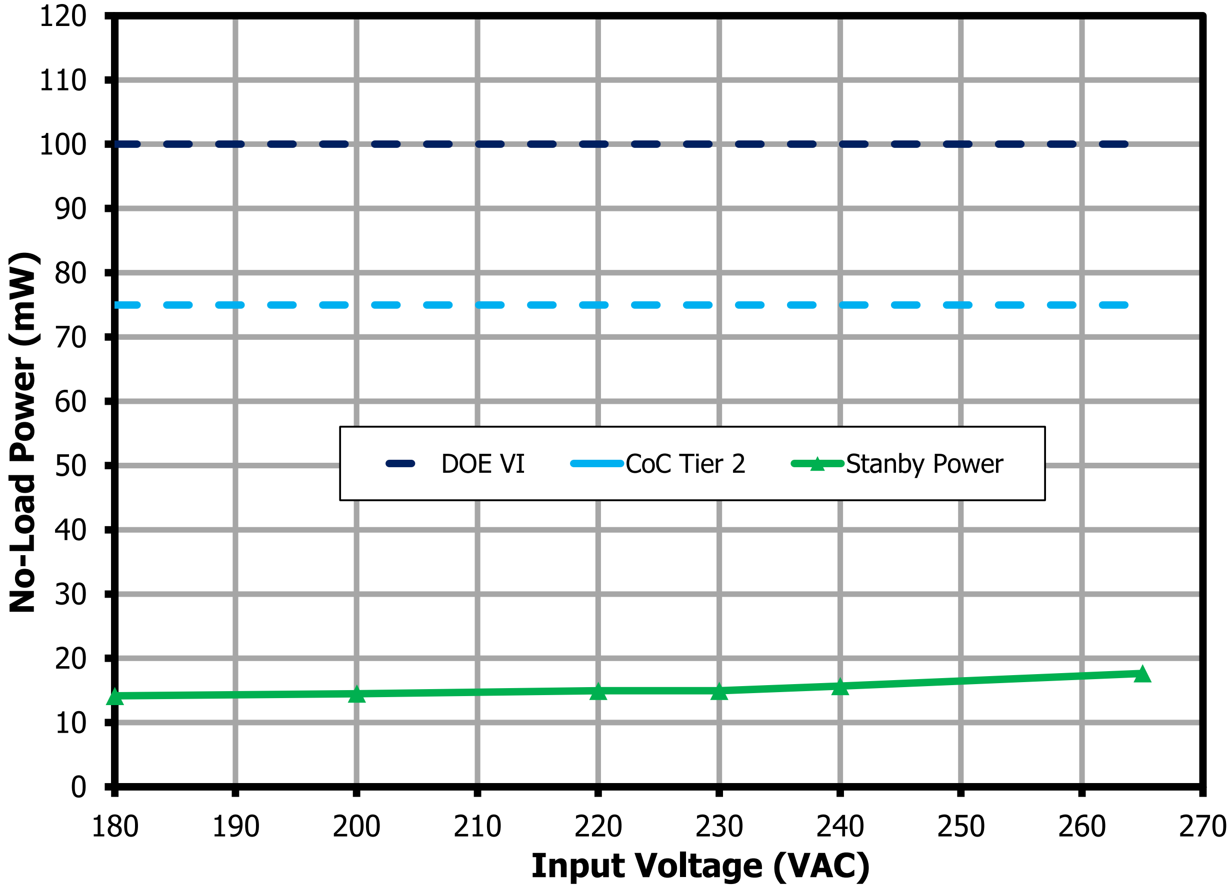


Figure 17 – No-Load Input Power vs. Line at V_{OUT} = 5 V.

9.5 Output Voltage Load Regulation

E-load is set at CC Mode Load

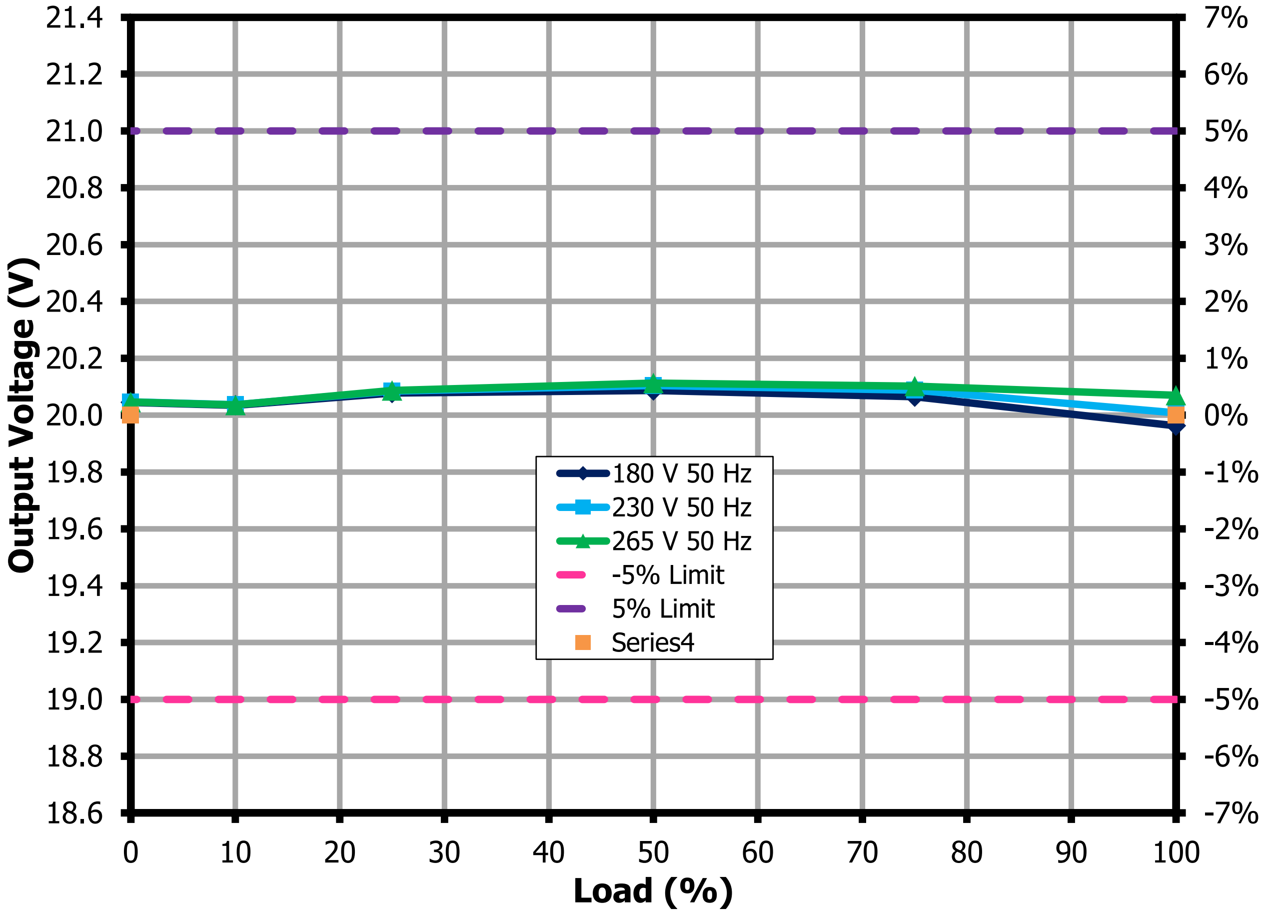


Figure 18 – Voltage Regulation vs. Load at V_{OUT} = 20 VDC / 3.5 A.

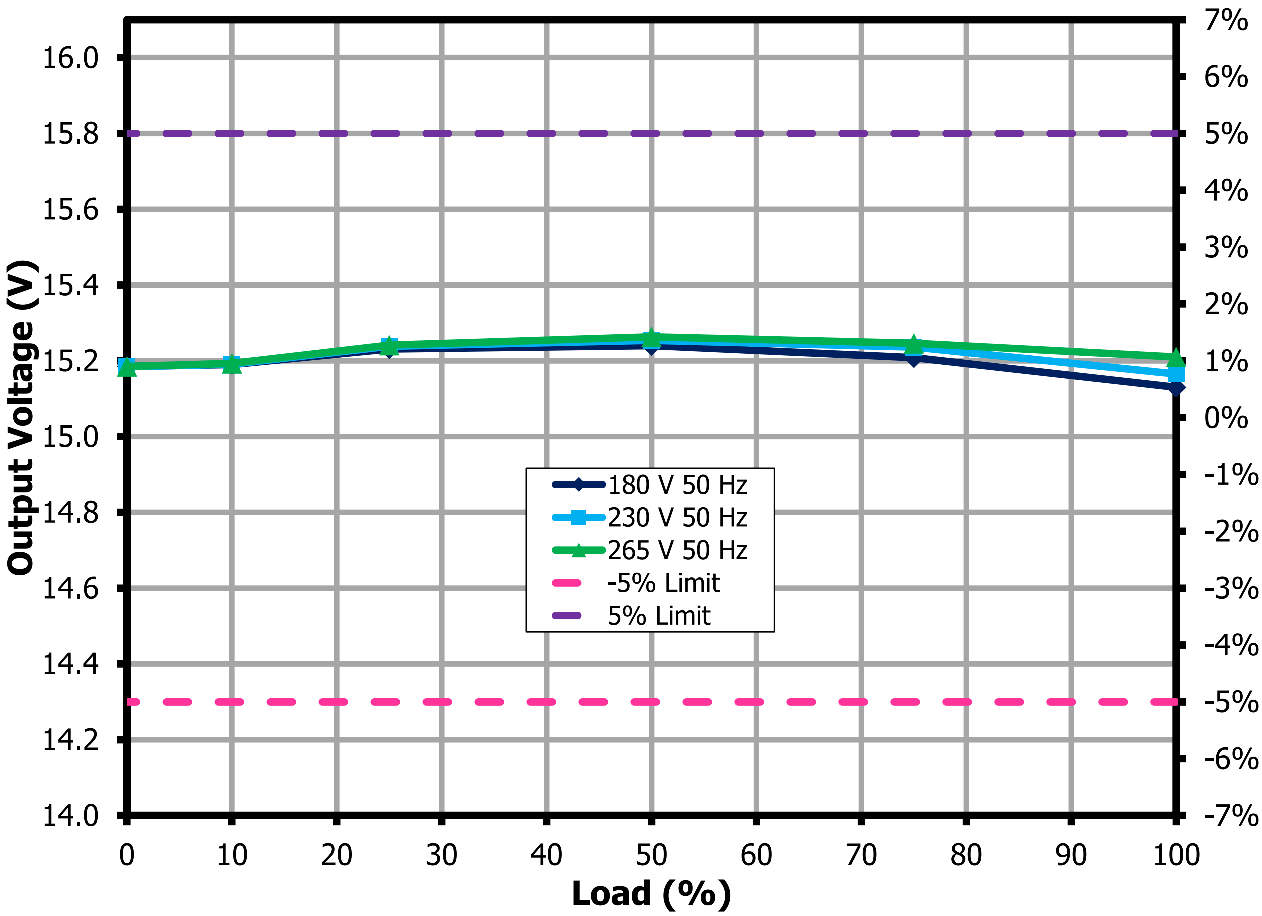


Figure 19 – Voltage Regulation vs. Load at V_{OUT} = 15 VDC / 4 A.

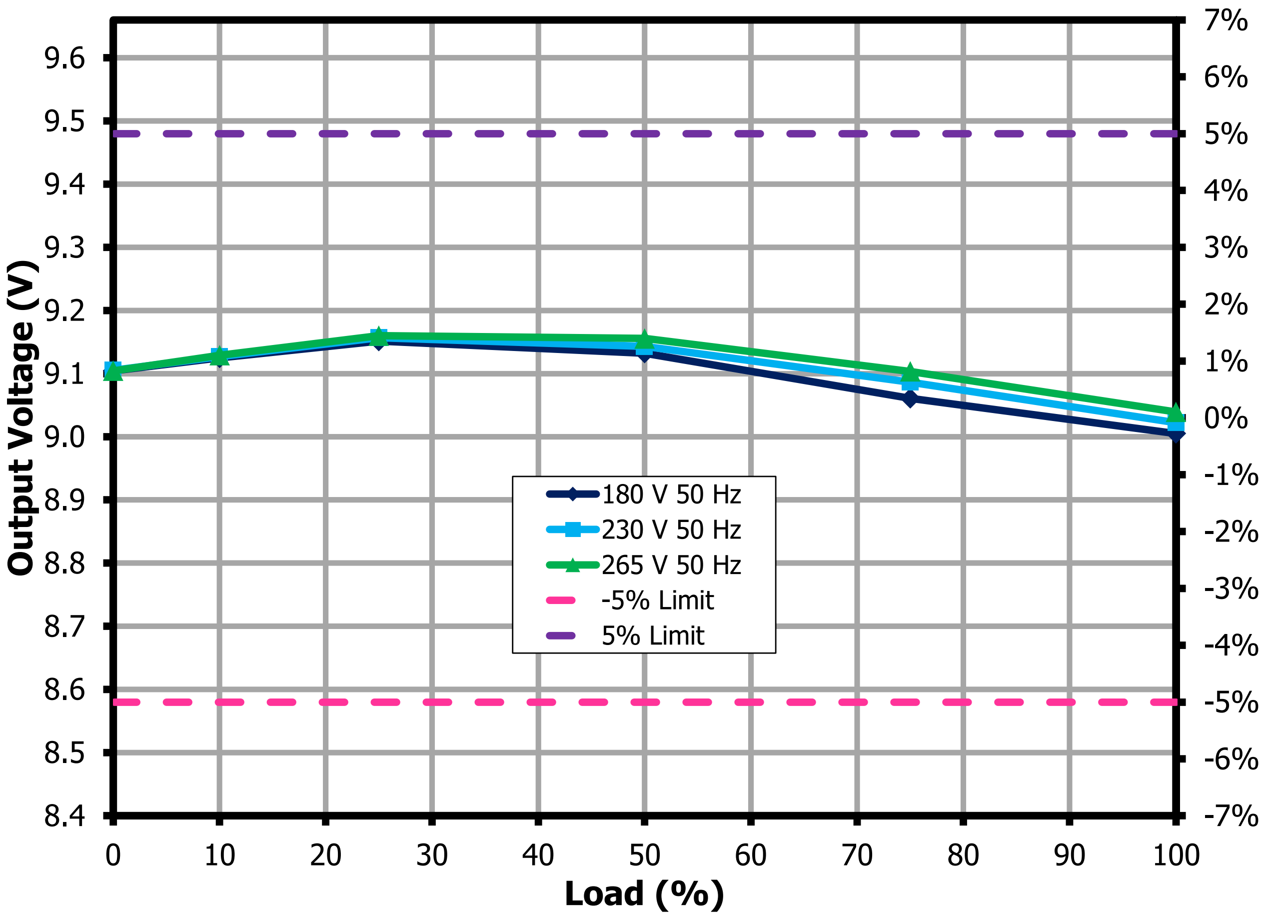


Figure 20 – Voltage Regulation vs. Load at V_{OUT} = 9 VDC / 5 A.

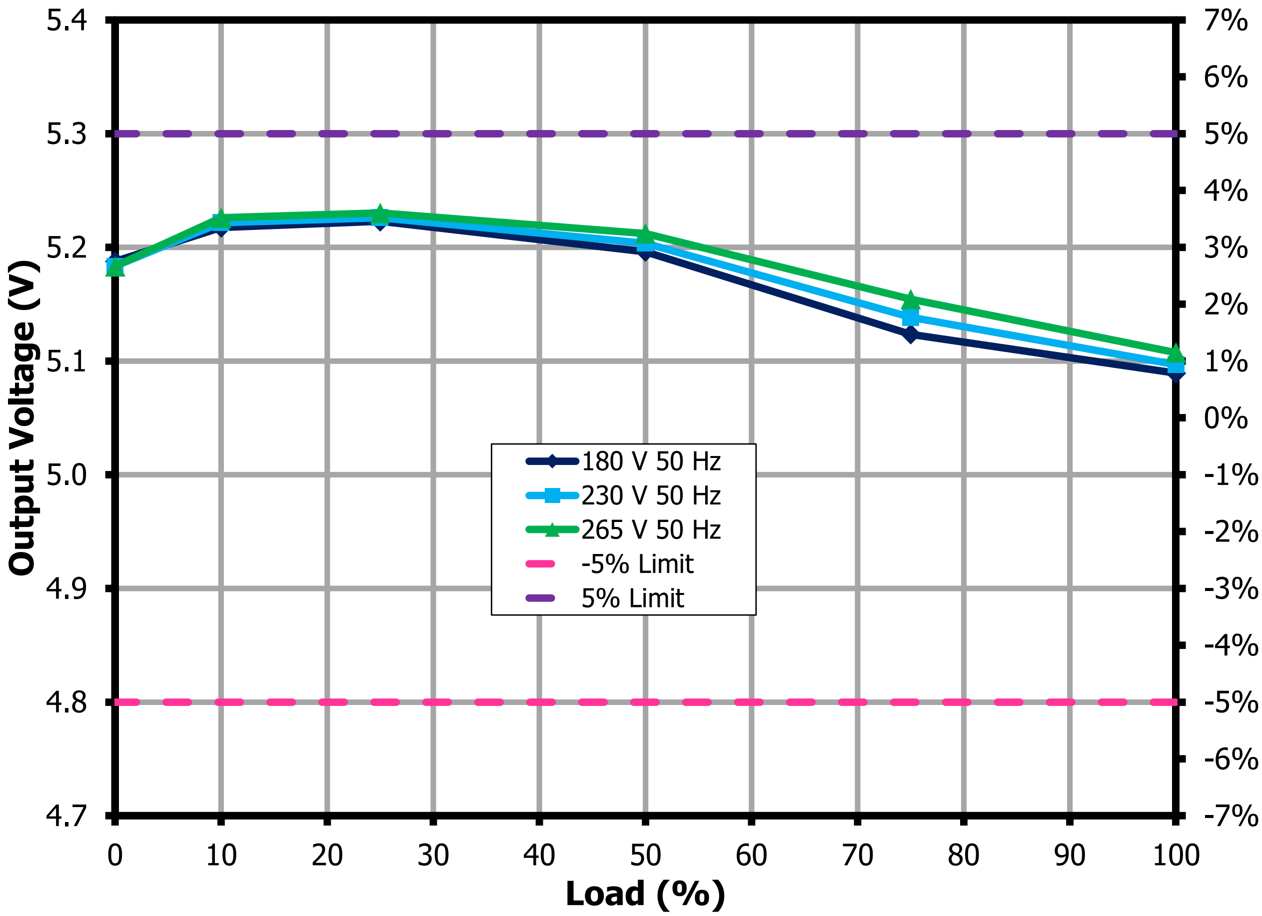


Figure 21 – Voltage Regulation vs. Load at V_{OUT} = 5 VDC / 6.5 A.

9.6 Test Data

9.6.1 Electrical Test Data at Full Load

	Input Setting		Input Measurement			Load Measurement			Efficiency (%)
	Voltage (Vac)	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
20 V / 3.5 A	180	50	179.92	881.60	73.72	19.95	3499.50	69.82	94.71
	200	50	200.00	835.50	73.83	19.99	3499.60	69.97	94.77
	220	50	219.99	792.50	73.84	20.00	3499.70	69.98	94.77
	230	50	230.01	740.50	73.83	20.00	3499.90	69.99	94.80
	240	50	240.07	760.20	73.90	20.01	3499.80	70.03	94.76
	265	50	265.05	738.90	74.13	20.06	3499.90	70.20	94.70
	Input Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	Voltage (Vac)	**Freq (Hz)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**V_{OUT} (V_{DC})**	**I_{OUT} (mA_{DC})**	**P_{OUT} (W)**	
15 V / 4 A	180	50	179.95	785.50	63.73	15.08	3999.10	60.30	94.61
	200	50	200.01	740.40	63.80	15.10	3999.00	60.38	94.64
	220	50	220.01	704.40	63.83	15.11	3999.00	60.41	94.65
	230	50	230.02	659.10	63.85	15.11	3999.00	60.43	94.65
	240	50	240.08	678.80	63.93	15.12	3999.00	60.48	94.60
	265	50	265.06	660.60	64.12	15.16	3999.00	60.61	94.52
	Input Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	Voltage (Vac)	**Freq (Hz)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**V_{OUT} (V_{DC})**	**I_{OUT} (mA_{DC})**	**P_{OUT} (W)**	
9 V / 5 A	180	50	179.97	620.30	47.69	8.95	4999.50	44.73	93.78
	200	50	200.04	589.30	47.77	8.96	4999.50	44.80	93.77
	220	50	220.03	566.00	47.89	8.98	4999.40	44.88	93.71
	230	50	230.05	523.80	47.91	8.98	4999.50	44.90	93.71
	240	50	240.11	548.60	47.97	8.98	4999.50	44.92	93.64
	265	50	265.09	527.00	48.08	8.99	4999.50	44.96	93.52
	Input Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	Voltage (Vac)	**Freq (Hz)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**V_{OUT} (V_{DC})**	**I_{OUT} (mA_{DC})**	**P_{OUT} (W)**	
5 V / 6.5 A	180	50	179.99	502.00	35.88	5.02	6499.70	32.64	90.97
	200	50	200.07	482.60	36.01	5.03	6499.70	32.69	90.79
	220	50	220.05	465.60	36.12	5.04	6499.70	32.74	90.64
	230	50	230.07	427.10	36.16	5.04	6499.70	32.76	90.60
	240	50	240.12	444.60	36.22	5.04	6499.80	32.78	90.51
	265	50	265.10	411.80	36.30	5.05	6499.80	32.83	90.45

9.6.2 Energy Efficiency Test Data

	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
20 V /3.5 A	100	3500	230.03	739.40	73.82	20.00	3499.10	69.98	94.80
	75	2625	230.05	592.60	55.66	20.08	2624.30	52.69	94.66
	50	1750	230.07	434.80	37.22	20.10	1749.30	35.16	94.47
	25	875	230.09	257.30	18.75	20.08	873.90	17.55	93.61
	10	350	230.10	117.84	7.74	20.03	349.50	7.00	90.48
	Average Efficiency at 20 V								**94.38**
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
15 V / 4 A	100	4000	230.04	660.30	63.86	15.11	3999.20	60.45	94.65
	75	3000	230.06	528.30	48.14	15.19	2999.20	45.55	94.61
	50	2000	230.08	391.20	32.18	15.21	1999.10	30.40	94.45
	25	1000	230.10	227.64	16.19	15.19	999.10	15.18	93.73
	10	400	230.11	103.46	6.66	15.14	399.50	6.05	90.83
	Average Efficiency at 15 V								**94.34**
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
9 V / 5 A	100	5000	230.06	525.00	47.89	8.98	4999.40	44.91	93.77
	75	3750	230.07	424.40	36.12	9.04	3749.50	33.89	93.83
	50	2500	230.08	315.00	24.17	9.07	2499.20	22.66	93.76
	25	1250	230.10	176.14	12.15	9.06	1249.50	11.32	93.18
	10	500	230.09	76.99	4.97	9.03	499.90	4.52	90.88
	Average Efficiency at 9 V								**93.63**
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
5 V / 6.5 A	100	6500	230.07	427.20	36.14	5.04	6500.00	32.76	90.65
	75	4875	230.08	344.80	26.96	5.09	4875.00	24.83	92.10
	50	3250	230.09	250.70	18.07	5.14	3250.00	16.69	92.36
	25	1625	230.10	136.53	9.10	5.14	1624.30	8.35	91.75
	10	650	230.10	60.73	3.74	5.14	649.30	3.34	89.22
	Average Efficiency at 5 V								**91.71**

9.6.3 Electrical Test Data at 20 V / 3.5 A

	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
180 V 50 Hz	100	3500	179.91	876.20	73.71	19.96	3499.00	69.85	94.76
	75	2625	179.93	701.20	55.61	20.07	2624.10	52.65	94.68
	50	1750	179.96	508.80	37.18	20.09	1749.00	35.13	94.49
	25	875	180.00	299.30	18.70	20.08	873.90	17.55	93.82
	10	350	180.02	137.18	7.68	20.04	349.50	7.00	91.15
	0	0	180.04	13.86	0.12	20.05	0	0	0.00
	Load Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	% Load	**Load (A)**	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
230 V 50 Hz	100	3500	230.01	737.70	73.79	20.01	3499.20	70.01	94.88
	75	2625	230.03	591.10	55.63	20.09	2624.20	52.72	94.77
	50	1750	230.05	433.40	37.20	20.10	1749.20	35.17	94.54
	25	875	230.08	256.60	18.74	20.09	873.90	17.55	93.66
	10	350	230.09	117.77	7.73	20.04	349.50	7.00	90.58
	0	0	230.10	14.86	0.14	20.05	0	0	0.00
	Load Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	% Load	**Load (A)**	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
265 V 50 Hz	100	3500	265.05	735.40	74.08	20.07	3499.10	70.23	94.80
	75	2625	265.07	598.20	55.73	20.10	2624.20	52.75	94.65
	50	1750	265.09	421.60	37.27	20.11	1749.10	35.18	94.39
	25	875	265.11	226.61	18.79	20.09	873.90	17.55	93.42
	10	350	265.12	103.92	7.77	20.04	349.50	7.00	90.12
	0	0	265.13	16.46	0.15	20.05	0	0	0.00

9.6.4 Electrical Test Data at 15 V / 4 A

	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
180 V 50 Hz	100	4000	179.95	784.80	63.74	15.08	3999.30	60.31	94.62
	75	3000	179.97	628.30	48.06	15.16	2999.30	45.46	94.60
	50	2000	180.00	461.60	32.13	15.19	1999.20	30.37	94.52
	25	1000	180.03	267.00	16.13	15.18	999.10	15.17	94.04
	10	400	180.04	120.76	6.60	15.14	399.50	6.05	91.65
	0	0	180.05	13.81	0.09	15.14	0	0	0.00
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
230 V 50 Hz	100	4000	230.04	661.30	63.86	15.12	3999.20	60.45	94.66
	75	3000	230.06	529.10	48.13	15.19	2999.20	45.55	94.63
	50	2000	230.08	391.90	32.17	15.20	1999.10	30.39	94.48
	25	1000	230.10	228.08	16.19	15.19	999.10	15.18	93.73
	10	400	230.11	103.58	6.66	15.14	399.50	6.05	90.83
	0	0	230.11	14.29	0.11	15.13	0	0	0.00
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
265 V 50 Hz	100	4000	265.06	663.80	64.10	15.16	3999.20	60.63	94.58
	75	3000	265.08	530.40	48.22	15.20	2999.10	45.57	94.51
	50	2000	265.09	370.20	32.24	15.21	1999.00	30.41	94.33
	25	1000	265.11	198.51	16.24	15.19	999.00	15.18	93.45
	10	400	265.12	91.46	6.70	15.14	399.40	6.05	90.28
	0	0	265.12	16.37	0.12	15.14	0	0	0.00

9.6.5 Electrical Test Data at 9 V / 5 A

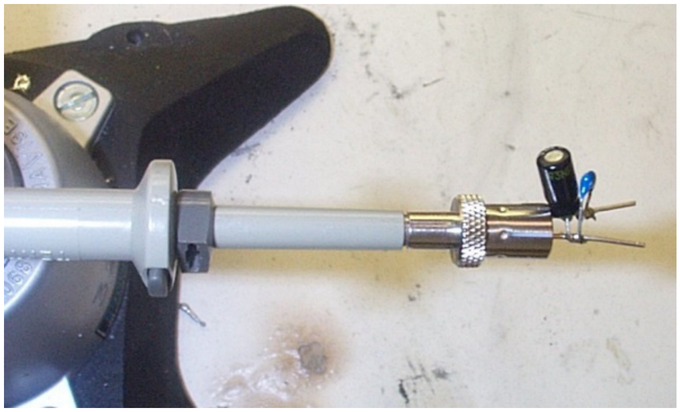
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
180 V 50 Hz	100	5000	99.96	940.10	48.06	8.98	4999.12	44.87	93.36
	75	3750	99.97	753.10	36.22	9.03	3748.88	33.86	93.47
	50	2500	99.98	554.30	24.31	9.10	2498.63	22.74	93.56
	25	1250	100.00	329.10	12.24	9.12	1248.38	11.39	93.03
	10	500	100.00	161.23	5.03	9.09	499.65	4.54	90.29
	0	0	100.01	20.81	0.060	9.07	0	0	0.00
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
230 V 50 Hz	100	5000	114.97	869.60	47.98	8.99	4999.12	44.95	93.69
	75	3750	114.98	699.50	36.15	9.06	3748.88	33.95	93.92
	50	2500	114.99	512.70	24.22	9.11	2499.00	22.77	94.03
	25	1250	115.00	308.50	12.15	9.13	1248.75	11.40	93.80
	10	500	115.01	142.58	4.94	9.10	499.65	4.55	92.01
	0	0	115.01	20.63	0.060	9.08	0	0	0.00
	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
265 V 50 Hz	100	5000	131.95	807.80	47.93	9.01	4999.12	45.04	93.97
	75	3750	131.96	649.90	36.16	9.07	3748.88	34.02	94.07
	50	2500	131.97	479.70	24.23	9.13	2498.63	22.80	94.11
	25	1250	131.98	284.90	12.15	9.13	1249.13	11.40	93.87
	10	500	131.98	128.37	4.95	9.10	499.65	4.55	91.85
	0	0	131.99	20.42	0.062	9.07	0	0	0.00

9.6.6 Electrical Test Data at 5 V / 6.5 A

	Load Setting		Input Measurement			Load Measurement			Efficiency (%)
	% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
180 V 50 Hz	100	6500	99.97	744.20	35.64	5.04	6498.45	32.75	91.88
	75	4875	99.98	596.80	26.77	5.07	4873.46	24.73	92.36
	50	3250	99.99	439.20	18.03	5.15	3248.85	16.72	92.73
	25	1625	100.00	264.00	9.07	5.17	1623.49	8.40	92.59
	10	650	100.00	122.44	3.69	5.17	648.87	3.35	90.92
	0	0	100.01	20.15	0.019	5.14	0	0	0.00
	Load Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	% Load	**Load (A)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**V_{OUT} (V_{DC})**	**I_{OUT} (mA_{DC})**	**P_{OUT} (W)**	
230 V 50 Hz	100	6500	114.98	693.80	35.81	5.05	6498.45	32.80	91.58
	75	4875	114.99	553.60	26.75	5.09	4873.84	24.80	92.71
	50	3250	115.00	410.10	18.00	5.15	3249.23	16.75	93.03
	25	1625	115.01	242.77	9.02	5.18	1623.49	8.40	93.16
	10	650	115.01	109.03	3.64	5.17	648.87	3.36	92.19
	0	0	115.01	20.09	0.021	5.13	0	0	0.00
	Load Setting		**Input Measurement**			**Load Measurement**			**Efficiency (%)**
	% Load	**Load (A)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**V_{OUT} (V_{DC})**	**I_{OUT} (mA_{DC})**	**P_{OUT} (W)**	
265 V 50 Hz	100	6500	131.96	645.50	35.88	5.06	6498.45	32.87	91.60
	75	4875	131.97	516.80	26.82	5.10	4873.84	24.88	92.76
	50	3250	131.97	388.20	18.02	5.16	3249.23	16.77	93.08
	25	1625	131.98	220.13	9.04	5.18	1623.49	8.41	93.03
	10	650	131.99	98.69	3.66	5.18	649.25	3.36	91.82
	0	0	131.99	19.99	0.023	5.13	0	0	0.00

9.7 Output Ripple Voltage

Set-up: Use x1 voltage probe with 2 capacitors (0.1 μF / 50 V ceramic and 47 μ F/ 50 V E-cap) connected across the probe tip and ground as shown below. Oscilloscope was set to AC coupling with frequency bandwidth of 20 MHz. Ripple voltage was measured at the end of 2-feet cable at room ambient temperature (25 ºC).



9.7.1 Output Ripple Voltage vs. Percent Load at 20 V / 3.5 A.

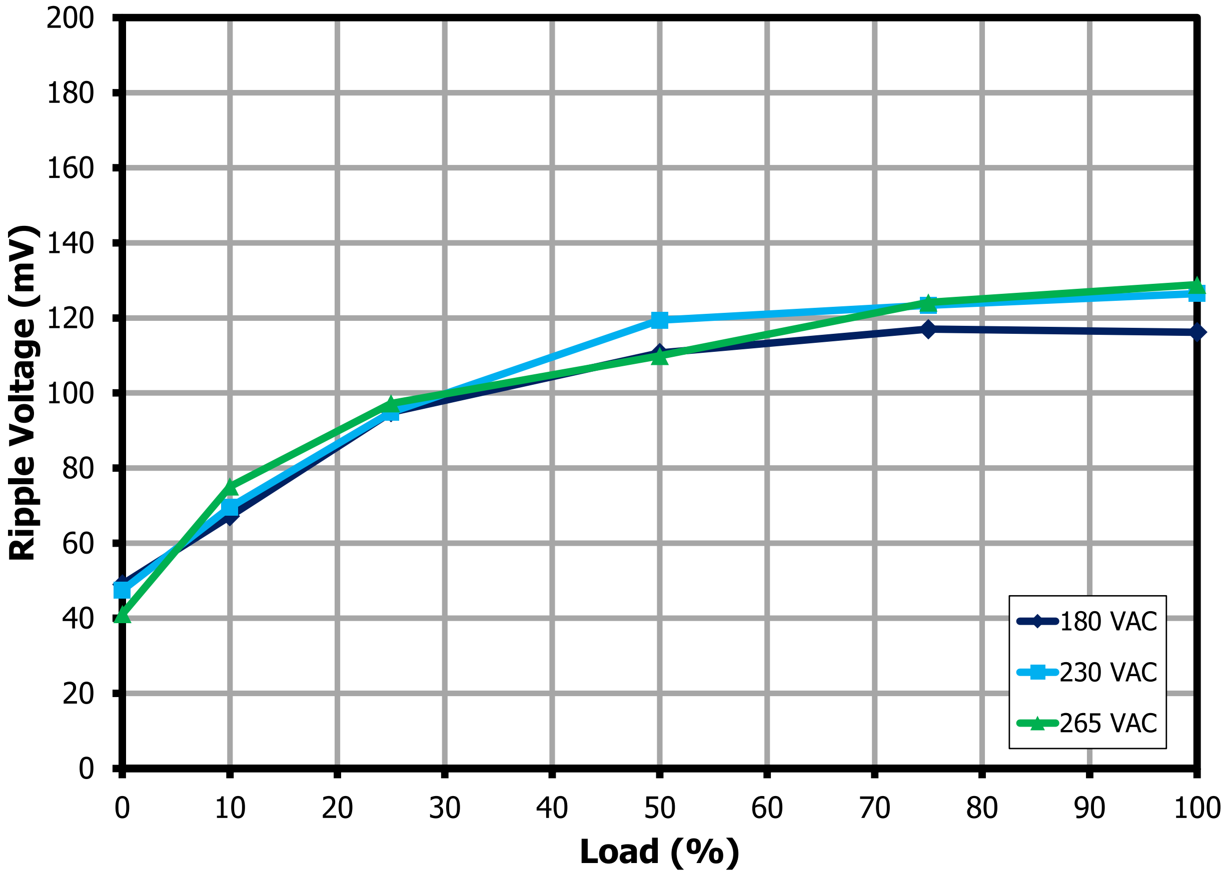


Figure 22 – Ripple Voltage vs. %Load at 20 V.

9.7.2 Output Ripple Voltage vs. Percent Load at 15 V / 4 A.

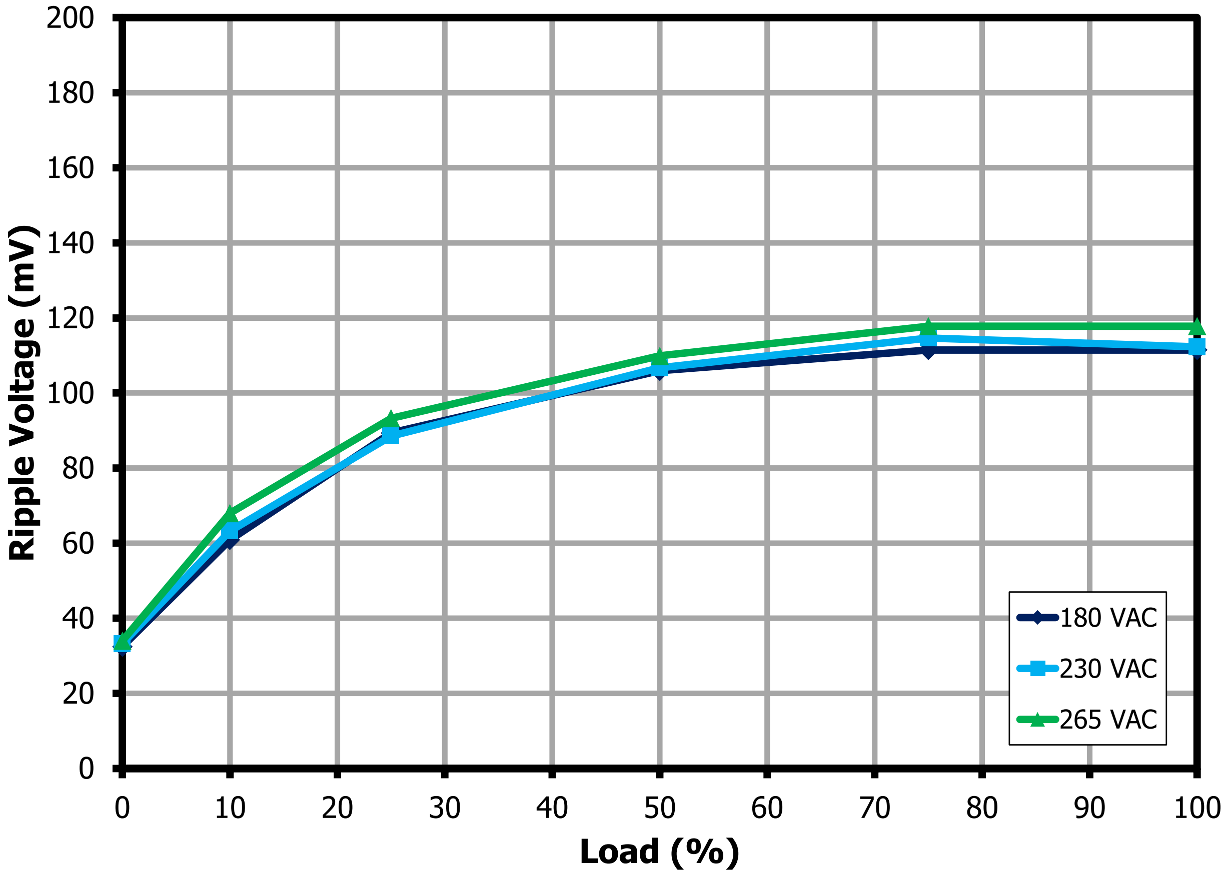


Figure 23 – Ripple Voltage vs. %Load at 15 V.

9.7.3 Output Ripple Voltage vs. Percent Load at 9 V / 5 A.

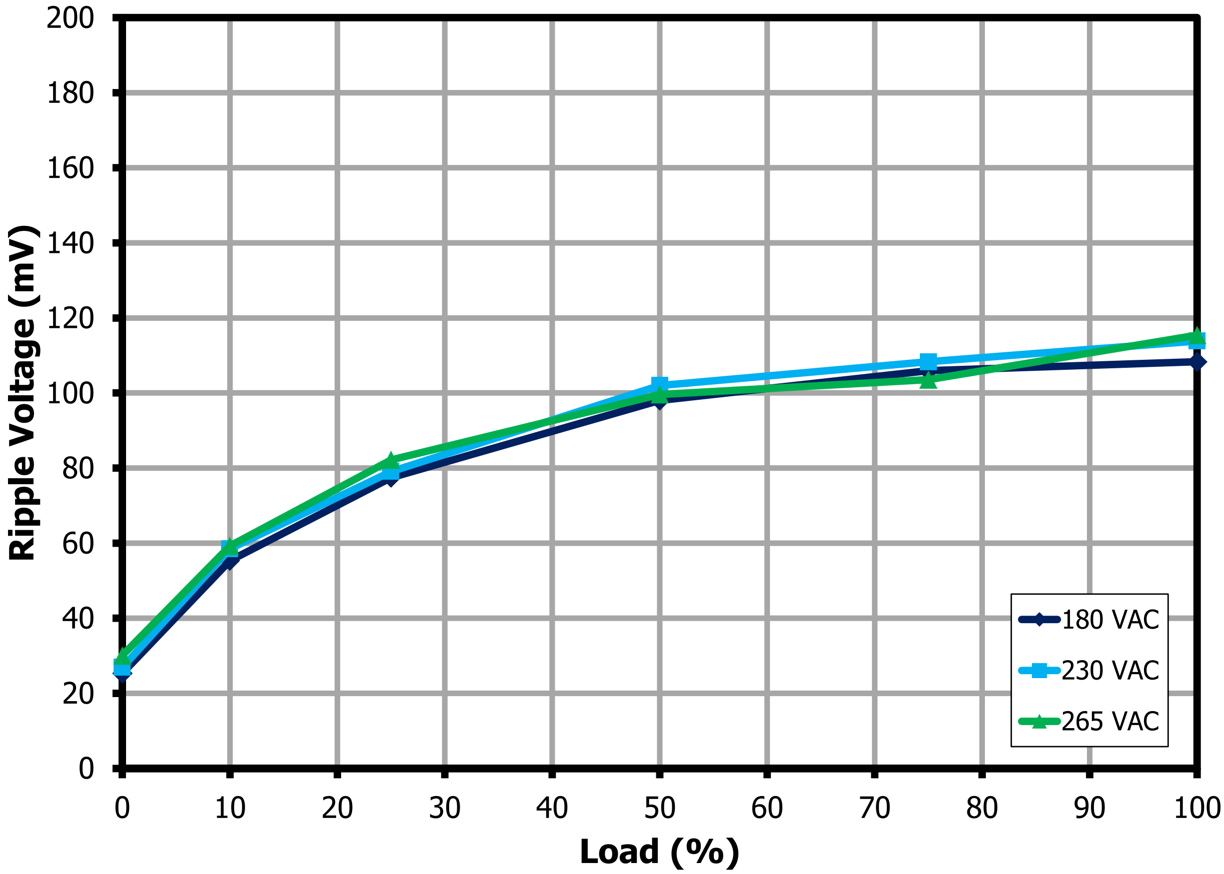


Figure 24 – Ripple Voltage vs. %Load at 9 V.

9.7.4 Output Ripple Voltage vs. Percent Load at 5 V / 6.5 A.

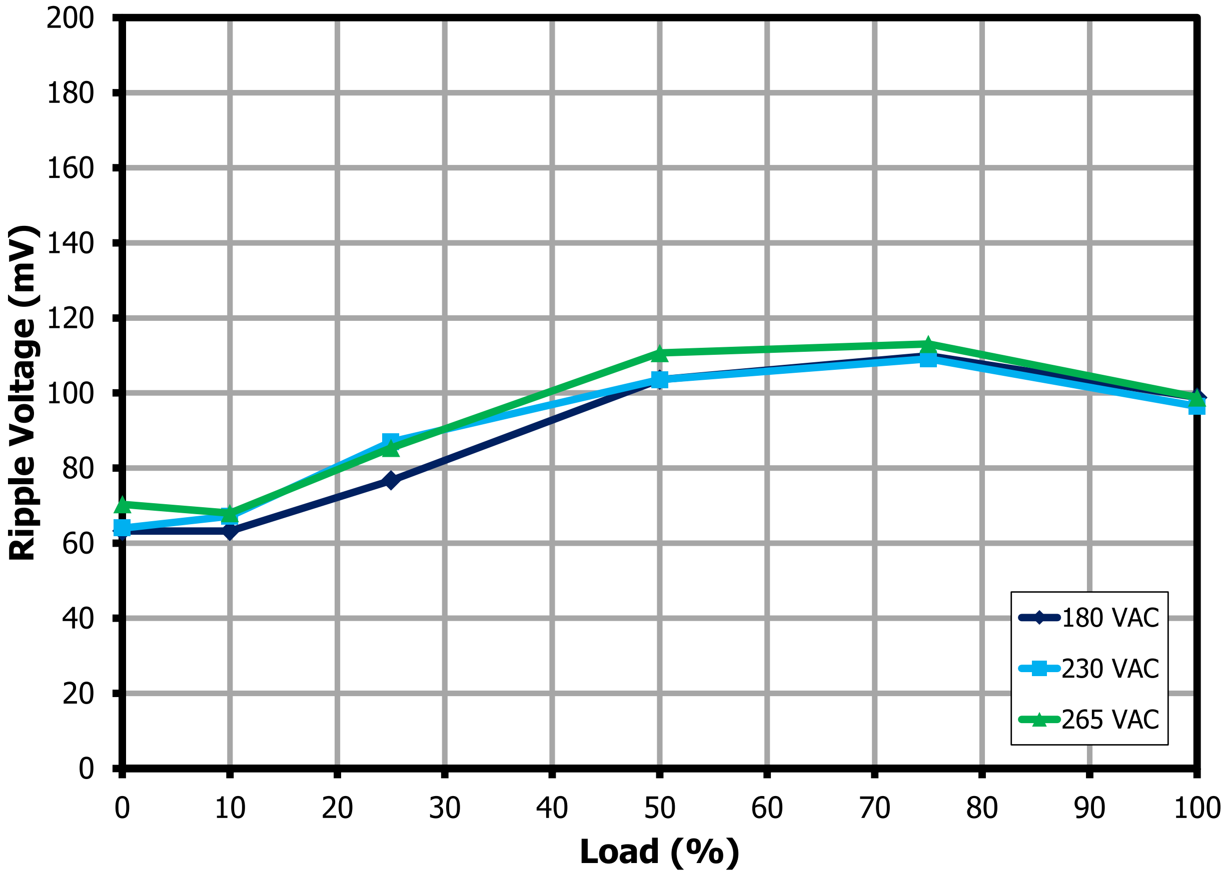


Figure 25 – Ripple Voltage vs. %Load at 5 V.

10 Thermal Performance

10.1 Thermal Scan at 25 ºC Ambient

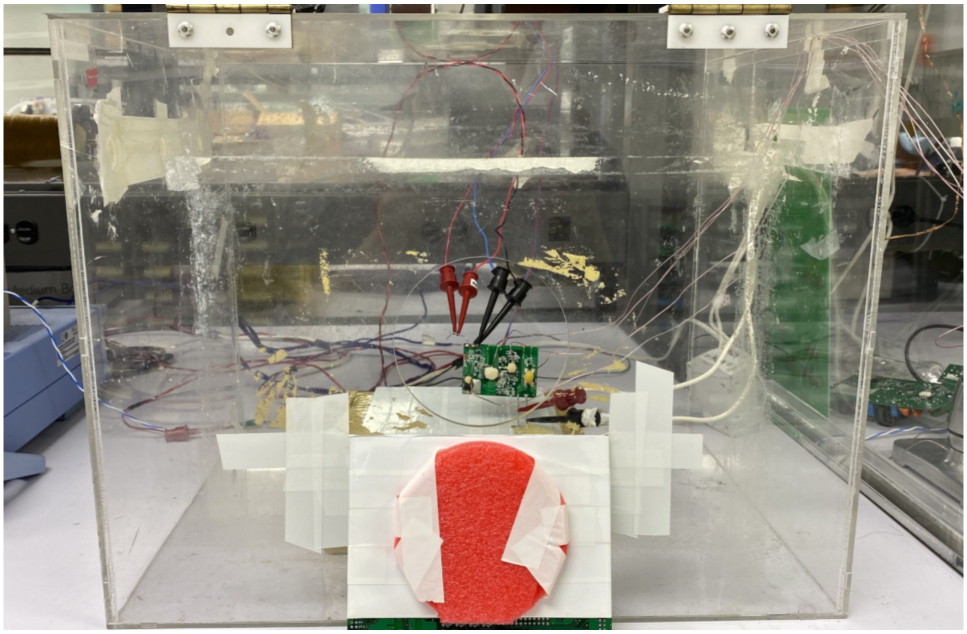


Figure 26 – Test Set-up Picture.

10.1.1 Thermal Scan Summary – 20 V, 3.5 A and Extended loading at 9 V, 6 A

Note: Tested using a thermocouple

20 V, 3.5 A Output				
Component	**Case Temperature (°C)**			
	100 VAC	**180 VAC**	**230 VAC**	**265 VAC**
U4 – InnoSwitch4-CZ	98.95	73.6	71.3	73.9
Q4 – SRFET	88	71.6	71.3	73.9
BR1 – Bridge Diode	80.85	57.6	52.6	52.1
U3 – ClampZero	82.3	67.1	66.3	67.8
T1 – Main TRF	81.35	70.7	71.7	73.5

Extend Loading 9 V, 6 A Output			
Component	**Case Temperature (°C)**		
	180 VAC	**230 VAC**	**265 VAC**
U4 – InnoSwitch4-CZ (Secondary)	90.1	77.7	74.7
Q4 – SRFET	90.7	85.7	85
BR1 – Bridge Diode	56.1	50.1	48.5
U3 – ClampZero	72.2	65.4	64.9
T1 – Main TRF (Core)	81.3	76.8	77

10.1.2 100 VAC Input 20 V / 3.5 A

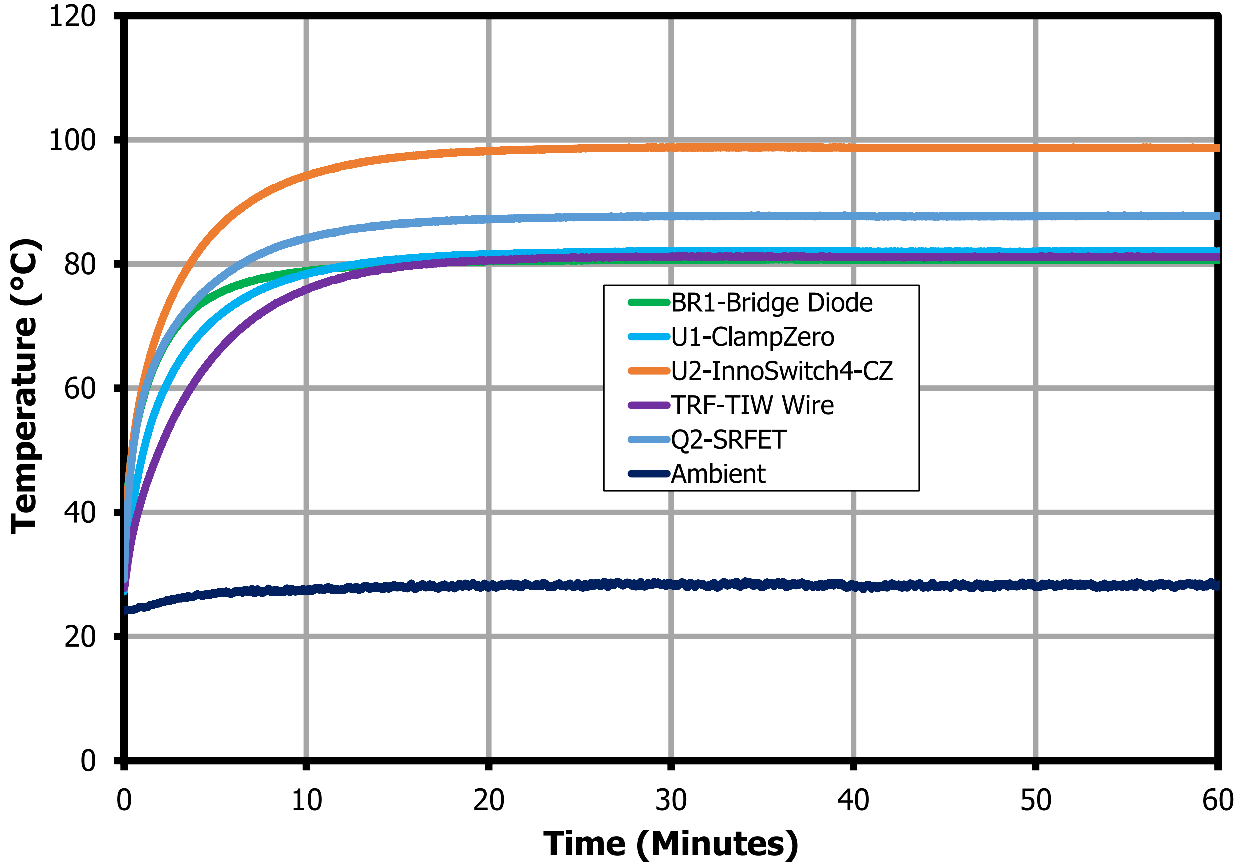


Figure 27 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	100 VAC
Ambient	28.6
TRF – TIW Wire	81.35
U2 – InnoSwitch4-CZ	98.95
U1 – ClampZero	82.3
Q2 – SRFET	88
BR1 – Bridge Diode	80.85

10.1.3 180 VAC Input 20 V / 3.5 A

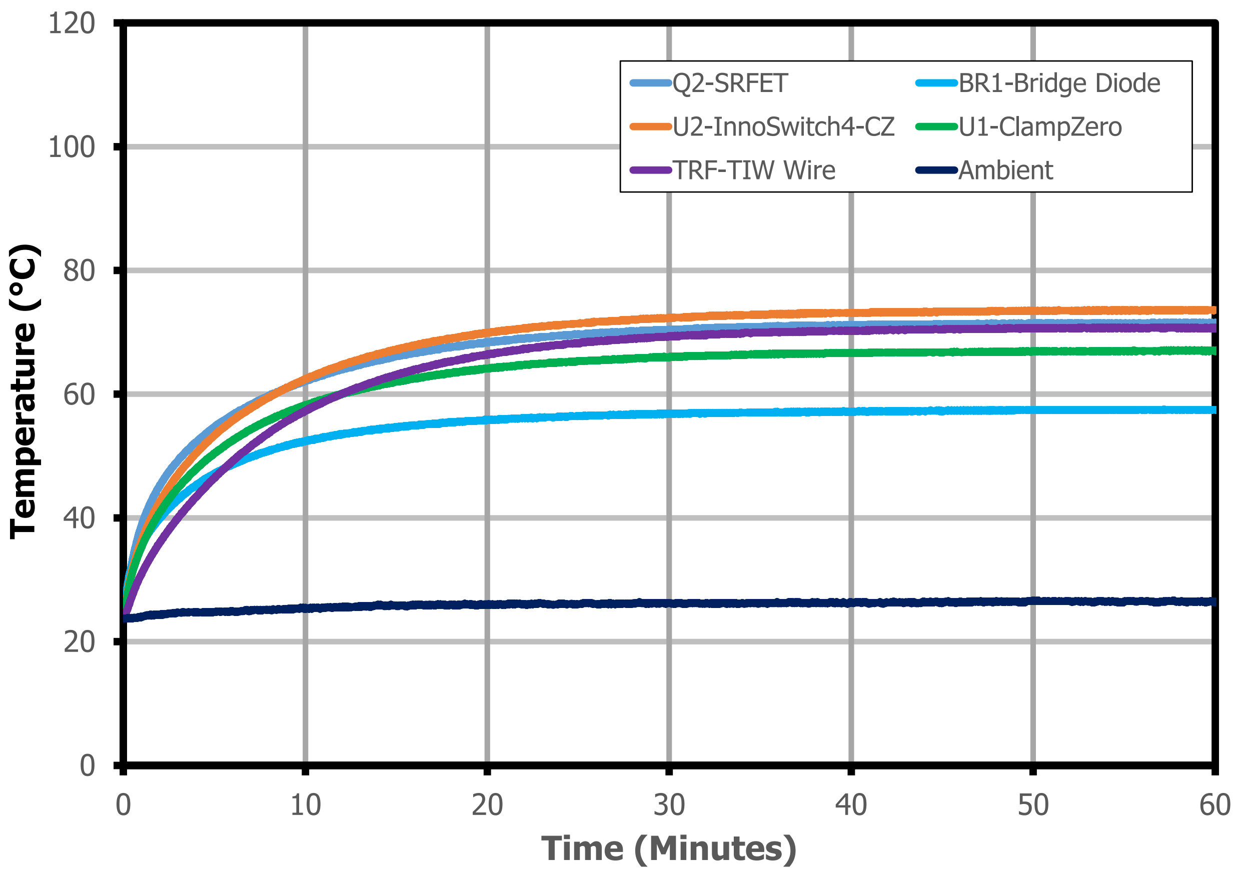


Figure 28 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	180 VAC
Ambient	26.5
TRF – TIW Wire	70.7
U2 – InnoSwitch4-CZ	73.6
U1 – ClampZero	67.1
Q2 – SRFET	71.6
BR1 – Bridge Diode	57.6

10.1.4 230 VAC Input 20 V / 3.5 A

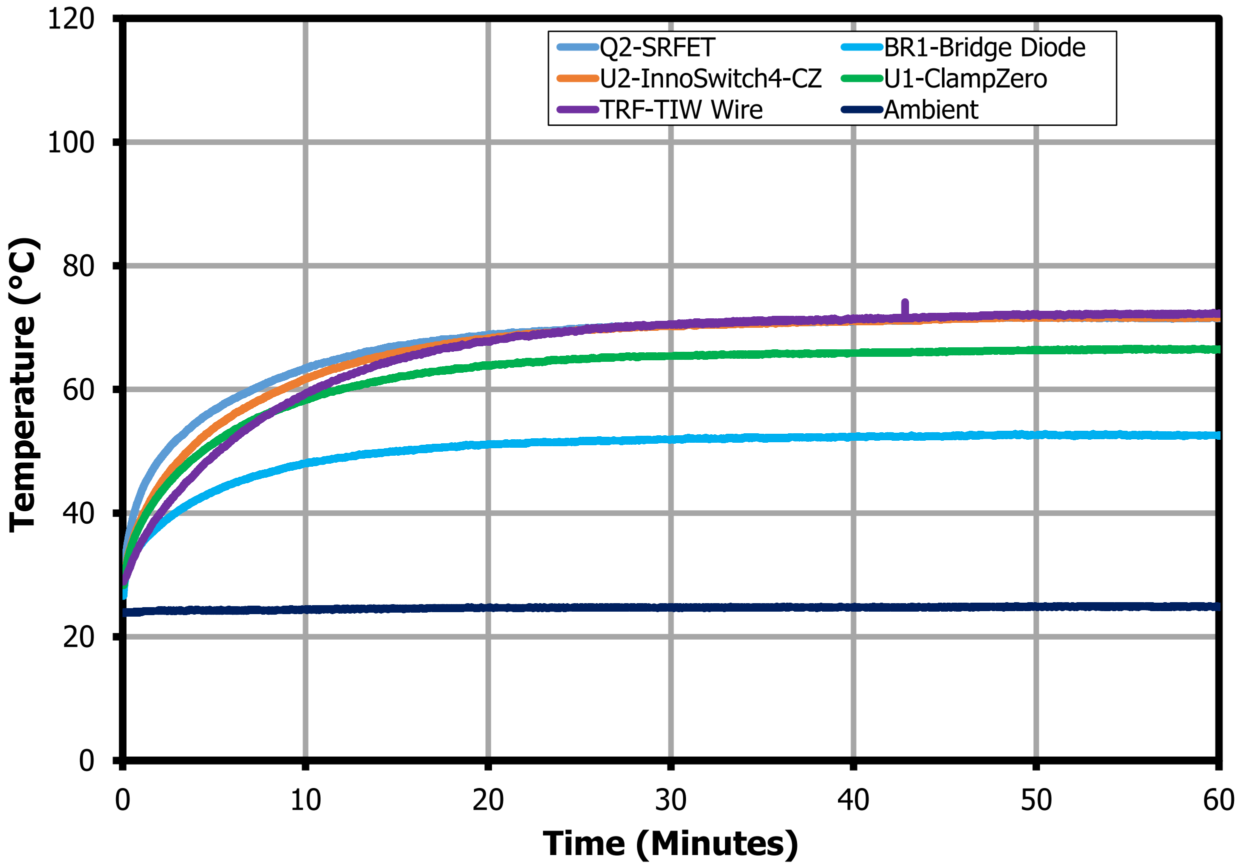


Figure 29 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	230 VAC
Ambient	24.8
TRF – TIW Wire	71.7
U2 – InnoSwitch4-CZ	71.3
U1 – ClampZero	66.3
Q2 – SRFET	71.3
BR1 – Bridge Diode	52.6

10.1.5 265 VAC Input 20 V / 3.5 A

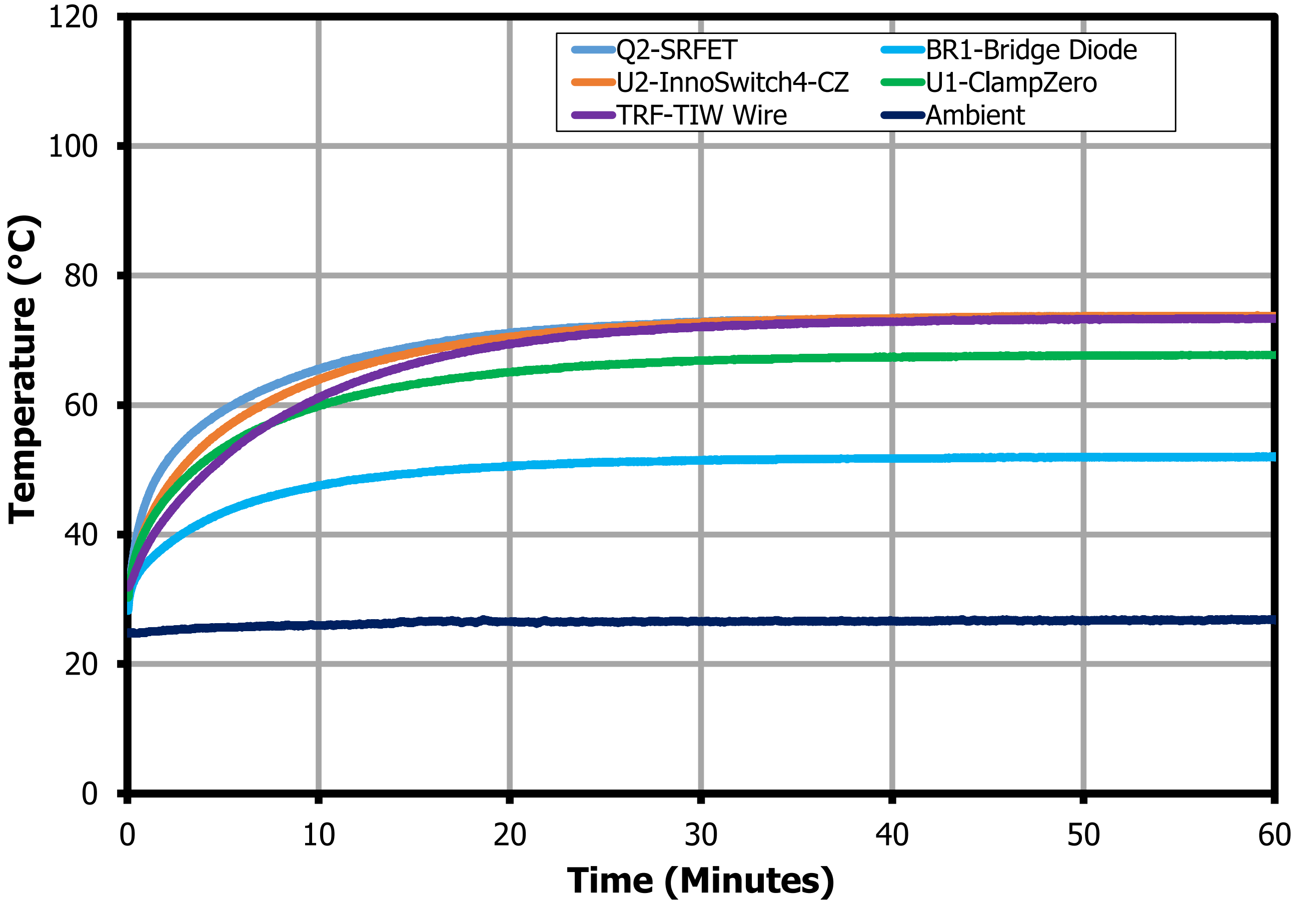


Figure 30 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	265 VAC
Ambient	25.3
TRF – TIW Wire	73.5
U2 – InnoSwitch4-CZ	73.9
U1 – ClampZero	67.8
Q2 – SRFET	73.9
BR1 – Bridge Diode	52.1

10.2 Thermal Scan with Extended Loading at 9 V / 6 A

10.2.1 180 VAC Input 9 V / 6 A

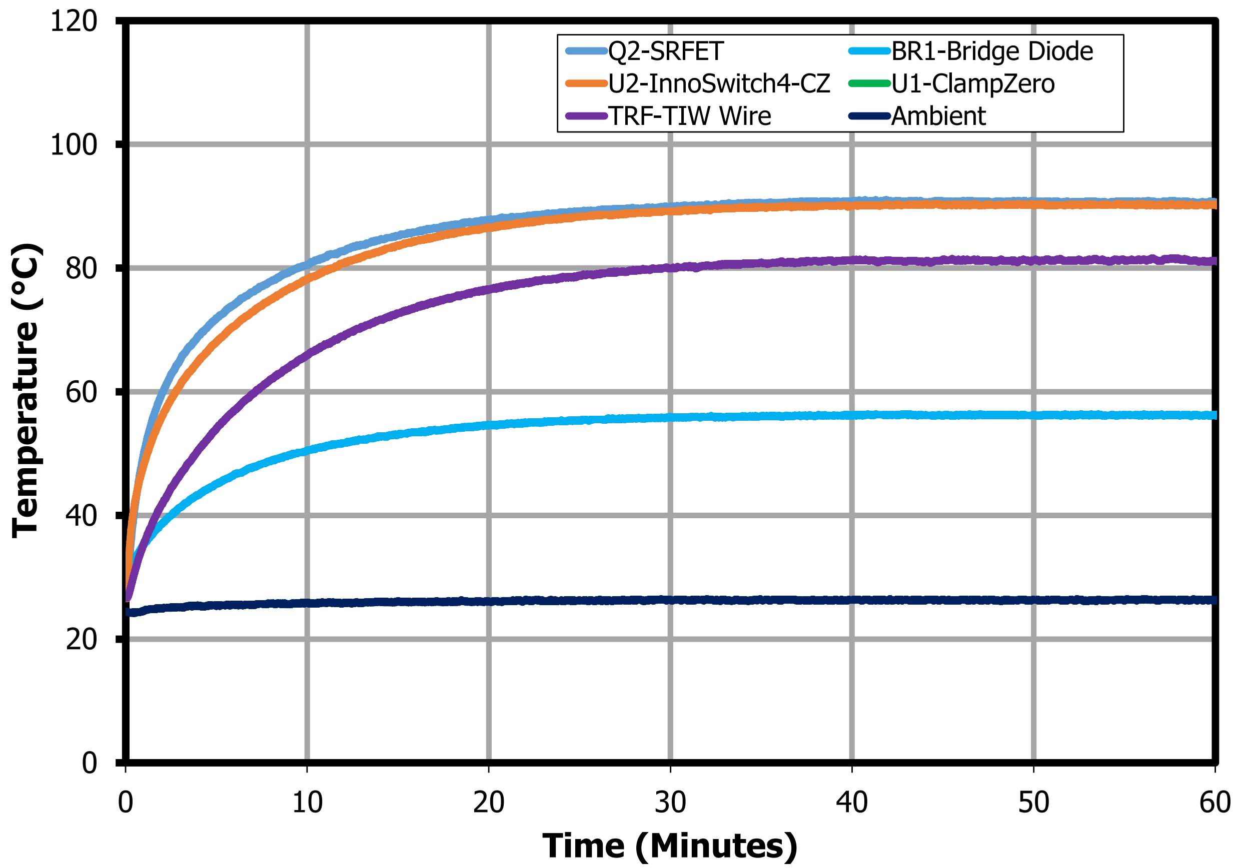


Figure 31 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	180 VAC
Ambient	26.3
TRF – TIW Wire	81.3
U2 – InnoSwitch4-CZ	90.1
U1 – ClampZero	72.2
Q2 – SRFET	90.7
BR1 – Bridge Diode	56.1

10.2.2 230 VAC Input 9 V / 6 A

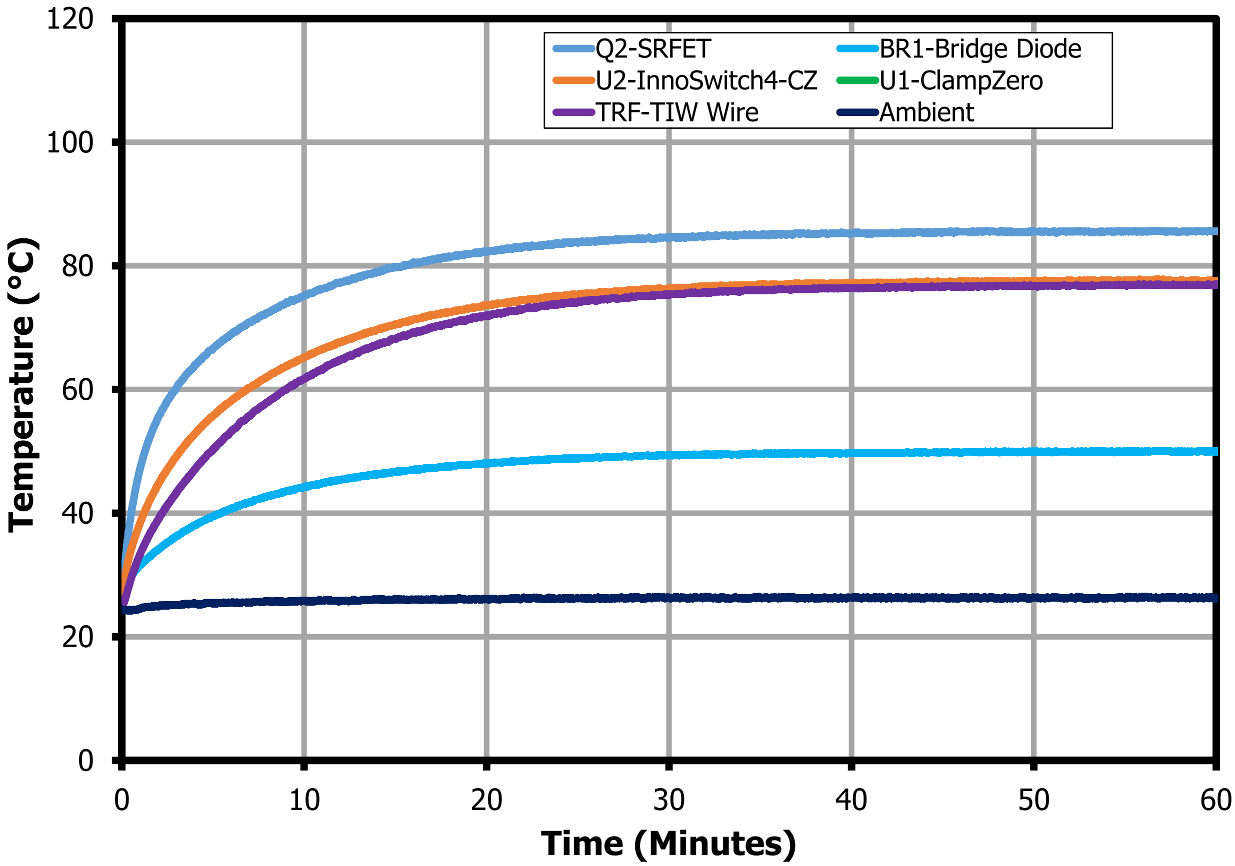


Figure 32 – Thermal Scan at 1 Hour.

Components	Temperature (°C) 230 VAC
Ambient	26.3
TRF – TIW Wire	76.8
U2 – InnoSwitch4-CZ	77.7
U1 – ClampZero	65.4
Q2 – SRFET	85.7
BR1 – Bridge Diode	50.1

10.2.3 265 VAC Input 9 V / 6 A

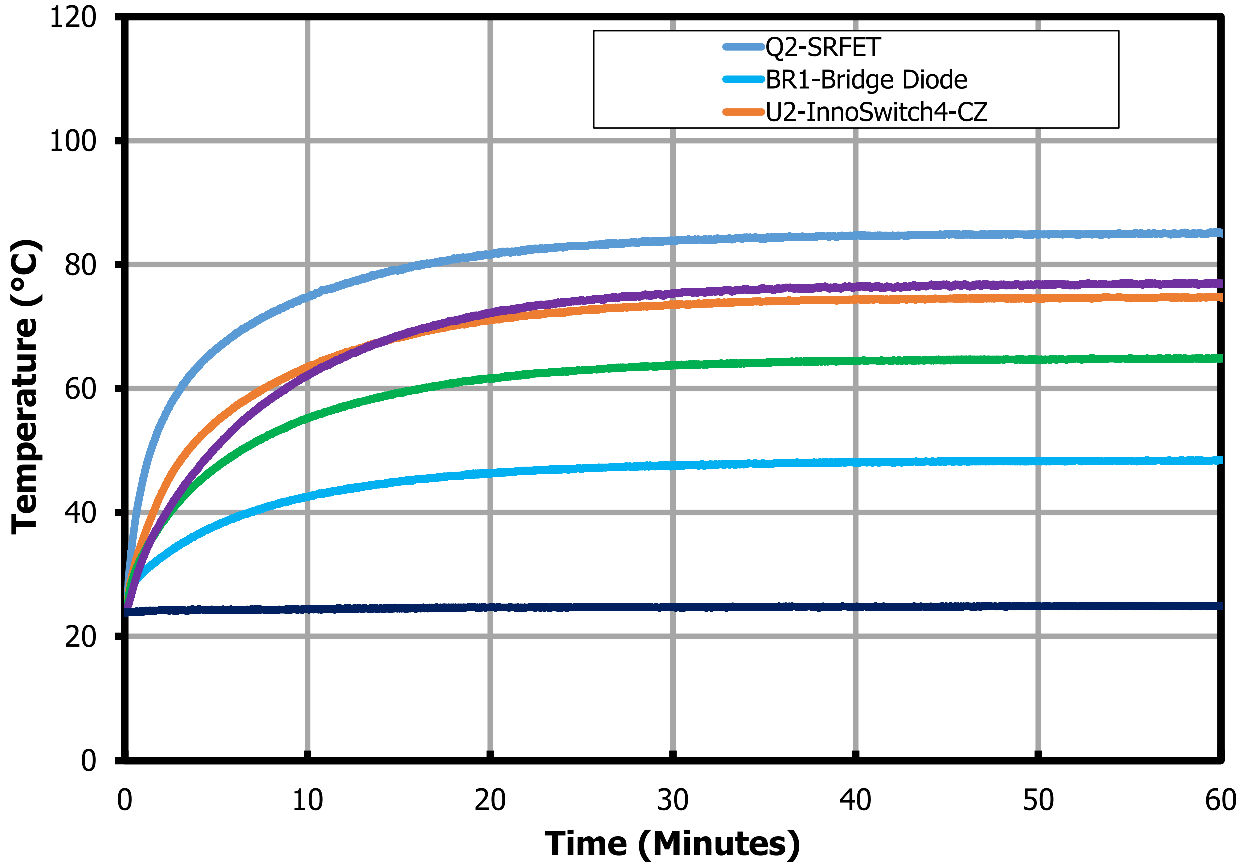


Figure 33 – Thermal Scan at 1 Hour.

Components	Temperature (°C)
	265 VAC
Ambient	24.8
TRF – TIW Wire	77
U2 – InnoSwitch4-CZ	74.7
U1 – ClampZero	64.9
Q2 – SRFET	85
BR1 – Bridge Diode	48.5

10.3 Thermal Performance at 50 ºC Ambient

10.3.1 Set-up Picture

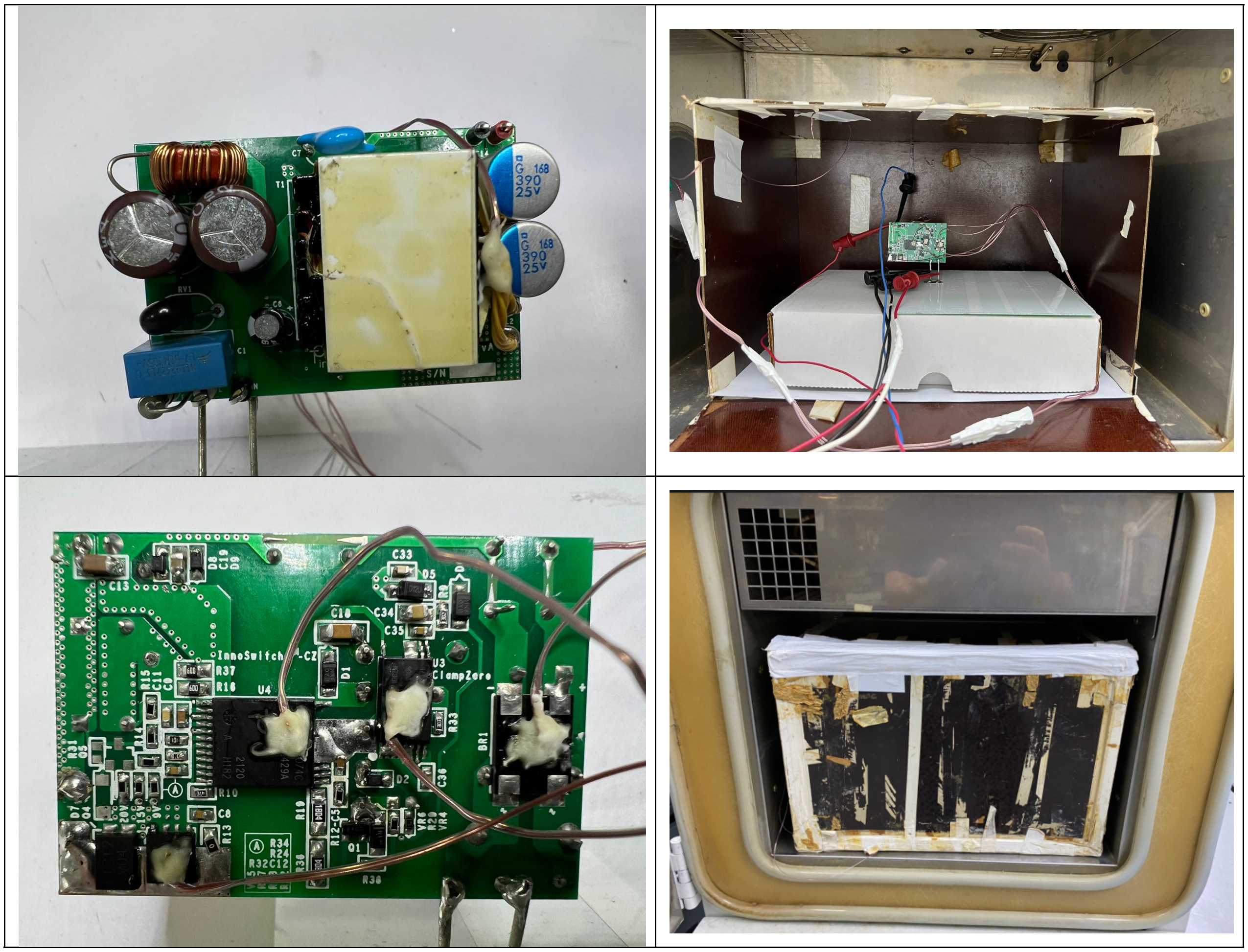


Figure 34 – Tested Using the Environmental Test Chamber**.**

The DUT is placed inside enclosure to prevent airflow.

10.3.2 Thermal Test Summary 20 V, 3.5 A Output at 50 ºC Ambient

Input / Output Condition	Temperature (°C)					
	AMB	T1 (Main TRF)	U4 (InnoSwitch4- CZ)	U3 (ClampZero)	Q4 (SR FET)	BR1
180 VAC 20 V – 3.5 A	55.2	96.9	98.6	92	98.3	81
265 VAC 20 V – 3.5 A	51.2	96.3	95.7	89.9	97	72.3
180 VAC 9 V – 5 A	49.7	86	84.5	77.5	94.8	68
265 VAC 9 V – 5 A	50.4	88.9	88.7	80.6	97.5	65.9
180 VAC 5 V – 6.5 A	50.3	91.2	94.4	81.5	106.5	66.3
265 VAC 5 V – 6.5 A	50.7	94	98	83.5	108.2	64.8

10.3.3 Thermal Data at 50 ºC Ambient

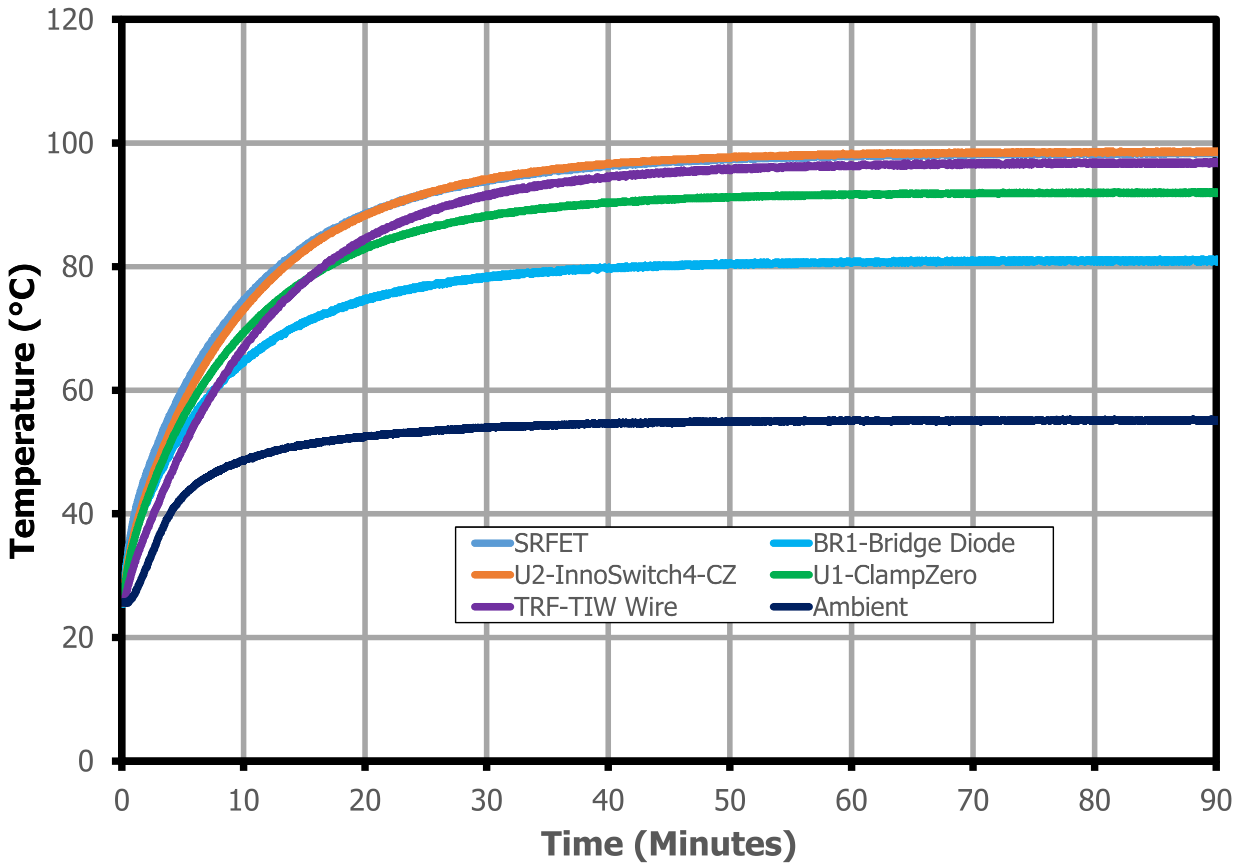


Figure 35 – Thermal Profile at 180 VAC, 20 V / 3.5 A.

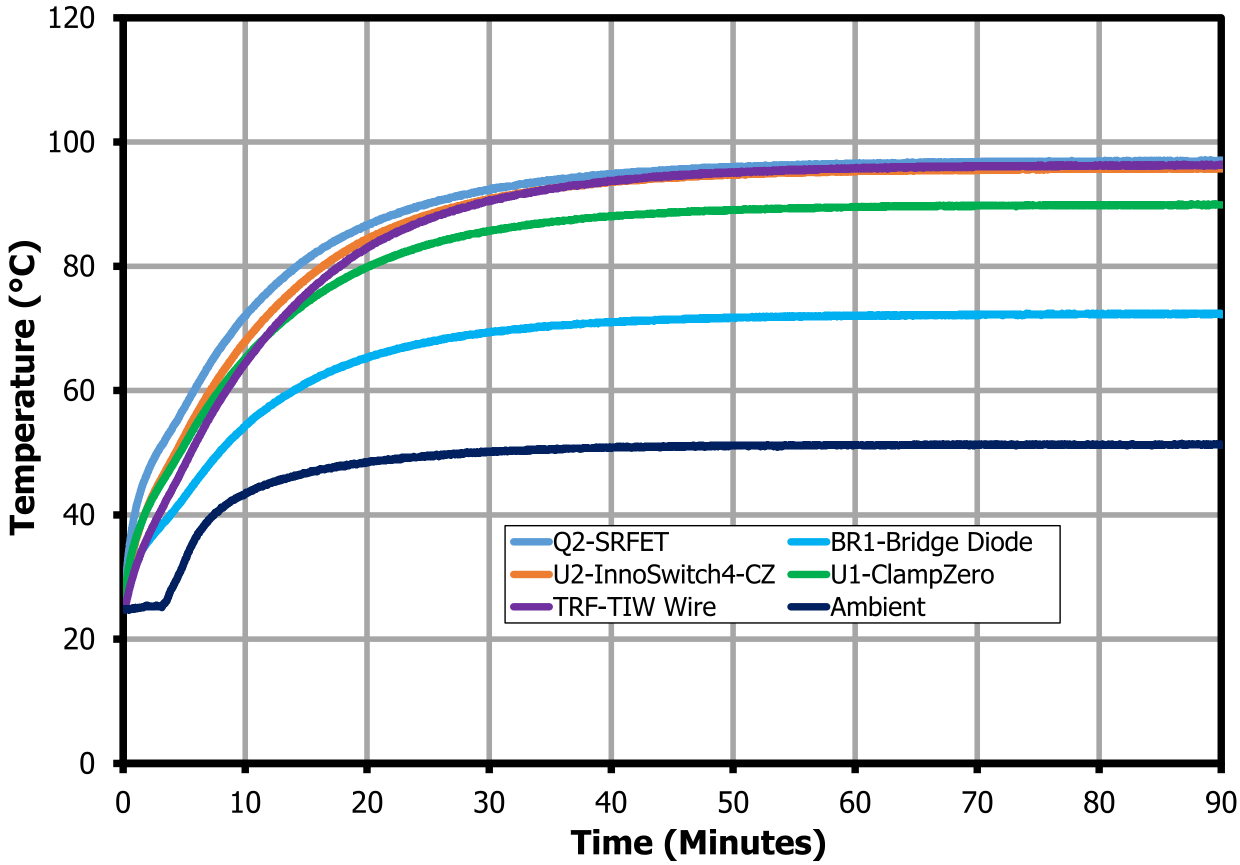


Figure 36 – Thermal Profile at 265 VAC, 20 V / 3.5 A.

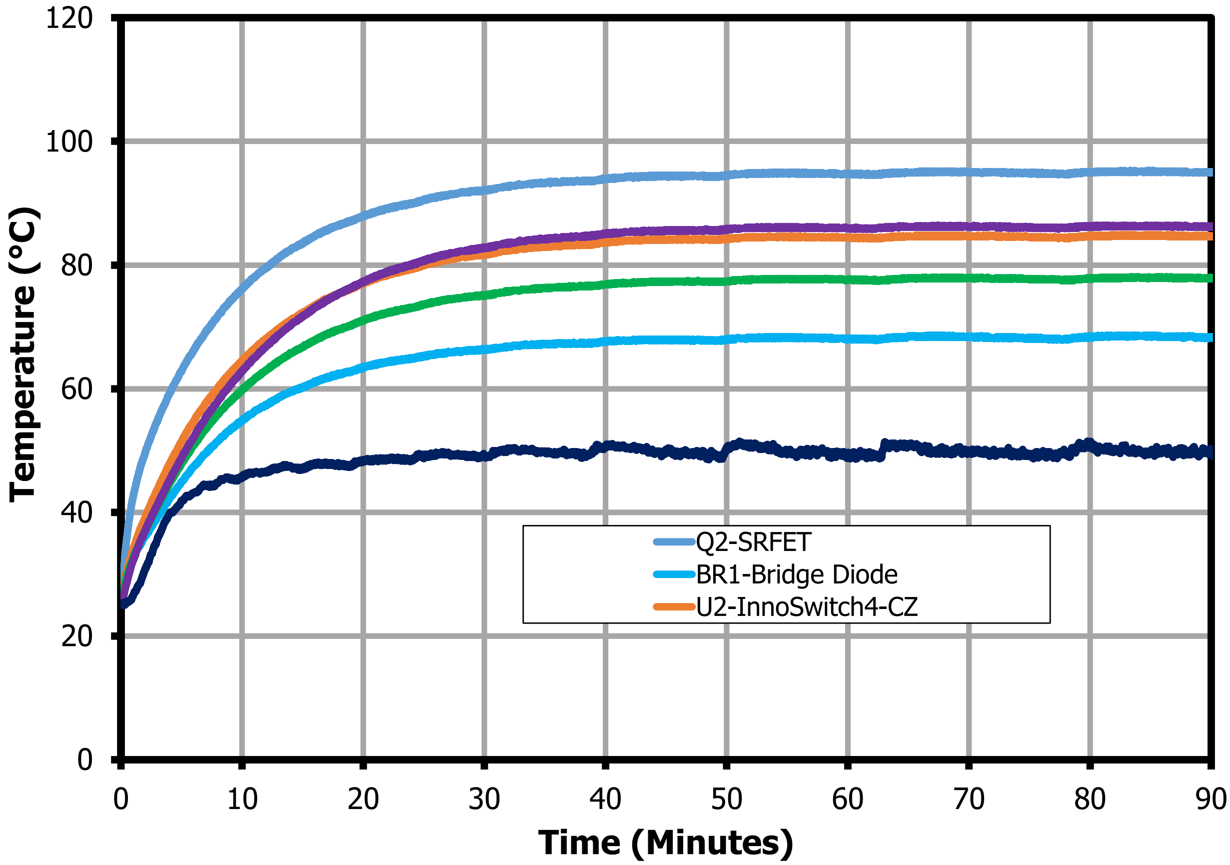


Figure 37 – Thermal Profile at 180 VAC, 9 V / 5 A.

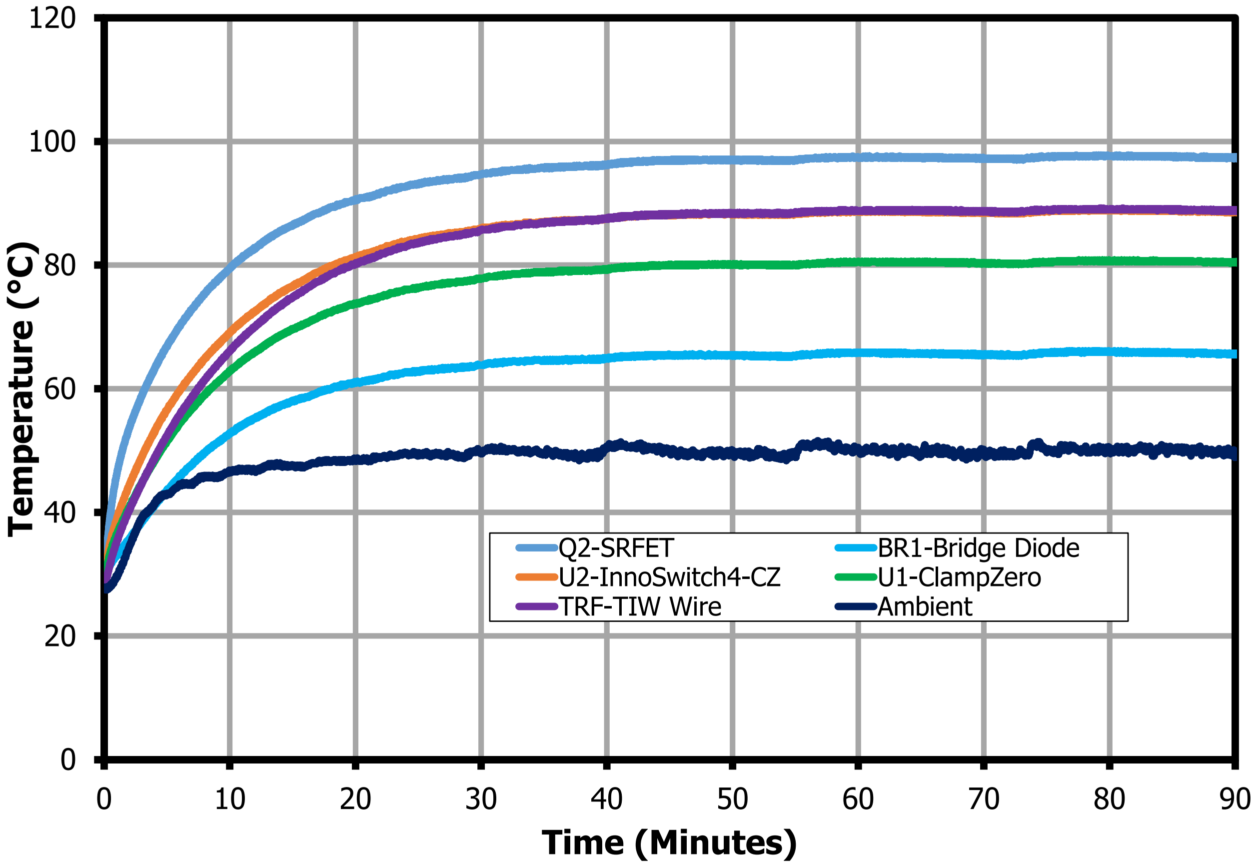


Figure 38 – Thermal Profile at 265 VAC, 9 V / 5 A.

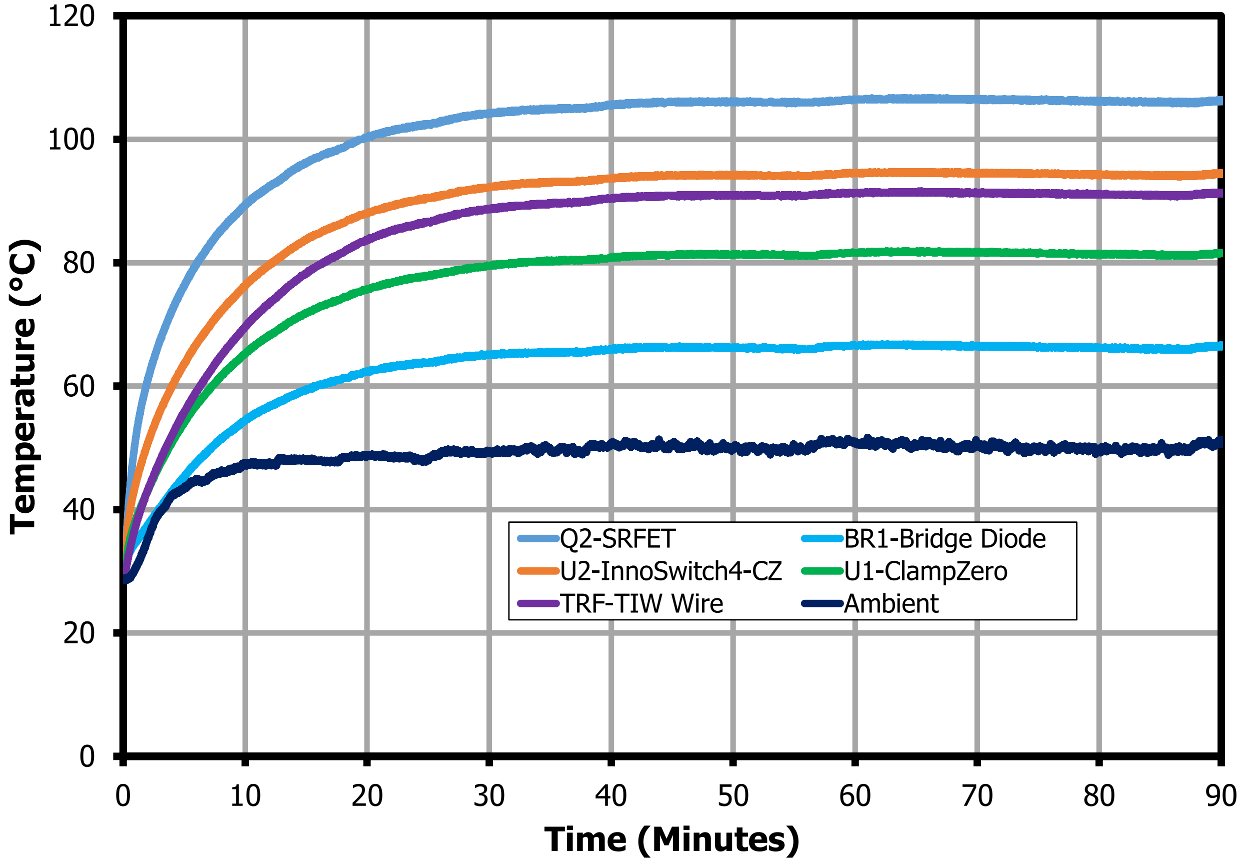


Figure 39 – Thermal Profile at 180 VAC, 5 V / 6.5 A.

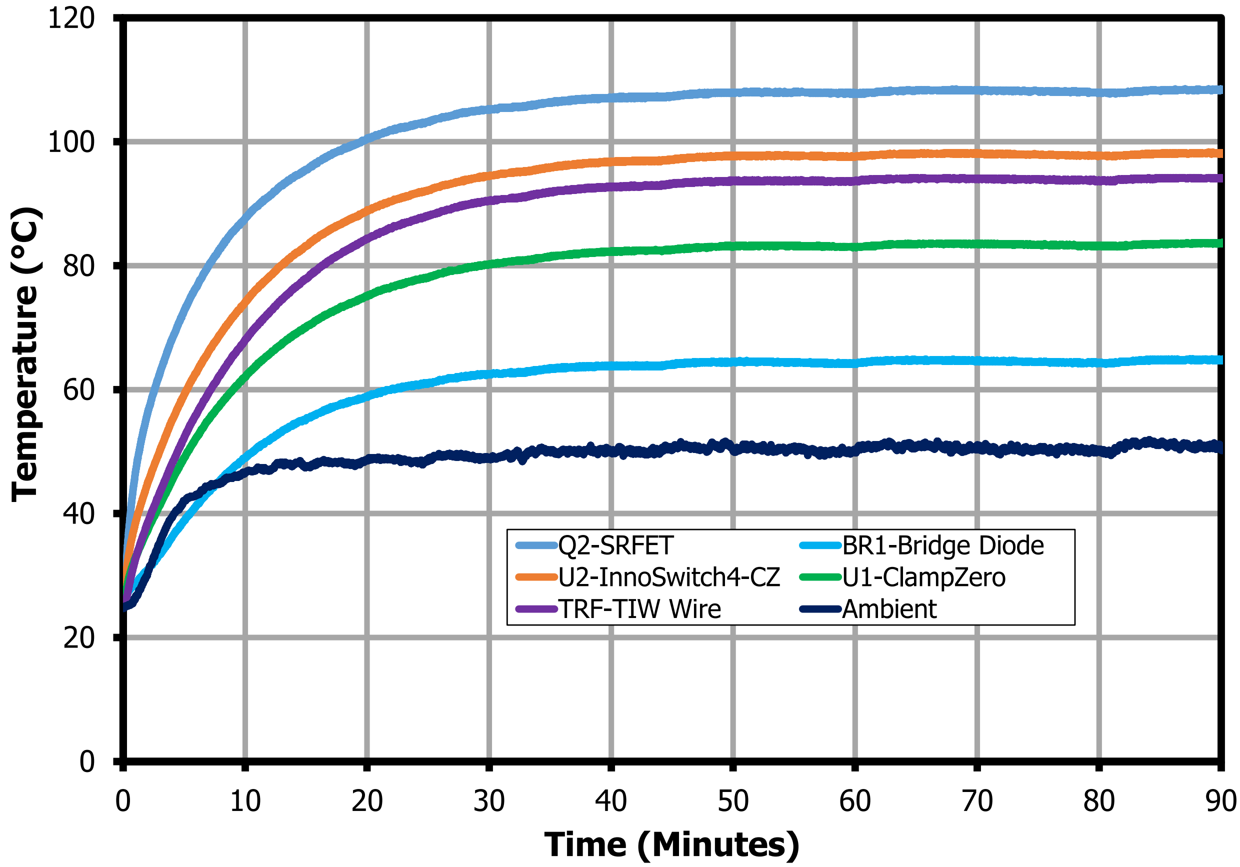


Figure 40 – Thermal Profile at 265 VAC, 5 V / 6.5 A.

11 Waveforms

11.1 Primary Drain Voltage and Current Waveform

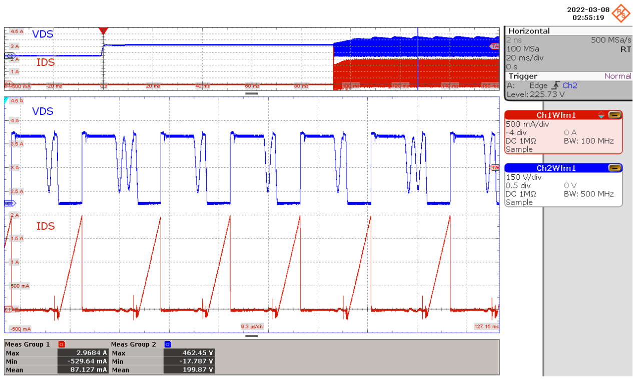


Figure 41 – 180 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Blue): V_{DS}, 150 V / div., 20 ms / div.
CH2(Red): I_{DS}, 0.5 A / div.
V_{DS} = 462.45 V, I_{DS} = 2.9684 A.

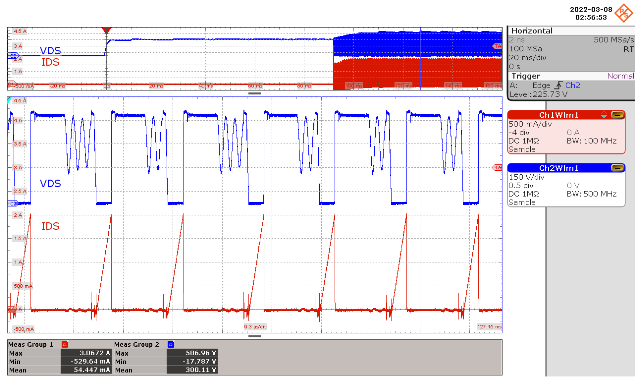


Figure 42 – 265 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Blue): V_{DS}, 150 V / div., 20 ms / div.
CH2(Red): I_{DS}, 0.5 A / div.
V_{DS} = 586.96 V, I_{DS} = 3.0672 A.

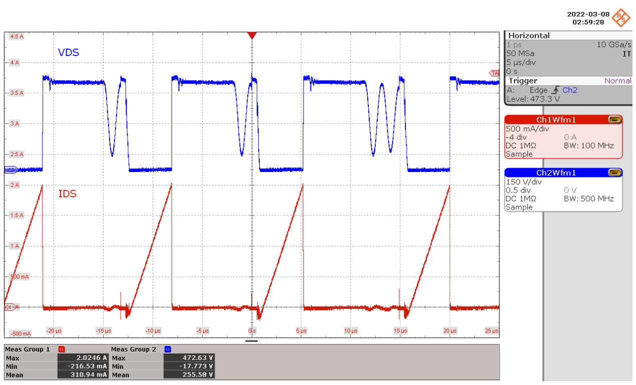


Figure 43 – 180 VAC 60 Hz, 20 V Full Load Normal.
CH1(Blue): V_{DS}, 150 V / div., 5 µs / div.
CH2(Red): I_{DS}, 0.5 A / div.
V_{DS} = 472.63 V, I_{DS} = 2.0246 A.

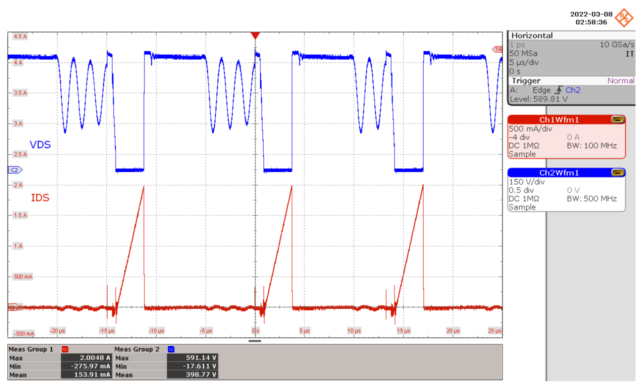


Figure 44 – 265 VAC 60 Hz, 20 V Full Load Normal.
CH1(Blue): V_{DS}, 150 V / div., 5 µ s / div.
CH2(Red): I_{DS}, 0.5 A / div.
V_{DS} = 591.14 V, I_{DS} = 2.0048 A.

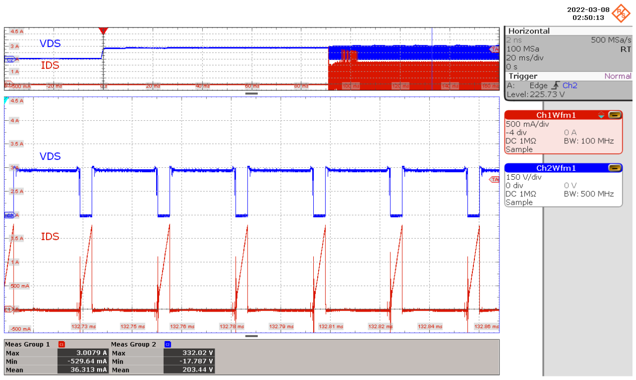


Figure 45 – 180 VAC 60 Hz, 5 V Full Load Start-up.
CH1(Red): I_{DS}, 0.5 A / div., 20 ms / div.
CH2(Blue): V_{DS}, 150 V / div.
V_{DS} = 332.02 V, I_{DS} = 3.0079 A.

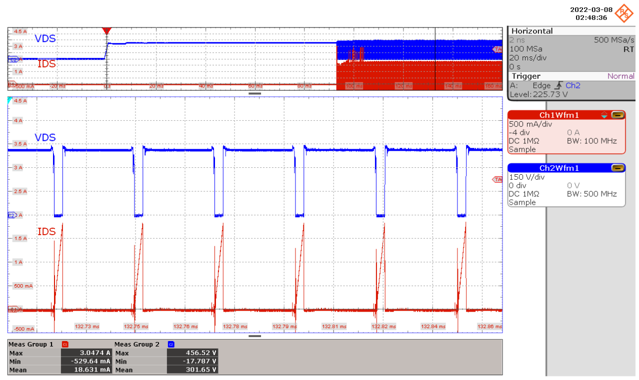


Figure 46 – 265 VAC 60 Hz, 5 V Full Load Start-up.
CH1(Red): I_{DS}, 0.5 A / div., 20 ms / div.
CH2(Blue): V_{DS}, 150 V / div.
V_{DS} = 456.52 V, I_{DS} = 3.0474 A.

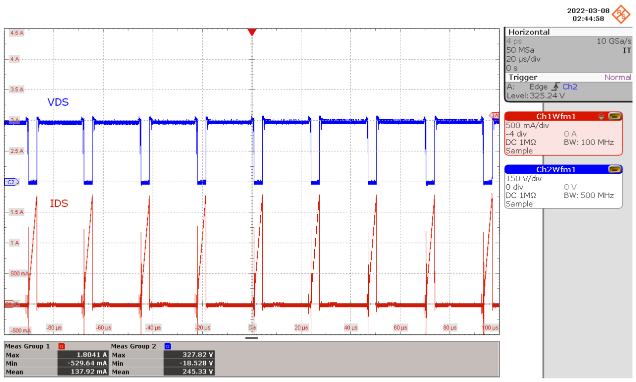


Figure 47 – 180 VAC 60 Hz, 5 V Full Load Normal.
CH1(Red): I_{DS}, 0.5 A / div., 20 μs / div.
CH2(Blue): V_{DS}, 150 V / div.
V_{DS} = 322.82 V, I_{DS} = 1.8041 A.

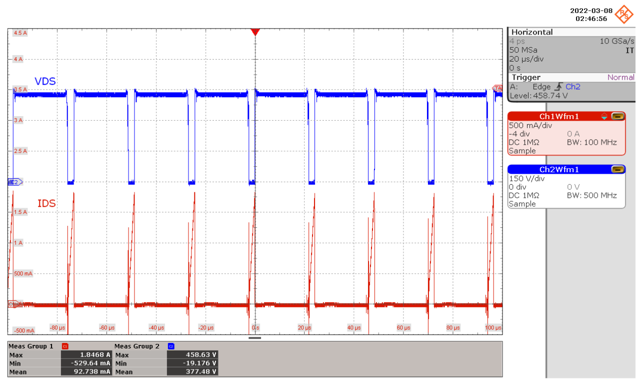


Figure 48 – 265 VAC 60 Hz, 5 V Full Load Normal.
CH1(Red): I_{DS}, 0.5 A / div., 20 μs / div.
CH2(Blue): V_{DS}, 150 V / div.
V_{DS} = 458.63 V, I_{DS} = 1.8468 A.

11.2 SR FET Drain Voltage Waveform

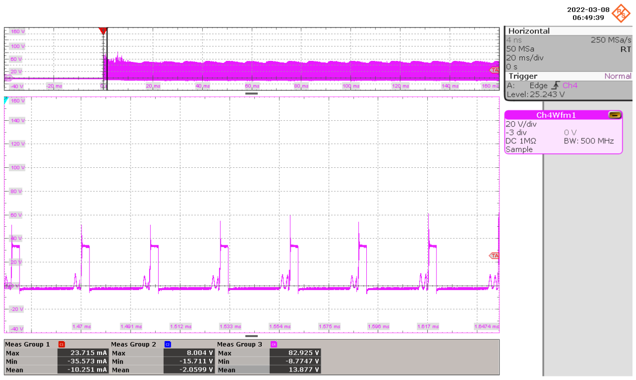


Figure 49 – 180 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Pink): V_{DS}, 20 V / div., 20 ms / div.
V_{DS} = 82.925 V.

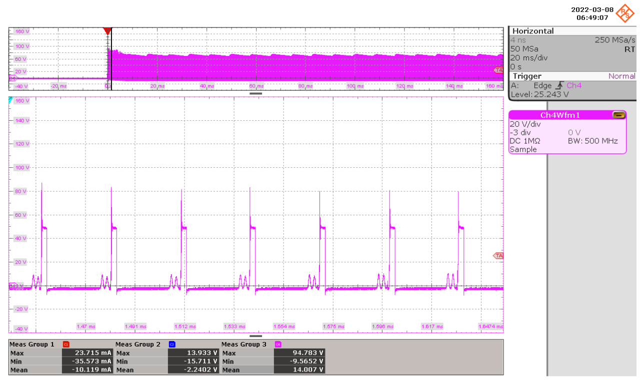


Figure 50 – 265 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Pink): V_{DS}, 20 V / div., 20 ms / div.
V_{DS} = 94.783 V.

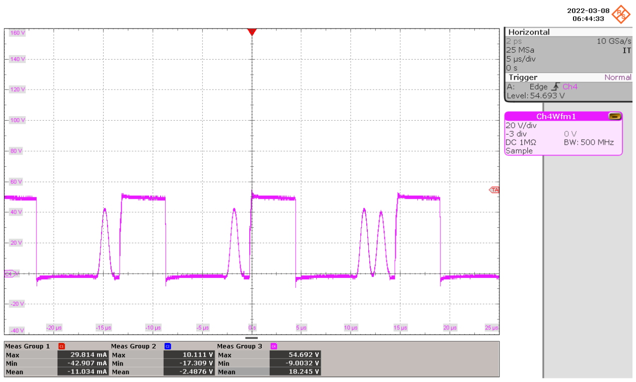


Figure 51 – 180 VAC 60 Hz, 20 V Full Load Normal.
CH1(Pink): V_{DS}, 20 V / div., 5 µs / div.
V_{DS} = 54.692 V.

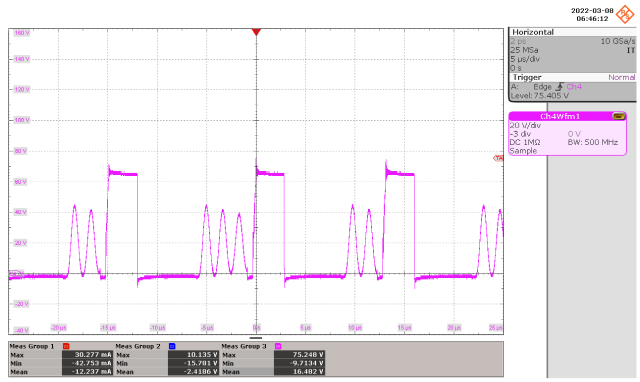


Figure 52 – 265 VAC 60 Hz, 20 V Full Load Normal.
CH1(Pink): V_{DS}, 20 V / div., 5 µs / div.
V_{DS} = 75.248 V.

11.3 Start-up Profile

Tested using an E-load set at constant current mode.

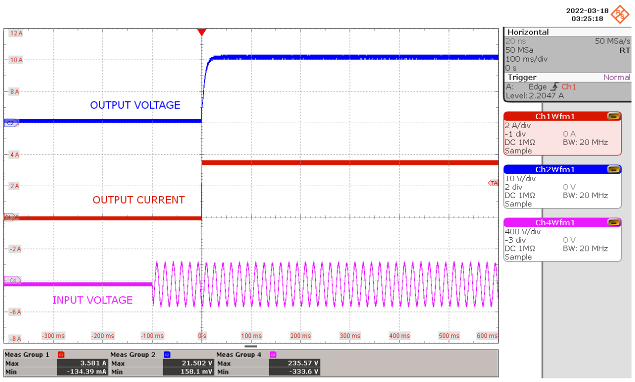


Figure 53 – 180 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 10 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

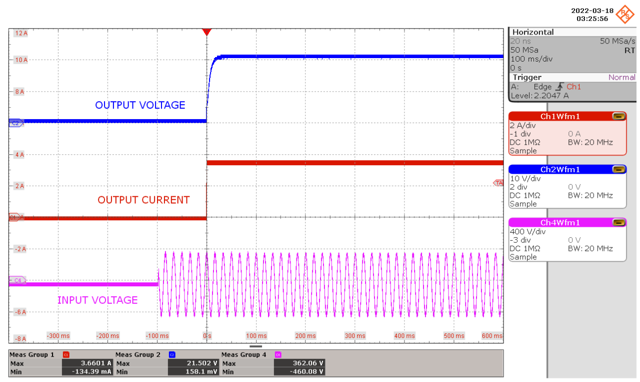


Figure 54 – 265 VAC 60 Hz, 20 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 10 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

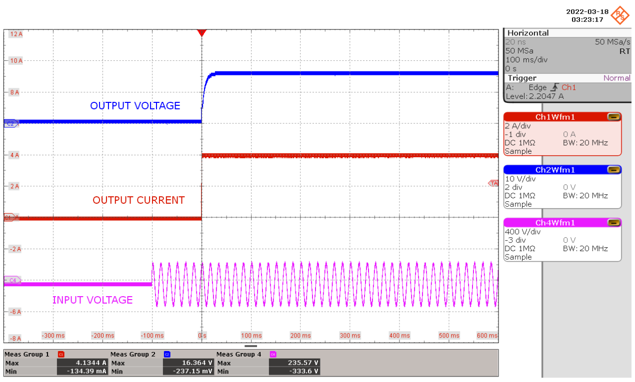


Figure 55 – 100 VAC 60 Hz, 15 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 10 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

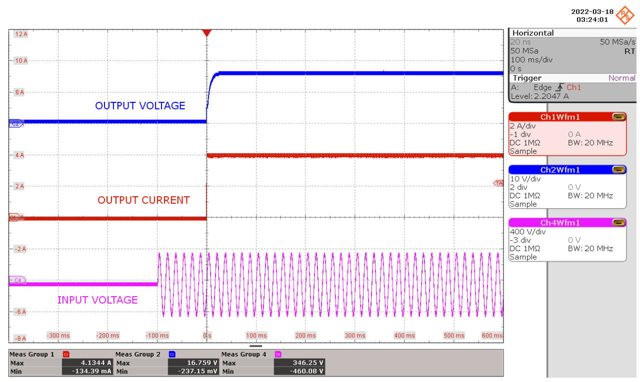


Figure 56 – 132 VAC 60 Hz, 15 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 10 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

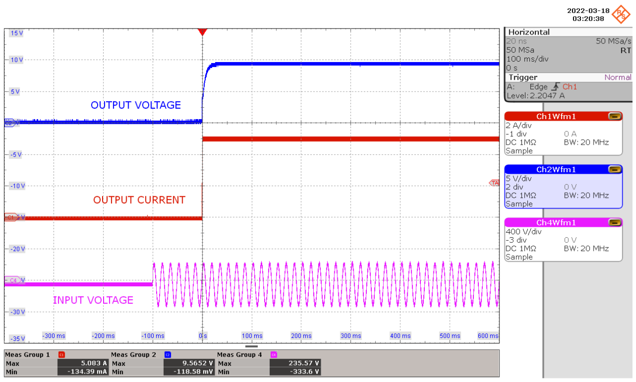


Figure 57 – 180 VAC 60 Hz, 9 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 5 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

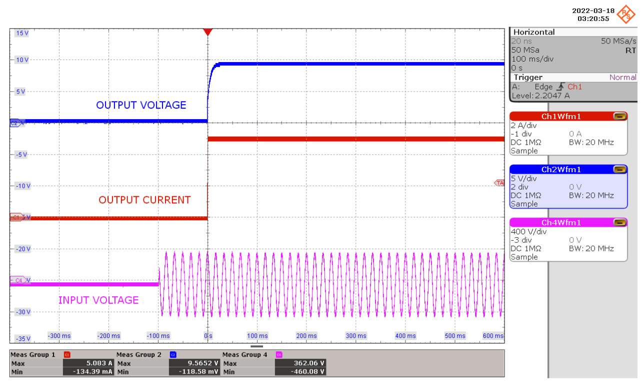


Figure 58 – 265 VAC 60 Hz, 9 V Full Load Start-up.
CH1(Red): I_{OUT}, 2 A / div.
CH2(Blue): V_{OUT}, 5 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

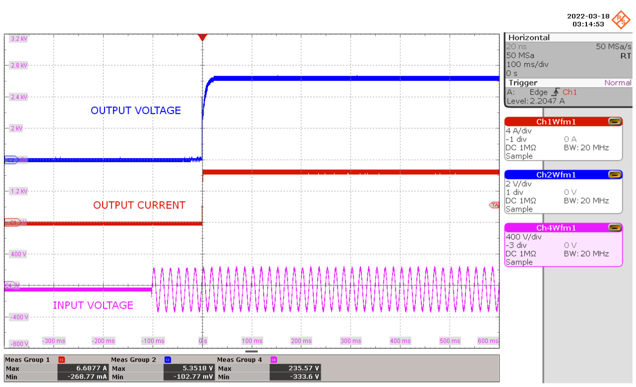


Figure 59 – 180 VAC 60 Hz, 5 V Full Load Start-up.
CH1(Red): I_{OUT}, 4 A / div.
CH2(Blue): V_{OUT}, 2 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

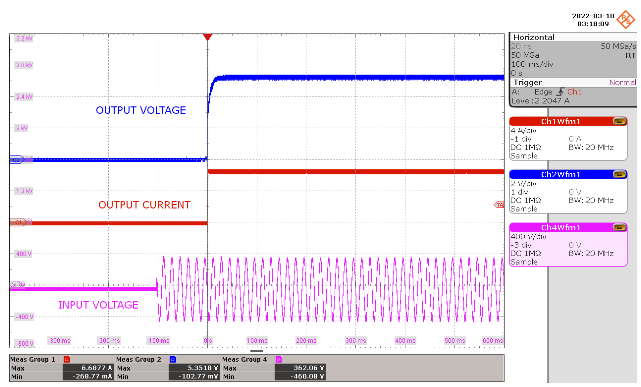


Figure 60 – 265 VAC 60 Hz, 5 V Full Load Start-up.
CH1(Red): I_{OUT}, 4 A / div.
CH2(Blue): V_{OUT}, 2 V / div.
CH3(Pink): V_{IN}, 400 V / div., 100 ms / div.

11.4 Transient Load Response

Tested using an E-Load set at dynamic constant current loading.

11.4.1 Transient Load at V_{OUT} = 20 V

Set-up: Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 200 mA / µs

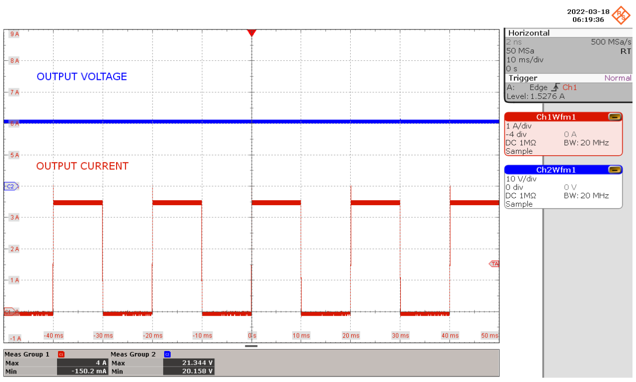


Figure 61 – 180 VAC 60 Hz, 0-3.5 A Transient Load.
CH1(Blue): V_{OUT}, 10 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 1 A / div.
$V_{OUT(MAX)}$ = 21.344 V, $V_{OUT(MIN)}$ = 20.158 V.

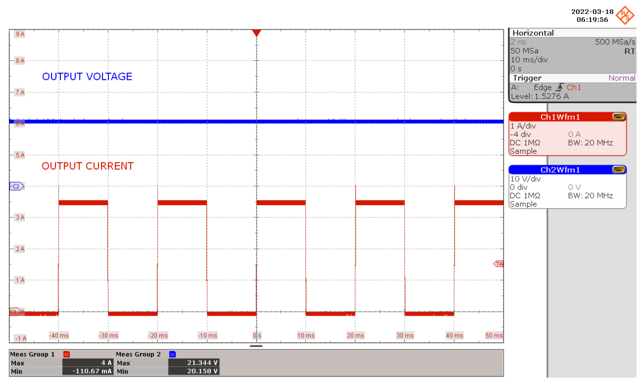


Figure 62 – 265 VAC 60 Hz, 0-3.5 A Transient Load.
CH1(Blue): V_{OUT}, 10 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 1 A / div.
$V_{OUT(MAX)}$ = 21.344 V, $V_{OUT(MIN)}$ = 20.158 V.

11.4.2 Transient Load at V_{OUT} = 15 V

Set-up: Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 200 mA / µs

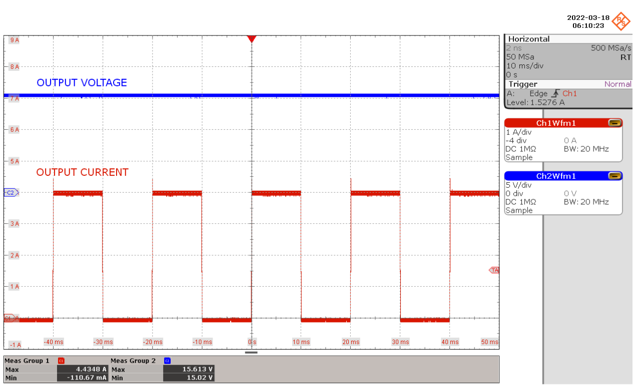


Figure 63 – 180 VAC 60 Hz, 0-4 A Transient Load.
CH1(Blue): V_{OUT}, 5 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 1 A / div.
$V_{OUT(MAX)}$ = 15.613 V, $V_{OUT(MIN)}$ = 15.02 V.

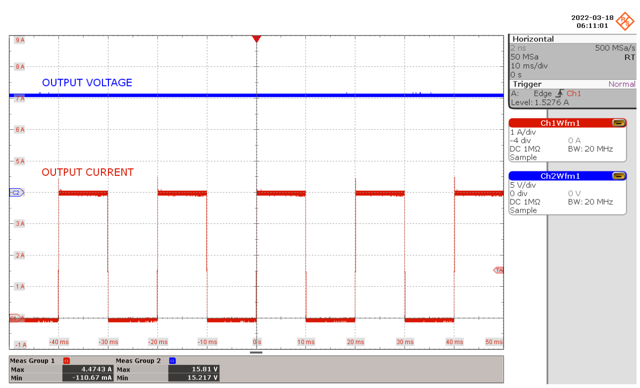


Figure 64 – 265 VAC 60 Hz, 0-4 A Transient Load.
CH1(Blue): V_{OUT}, 5 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 1 A / div.
$V_{OUT(MAX)}$ = 15.81 V, $V_{OUT(MIN)}$ = 15.217 V.

11.4.3 Transient Load at V_{OUT} = 9 V

Set-up: Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 200 mA / us

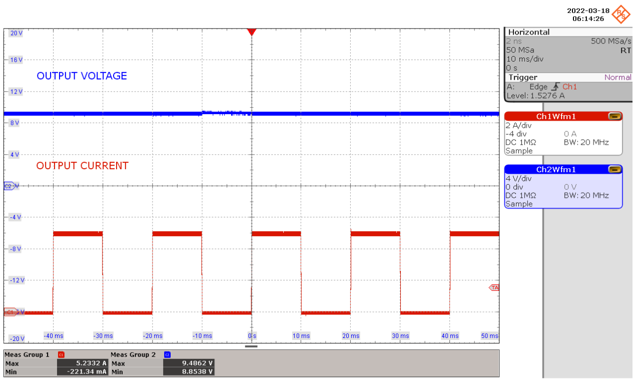


Figure 65 – 180 VAC 60 Hz, 0-5 A Transient Load.
CH1(Blue): V_{OUT}, 4 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 2 A / div.
$V_{OUT(MAX)}$ = 9.4862 V, $V_{OUT(MIN)}$ = 8.8538 V.

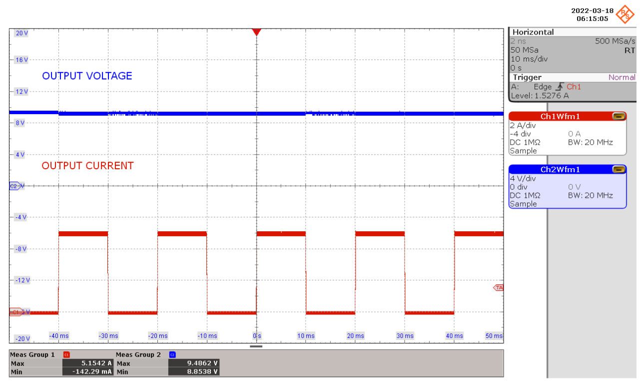


Figure 66 – 265 VAC 60 Hz, 0-5 A Transient Load.
CH1(Blue): V_{OUT}, 4 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 2 A / div.
$V_{OUT(MAX)}$ = 9.4862 V, $V_{OUT(MIN)}$ = 8.8538 V.

11.4.4 Transient Load at V_{OUT} = 5 V

Set-up: Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 200 mA / us

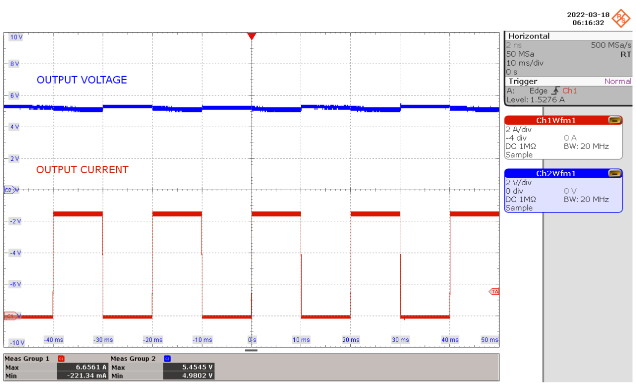


Figure 67 – 180 VAC 60 Hz, 0-6.5 A Transient Load.
CH1(Blue): V_{OUT}, 2 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 2 A / div.
$V_{OUT(MAX)}$ =5.4545 V, $V_{OUT(MIN)}$ = 4.9802 V.

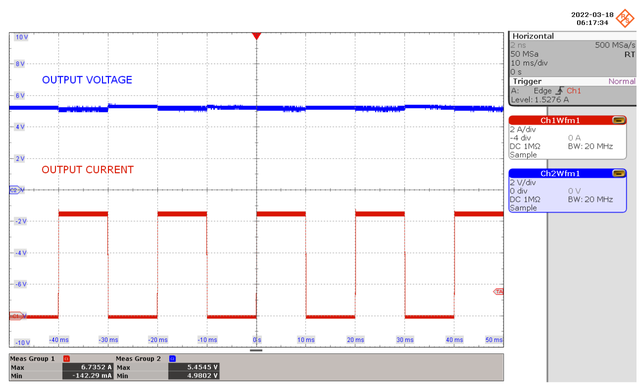


Figure 68 – 265 VAC 60 Hz, 0-6.5 A Transient Load.
CH1(Blue): V_{OUT}, 2 V / div., 10 ms / div.
CH2(Red): I_{OUT}, 2 A / div.
$V_{OUT(MAX)}$ =5.4545 V, $V_{OUT(MIN)}$ = 4.9802 V.

11.5 Output Ripple Voltage Waveforms

Tested at room ambient temperature using an E-load at constant current mode setting.

11.5.1 Output Ripple Voltage at V_{OUT} = 20 VDC / 3.5 A

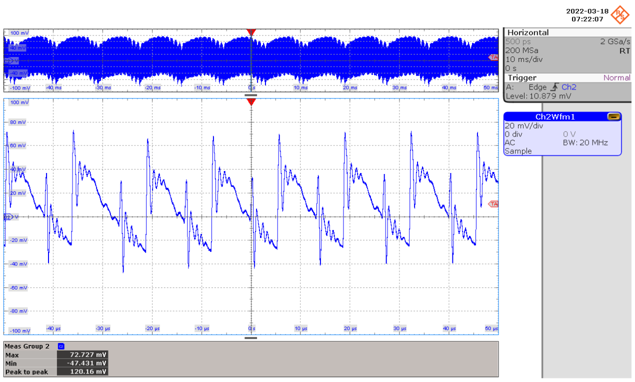


Figure 69 – 180 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 120.16 mV.

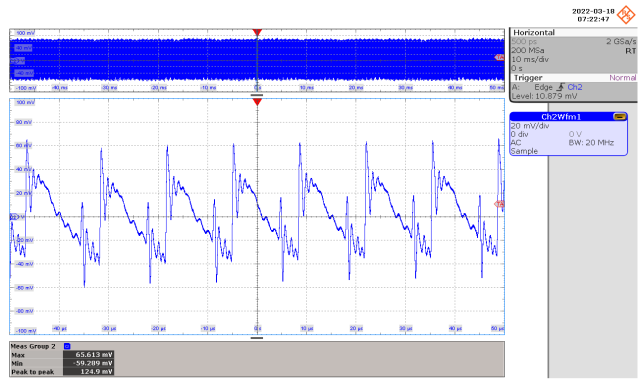


Figure 70 – 265 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 124.9 mV.

11.5.2 Output Ripple Voltage at V_{OUT} = 15 VDC / 4 A

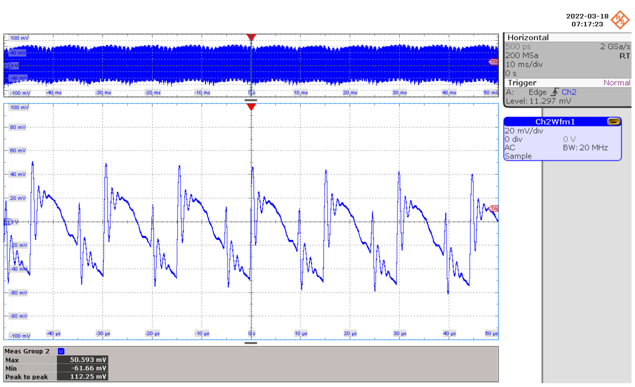


Figure 71 – 180 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 112.25 mV.

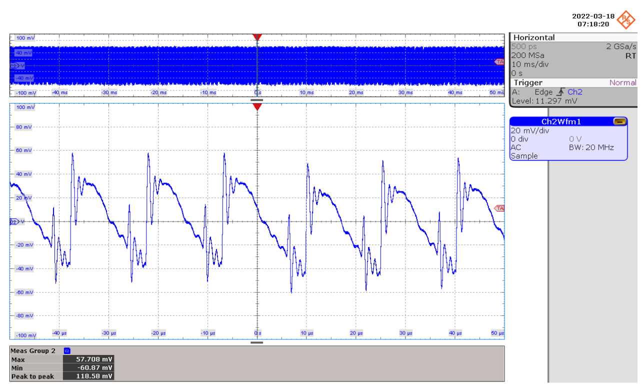
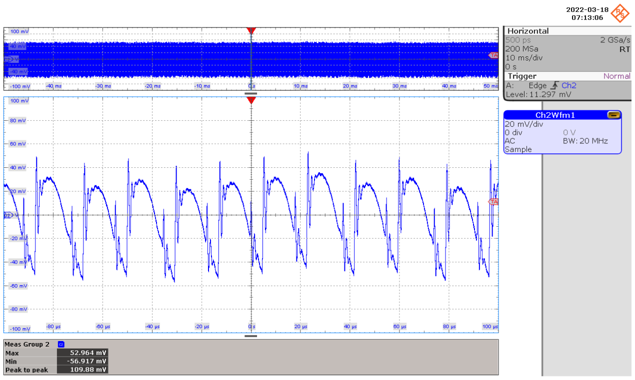


Figure 72 – 265 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 118.58 mV.

11.5.3 Output Ripple Voltage at V_{OUT} = 9 VDC / 5 A



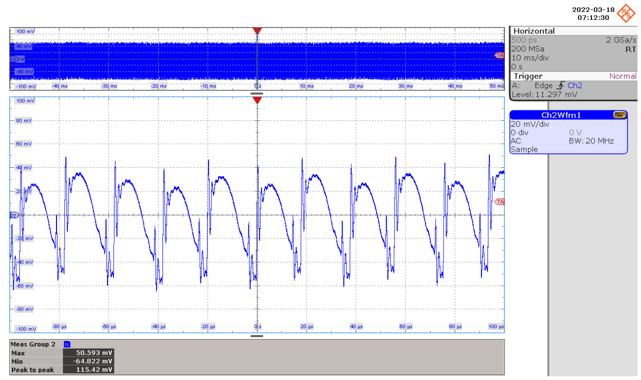
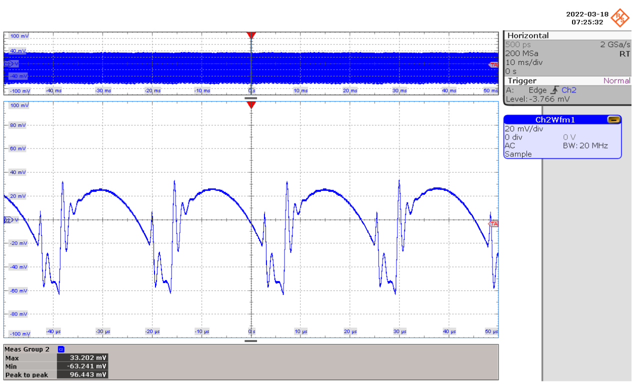


Figure 73 – 180 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 109.88 mV.

Figure 74 – 265 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 115.42 mV.

11.5.4 Output Ripple Voltage at V_{OUT} = 5 VDC / 6.5 A



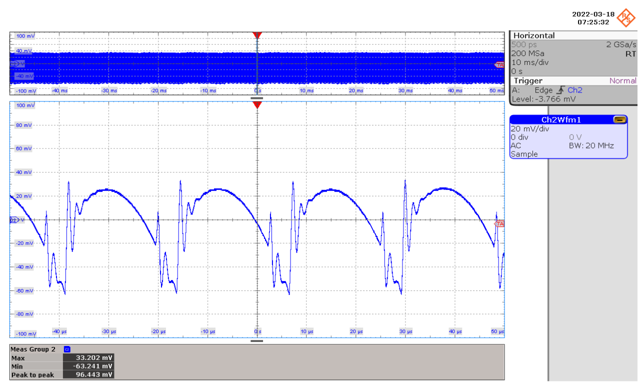


Figure 75 – 180 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 96.443 mV.

Figure 76 – 265 VAC 60 Hz, Full Load Normal.
Upper:V_{OUT}, 20 mV / div., 10 ms / div.
V_{RIPPLE} = 96.443 mV.

11.6 Output Short-Circuit

11.6.1 Output Short-Circuit

Waveforms are captured during the unit was running with an output shorted

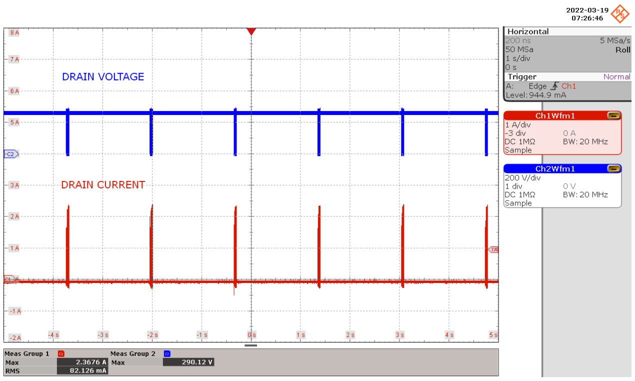


Figure 77 – 180 VAC 60 Hz, Output Short Normal.
CH1(Red): I_D, 1 A / div., 1 s / div.
CH2(Blue): V_D, 200 V / div.

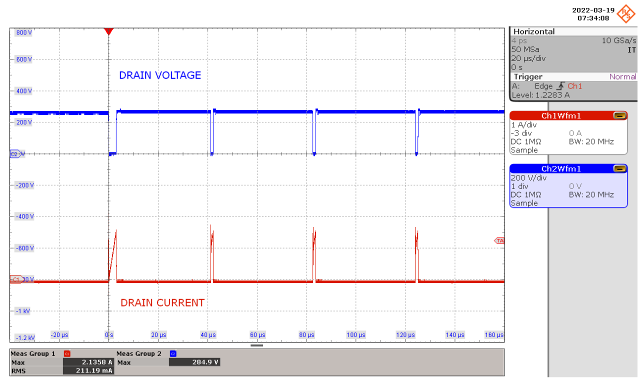


Figure 78 – 180 VAC 60 Hz, Output Short Normal.
Zoom in
CH1(Red): I_D, 1 A / div., 20 us / div.
CH2(Blue): V_D, 200 V / div.

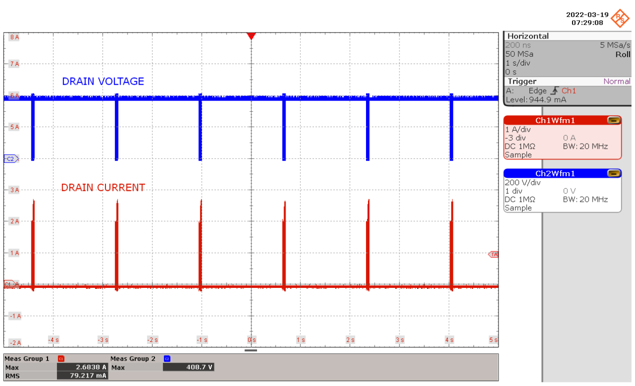


Figure 79 – 265 VAC 60 Hz, Output Short Normal.
CH1(Red): I_D, 1 A / div., 1 s / div.
CH2(Blue): V_D, 200 V / div.

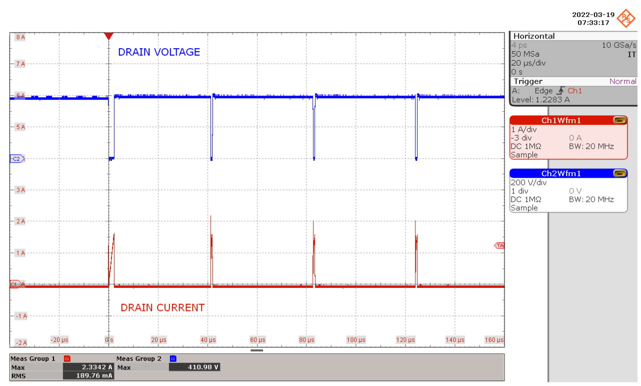


Figure 80 – 265 VAC 60 Hz, Output Short Normal.
Zoom in
CH1(Red): I_D, 1 A / div., 10 us / div.
CH2(Blue): V_D, 200 V / div.

11.6.2 Start Up with Output Shorted

Note: Unit was powered up with output shorted.

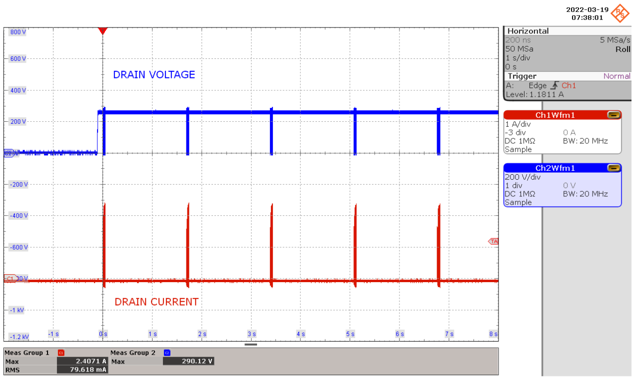


Figure 81 – 180 VAC 60 Hz, Short-Start-up.
CH1(Red): I_D, 1 A / div., 1 s / div.
CH2(Blue): V_D, 200 V / div.

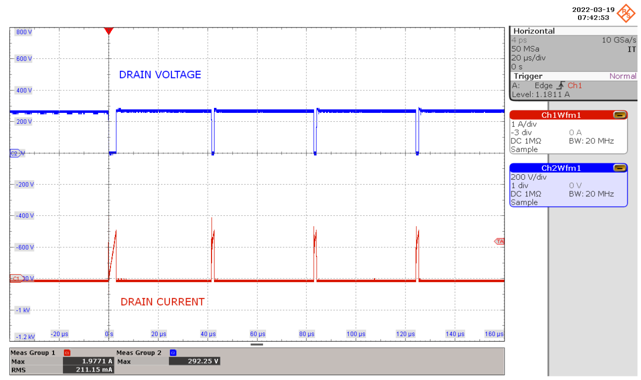


Figure 82 – 180 VAC 60 Hz, Short-Start-up.
Zoom in
CH1(Red): I_D, 1 A / div., 20 µs / div.
CH2(Blue): V_D, 200 V / div.

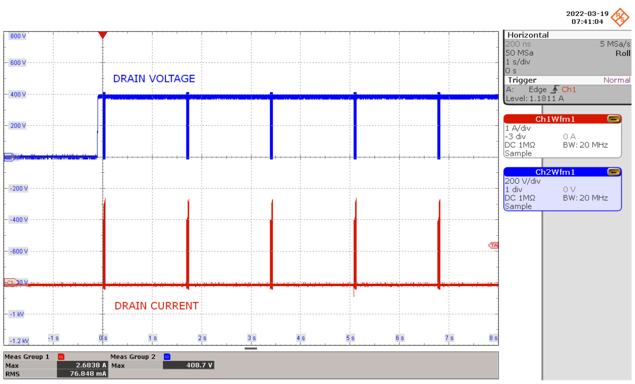


Figure 83 – 265 VAC 60 Hz, Short-Start-up
CH1(Red): I_D, 1 A / div., 1 s / div.
CH2(Blue): V_D, 200 V / div.

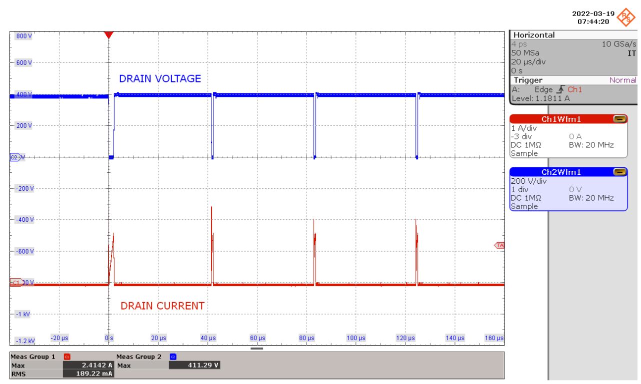


Figure 84 – 265 VAC 60 Hz, Short-Start-up.
Zoom in
CH1(Red): I_D, 1 A / div., 20 µs / div.
CH2(Blue): V_D, 200 V / div.

12 Conducted EMI

12.1 Test Set-up

EMI measurement was done using a resistor load.

12.2 Equipment and Load Used

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Variable Voltage Transformer set at 230 VAC

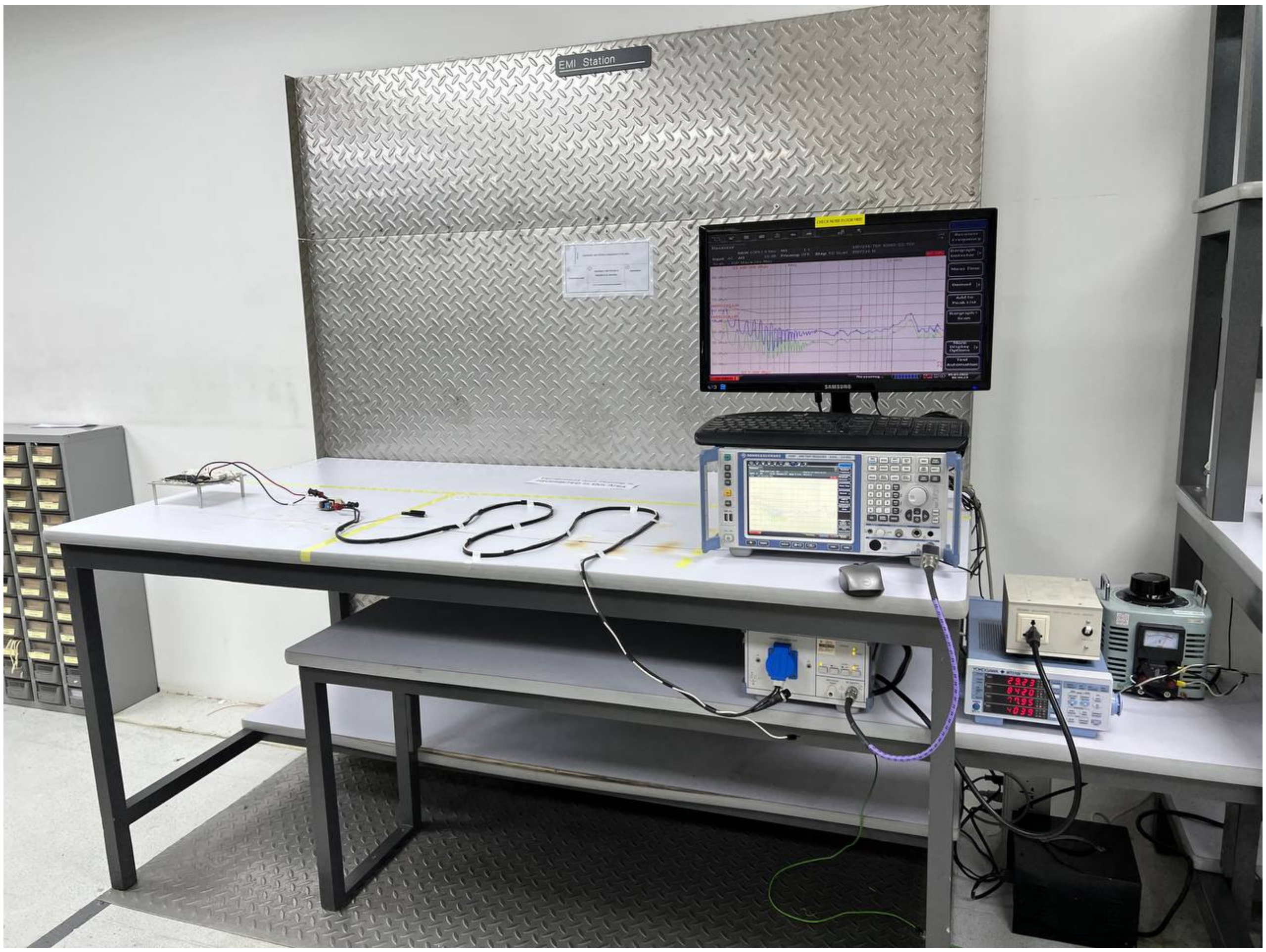


Figure 85 – Conducted EMI Test Set-up.

12.3 Conducted EMI at V_{OUT} = 20 V Full Load with Output Floating

12.3.1 Output Load: 5.71 Ω (20 V / 3.5 A) Fixed Resistor

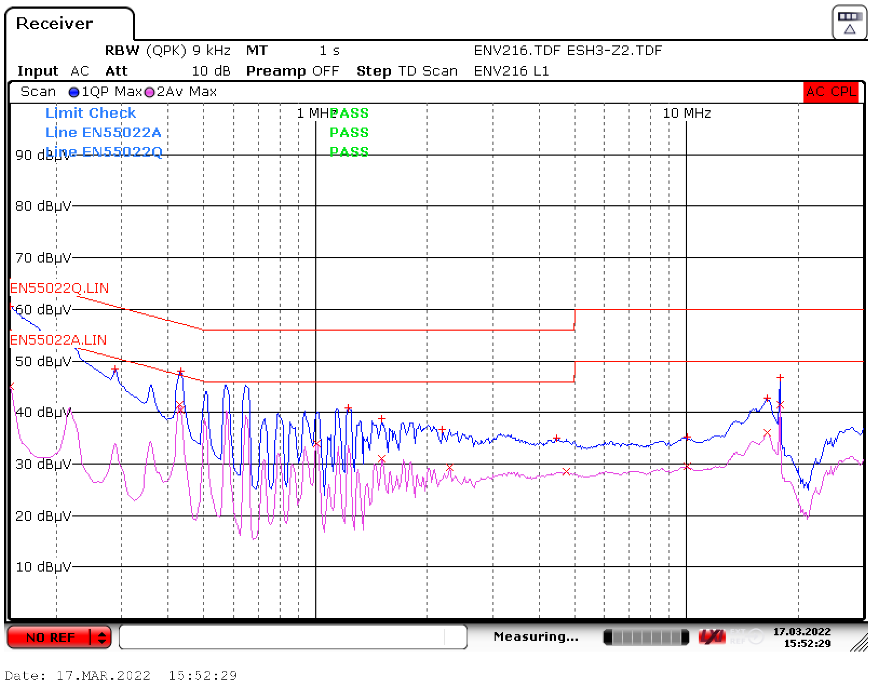


Figure 86 – Conducted EMI (LINE) at V_{OUT} = 20 V Full Load, 230 VAC 60 Hz, Floating Output

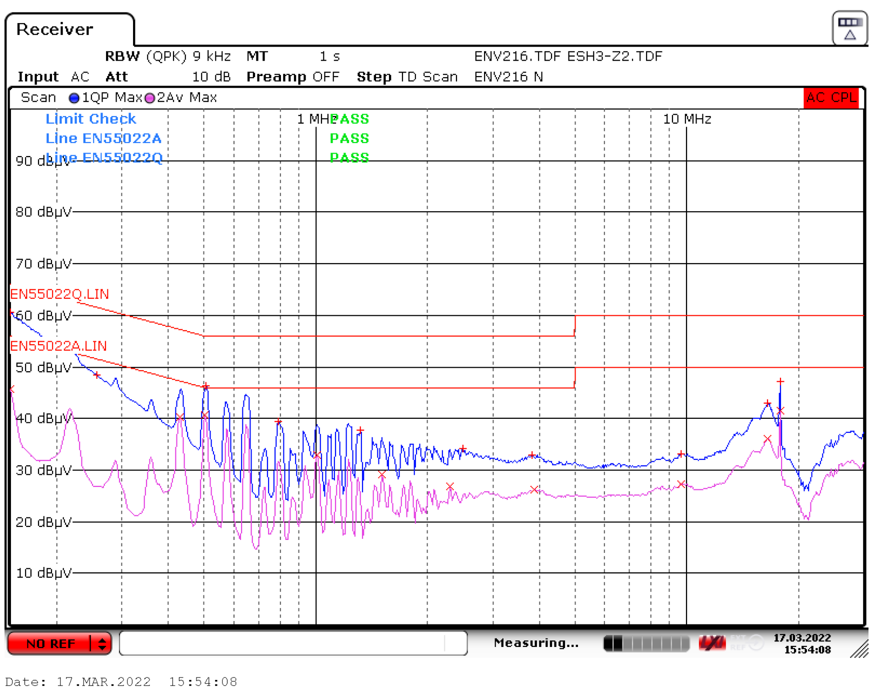


Figure 87 – Conducted EMI (NEUTRAL) at V_{OUT} = 20 V Full Load, 230 VAC 60 Hz, Floating Output

12.4 Conducted EMI at V_{OUT} = 15 V Full Load with Output Floating

12.4.1 Output Load: 3.75 Ω (15 V / 4 A) Fixed Resistor

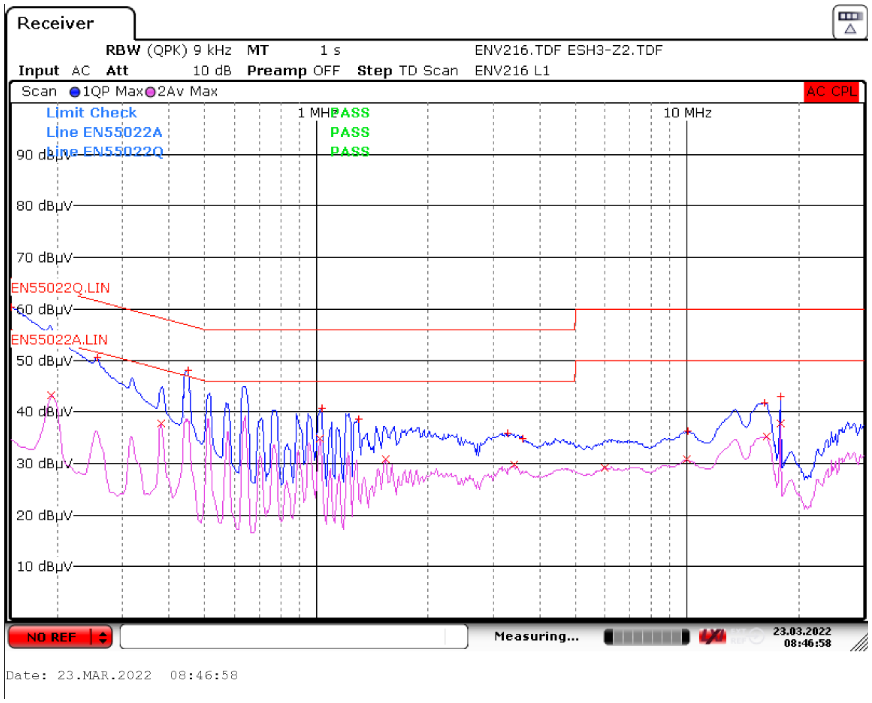


Figure 88 – Conducted EMI (LINE) at V_{OUT} = 15 V Full Load, 115 VAC 60 Hz, Floating Output

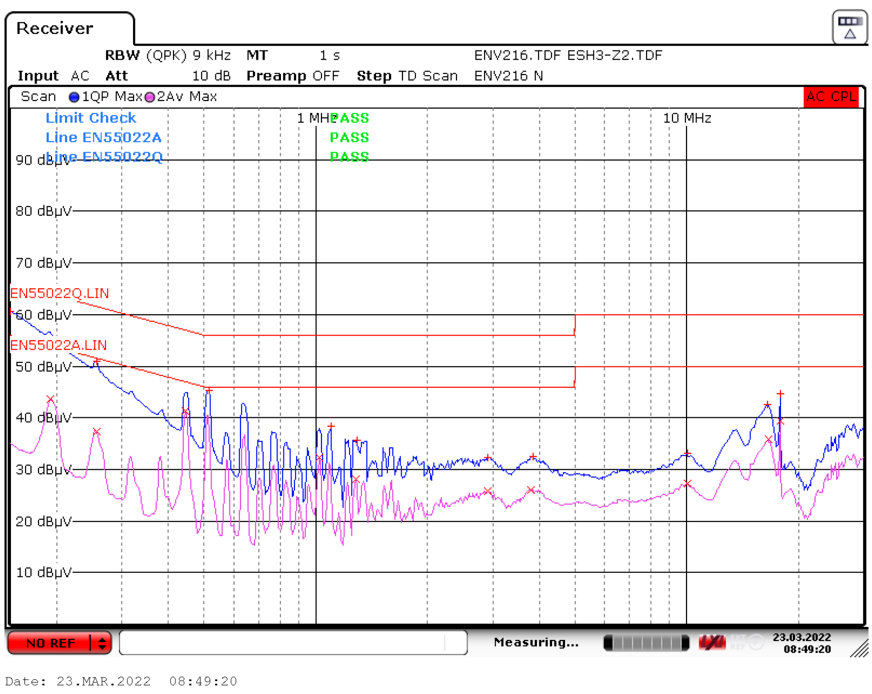


Figure 89 – Conducted EMI (NEUTRAL) at V_{OUT} = 15 V Full Load, 115 VAC 60 Hz, Floating Output

Conducted EMI at V_{OUT} = 9 V Full Load with Output Floating

12.4.2 Output Load: 1.8 Ω (9 V / 5 A) Fixed Resistor

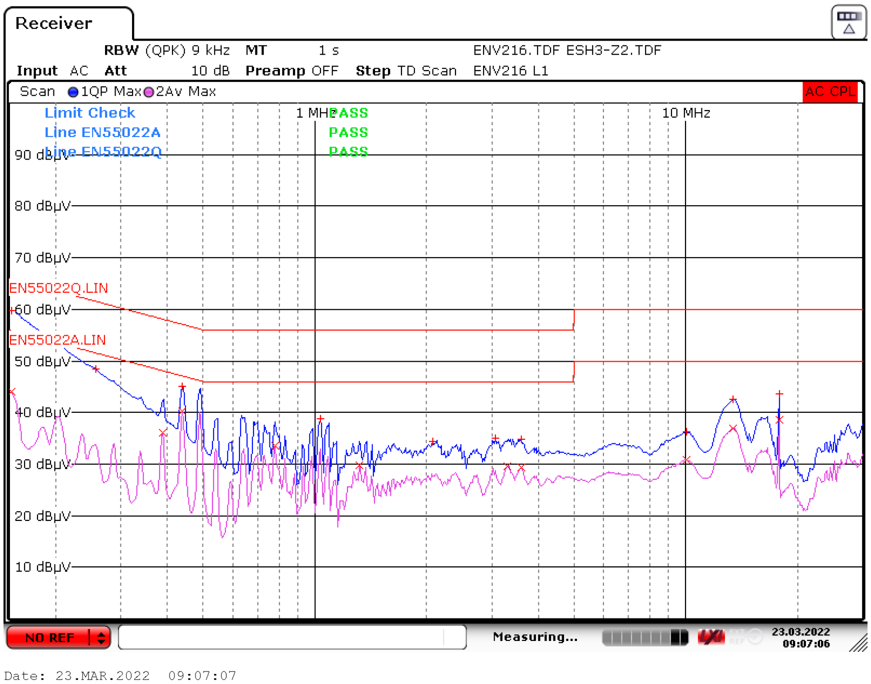


Figure 90 – Conducted EMI (LINE) at V_{OUT} = 9 V Full Load, 115 VAC 60 Hz, Floating Output

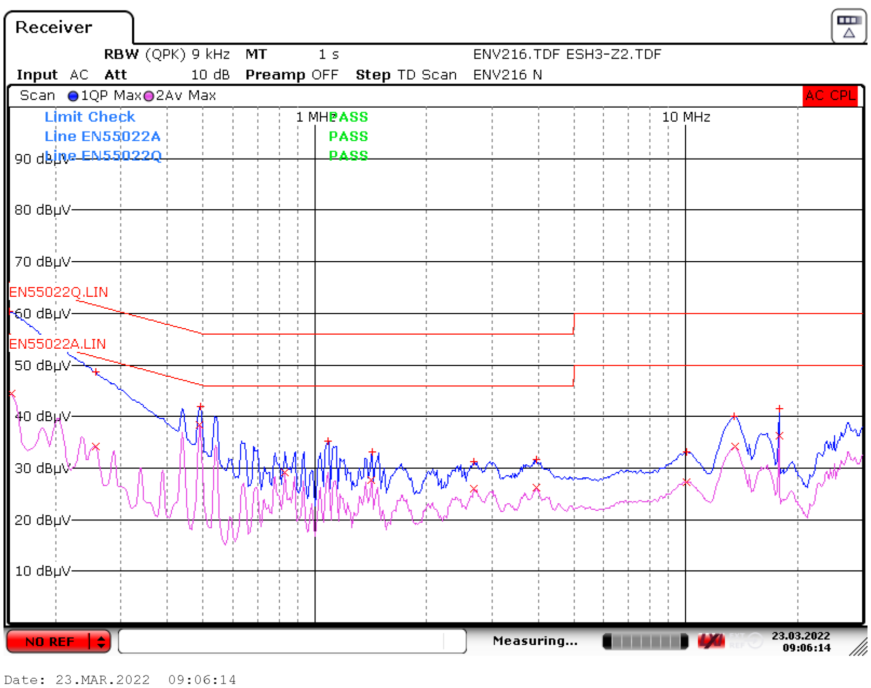


Figure 91 – Conducted EMI (NEUTRAL) at V_{OUT} = 9 V Full Load, 115 VAC 60 Hz, Floating Output

12.5 Conducted EMI at V_{OUT} = 5 V Full Load with Output Floating

12.5.1 Output Load: 0.77 Ω (5 V / 6.5 A) Fixed Resistor

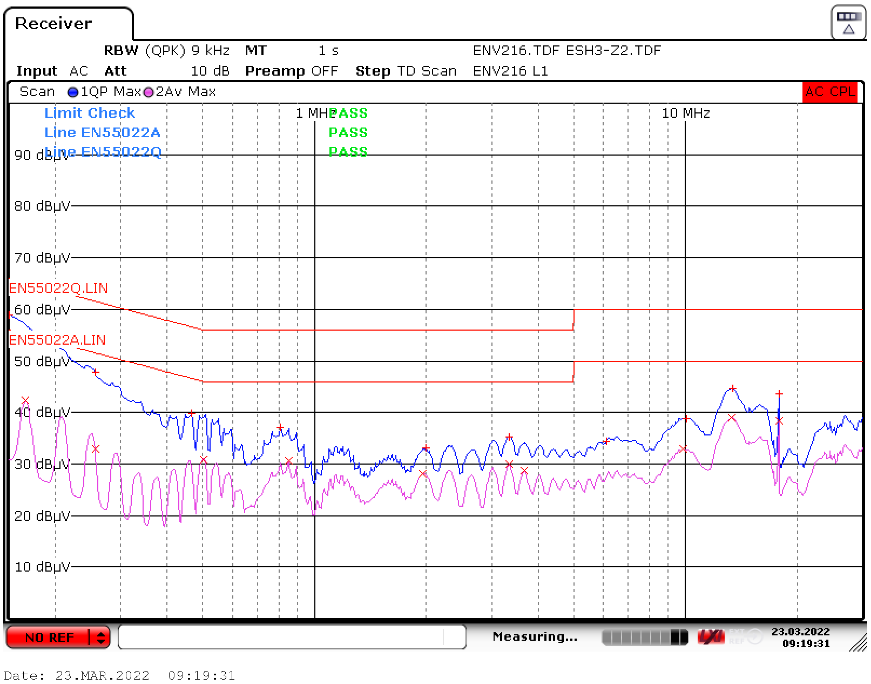


Figure 92 – Conducted EMI (LINE) at V_{OUT} = 5 V Full Load, 115 VAC 60 Hz, Floating Output

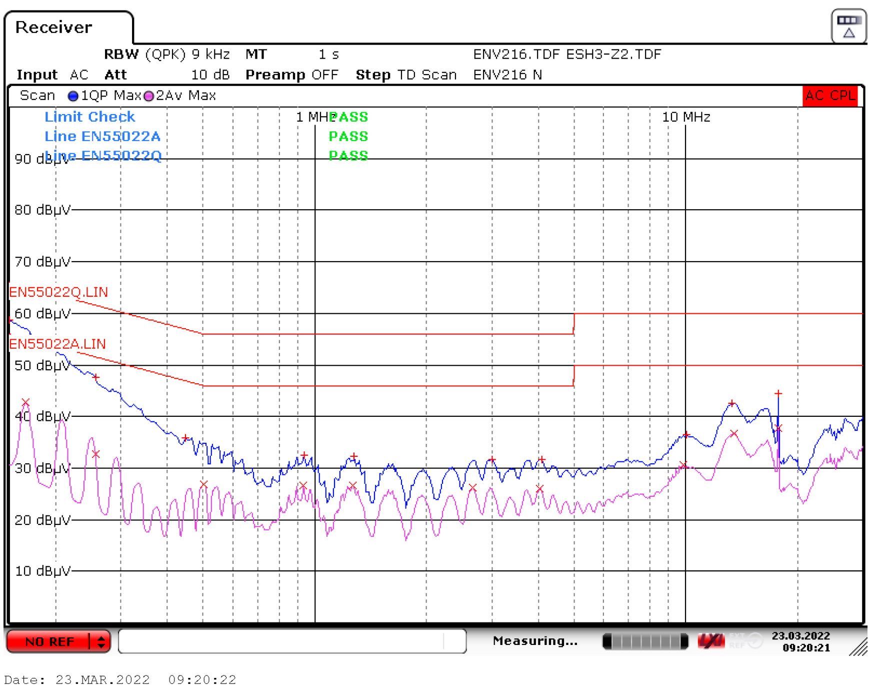


Figure 93 – Conducted EMI (NEUTRAL) at V_{OUT} = 5 V Full Load, 115 VAC 60 Hz, Floating Output

13 Line Immunity

Output Load set at max load (20 V / 3.5 A) using a 5.7 Ω fixed resistor

13.1 Differential Surge Test Results

Source Impedance: 2Ω
Repetition Rate: 1/30 s
No. of surge strike per location: 10 strikes

Differential Surge	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000 V	230	L to N	0	Pass / Class B
+2000 V	230	L to N	90	Pass / Class B
+2000 V	230	L to N	270	Pass / Class B
-2000 V	230	L to N	0	Pass / Class B
-2000 V	230	L to N	90	Pass / Class B
-2000 V	230	L to N	270	Pass / Class B

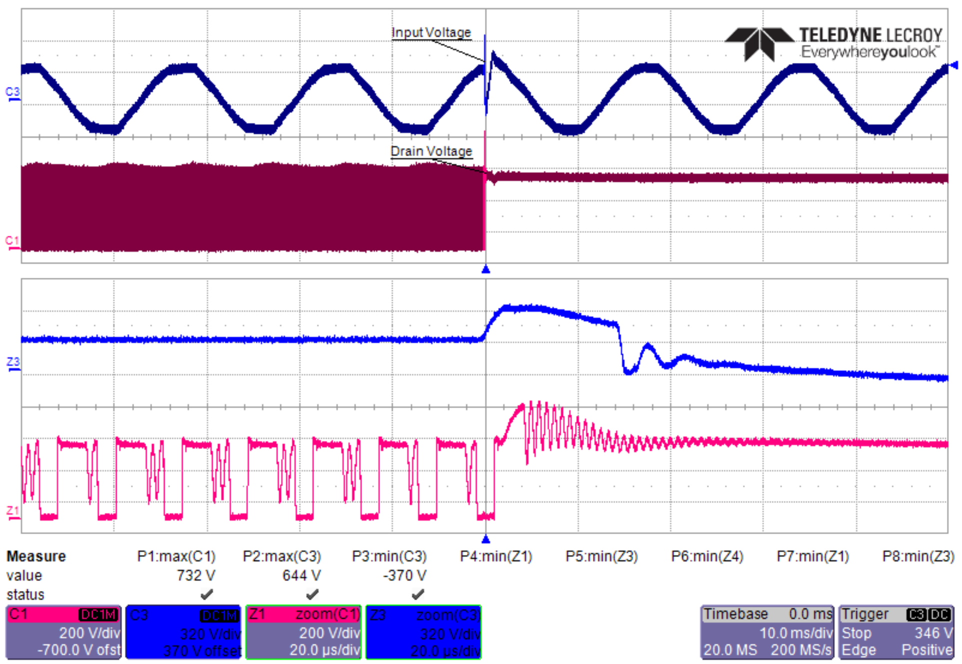


Figure 94 – 230 VAC 60 Hz, +2 kV Differential Surge L-N.
Injection Phase: 90º.
Upper: V_{IN}, 320 V / div.
Lower: V_{DRAIN}, 200 V / div., 20 µs / div.
V_{DS} = 732 V.

13.2 Ring Wave Surge Test Results

Source Impedance: 12Ω
Repetition Rate: 1/30 s
No. of surge strike per location: 10 strikes

Differential Ringwave Voltage	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500 V	230	L to N	0	Pass / Class A
+2500 V	230	L to N	90	Pass / Class A
+2500 V	230	L to N	270	Pass / Class A
-2500 V	230	L to N	0	Pass / Class A
-2500 V	230	L to N	90	Pass / Class A
-2500 V	230	L to N	270	Pass / Class A

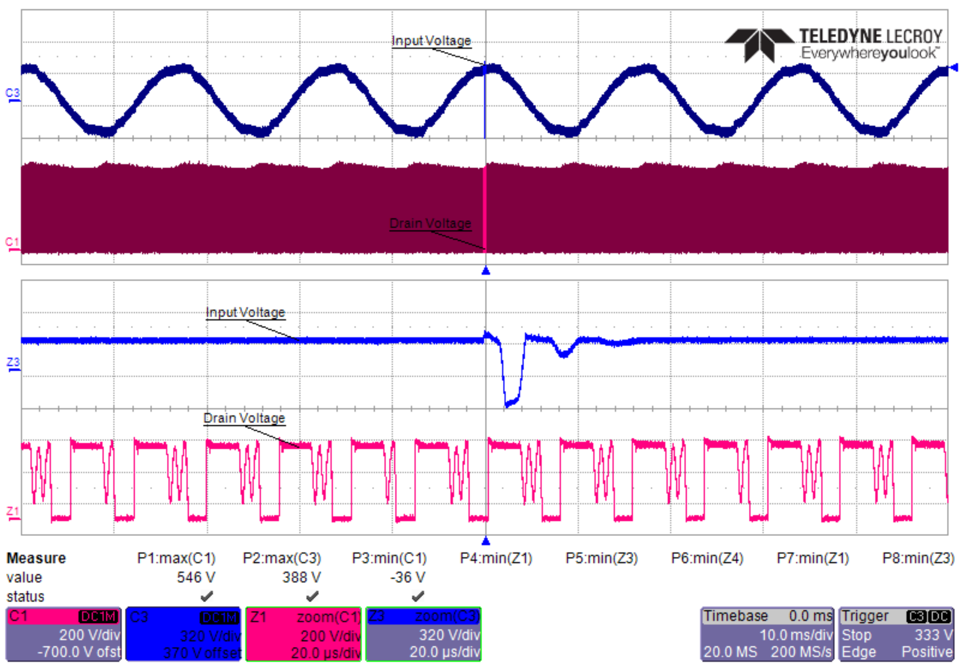


Figure 95 – 230 VAC 60 Hz, 2.5kV Ring Wave L-N.
Injection Phase: 90º.
Upper: V_{IN}, 320 V / div.
Lower: V_{DRAIN}, 200 V / div., 20 µs / div.
V_{DS} = 546 V.

13.3 Electrical Fast Transients (EFT) Test Results

Tested at 5 kHz and 100 kHz EFT Burst frequency. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.3.1 5 kHz EFT

Test Voltage (V)	Input Voltage (VAC)	Test Time (s)	Frequency (kHz)	Burst Duration (ms)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)	Remarks
2000	230	60	5	15	L to N	0	Pass	No AR/No damage
-2000	230	60	5	15	L to N	0	Pass	No AR/No damage
2000	230	60	5	15	L to N	90	Pass	No AR/No damage
-2000	230	60	5	15	L to N	90	Pass	No AR/No damage
2000	230	60	5	15	L to N	270	Pass	No AR/No damage
-2000	230	60	5	15	L to N	270	Pass	No AR/No damage
4000	230	60	5	15	L to N	0	Pass	No AR/No damage
-4000	230	60	5	15	L to N	0	Pass	No AR/No damage
4000	230	60	5	15	L to N	90	Pass	No AR/No damage
-4000	230	60	5	15	L to N	90	Pass	No AR/No damage
4000	230	60	5	15	L to N	270	Pass	No AR/No damage
-4000	230	60	5	15	L to N	270	Pass	No AR/No damage

13.3.2 100 kHz EFT

Test Voltage (V)	Input Voltage (VAC)	Test Time (s)	Frequency (kHz)	Burst Duration (μs)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)	Remarks
2000	230	60	100	750	L to N	0	Pass	No AR/No damage
-2000	230	60	100	750	L to N	0	Pass	No AR/No damage
2000	230	60	100	750	L to N	90	Pass	No AR/No damage
-2000	230	60	100	750	L to N	90	Pass	No AR/No damage
2000	230	60	100	750	L to N	270	Pass	No AR/No damage
-2000	230	60	100	750	L to N	270	Pass	No AR/No damage
4000	230	60	100	750	L to N	0	Pass	No AR/No damage
-4000	230	60	100	750	L to N	0	Pass	No AR/No damage
4000	230	60	100	750	L to N	90	Pass	No AR/No damage
-4000	230	60	100	750	L to N	90	Pass	No AR/No damage
4000	230	60	100	750	L to N	270	Pass	No AR/No damage
-4000	230	60	100	750	L to N	270	Pass	No AR/No damage

14 ESD

Unit was subjected to ±8 kV ESD contact discharge test and ±8 kV ESD to ±15 kV ESD air discharge test. An LED indicator connected across the resistor load was used to observe the output behavior during to ESD. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Note: Output Load set at max load (20 V / 3 A) using a 6.67 Ω Fixed Resistor

14.1 ESD Contact Discharge 20 V 3.5 A Output (End of Output Cable)

No.	Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Pass / Fail
1	+8.8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-8.8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass

14.2 ESD Contact Discharge 5 V 6.5 A Output (End of Output Cable)

No.	Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Pass / Fail
1	+8.8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-8.8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass

14.3 ESD Air Discharge 20 V 3.5 A Output (End of Output Cable)

No.	Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Pass / Fail
1	+8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	+12	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-12	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	+16.5	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-16.5	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass

14.4 ESD Air Discharge 5 V 6.5 A Output (End of Output Cable)

No.	Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Pass / Fail
1	+8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-8	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	+12	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-12	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	+16.5	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass
1	-16.5	10	+ Output Terminal End of cable	No Damage / No AR	Pass
2		10	- Output Terminal End of cable	No Damage / No AR	Pass

15 Brown-Out / Brown-Out Recovery Test

No abnormal overheating or voltage overshoot / undershoot was observed during and after 0.5 V / s. The unit works normally after the brown-out test.

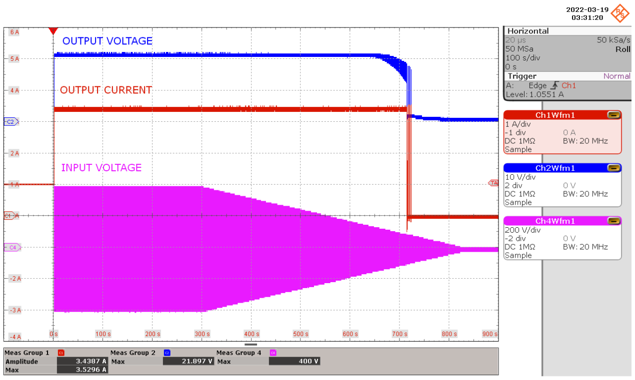


Figure 96 – Brown-Out at V_{OUT} = 20 V.
V_{IN} = 265 V – 0 V, Slew Rate = 0.5 V / s.
CH1(Red): I_{OUT}, 1 A / div., 100 s / div.
CH2(Blue): V_{out}, 10 V / div.
CH4(Pink): V_{IN}, 200 V / div.

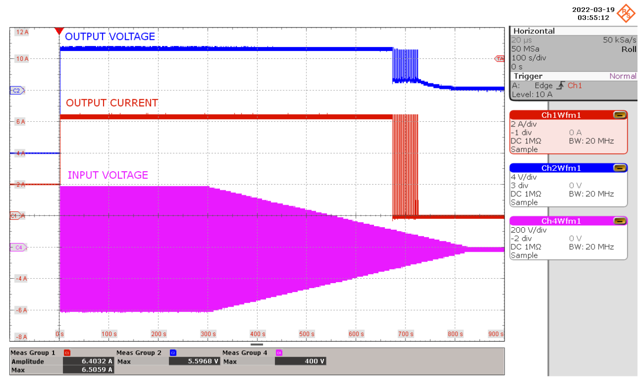


Figure 97 – Brown-in at V_{OUT} = 5 V.
V_{IN} = 0 V – 265 V, Slew Rate = 0.5 V / s.
CH1(Red): I_{OUT}, 2 A / div., 100 s / div.
CH2(Blue): V_{out}, 4 V / div.
CH4(Pink): V_{IN}, 200 V / div.

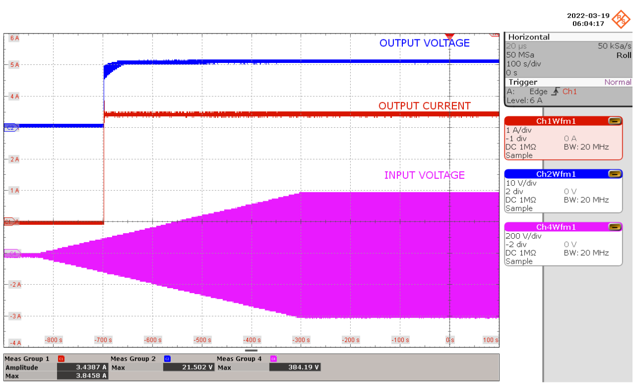


Figure 98 – Brown-Out at V_{OUT} = 20 V.
V_{IN} = 265 V – 0 V, Slew Rate = 0.5 V / s.
CH1(Red): I_{OUT}, 1 A / div., 100 s / div.
CH2(Blue): V_{out}, 10 V / div.
CH4(Pink): V_{IN}, 200 V / div.

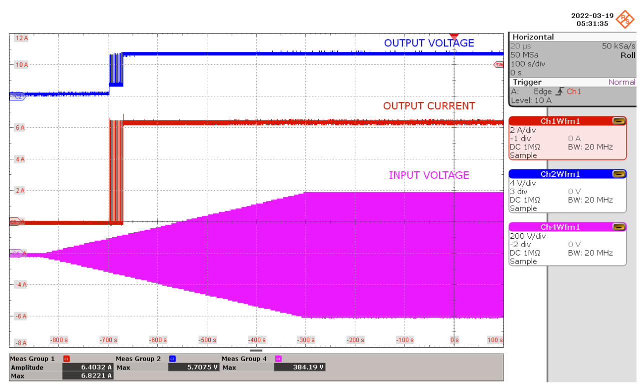


Figure 99 – Brown-in at V_{OUT} = 5 V.
V_{IN} = 0 V – 265 V, Slew Rate = 0.5 V / s.
CH1(Red): I_{OUT}, 2 A / div., 100 s / div.
CH2(Blue): V_{out}, 4 V / div.
CH4(Pink): V_{IN}, 200 V / div.

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
10-Nov-22	JEE	1.0	Initial release	Apps & Mktg

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