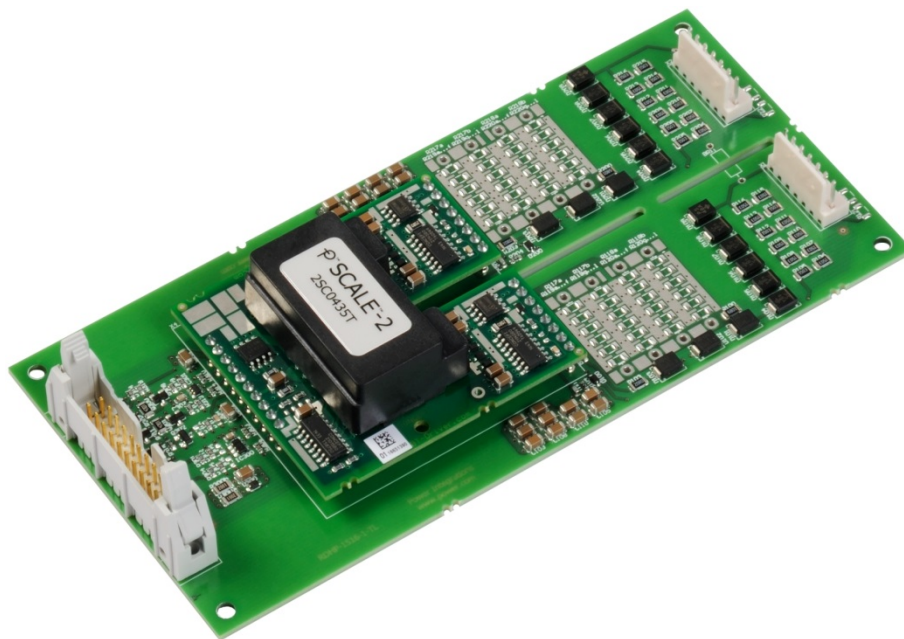


General Purpose Base Board for Gate Driver Core 2SC0435T

Application	General purpose drives, traction, solar power and others
Specification	Suitable for IGBT power modules in various housings Up to 1200V DC-link voltage Electrical interfaces Advanced Active Clamping Short-circuit detection
Author	High-Power Application Engineering Department
Document Number	RDHP-1516
Revision¹	A.4



¹ The letter refers to the hardware revision. The number refers to the documentation revision.

Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1700V
- Advanced Active Clamping
- Short-circuit detection
- Electrical command inputs and status outputs
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Direct or Half-Bridge mode selection
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done

Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0435T gate driver family is recommended.

Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR03) package can be selected.

Turn-on gate resistors:

Channel	SMD Package	THT Package
1	R119a ... R119l	R117a, R117b
2	R219a ... R219l	R217a, R217b

Turn-off gate resistors:

Channel	SMD Package	THT Package
1	R120a ... R120l	R118a, R118b
2	R220a ... R220l	R218a, R218b

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0435T.

V_{CEsat} Monitoring

In the schematic and bill of material, the resistor networks of the V_{CEsat} monitoring function are marked with "N.A." (not assembled), as their concrete value depends on the IGBT power module and applied DC-link voltage.

Recommended values are listed in the following table:

IGBT voltage	Max. DC-link voltage	R104	R105 to R116	R204	R205 to R216
1200V	800V	120k Ω	100k Ω	120k Ω	100k Ω
1700V	1200V	120k Ω	150k Ω	120k Ω	150k Ω

Recommended values of the blanking capacitors C100 and C200 as well as further details of the V_{CEsat} monitoring function are described in the corresponding application manual of the gate driver 2SC0435T.

Soft Shut Down (SSD)

For this design proposal no dedicated Soft Shut Down function is implemented. Instead, for over voltage protection Advanced Active Clamping is implemented.

Advanced Active Clamping

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic Active Clamping topologies

implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate.

Advanced active clamping topologies implement the same structure as basic active clamping topologies, but in addition a fraction of the active clamping current is fed into the gate driver core at pins ACLx via 20Ω resistors. In this case, when active clamping is activated, the turn-off MOSFET of the 2SC0435T driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping – is mainly integrated in the secondary-side ASIC of gate driver core 2SC0435T.

In the schematic and bill of material, the TVS networks (D104 to D109 and D204 to D209) are marked with "N.A." (not assembled), as their specific value depends on the IGBT power module and applied DC-link voltage. Recommended values are listed in the following tables.

IGBT voltage	Max. DC-link voltage	D101, D201	D104 ... D108, D204 ... D208	D109, D209
600V	400V	STPS340U	P6SMJ70A	P6SMBJ70CA
1200V	800V	STPS340U	SMBJ130A-E3	SMBJ130CA-E3
1700V	1200V	STPS340U	P6SMB220A	P6SMB220CA

For further details and alternative TVS diodes refer to the application manual of the gate driver core 2SC0435T.

Minimum Pulse Suppression

This design possesses the option to implement a minimum pulse suppression with a time constant τ . If required the minimum pulse suppression can be set by adjusting C305 and C306. The time constant τ is given by the following equations:

$$\tau_1 = 0.88\text{k}\Omega \cdot C305$$

$$\tau_2 = 0.88\text{k}\Omega \cdot C306$$

Recommended values of C305 and C306 are in the range of 100pF ($\tau_x = 88\text{ns}$) to 470pF ($\tau_x = 414\text{ns}$), depending on actual application conditions.

Blocking Time

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

The terminal TB allows the default blocking time of typically 99ms (R319) to be reduced by connecting an optional external resistor to GND. The external resistor R_b needs to be equal or larger than 129kΩ to fulfill the following formula:

$$(R_b + 6.8\text{k}\Omega) \parallel 150\text{k}\Omega \triangleq T_b + 51\text{ms} \text{ with } 20\text{ms} < T_b < 99\text{ms}$$

In case the terminal TB is directly shorted to GND ($R_b = 0\Omega$), the blocking time is set to its minimum value as described in the datasheet of the gate driver core 2SC0435T.

Interfaces

Electrical Interfaces

X3		
Pin	Designation	Description
1	VDC	15V supply (referenced to GND)
3	VDC	15V supply (referenced to GND)
5	VCC	15V supply (referenced to GND)
7	VCC	15V supply (referenced to GND)
9	SO2	Status output channel 2
11	INB	Command input channel 2
13	SO1	Status output channel 1
15	INA	Command input channel 1
17	MOD	Mode selector
19	TB	Set blocking time

X3		
Pin	Designation	Description
2	GND	Ground
4	GND	Ground
6	GND	Ground
8	GND	Ground
10	GND	Ground
12	GND	Ground
14	GND	Ground
16	GND	Ground
18	GND	Ground
20	GND	Ground

X1		
Pin	Designation	Description
1	C1	Collector channel 1
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	n.c.	Not connected
6	G1	Gate channel 1
7	VE1	Emitter channel 1

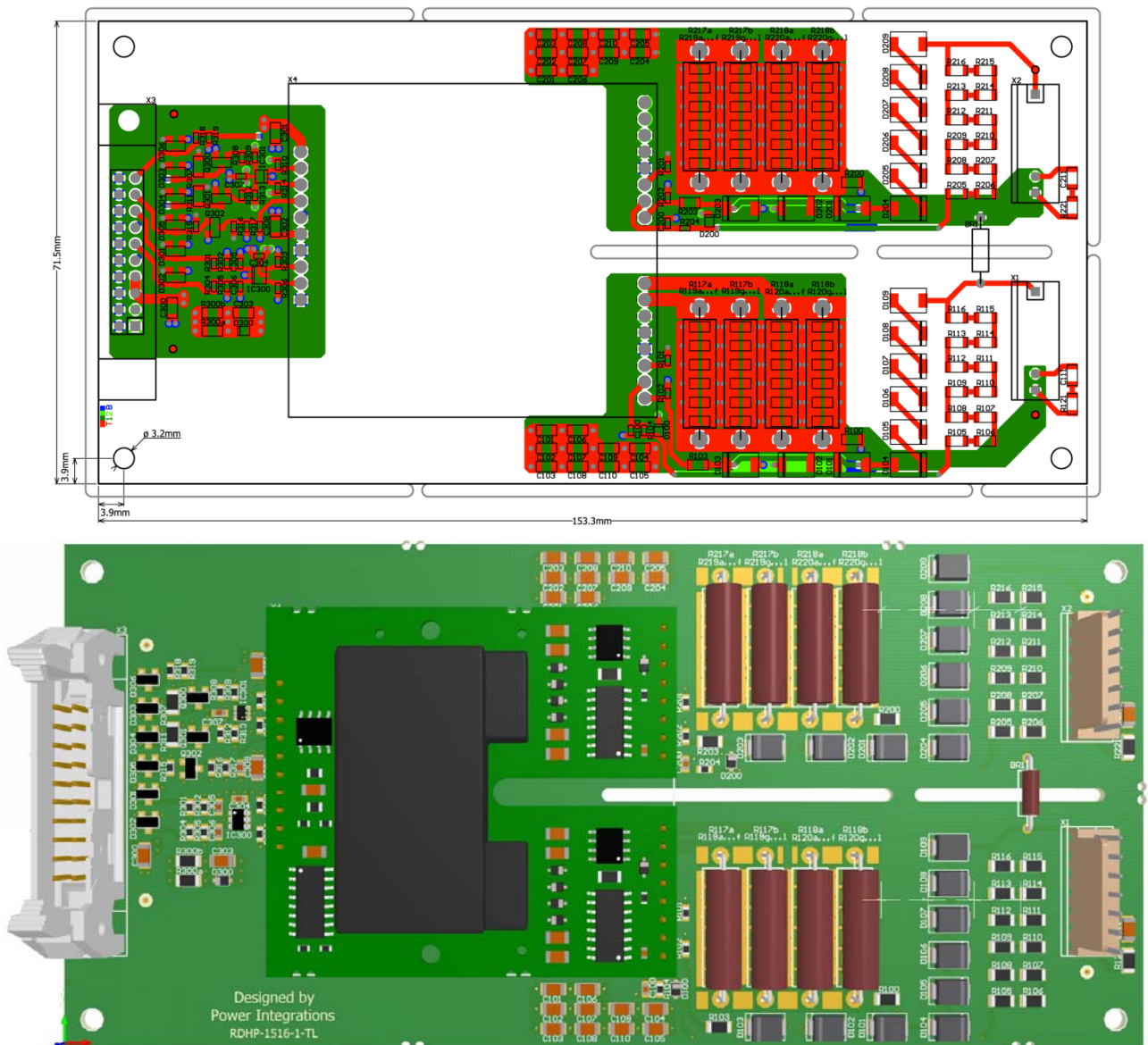
X2		
Pin	Designation	Description
1	C2	Collector channel 2
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	n.c.	Not connected
6	G2	Gate channel 2
7	VE2	Emitter channel 2

CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm (for gate driver cores with terminal length of 2.54mm) and 2.0mm (for gate driver cores with terminals length ≥ 3.1 mm).



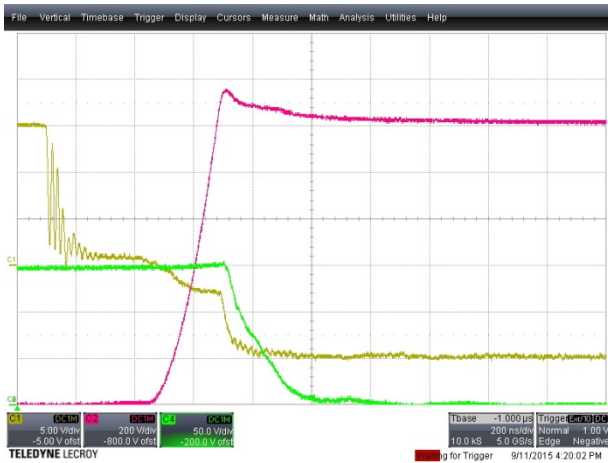
Switching Characteristic

Turn-On/Off

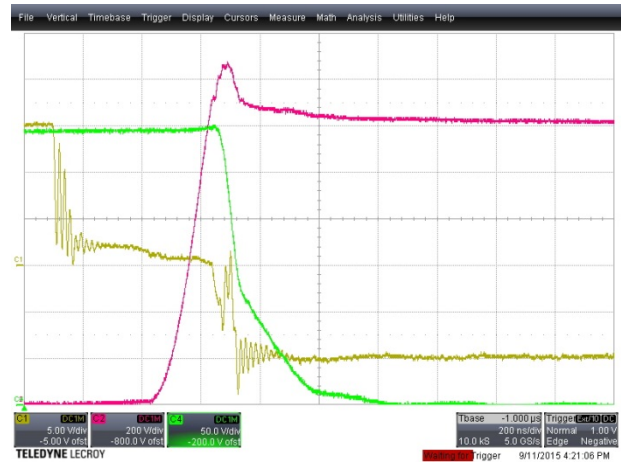
The measurement examples shown with the IGBT power module FF150R17KE4 from Infineon Technologies ($R_{Gon} = 4.7\Omega$ and $R_{Goff} = 4.7\Omega$) were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of $1200V_{DC}$. The adjusted load current is either $150A$ (I_{nom}) or $300A$ ($2x I_{nom}$).

Channel assignment:

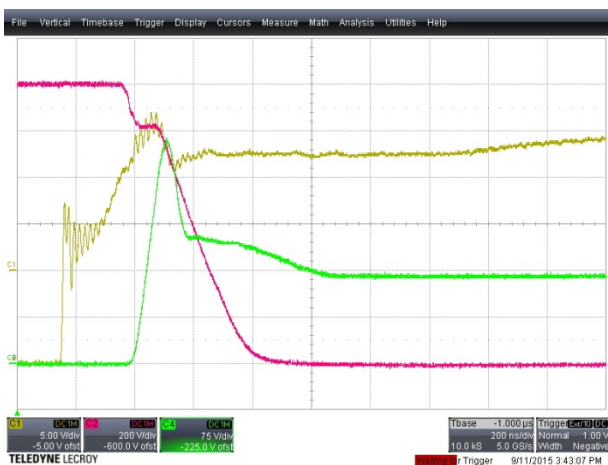
- Channel C1: Gate-emitter voltage
- Channel C2: Collector-emitter voltage
- Channel C3: Collector current ($1V \cong 1A$)



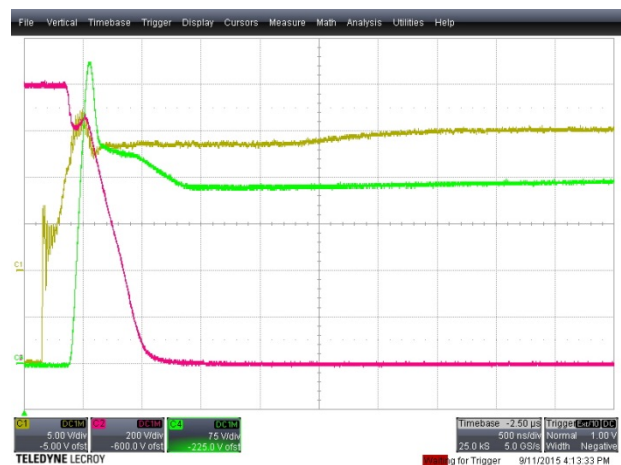
Turn-off bottom side (I_{nom})



Turn-off bottom side ($2x I_{nom}$)



Turn-on bottom side (I_{nom})



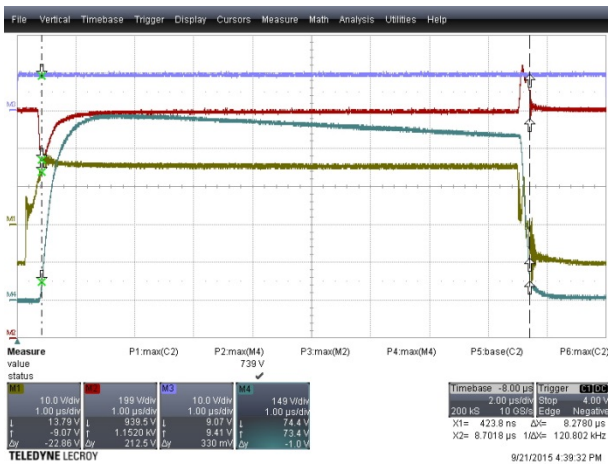
Turn-on bottom side ($2x I_{nom}$)

Short-Circuit

The measurement example shown with the IGBT power module FF150R17KE4 from Infineon Technologies ($R_{Gon} = 4.7\Omega$ and $R_{Goff} = 4.7\Omega$) was carried out at room temperature with an initial DC-link voltage of $1200V_{DC}$.

Channel assignment:

- Channel M1: Gate-emitter voltage
- Channel M2: Collector-emitter voltage
- Channel M3: Command input signal
- Channel M4: Collector current ($1V \triangleq 1A$)



Bottom side

Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

- /1/ 2SC0435T2xx-17 Data Sheet, Power Integrations
- /2/ 2SC0435T2xx-17 Description & Application Manual, Power Integrations
- /3/ Application Note AN-0902, "Avoiding ESD with CONCEPT Drivers", Power Integrations

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