

DI-57 Design Idea DPA-Switch®

60 W DC-DC Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Telecom	DPA426R	60 W	36 – 75 VDC	12 V	Flyback

Design Highlights

- Low cost 400 kHz flyback design
- Simple Zener referenced 12 V output
- Efficiency – 82% at 36 VDC and full load
- Low component count
- Accurate line OV and UV protection
- Thermal, short circuit and output overload protection
- No current sense components

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. Resistor R1 programs the under/over voltages and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Resistor R3 programs the DPA-Switch current limit at 85% of nominal to minimize fault and overload power. Drain voltage clamping is provided by diode D4 and Zener diode VR1 with optional components C4 and R2 to provide high frequency snubbing.

The output is rectified by diode D2 with optional high frequency damping from components C9, R15 and R16. The output capacitors are alternated to share the ripple current evenly between the Oscon capacitors (C10-C14) and the ceramic capacitors (C15-C18). A final decoupling ceramic capacitor C19 is placed at the output pins of the power supply.

Output regulation is taken from the +12 V output. Zener diode VR2 is DC-biased by resistor R7 with the opto-diode of U2 providing feedback and resistor R6 programming the gain. Optional capacitor C8 implements a soft-finish network to slow the rise of the output voltage at start-up.

The bias winding is rectified and filtered by D1 and C23 and provides operating power to the DPA-Switch. The regulation is fed back from the secondary through the opto-transistor of U2.

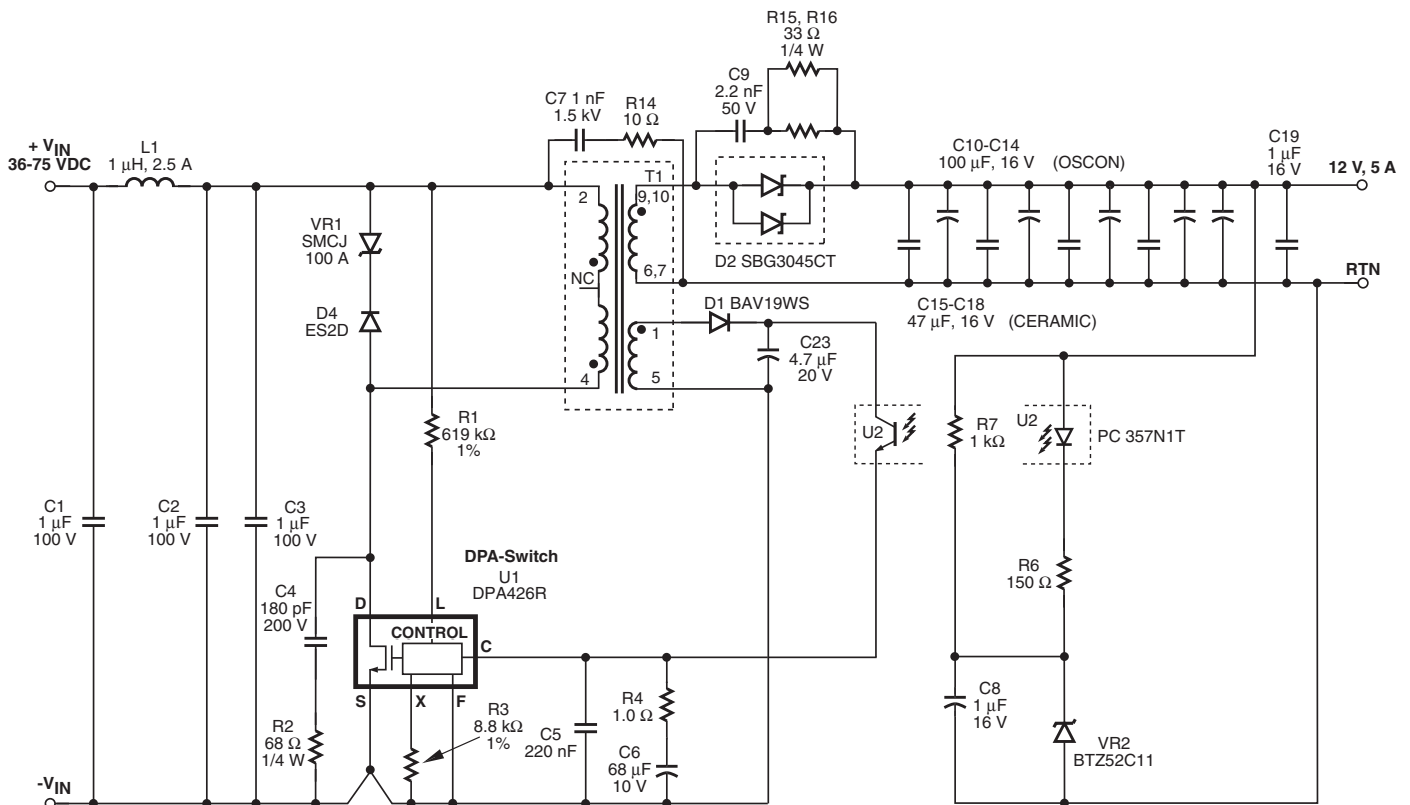


Figure 1. 60 W, 12 V, 5 A, DC-DC Converter.

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Key Design Points

- For the nominal under-voltage set point V_{UV} :
 $R1 = (V_{UV} - 2.35) / 50 \mu A$
 $V_{OV} = (R1 \times 135 \mu A) + 2.5 V$
- For highest efficiency designs: use continuous conduction mode operation, this design uses approximately 0.5 KRP; minimize turns in the transformer and at this (60 W) power level, keep AC flux density $B_M < 1100$ Gauss; fully fill a single layer for each winding to minimize leakage inductance and maximize copper fill factor; if possible use a Schottky rectifier diode (D2) with a low-forward drop.
- The transformer primary is split in order to minimize leakage inductance to obtain better efficiency.
- Tighter output voltage tolerance is possible by using a TL431 (and associated components) in place of the Zener diode VR2.
- Follow good layout practices:
 - For length of the secondary current loop from transformer pins 9 & 10, diode D2 and capacitors C10 to C18 and back to pins 6 & 7 of the transformer: ensure identical path length for each of the capacitors C10 to C18 to ensure they equally share the ripple current.

Transformer Parameters

Core Material	Ferroxcube P/N: EFD25 3F3
Bobbin	10-pin EFD25 surface mount bobbin
Winding Details	Primary: 8T + 8T, 2 × 24 AWG Bias: 5T, 1 × 34 AWG +12 V: 5T, 4 × 27 AWG
Winding Order (pin numbers)	Primary-1 (4-NC), Bias (1-5), +12 V (9,10-6,7), Primary-2 (NC-2)
Primary Inductance	21 $\mu H \pm 25\%$ (at 400 kHz)
Primary Resonant Frequency	3.0 MHz (minimum)
Leakage Inductance	1 μH (maximum)

Table 1. Transformer Parameters. (AWG = American Wire Gauge, NC = No Connection)

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