Design Example Report

Title	***10 W Isolated Power Supply with Lossless Generation of AC Zero Crossing Signal and X Capacitor Discharge Using LinkSwitch™-TNZ LNK3317D***
Specification	90 VAC – 305 VAC Input, 12 V / 0.75 A and 5 V / 0.2 A Outputs
Application	Home Appliance and Industrial Power
Author	Applications Engineering Department
Document Number	DER-879
Date	March 29, 2021
Revision	1.0

Summary and Features

- Highly integrated solution with LNK3317D
- Low-component count with integrated 725 V power MOSFET, current sensing and protection
- Wide-range AC input
- Meets all existing and proposed energy efficiency standards including ErP
- No-load consumption <30 mW across AC line
- More than 300 mW available in stand-by while meeting 500 mW max input power
- Isolated zero crossing signal output synchronized to AC line
- X capacitor discharge
- Meets EN550022 and CISPR-22 Class B conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes an isolated flyback converter designed to provide dual output voltages at 12 V and 5 V from a wide input voltage range of 90 VAC to 305 VAC, as well as a zero crossing detection (ZCD) signal, and X capacitor discharge. X capacitor is typically not required at this power level but included in this design to demonstrate the X capacitor discharge function when using LinkSwitch-TNZ as an auxiliary power supply in a higher power application. This power supply utilizes the LNK3317D from the LinkSwitch-TNZ family of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

Figure 1 – Populated Circuit Board, Top View.

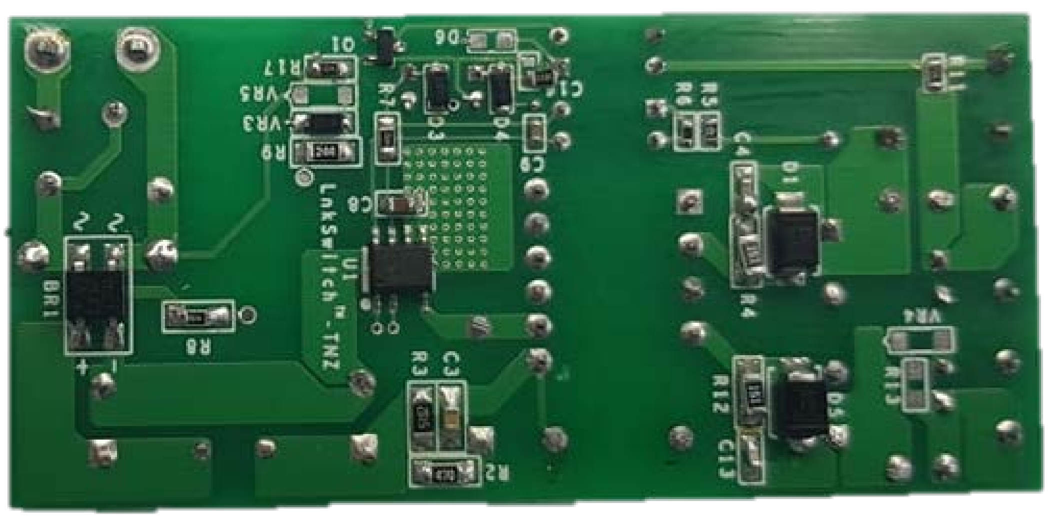

Figure 2 – Populated Circuit Board, Bottom View.

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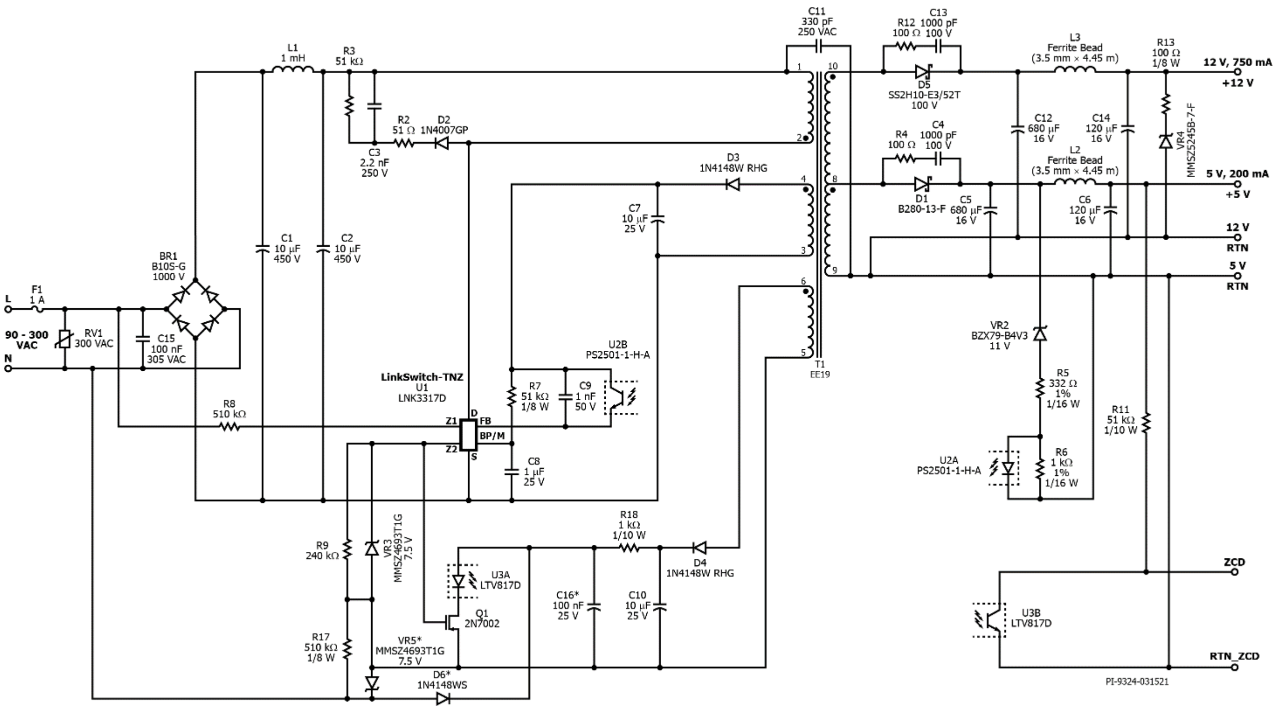
2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		305	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
No-load Input Power				25	mW	230 VAC.
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	± 5%.
Output Current 1	I_{OUT1}	20	200		mA	
Output Voltage 2	V_{OUT2}	10.8	12	13.2	V	± 10%.
Output Current 2	I_{OUT2}	75	750		mA	
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz Bandwidth.
Total Output Power						
Continuous Output Power	P_{OUT}		10		W	
Efficiency						
Full Load	η		77		%	Measured at P_{OUT} 25 °C.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC 60950, UL 60950-1				
Surge			1		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Surge: 2 Ω.
Ring Wave			2.5		kV	Ring Wave: 12 Ω.

3 Schematic



*Optional component.

Figure 3 – Full Schematic.

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4 Circuit Description

This circuit is configured as a flyback topology power supply utilizing the LNK3317D.

4.1 *Input Rectifier and Filter*

Input fuse F1 provides safety protection from component failures. Varistor RV1 acts as a voltage clamp that limits the voltage spike across the DC bus during line transient surge events. The AC input voltage is rectified by input bridge BR1. The rectified DC is then filtered by the bulk storage capacitors C1 and C2. Inductor L1, C1 and C2 form an input pi filter, which attenuates differential mode conducted EMI. Capacitor C15 is an optional component added on this design to demonstrate X capacitor discharge function in the LNK3317D IC. It also provides additional EMI attenuation.

4.2 *LNK3317 Operation*

The LNK3317D device U1 integrates the power switching device, oscillator, control, start-up, and protection functions.

The rectified and filtered input voltage is applied to the primary winding of T1. One side of the power transformer (T1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN (D) pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, delivering energy from bulk capacitor to transformer. When that current reaches the limit threshold, the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy is delivered to the output capacitor during off time.

When the power MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consists of D2, C3, R2 and R3. Resistor R2 and R3 not only damp the high frequency leakage ring that occurs when the power MOSFET turns off, but also limit the reverse current through D1 and D5 when the power MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of ≤2 μs.) to be used for D2. The slow diode also improves conducted EMI and efficiency.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to FB pin. The FB pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the FB pin current is <49 μA, the next switching cycle begins, and is terminated when the current through the power MOSFET reaches the internal current limit threshold.

4.3 *Output Rectification and Filtering*

Output rectification is provided by D1 for the 5 V output and D5 for the 12 V output. Low ESR capacitors C5, C6, C12 and C14 achieve minimum output voltage ripple and noise in a small can size for the rated ripple current specification. For each output, a post filter that include ferrite beads L2 and L3 attenuates noise and ripple further to meet the ripple specification.

4.4 *Feedback and Output Voltage Regulation*

In this dual output power supply, only the 5 V output is regulated. The 12 V winding is placed in series with the 5 V winding. The supply's output voltage regulation set point is set by the voltage that develops across Zener diode VR2, R5 and the LED in optocoupler U2. The value of R6 was calculated to bias VR2 to about 0.5 mA when it goes into reverse avalanche conduction. This ensures that it is operating close to its rated knee current. Resistor R5 limits the maximum current during load transients. The values of R5 and R6 can both be varied slightly to fine-tune the output regulation set point. When the output voltage rises above the set point, the LED in U2 becomes forward biased. On the primary-side, the photo-transistor of U2 turns on and injects current into the FB pin of U1. Just before the start of each switching cycle, the controller checks the FB pin current. If the current flowing out of the EN/UV pin is greater than 49 μA, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point.

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4.5 *Zero Crossing Detection*

In this application, Z1 and Z2 pins are utilized to generate a zero crossing signal and provide X capacitor discharge for C15.

In this design, provision is made for two different circuit configurations of zero crossing detection. Each configuration and corresponding schematic are explained in detail next.

4.5.1 Zero Crossing Detection with Bias

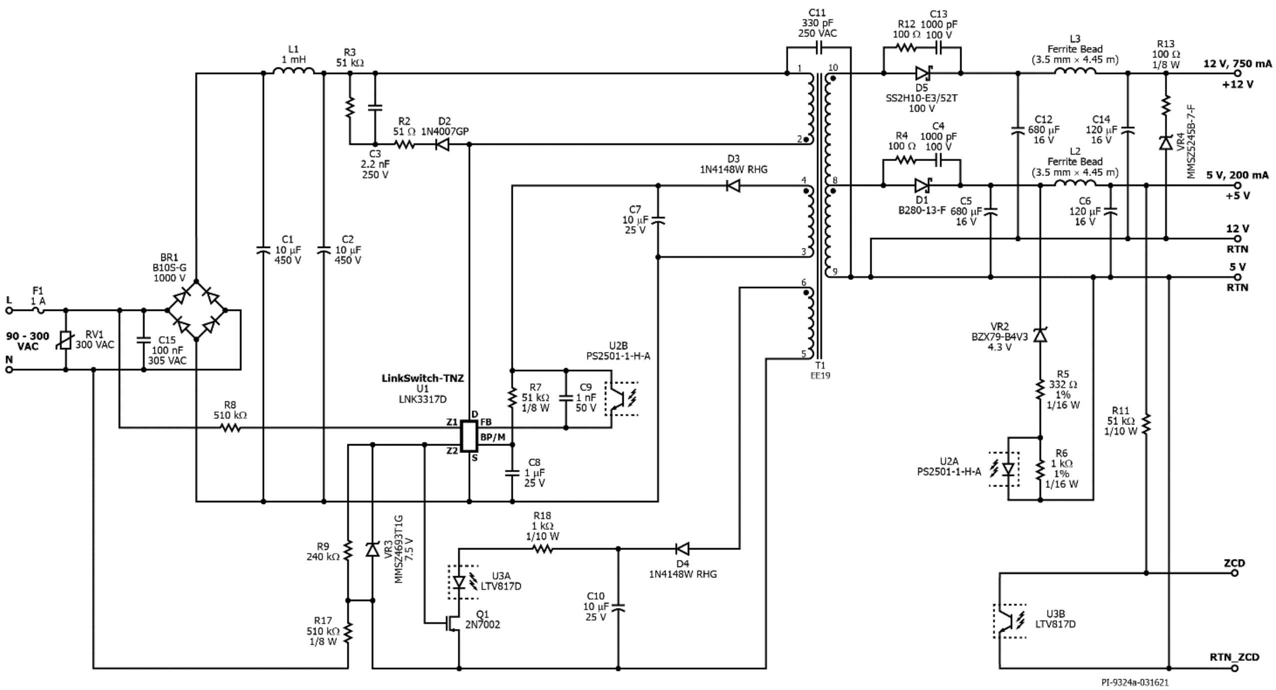

Figure 4 – Zero Crossing Configuration with Bias Winding

During the positive half-cycle of the AC input voltage, the Z1-Z2 pins draw 22 µA of supply current that flows from Line to Neutral. This current develops a voltage drop across R9 that consequently turns on Q1 and allows current to conduct between Q1's drain and source pins. Zener diode VR3 is placed to protect Q1 from excessive gate-source voltages. When Q1 conducts, optocoupler U3 is forward biased. Current flowing through U3 is determined by resistor R18 and bias voltage rectified by capacitor C10 and diode D4. At the secondary-side, the ZCD output is pulled down by the transistor output of optocoupler U3. Therefore, when AC voltage is positive, ZCD output is zero.

During the negative half-cycle of the AC input voltage, the Z1-Z2 pins draw the same 22 µA of supply current, but this time it flows from Neutral to Line. Zener diode VR3 is forward biased, developing a small negative voltage across Q1's gate and source pins. No current flows through optocoupler U3, and so the ZCD output at the secondary is pulled up by resistor R11 to the 5 V output. Therefore, when AC voltage is negative, ZCD output is 5 V.

The signal observed at the ZCD pin is a square wave switching between 5 V and 0 V, with its edges synchronized to the AC input zero crossings.

4.5.2 Zero Crossing Detection without Bias

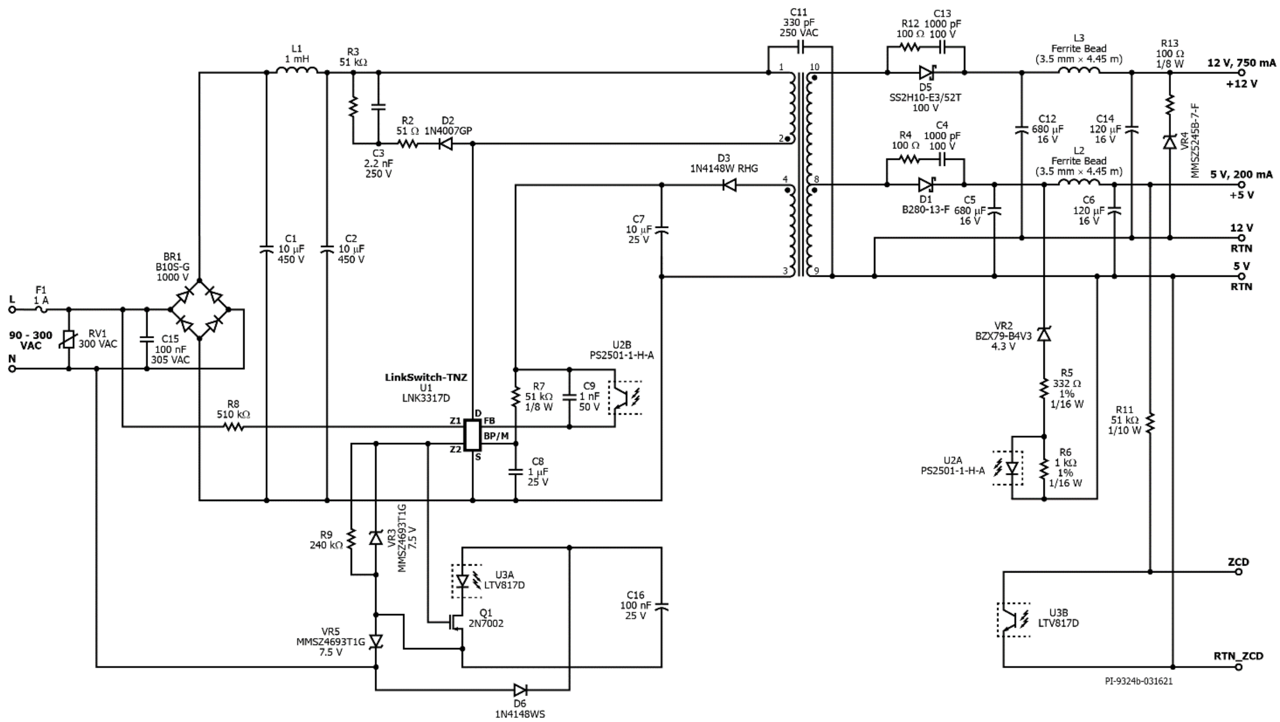

Figure 5 – Zero-crossing Configuration without Bias

The first configuration showed that the ZCD signal switches both when AC crosses from negative to positive half, and when AC crosses from positive to negative half. However, this configuration depends on the presence of an additional bias winding that is needed to forward bias the optocoupler during the entire AC positive half. The second configuration eliminates the need for the bias winding but produces only a ZCD signal that switches when AC crosses from negative to positive half.

During the AC negative half-cycle, the Z1-Z2 supply current charges up capacitor C16 thru diode D6. When the total voltage across capacitor C16 and diode D6 exceeds the Zener voltage of VR5, diode D6 turns off and capacitor C16 stops charging. The negative voltage across VR3 ensures that Q1 remains off.

During the AC positive half-cycle, similar to the first configuration, Q1 is turned on by Zener diode VR3 and resistor R9. Optocoupler conducts current, but only momentarily, until all the charge in C16 has been depleted. At the secondary, the ZCD output is momentarily pulled low by the transistor output of optocoupler U3, but then gradually

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goes back to 5 V as the voltage across capacitor C16 goes down. The ZCD output remains at 5 V for the remainder of the positive half cycle.

4.6 *EMI Design Aspects*

In addition to the simple input π filter (C1, L1 and C2) for differential mode EMI, this design makes use of shielding techniques in the transformer to reduce common mode EMI displacement currents. The first shield placed between primary and secondary windings acts to balance out the noise currents from both primary and secondary. A secondary shield is placed between the second primary winding and the zero crossing bias winding in order to reduce the coupling of noise into the Neutral node. Resistor R17 blocks any common mode noise from exiting into the Neutral node. These techniques combined with the frequency jitter of LNK3317D give excellent conducted EMI performance.

5 PCB Layout

Layers: 2
PCB Board Thickness: 1.59 mm/0.062 inches
Material: FR4
Copper: 2 oz

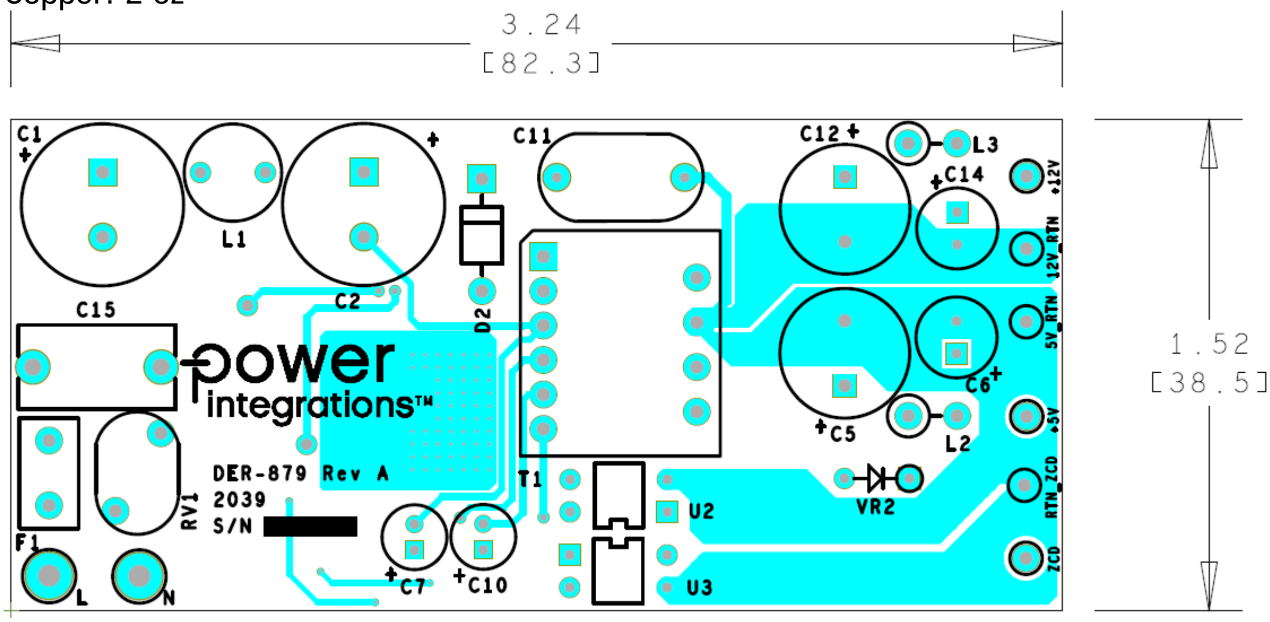

Figure 6 – Populated Circuit Board, Top View.

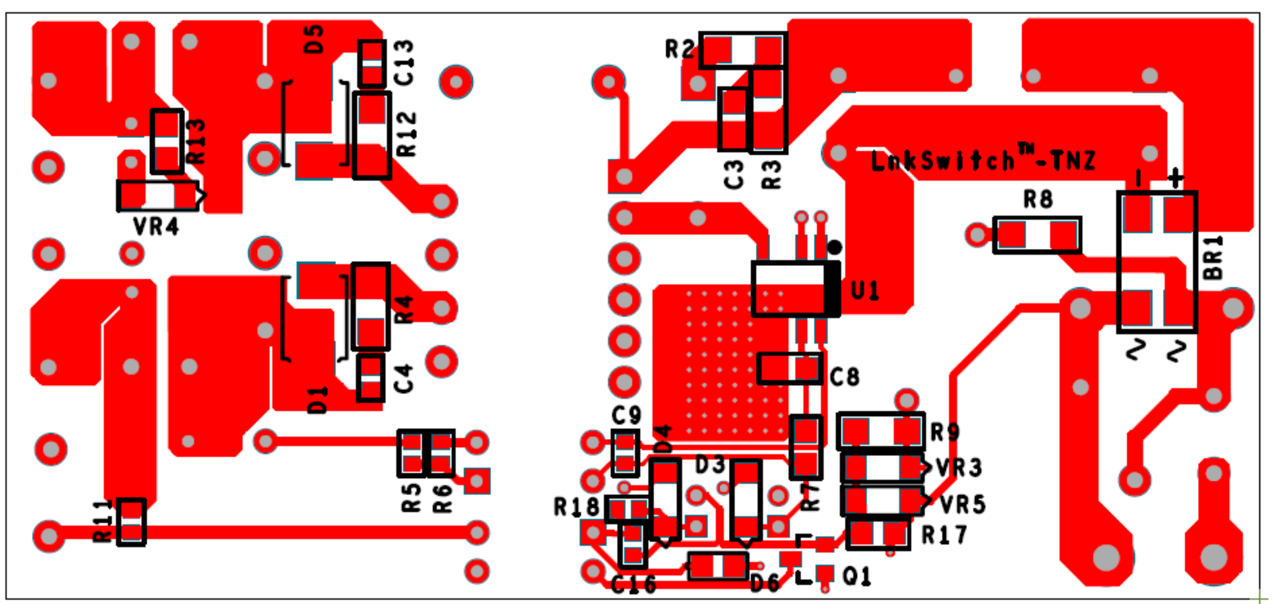

Figure 7 – Populated Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	2	C1 C2	10 µF, 450 V, Electrolytic, (12.5 x 20)	EKMG451ELL100MK20S	United Chemi-Com
3	1	C3	2.2 nF, 250 V, Ceramic, X7R, 0805	C2012X7R2E222K085AA	TDK
4	2	C4 C13	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
5	2	C5 C12	680 µF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE160ELL681MJ16S	Nippon Chemi-Con
6	2	C6 C14	120 µF, 16 V, Electrolytic, Very Low ESR, 130 mΩ, (6.3 x 11)	EKZE160ELL121MF11D	United Chemi-Con
7	2	C7 C10	10 µF, 25 V, Electrolytic, Gen. Purpose, (5 x 12)	ECA-1EM100	Panasonic
8	1	C8	1 µF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
9	1	C9	1 nF 50 V Ceramic C0G/NP0 0603	GRM1885C1H102JA01D	Murata
10	1	C11	330 pF, 300 VAC, Ceramic, Radial, X1Y1	DE1B3RA331KN4AP01F	TDK
11	1	C15	100 nF, 305 VAC, Film, X2	B32921C3104M	Epcos
12	1	C16	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KXXAC	Vishay
13	1	D1	80 V, 2 A, Schottky, SMD, SMB/DO214AA	B280-13-F	Diodes, Inc.
14	1	D2	Diode GEN PURP 1 kV 1A DO41	1N4007G-T	Diodes, Inc.
15	2	D3 D4	Diode, GEN PURP, 100V, 150 mA, SOD123, SOD-123F	1N4148W RHG	Taiwan Semi
16	1	D5	100 V, 2 A, Schottky, SMD, SMB	SS2H10-E3/52T	Vishay
17	1	D6	Diode, GEN PURP, 75 V 150 mA, SOD323	1N4148WS-7-F	Diodes, Inc.
18	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
19	1	L1	1 mH, 0.30 A, Ferrite Core	CTCH895F-102K	CT Parts
20	2	L2 L3	3.5 mm x 4.45 mm, 56 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
21	1	Q1	60 V, 115 mA, SOT23-3	2N7002-7-F	Diodes, Inc.
22	1	R2	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
23	1	R3	RES, 51 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ513V	Panasonic
24	2	R4 R12	RES, 100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ101V	Panasonic
25	1	R5	RES, 332 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3320V	Panasonic
26	1	R6	RES, 1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
27	1	R7	RES, 51 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ513V	Panasonic
28	1	R8	RES, 510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
29	1	R9	RES, 240 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ244V	Panasonic
30	1	R11	RES, 51 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ513V	Panasonic
31	1	R13	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
32	1	R17	RES, 510 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ514V	Panasonic
33	1	R18	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
34	1	RV1	300 VAC, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
35	1	T1	Bobbin, EE19, Vertical, 10 pins, 6pri, 4sec	TF-1939	Taiwan Shulin
36	1	U1	LinkSwitch-TNZ, SO8	LNK3317D	Power Integrations
37	1	U2	OPTOISOLATOR 5 kV TRANS 4DIP	PS2501-1-H-A	Renesas
38	1	U3	Optocoupler, 35 V, CTR 300-600%, 4-DIP	LTV-817D	Liteon
39	1	VR2	4.3 V, 500 mW, 2%, DO-35	BZX79-B4V3,133	NXP Semi
40	2	VR3 VR5	Diode, ZENER, 7.5 V, ±5%, 500 mW, SOD123, 150°C	MMSZ4693T1G	ON Semi
41	1	VR4	Diode ZENER 15 V 500 mW SOD123	MMSZ5245B-7-F	Diodes, Inc.

Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	+12 V +5 V	Test Point, RED, Miniature TH MOUNT	5000	Keystone
2	3	12 V_RTN 5 V_RTN RTN_ZCD	Test Point, BLK, Miniature TH MOUNT	5001	Keystone
3	1	ZCD	Test Point, BLUE, Miniature TH MOUNT	5117	Keystone
4	1	L	Test Point, WHT, TH MOUNT	5012	Keystone
5	1	N	Test Point, BLK, TH MOUNT	5011	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

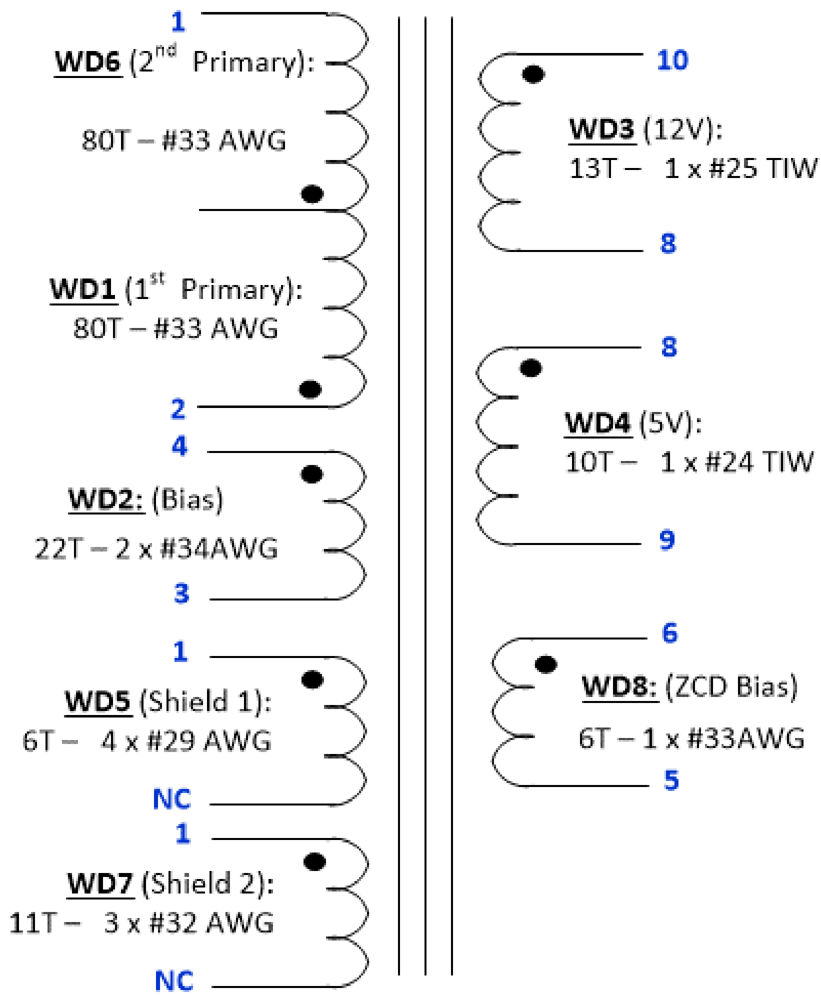

Figure 8 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 3 with all other windings open.	1461 µH
Tolerance	Tolerance of Primary Inductance.	±10%
Leakage Inductance	Measured across primary winding with all other windings shorted.	<45 µH

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7.3 *Material List*

Item	Description
[1]	Core: EE19.
[2]	Bobbin: EE19, Vertical, 10 Pins. PI#: 25-00924-00.
[3]	Magnet Wire: #29 AWG.
[4]	Magnet Wire: #32 AWG.
[5]	Magnet Wire: #33 AWG.
[6]	Magnet Wire: #34 AWG.
[7]	Tripe Insulated Wire: #24 AWG.
[8]	Tripe Insulated Wire: #25 AWG.
[9]	Polyester Tape: 9.1 mm.
[10]	Polyester Tape: 5.5 mm.
[11]	Varnish: Dolph BC 359 or Equivalent.

7.4 *Transformer Build Diagram*

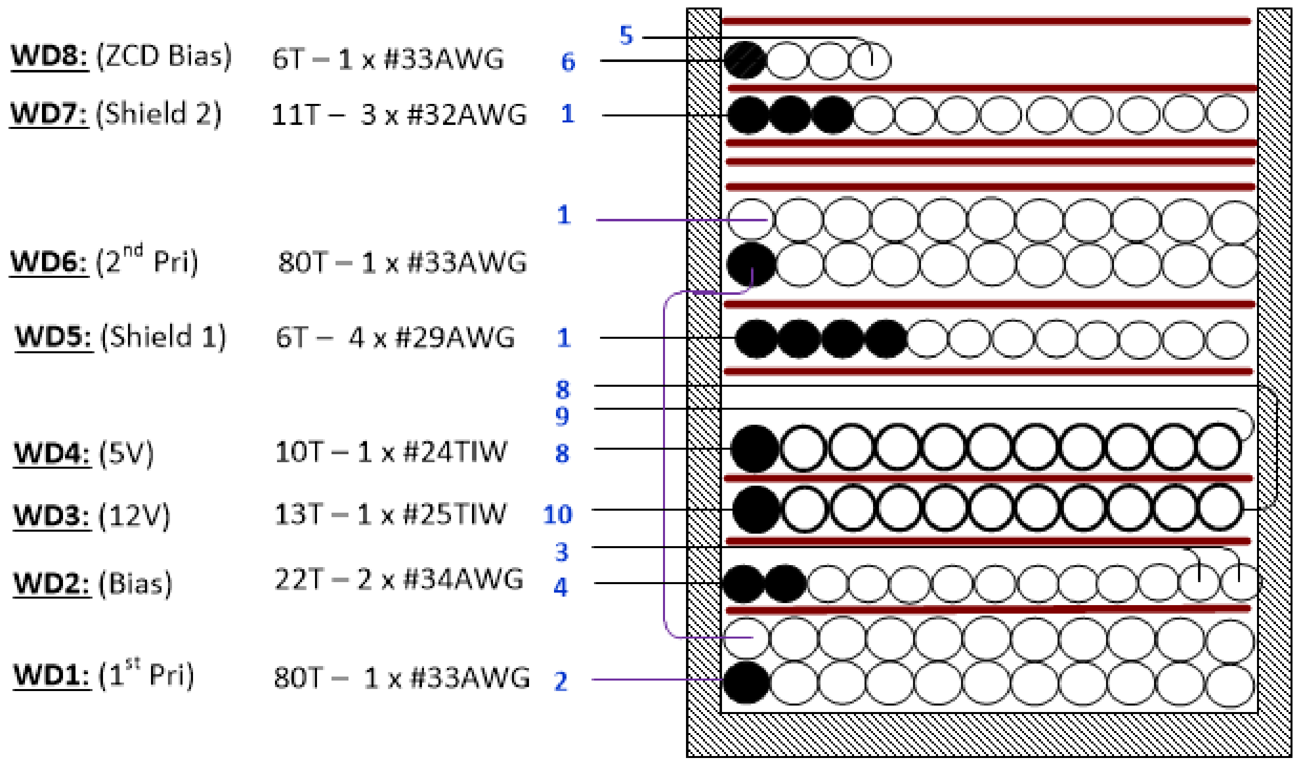

Figure 9 – Transformer Build Diagram.

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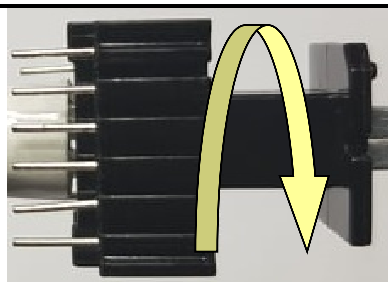
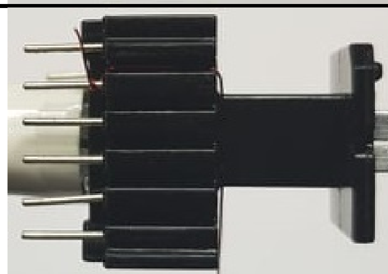
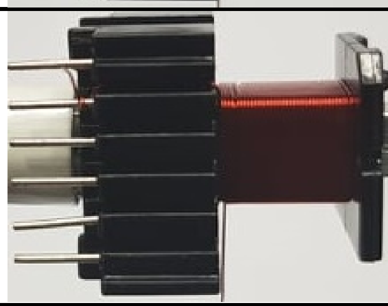
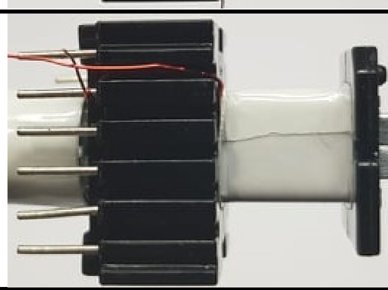
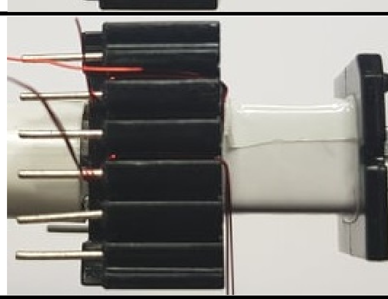
7.5 *Transformer Instructions*

Winding Preparation W1 1st Primary	Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise. Start at pin 2. Wind 80T of wire Item [5] in 2 layers. Leave 5 meters of wire Item [5] for 2nd primary winding.
Insulation W2 Bias	Place 1 layer of tape Item [9]. Start at pin 4. Wind 22T of 2 strands of wire Item [6] in 1 layer. Return to pin 3.
Insulation W3 12 V	Place 1 layer of tape Item [9].Start at pin 10. Wind 13T of wire Item [8] in 1 layer. Leave 2 inches of wire Item [8] on the right side.
Insulation W4 5 V	Place 1 layer of tape Item [9]. Start at pin 8. Wind 10T of wire Item [7] in one layer. Return to pin 9. Then return previous (12 V) winding to pin 8.
Insulation W5 Shield 1	Place 1 layer of tape Item [9]. Start at pin 1. Wind 6T of 4 strands of wire Item [3] in one layer. Cut the wire with no connection.
Insulation W6 2nd Primary	Place 1 layer of tape Item [9]. Continue winding 80T of wire Item [5] in two layers. Return to pin 1.
Insulation W7 Shield 2	Place 3 layers of tape Item [9]. Start at pin 1. Wind 11T of 3 strands of wire Item [4] in one layer. Cut the wire with no connection.
Insulation W8 ZCD	Place 1 layer of tape Item [9]. Start at pin 6. Wind 6T of wire Item [5]. Return to pin 5.
Insulation	Place 1 layer of tape Item [9].
Assembly	Grind core Item [1] halves for specified primary inductance. Wrap core halves with tape Item [10]. Dip in varnish Item [11].

7.6 *Transformer Winding Illustrations*

Winding Preparation		Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise.
W1 **1st Primary**		Start at pin 2. Wind 80T of wire Item [5] in 2 layers.
		Leave 5 meters of wire Item [5] for 2nd primary winding.
Insulation		Place 1 layer of tape Item [9].
W2 **Bias**		Start at pin 4. Wind 22T of 2 strands of wire Item [6] in 1 layer.

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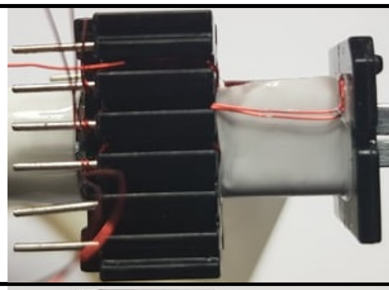
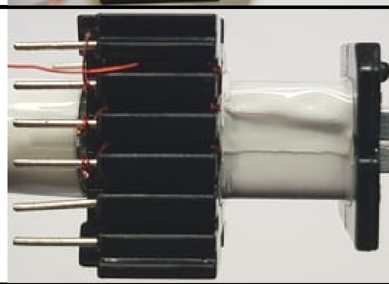
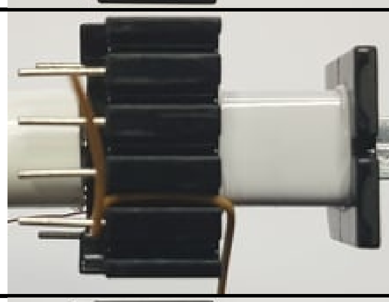
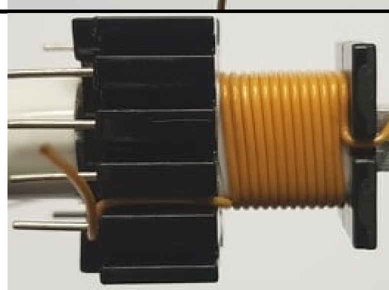
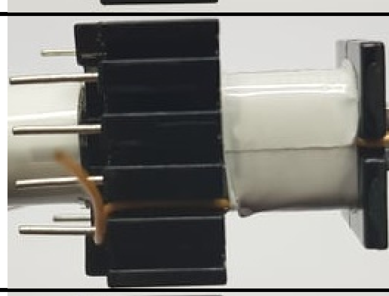
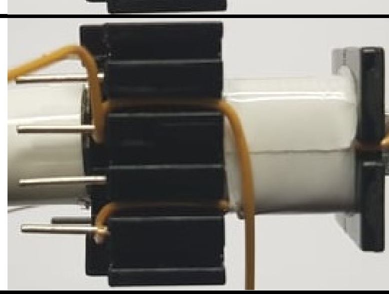
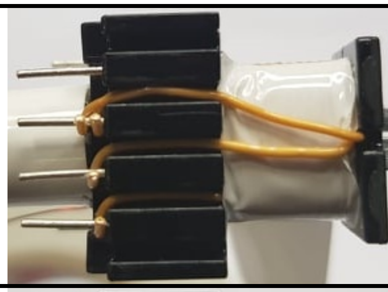
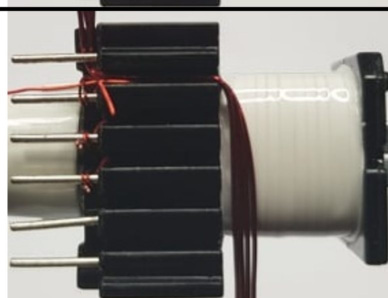
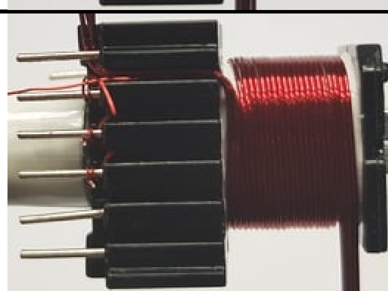
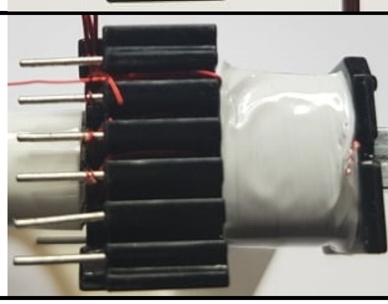
		Return to pin 3.
Insulation		Place 1 layer of tape Item [9].
W3 **12 V**		Start at pin 10. Wind 13T of wire Item [8] in 1 layer.
		Leave 2 inches of wire Item [8] on the right side.
Insulation		Place 1 layer of tape Item [9].
W4 **5 V**		Start at pin 8. Wind 10T of wire Item [7] in one layer.

		Return to pin 9. Then return previous (12 V) winding to pin 8.
Insulation		Place 1 layer of tape Item [9].
W5 Shield 1		Start at pin 1. Wind 6T of 4 strands of wire Item [3] in one layer.
		Cut the wire with no connection
Insulation		Place 1 layer of tape Item [9].

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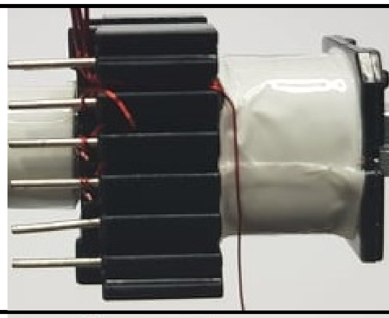
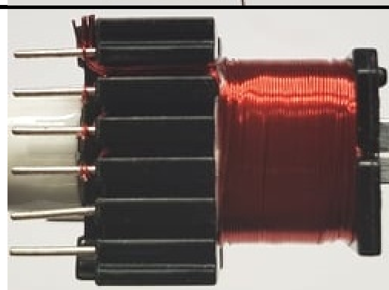
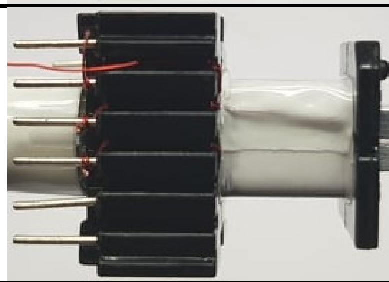
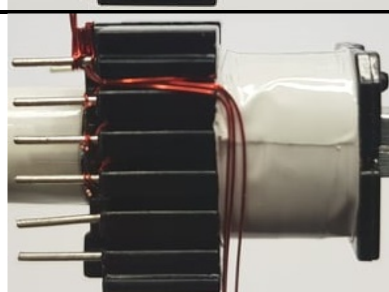
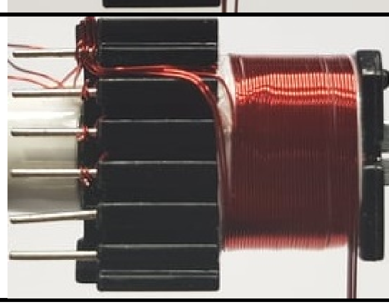
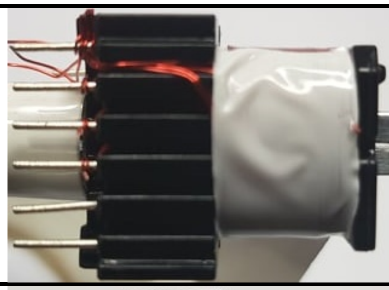
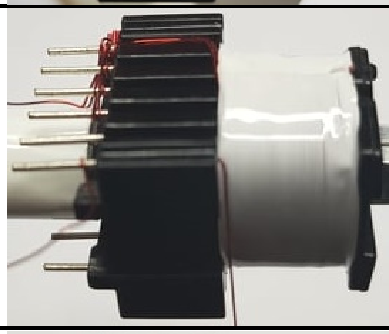
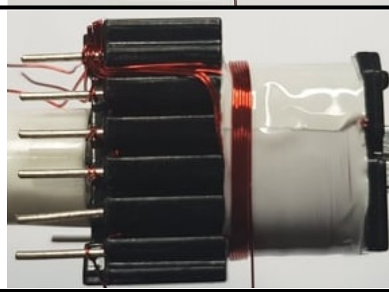
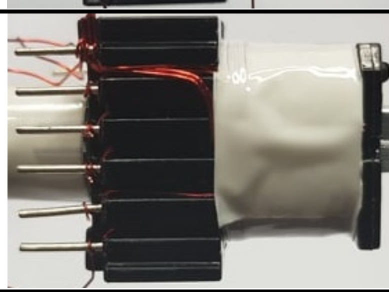
<table>
<tr><td rowspan="2">W6
2nd Primary</td><td></td><td>Continue winding 80T of wire Item [5] in two layers.</td></tr>
<tr><td></td><td>Return to pin 1.</td></tr>
<tr><td>Insulation</td><td></td><td>Place 3 layers of tape Item [9].</td></tr>
<tr><td rowspan="2">W7
Shield 2</td><td></td><td>Start at pin 1. Wind 11T of 3 strands of wire Item [4] in one layer.</td></tr>
<tr><td></td><td>Cut the wire with no connection.</td></tr>
</table>

Insulation		Place 1 layer of tape Item [9].
W8 ZCD		Start at pin 6. Wind 6T of wire Item [5].
		Return to pin 5.
Insulation		Place 1 layer of tape Item [9].
Assembly		Grind core Item [1] halves for specified primary inductance. Wrap core halves with tape Item [10]. Dip in varnish Item [11]

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9 Transformer Design Spreadsheet

ACDC_LinkSwitchTNZ_ Flyback_091520; Rev.0.1; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-TNZ Flyback Design Spreadsheet
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			Custom		AC line voltage range
VACMIN	90.00		90.00	V	Minimum AC line voltage
VACMAX	305.00		305.00	V	Maximum AC line voltage
fL			60.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
VOUT	5.00		5.00	V	Output voltage
IOUT	2.000		2.000	A	Average output current
EFFICIENCY (User Estimate)			0.80		Overall efficiency estimate
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the primary switch off-state to the total system losses
POUT			10.00	W	Continuous output power
CIN	20.00		20.00	uF	Input capacitor
VMIN			92.62	V	Valley voltage of the rectified minimum AC line voltage
VMAX			431.34	V	Peak voltage of the maximum AC line voltage
FEEDBACK	BIAS		BIAS		Type of feedback required. Choose "BIAS" for bias winding feedback and "OPTO" for an optocoupler feedback
BIAS WINDING	YES		YES		Select whether a bias winding is required or not
INPUT STAGE RESISTANCE			10.0	Ohms	Input stage resistance (includes thermistor, filtering components, etc)
PLOSS_INPUTSTAGE			0.182	W	Maximum input stage power loss
LINKSWITCH-TNZ VARIABLES					
CURRENT LIMIT MODE	RED		RED		Choose "STD" for Standard current limit or "RED" for reduced current limit
PACKAGE			SO-8C		Device package
DEVICE SERIES	LNK3317		LNK3317		Generic LinkSwitch-TNZ device
DEVICE CODE			LNK3317D		Required LinkSwitch-TNZ device
ILIMITMIN			0.526	A	Minimum current limit of the device
ILIMITTYP			0.599	A	Typical current limit of the device
ILIMITMAX			0.672	A	Maximum current limit of the device
RDSON			12.9	Ohms	Switch on-state drain-to-source resistance at 100 degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			70000	Hz	Maximum switching frequency
BVDSS			725	V	Device breakdown voltage
PRIMARY WAVEFORM PARAMETERS					
OPERATION MODE			CCM		Continuous mode of operation
VOR	91.0		91.0	V	Voltage reflected across the primary winding when the primary switch is off
VDSON			2.00	V	Primary switch on-time drain-to-source voltage
VDSOFF			592.3	V	Primary switch off-time drain-to-source voltage stress
KRP/KDP			0.933		Degree on how much the operation tend to be continuous or discontinuous
KP_TRANSIENT			0.378		KP value under transient conditions
DUTY			0.501		Maximum duty cycle
TIME_ON_MIN			1.795	us	Primary switch minimum on-time
IPEAK_PRIMARY			0.748	A	Maximum primary peak current
IPED_PRIMARY			0.035	A	Maximum primary pedestal current
IAVG_PRIMARY			0.138	A	Maximum primary average current
IRMS_PRIMARY			0.247	A	Maximum root-mean-squared value of the

					primary current
PLOSS_SWITCH			0.911	W	Maximum primary switch power loss
THERMAL RESISTANCE OF SWITCH			100	degC/W	Net thermal resistance of primary switch
T_RISE_SWITCH			91.1	degC	Maximum temperature rise of the switch in degrees Celsius
LPRIMARY_MIN			1315	uH	Minimum primary inductance
LPRIMARY_TYP			1461	uH	Typical primary inductance
LPRIMARY_MAX			1607	uH	Maximum primary inductance
LPRIMARY_TOL			10	%	Primary inductance tolerance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			11.961	A	Peak secondary current
IRMS_SECONDARY			4.186	A	Maximum root-mean-squared value of the secondary current
IRIPPLE_SECONDARY			11.961	A	Maximum ripple value of the secondary current
PIV_SECONDARY			31.8	V	Peak inverse voltage of the secondary diode
VF_SECONDARY			0.70	V	Forward voltage drop of the secondary diode
TRANSFORMER CONSTRUCTION PARAMETERS					
Core Selection					
CORE	EE19		EE19		Select the transformer core
BOBBIN			B-EE19-H		Select the bobbin
AE			23.00	mm^2	Cross-sectional area of the core
LE			39.40	mm	Effective magnetic path length of the core
AL			1250.0	nH/(T^2)	Ungapped effective inductance of the core
VE			0.0	mm^3	Effective volume of the core
AW			0.00	mm^2	Window area of the bobbin
BW			9.10	mm	Width of the bobbin
MLT			26.40	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin
Primary Winding					
NPRIMARY			160	turns	Primary winding number of turns
BMAX		Info	3179	Gauss	The target magnetic flux density of 1500 Gauss has been exceeded. Increase the number of turns in secondary
BAC			1590	Gauss	AC flux density
ALG			57	nH/(T^2)	Gapped core effective inductance
LG			0.483	mm	Core gap length
LAYERS_PRIMARY			5	layers	Number of primary winding layers
AWG_PRIMARY	33		33		Primary winding wire size in AWG
OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			203	mil^2/A	Primary winding wire CMA
Secondary Winding					
NSECONDARY	10		10	turns	Secondary winding number of turns
AWG_SECONDARY			20		Secondary winding wire size in AWG
OD_SECONDARY_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.812	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			244	mil^2/A	Secondary winding wire CMA
Bias Winding					
NBIAS			22	turns	Bias winding number of turns
VF_BIAS			0.70	V	Forward voltage drop of bias diode
VBIAS			12.00	V	Voltage across the bias winding
PIV_BIAS			71.79	V	Peak inverse voltage on the bias diode
RBP			84500	Ohms	BP pin resistor
CBP			1.0	uF	BP pin capacitor
Primary Winding Losses					
PLOSS_PRIMARYWINDING			0.174	W	Maximum power loss dissipated in the primary winding

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FEEDBACK PARAMETERS					
DIODE_BIAS			1N4003-4007		Recommended bias diode is 1N400X
RUPPER			15000	Ohms	Resistor divider component between bias winding and FB pin of LinkSwitch-TNZ
RLOWER			3000	Ohms	Resistor divider component between FB pin of LinkSwitch-TNZ and primary RTN
X-CAPACITOR DISCHARGE COMPONENTS					
XCAP REQUIRED	YES		YES		Select whether an X-capacitor is required or not
XCAP			100.0	nF	X-capacitor in the input
TOLERANCE_RZ	0.05		5%		Tolerance of the X-capacitor discharge resistors
RZ1	0.50		0.50	MOhms	X-capacitor discharge resistor connected from the input line to Z1 pin of LinkSwitch-TNZ
RZ2			0.50	MOhms	X-capacitor discharge resistor connected from the input neutral to Z2 pin of LinkSwitch-TNZ
t_XCAP_DISCHARGE			0.207	sec	Actual time (worst-case) to discharge the X-capacitor to 60 V after AC input disconnection
MULTIPLE OUTPUT PARAMETERS					
Output 1					
VOUT1			5.00	V	Output voltage 1
IOUT1	0.200		0.200	A	Output current 1
POUT1			1.00	W	Output power 1
VD1			0.70	V	Forward voltage drop of secondary diode for output 1
NS1			10	turns	Number of turns for output 1
ISPEAK1			11.96	A	Instantaneous peak value of the secondary current for output 1
ISRMS1			0.419	A	Root-mean-squared value of the secondary current for output 1
ISRIPPLE1			11.961	A	Current ripple on the secondary current waveform for output 1
PIV1_CALCULATED			31.8	V	Computed peak inverse voltage stress on the secondary diode for output 1
PIV1_RATING			50	V	Peak inverse voltage rating on the secondary diode for output 1
TRR1			50	ns	Reverse recovery time of the secondary diode for output 1
IFM1			1.00	A	Maximum forward continuous current of the secondary diode for output 1
DIODE1_RECOMMENDED			UF4001		Recommended diode for output 1
PLOSS_DIODE1			0.437	W	Maximum secondary diode power loss for output 1
VOUT1_RIPPLE			50	mV	Output voltage ripple for output 1
ESR_COUT1			4	mOhms	Equivalent series resistance of the output capacitor for output 1
IRMS_COUT1			0.368	A	Root-mean-squared value of the output capacitor current for output 1
PLOSS_COUT1			0.001	W	Maximum output capacitor power loss for output 1
CMS1			84	Cmils	Bare conductor effective area in circular mils for output 1
AWGS1			30	AWG	Wire size of winding for output 1
ODS1_INSULATED			0.559	mm	Secondary winding wire outer diameter with insulation for output 1
ODS1_BARE			0.255	mm	Secondary winding wire outer diameter without insulation for output 1
PLOSS_SECONDARYWINDING1			0.016	W	Maximum power loss dissipated of secondary winding for output 1
Output 2					
VOUT2	12.00		12.00	V	Output voltage 2
IOUT2	0.750		0.750	A	Output current 2
POUT2			9.00	W	Output power 2

VD2			0.70	V	Forward voltage drop of secondary diode for output 2
NS2			23	turns	Number of turns for output 2
ISPEAK2			5.200	A	Instantaneous peak value of the secondary current for output 2
ISRMS2			1.570	A	Root-mean-squared value of the secondary current for output 2
ISRIPPLE2			5.200	A	Current ripple on the secondary current waveform for output 2
PIV2_CALCULATED			73.7	V	Computed peak inverse voltage stress on the secondary diode for output 2
PIV2_RATING			200	V	Peak inverse voltage rating on the secondary diode for output 2
TRR2			25	ns	Reverse recovery time of the secondary diode for output 2
IFM2			2.00	A	Maximum forward continuous current of the secondary diode for output 2
DIODE2_RECOMMENDED			BYV27-200		Recommended diode for output 2
PLOSS_DIODE2			0.433	W	Maximum secondary diode power loss for output 2
VOUT2_RIPPLE			120	mV	Output voltage ripple for output 2
ESR_COUT2			23	mOhms	Equivalent series resistance of the output capacitor for output 2
IRMS_COUT2			1.379	A	Root-mean-squared value of the output capacitor current for output 2
PLOSS_COUT2			0.044	W	Maximum output capacitor power loss for output 2
CMS2			314	Cmils	Bare conductor effective area in circular mils for output 2
AWGS2			25	AWG	Wire size of winding for output 2
ODS2_INSULATED			0.760	mm	Secondary winding wire outer diameter with insulation for output 2
ODS2_BARE			0.455	mm	Secondary winding wire outer diameter without insulation for output 2
PLOSS_SECONDARYWINDING2			0.158	W	Maximum power loss dissipated of secondary winding for output 2
POUT_TOTAL			10.00	W	Total power of all outputs
NEGATIVE OUTPUT	N/A		N/A		If a negative output exists, select the output number (e.g. if VO2 is a negative output, select 2)

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10 Performance Data

10.1 *Efficiency*

10.1.1 Average Efficiency

% Load	Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)	Average Efficiency (%)
	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)		
100	115	209.23	12.65	11.97	750.00	8.98	4.99	198.11	0.99	78.77	78.64
75	115	165.73	9.45	12.00	562.48	6.75	5.00	148.18	0.74	79.27	
50	115	119.35	6.30	12.01	374.93	4.50	5.01	98.07	0.49	79.27	
25	115	71.94	3.23	12.00	187.42	2.25	5.02	48.15	0.24	77.27	
100	230	134.43	12.47	12.00	750.00	9.00	4.99	198.11	0.99	80.08	78.39
75	230	107.60	9.40	12.01	562.48	6.76	4.99	147.90	0.74	79.77	
50	230	80.69	6.36	12.02	374.93	4.51	5.00	98.17	0.49	78.63	
25	230	49.74	3.32	12.02	187.39	2.25	5.01	48.24	0.24	75.08	

10.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.

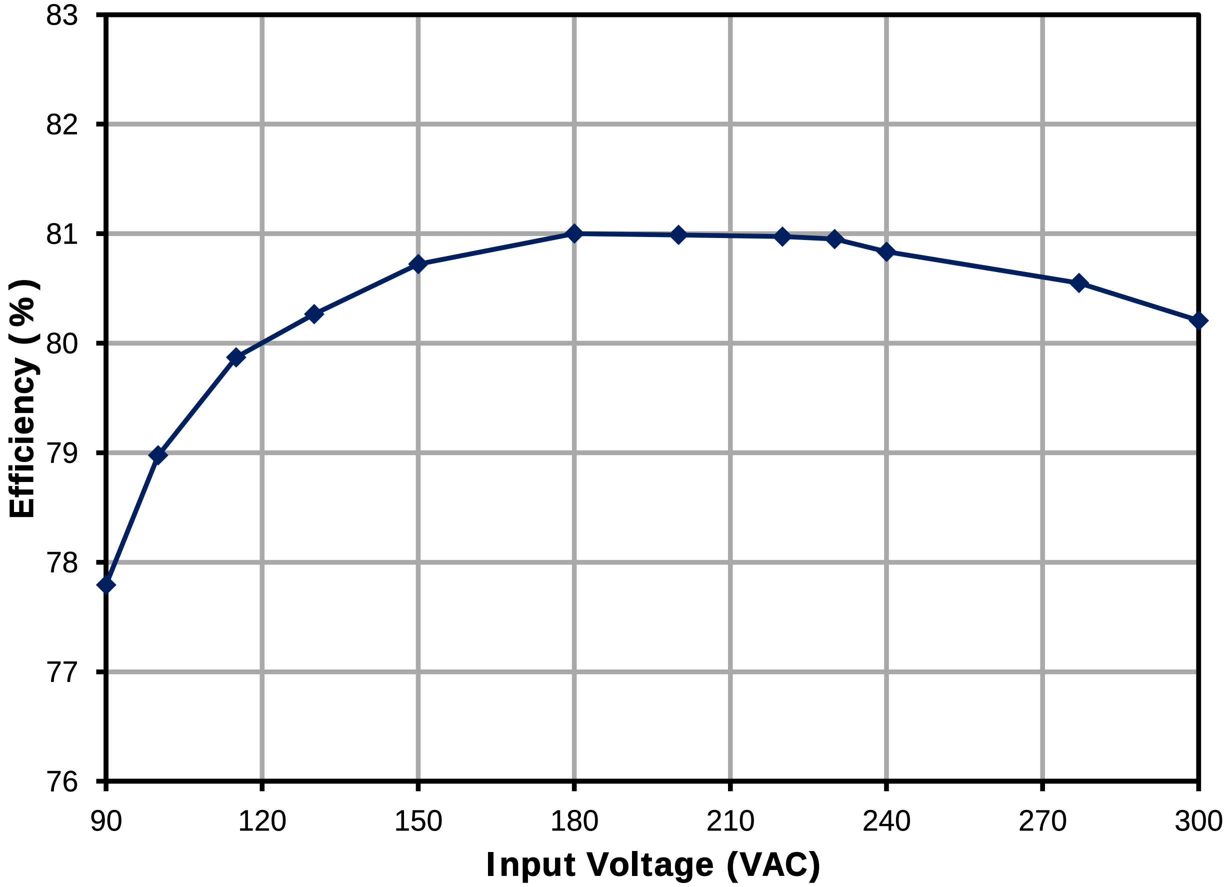

Figure 10 – Full Load Efficiency vs. Line.

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10.1.3 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

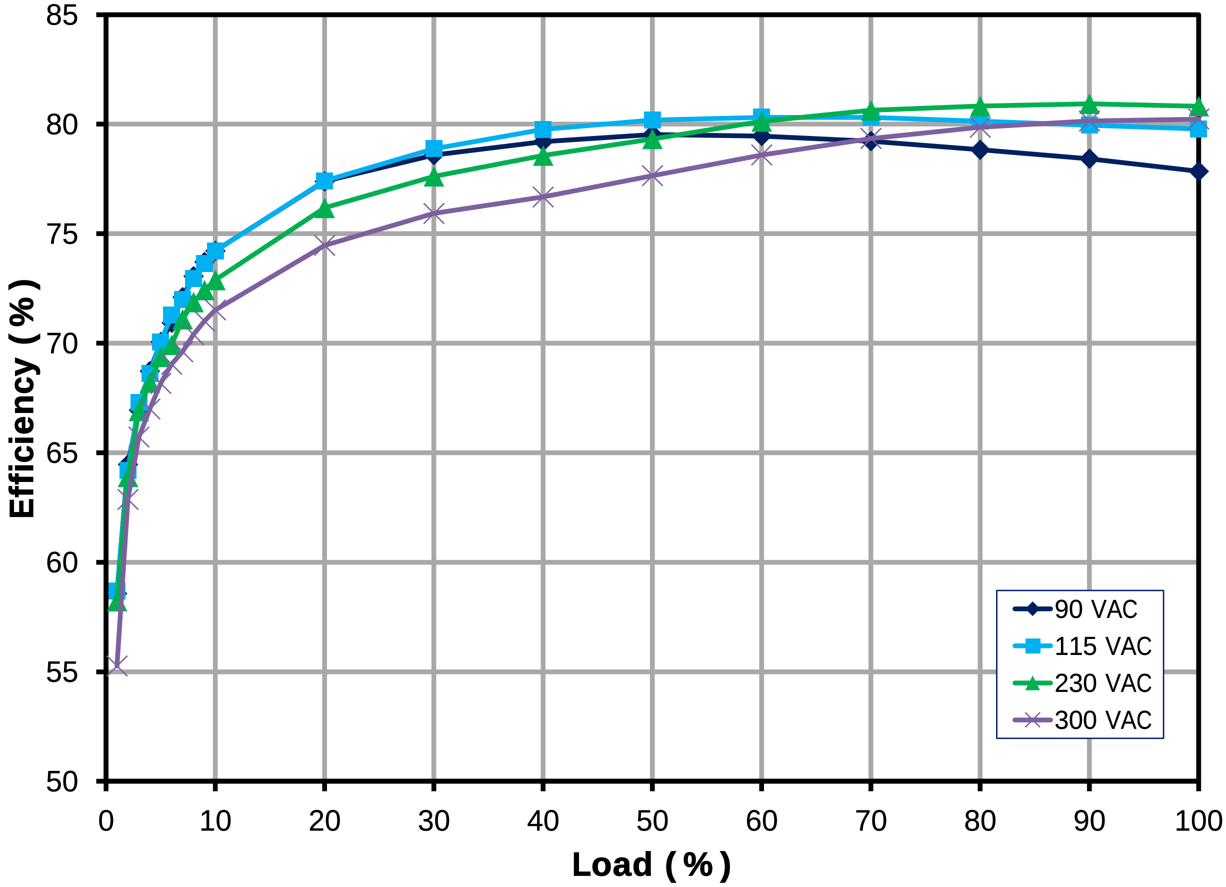

Figure 11 – Efficiency vs. Percentage Load.

10.2 *Available Standby Output Power*

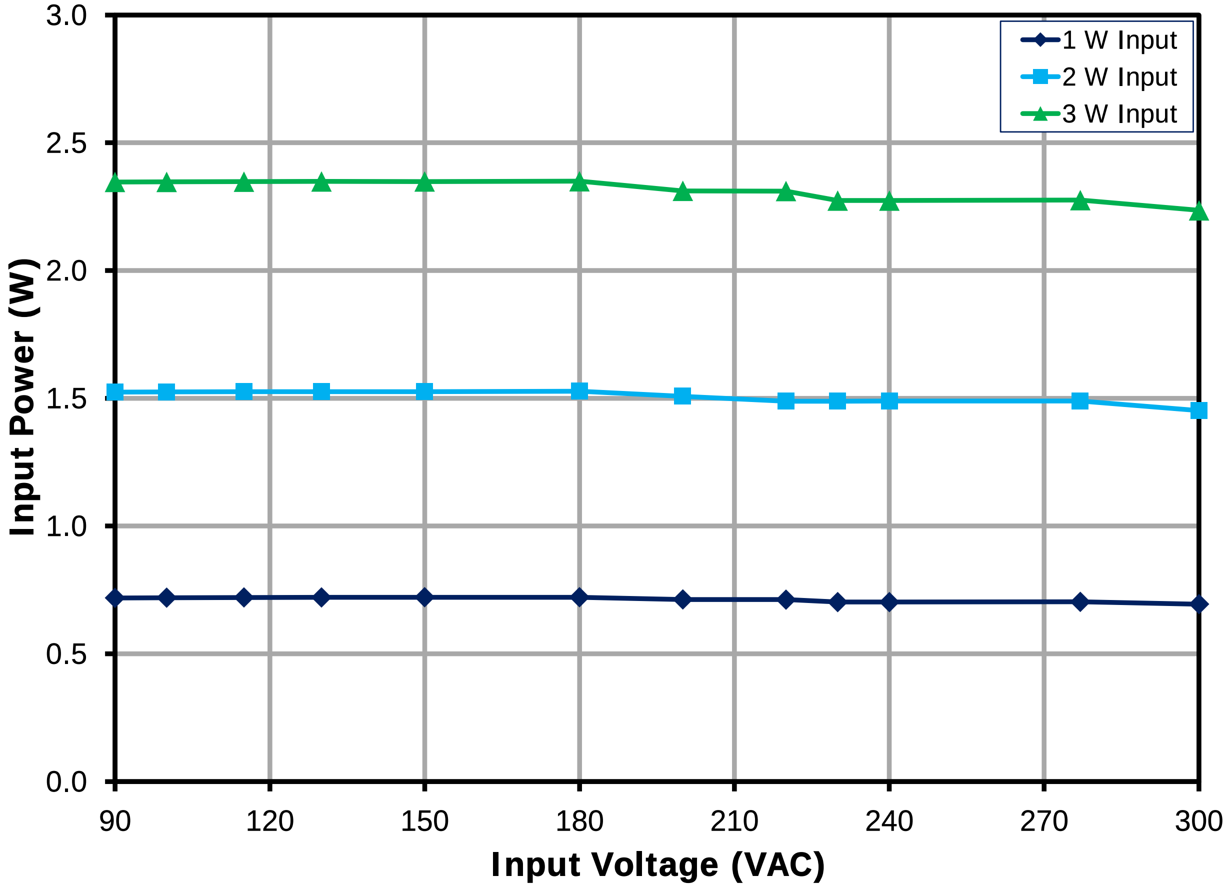

Figure 12 – Available Standby Output Power for 1 W, 2 W and 3 W Input Power.

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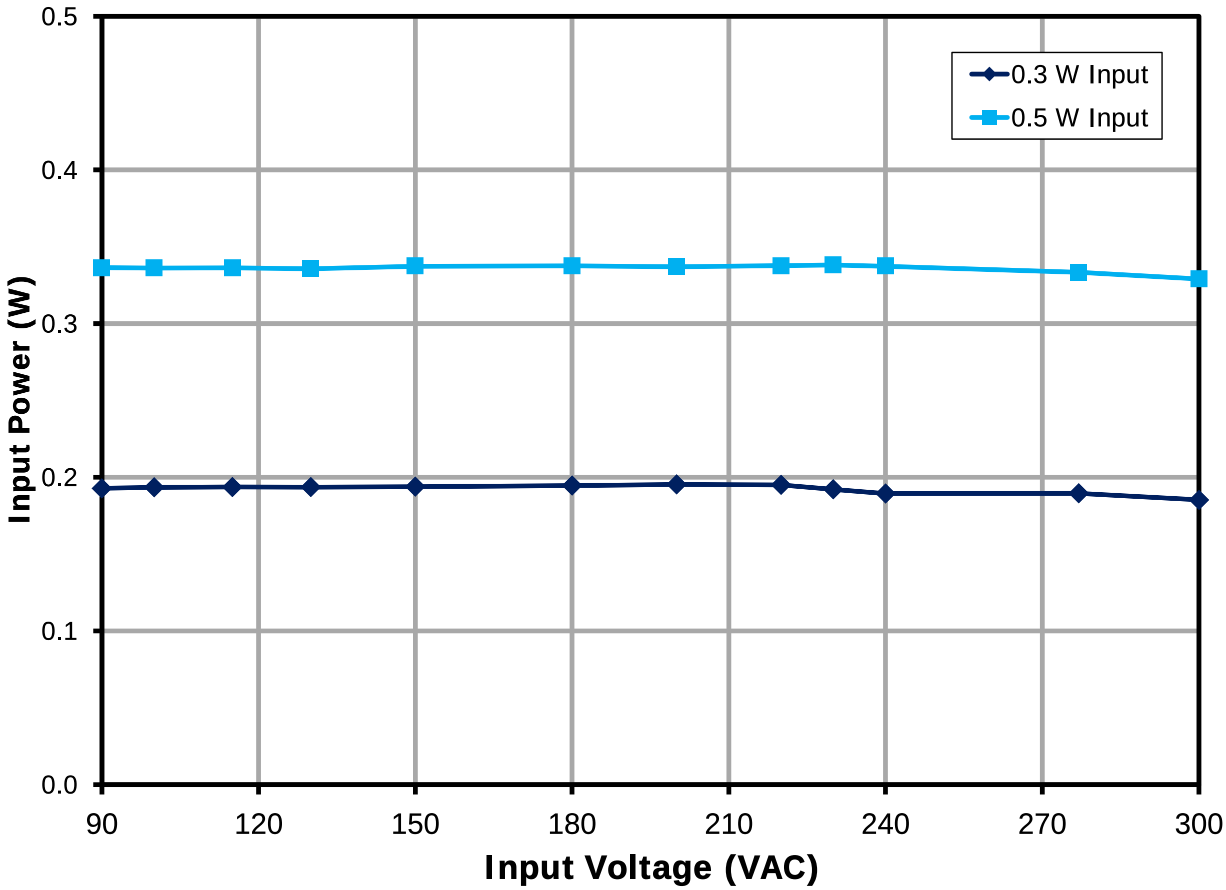

Figure 13 – Available Standby Output Power for 0.3 W and 0.5 W Input Power.

10.3 *No-Load Input Power*

Test Condition: Soak for 15 minutes each line and 1 minute integration time.

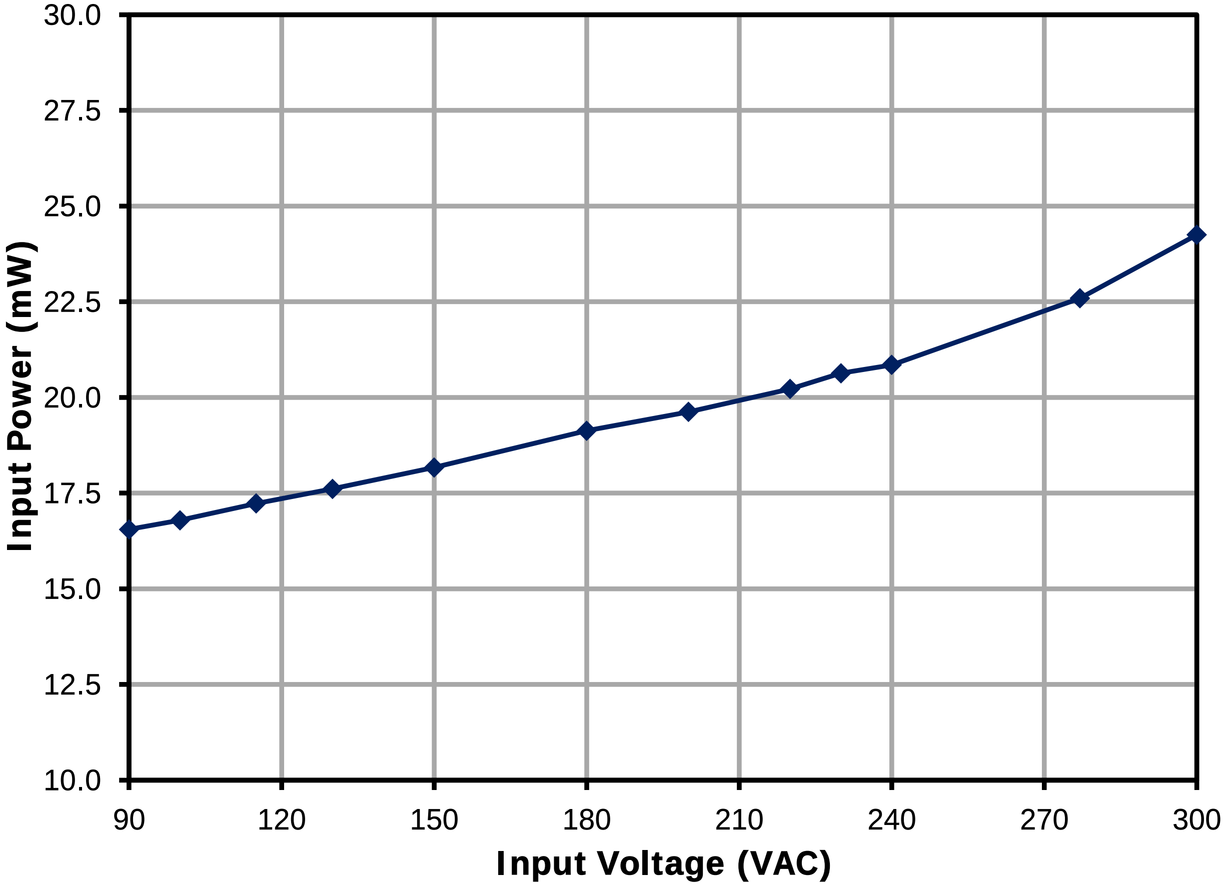

Figure 14 – No-Load Input Power vs. Line at Room Temperature.

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10.4 *Line Regulation*

10.4.1 12 V Line Regulation

Test Condition: Soak for 15 minutes for each line.

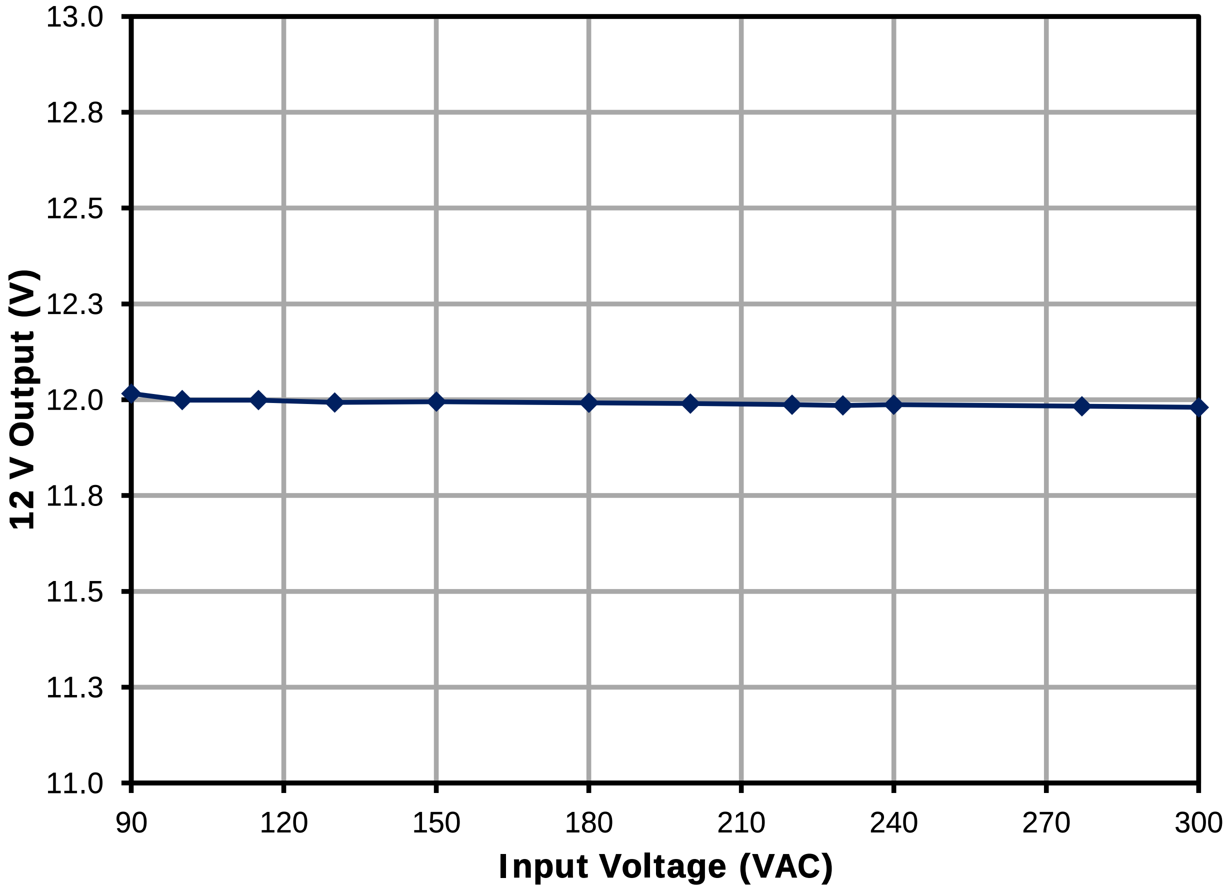

Figure 15 – Output Voltage vs. Line Voltage.

10.4.2 5 V Line Regulation

Test Condition: Soak for 15 minutes for each line.

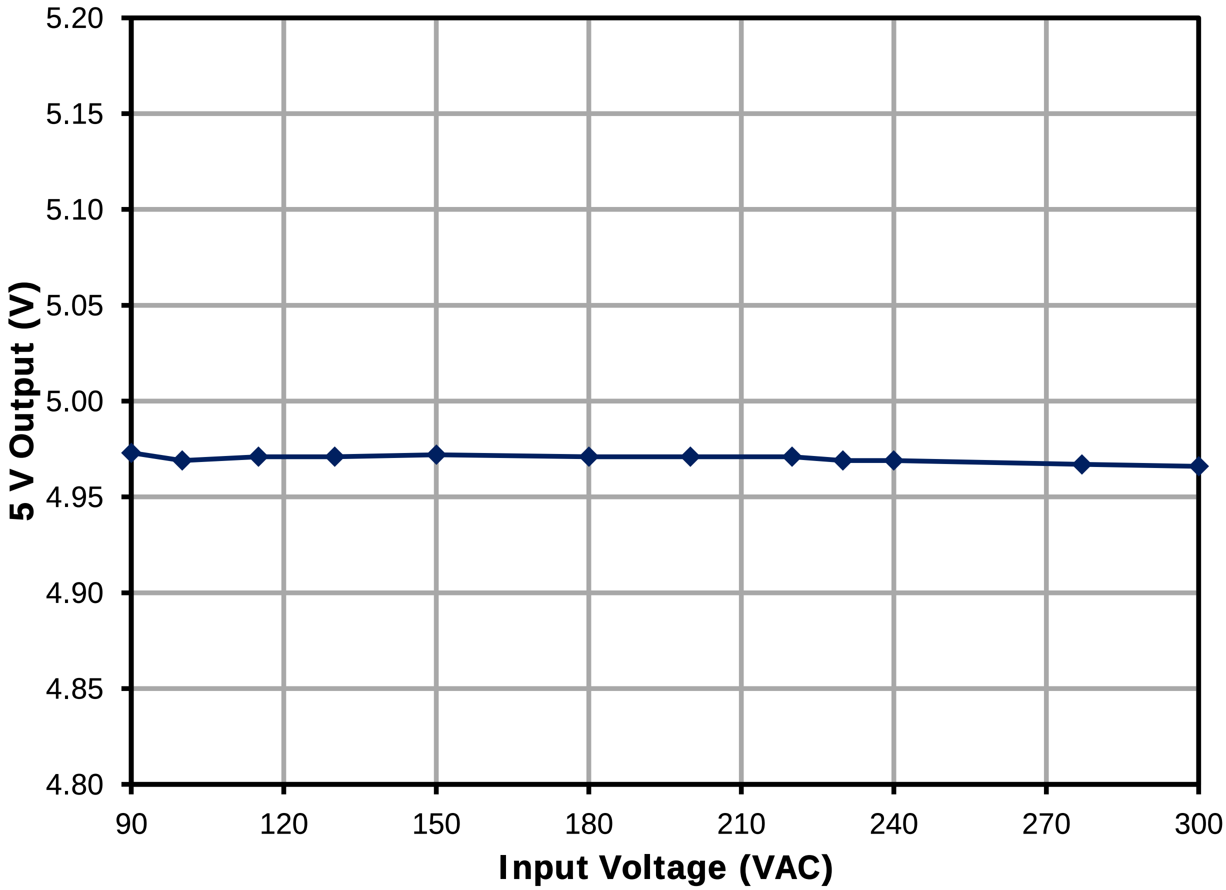

Figure 16 – Output Voltage vs. Line Voltage.

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10.5 *Load Regulation*

10.5.1 12 V Line Regulation with Balanced Load

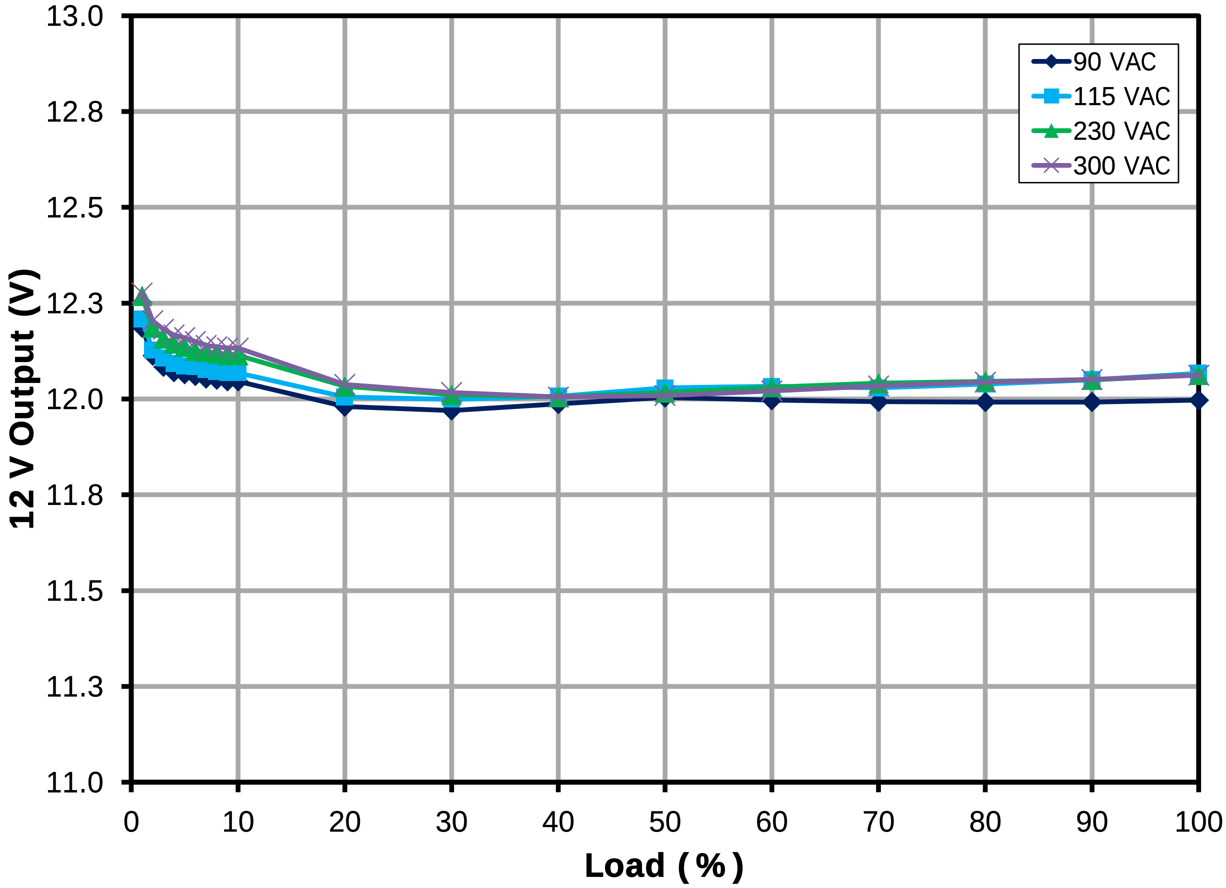

Figure 17 – Output Voltage vs. Percent Load.

10.5.2 5 V Line Regulation with Balanced Load

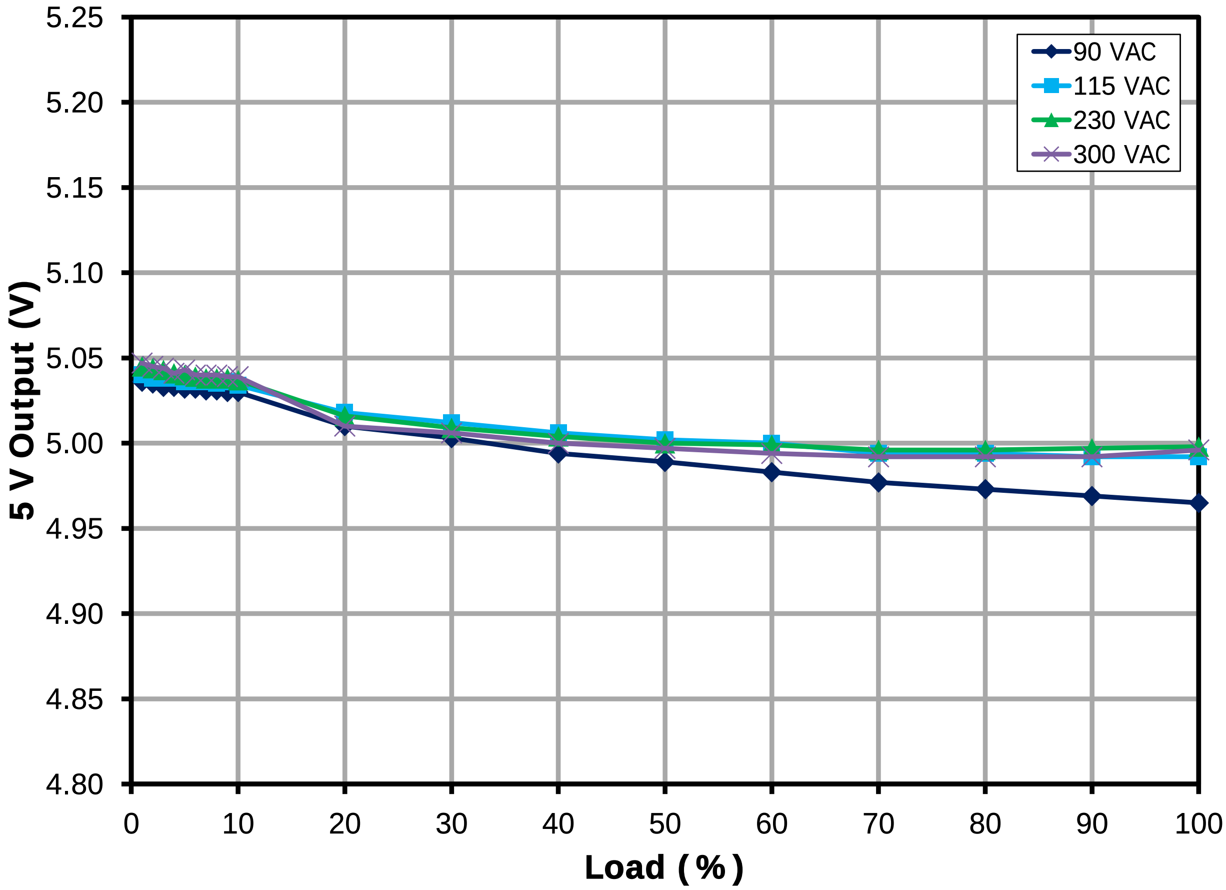

Figure 18 – Output Voltage vs. Percent Load.

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10.5.3 12 V Line Regulation with 5 V fixed at 200 mA

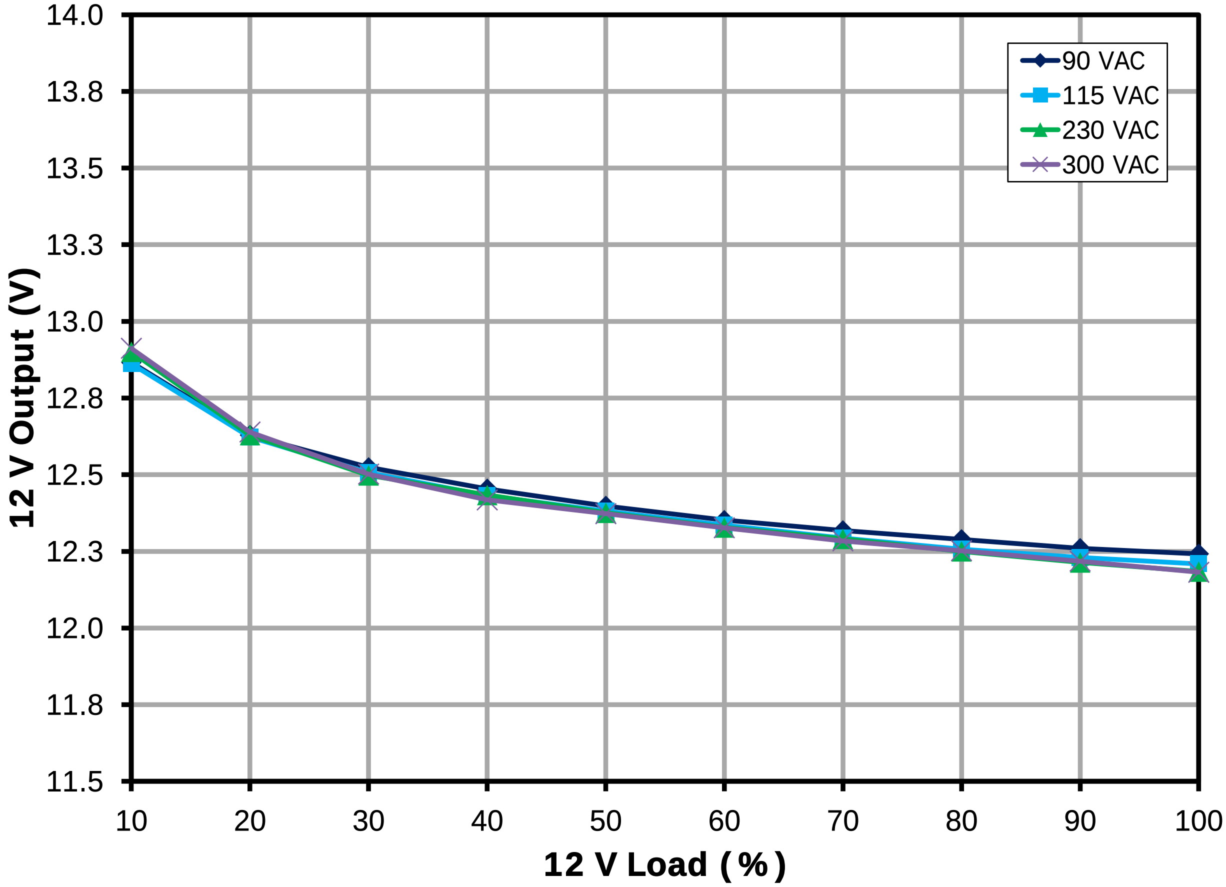

Figure 19 – Output Voltage vs. Percent Load.

10.5.4 12 V Line Regulation with 5 V fixed at 20 mA

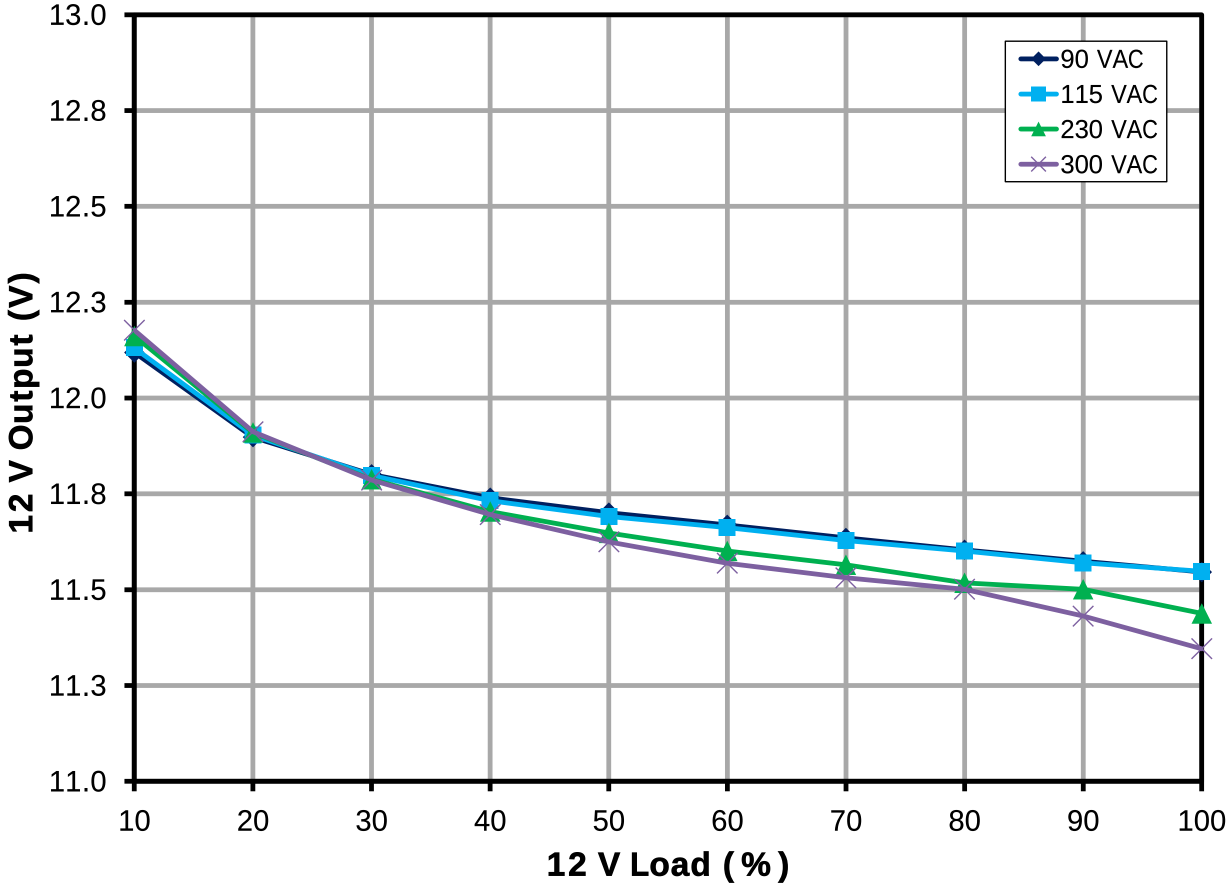

Figure 20 – Output Voltage vs. Percent Load.

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10.5.5 5 V Line Regulation with 12 V fixed at 750 mA

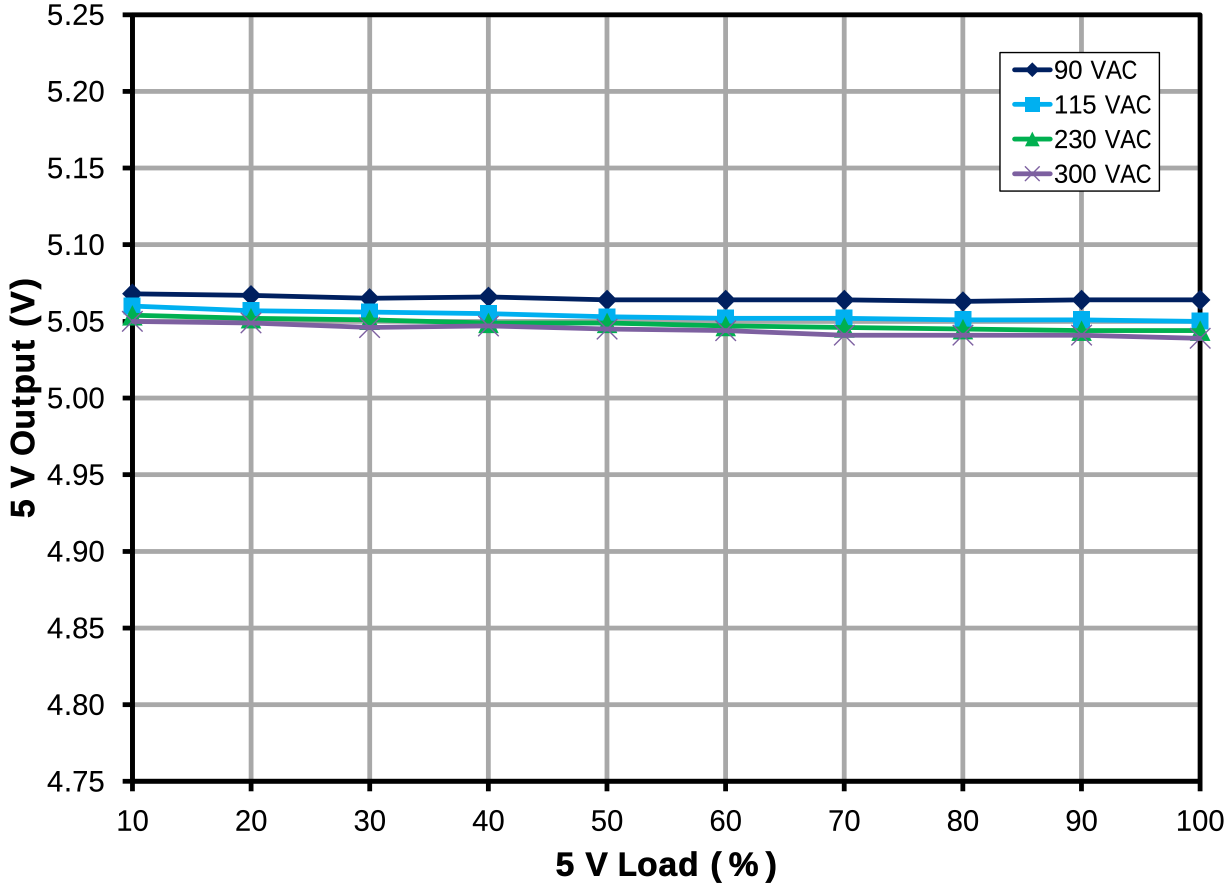

Figure 21 – Output Voltage vs. Percent Load.

10.5.6 5 V Line Regulation with 12 V fixed at 75 mA

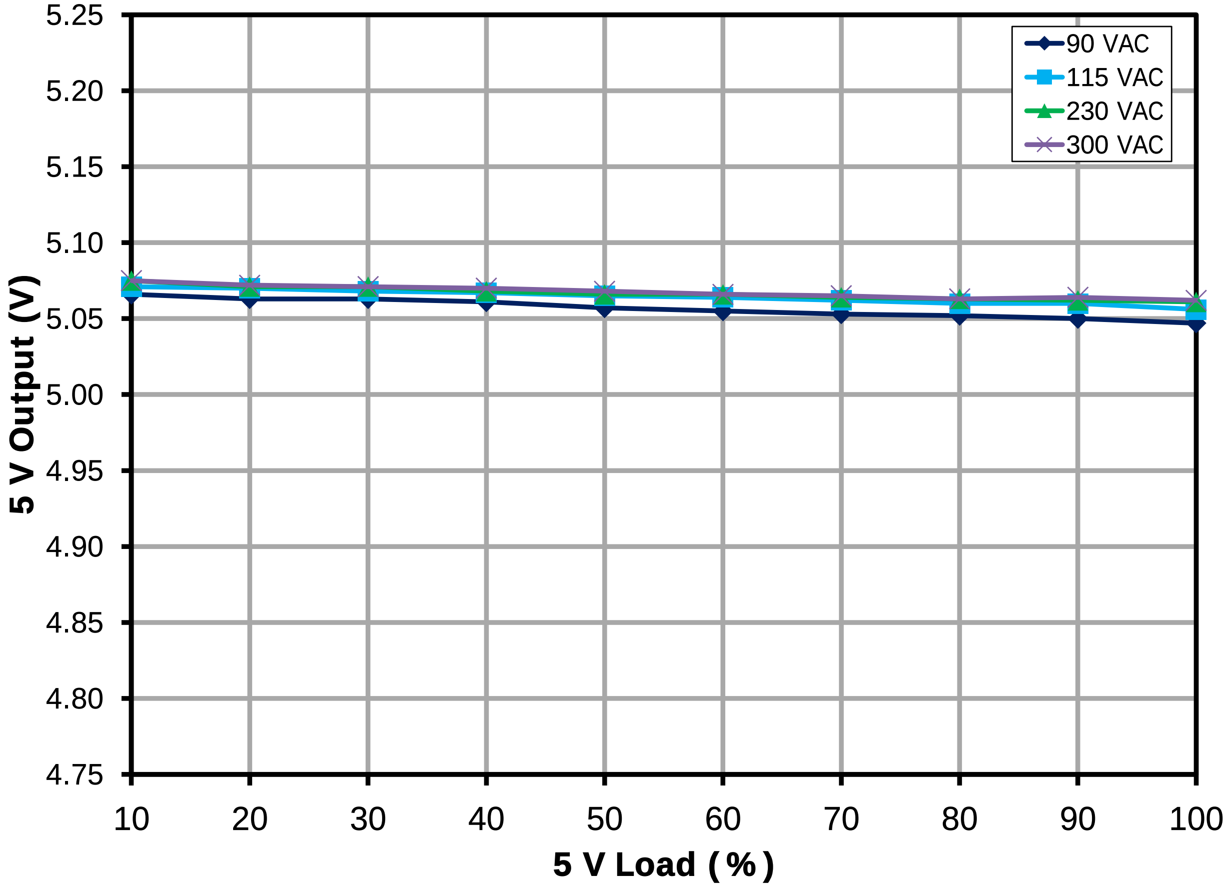

Figure 22 – Output Voltage vs. Percent Load.

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11 Waveforms

11.1 *Zero Crossing Detection – With Bias Winding Configuration*

11.1.1 Zero Crossing Detection at Normal Operation

11.1.1.1 100% Load

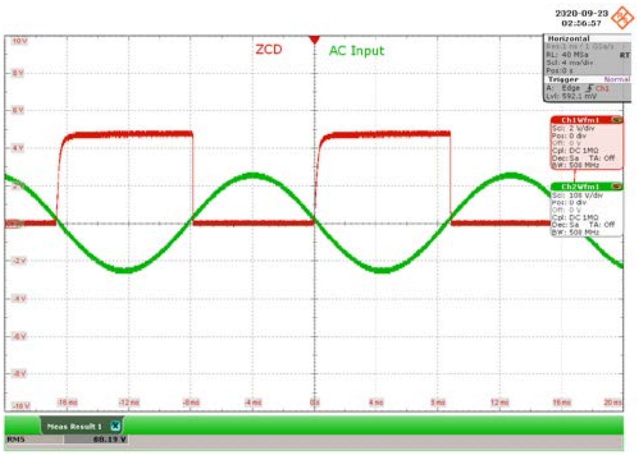

Figure 23 – 90 VAC 60 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

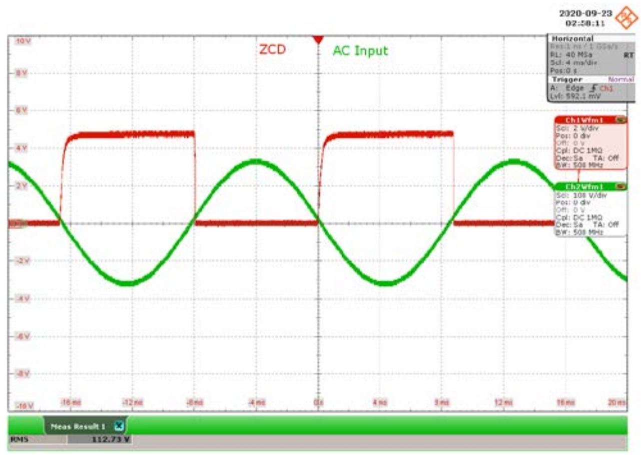

Figure 24 – 115 VAC 60 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

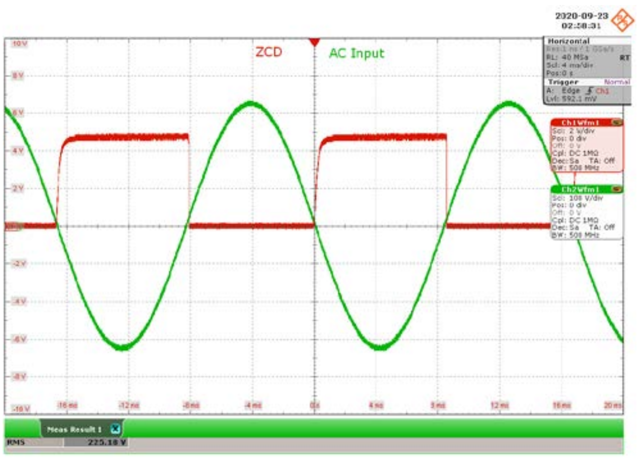

Figure 25 – 230 VAC 50 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

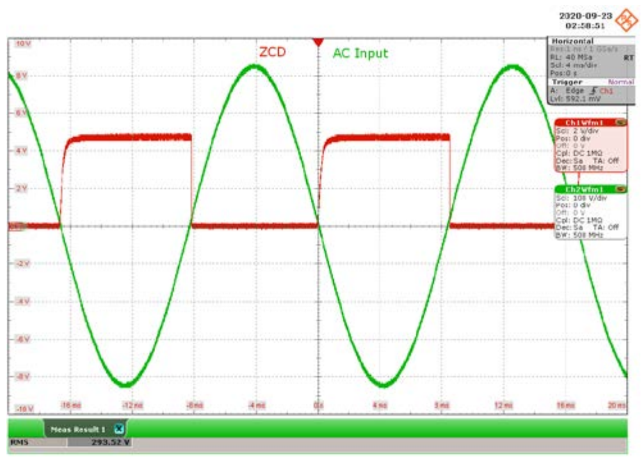

Figure 26 – 300 VAC 50 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

11.1.1.2 0% Load

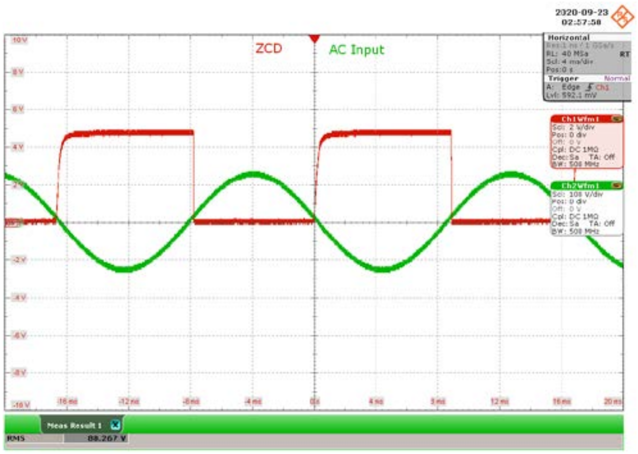

Figure 27 – 90 VAC 60 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

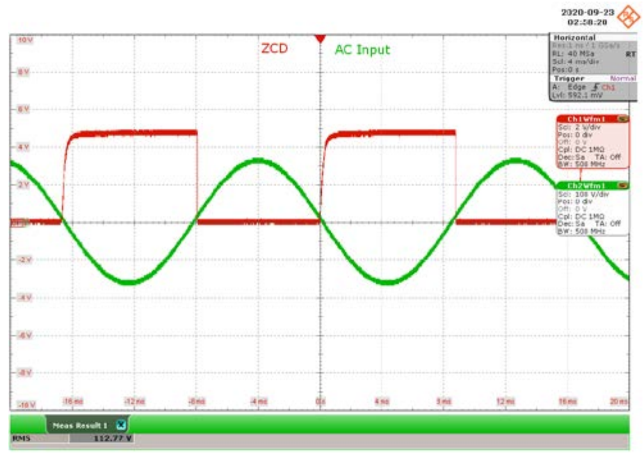

Figure 28 – 115 VAC 60 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

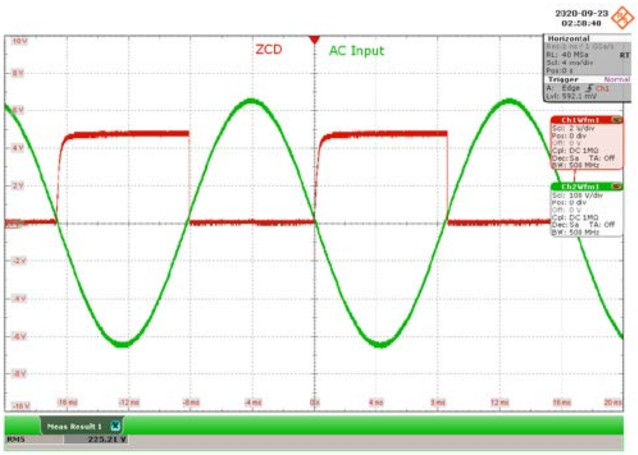

Figure 29 – 230 VAC 50 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

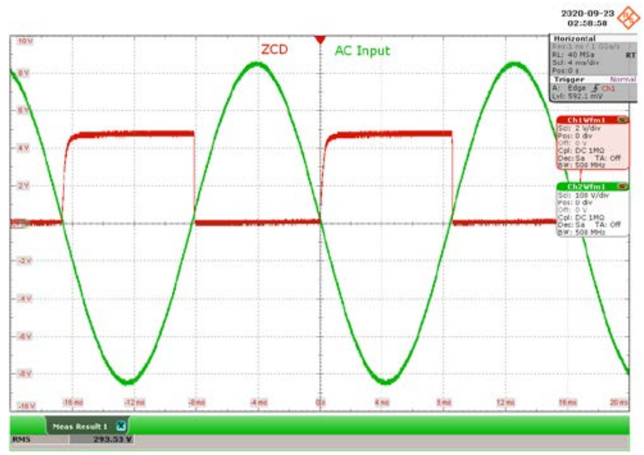

Figure 30 – 300 VAC 50 Hz.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

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11.1.2 Zero Crossing Detection at Start-up

11.1.2.1 0° Start-up Phase

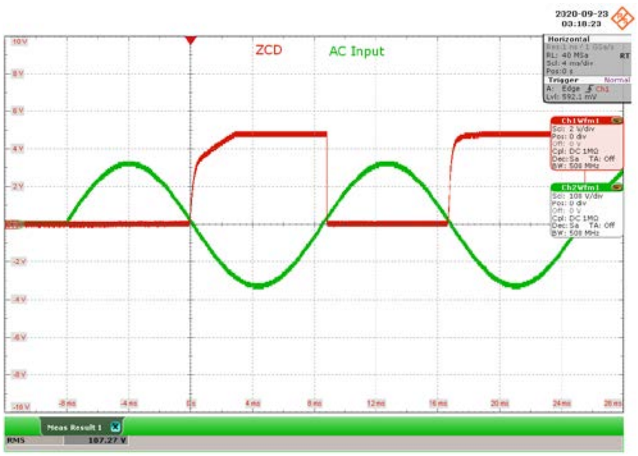

Figure 31 – 115 VAC 60 Hz, No Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

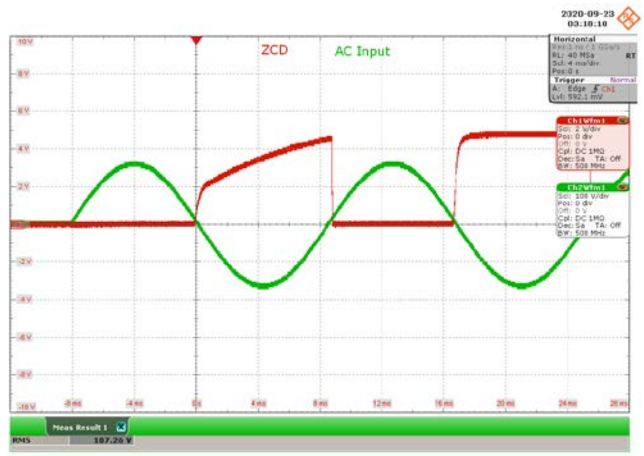

Figure 32 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

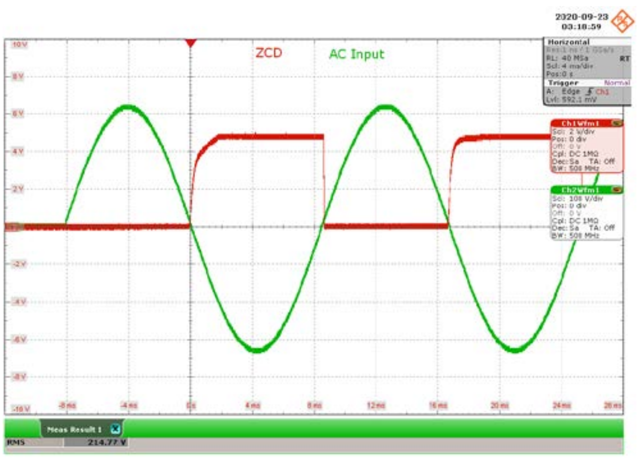

Figure 33 – 230 VAC 50 Hz, No Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

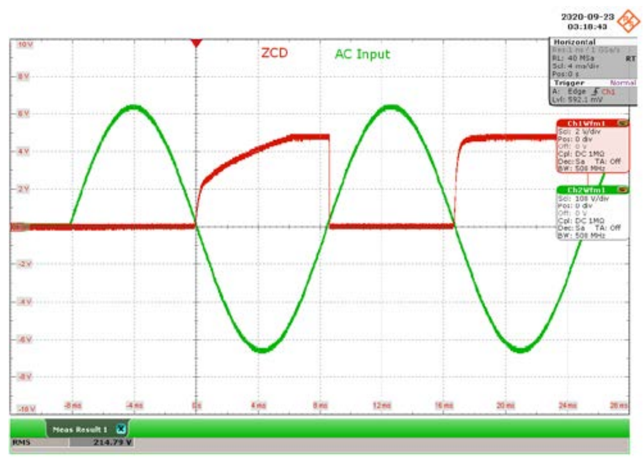

Figure 34 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: $V_{IN,}$ 100 V / div., 4 ms / div.

11.1.2.2 90° Start-up Phase

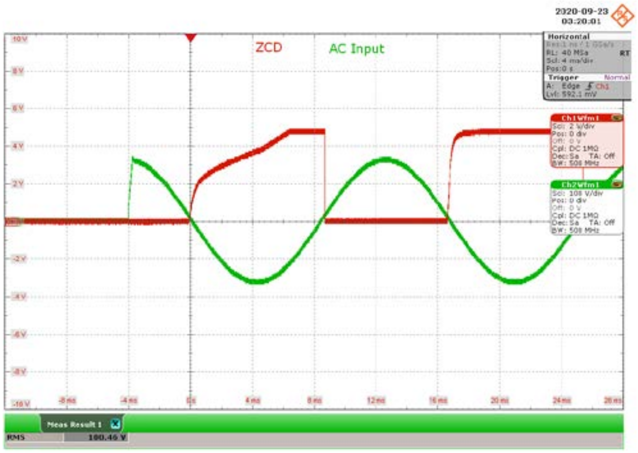

Figure 35 – 115 VAC 60 Hz, No Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

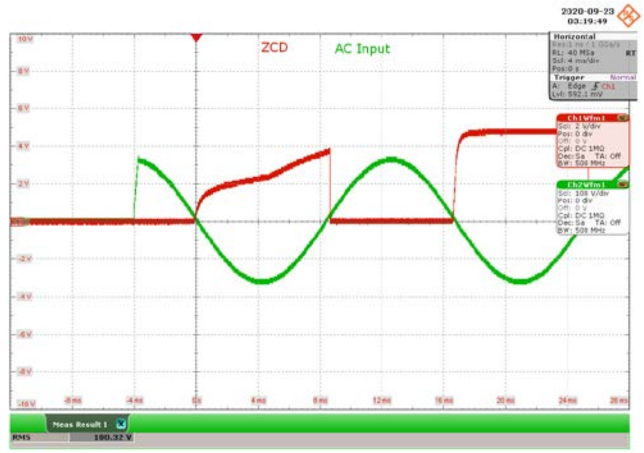

Figure 36 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

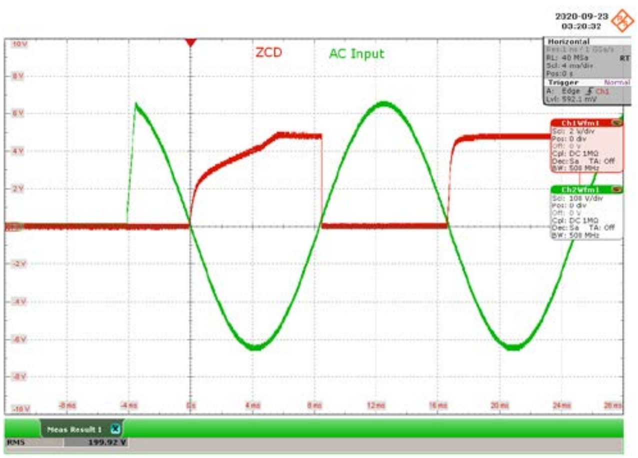

Figure 37 – 230 VAC 50 Hz, No Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

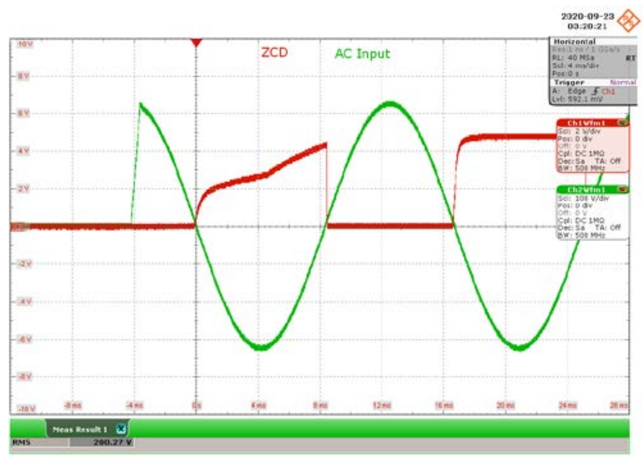

Figure 38 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.

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11.1.3 Zero Crossing Detection Delay

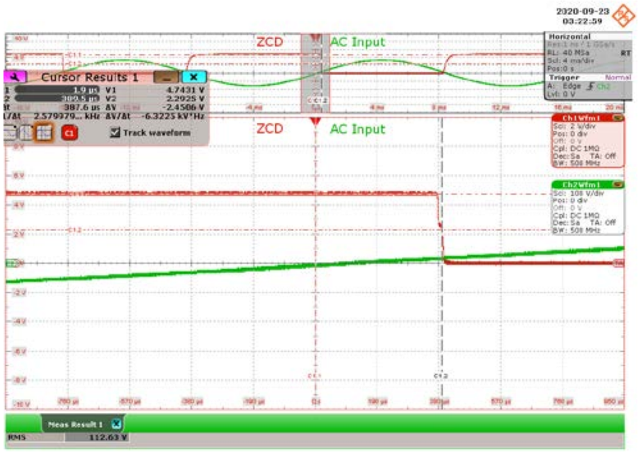

Figure 39 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.
Falling Edge Delay = 387.6 µs.

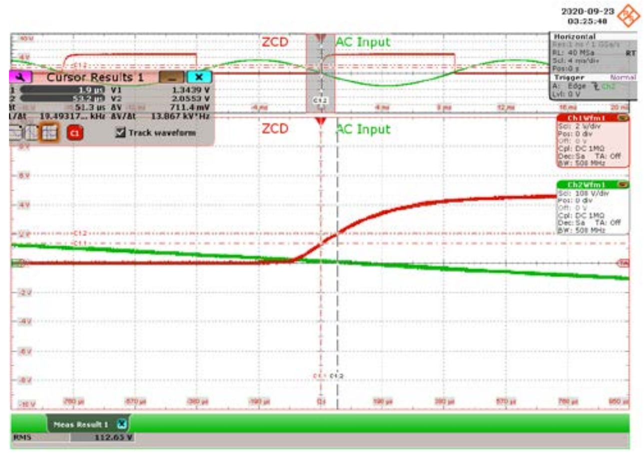

Figure 40 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.
Rising Edge Delay = 51.3 µs.

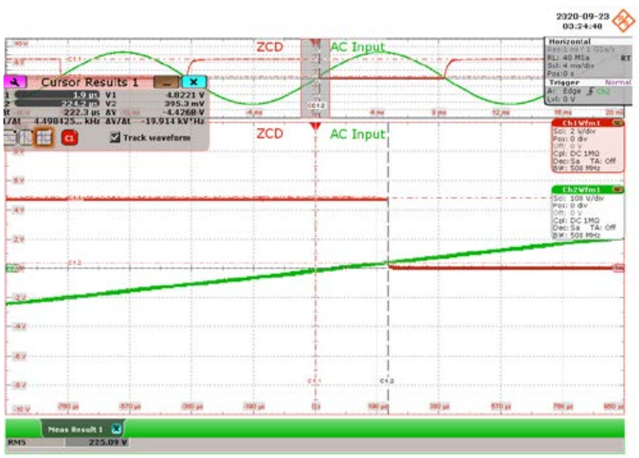

Figure 41 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.
Falling Edge Delay = 222.3 µs.

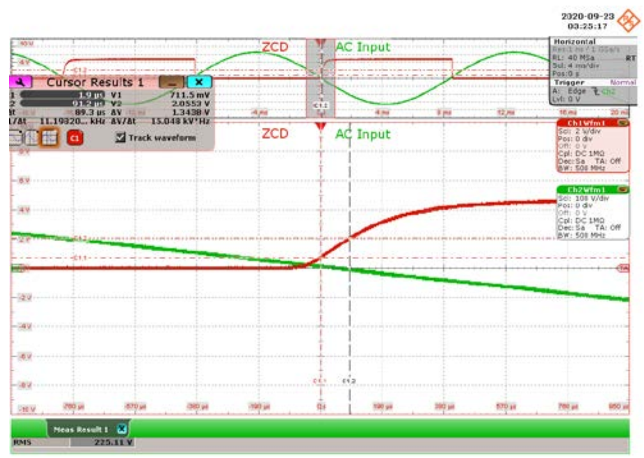

Figure 42 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 4 ms / div.
CH2: V_{IN}, 100 V / div., 4 ms / div.
Rising Edge Delay = 89.3 µs.

11.2 *Zero Crossing Detection – Without Bias Winding Configuration*

11.2.1 Zero Crossing Detection at Normal Operation

11.2.1.1 100% Load

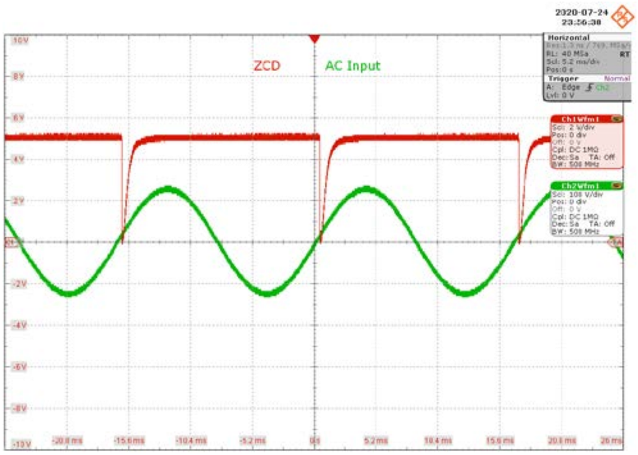

Figure 43 – 90 VAC 60 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

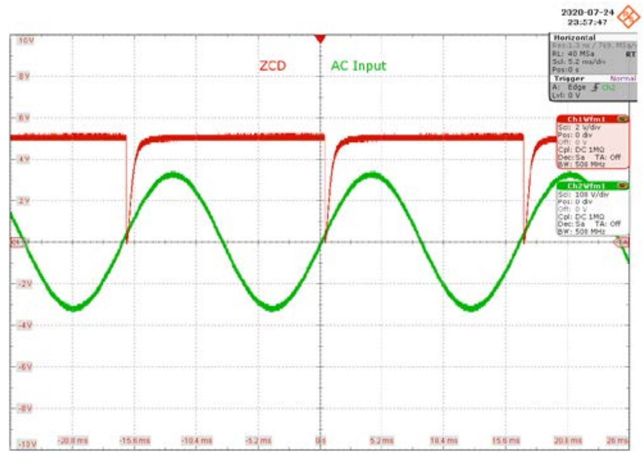

Figure 44 – 115 VAC 60 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

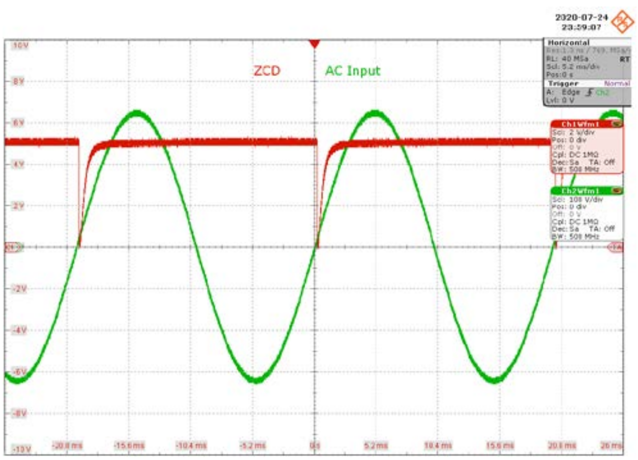

Figure 45 – 230 VAC 50 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

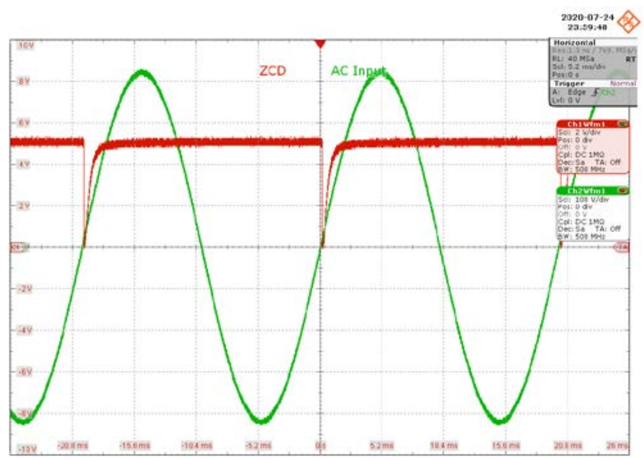

Figure 46 – 300 VAC 50 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

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11.2.1.2 0% Load

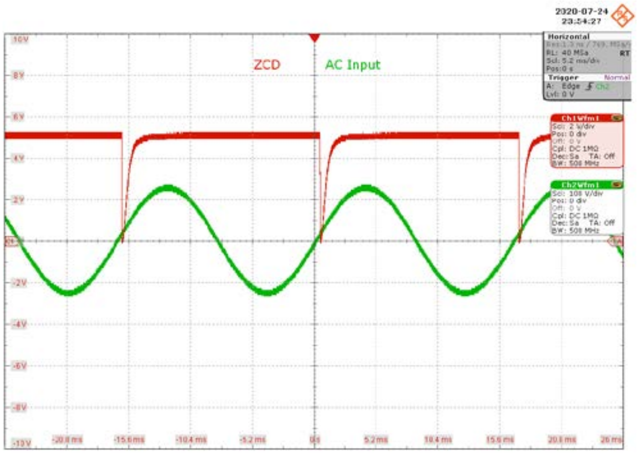

Figure 47 – 90 VAC 60 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

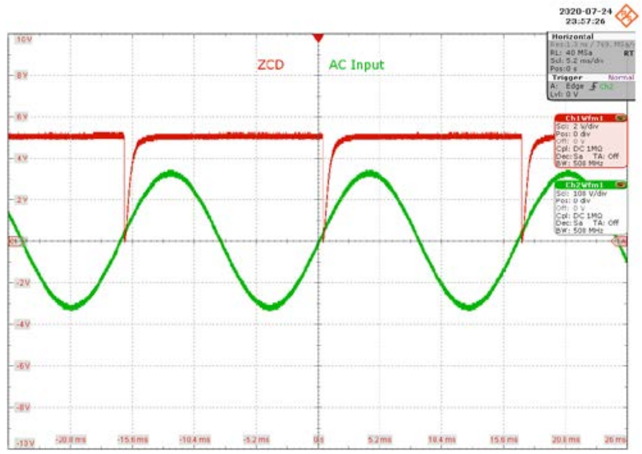

Figure 48 – 115 VAC 60 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

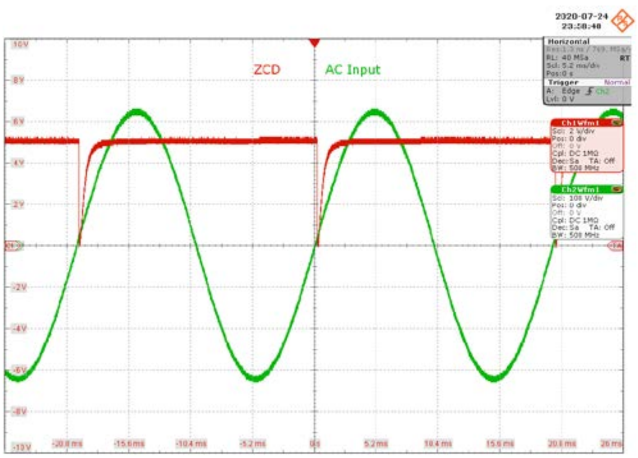

Figure 49 – 230 VAC 50 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

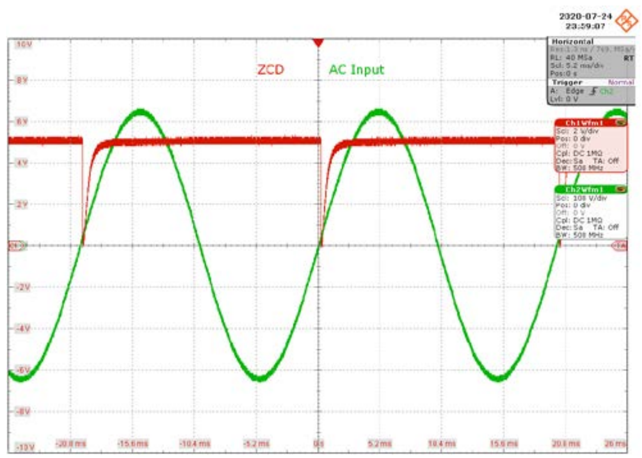

Figure 50 – 300 VAC 50 Hz.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.

11.2.2 Zero Crossing Detection at Start-up

11.2.2.1 0° Start-up Phase

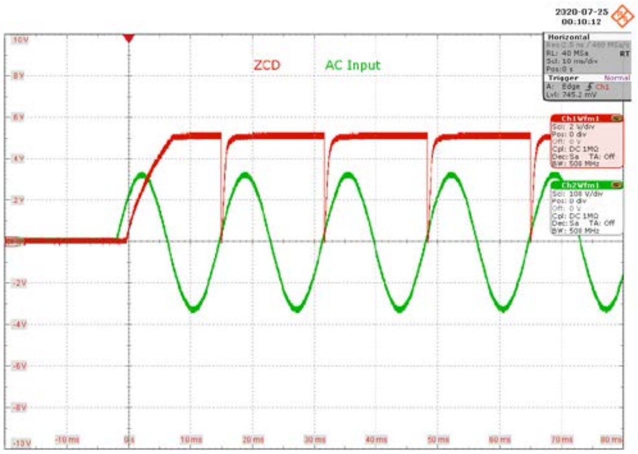

Figure 51 – 115 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

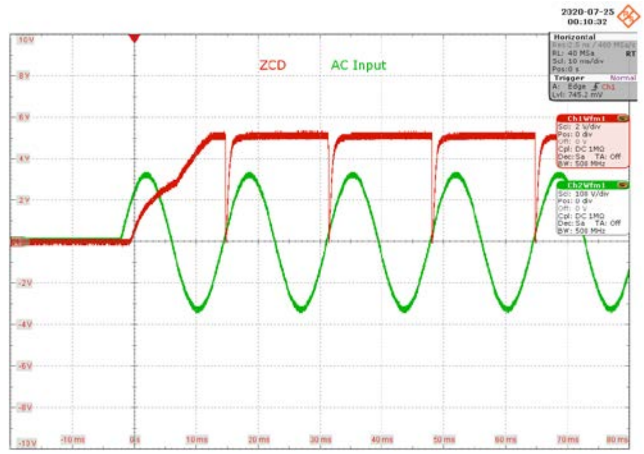

Figure 52 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

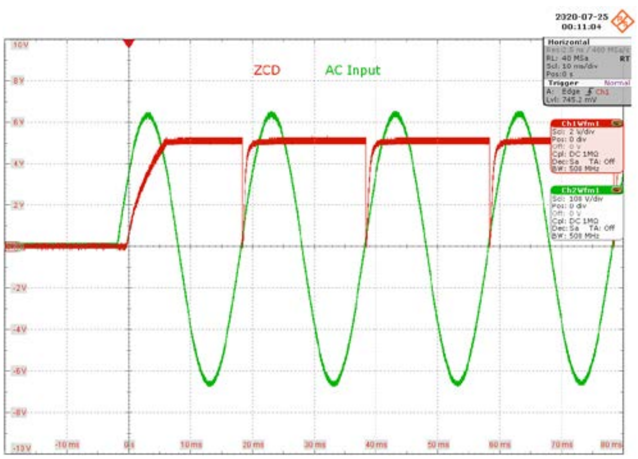

Figure 53 – 230 VAC 50 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

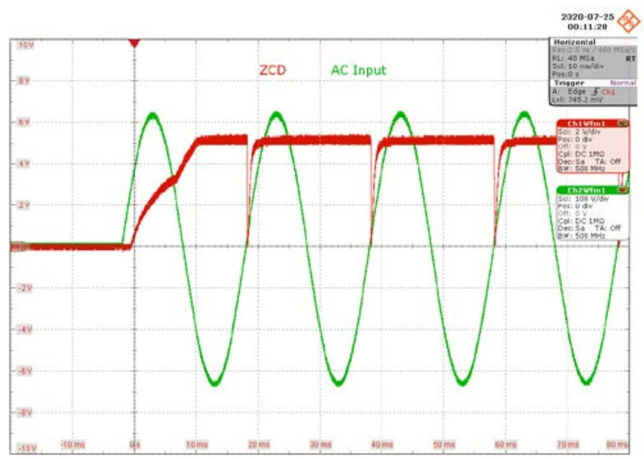

Figure 54 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

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11.2.2.2 90° Start-up Phase

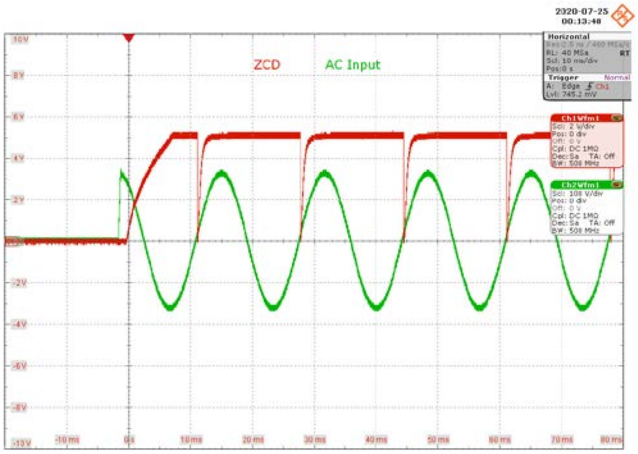

Figure 55 – 115 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

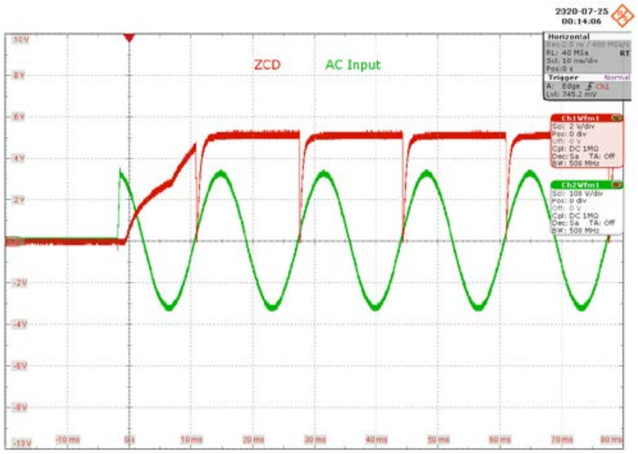

Figure 56 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

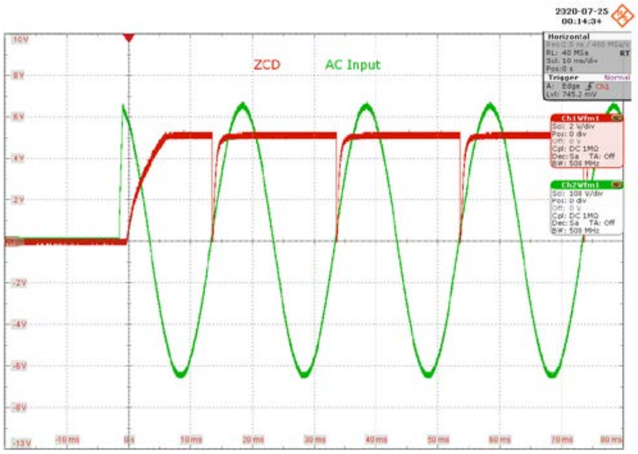

Figure 57 – 230 VAC 50 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

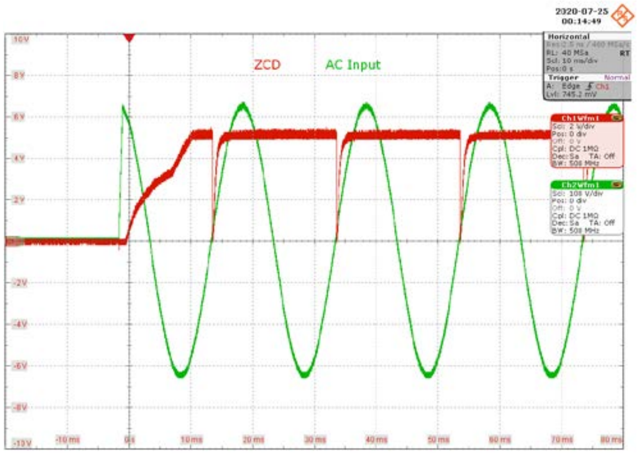

Figure 58 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH2: V_{IN}, 100 V / div., 10 ms / div.

11.2.3 Zero Crossing Detection Delay

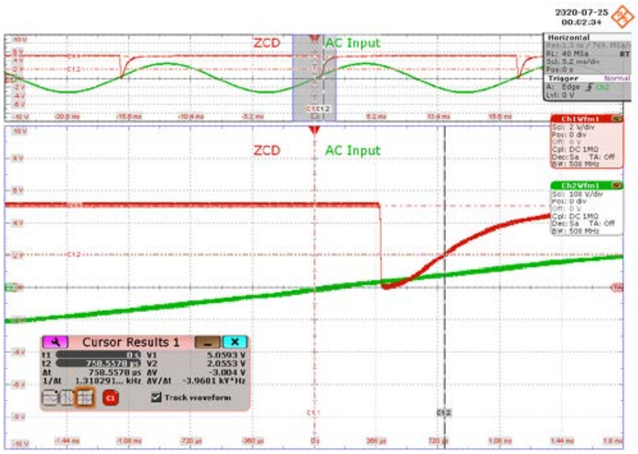

Figure 59 – 115 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.
Falling Edge Delay = 758 µs.

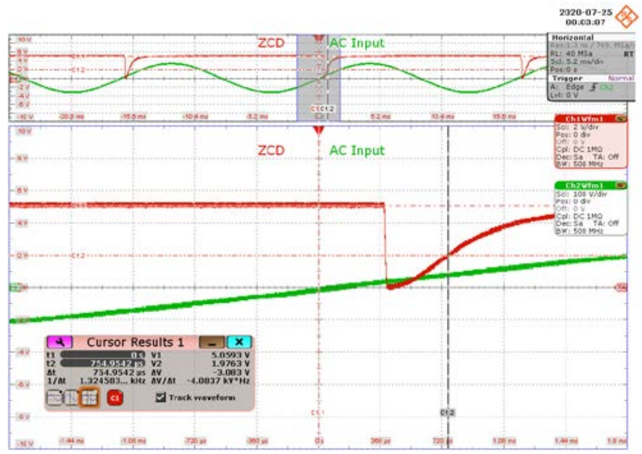

Figure 60 – 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.
Falling Edge Delay = 754 µs.

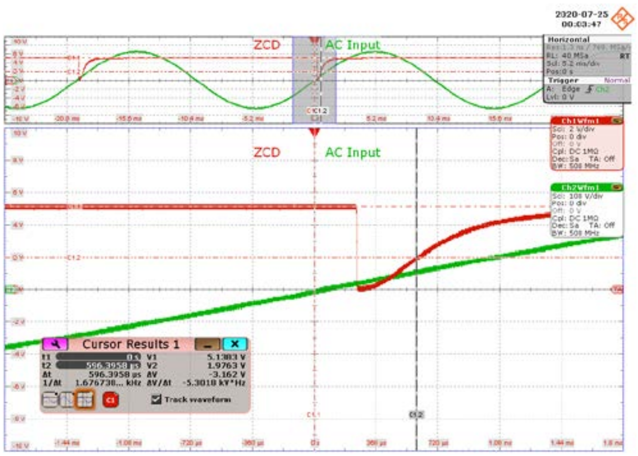

Figure 61 – 230 VAC 50 Hz, No-Load.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.
Falling Edge Delay = 596 µs.

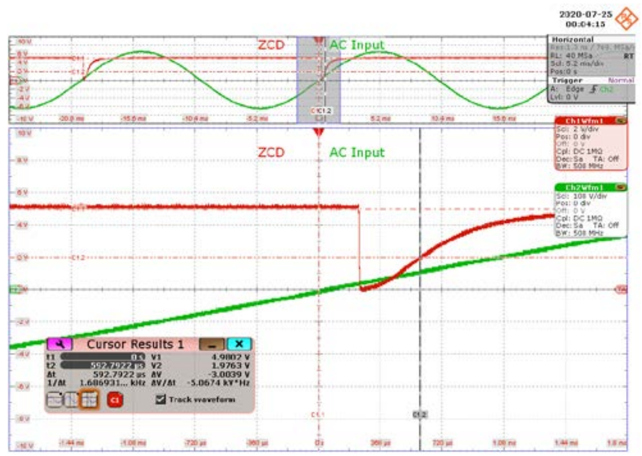

Figure 62 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 5.2 ms / div.
CH2: V_{IN}, 100 V / div., 5.2 ms / div.
Falling Edge Delay = 592 µs.

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11.3 *Load Transient Response*

11.3.1 12 V Dynamic Load

Test Condition: Dynamic load frequency = 1 kHz, Duty cycle = 50 %, 5 V at Full Load

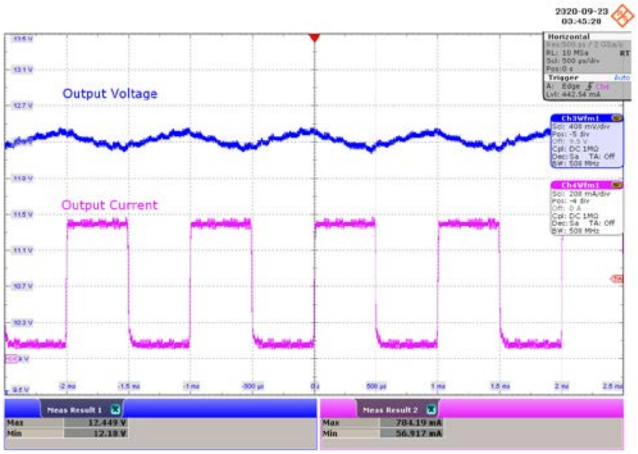

Figure 63 – 90 VAC 60 Hz.
CH3: V_{OUT}, 400 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 12.45 V, V_{MIN}: 12.18 V.

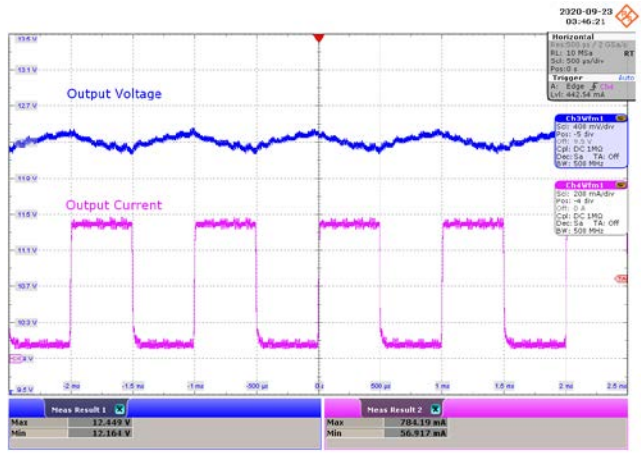

Figure 64 – 115 VAC 60 Hz.
CH3: V_{OUT}, 400 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 12.45 V, V_{MIN}: 12.16 V.

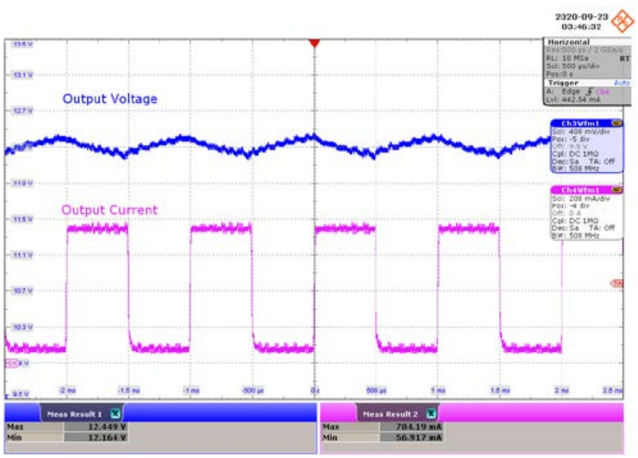

Figure 65 – 230 VAC 50 Hz.
CH3: V_{OUT}, 400 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 12.45 V, V_{MIN}: 12.16 V.

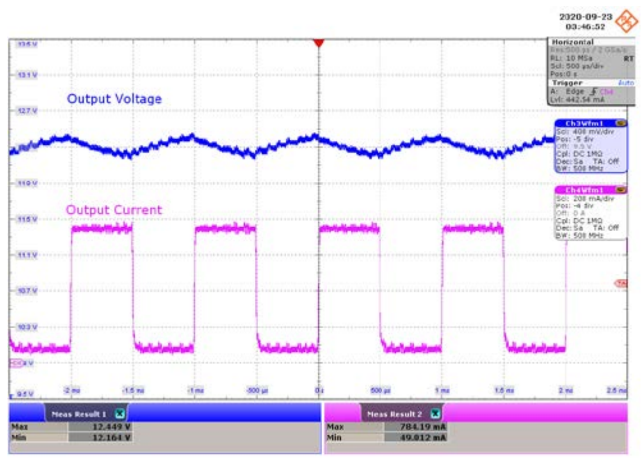

Figure 66 – 300 VAC 50 Hz.
CH3: V_{OUT}, 400 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 12.45 V, V_{MIN}: 12.16 V.

11.3.2 5 V Dynamic Load

Test Condition: Dynamic load frequency = 1 kHz, Duty cycle = 50 %, 12 V at Full Load

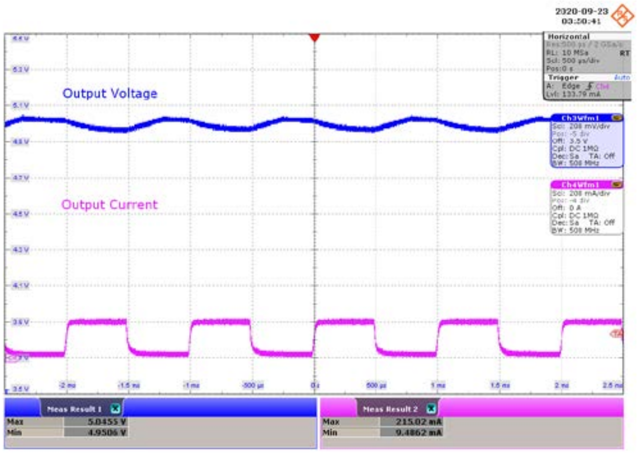

Figure 67 – 90 VAC 60 Hz.
CH3: V_{OUT}, 200 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 5.05 V, V_{MIN}: 4.95 V.

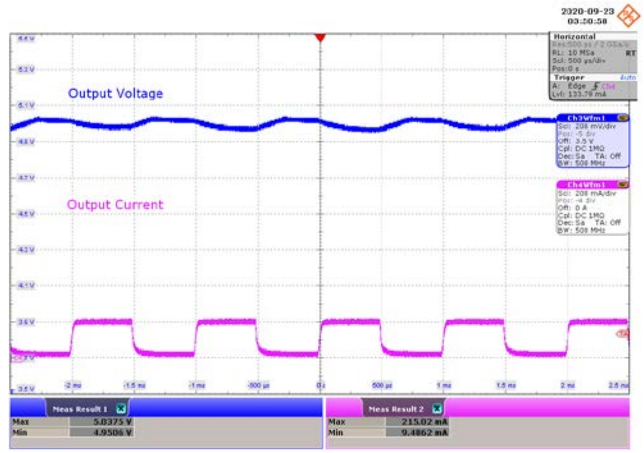

Figure 68 – 115 VAC 60 Hz.
CH3: V_{OUT}, 200 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 5.04 V, V_{MIN}: 4.95 V.

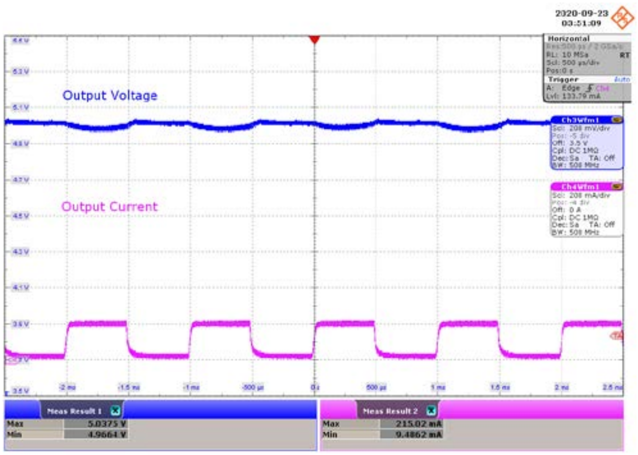

Figure 69 – 230 VAC 50 Hz.
CH3: V_{OUT}, 200 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 5.04 V, V_{MIN}: 4.97 V.

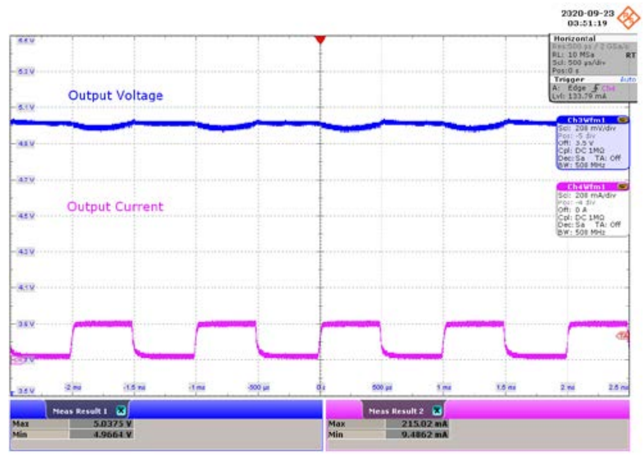

Figure 70 – 300 VAC 50 Hz.
CH3: V_{OUT}, 200 mV / div., 500 µs / div.
CH4: I_{OUT}, 200 mA / div., 500 µs / div.
V_{MAX}: 5.04 V, V_{MIN}: 4.97 V.

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11.4 *Output Voltage at Start-up*

11.4.1 12 V Start-up

Test Condition: CR = 16

11.4.2 5 V Start-up

Test Condition: CR = 16 for 12 V output, CR = 25 for 5 V output

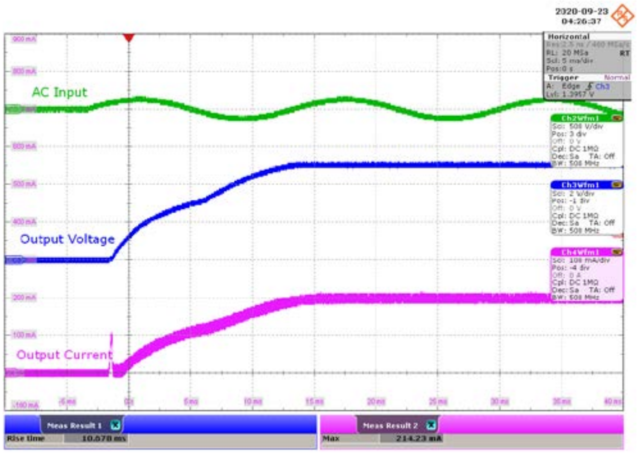

Figure 75 – 90 VAC 60 Hz.
CH2: $V_{IN,}$ 500 V / div., 5 ms / div.
CH3: $V_{OUT,}$ 2 V / div., 5 ms / div.
CH4: I_{OUT}, 100 mA / div., 5 ms / div.
Rise Time = 10.68 ms.

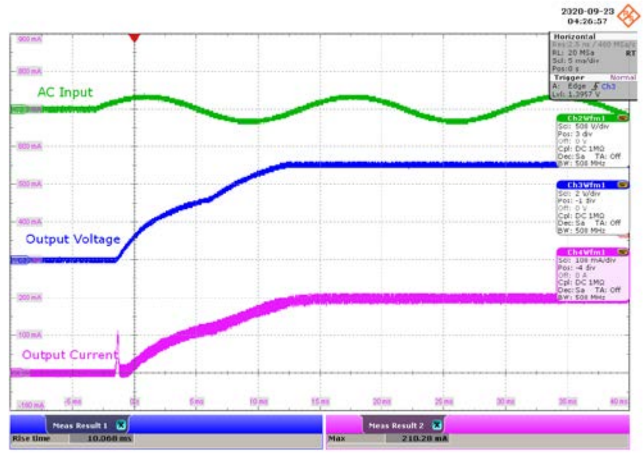

Figure 76 – 115 VAC 60 Hz.
CH2: $V_{IN,}$ 500 V / div., 5 ms / div.
CH3: $V_{OUT,}$ 2 V / div., 5 ms / div.
CH4: I_{OUT}, 100 mA / div., 5 ms / div.
Rise Time = 10.07 ms.

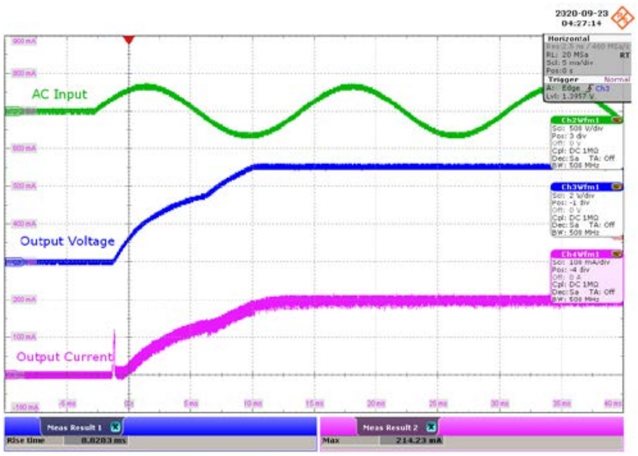

Figure 77 – 230 VAC 50 Hz.
CH2: $V_{IN,}$ 500 V / div., 5 ms / div.
CH3: $V_{OUT,}$ 2 V / div., 5 ms / div.
CH4: I_{OUT}, 100 mA / div., 5 ms / div.
Rise Time = 8.83 ms.

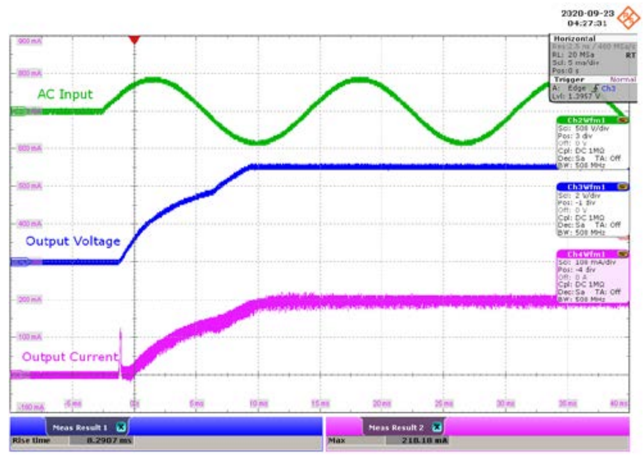

Figure 78 – 300 VAC 50 Hz.
CH2: $V_{IN,}$ 500 V / div., 5 ms / div.
CH3: $V_{OUT,}$ 2 V / div., 5 ms / div.
CH4: I_{OUT}, 100 mA / div., 5 ms / div.
Rise Time = 8.29 ms.

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11.5 *Switching Waveforms*

11.5.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

11.5.1.1 100% Load

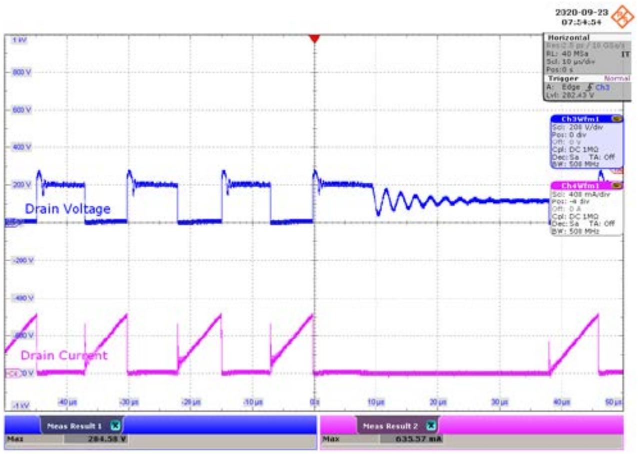

Figure 79 – 90 VAC 60 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 284.58 V.
$I_{DS(MAX)}$ = 635.57 mA.

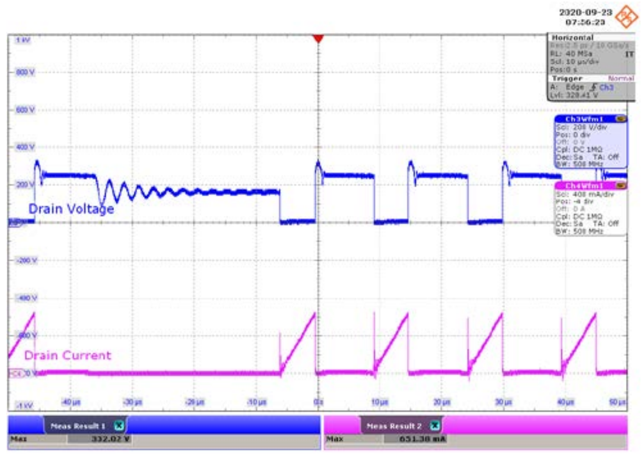

Figure 80 – 115 VAC 60 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 332.02 V.
$I_{DS(MAX)}$ = 651.38 mA.

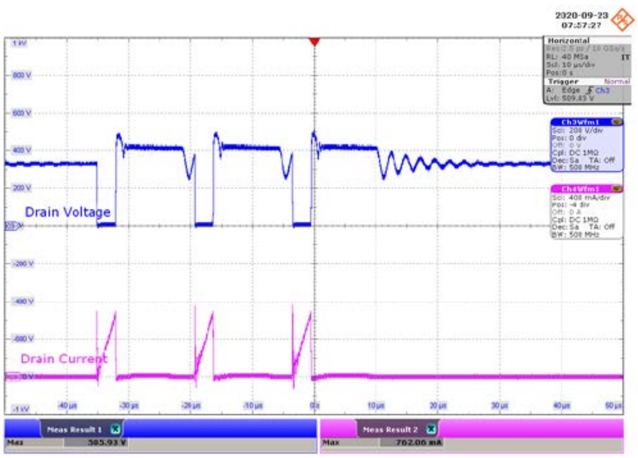

Figure 81 – 230 VAC 50 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 505.93 V.
$I_{DS(MAX)}$ = 762.06 mA.

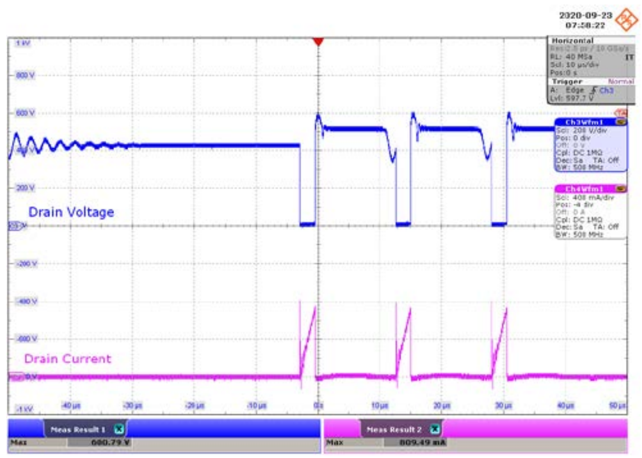

Figure 82 – 300 VAC 50 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 600.79 V.
$I_{DS(MAX)}$ = 804.49 mA.

11.5.1.2 0% Load

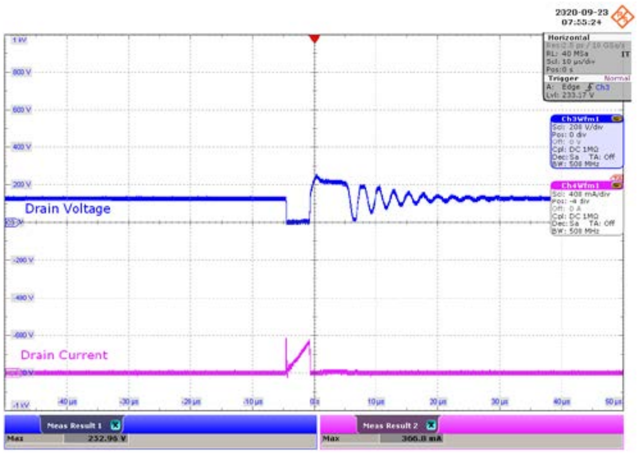

Figure 83 – 90 VAC 60 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 252.96 V.
$I_{DS(MAX)}$ = 366.8 mA.

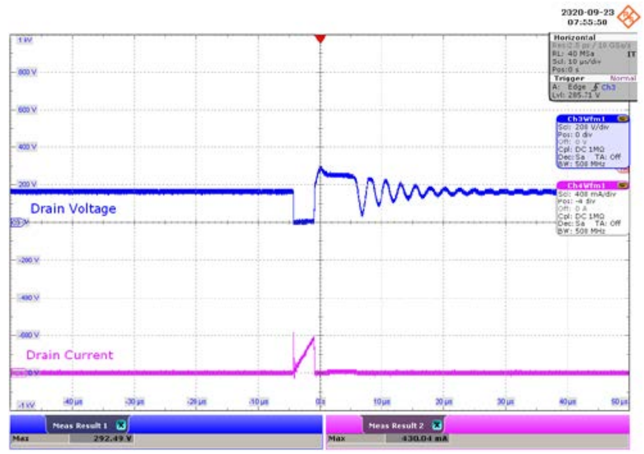

Figure 84 – 115 VAC 60 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 292.49 V.
$I_{DS(MAX)}$ = 430.04 mA.

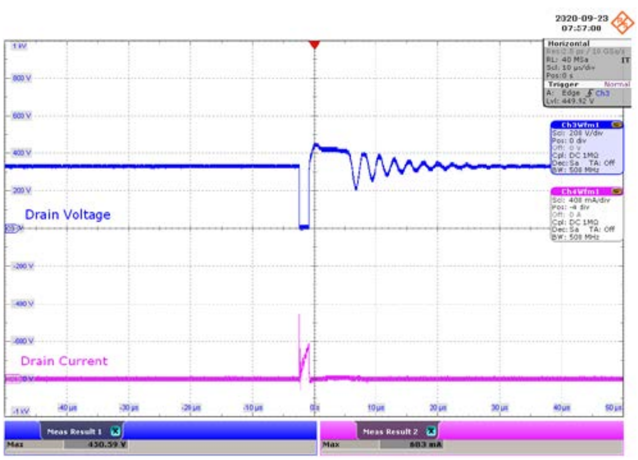

Figure 85 – 230 VAC 50 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 450.59 V.
$I_{DS(MAX)}$ = 683.00 mA.

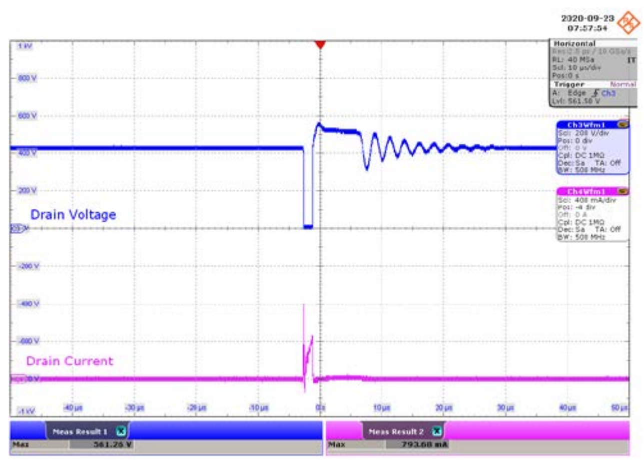

Figure 86 – 300 VAC 50 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 561.26 V.
$I_{DS(MAX)}$ = 793.68 mA.

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11.5.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

11.5.2.1 100% Load

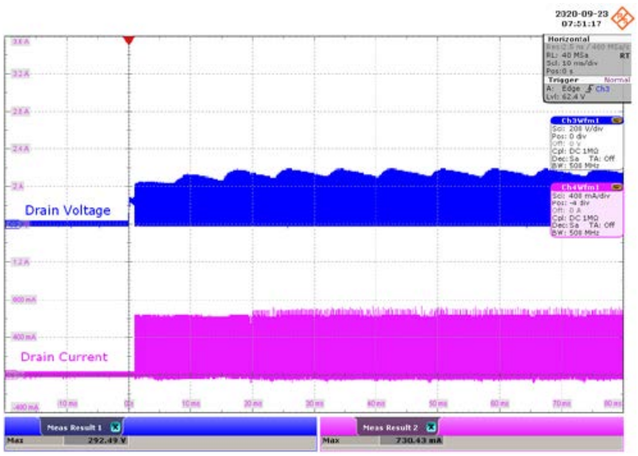

Figure 87 – 90 VAC 60 Hz.
CH3: V_{DS}, 200 V / div., 10 ms / div.
CH4: I_{DS}, 400 mA / div., 10 ms / div.
$V_{DS(MAX)}$ = 292.49 V.
$I_{DS(MAX)}$ = 730.43 mA.

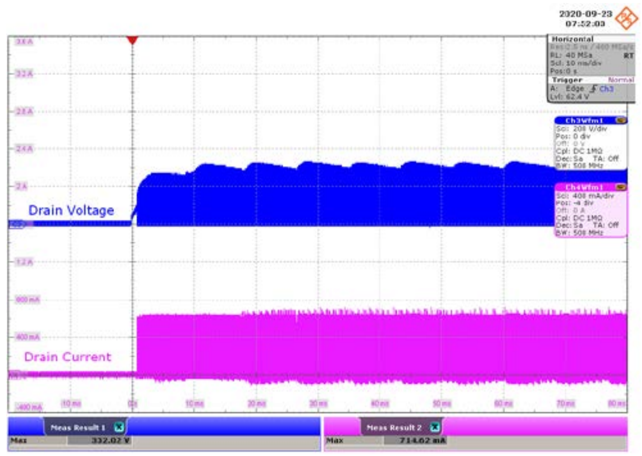

Figure 88 – 115 VAC 60 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 332.02 V.
$I_{DS(MAX)}$ = 714.62 mA.

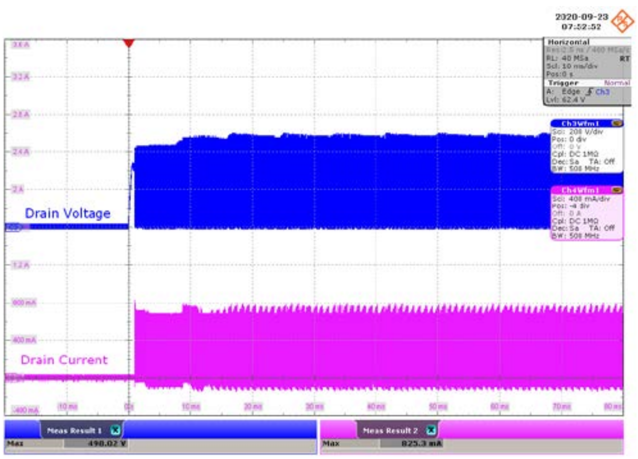

Figure 89 – 230 VAC 50 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 498.02 V.
$I_{DS(MAX)}$ = 825.3 mA.

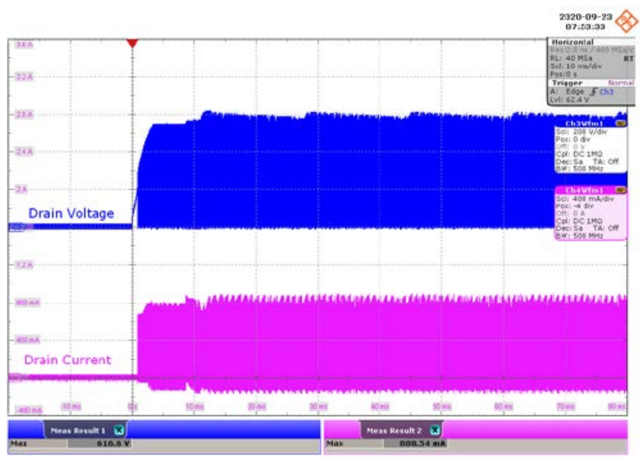

Figure 90 – 300 VAC 50 Hz.
CH3: V_{DS}, 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 616.6 V.
$I_{DS(MAX)}$ = 888.54 mA.

11.5.2.2 0% Load

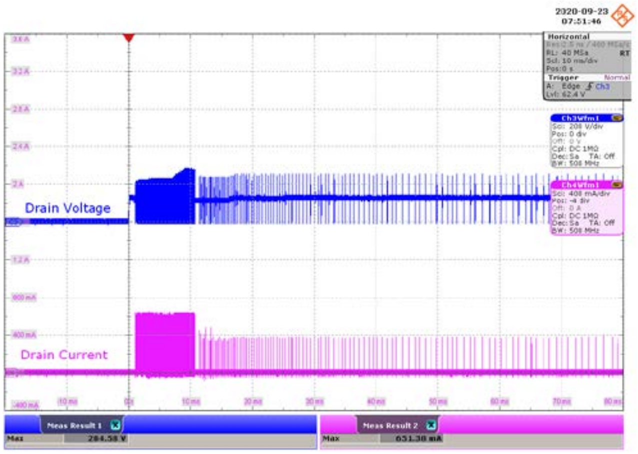

Figure 91 – 90 VAC 60 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 284.58 V.
$I_{DS(MAX)}$ = 651.38 mA.

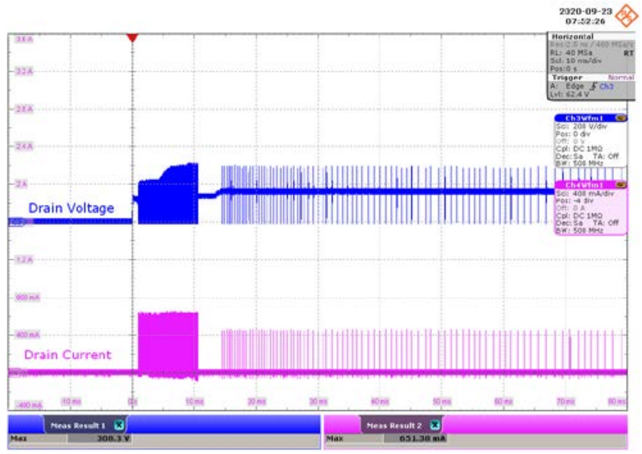

Figure 92 – 115 VAC 60 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 308.3 V.
$I_{DS(MAX)}$ = 651.38 mA.

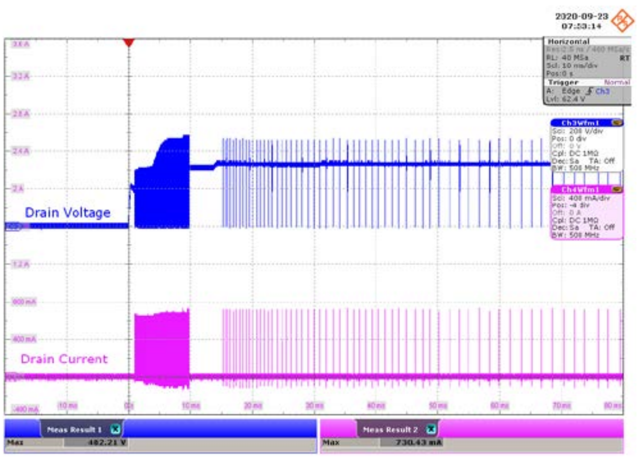

Figure 93 – 230 VAC 50 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 482.21 V.
$I_{DS(MAX)}$ = 730.43 mA.

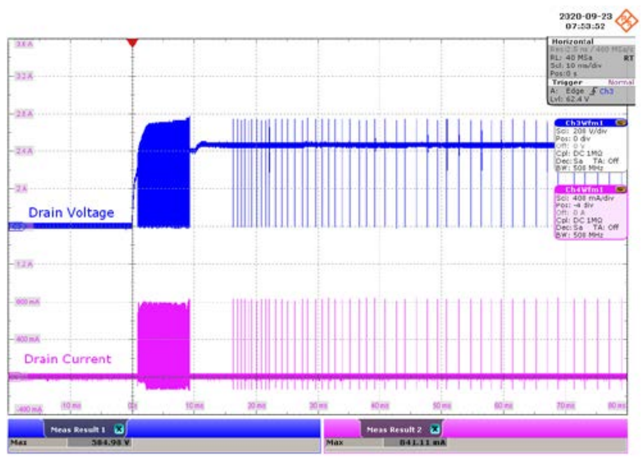

Figure 94 – 300 VAC 50 Hz.
CH3: $V_{DS,}$ 200 V / div., 10 µs / div.
CH4: I_{DS}, 400 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 584.98 V.
$I_{DS(MAX)}$ = 841.11 mA.

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11.5.3 12 V Output Diode Voltage and Current at Normal Operation

11.5.3.1 100% Load

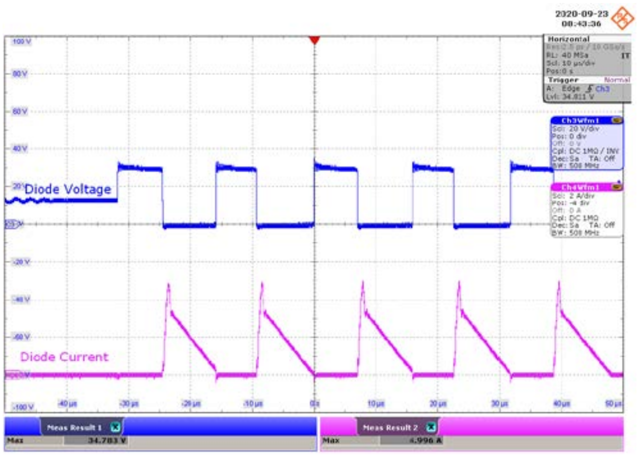

Figure 95 – 90 VAC 60 Hz.
CH3: $V_{D,}$ 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 34.78 V.
$I_{D(MAX)}$ = 5.00 A.

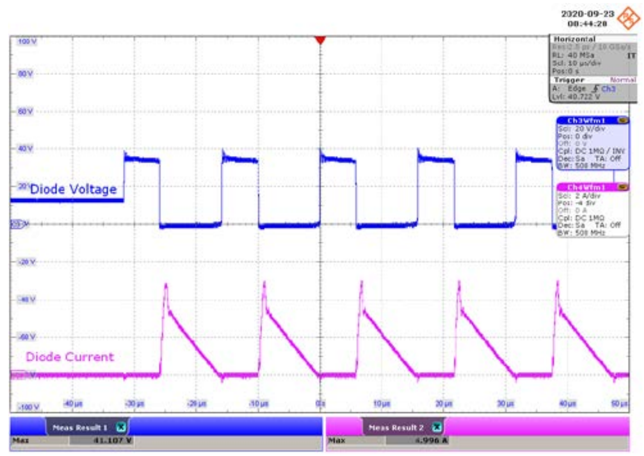

Figure 96 – 115 VAC 60 Hz.
CH3: $V_{D,}$ 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 41.11 V.
$I_{D(MAX)}$ = 5.0 A.

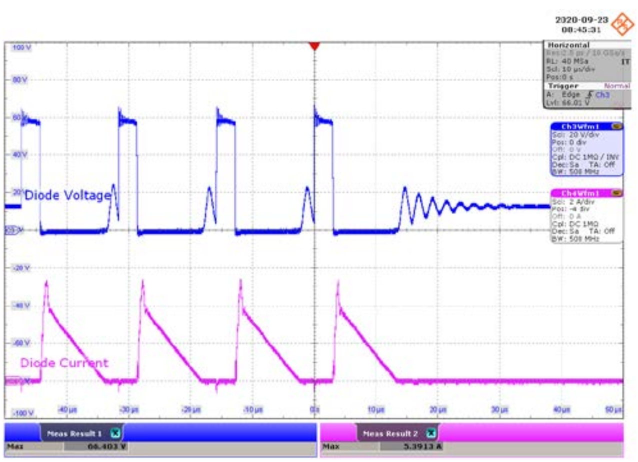

Figure 97 – 230 VAC 50 Hz.
CH3: $V_{D,}$ 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 66.40 V.
$I_{D(MAX)}$ = 5.39 A.

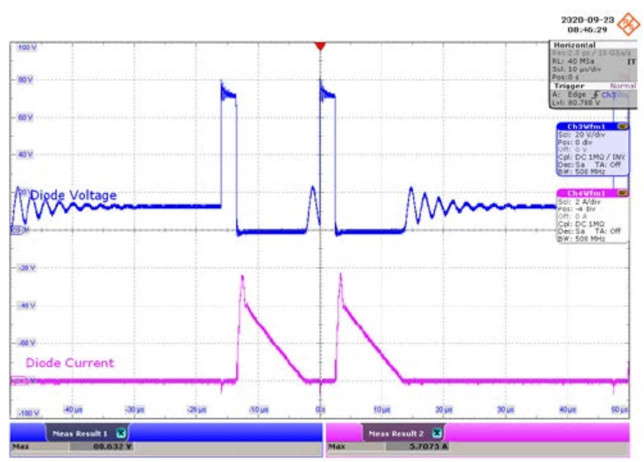

Figure 98 – 300 VAC 50 Hz.
CH3: $V_{D,}$ 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 80.63 V.
$I_{D(MAX)}$ = 5.71 A.

11.5.3.2 0% Load

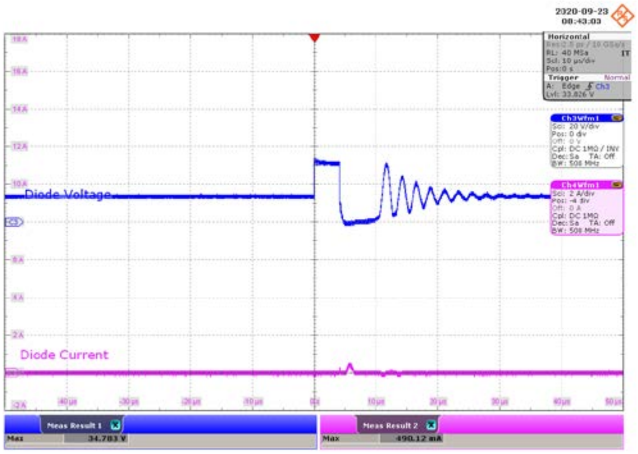

Figure 99 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 34.78 V.
$I_{D(MAX)}$ = 0.49 A.

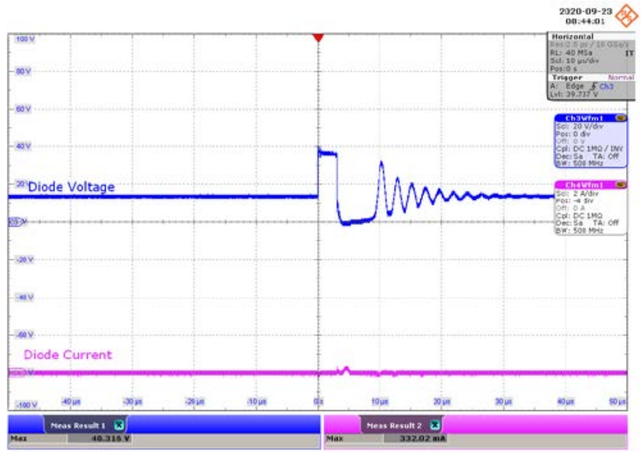

Figure 100 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 40.32 V.
$I_{D(MAX)}$ = 0.33 A.

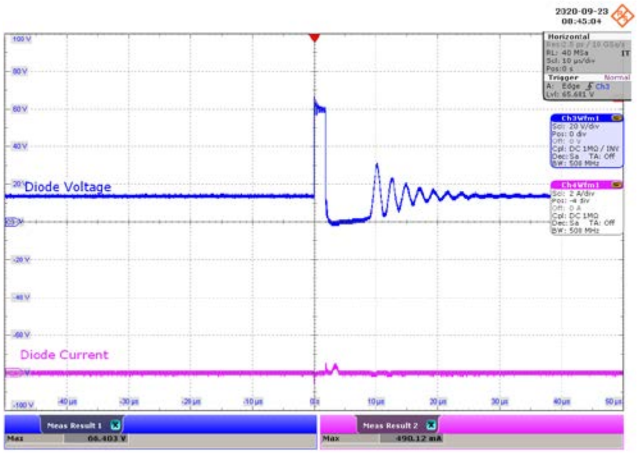

Figure 101 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 66.40 V.
$I_{D(MAX)}$ = 0.49 A.

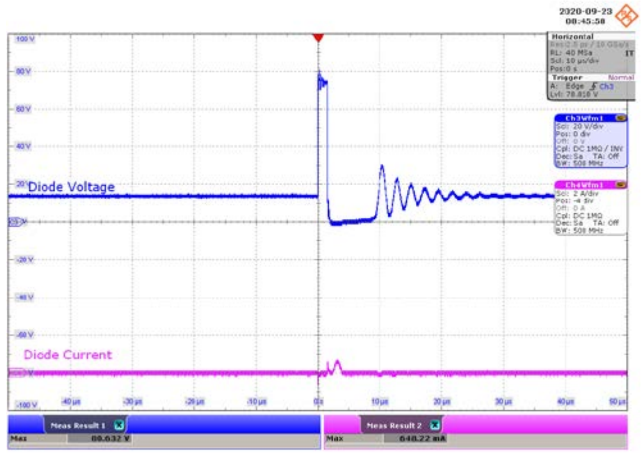

Figure 102 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 2 A / div., 10 µs / div.
PIV = 80.63 V.
$I_{D(MAX)}$ = 0.65 A.

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11.5.4 12 V Output Diode Voltage and Current at Start-up Operation

11.5.4.1 100% Load

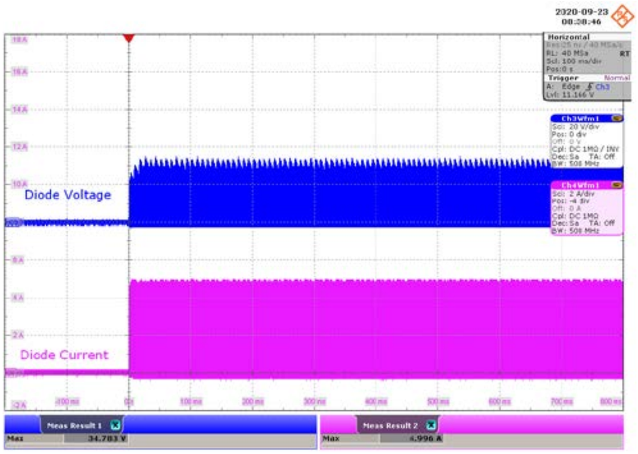

Figure 103 – 90 VAC 60 Hz.
CH3: $V_{D,}$ 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 34.78 V.
$I_{D(MAX)}$ = 5.00 A.

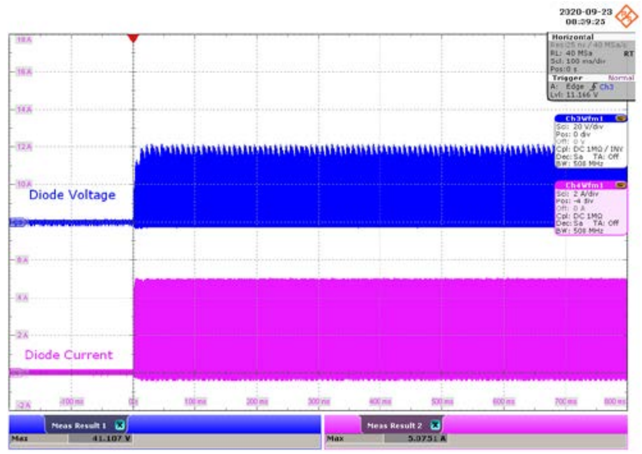

Figure 104 – 115 VAC 60 Hz.
CH3: $V_{D,}$ 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 41.11 V.
$I_{D(MAX)}$ = 5.08 A.

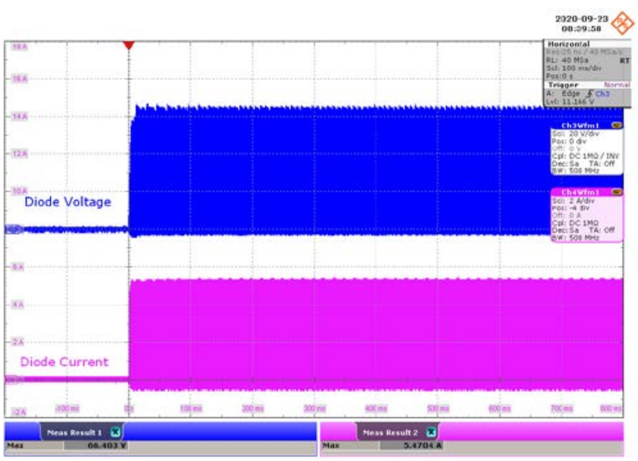

Figure 105 – 230 VAC 50 Hz.
CH3: $V_{D,}$ 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 66.40 V.
$I_{D(MAX)}$ = 5.47 A.

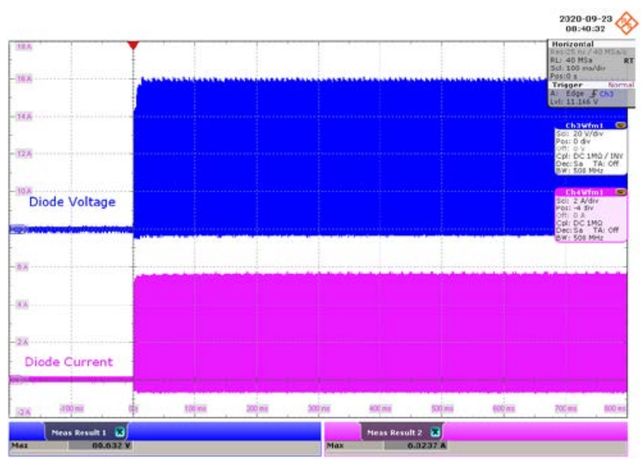

Figure 106 – 300 VAC 50 Hz.
CH3: $V_{D,}$ 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 80.63 V.
$I_{D(MAX)}$ = 6.02 A.

11.5.4.2 0% Load

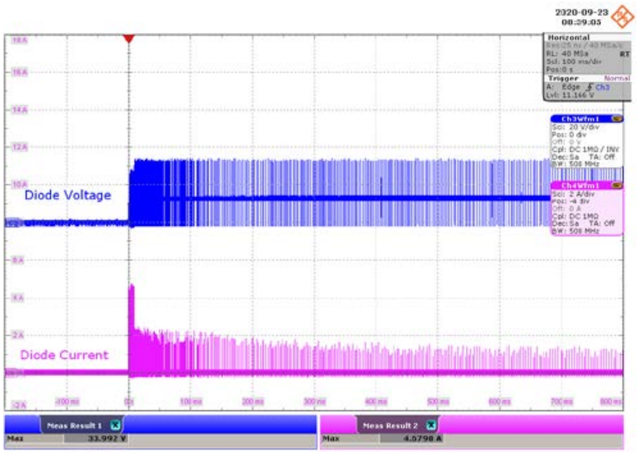

Figure 107 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 33.99 V.
$I_{D(MAX)}$ = 4.68 A.

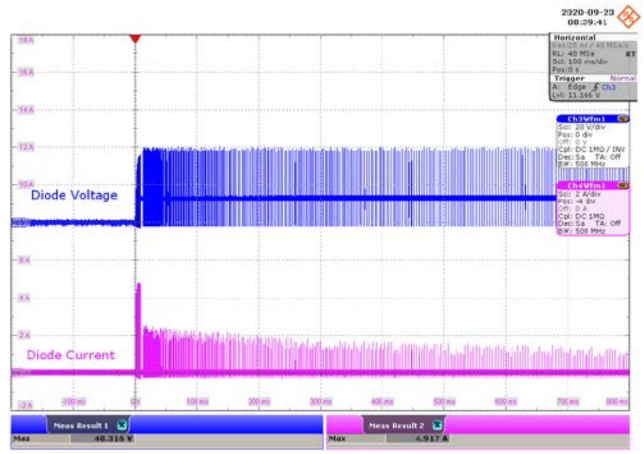

Figure 108 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 40.32 V.
$I_{D(MAX)}$ = 4.92 A.

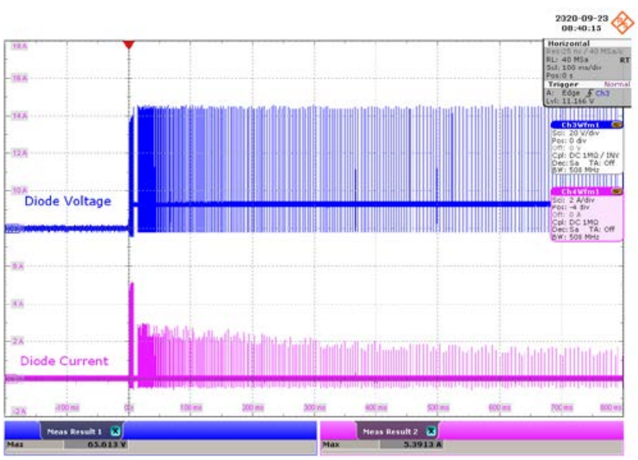

Figure 109 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 65.61 V.
$I_{D(MAX)}$ = 5.39 A.

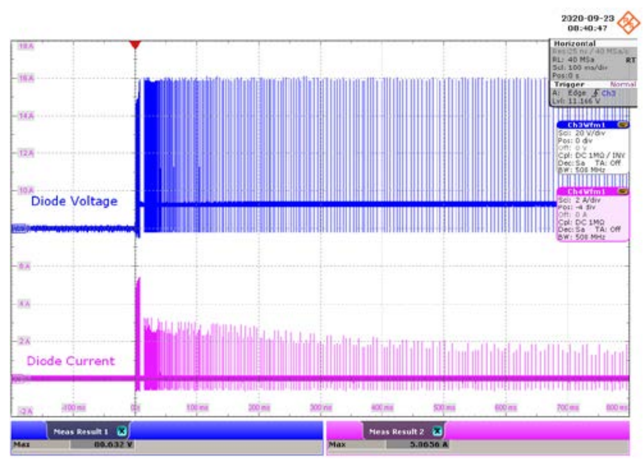

Figure 110 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 2 A / div., 100 ms / div.
PIV = 80.63 V.
$I_{D(MAX)}$ = 5.87 A.

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11.5.1 5 V Output Diode Voltage and Current at Normal Operation

11.5.1.1 100% Load

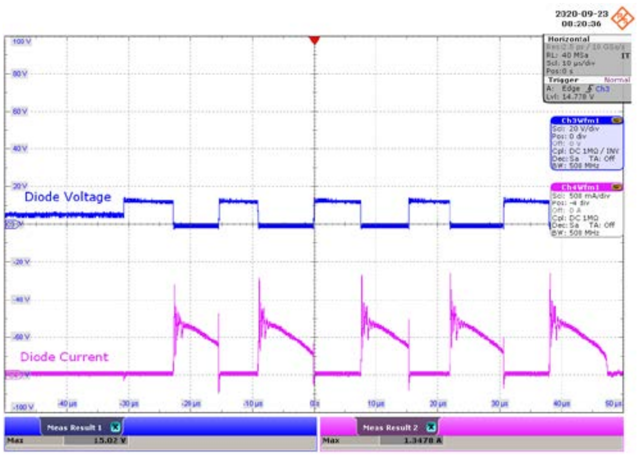

Figure 111 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 15.02 V.
$I_{D(MAX)}$ = 1.35 A.

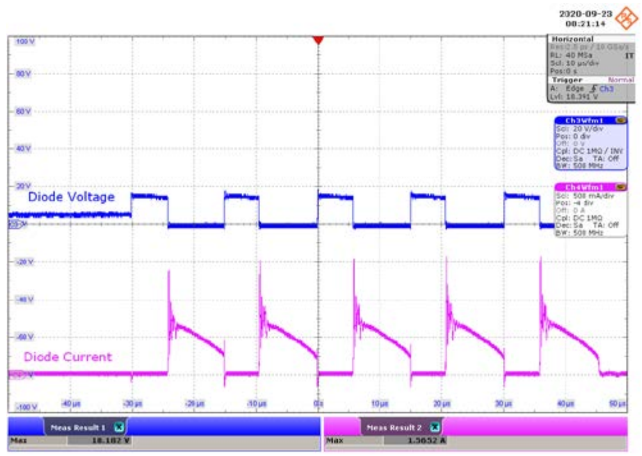

Figure 112 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 18.18 V.
$I_{D(MAX)}$ = 1.56 A.

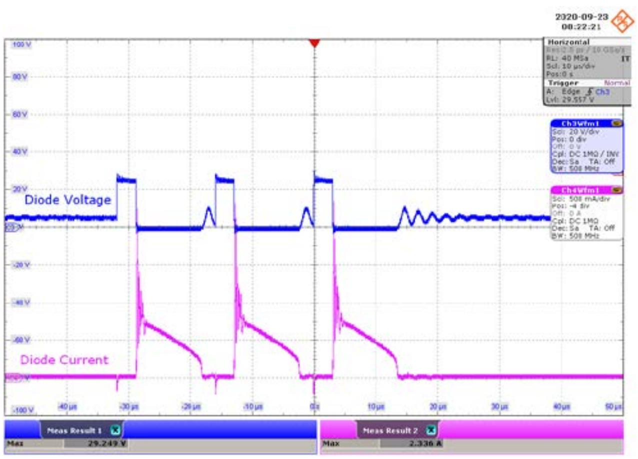

Figure 113 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 29.25 V.
$I_{D(MAX)}$ = 2.34 A.

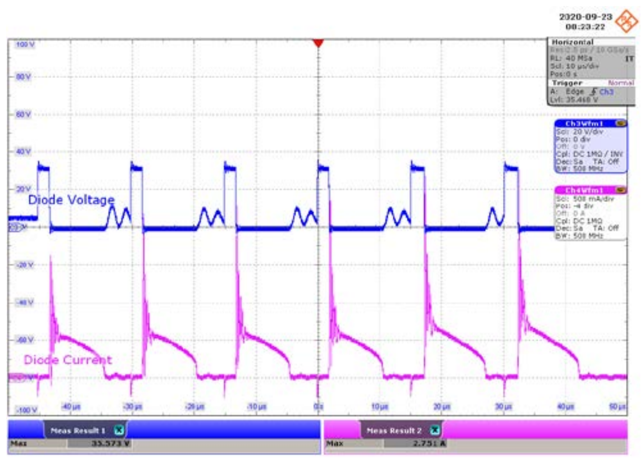

Figure 114 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 35.57 V.
$I_{D(MAX)}$ = 2.75 A.

11.5.1.2 0% Load

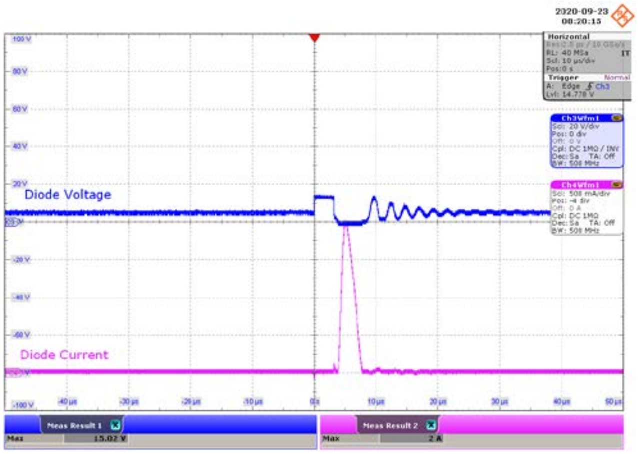

Figure 115 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 15.02 V.
$I_{D(MAX)}$ = 2.0 A.

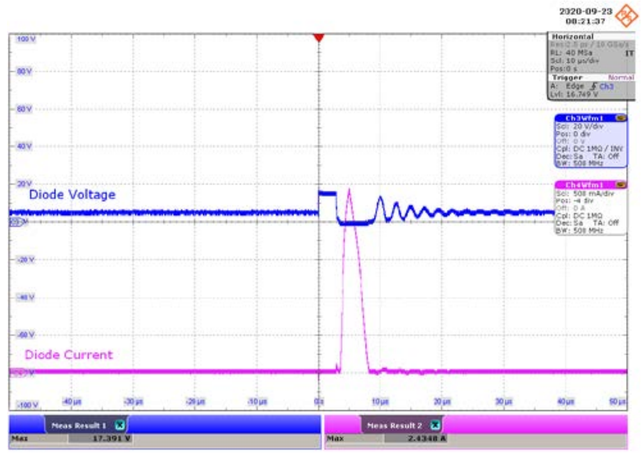

Figure 116 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 17.39 V.
$I_{D(MAX)}$ = 2.43 A.

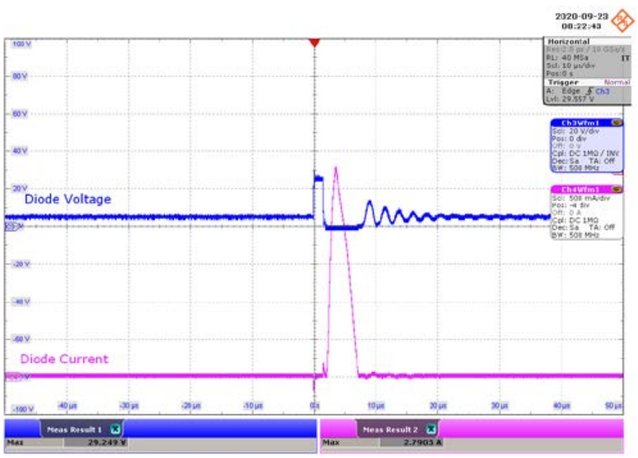

Figure 117 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 29.25 V.
$I_{D(MAX)}$ = 2.79 A.

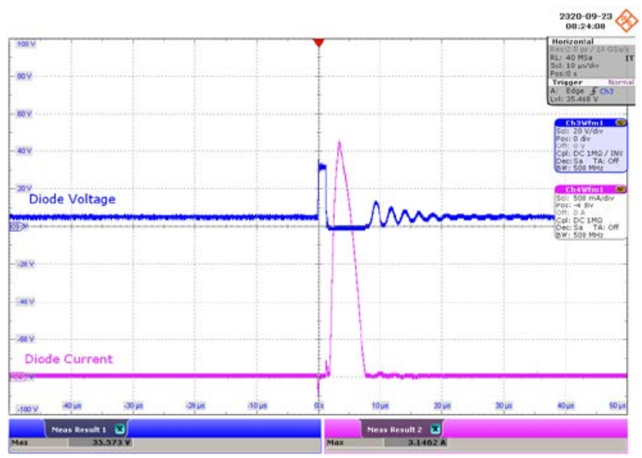

Figure 118 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 10 µs / div.
CH4: I_D, 500 mA / div., 10 µs / div.
PIV = 35.57 V.
$I_{D(MAX)}$ = 3.15 A.

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11.5.1 5 V Output Diode Voltage and Current at Start-up Operation

11.5.1.1 100% Load

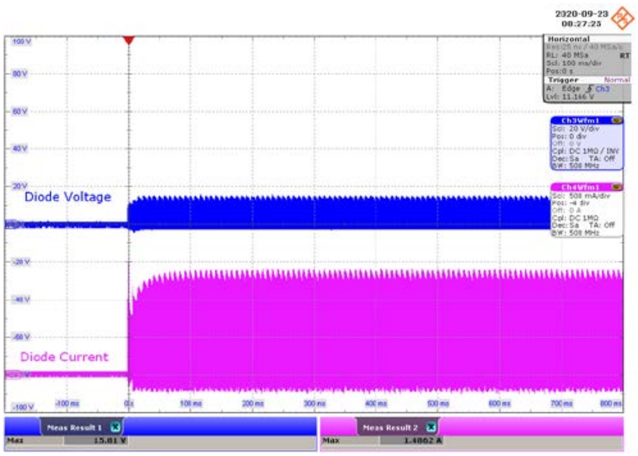

Figure 119 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 15.81 V.
$I_{D(MAX)}$ = 1.49 A.

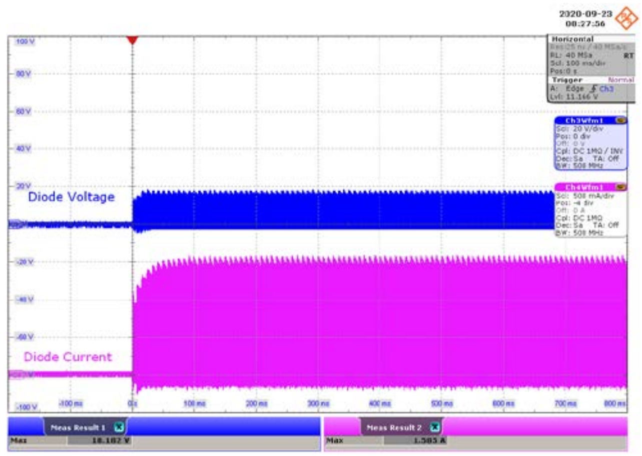

Figure 120 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 18.18 V.
$I_{D(MAX)}$ = 1.58 A.

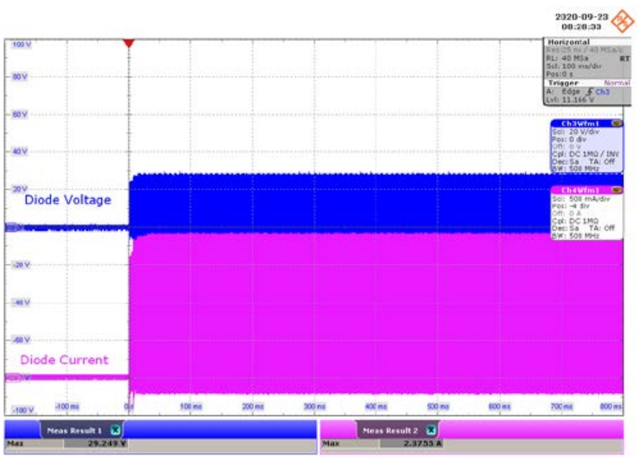

Figure 121 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 29.25 V.
$I_{D(MAX)}$ = 2.37 A.

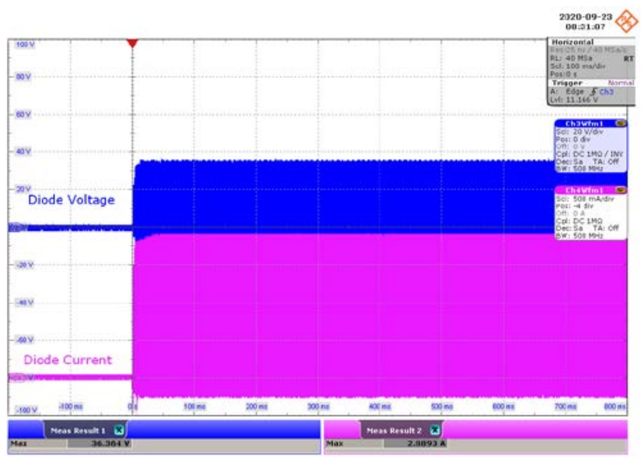

Figure 122 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 36.36 V.
$I_{D(MAX)}$ = 2.89 A.

11.5.1.2 0% Load

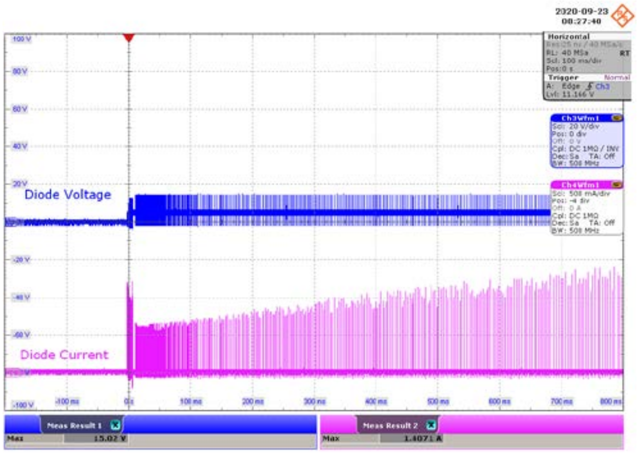

Figure 123 – 90 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 15.02 V.
$I_{D(MAX)}$ = 1.41 A.

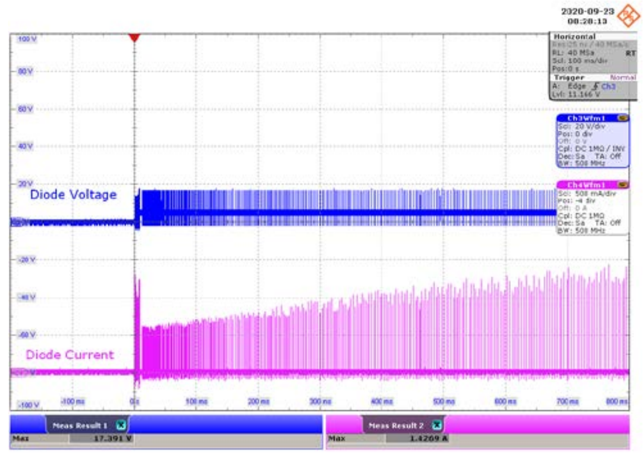

Figure 124 – 115 VAC 60 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 17.39 V.
$I_{D(MAX)}$ = 1.43 A.

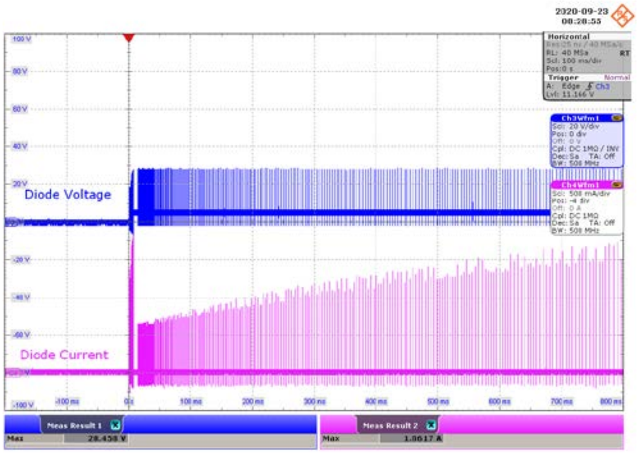

Figure 125 – 230 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 28.46 V.
$I_{D(MAX)}$ = 1.86 A.

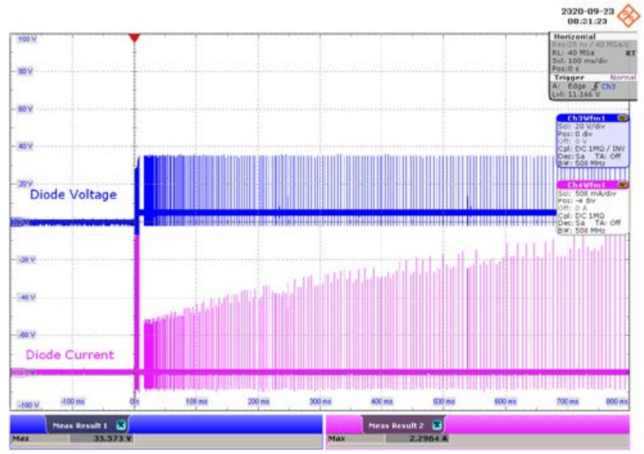

Figure 126 – 300 VAC 50 Hz.
CH3: V_D, 20 V / div., 100 ms / div.
CH4: I_D, 500 mA / div., 100 ms / div.
PIV = 35.57 V.
$I_{D(MAX)}$ = 2.30 A.

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11.6 *Brown-In and Brown-Out*

11.6.1 Brown-in

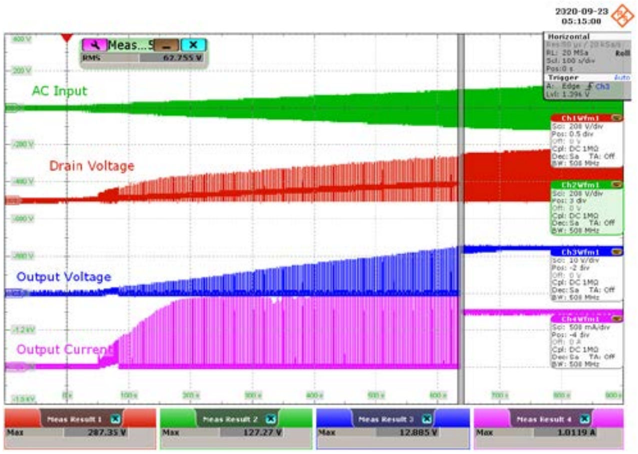

Figure 127 – Brown-in, Full Load.
CH1: V_{DS}, 200 V / div., 100 s / div.
CH2: V_{IN}, 200 V / div., 100 s / div.
CH3: V_{OUT}, 10 V / div., 100 s / div.
CH4: I_{DS}, 500 mA / div., 100 s / div.

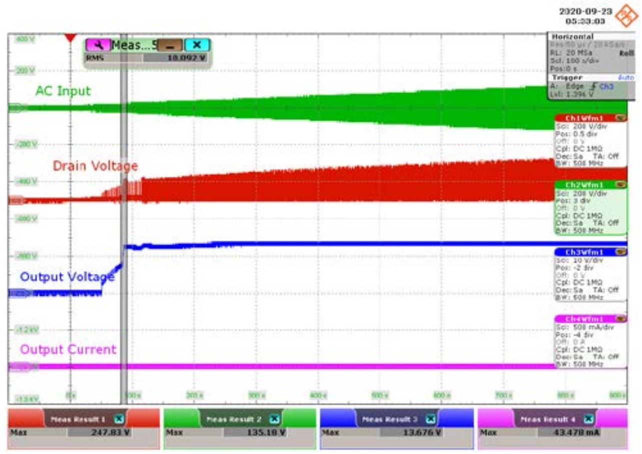

Figure 128 – Brown-in, No-Load.
CH1: V_{DS}, 200 V / div., 100 s / div.
CH2: V_{IN}, 200 V / div., 100 s / div.
CH3: V_{OUT}, 10 V / div., 100 s / div.
CH4: I_{DS}, 500 mA / div., 100 s / div.

11.6.2 Brown-out

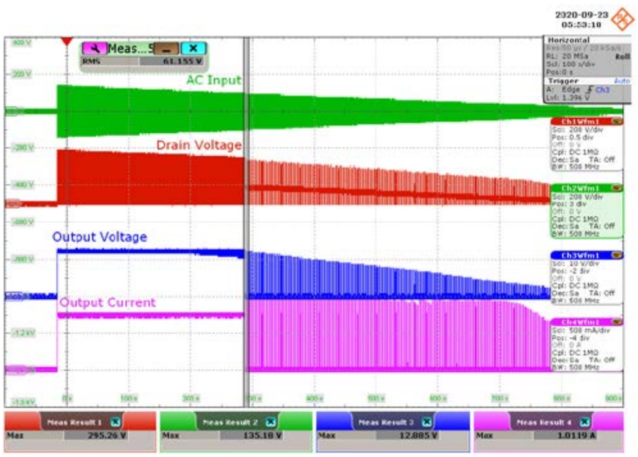

Figure 129 – Brown-out, Full Load.
CH1: V_{DS}, 200 V / div., 100 s / div.
CH2: V_{IN}, 200 V / div., 100 s / div.
CH3: V_{OUT}, 10 V / div., 100 s / div.
CH4: I_{DS}, 500 mA / div., 100 s / div.

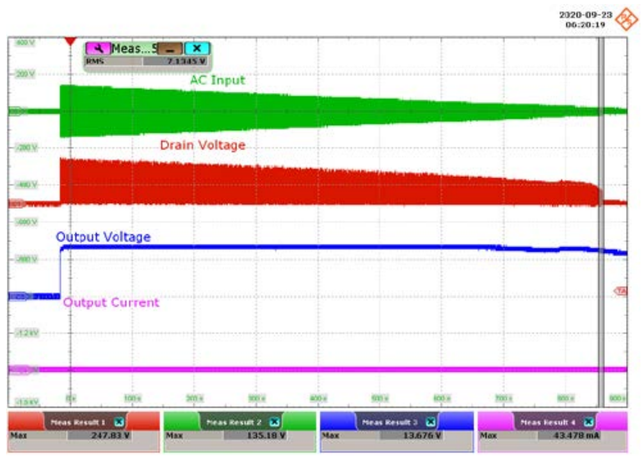

Figure 130 – Brown-out, No-Load.
CH1: V_{DS}, 200 V / div., 100 s / div.
CH2: V_{IN}, 200 V / div., 100 s / div.
CH3: V_{OUT}, 10 V / div., 100 s / div.
CH4: I_{DS}, 500 mA / div., 100 s / div.

11.7 *Fault Conditions*

11.7.1 Output Short-Circuit

Test Condition: Short-circuit applied at start-up

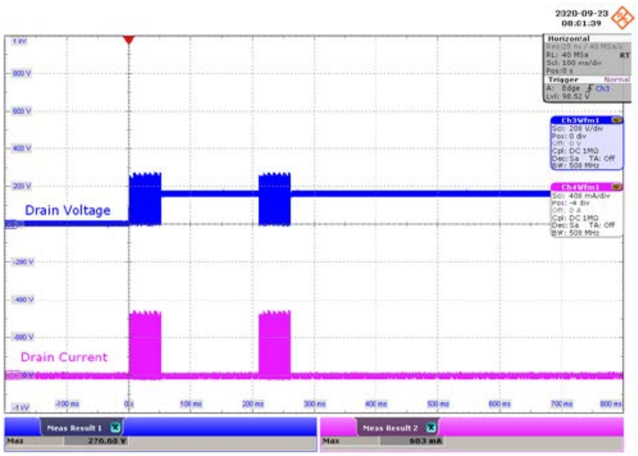

Figure 131 – 115 VAC 60 Hz.
CH3: V_{DS}, 200 V / div., 100 ms / div.
CH4: I_{DS}, 400 mA / div., 100 ms / div.
$V_{DS(MAX)}$ = 276.68 V.
$I_{DS(MAX)}$ = 0.68 A.

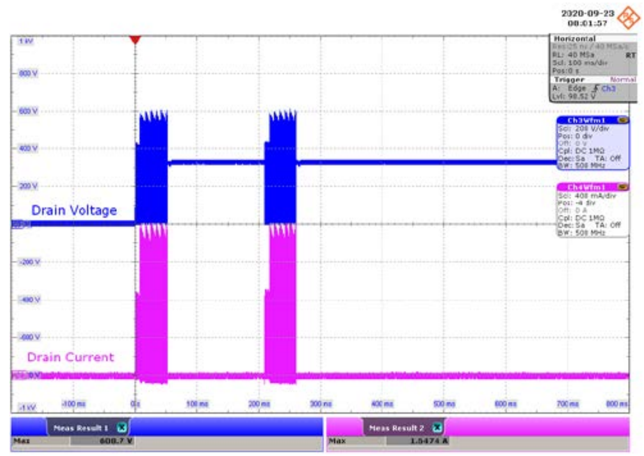

Figure 132 – 230 VAC 50 Hz.
CH3: V_{DS}, 200 V / div., 100 ms / div.
CH4: I_{DS}, 400 mA / div., 100 ms / div.
$V_{DS(MAX)}$ = 608.7 V.
$I_{DS(MAX)}$ = 1.65 A.

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11.8 *Output Voltage Ripple*

11.8.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

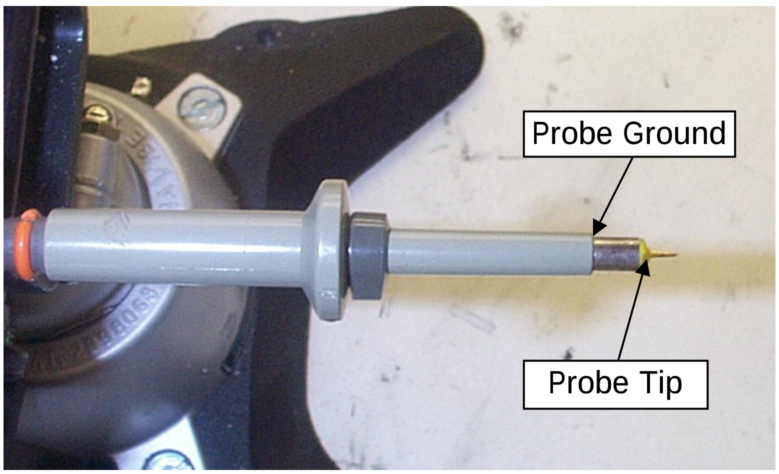

Figure 133 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

Figure 134 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.8.2 Measurement Results

11.8.2.1 100% Load Condition

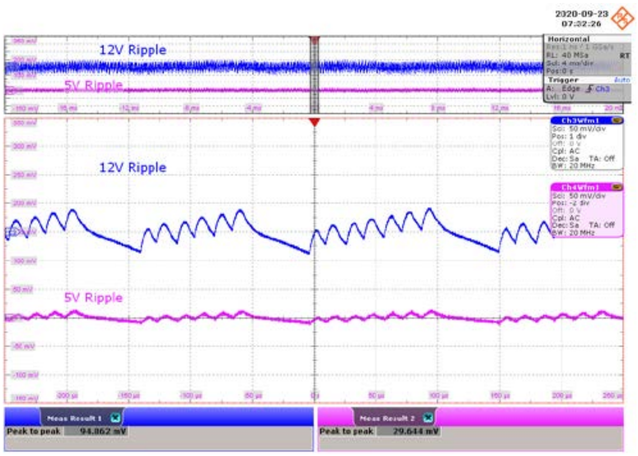

Figure 135 – 90 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 94.86 mV.
5 V Ripple = 29.64 mV.

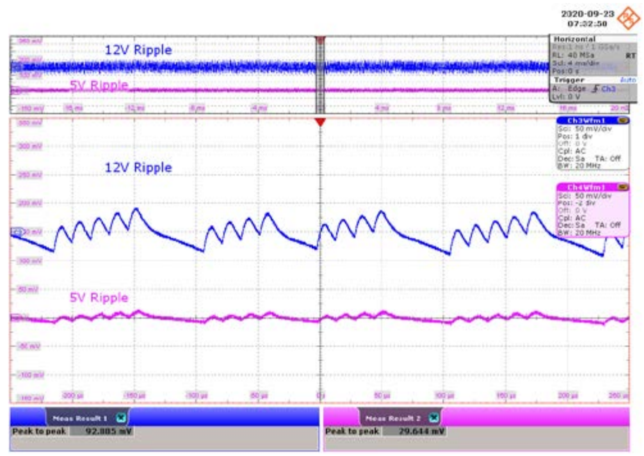

Figure 136 – 115 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 92.89 mV.
5 V Ripple = 29.64 mV.

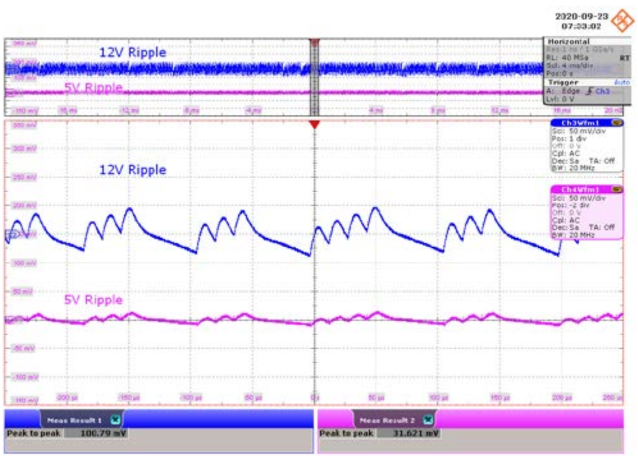

Figure 137 – 230 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 100.79 mV.
5 V Ripple = 31.62 mV.

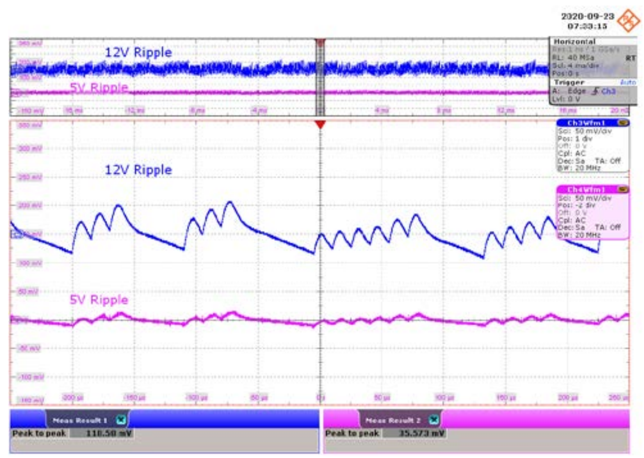

Figure 138 – 300 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 118.58 mV.
5 V Ripple = 33.57 mV.

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11.8.2.2 75% Load Condition

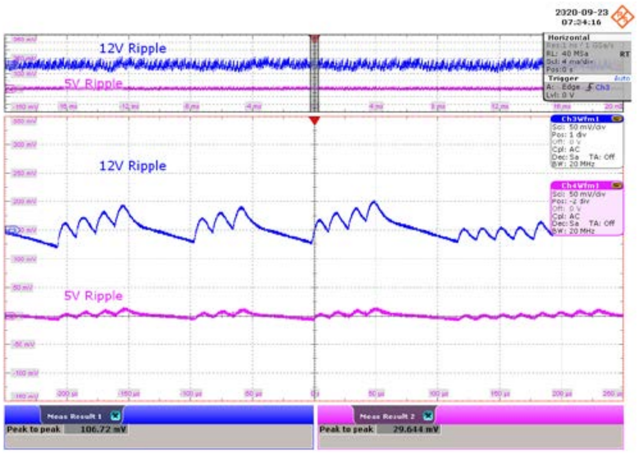

Figure 139 – 90 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 106.72 mV.
5 V Ripple = 29.64 mV.

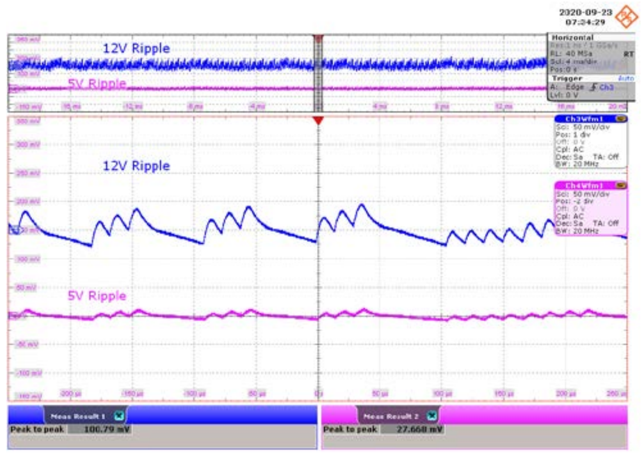

Figure 140 – 115 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 100.79 mV.
5 V Ripple = 27.67 mV.

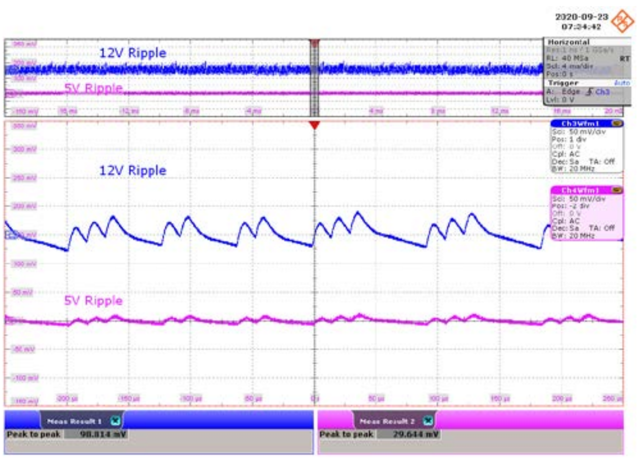

Figure 141 – 230 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 98.81 mV.
5 V Ripple = 29.64 mV.

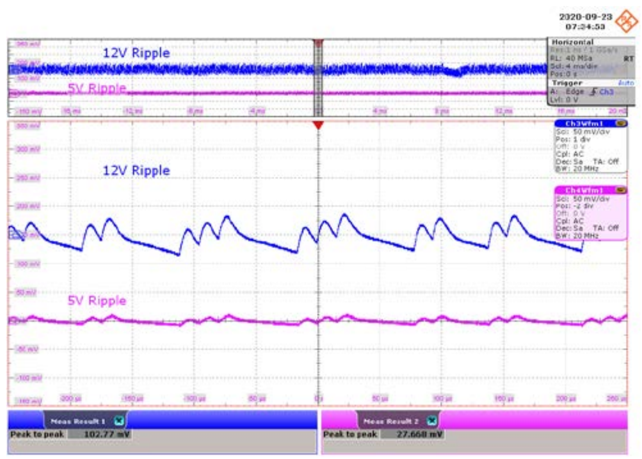

Figure 142 – 265 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 102.77 mV.
5 V Ripple = 27.67 mV.

11.8.2.3 50% Load Condition

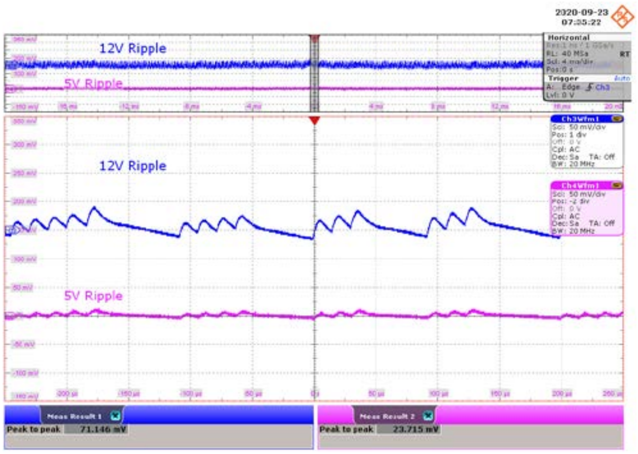

Figure 143 – 90 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 71.15 mV.
5 V Ripple = 23.71 mV.

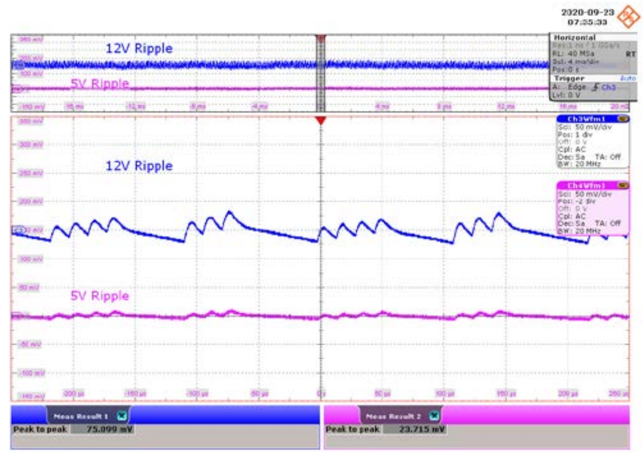

Figure 144 – 115 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 75.10 mV.
5 V Ripple = 23.71 mV.

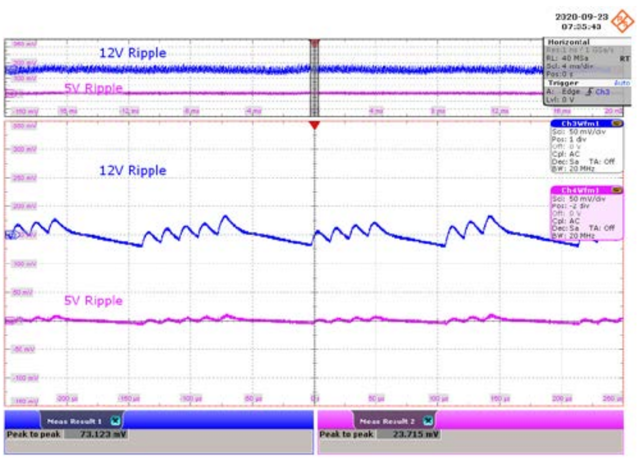

Figure 145 – 230 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 73.12 mV.
5 V Ripple = 23.71 mV.

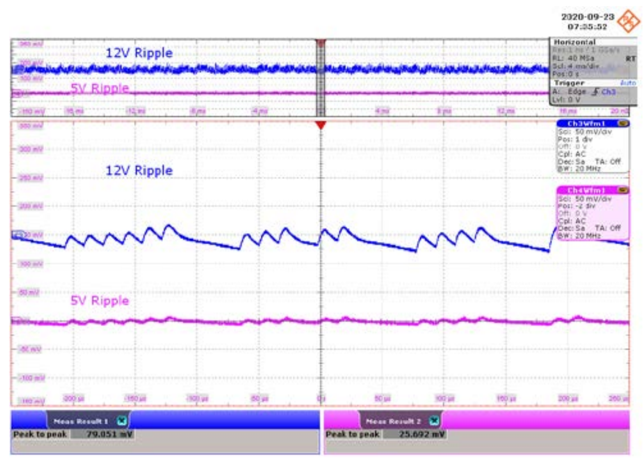

Figure 146 – 300 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 79.05 mV.
5 V Ripple = 25.69 mV.

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11.8.2.4 25% Load Condition

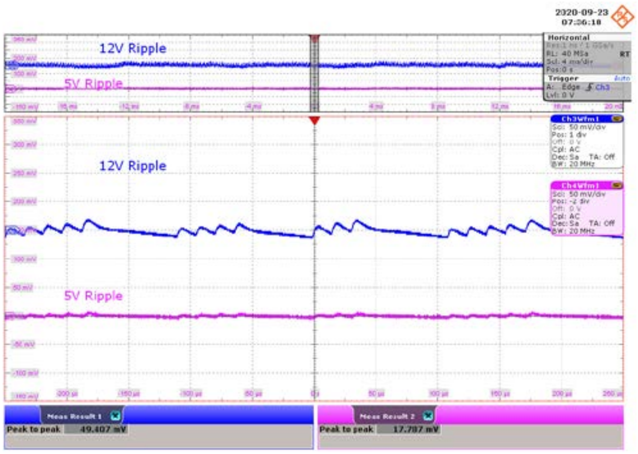

Figure 147 – 90 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 49.41 mV.
5 V Ripple = 17.79 mV.

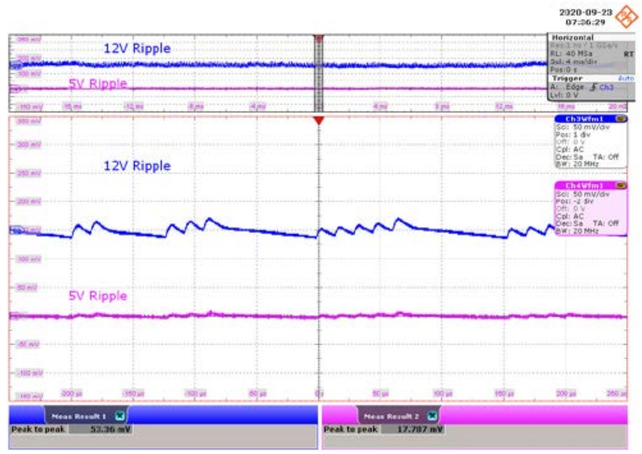

Figure 148 – 115 VAC 60 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 53.36 mV.
5 V Ripple = 17.79 mV.

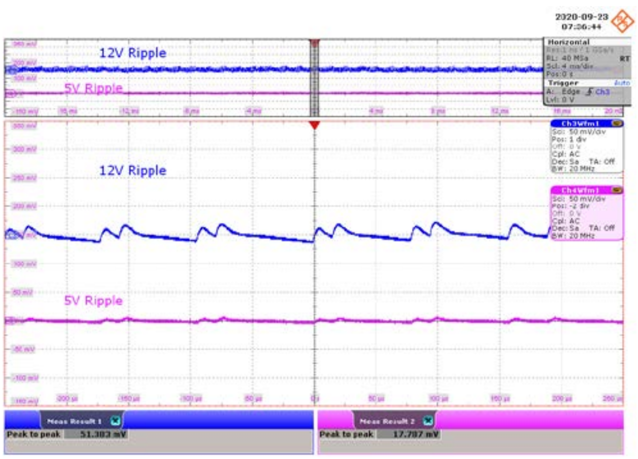

Figure 149 – 230 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 51.38 mV.
5 V Ripple = 17.79 mV.

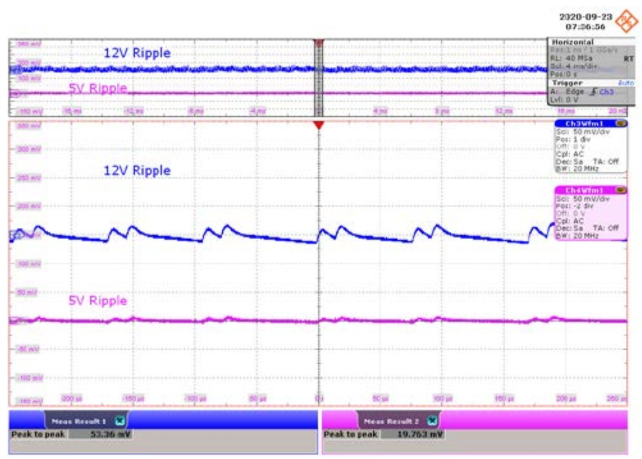

Figure 150 – 300 VAC 50 Hz.
CH3: 12 V, 50 mV / div., 4 ms / div.
CH4: 5 V, 50 mV / div., 4 ms / div.
12 V Ripple = 53.36 mV.
5 V Ripple = 19.76 mV.

11.8.3 Output Ripple Voltage Graph from 0% - 100%

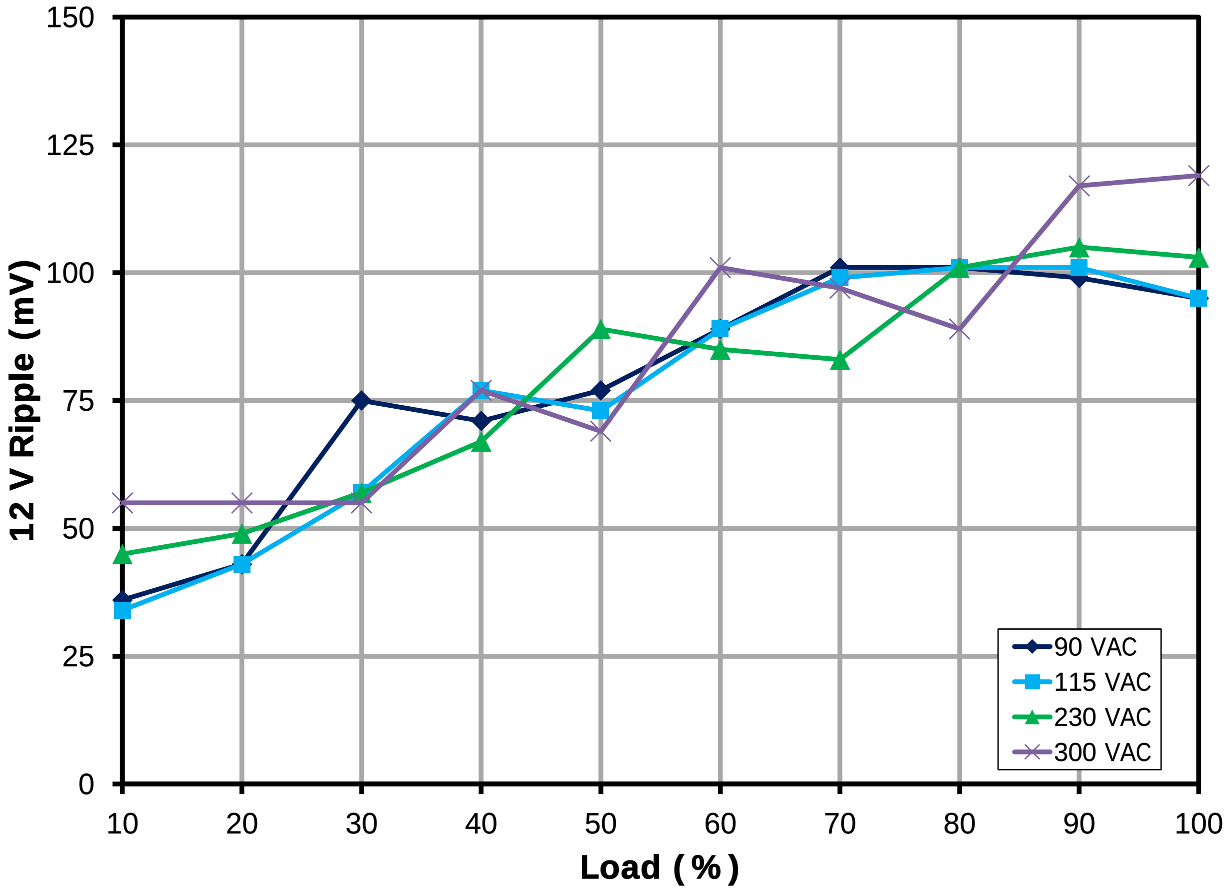

Figure 151 – 12 V Ripple Measured at the Board Output Terminals at Room Temperature.

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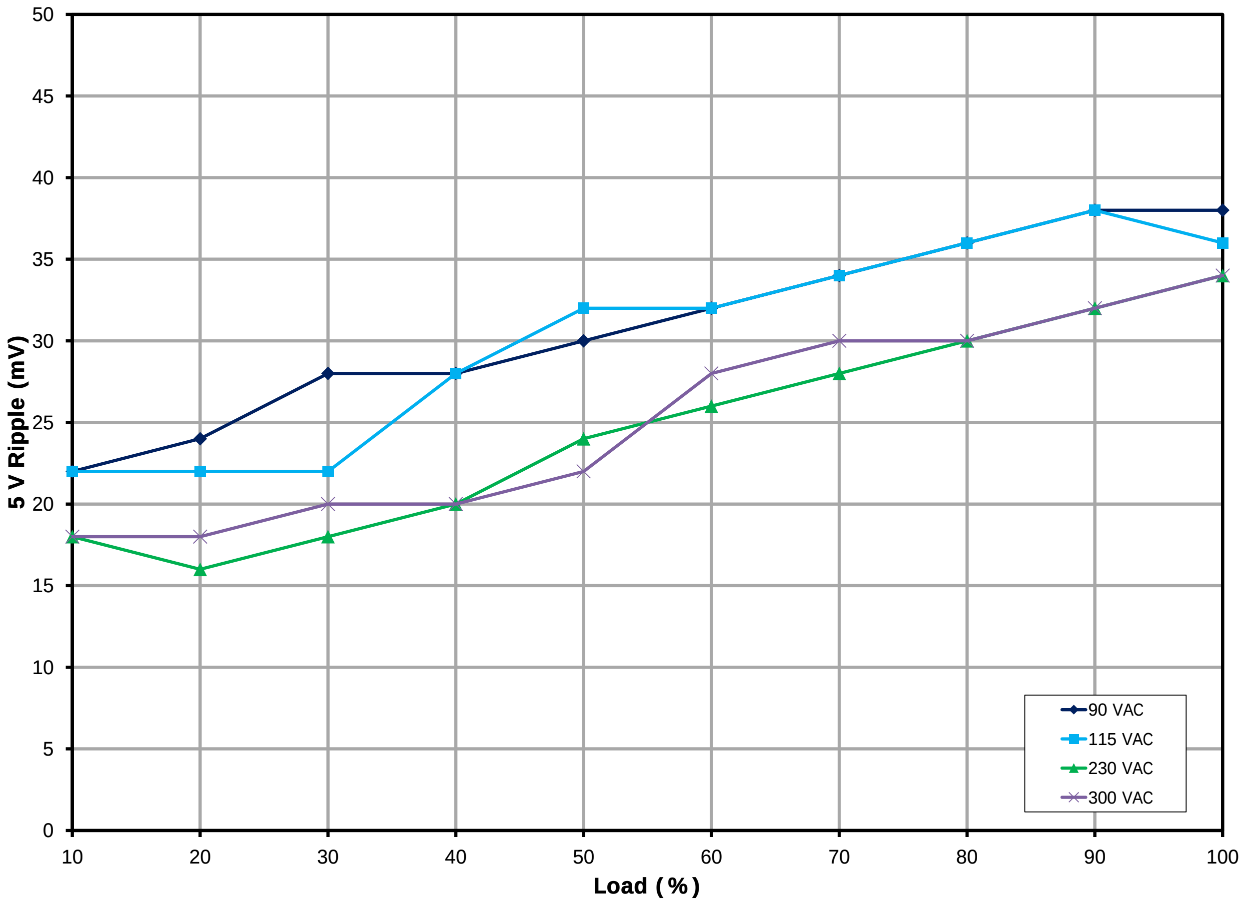

Figure 152 – 5 V Ripple Measured at the Board Output Terminals at Room Temperature.

11.9 *X Capacitor Discharge Time*

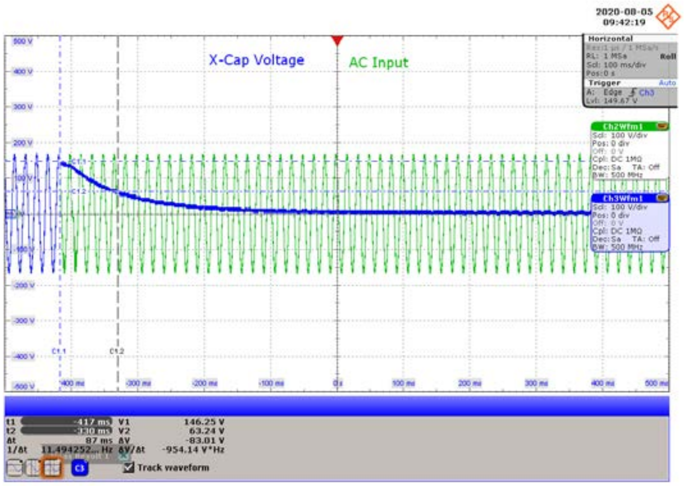

Figure 153 – 115 VAC 60 Hz, No-load.
CH2: $V_{IN,}$ 100 V / div., 100 ms / div.
CH3: $V_{XCAP,}$ 100 V / div., 100 ms / div.
X Capacitor Discharge Time = 87 ms.

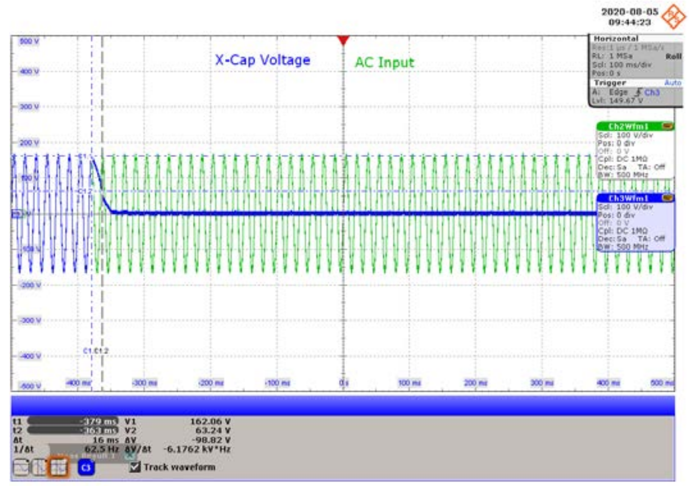

Figure 154 – 115 VAC 60 Hz, Full load.
CH2: $V_{IN,}$ 100 V / div., 100 ms / div.
CH3: $V_{XCAP,}$ 100 V / div., 100 ms / div.
X Capacitor Discharge Time = 16 ms.

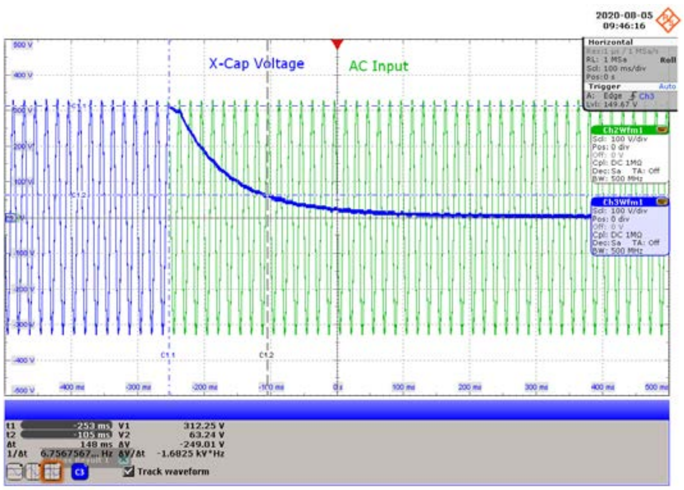

Figure 155 – 230 VAC 50 Hz, No-load.
CH2: $V_{IN,}$ 100 V / div., 100 ms / div.
CH3: $V_{XCAP,}$ 100 V / div., 100 ms / div.
X Capacitor Discharge Time = 148 ms.

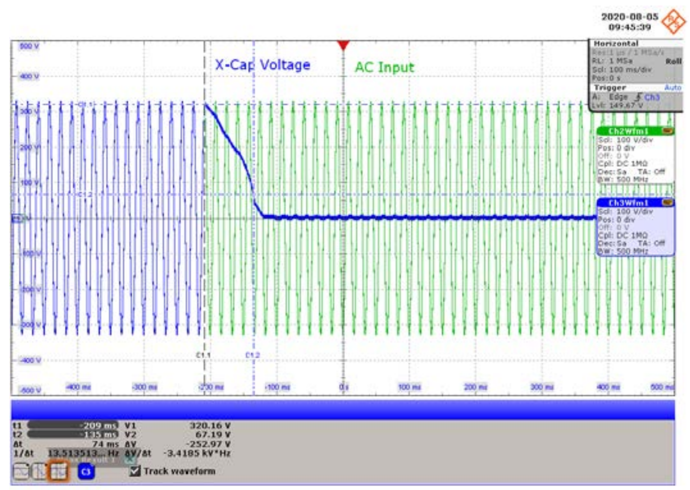

Figure 156 – 230 VAC 50 Hz, Full load.
CH2: $V_{IN,}$ 100 V / div., 100 ms / div.
CH3: $V_{XCAP,}$ 100 V / div., 100 ms / div.
Capacitor Discharge Time = 74 ms.

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12 Thermal Performance

12.1 *Test Set-Up*

Thermal evaluation was performed room temperature with the circuit board enclosed inside an acrylic box.

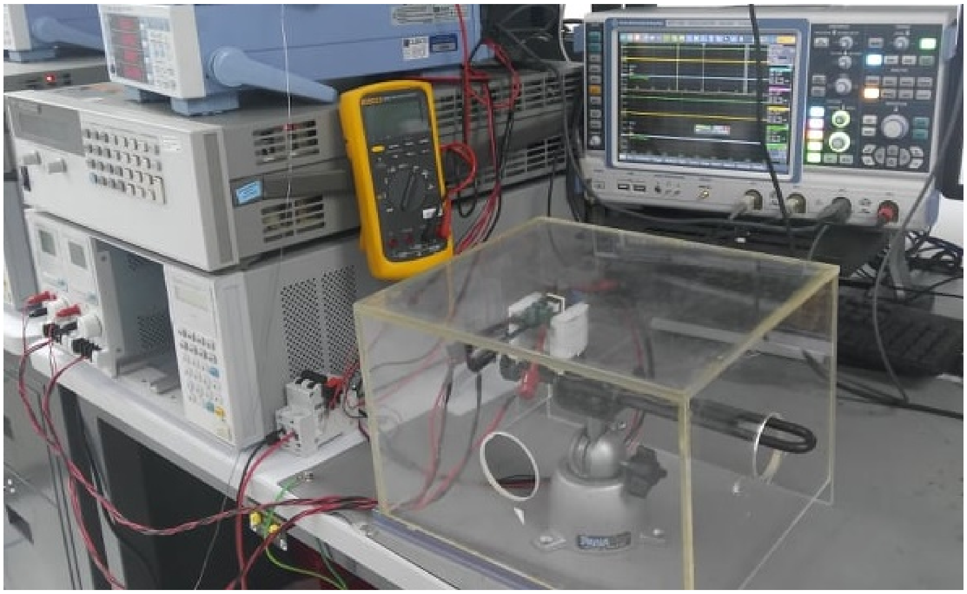

Figure 157 – Thermal Performance Set-up Using an Acrylic Box.

12.2 *Thermal Performance at Room Temperature*

12.2.1 90 VAC at room temperature

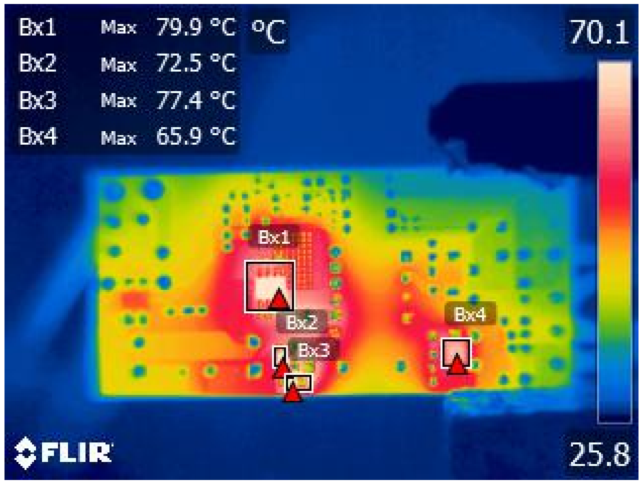

Figure 158 – Thermal Performance at 90 VAC, Bottom Side.

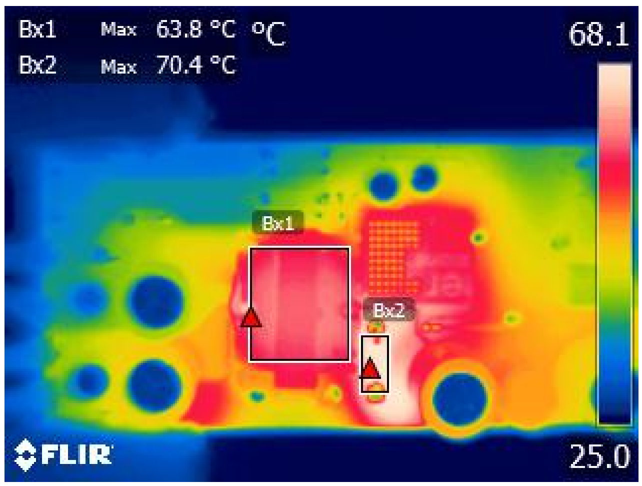

Figure 159 – Thermal Performance at 90 VAC, Top Side.

Component	Temperature (°C)
LNK3317D (U1)	79.9
Snubber Resistor (R3)	72.5
Snubber Resistor (R2)	77.4
Output Diode (D5)	65.9
Transformer (T1)	63.8
Snubber Diode (D2)	70.4
Ambient	25.0

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12.2.2 115 VAC at Room Temperature

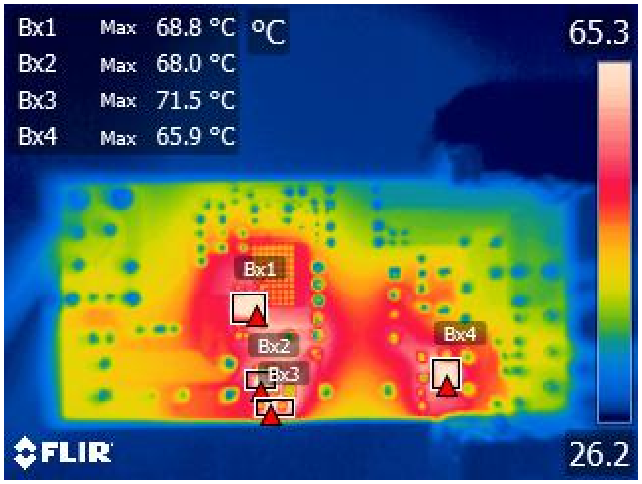

Figure 160 – Thermal Performance at 90 VAC, Bottom Side.

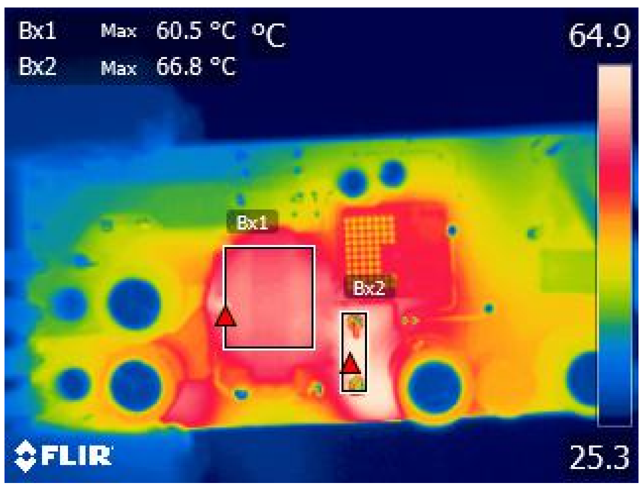

Figure 161 – Thermal Performance at 115 VAC, Top Side.

Component	Temperature (°C)
LNK3317D (U1)	68.8
Snubber Resistor (R3)	68.0
Snubber Resistor (R2)	71.5
Output Diode (D5)	65.9
Transformer (T1)	60.5
Snubber Diode (D2)	66.8
Ambient	25.0

12.2.3 230 VAC at Room Temperature

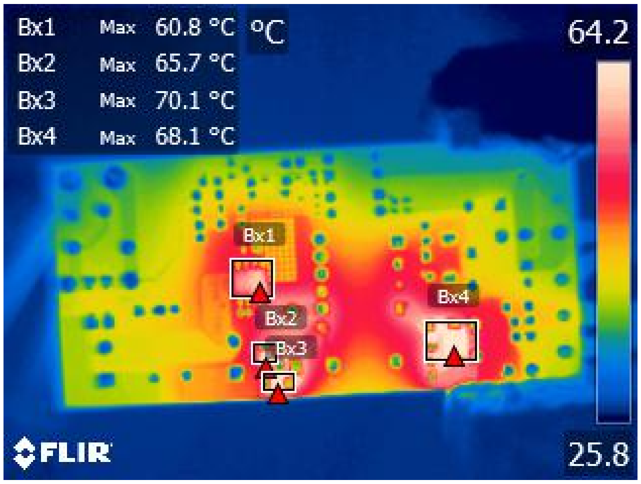

Figure 162 – Thermal Performance at 230 VAC, Bottom Side.

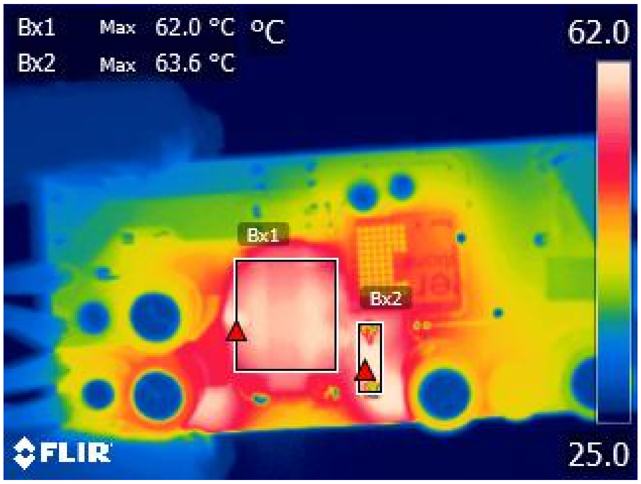

Figure 163 – Thermal Performance at 230 VAC, Top Side.

Component	Temperature (°C)
LNK3317D (U1)	60.8
Snubber Resistor (R3)	65.7
Snubber Resistor (R2)	70.1
Output Diode (D5)	68.1
Transformer (T1)	62.0
Snubber Diode (D2)	63.6
Ambient	25.0

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12.2.4 300 VAC at Room Temperature

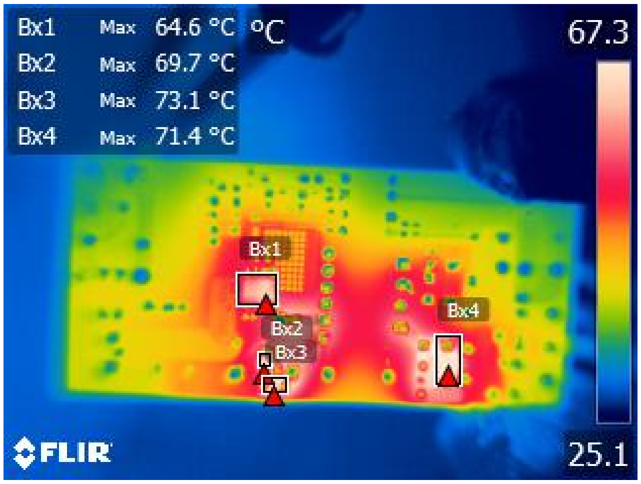

Figure 164 – Thermal Performance at 300 VAC, Bottom Side.

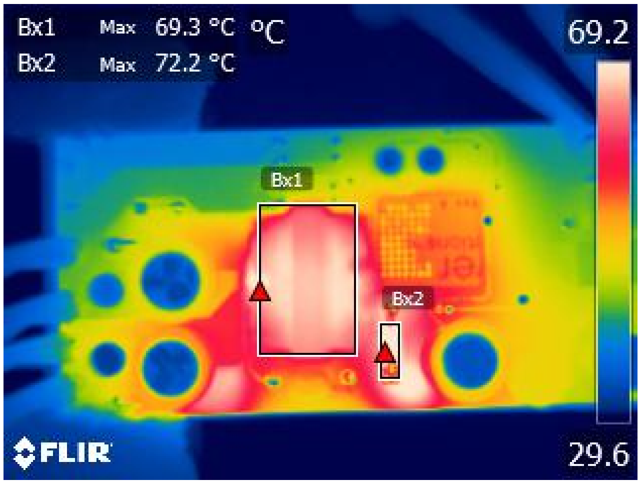

Figure 165 – Thermal Performance at 300 VAC, Top Side.

Component	Temperature (°C)
LNK3317D (U1)	64.6
Snubber Resistor (R3)	69.7
Snubber Resistor (R2)	73.1
Output Diode (D5)	71.4
Transformer (T1)	69.3
Snubber Diode (D2)	72.2
Ambient	25.0

13 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V, 1 A). Measurements were taken with an Artificial Hand connected and a floating DC output load resistor. A DC output cable was included.

13.1 *Test Set-up Equipment*

13.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.

13.2 *Test Set-up*

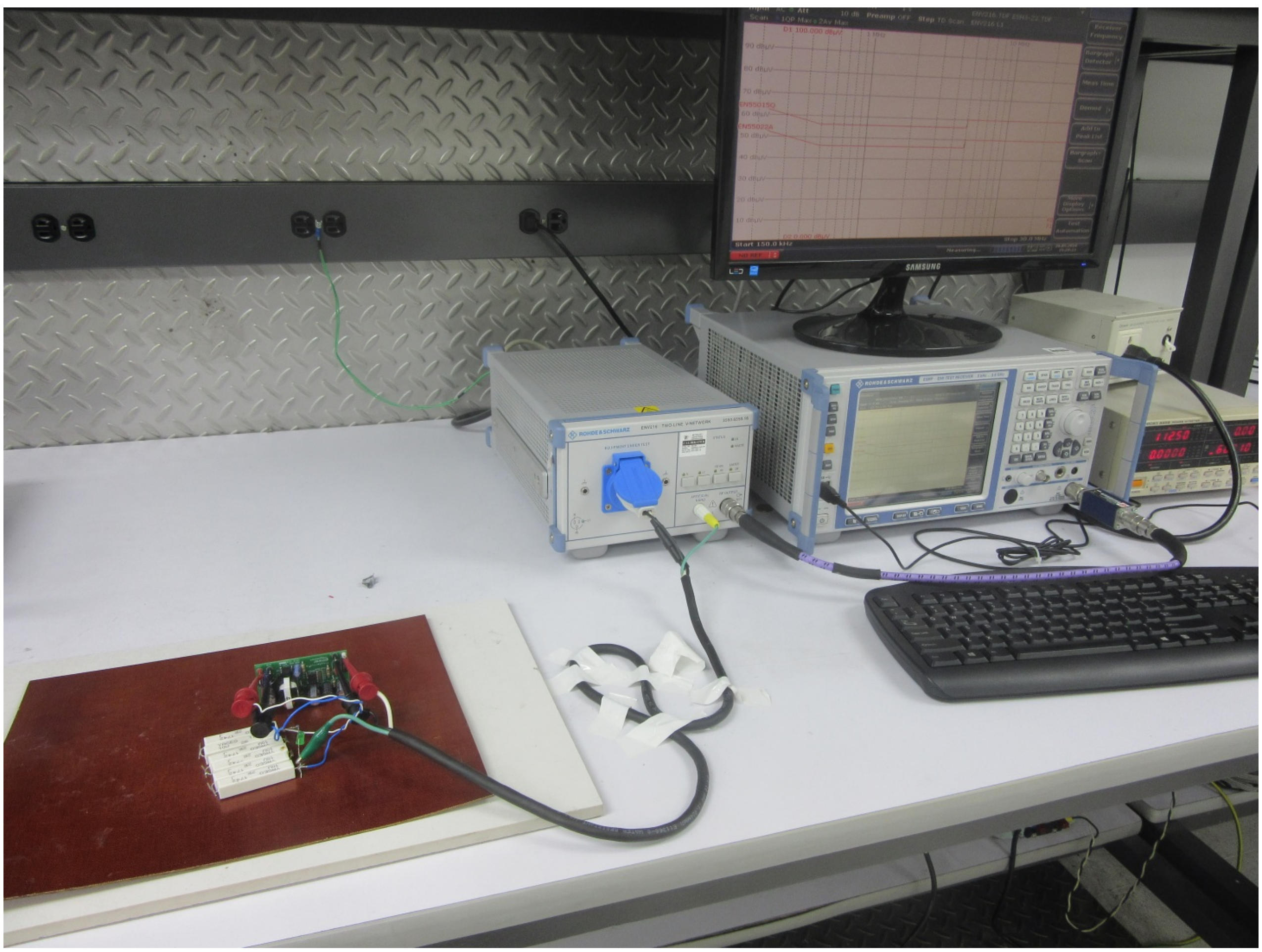

Figure 166 – EMI Test Set-up.

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13.3 *Test Results*

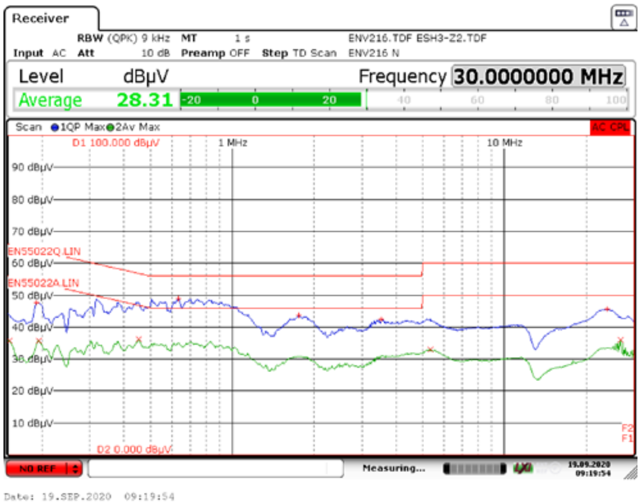

Figure 167 – 115 VAC 60 Hz, Artificial Hand.

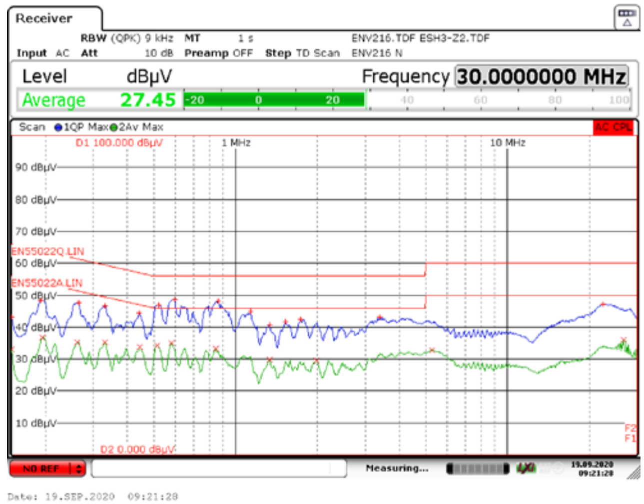

Figure 168 – 230 VAC 60 Hz, Artificial Hand.

14 Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

14.1 *Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

14.2 *Ring Wave*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
+2500	230	L to N	180	Pass
-2500	230	L to N	180	Pass
+2500	230	L to N	270	Pass
-2500	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
29-Mar-21	JPB	1.0	Initial Release.	Apps & Mktg

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