Design Example Report

Title	***180 W Power Supply with InnoSwitch™4-CZ PowiGaN™ INN4177C-H189, ClampZero™ CPZ1076M and HiperPFS™-5 PFS5177F***
Specification	90 VAC – 265 VAC Input; 20 V / 9 A Output
Application	Battery Charging
Author	Applications Engineering Department
Document Number	DER-930
Date	August 1, 2022
Revision	1.0

Summary and Features

- Integrated PFC and flyback stages for a very low component count design
- Quasi-resonant DCM control ensures low switching losses, small inductor size, and permits use of low-cost boost diode
- InnoSwitch4-CZ – active clamp flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- Zero voltage switching in both CCM and DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
    - Insensitive to transformer variation
- 95% Full-load efficiency at 230 VAC
- 93.7% Full-load efficiency at 115 VAC
- 92.8% Full-load efficiency at 90 VAC, meets DOE6 and CoC v5 2016 efficiency requirement
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <100 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B conducted EMI

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 180 W, 20 V / 9 A output power supply using HiperPFS-5 PFS5177F, InnoSwitch4-CZ INN4177C-H189, and ClampZero CPZ1076M.

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-CZ active clamp flyback controller providing exceptional performance.

This document contains the power supply specifications, schematic diagram, bill of materials (BOM), printed circuit board (PCB) layout, transformer documentation, and performance data.

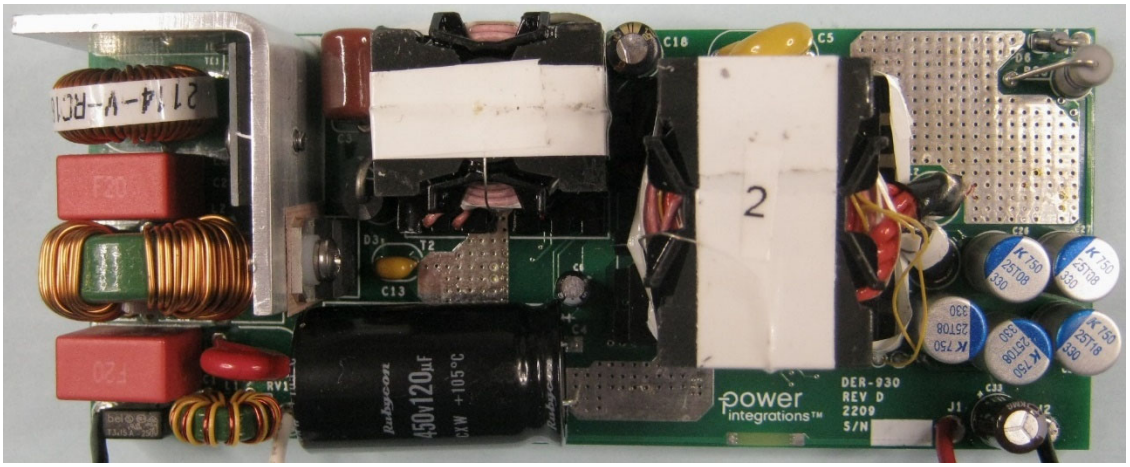


Figure 1 – Populated Circuit Board Photograph - Top.

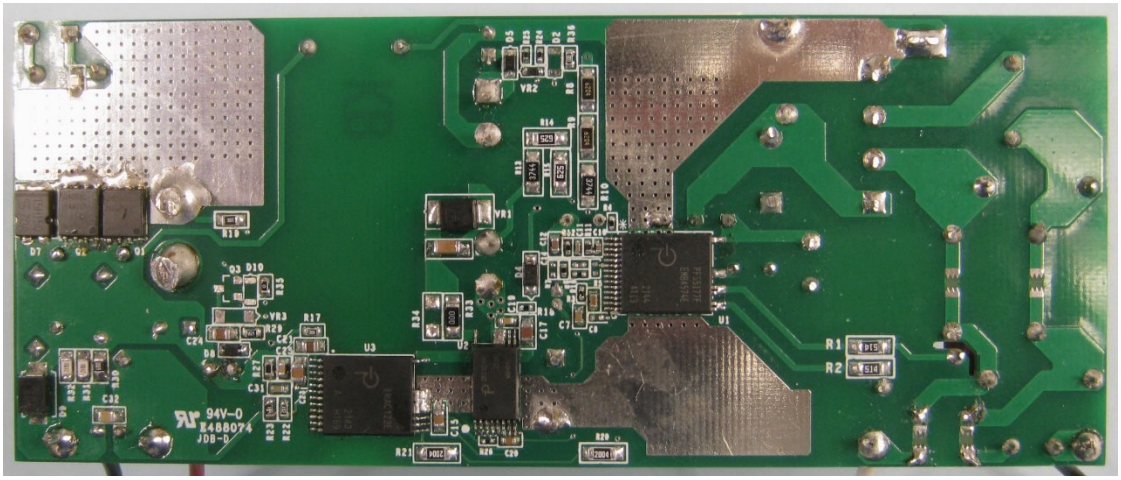


Figure 2 – Populated Circuit Board Photograph - Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-Load Input Power	P_{IN}		79		mW	Measured at 230 VAC.
Output						
Voltage	V_{OUT}		20		V	
Current	I_{OUT}		9		A	
Continuous Power	P_{OUT}	180			W	
Voltage Ripple				<250	mV	
Efficiency						
Average Efficiency			94.68		%	Measured at 230 VAC.
10% Load Efficiency			91.19		%	Measured at 230 VAC.
Conducted EMI						Meets CISPR22 / EN55022B.

Table 1 – DER-930 Power Supply Specifications.

Note: To use this design for a charger / adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

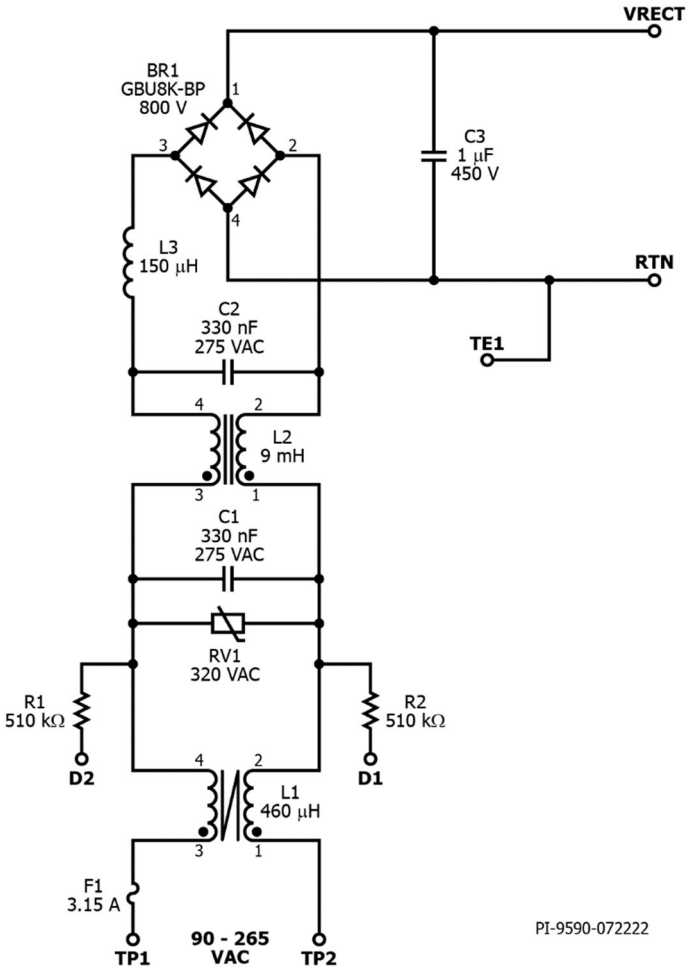


Figure 3 – DER-930 Schematic – Input Section.

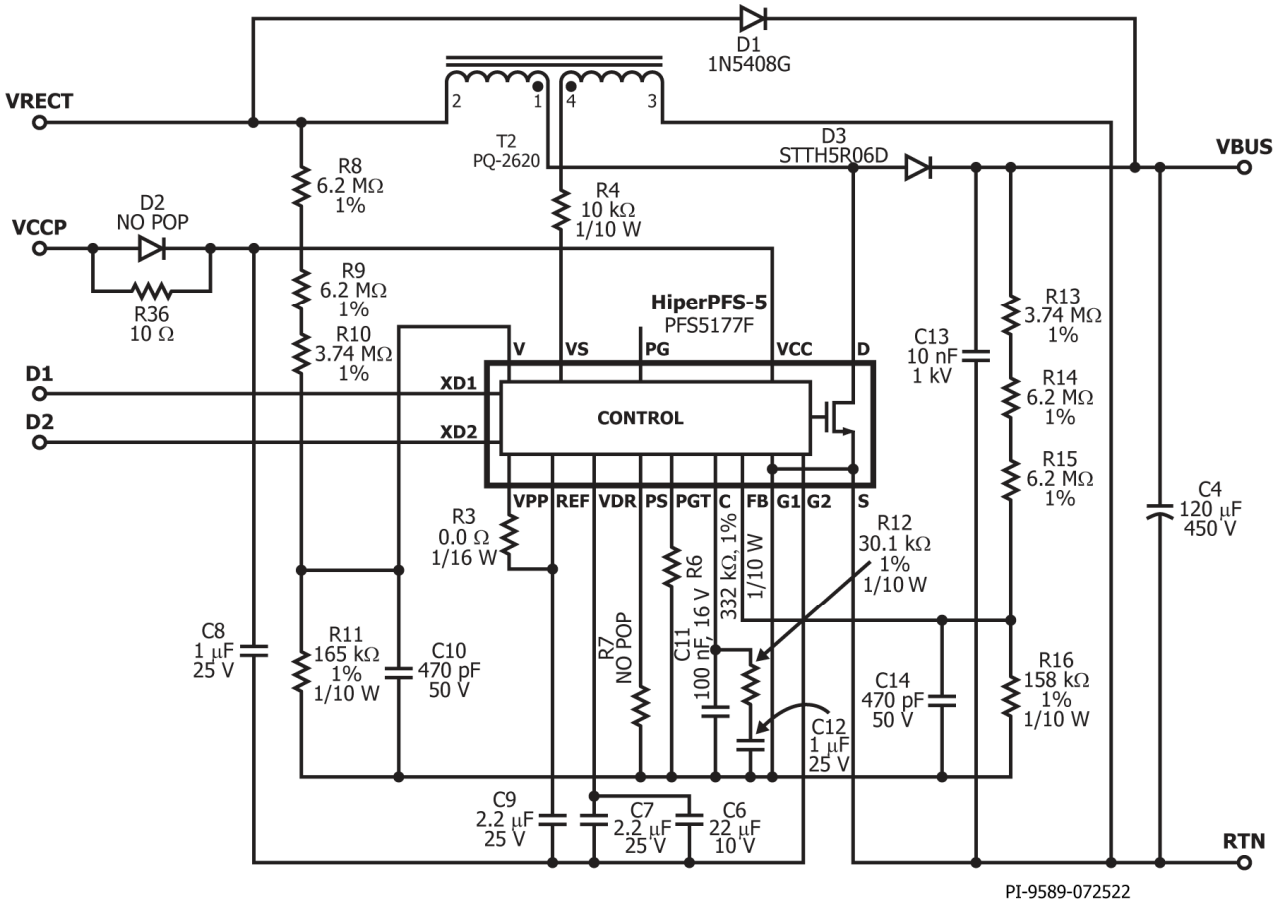


Figure 4 – DER-930 Schematic – PFC Section.

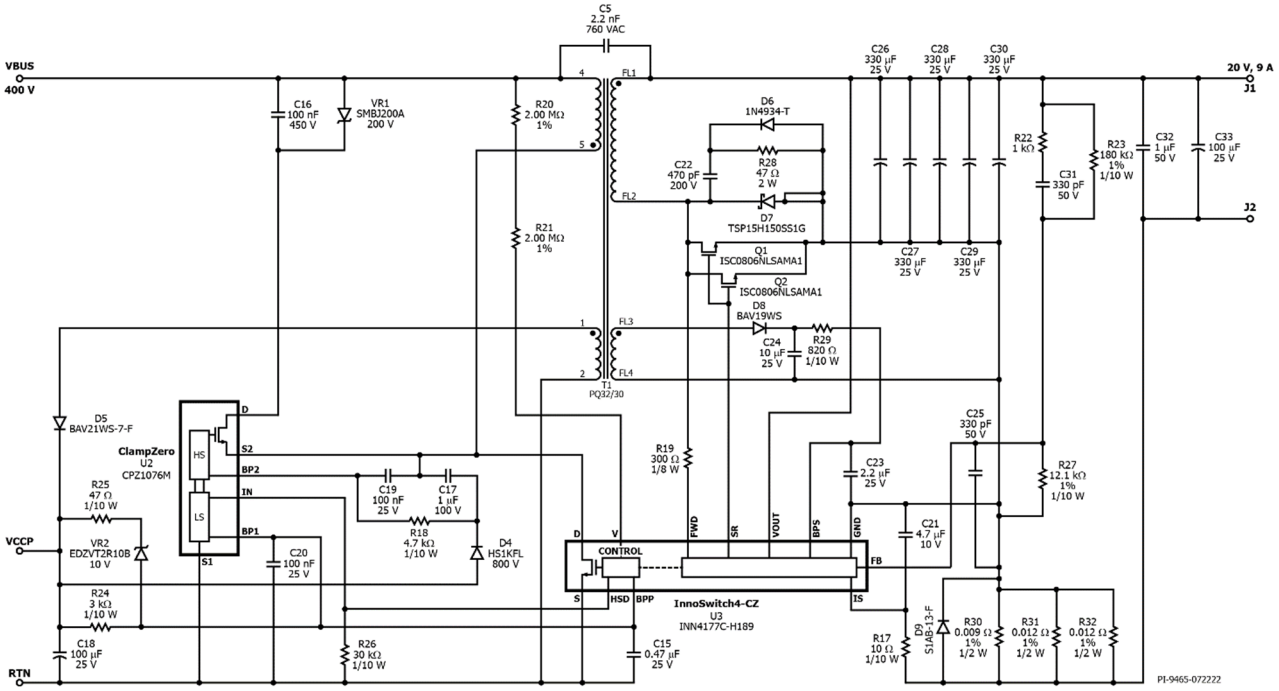


Figure 5 – DER-930 Schematic – Flyback Section.

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. Metal oxide varistor RV1 offers protection during line surge events by effectively clamping the input voltage seen by the power supply. Common mode chokes L1 and L2, differential mode choke L3, along with capacitors C1, C2, and C5 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC.

The X-capacitor discharge function is included in IC U1, and along with resistors R1 and R2, the IC discharges the stored energy in capacitors C1 and C2 when the power supply is disconnected from AC mains. The X-capacitor discharge function eliminates static losses in R1 and R2 by only connecting these components across C1 when AC input is removed.

4.2 *HiperPFS-5 PFS5177F PFC Boost Converter*

The HiperPFS-5 family incorporates a novel quasi-resonant DCM PFC controller with 750 V PowiGaN, X-capacitor discharge, and high-voltage self-start-up in a low-profile power package. HiperPFS-5 devices eliminate the need for external current sense resistors and their associated power loss and use an innovative control technique that adjusts the switching frequency over output load, input line voltage, and input line cycle. Low switching and conduction losses from PowiGAN, allow designs of up to 220 W without a heat sink.

The PFC power stage is comprised of the boost inductor T2, boost diode D3, bypass diode D1, bulk capacitor C4, and HiperPFS-5 U1. Capacitor C13 provides a short return path to the source pin of U1 for improved EMI results.

The VALLEY SENSING (VS) pin is connected to the auxiliary winding on inductor T2 through an external resistor R4. The resistor is used to limit the current through VS pin and allow for fine adjustment of timing for valley switching.

The VOLTAGE MONITOR (V) pin is tied to the rectified high-voltage DC rail through approximately 100:1 high-impedance resistor dividers R8, R9, R10 and R11. A small ceramic capacitor C10 forms an 80 μs time constant to bypass any switching noise present on the rectified DC bus.

The POWER SELECTION (PS) resistor is not used in this design since this design delivers 100% of its nominal output power.

The REF pin is connected to a bypass capacitor C9 while the VPP pin must be connected to REF pin via R3. Capacitor C11 and series R-C circuit R12/C12 are connected to COMPENSATION (C) pin for loop pole / zero compensation.

The FEEDBACK (FB) pin is connected to the main voltage regulation feedback resistor divider network of upper FB resistors R13, R14, and R15 and bottom FB resistor R16. The divider ratio was selected to ensure that nominal PFC output voltage is 394 V. A small ceramic filter capacitor C14 is added to form an 80 μs time constant with the bottom FB resistor.

The BIAS POWER (VCC) pin is used to power the IC and comes from the output of the linear regulator used to supply InnoSwitch-CZ and ClampZero as well. Capacitor C8 is the bypass capacitor of VCC and resistor R36 is added to isolate the supply.

4.3 *InnoSwitch4-CZ IC Primary*

One end of the transformer T1 primary is connected to the rectified DC bus, while the other is connected to the drain terminal of the PowiGaN switch inside the InnoSwitch4-CZ IC (U3).

Resistors R20 and R21 connected to the V pin provide input voltage sensing for the InnoSwitch4-CZ IC. The value of the bypass capacitor C15 was chosen based on the desired current limit of the InnoSwitch4-CZ IC. The BPP pin of the InnoSwitch4-CZ IC also supplies the ClampZero IC (U2).

The primary clamp capacitor C16 limits the peak drain voltage of the PowiGaN switch inside the InnoSwitch4-CZ IC. The energy stored in the leakage inductance of the transformer T1 is transferred to capacitor C16. Part of the magnetizing energy is also transferred to capacitor C5 depending on the capacitance value used. TVS diode VR1 acts as fail-safe to protect the InnoSwitch4-CZ IC from excessive drain voltage if there is any malfunction in the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ IC generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U2) turns on, to achieve soft switching of the InnoSwitch4-CZ primary switch, clamp capacitor C16 starts to charge the leakage inductance of the transformer during CCM operation and both the leakage and magnetizing inductance of the transformer during DCM operation. A small delay from the high-side switch turn off is provided to achieve zero voltage switching on the primary switch. This delay is programmable by the value of resistor R26.

Capacitor C20 is used to provide local decoupling at the BP1 pin of U2. Capacitor C19 provides the decoupling for the BP2 pin. Diode D4 and capacitor C17 forms a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R18 limits the current flowing into the BP2 pin.

The InnoSwitch4-CZ IC is self-starting, using an internal high-voltage current source to charge the primary bypass pin capacitor, C15, when AC is first applied. During normal operation, the primary-side section is powered by a bias winding on the transformer T1. Output of this bias winding is rectified using diode D5 and filtered using capacitor C18 to

provide a constant voltage source to supply the BPP pin of U3. Resistor R24 limits the current being supplied to the primary bypass pin of the InnoSwitch4-CZ IC.

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of the switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range, and at light load or no-load, most cycles are disabled, while the cycles that are enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the primary switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is achieved using Zener diode VR2 and the current limiting resistor R25. In a flyback converter, the output of the bias winding tracks the output voltage of the converter by winding turns-ratio. In case of overvoltage at the output of the converter, the bias winding voltage increases and causes VR2 to breakdown, which then causes a current to flow into the BPP pin of the InnoSwitch4-CZ IC. If the current flowing in the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-CZ IC auto-restarts to prevent any further increase in output voltage.

4.4 *InnoSwitch4-CZ IC Secondary*

The secondary-side of the InnoSwitch4-CZ IC provides the output voltage and output current sensing, and a signal to drive a SR FET providing synchronous rectification. The secondary winding of the transformer is rectified by SR FET Q1, Q2 and diode D7 and filtered by capacitors C26, C27, C28, C29 and C30. Capacitor C32 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber formed by resistor R28, capacitor C22, and diode D6. Diode D6 minimizes the dissipation in resistor R8.

The gate of Q1 is turn on by the secondary-side controller of U3, based on the winding voltage sensed via resistor R19 fed into the FWD pin of the InnoSwitch4-CZ IC. In continuous conduction of operation, the SR FET is turned off prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous conduction mode of operation, the SR FET is turned off when the voltage drop across it falls below $V_{SR(TH)}$.

The secondary-side of the U3 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve system efficiency, a bias winding circuit was used. Diode D8 rectified the output of the secondary bias winding and capacitor C24 provides filtering. Resistor R29 limits the current being supplied to the BPS pin of the InnoSwitch4-CZ IC. Capacitor C23 provides local decoupling to the BPS pin of U3.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing resistors R23 and R27. The voltage across resistor R27 is fed into the FB pin of U3 with an internal reference voltage of 1.265 V. Capacitor C25 provides noise filtering of the signal at the FB pin.

Output current is sensed by monitoring the voltage drop across resistors R30, R31 and R32 between the IS and secondary GND pins with a threshold of approximated 35 mV. Resistor R17 and C21 provides filtering for the IS pin. Once the internal current sense threshold is exceeded, the device regulates the number of switching cycles to maintain a fixed output current. Resistors R30, R31 and R32 also acts as a back-up protection in case of output short-circuit. Diode D9 is used to limit the voltage rise on IS pin in the event of output capacitor short-circuit condition.

5 PCB Layout

Layers: Two (2)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 2 oz

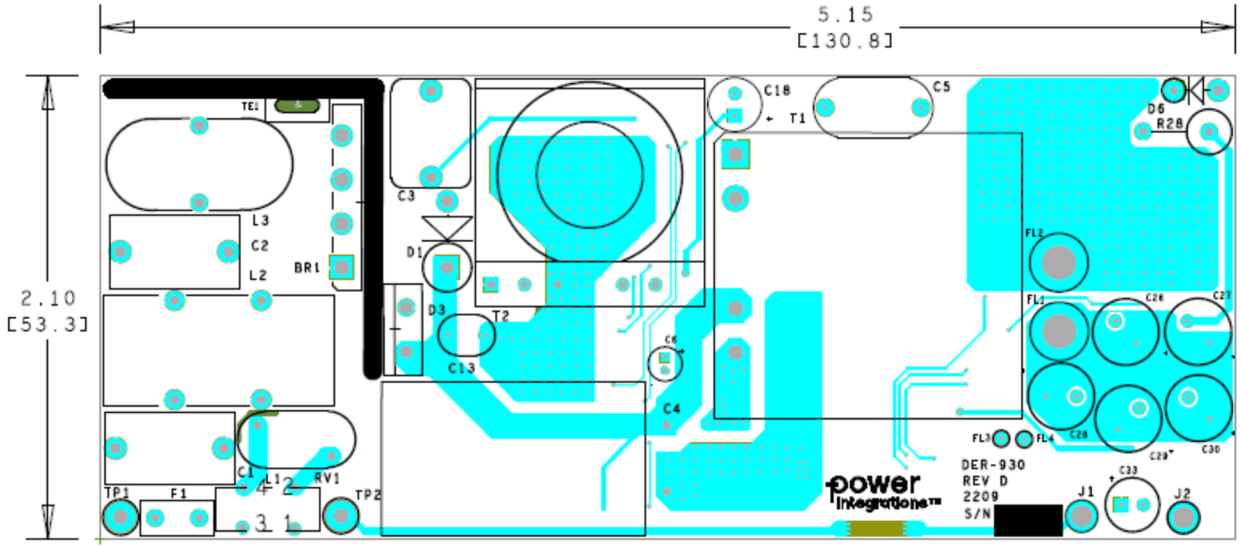


Figure 6 – DER-930 Board PCB Layout, Top.

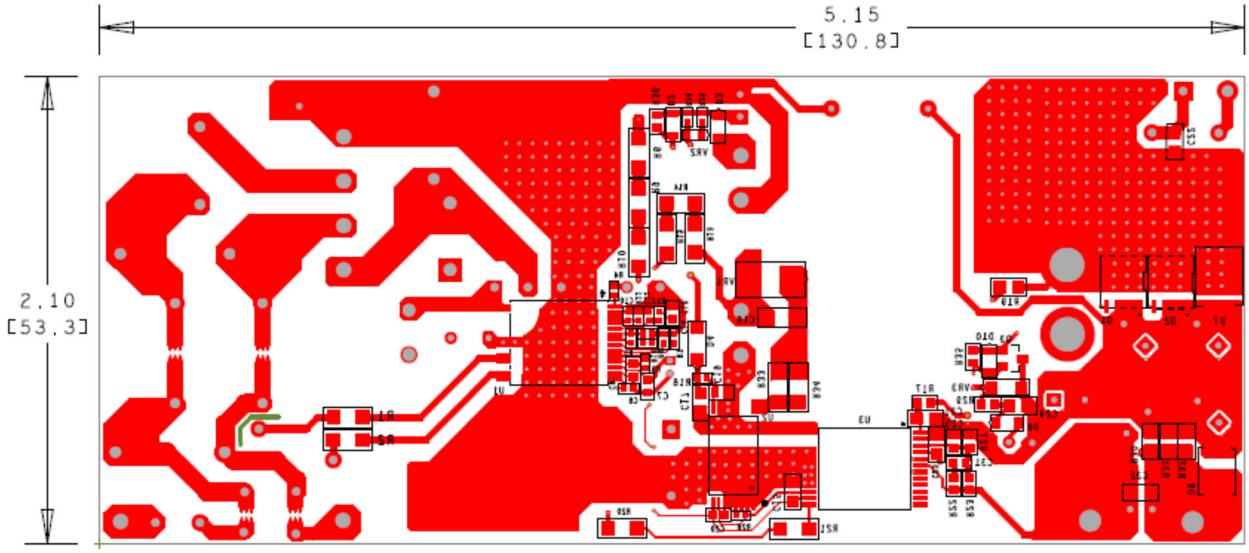


Figure 7 – DER-930 Board PCB Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	2	C1 C2	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
3	1	C3	FILM, 1.0 µF, 10%, 450 VDC, RADIAL	ECW-FD2W105Q1	Panasonic
4	1	C4	120 µF, 450 V, Aluminum Electrolytic, Radial, Can - 12000 Hrs @ 105 °C, (18 x 30)	450LXW120MEFR18X30	Rubycon
5	1	C5	CER, 2200 pF, ±20%, 760 VAC, Safety, X1, Y1, Radial, Disc	AY1222M47Y5UC63L0	Vishay
6	1	C6	22 µF, 10 V, Aluminum Electrolytic, Radial, Can 1000 Hrs @ 105 °C, (4 x7)	EEA-GA1A220	Panasonic
7	2	C7 C9	2.2 µF, ±10%, 25 V, Ceramic, X5R, 0603	GRM188R61E225KA12D	Murata
8	1	C8	1 µF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
9	2	C10 C14	470 pF, ±5%, 50 V, C0G, NP0, -55 °C ~ 125 °C, Low ESL, 0402	C0402C471J5GACTU	Kemet
10	1	C11	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
11	1	C12	1 µF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
12	1	C13	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
13	1	C15	0.47 µF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
14	1	C16	100 nF, 450 V, Ceramic, X7T, 1206	C3216X7T2W104K160AA	TDK
15	1	C17	1 µF, 100 V, Ceramic, X7S, 0805	C2012X7S2A105K125AB	TDK
16	1	C18	100 µF, 25 V, Electrolytic, (6.3 x 11)	EEU-FC1E101S	Panasonic
17	1	C19	100 nF, 0.1 µF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
18	1	C20	0.1 µF, ±10%, 25 V, Ceramic, X7R, 0603	06033C104KAT4A	AVX
19	1	C21	4.7 µF, 10 V, Ceramic, X5R, 0805	C0805C475K8PACTU	Kemet
20	1	C22	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
21	1	C23	2.2 µF, ±10%, 25V, Ceramic Capacitor X7R, 0805	CL21B225KAFNFNE	Samsung
22	1	C24	10 µF ±10% 25V Ceramic Capacitor X7S 0805	C2012X7S1E106K125AC	TDK
23	2	C25 C31	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
24	5	C26 C27 C28 C29 C30	330 µF, ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105°C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
25	1	C32	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
26	1	C33	100 µF, 25 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG250ELL101MF11D	Nippon Chemi-Con
27	1	D1	1000 V, 3 A, Rectifier, DO-201AD	1N5408G	ON Semi
28	1	D8	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
29	1	D3	600 V, 5 A, Ultrafast Recovery, 40 ns, TO-220AC	STTH5R06D	ST Semi
30	1	D4	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
31	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
32	1	D6	100 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4934-T	Diodes, Inc.
33	1	D7	Diode, Schottky, Trench, 150 V, 15 A, SMT, TO-277A (SMPC)	TSP15H150S S1G	Taiwan Semi
34	1	D9	50 V, 1 A, Standard Recovery, GPP, SMB	S1AB-13-F	Diodes, Inc.
35	1	F1	3.15 A, 250 V, Slow, RST	RST 3.15-BULK	Belfuse
36	1	L1	460 µH, Toroidal Common Mode Choke, custom, wound on 32-00315-00 core	32-00432-00	Power Integrations
37	1	L2	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
38	1	L3	150 µH, 3.4 A, Vertical Toroidal	2114-V-RC	Bourns
39	2	Q1 Q2	MOSFET, N-Channel, 100 V, 16 A (Ta), 97 A (Tc), 2.5 W (Ta), 96 W (Tc), Surface Mount, PG-TDSON-8-7,8-PowerTDFN	ISC0806NLSATMA1	Infineon
40	2	R1 R2	RES, 510 kΩ, ±5%, ¼ W, Chip Resistor 1206, Moisture Resistant, Thick Film	RC1206JR-07510KL	YAGEO
41	1	R3	RES, 0 Ω, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Vishay
42	1	R4	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic

43	1	R6	RES, 332.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3323X	Panasonic
44	4	R8 R9 R14 R15	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
45	2	R10 R13	RES, 3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
46	1	R11	RES, 165.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
47	1	R12	RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
48	1	R16	RES, 158.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1583X	Panasonic
49	2	R17 R36	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
50	1	R18	RES, 4.7 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ472X	Panasonic
51	1	R19	RES, 300 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
52	2	R20 R21	RES, 2 MΩ, 1%, 1/4 W, Moisture Resistant, Thick Film, 1206	AC1206FR-072ML	Yageo
53	1	R22	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
54	1	R23	RES, SMD, 180.0 kΩ, 1%, 1/10 W, ±100ppm/°C, -55 °C ~ 155 °C, 0603, Moisture Resistant, Thick Film	RC0603FR-07180KL	Yageo
55	1	R24	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ302X	Panasonic
56	1	R25	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
57	1	R26	RES, 30 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ303X	Panasonic
58	1	R27	RES, 12.1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1212V	Panasonic
59	1	R28	RES, 47 Ω, 5%, 2 W, Metal Oxide	RSF200JB-47R	Yageo
60	1	R29	RES, 820 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ821V	Panasonic
61	1	R30	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
62	2	R31 R32	RES, 0.012 Ω, ±1%, 0.5 W, 0805, Current Sense, Metal Foil	KRL1220E-M-R012-F-T5	Susumu
63	1	R33	RES, 0 Ω, Jumper, ½ W, Chip Resistor 1206, Pulse Withstanding Thick Film	RCS12060000Z0EA	Vishay
64	1	R35	RES,0 Ω Jumper, 1/10 W Chip Resistor 0603 Moisture Resistant Thick Film	RC0603FR-070RL	Yageo
65	1	RV1	320 Vac, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
66	1	T1	Bobbin, PQ32/30, Vertical, 12 pins	BQ32/30-1112CPFR	TDK
67	1	T2	Bobbin, PQ-2620, 6 pins, 6pri, 0sec	PQ-2620	Golden Bamboo Electronics Zhuhai
68	1	TE1	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	
69	1	U1	HiperPFS-5, 185 W, InSOP-T28F	PFS5177F	Power Integrations
70	1	U2	Clampzero, MinSOP-16	CPZ1076M	Power Integrations
71	1	U3	InnoSwitch4-CZ, 385 VDC, 200 W, insop-24D	INN4177C-H189	Power Integrations
72	1	VR1	200 V, 224 V breakdown, 1.9 A peak Pulse, 600 W peak pulse, DO214AA (SMB)(SMBJ)	SMBJ200A	Littelfuse
73	1	VR2	10 V, 5%, 150 mW, SSMINI-2,SC-79, SOD-523,EMD2	EDZVT2R10B	Rohm Semi

7 Common Mode Choke Specifications (L1)

7.1 *Electrical Diagram*

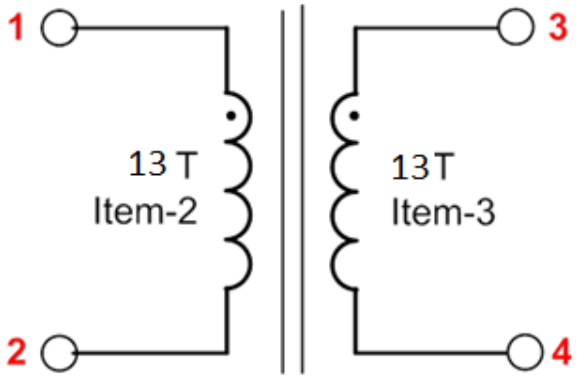


Figure 8 – Choke Electrical Diagram.

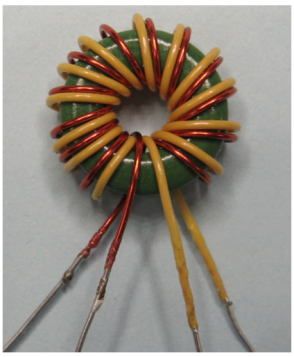
7.2 *Electrical Specifications*

Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	460 µH ±25%

7.3 *Material List*

Item	Description
[1]	Toroidal Core: GL50 T 12X6X4-C, PI#: 32-00315-00.
[2]	Triple Insulated Wire: #25 AWG, Triple Coated.
[3]	Magnet Wire: #25 AWG, Double Coated.

7.4 *Assembled Picture*



8 PFC Inductor Specification (T2)

8.1 *Electrical Diagram*

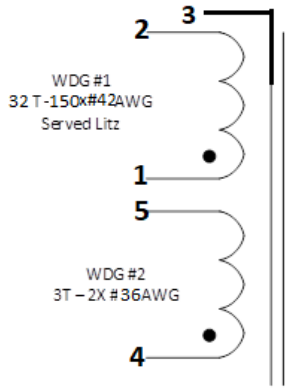


Figure 9 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	168 µH +5%
Resonant Frequency	Pins. N/A	kHz (Min.)

8.3 *Material List*

Item	Description
[1]	Core: TDK PC95PQ26/20Z-12. PI P/N 99-00033-00
[2]	Bobbin: PQ26/20, Vertical, 6 pins. PI P/N 25-01137-00
[3]	Litz Wire: 150x #42 AWG Single Coated Solderable, Served.
[4]	2x #36 AWG.
[5]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9 mm Wide.
[6]	Bus Wire, #24 AWG (connect to pin 3).
[7]	Varnish: Dolph BC-359, or Equivalent.
[8]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 36 mm Wide.
[9]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9.3 mm Wide.

8.4 *Inductor Build Diagram*

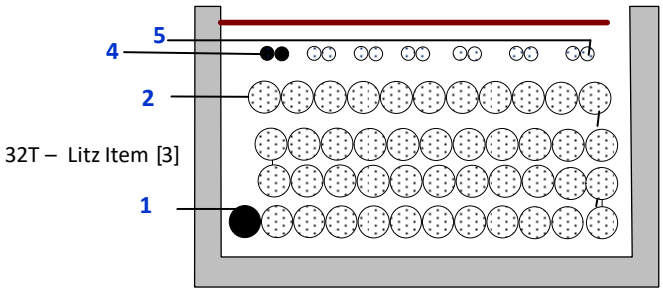
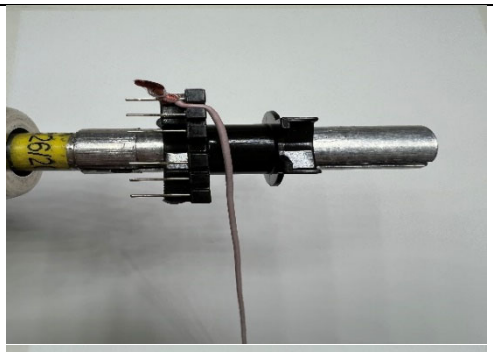
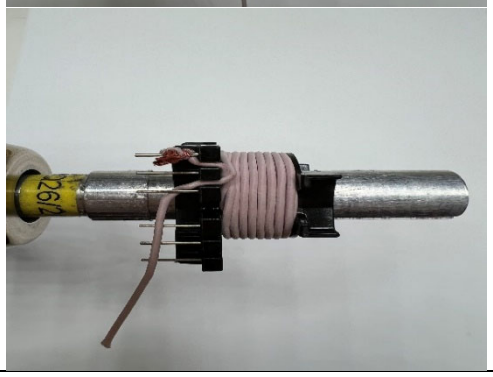
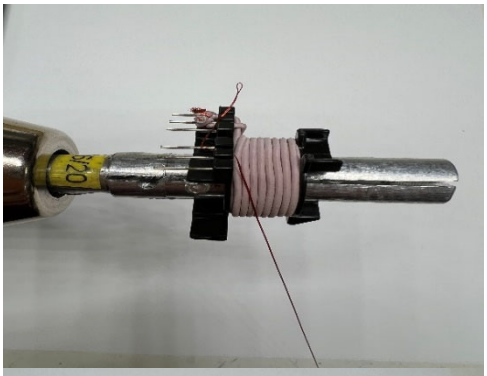
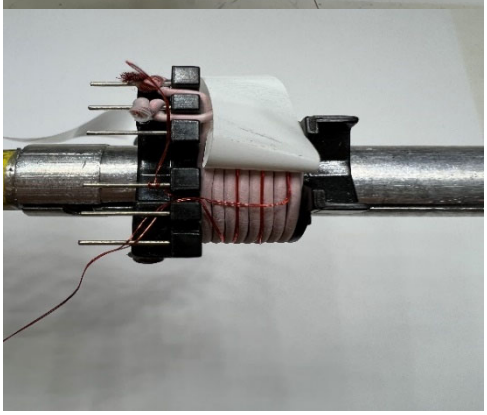
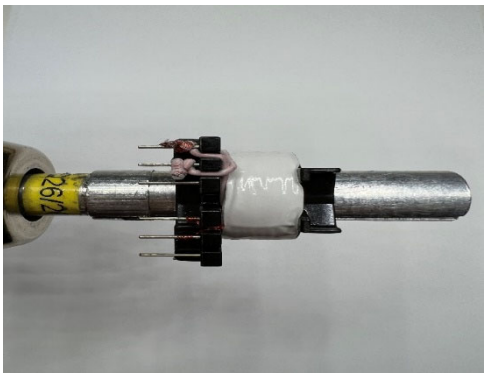
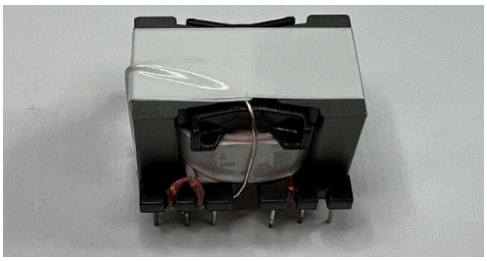
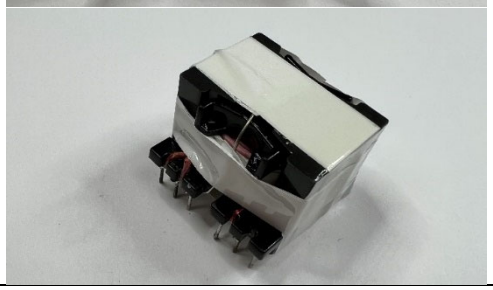


Figure 10 – Inductor Build Diagram.

8.5 *Winding Illustrations*

WD#1 Primary	 	Start at pin 1, wind 32 turn of wire Item [3] in 4 layers, from left to right, then terminate at pin 2.

WD#2	 	Start at pin 4, wind 2 wires of Item [4] for 3 turns from left to right, then bring wires back across bobbin and terminate at pin 5.
Insulation		1 layer of tape Item [5]
Finish		Gap cores to get 168 μH, solder but wire Item [6] to pin 3 which leans along with core halves. Secure with 2 layers of tape.

		Varnish with Item [7].
Finish	 	Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer and tape around 1 turn of tape Item [9]. See picture beside.

9 Transformer Specification (T1)

9.1 *Electrical Diagram*

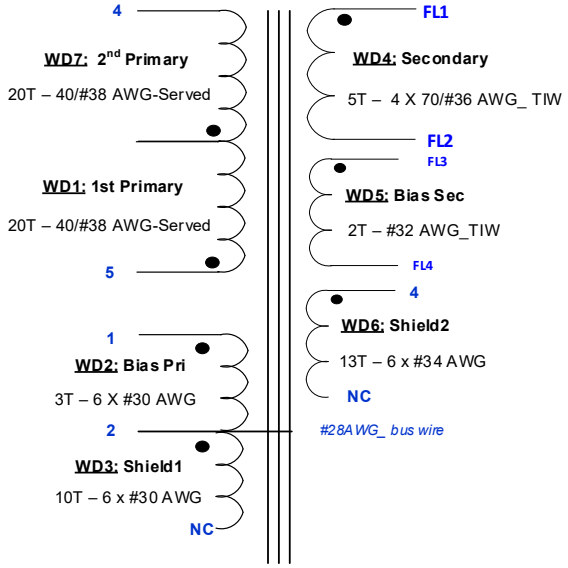


Figure 11 – Transformer Electrical Diagram.

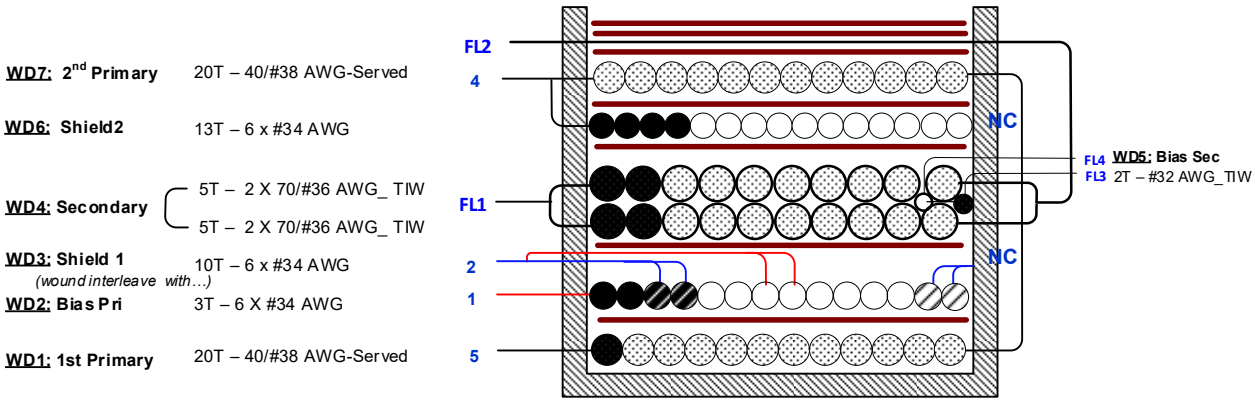
9.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 5 and 4, with all other windings open.	430 µH ±5%
Resonant Frequency	Between pin 5 and 4, other windings open.	800 kHz (Min.)
Primary Leakage Inductance	Between pin 5 and 4, with pins: FL1 - FL2 shorted.	5.5 µH (Max.)

9.3 *Material List*

Item	Description
[1]	Core: P32/30-PC95; or Equivalent.
[2]	Bobbin: PQ32/30- TDK or Shulin; PI#: 25-00918-00.
[3]	Magnet Wire: 40/#38 AWG, Served Litz.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: 70/#36 AWG, Served Litz_TIW.
[6]	Magnet Wire: #32 AWG_TIW.
[7]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper, 40.0 mm Length.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 18.6 mm Width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.0 mm Width.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 36 mm x 52 mm.
[11]	Varnish: Dolph BC-359.

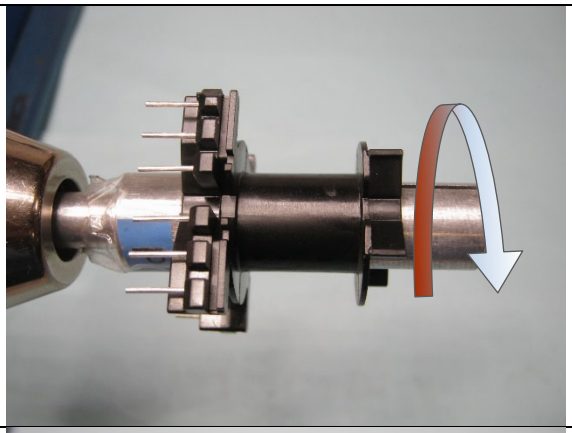
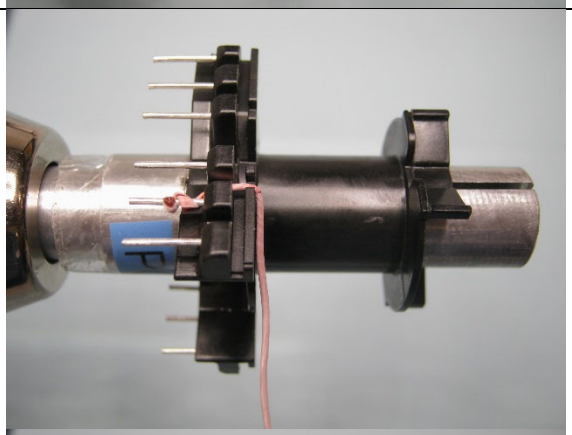
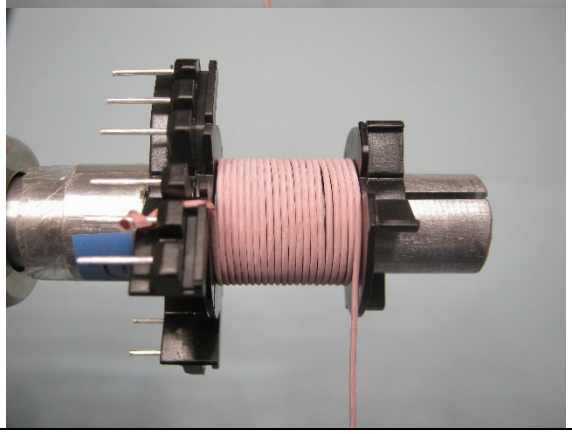
9.4 *Transformer Build Diagram*

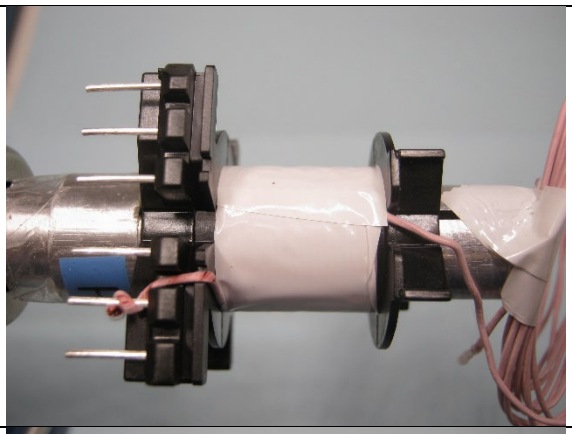
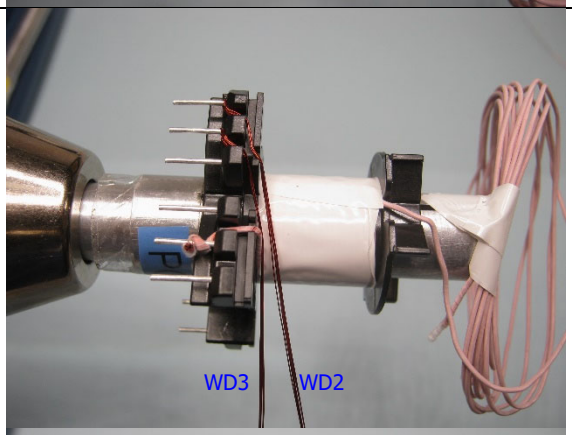
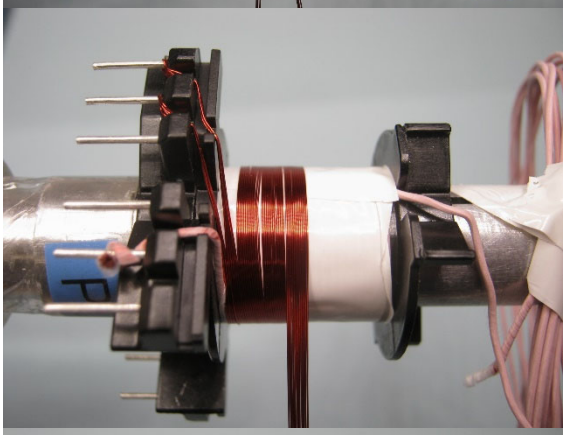
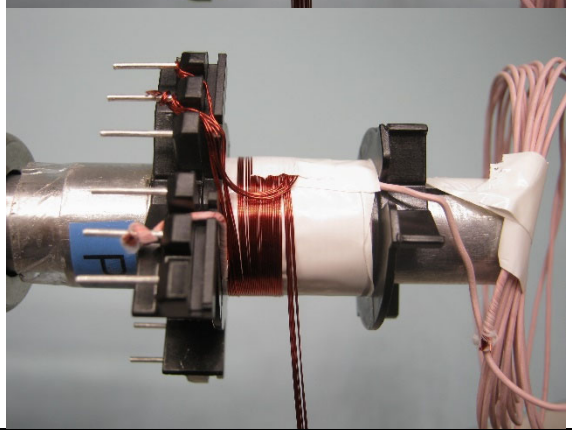


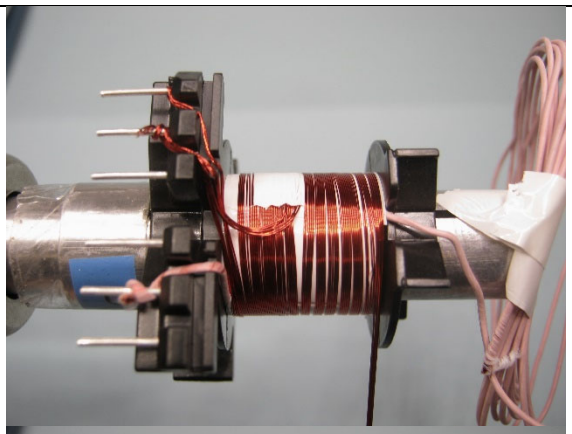
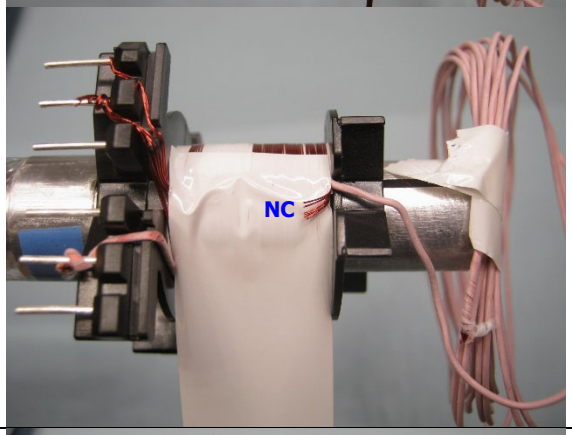
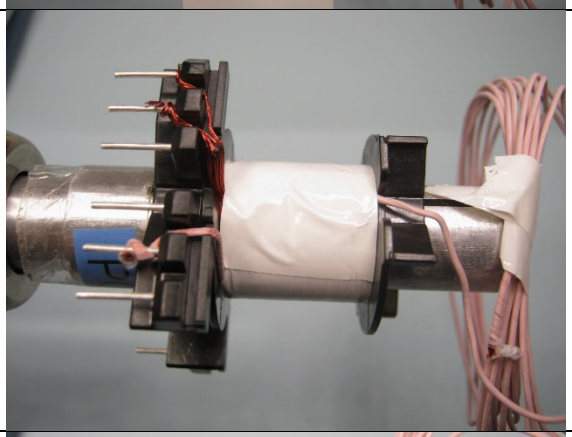
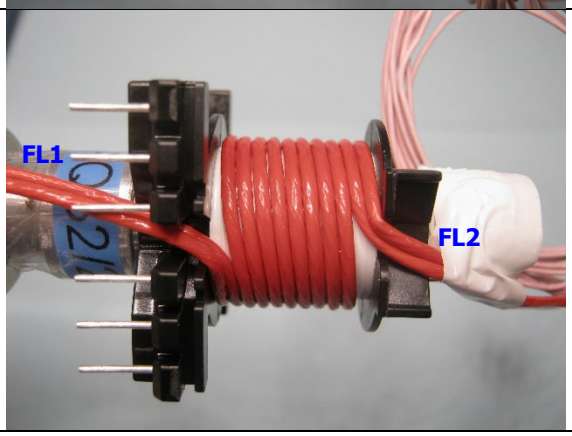
9.5 *Transformer Winding Instruction*

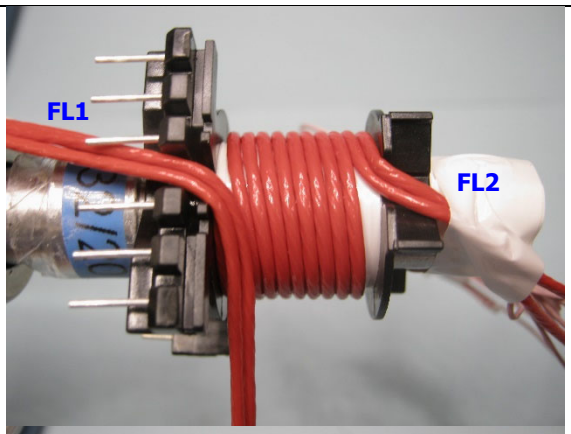
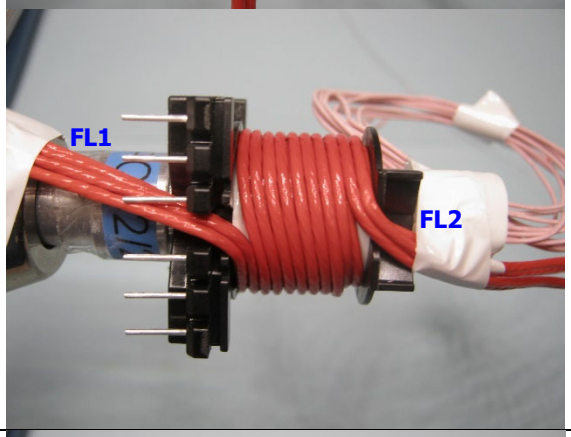
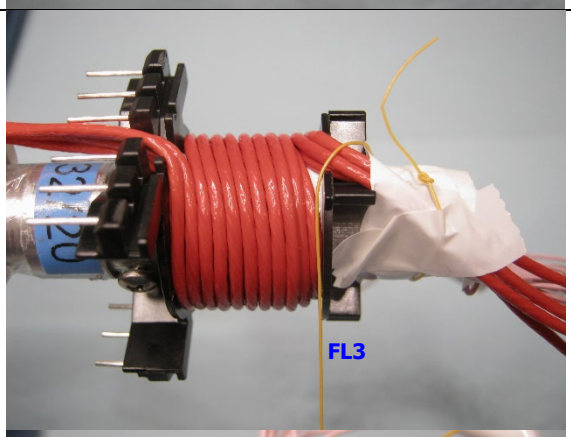
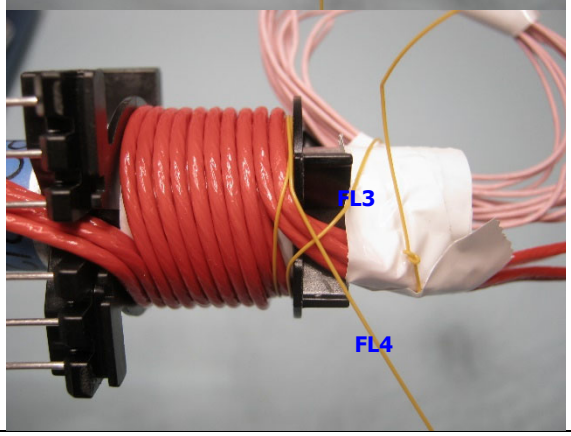
Winding Preparation	Place the bobbin Item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 1st Primary	Start at pin 5, wind 20 turns of wire Item [3] in 1 layer, from left to right, at the last turn exit the wire out of the bobbin leave enough length of this wire for WD7:2nd Primary.
Insulation	1 layer of tape Item [8].
WD2 & WD3 Bias & Shield 1	Use 6 wires Item [4], starting at pin 1 for WD2, also use 6 wires Item [4], starting at pin 2 for WD3. Wind all these wires in parallel, at 3rd turn, place 1 small piece of tape to hold wires, bring 6 wires for WD2 to the left to terminate at pin 2. Continue to wind 6 wires for WD3 to 10th turn then cut short wires as No-Connect (NC).
Insulation	1 layer of tape Item [8].
WD4 Secondary	Start at the slot on the left on secondary side of the bobbin, use 2 wires Item [5], leave ~25mm floating, and mark as FL1, wind 5 bi-filar turns in 1 layer. At the last turn, exit the wire at the slot on the right also leave ~ 45mm floating and mark as FL2 for 1st halves of Secondary. Repeat another winding as above for 2nd halves of Secondary which is parallel with 1st halves Secondary.
WD5 Secondary Bias	Use wire Item [7], start from the right and on the primary side of bobbin, leaving ~ 50mm and mark as FL3. Wind 2 turns and exit the wire also leaving 50mm and mark as FL4.
Insulation	1 layer of tape Item [8].
WD6 Shield2	Start at pin 4, use 6 wires Item [4], wind 13 turns from left to right. At the last turn, cut short the wires as No-Connect.
Insulation	1 layer of tape Item [8].
WD7 2nd Primary	Use wire floating from WD1, wind 20 turns from right to left, and terminate at pin 4.
Insulation	1 layer of tape Item [8] and bring the secondary wires FL2 to the left in between layers of tape.
Finish	Cut short secondary wires ~25 mm and tin individually for all ends ~12 mm (see picture below) Gap cores to 430 µH, solder bus wire Item [7] to pin 2 which leans along with core halves, and secure with tape. Places 2 layers of tape Item [10] at the bottom of transformer, then wrap up to cover secondary side of transformer, and wrap around the body of transformer 1 layer of tape Item [9], *(see illustration below).* Varnish Item [11].

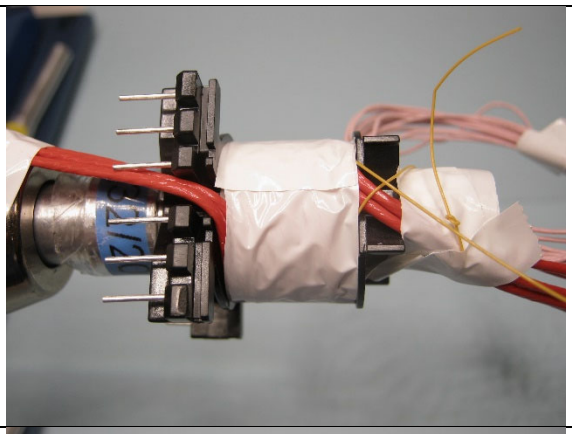
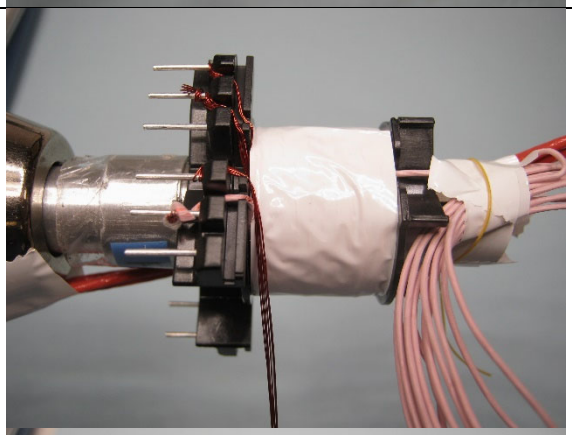
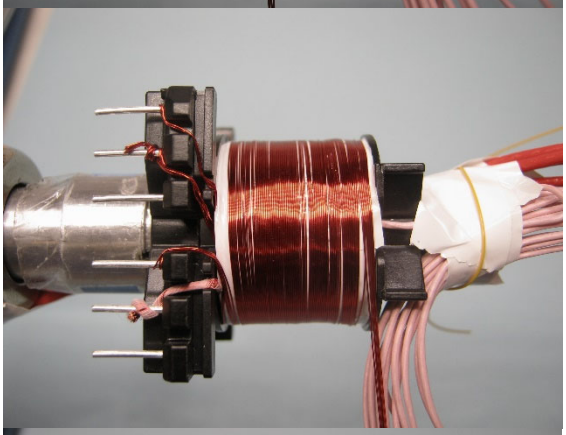
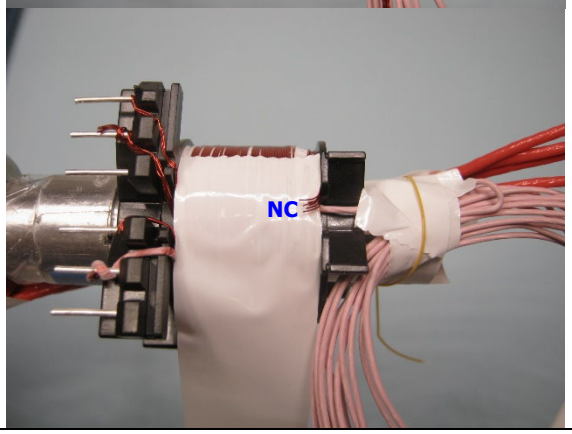
9.6 *Winding Illustrations*

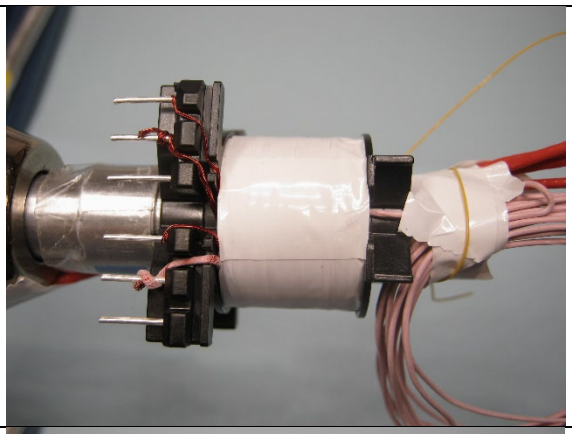
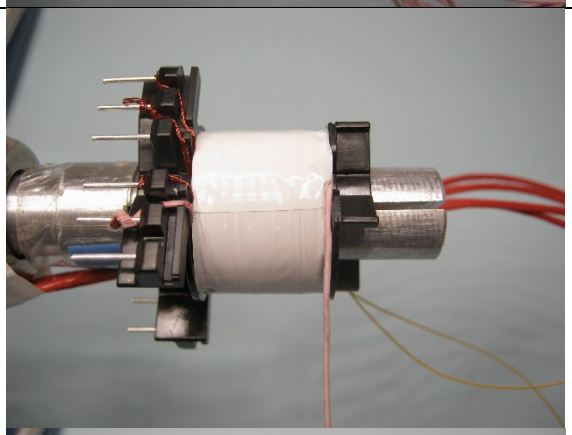
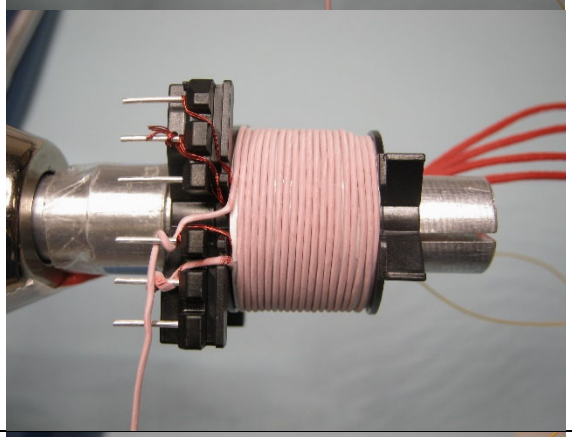
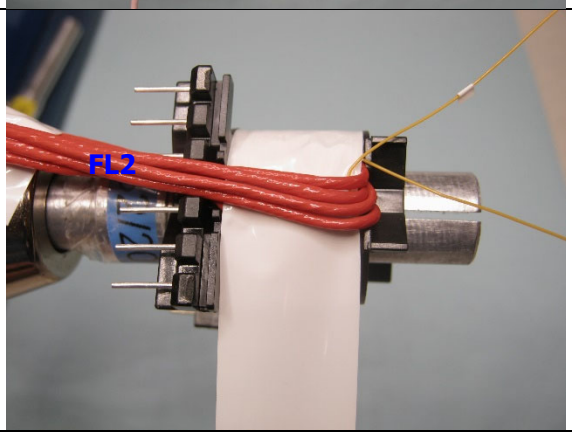
Winding Preparation		Place the bobbin Item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 **1st Primary**	 	Start at pin 5, wind 20 turns of wire Item [3] in 1 layer, from left to right, at the last turn exit the wire out of the bobbin leave enough length of this wire for WD7:2nd Primary.

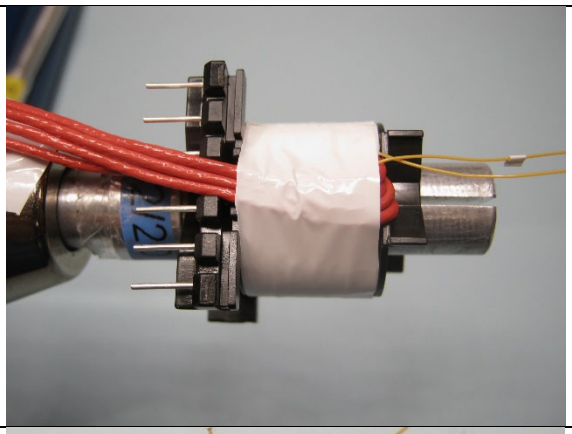
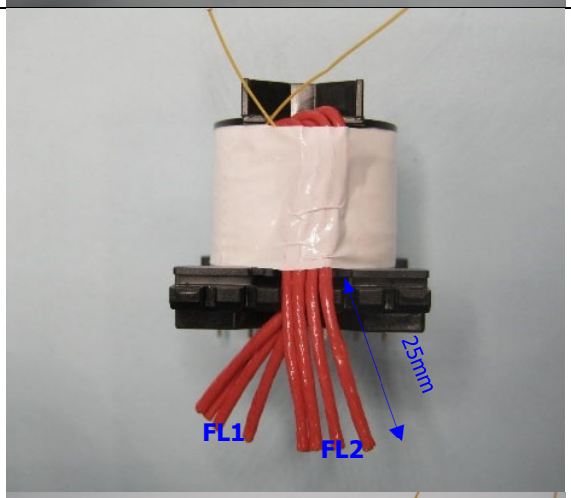
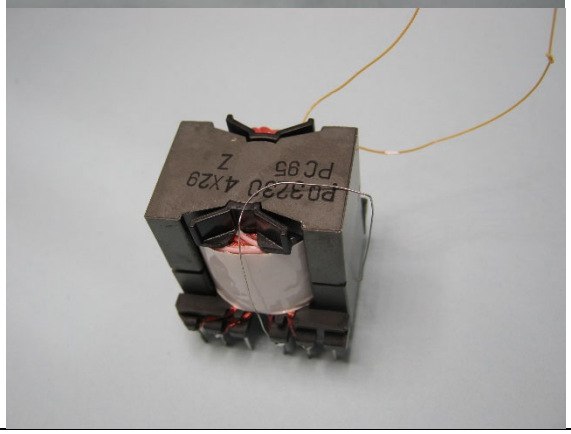
Insulation		1 layer of tape Item [8].
WD2 & WD3 **Bias & Shield 1**	  	Use 6 wires Item [4], starting at pin 1 for WD2, also use 6 wires Item [4], starting at pin 2 for WD3. Wind all these wires in parallel, at 3rd turn, place 1 small piece of tape to hold wires, bring 6 wires for WD2 to the left to terminate at pin 2. Continue to wind 6 wires for WD3 to 10th turn then cut short wires as No-Connect (NC).

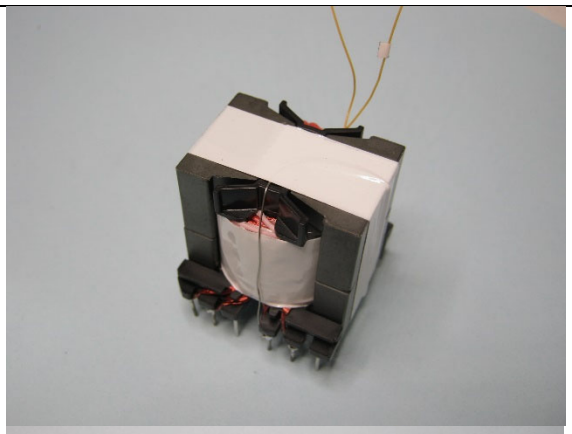
	 	
Insulation		1 layer of tape Item [8].
WD4 Secondary		Start at the slot on the left on secondary side of the bobbin, use 2 wires Item [5], leave ~25 mm floating, and mark as FL1, wind 5 bi-filar turns in 1 layer. At the last turn, exit the wire at the slot on the right also leave ~45 mm floating and mark as FL2 for 1st halves of Secondary. Repeat another winding as above for 2nd halves of

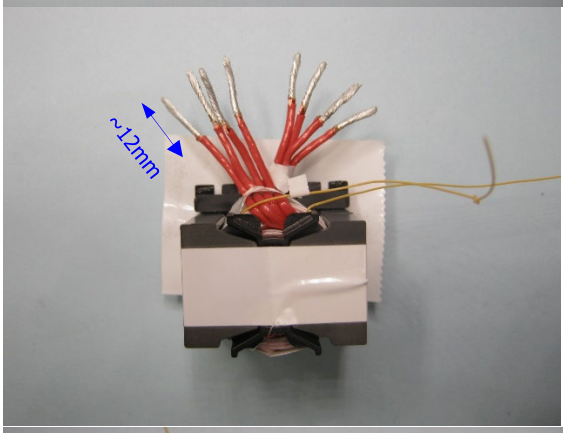
	 	Secondary which is parallel with 1st halves Secondary.
WD5 **Secondary Bias**	 	Use wire Item [7], start from the right and on the primary side of bobbin, leaving ~50 mm and mark as FL3. Wind 2 turns and exit the wire also leaving 50 mm and mark as FL4.

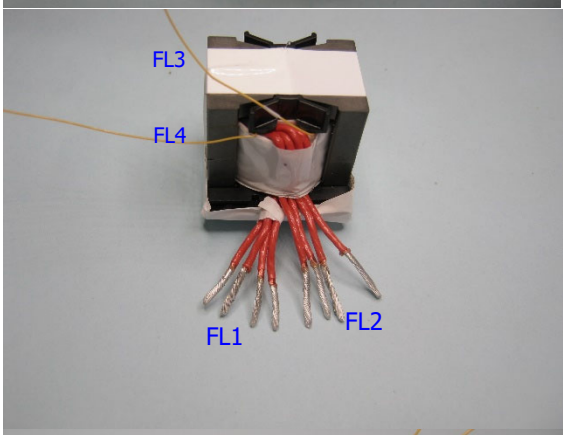
Insulation		1 layer of tape Item [8].
WD6 **Shield2**	  	Start at pin 4, use 6 wires Item [4], wind 13 turns from left to right. At the last turn, cut short the wires as No-Connect.

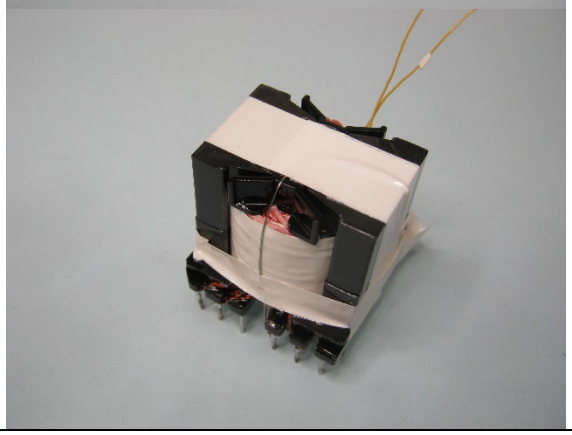
Insulation		1 layer of tape Item [8].
WD7 **2nd Primary**	 	Use wire floating from WD1, wind 20 turns from right to left, and terminate at pin 4.
Insulation		1 layer of tape Item [8] and bring the secondary wires FL2 to the left in between layers of tape.

		
Finish	 	Cut short secondary wires ~ 25mm. Gap cores to 430 μH, solder bus wire Item [7] to pin 2 which leans along with core halves, and secure with tape. Places 2 layers of tape Item [10] at the bottom of transformer, then wrap up to cover secondary side of transformer, and wrap around the body of transformer 1 layer of tape Item [9], *(see illustration below).* Varnish Item [11].




~12mm


FL3
FL4
FL1
FL2



10 Heat Sink

10.1 *Heat Sink Drawing*

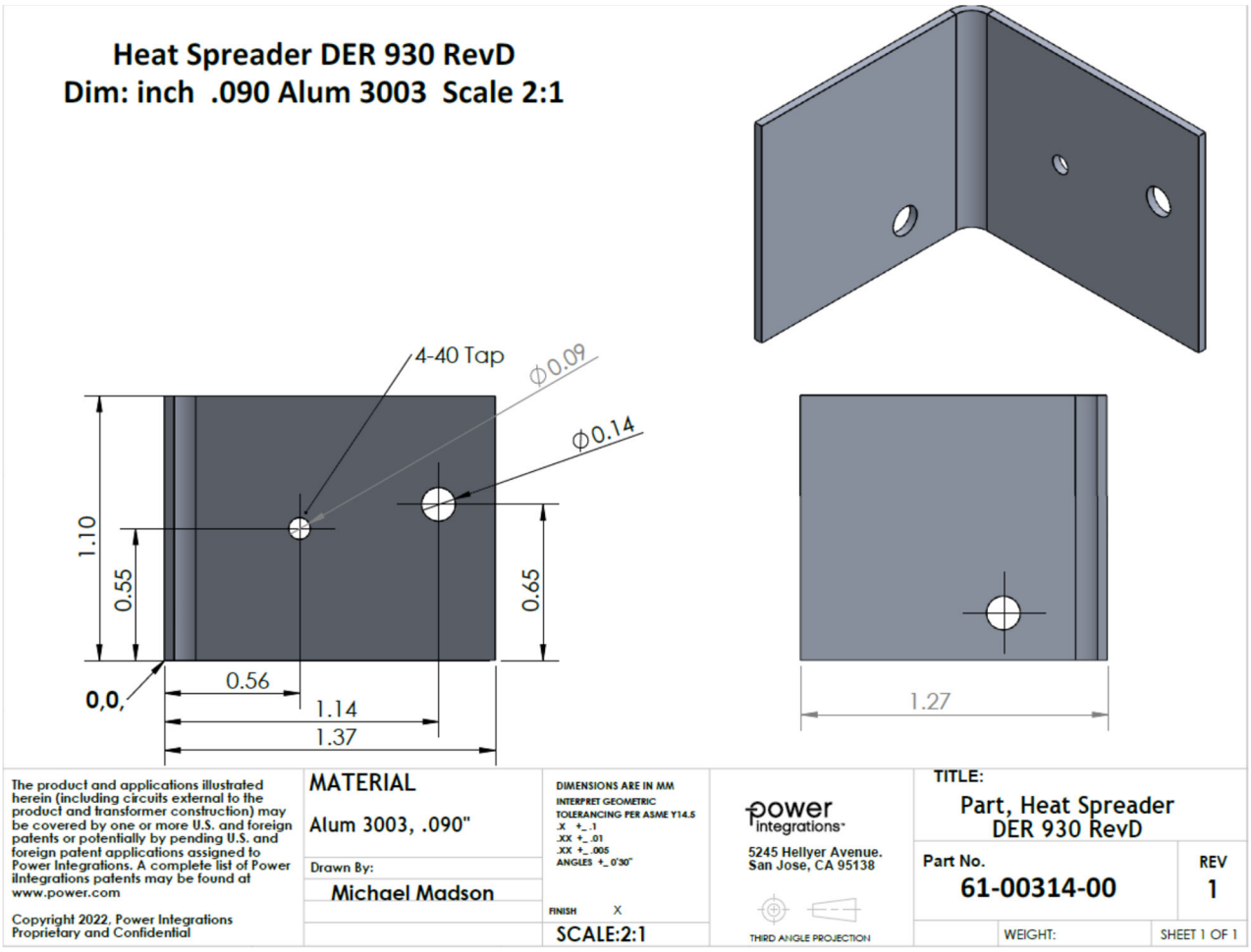


Figure 12 – Bridge Rectifier and PFC Boost Diode Heat Sink Drawing.

10.2 *Heat Sink Fab Drawing*

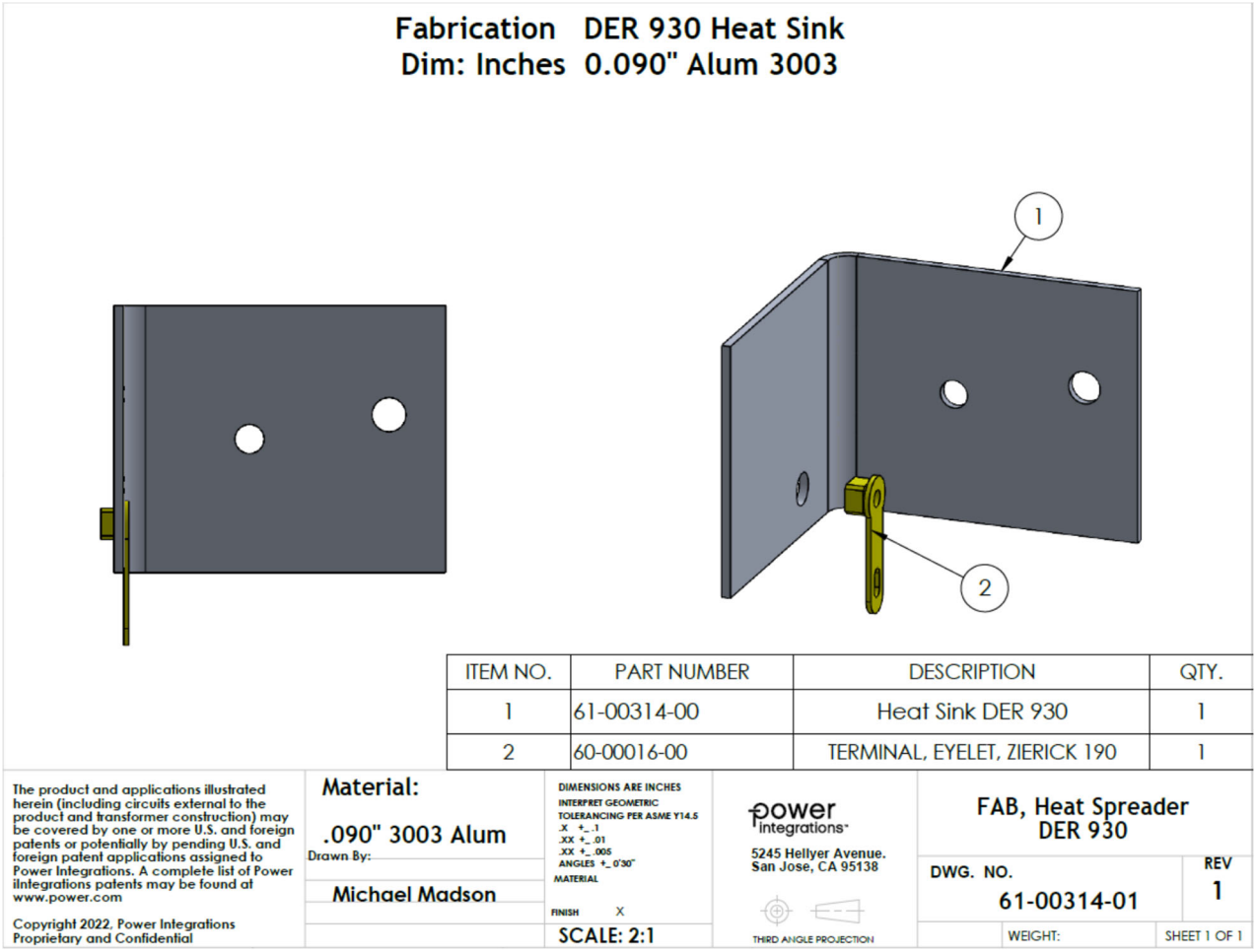
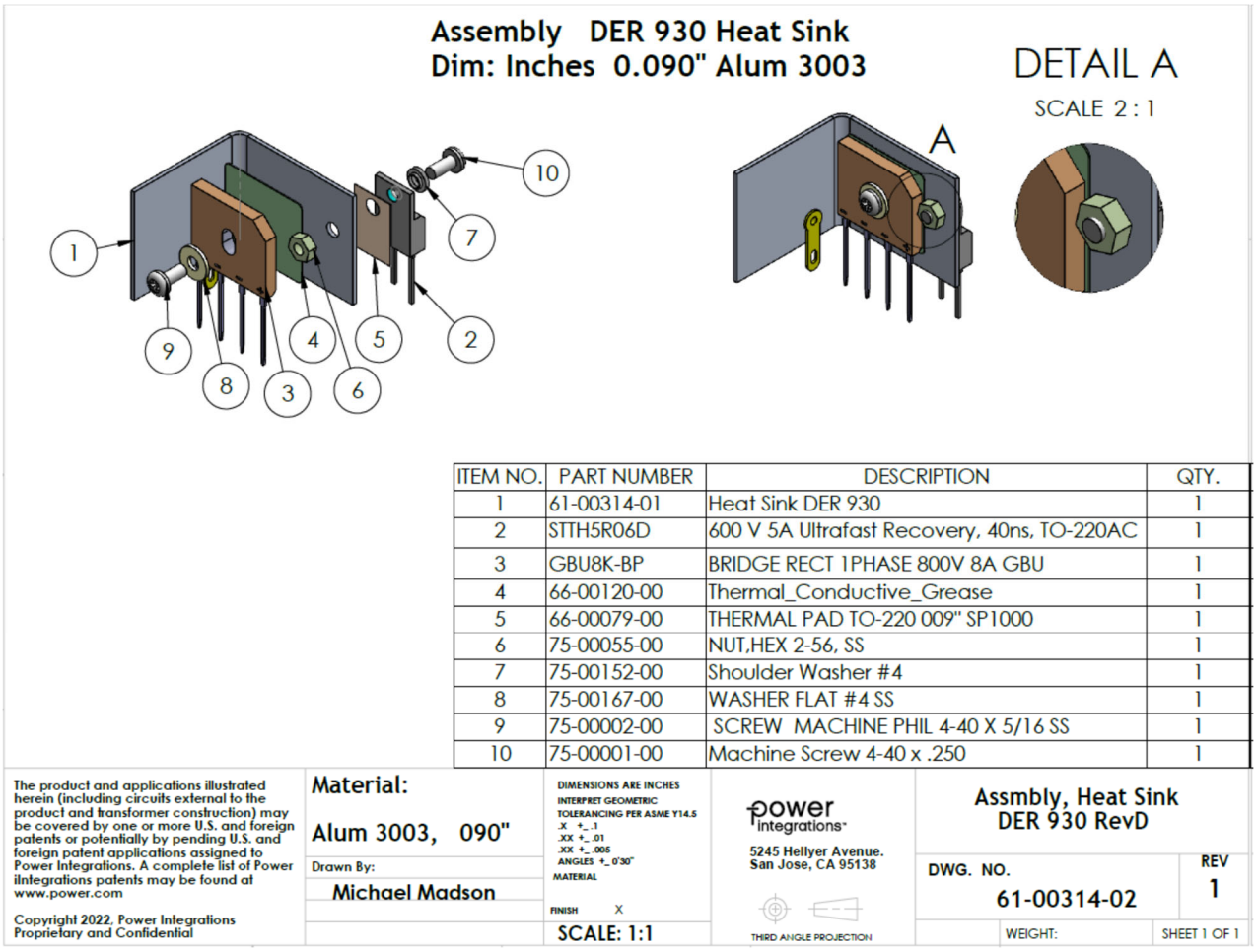


Figure 13 – Bridge Rectifier and PFC Boost Diode Heat Sink Fabrication Drawing.

10.3 *Heat Sink Assembly Drawing*



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00314-01	Heat Sink DER 930	1
2	STTH5R06D	600 V 5A Ultrafast Recovery, 40ns, TO-220AC	1
3	GBU8K-BP	BRIDGE RECT 1PHASE 800V 8A GBU	1
4	66-00120-00	Thermal_Conductive_Grease	1
5	66-00079-00	THERMAL PAD TO-220 009" SP1000	1
6	75-00055-00	NUT,HEX 2-56, SS	1
7	75-00152-00	Shoulder Washer #4	1
8	75-00167-00	WASHER FLAT #4 SS	1
9	75-00002-00	SCREW MACHINE PHIL 4-40 X 5/16 SS	1
10	75-00001-00	Machine Screw 4-40 x .250	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

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Material:
Alum 3003, 090"

Drawn By:
Michael Madson

DIMENSIONS ARE INCHES
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power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

Assmbly, Heat Sink
DER 930 RevD

DWG. NO. 61-00314-02
REV 1
WEIGHT:
SHEET 1 OF 1

Figure 14 – Bridge Rectifier and PFC Boost Diode Heat Sink Assembly Drawing.

11 PFC Inductor Design Spreadsheet

1	Hiper_PFS-5_Boost_051822; Rev.1.1; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO			400	VDC	Nominal load voltage
9	PO	189		189	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.9600		0.9600		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX	14		14	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN	300		300	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			159	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)			168	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)			177	uH	Maximum PFC inductance value
24	LP_TOL			5.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			168	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.13		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			2.19	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			2.60	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.47	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection
36	PFS Part Number	PFS5177F	Warning	PFS5177F		Peak power rating for the device has been exceeded. Output might droop. Change the input voltage range, enter higher output power selection factor, or select a larger device.
37	Self-Supply Feature	Yes		Yes		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	1.0		1.0		Programmable output power selection factor
39	PO_MAX_DEV			185	W	Maximum output power of the device

40	IOCP min			6.44	A	Minimum Current limit
41	IOCP typ			7.40	A	Typical current limit
42	IOCP max			8.36	A	Maximum current limit
43	IP			5.85	A	MOSFET peak current
44	IRMS			2.25	A	PFS MOSFET RMS current
45	RDSON			0.23	Ohms	Typical RDSon at 100 'C
46	FS_PK			84.0	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			73.9	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			1.170	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.020	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			1.190	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			47.63	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	Auto		PQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	Auto		PQ26/20		Core part number
62	Ae			119.00	mm^2	Core cross sectional area
63	Le			46.30	mm	Core mean path length
64	AL			5490.00	nH/t^2	Core AL value
65	Ve			5.47	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			3.30	mm	Core height/Height of window; ID if toroid
67	MLT			56.2	mm	Mean length per turn
68	BW			9.20	mm	Bobbin width
69	LG			0.86	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)			3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3889	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			2582	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
77	I_TEST			7.4	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3441	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
80	**Wire**					
81	TURNS			32		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)

82	ILRMS			2.60	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	42		42	AWG	Inductor wire gauge
85	Filar	150		150		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.064	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			1.09	mm	Will be different than OD if Litz
88	DCR			0.084	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.35		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J			5.48	A/mm^2	Estimated current density of wires. It is recommended that 4 < J < 6
91	Layers			3.99		Estimated layers in winding
92	**Auxiliary Winding**					
93	N_AUX	3		3		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX			1.71	V	Maximum voltage across the auxiliary winding
95	V_VS_MIN			-35.13	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2524	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.282	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.601	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			0.883	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	STTH5R06		STTH5R06		PFS Diode Part Number
106	Type / Part Number			ULTRAFAST		PFC Diode Type / Part Number
107	Manufacturer			ST		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			5.00	A	Diode rated forward current
110	Qrr			125.0	nC	Qrr at High Temperature
111	VF			1.80	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.861	W	Estimated Diode conduction losses
113	PSW_DIODE			0.000	W	Estimated Diode switching losses
114	P_DIODE			0.861	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
117	HEATSINK Theta-CA			66.19	degC/W	Maximum thermal resistance of heatsink
118	IFSM			50.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	120		120	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			13.1	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			22.2	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			1.38	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.55	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.30	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			1.17	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.126	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.753	W	Estimated High frequency ESR loss in Output capacitor
131	Total CO LOSS			0.879	W	Total estimated losses in Output Capacitor
134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			8.43	A^2*s	Minimum I^2t rating for fuse

136	Fuse Current rating			3.39	A	Minimum Current rating of fuse
137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			2.11	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			3.545	W	Estimated Bridge Diode conduction loss
141	CIN			0.68	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.010	W	Input Capacitor Loss
144	RT1			9.37	ohms	Input Thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
150	RPS			> 400	kOhms	Power programmability resistor. Leaving PS pin open is acceptable
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			320.5	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			26.1	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			1.190	W	Total estimated losses in PFS
174	Boost diode Losses			0.861	W	Total estimated losses in Output Diode
175	Input Bridge losses			3.545	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.010	W	Total estimated losses in input capacitor
177	Inductor losses			0.883	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.879	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.479	W	Total estimated losses in EMI choke copper
180	Total losses			7.845	W	Overall loss estimate
181	Efficiency			96.01	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			1.046	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the HiperPFS-5

						part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2	330		330	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
190	LDM_calc			251	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
191	CX1	330		330	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			221	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	**Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.**					

Note: The warnings on the spreadsheet have been verified to not be an issue for this design.

12 Transformer Design Spreadsheet

1	ACDC_InnoSwitch4-CZ_Flyback_051822; Rev.2.1; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 CZ Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	300		300	V	Minimum DC input voltage
5	VIN_MAX	410		410	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Range of AC input voltage
7	LINEFREQ				Hz	AC Input voltage frequency
8	CAP_INPUT				uF	Input capacitor
9	VOUT			20.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	9.000		9.000	A	Output current
12	POUT			180.00	W	Output power
13	EFFICIENCY	0.97		0.97		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	INN4177		INN4177		Generic device code
22	DEVICE_CODE			INN4177C		Actual device code
23	POUT_MAX			200	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.25	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			4.278	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			4.600	A	Typical current limit of the primary switch
27	ILIMIT_MAX			4.922	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.15	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			620.0	V	Peak drain voltage on the primary switch during turn-off
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	57000		57000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	160.0		160.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			300.00	V	Valley of the minimum input AC voltage at full load
38	KP			1.18		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			DCM		Mode of operation
40	DUTYCYCLE			0.312		Primary switch duty cycle
41	TIME_ON			6.49	us	Primary switch on-time
42	TIME_OFF			11.64	us	Primary switch off-time
43	LPRIMARY_MIN			408.0	uH	Minimum primary inductance
44	LPRIMARY_TYP			429.5	uH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			451.0	uH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			4.386	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal

51	IAVG_PRIMARY			0.611	A	Primary switch average current
52	IRIPPLE_PRIMARY			4.386	A	Primary switch ripple current
53	IRMS_PRIMARY			1.337	A	Primary switch RMS current
55	**SECONDARY CURRENT**					
56	IPEAK_SECONDARY			35.091	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
58	IRMS_SECONDARY			14.644	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	PQ32/30		PQ32/30		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE			B65879B0000R095		Core code
66	AE			153.80	mm^2	Core cross sectional area
67	LE			67.80	mm	Core magnetic path length
68	AL			6100	nH/turns^2	Ungapped core effective inductance
69	VE			10440.0	mm^3	Core volume
70	BOBBIN			B65880E2012D001		Bobbin
71	AW			104.00	mm^2	Window area of the bobbin
72	BW			18.50	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			40		Primary turns
77	BPEAK			3693	Gauss	Peak flux density
78	BMAX			3164	Gauss	Maximum flux density
79	BAC			1582	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			268	nH/turns^2	Typical gapped core effective inductance
81	LG			0.688	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			3		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY	5		5		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			2		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	**CLAMPZERO**					
96	LLEAK			4.30	uH	Primary winding leakage inductance
97	CCLAMP			100.0	nF	Primary clamp capacitor
98	RD_CLAMPZERO	130		130	kΩ	HSD resistor
99	TLLDL/THLDL			430.0	ns	HSD resistor programmed delay
100	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			375.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
101	TIME_VDS_VALLEY			42.7	ns	Time taken by the VDS ring to reach its first valley
102	IPEAK_CLAMPZERO			4.333	A	Active clamp peak current
104	**LINE UNDERVOLTAGE**					
105	BROWN-IN REQURED	112.0		112.0	V	Required AC RMS/DC line voltage brown-in threshold
106	RLS			4.00	MΩ	Connect two 2 MOhm resistors to the V-pin for the required UV/OV threshold
107	BROWN-IN ACTUAL			113.4	V	Actual AC RMS/DC brown-in threshold
108	BROWN-OUT ACTUAL			102.5	V	Actual AC RMS/DC brown-out threshold

110	**LINE OVERVOLTAGE**					
111	OVERVOLTAGE_LINE			477.4	V	Actual AC RMS/DC line over-voltage threshold
113	**PRIMARY BIAS DIODE**					
114	VBIAS_PRIMARY	10.0		10.0	V	Rectified primary bias voltage
115	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
116	VREVERSE_BIASDIODE_PRIMARY			40.75	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
117	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
118	CBPP			0.47	uF	BPP pin capacitor
122	**SECONDARY COMPONENTS**					
123	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
124	RFB_LOWER			6.81	kΩ	Lower feedback resistor
125	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127	**SECONDARY BIAS DIODE**					
128	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
129	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
130	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
131	VREVERSE_BIASDIODE_SECONDARY			25.50	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
132	CBIAS_SECONDARY			10	uF	Bias winding rectification capacitor
133	CBPS			2.20	uF	BPP pin capacitor
136	**MULTIPLE OUTPUT PARAMETERS**					
137	**OUTPUT 1**					
138	VOUT1			20.00	V	Output 1 voltage
139	IOUT1			9.00	A	Output 1 current
140	POUT1			180.00	W	Output 1 power
141	IRMS_SECONDARY1			14.644	A	Root mean squared value of the secondary current for output 1
142	IRIPPLE_CAP_OUTPUT1			11.552	A	Current ripple on the secondary waveform for output 1
143	NSECONDARY1			5		Number of turns for output 1
144	VREVERSE_RECTIFIER1			71.25	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
145	SRFET1	AONS66920		AONS66920		Secondary rectifier (Logic MOSFET) for output 1
146	VF_SRFET1			0.096	V	SRFET on-time drain voltage for output 1
147	VBREAKDOWN_SRFET1			100	V	SRFET breakdown voltage for output 1
148	RDSON_SRFET1			10.7	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
176	PO_TOTAL			180.00	W	Total power of all outputs
177	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

13 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. For data points showing performance across varying input line voltage and output load current, measurements were taken from full load to no load, with input line voltage from low-line to high-line, at room temperature ambient (approximately 25 °C) unless otherwise specified.

13.1 *No-Load Input Power*

Note: For each line voltage, soak time = 10 min and integration time = 10 min.

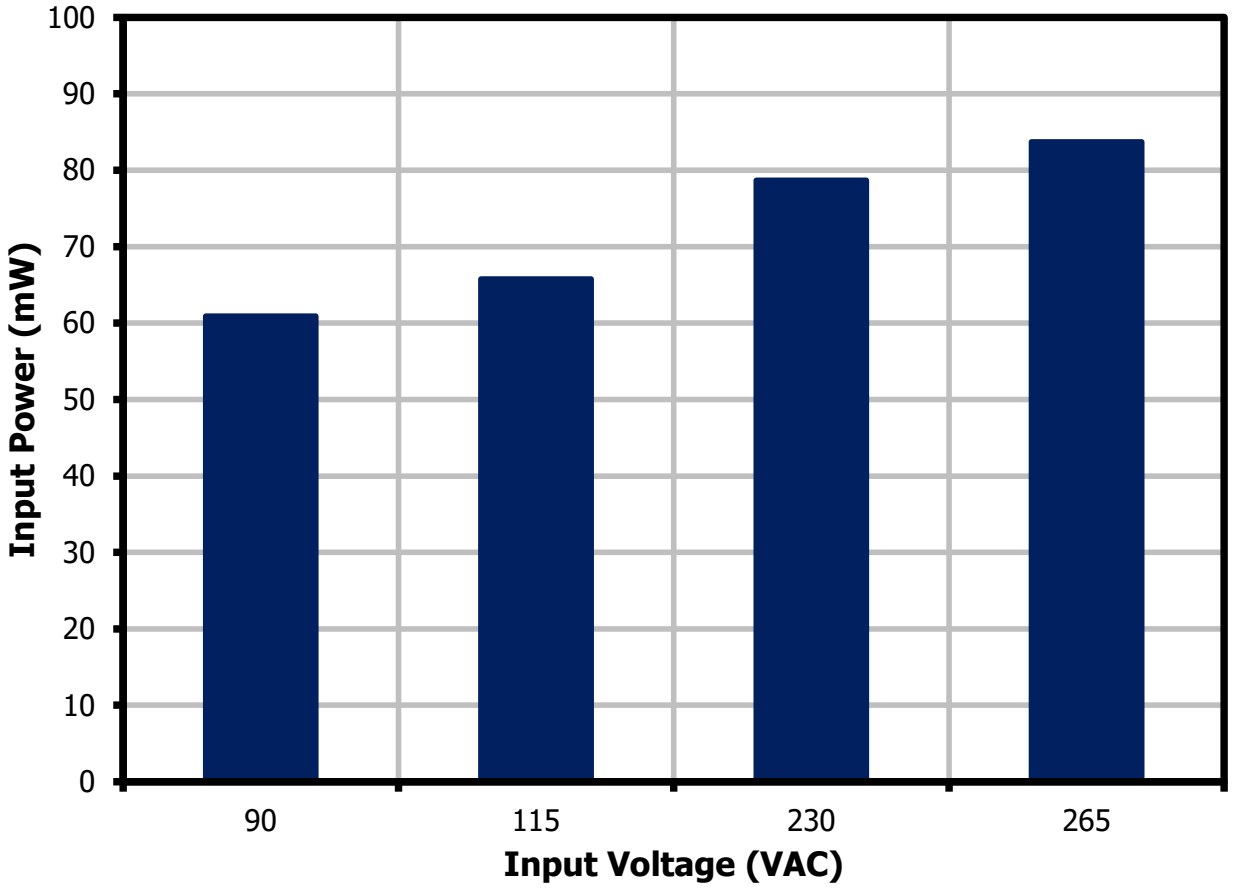


Figure 15 – No-Load Input Power vs. Input Line Voltage.

13.2 *Average and 10% Load Efficiency*

Measurements were taken after 30-minute delay per input line voltage and 5-minute delay per load condition. Output voltage was measured on the board.

13.2.1 Output: 20 V / 9 A

Input (VAC)	Load (%)	Design Performance					
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
90	100	195.97	20.18	9.008	181.77	92.75	**92.90**
	75	146.82	20.20	6.757	136.51	92.98	
	50	97.80	20.21	4.506	91.05	93.10	
	25	48.93	20.15	2.253	45.40	92.79	
	10	19.97	20.09	0.903	18.13	90.77	
115	100	194.03	20.18	9.008	181.80	93.70	**93.60**
	75	145.63	20.20	6.757	136.52	93.74	
	50	97.16	20.21	4.506	91.07	93.73	
	25	48.71	20.15	2.253	45.41	93.23	
	10	19.96	20.09	0.903	18.13	90.85	
230	100	191.36	20.18	9.008	181.76	94.98	**94.68**
	75	143.78	20.20	6.758	136.49	94.93	
	50	96.02	20.21	4.506	91.06	94.83	
	25	48.33	20.16	2.253	45.41	93.96	
	10	19.88	20.09	0.903	18.13	91.19	
265	100	191.00	20.18	9.008	181.77	95.17	**94.84**
	75	143.56	20.20	6.758	136.50	95.08	
	50	95.89	20.21	4.507	91.06	94.96	
	25	48.23	20.15	2.253	45.41	94.15	
	10	19.82	20.09	0.903	18.14	91.51	

13.3 *Efficiency Across Line at 100% Load (On Board)*

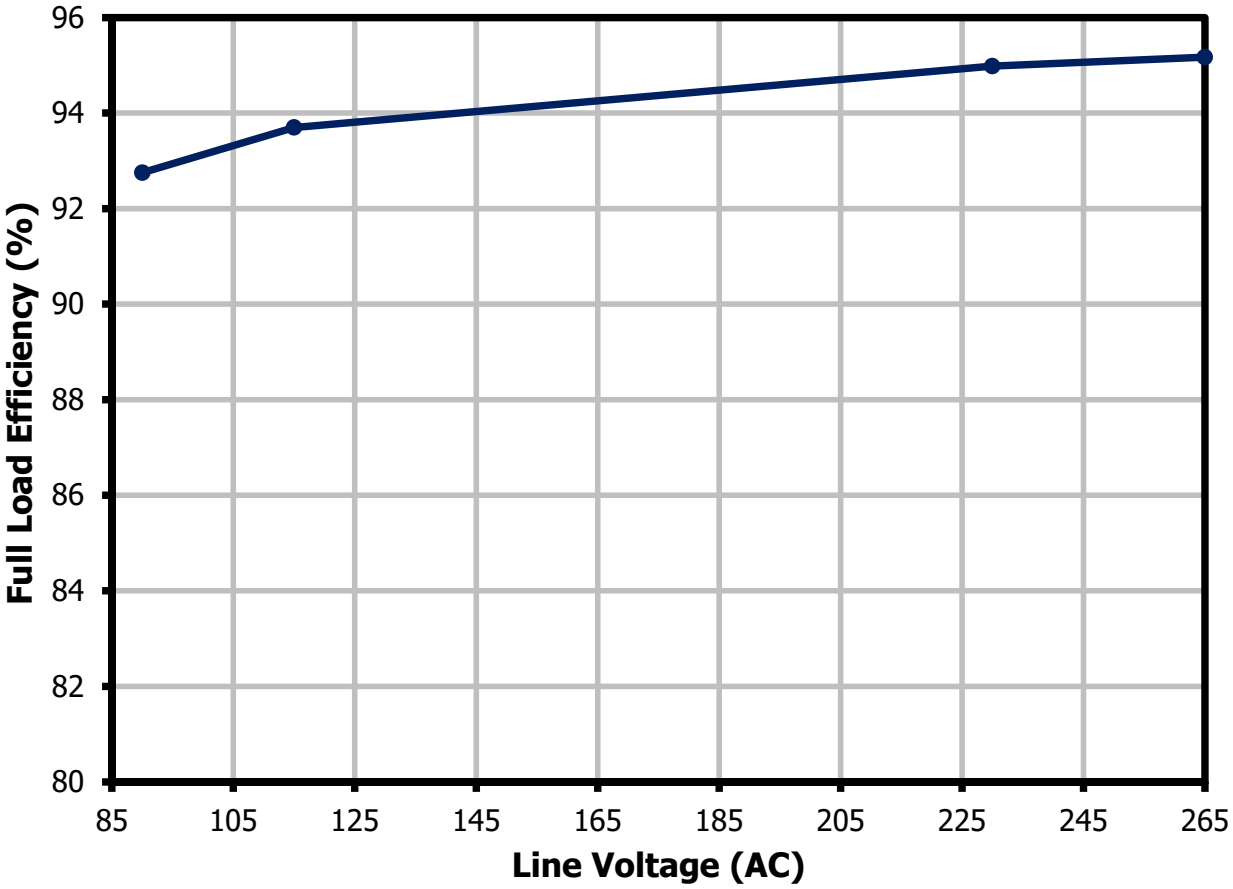


Figure 16 – Full Load Efficiency vs. Input Line for 20 V / 9 A Output, Room Temperature.

13.4 *Efficiency Across Load (On Board)*

13.4.1 Output: 20 V

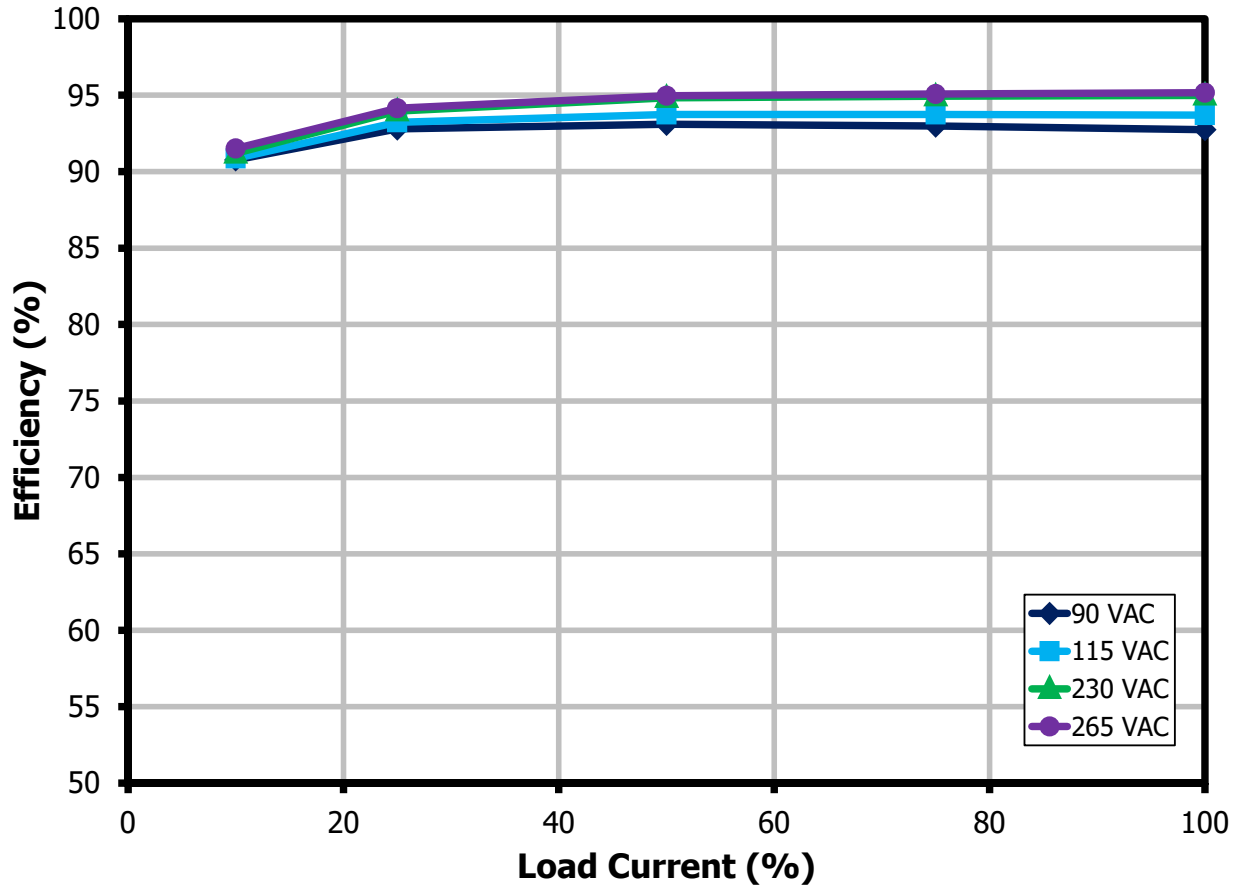


Figure 17 – Efficiency vs. Load for 20 V Output, Room Temperature.

13.5 *Load Regulation (On Board)*

13.5.1 Output: 20 V

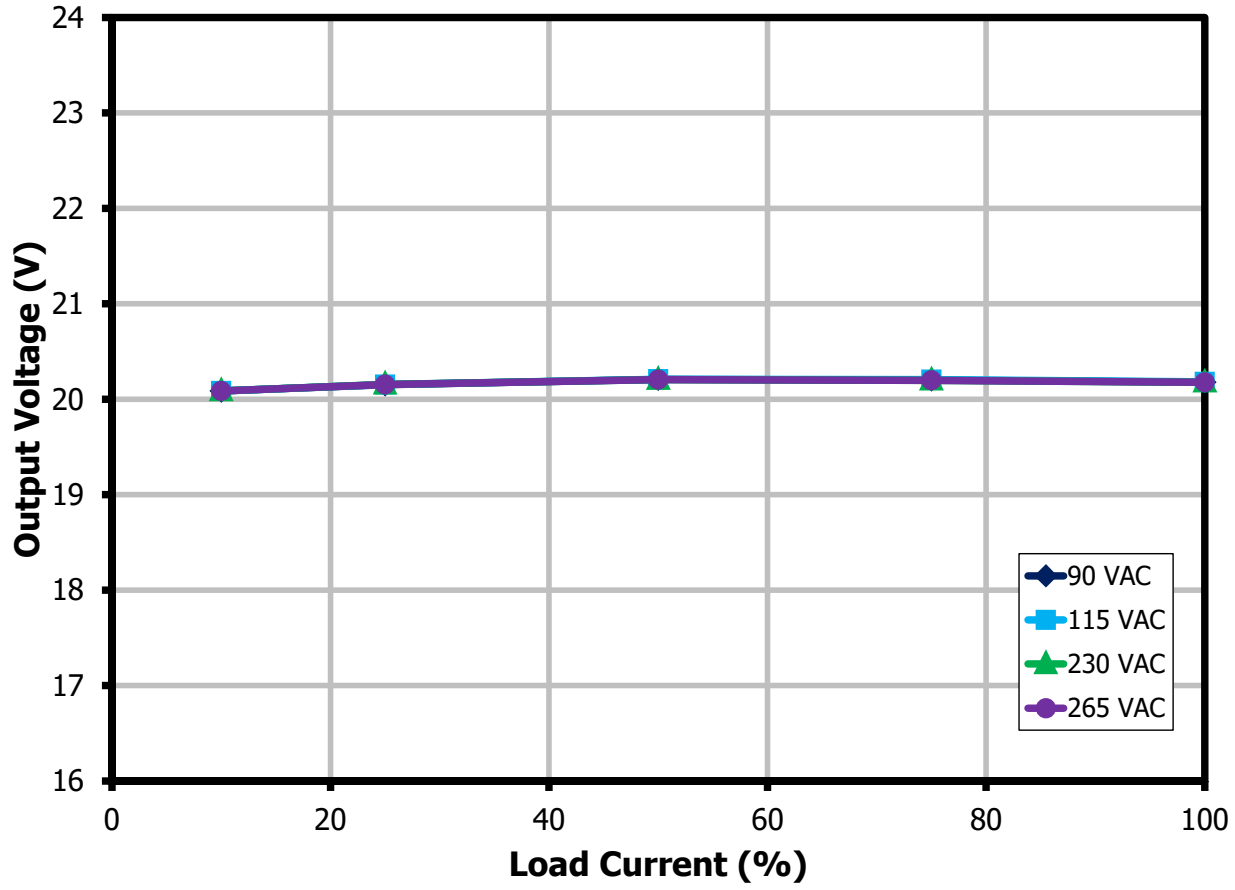


Figure 18 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

13.6 *Line Regulation (On Board)*

13.6.1 Output: 20 V / 9 A

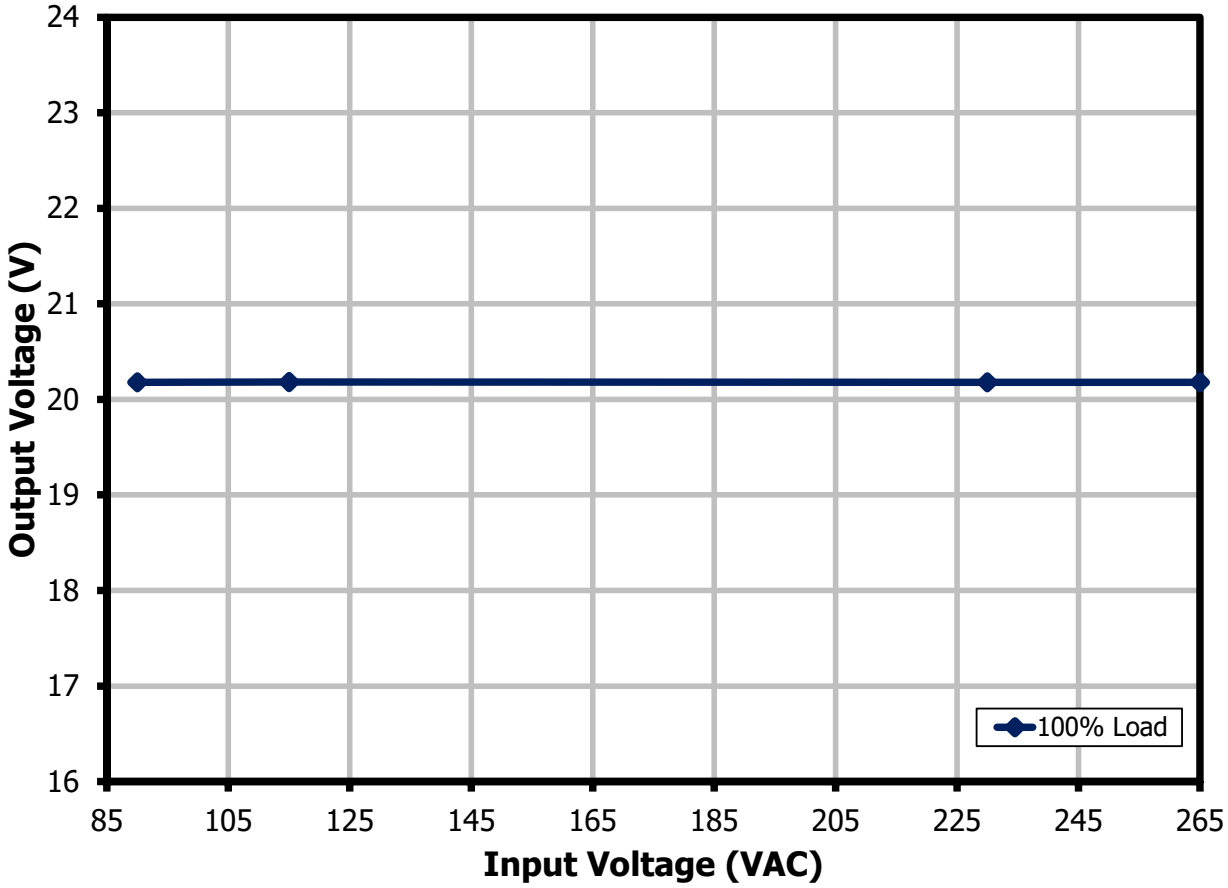


Figure 19 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

13.7 *Power Factor*

13.7.1 Power Factor vs. Load

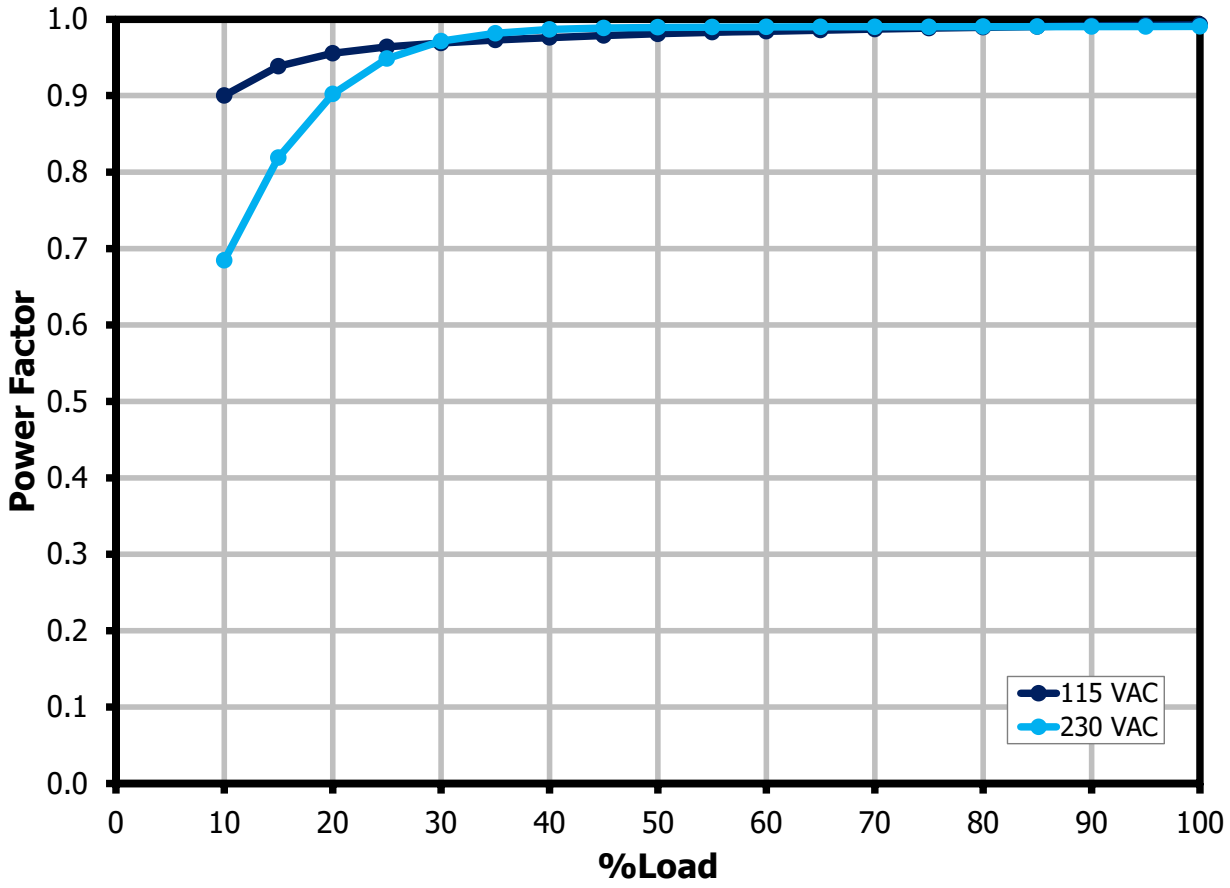


Figure 20 – Power Factor vs. Load for 20 V Output, Room Temperature.

13.8 *THD*

13.8.1 THD vs. Load

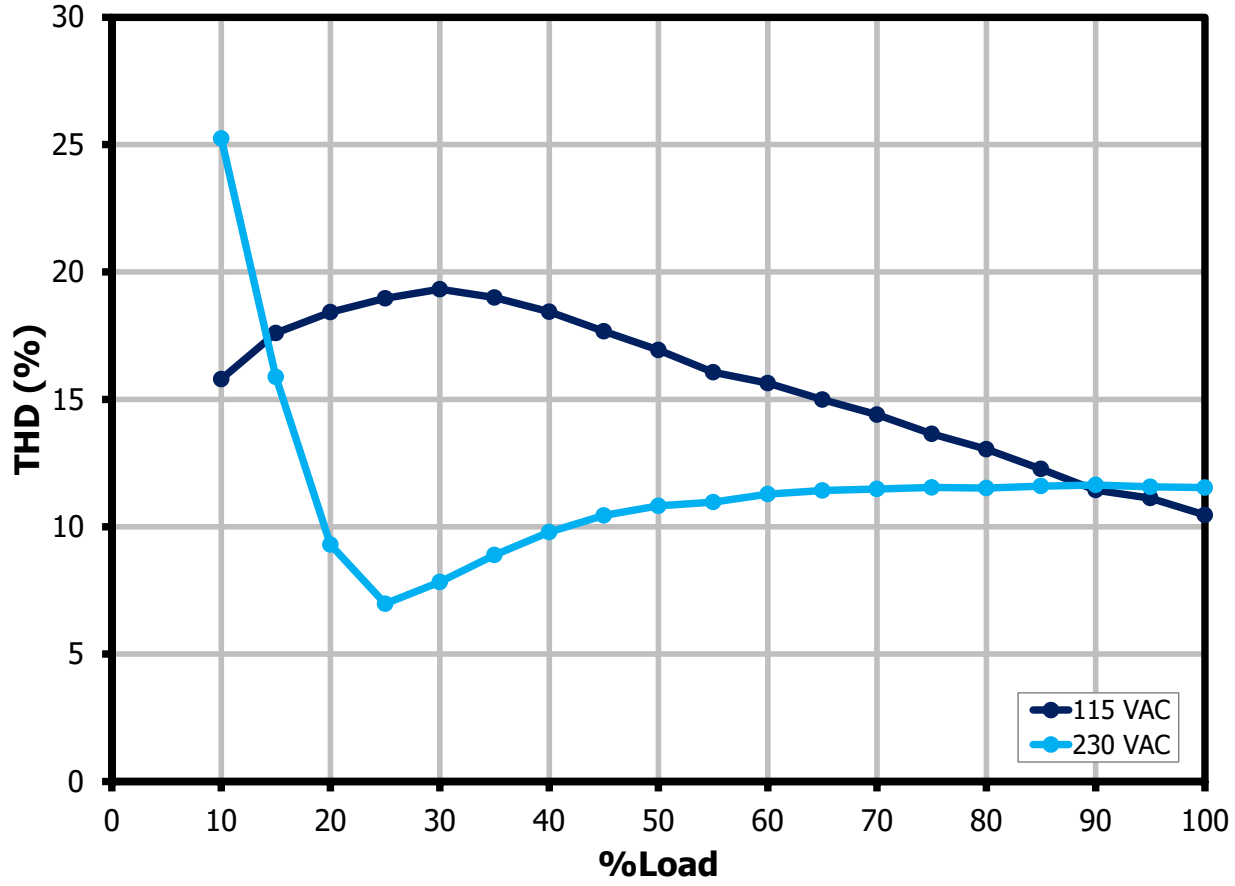


Figure 21 – THD vs. Load for 20 V Output, Room Temperature.

14 Thermal Performance

14.1 *Thermal Performance in Open Case, Room Temperature*

Note: 1. Open case thermal images are taken at room temperature ambient with the unit inside a closed acrylic box and 2-hour soak per condition.
2. For enclosed adapter application, this design requires use of metallic heat spreader and suitable thermally conductive insulator pads to ensure low temperature of the bridge rectifiers, HiperPFS-5, InnoSwitch4-CZ IC, and SR FETs. The performance data below is for open case operation and does not use heat spreader for cooling.

14.1.1 Output: 20 V / 9 A

Parameter	Temperature (°C) at 90 VAC	Temperature (°C) at 265 VAC
Ambient Temperature	40	37.2
HiperPFS-5 (U1)	110.7	67.7
ClampZero (U2)	101.6	86.8
InnoSwitch4-CZ (U3)	102	88.2
SR FET (Q1/Q2)	96.2	92.7
Schottky Diode (D7)	94.8	91.3
Bridge (BR1)	119.2	68.6
XFMR Core (T1)	91.1	83.5
XFMR Secondary Winding (T1)	97.8	90.8
SR Snubber Resistor (R28)	76.7	71.2
Primary Bias Diode (D5)	97.1	80.3
Output Capacitor (C26)	90.7	84
PFC Inductor core (T2)	90.3	59.9
PFC Inductor Winding (T2)	95.8	62.8
Bulk Capacitor (C4)	87.2	63.4
PFC Boost Diode (D3)	110.9	81.9
Heat Sink	111.1	68.9
Common Mode Choke (L2)	85.4	50.7
Differential Mode Choke (L3)	93.4	55.9
Secondary Rsense (R30)	88.6	87.7

15 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C).

15.1 *Input Voltage and Current Waveforms*

15.1.1 Output: 20 V / 9 A

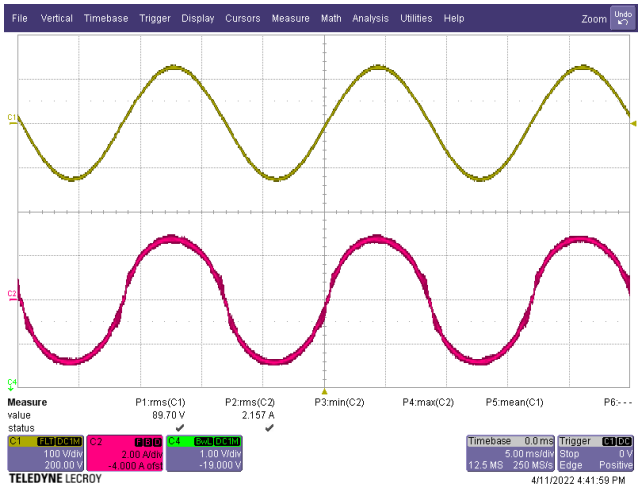


Figure 22 – Input Voltage and Current.
90 VAC.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 2 A / div.
Time: 5 ms / div.

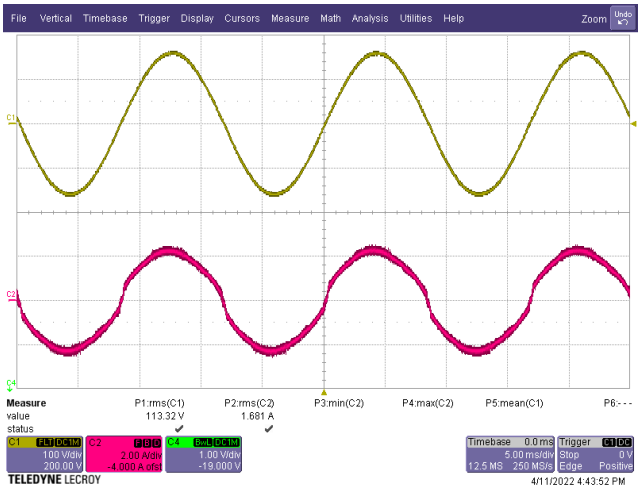


Figure 23 – Input Drain Voltage and Current.
115 VAC.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 2 A / div.
Time: 5 ms / div.

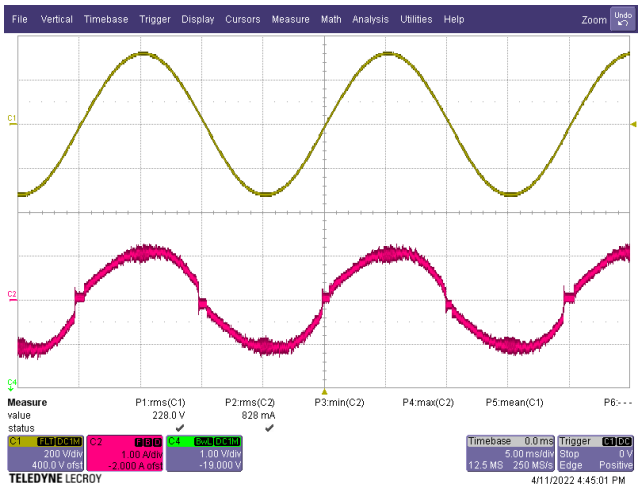


Figure 24 – Input Voltage and Current.
230 VAC.
CH1: V_{IN_AC}, 200 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 5 ms / div.

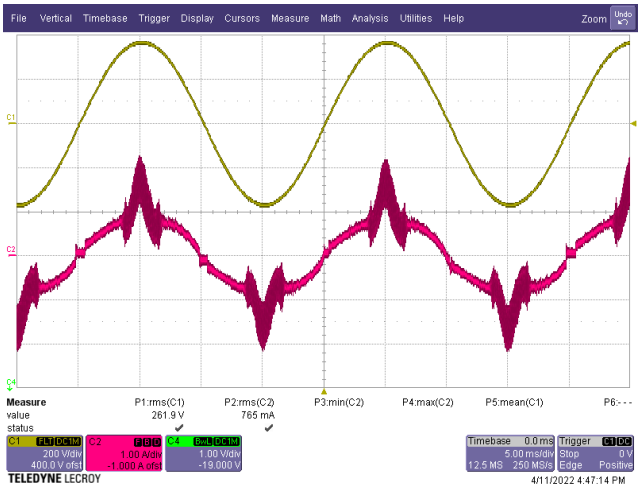


Figure 25 – Input Drain Voltage and Current.
265 VAC.
CH1: V_{IN_AC}, 200 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 5 ms / div.

15.2 *PFC Inductor Current and HiperPFS-5 Drain Voltage Waveforms*

15.2.1 Output: 20 V / 9 A

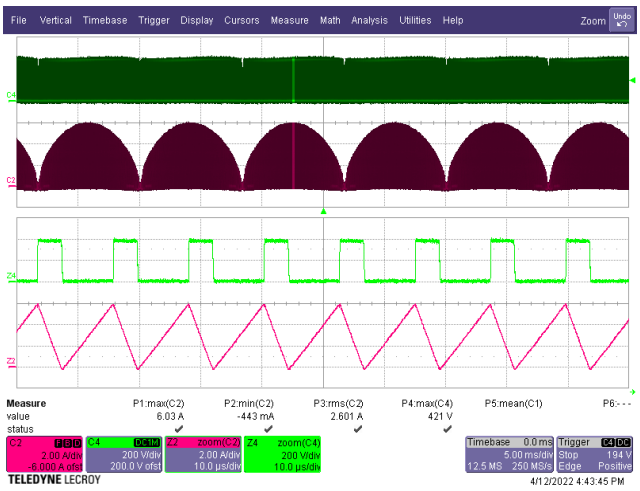


Figure 26 – PFC Inductor Current and HiperPFS-5. Drain Voltage 90 VAC.
V_{DS_PFS} = 421 V Maximum.
I_{L_PFC} = 6.03 A Maximum.
CH4: V_{DS_PFS}, 200 V / div.
CH2: I_{L_PFC}, 2 A / div.
Time: 5 ms / div. (10 μs / div. Zoom).

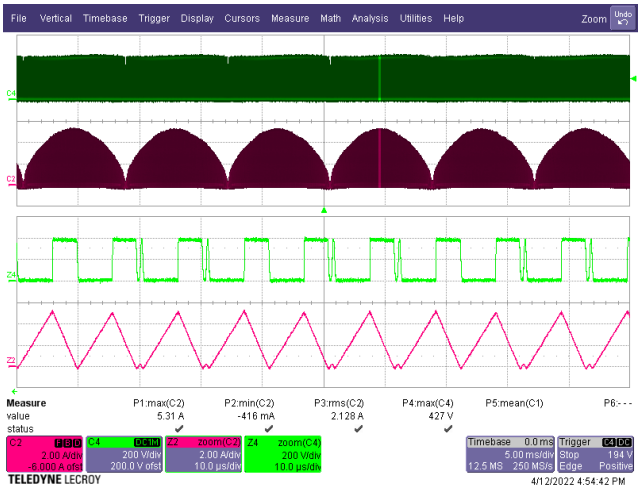


Figure 27 – PFC Inductor Current and HiperPFS-5. Drain Voltage 115 VAC.
V_{DS_PFS} = 427 V Maximum.
I_{L_PFC} = 5.31 A Maximum.
CH4: V_{DS_PFS}, 200 V / div.
CH2: I_{L_PFC}, 2 A / div.
Time: 5 ms / div. (10 μs / div. Zoom).

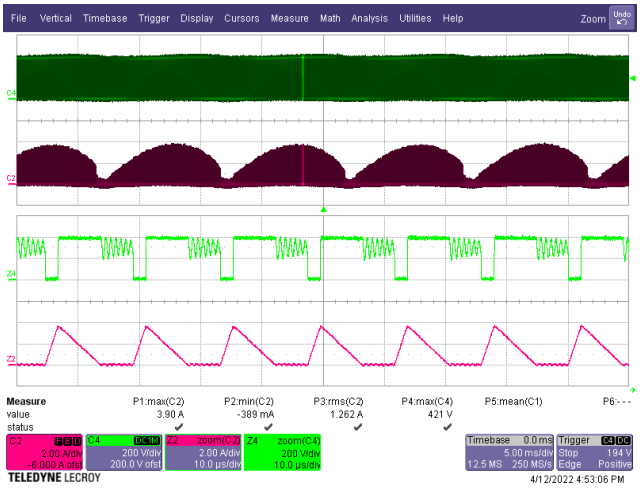


Figure 28 – PFC Inductor Current and HiperPFS-5. Drain Voltage 230 VAC.
V_{DS_PFS} = 421 V Maximum.
I_{L_PFC} = 3.9 A Maximum.
CH4: V_{DS_PFS}, 200 V / div.
CH2: I_{L_PFC}, 2 A / div.
Time: 5 ms / div. (10 μs / div. Zoom).

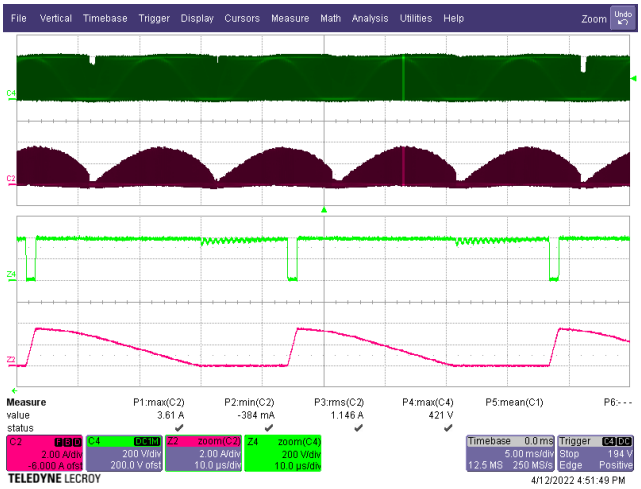


Figure 29 – PFC Inductor Current and HiperPFS-5. Drain Voltage 265 VAC.
V_{DS_PFS} = 421 V Maximum.
I_{L_PFC} = 3.61 A Maximum.
CH4: V_{DS_PFS}, 200 V / div.
CH2: I_{L_PFC}, 2 A / div.
Time: 5 ms / div. (10 μs / div. Zoom).

15.3 ***Start-up Waveforms***

15.3.1 Output Voltage and Current

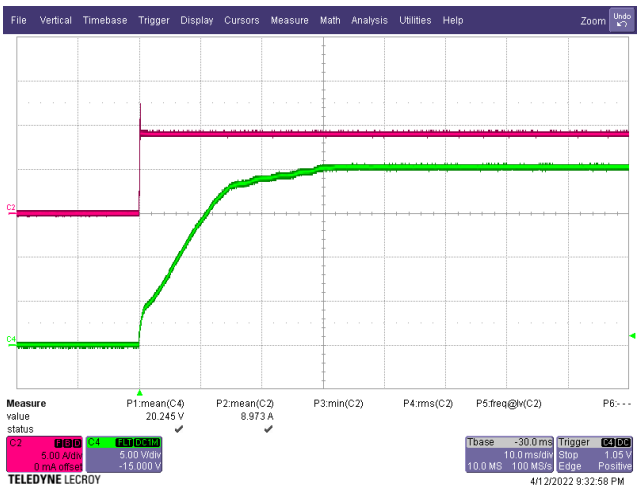


Figure 30 – Output Voltage and Current at Start-up.
20 V, 9 A.
V_{OUT} = 20.245 V Steady-State.
CH4: V_{OUT}, 5 V / div.
CH2: I_{LOAD}, 5 A / div.
Time: 10 ms / div.

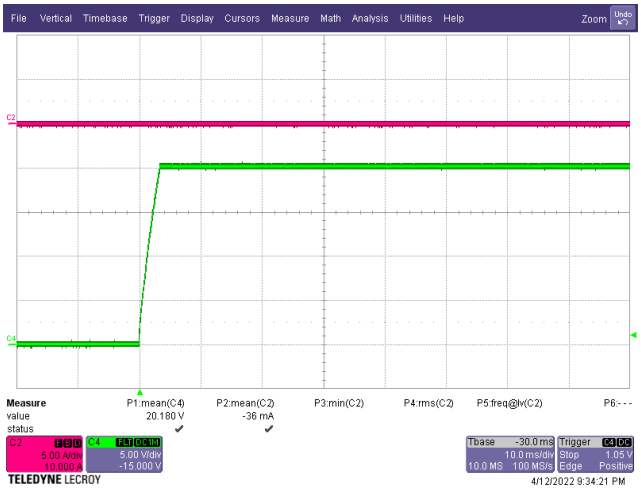


Figure 31 – Output Voltage and Current at Start-up.
20 V, 0 A.
V_{OUT} = 20.18 V Steady-State.
CH4: V_{OUT}, 5 V / div.
CH2: I_{LOAD}, 5 A / div.
Time: 10 ms / div.

15.3.1 HiperPFS-5 Drain Voltage, Input Voltage and Inductor Current

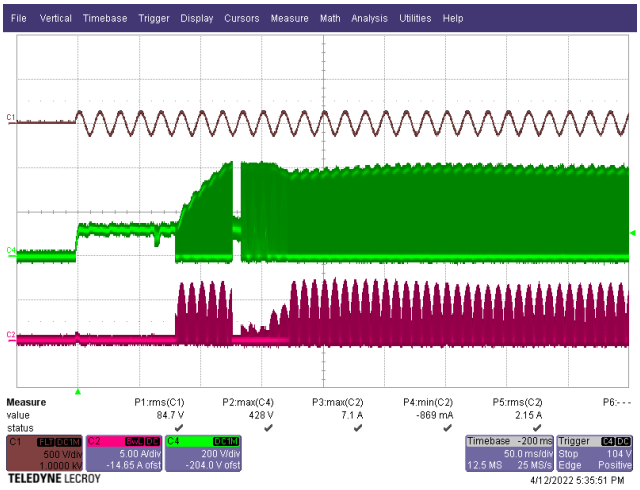


Figure 32 – PFC Inductor Current and HiperPFS-5.
Drain Voltage at start-up 90 VAC.
V_{DS_PFS} = 428 V Maximum.
I_{L_PFC} = 7.1 A Maximum.
CH1: V_{IN}, 500 V / div.
CH2: I_{L_PFC}, 5 A / div.
CH4: V_{DS_PFS}, 200 V / div.
Time: 50 ms / div.

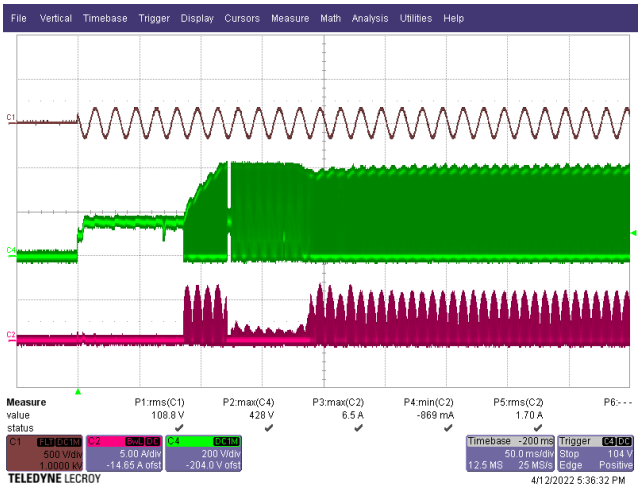


Figure 33 – PFC Inductor Current and HiperPFS-5.
Drain Voltage at start-up 115 VAC.
V_{DS_PFS} = 428 V Maximum.
I_{L_PFC} = 6.5 A Maximum.
CH1: V_{IN}, 500 V / div.
CH2: I_{L_PFC}, 5 A / div.
CH4: V_{DS_PFS}, 200 V / div.
Time: 50 ms / div.

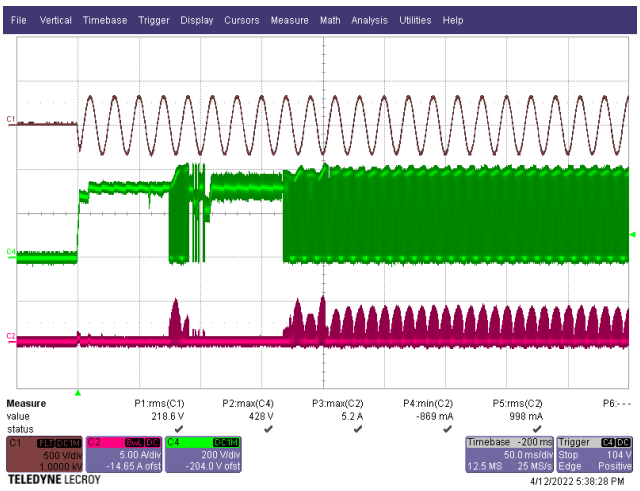


Figure 34 – PFC Inductor Current and HiperPFS-5. Drain Voltage at start-up 230 VAC.
V_{DS_PFS} = 428 V Maximum.
I_{L_PFC} = 5.2 A Maximum.
CH1: V_{IN}, 500 V / div.
CH2: I_{L_PFC}, 5 A / div.
CH4: V_{DS_PFS}, 200 V / div.
Time: 50 ms / div.

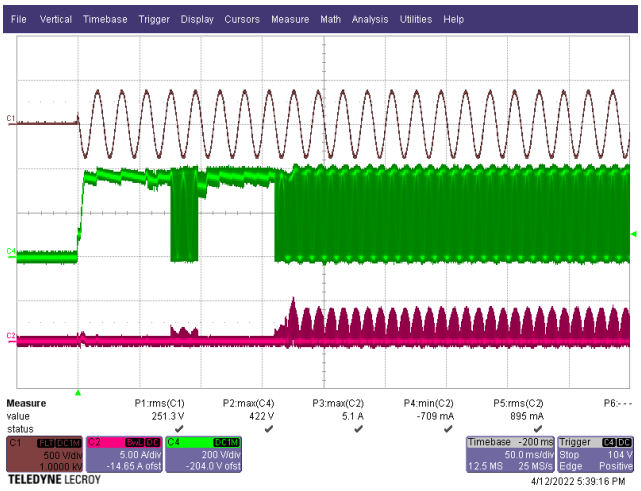


Figure 35 – PFC Inductor Current and HiperPFS-5. Drain Voltage at start-up 265 VAC.
V_{DS_PFS} = 422 V Maximum.
I_{L_PFC} = 5.1 A Maximum.
CH1: V_{IN}, 500 V / div.
CH2: I_{L_PFC}, 5 A / div.
CH4: V_{DS_PFS}, 200 V / div.
Time: 50 ms / div.

15.3.2 Primary Drain Voltage and Current

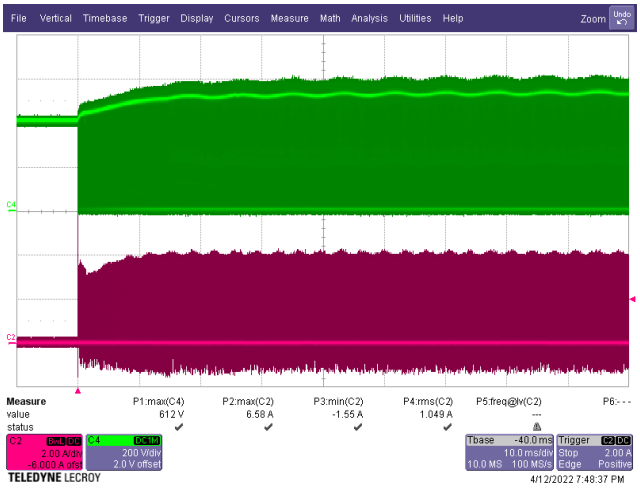


Figure 36 – Primary Drain Voltage and Current. 20 V, 9 A.
V_{DS_PRI} = 612 V Maximum.
CH4: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 2 A / div.
Time: 10 ms / div.

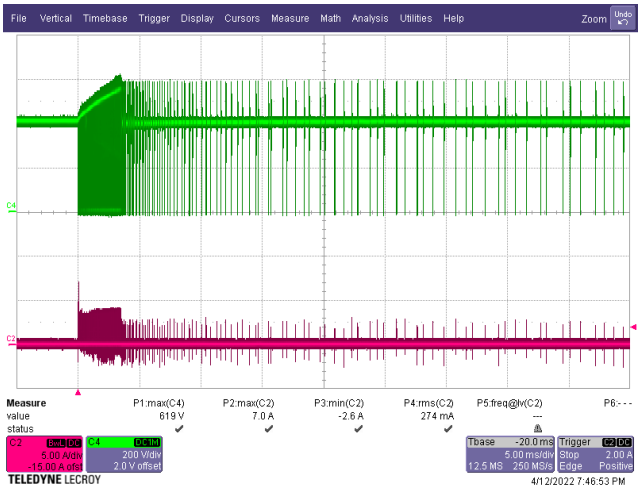


Figure 37 – Primary Drain Voltage and Current. 20 V, 0 A.
V_{DS_PRI} = 619 V Maximum.
CH4: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 5 A / div.
Time: 5 ms / div.

15.3.3 Clamp Zero Drain Voltage and Current

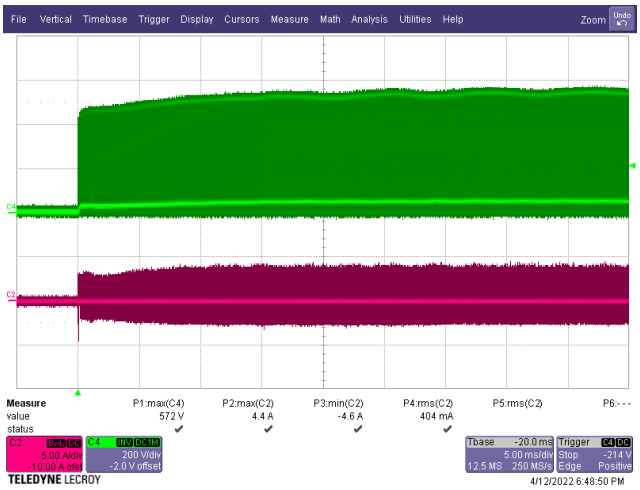


Figure 38 – Primary Drain Voltage and Current.
20 V, 9.0 A Load.
V_{DS_CPZ} = 572 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 5 A / div.
Time: 5 ms / div.

Figure 39 – Primary Drain Voltage and Current.
20 V, 0 A Load.
V_{DS_CPZ} = 584 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 5 A / div.
Time: 5 ms / div.

15.3.4 SR FET Drain Voltage and Current

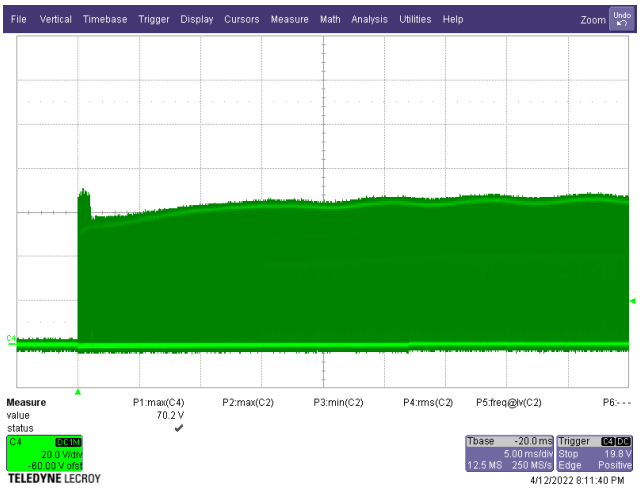


Figure 40 – SR FET Drain Voltage and Current.
20 V, 9 A Load.
V_{DS_SRFET} = 70.2 Maximum.
CH4: V_{DS_SRFET}, 20 V / div.
Time: 5 ms / div.

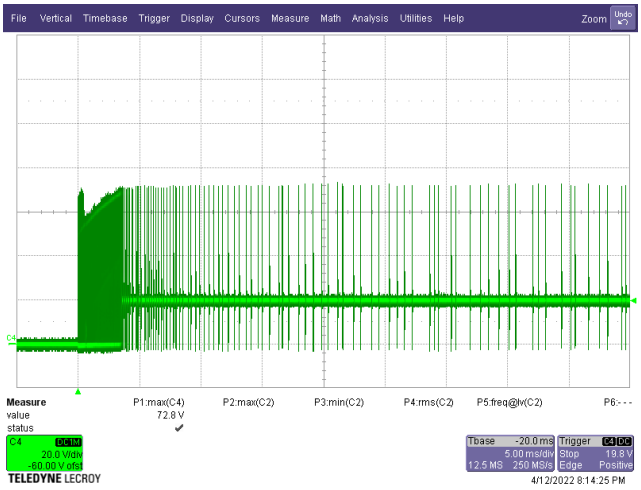


Figure 41 – SR FET Drain Voltage and Current.
20 V, 0 A Load.
V_{DS_SRFET} = 72.8 Maximum.
CH4: V_{DS_SRFET}, 20 V / div.
Time: 5 ms / div.

15.4 ***Primary Drain Voltage (Steady-State)***

15.4.1 Output: 20 V / 9 A

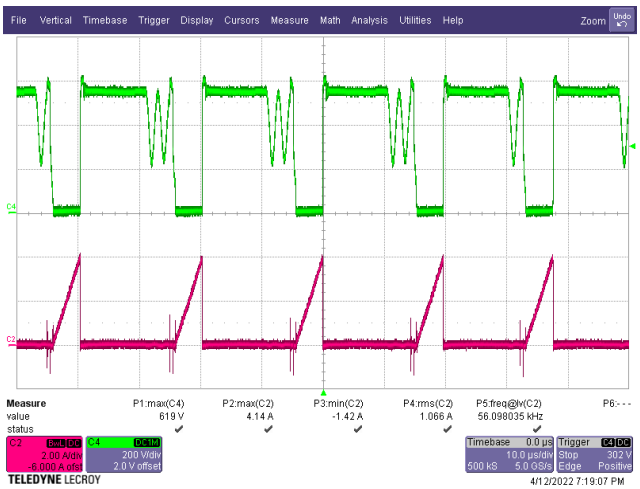


Figure 42 – Primary Drain Voltage and Current.
20 V, 9 A Load.
V_{DS_CPZ} = 619 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 2 A / div.
Time: 10 µs / div.

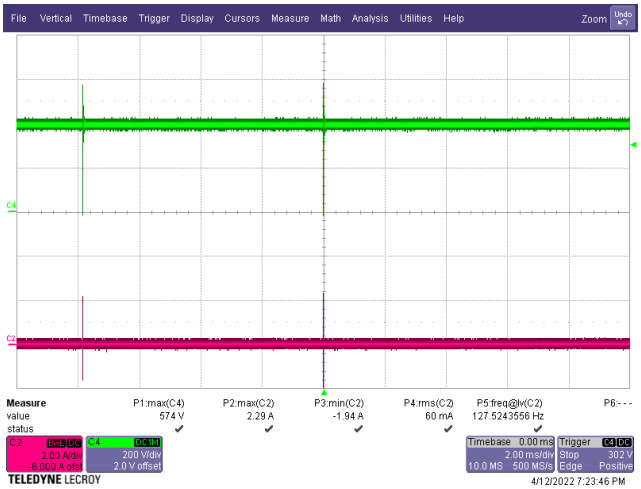


Figure 43 – Primary Drain Voltage and Current.
20 V, 0 A Load.
V_{DS_CPZ} = 574 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 2 A / div.
Time: 2 ms / div.

15.5 *ClampZero Drain Voltage and Current (Steady-State)*

15.5.1 Output: 20 V

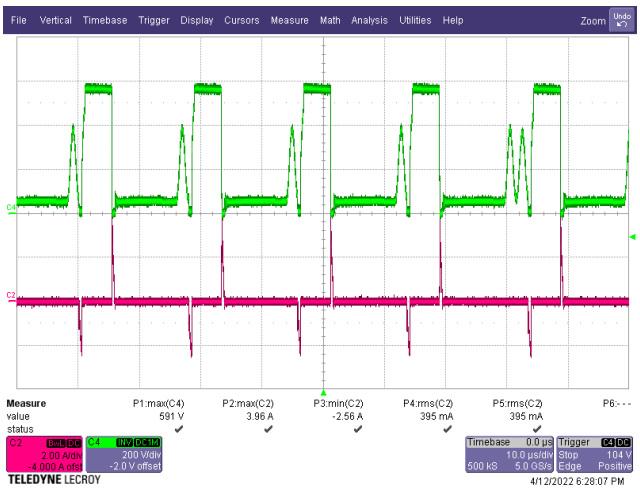


Figure 44 – ClampZero Drain Voltage and Current.
20 V, 9 A Load.
V_{DS_CPZ} = 591 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 2 A / div.
Time: 10 µs / div.

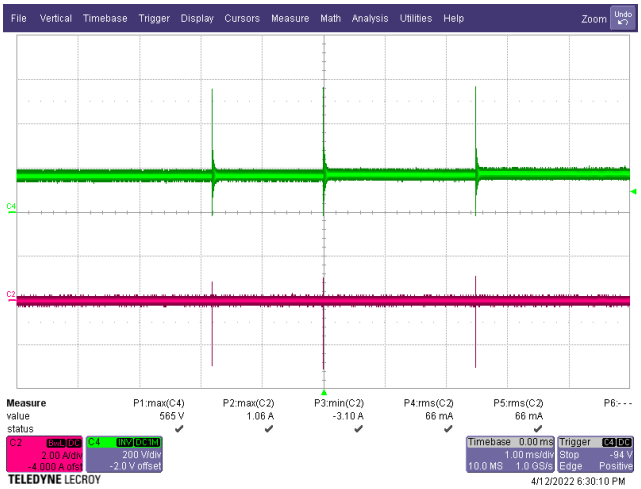


Figure 45 – ClampZero Drain Voltage and Current.
20 V, 0 A Load.
V_{DS_CPZ} = 565 V Maximum.
CH4: V_{DS_CPZ}, 200 V / div.
CH2: I_{DS_CPZ}, 2 A / div.
Time: 10 µs / div.

15.6 ***SR FET Drain Voltage (Steady-State)***

15.6.1 Output: 20 V

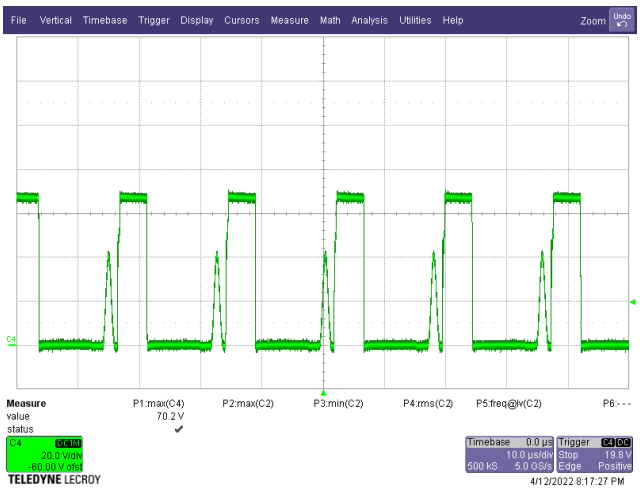


Figure 46 – SR FET Drain Voltage.
20 V, 9 A Load.
V_{DS_SRFET} = 70.2 Maximum.
CH4: V_{DS_SRFET}, 20 V / div.
Time: 10 µs / div.

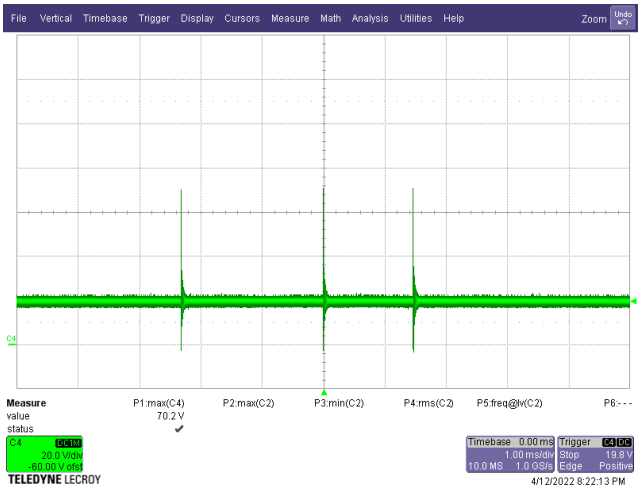


Figure 47 – SR FET Drain Voltage.
20 V, 0 A Load.
V_{DS_SRFET} = 70.2 Maximum.
CH4: V_{DS_SRFET}, 20 V / div.
Time: 1 ms / div.

15.7 *Load Transient Response*

Output voltage waveform on the board was captured with dynamic load transient from 0% to 100%. Duration for load states (high = 500 μs; low = 500 μs) was chosen to clearly show steady-state for each load condition. Load slew rate is set to 1 A / μs.

15.7.1 Output: 20 V

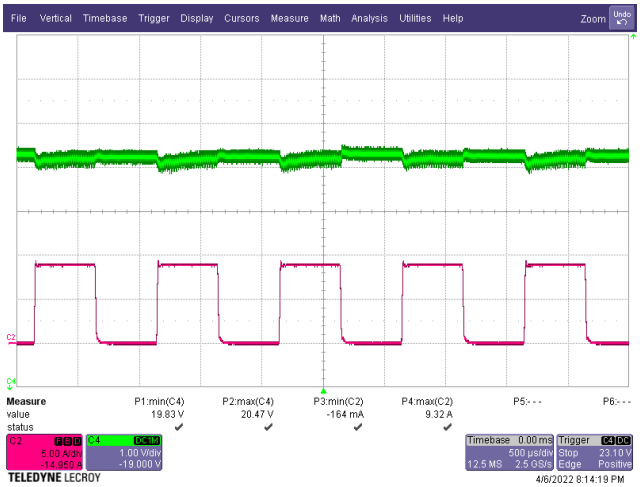


Figure 48 – Transient Response.
20 V, 0 A to 9 A Load.
V_{OUT} = 20.47 V Max., 19.83 V Min.
CH4: V_{OUT}, 1 V / div.
CH2: I_{OUT}, 5 A / div.
Time: 500 μs / div.

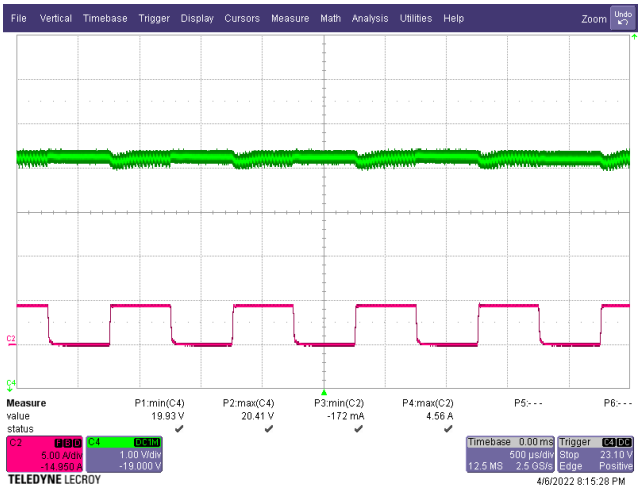


Figure 49 – Transient Response.
20 V, 0 A to 4.5 A Load.
V_{OUT} = 20.41 V Max., 19.93 V Min.
CH4: V_{OUT}, 1 V / div.
CH2: I_{OUT}, 5 A / div.
Time: 500 μs / div.

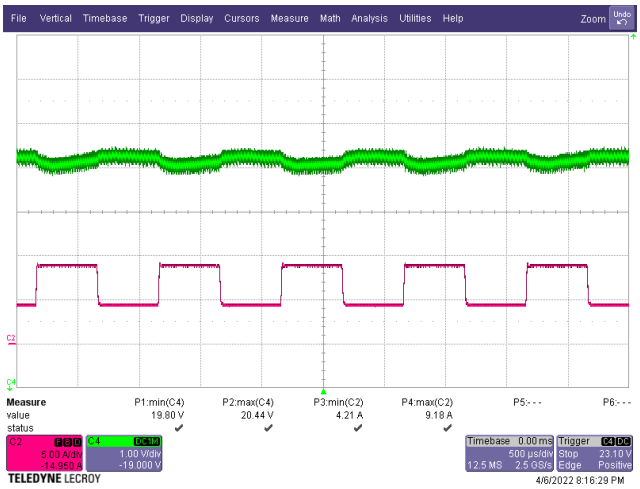


Figure 50 – Transient Response.
20.0 V, 4.5 A to 9 A Load.
V_{OUT} = 20.44 V Max., 19.80 V Min.
CH4: V_{OUT}, 1 V / div.
CH2: I_{OUT}, 5 A / div.
Time: 500 µs / div.

15.8 *Output Ripple Measurements*

15.8.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

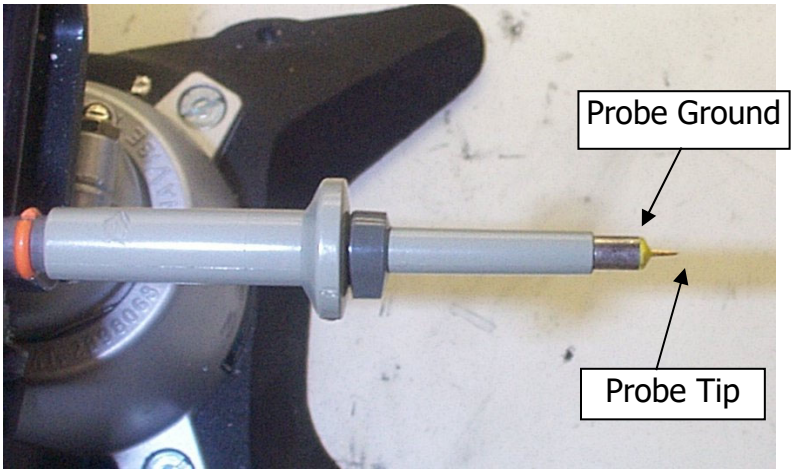


Figure 51 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

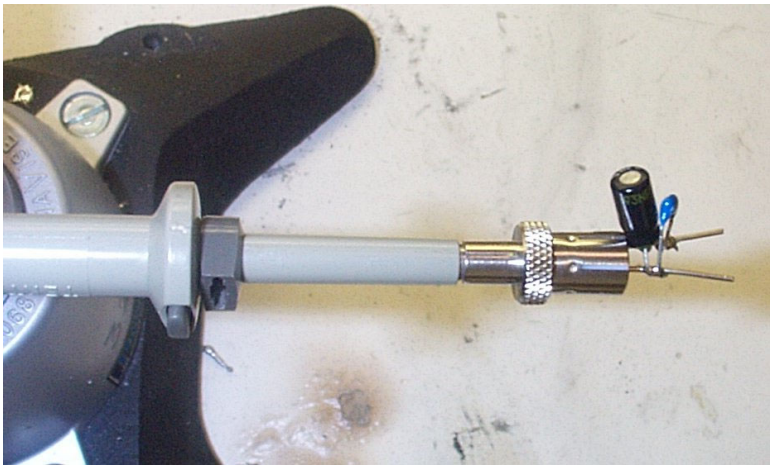


Figure 52 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

15.8.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured on the board using the ripple measurement probe with decoupling capacitors.

15.8.2.1 Output: 20 V / 9 A

Figure 53 – Output Voltage Ripple.
20 V, 9 A Load.
$V_{OUT(AC)}$ = 214 mV Peak-to-Peak.
CH4: $V_{OUT(AC)}$, 100 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom).

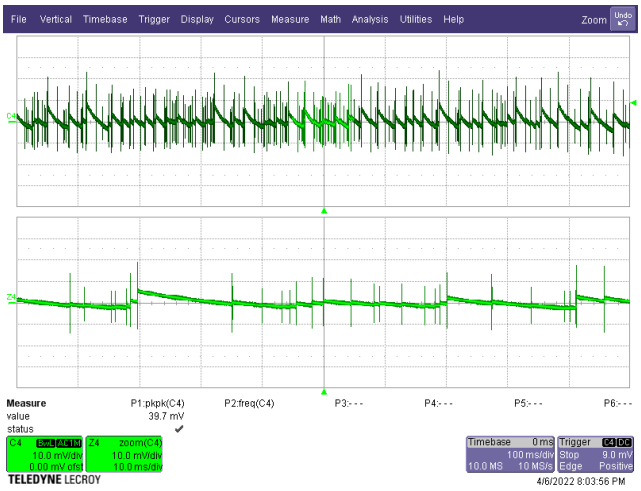


Figure 54 – Output Voltage Ripple.
20 V, 0 A Load.
$V_{OUT(AC)}$ = 39.7 mV Peak-to-Peak.
CH4: $V_{OUT(AC)}$, 50 mV / div.
Time: 100 ms / div. (10 ms / div. Zoom).

16 CV/CC Profile

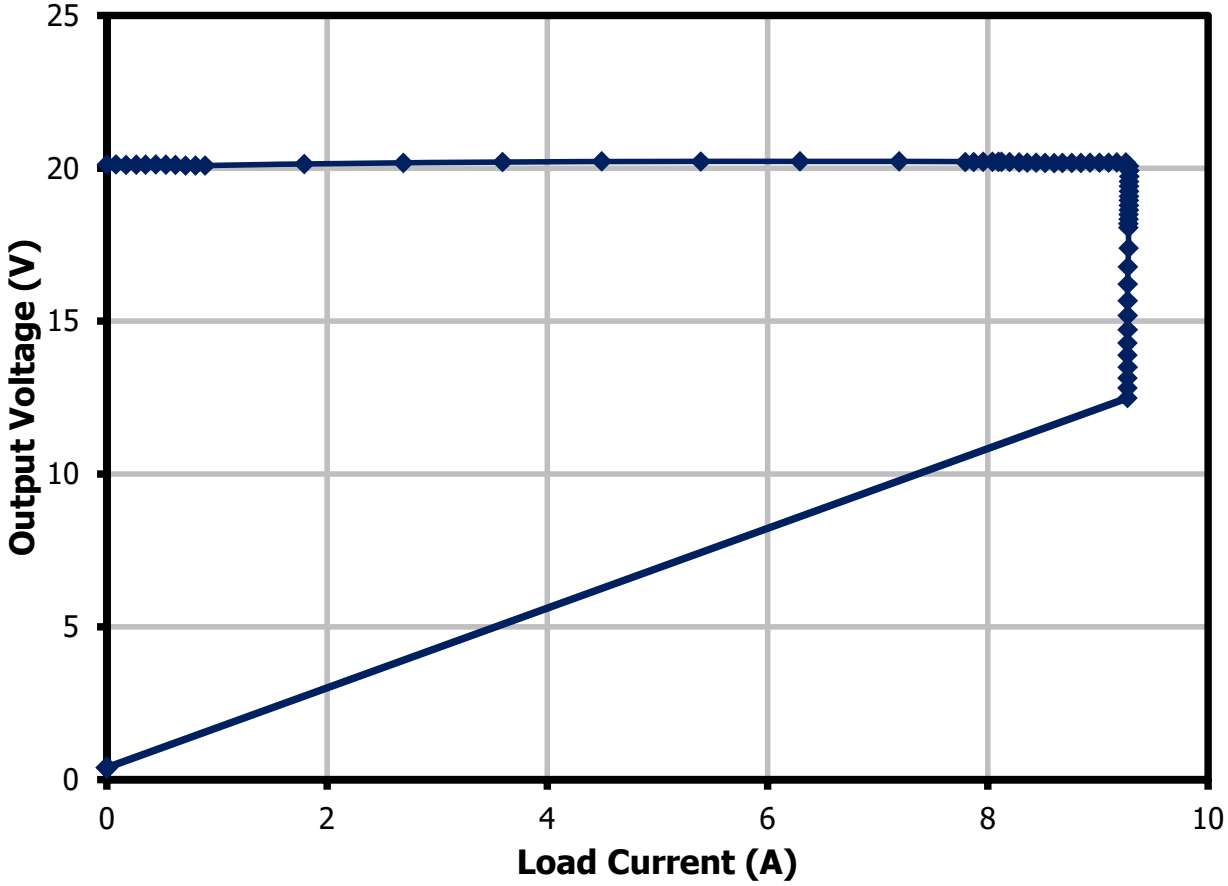
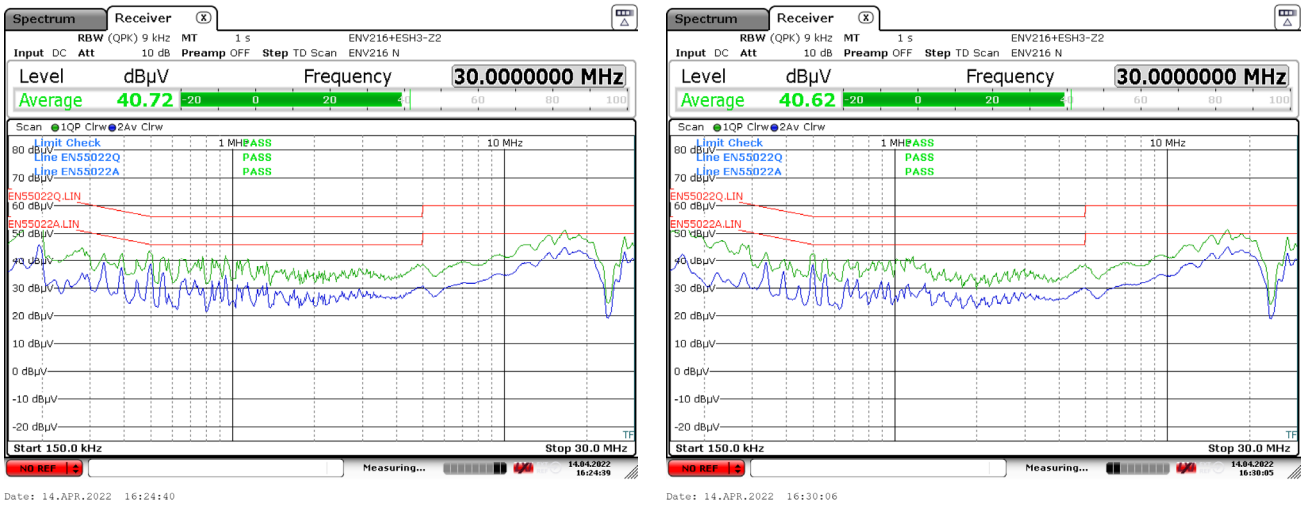


Figure 55 – Output Current vs. Output Voltage, Room Temperature.

17 Conducted EMI

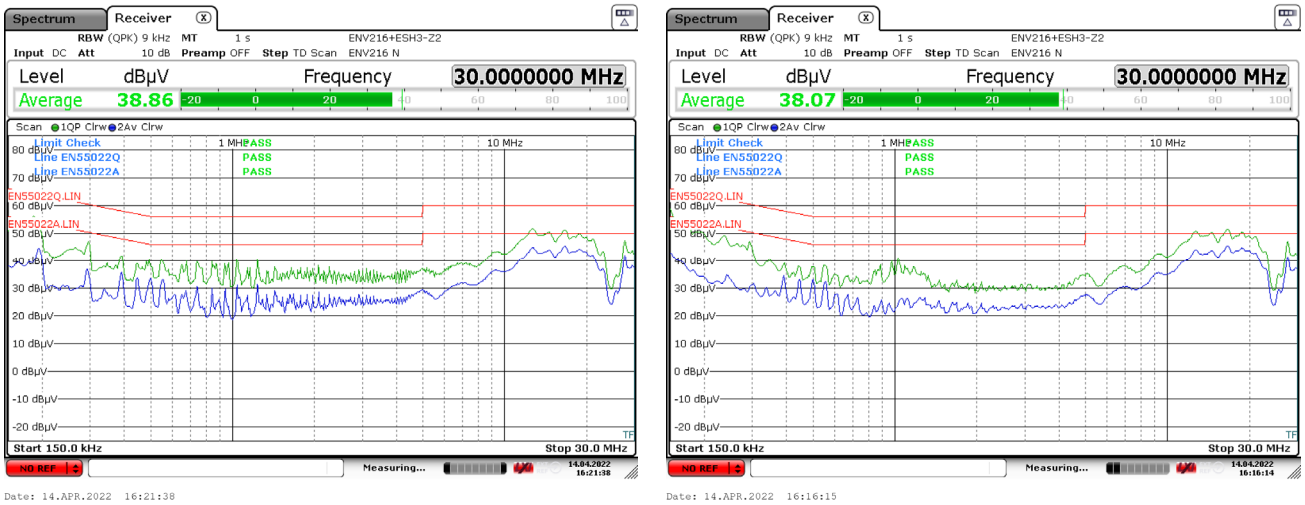
17.1 *Ground (QPK / AV)*

17.1.1 Output: 20 V / 9 A



115 VAC. 230 VAC.

Figure 56 – Ground EMI, 20 V / 9 A Load [Line Scan].



115 VAC. 230 VAC.

Figure 57 – Ground EMI, 20 V / 9 A Load [Neutral Scan].

18 Line Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

18.1 *Differential Mode Surge (L to N), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+1000	0	10	Pass
-1000	0	10	Pass
+1000	90	10	Pass
-1000	90	10	Pass
+1000	180	10	Pass
-1000	180	10	Pass
+1000	270	10	Pass
-1000	270	10	Pass

18.2 *Common Mode Surge (L to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

18.3 *Common Mode Surge (N to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

18.4 *Common Mode Surge (L, N to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

19 Electrostatic Discharge

The unit was tested with ±16.5 kV air discharge and ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- On-board +VOUT and GND

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

19.1 *Air Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+16.5	VOUT	10	Pass
-16.5	VOUT	10	Pass
+16.6	GND	10	Pass
-16.5	GND	10	Pass

19.2 *Contact Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+8.8	VOUT	10	Pass
-8.8	VOUT	10	Pass
+8.8	GND	10	Pass
-8.8	GND	10	Pass

20 Revision History

Date	Author	Revision	Description & Changes	Reviewed
01-Aug-22	SS	1.0	Initial Release.	Apps & Mktg

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